

**Invalidity of U.S. Patent No. 10,877,233 (the “’233 Patent”) in View of
Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Refiner (“TI DS110DF111”)**

TI DS110DF111 was published in June 2015. TI DS110DF111 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the ’233 Patent is responsive to Complainant’s apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents’ claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents’ understanding of the proper scope of the Asserted Claims of the ’233 Patent.

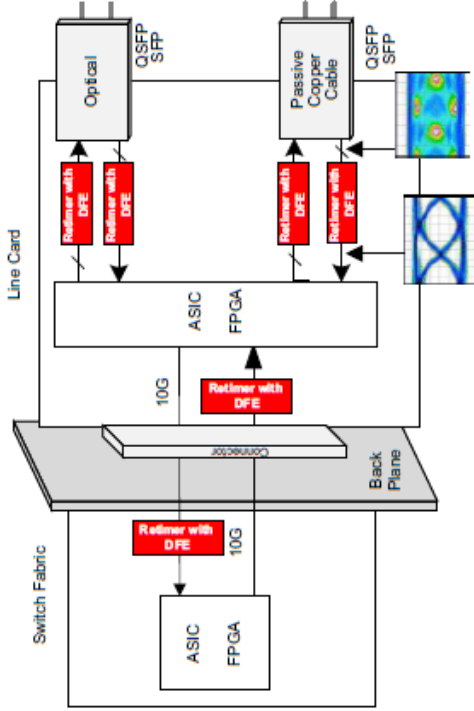
All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant’s infringement and/or domestic industry contentions, and/or information obtained during discovery as the Investigation progresses.

To the extent Complainant alleges that TI DS110DF111 does not disclose any particular limitation of the Asserted Claims of the ’233 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the ’233 Patent to modify TI DS110DF111 and/or to combine the teachings of TI DS110DF111 with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the ’233 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the ’233 Patent that it contends is not fully disclosed by TI DS110DF111, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

A. INDEPENDENT CLAIM 1

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
1[pre] A cable that comprises:	To the extent the preamble is limiting, TI DS110DF111 discloses and/or renders obvious this limitation.
3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve BER < 1x10⁻¹⁵. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data.	

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	DS110DF111, 1. 8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  Figure 9. Typical Application DS110DF111, 43.

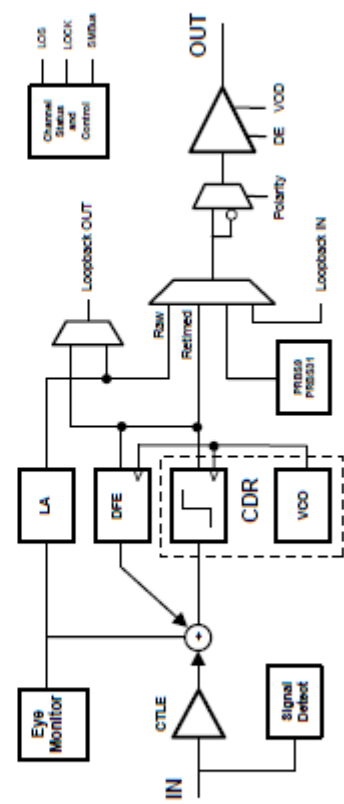
Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent transient Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The functional block diagram illustrates the internal components of the DS110DF111. An input signal (IN) enters from the bottom left and passes through a CTLE (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from a 'Signal Detect' block. This sum is then processed by a CDR (Clock and Data Recovery) block, which is part of a larger dashed box containing a VCO (Voltage-Controlled Oscillator). The CDR output is fed into a DFE (Decision Feedback Equalizer) block, followed by a LA (Limiting Amplifier) block. The LA output is monitored by an 'Eye Monitor' block. A feedback path labeled 'Loopback OUT' branches off from the LA output and is fed back into the CDR. The main signal path continues from the LA through a 'Raw' signal stage, then a 'Refined' signal stage, and finally a 'Polarity' block. The output of the polarity block is fed into an output driver (represented by a triangle) which produces the final 'OUT' signal. This output driver is also controlled by 'DE' (de-emphasis) and 'VCO' signals. A 'Channel Status and Control' block at the top right provides status signals (LOS, LOCK, STATUS) and a 'Loopback IN' signal to the 'Polarity' block. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
1[a] a first data recovery and remodulation	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. To the extent that this preamble is not disclosed, either explicitly or inherently, by TI DS110DF111, this preamble is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[a] a first data recovery and remodulation	TI DS110DF111 discloses and/or renders obvious this limitation.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
(DDR) device that exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	DS110DF111, 1. 8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table. Figure 9. Typical Application DS110DF111, 43.

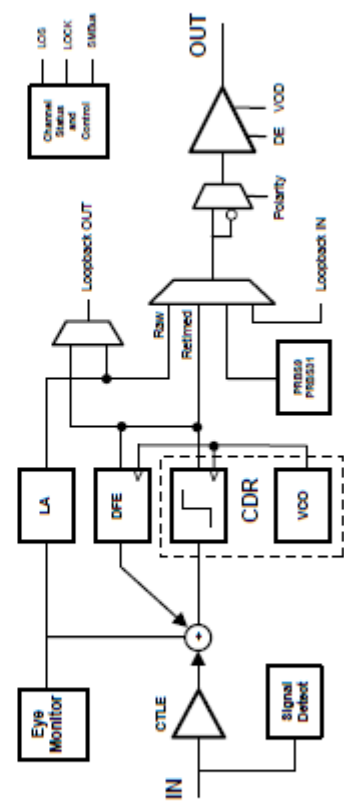
Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent transient Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The functional block diagram illustrates the internal components of the DS110DF111. An input signal (IN) enters from the bottom left, passing through a CTLE (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from a 'Signal Detect' block. This sum is then processed by a CDR (Clock and Data Recovery) block, which is part of a larger dashed box containing a VCO (Voltage-Controlled Oscillator). The CDR output is fed into a DFE (Decision Feedback Equalizer) block, followed by a LA (Limiting Amplifier) block. The LA output is connected to an 'Eye Monitor' block and also provides a 'Loopback OUT' signal. The 'Loopback OUT' signal is fed back into the CDR block. The CDR block also receives a 'Loopback IN' signal from a 'Phase FREQ' block. The output of the CDR is a 'Raw' signal, which is then processed by a 'Refined' block. The 'Refined' block's output is connected to a 'Channel Status and Control' block, which has inputs for LOS (Loss of Signal), LOCK, and STATUS. The 'Refined' signal is also connected to an output driver block, which has inputs for 'Polarity' and 'DE' (De-emphasis), and produces the final 'OUT' signal. A 'Signal Detect' block is also connected to the output driver. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaptation algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaptation Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
1[b] a second DRR device that exchanges inbound and outbound multi-lane data	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7. Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
	TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
streams with a second host interface port via a second end connector plug; and	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”) 8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table. Switch Fabric Line Card Back Plane ASIC FPGA Retimer with DFE 10G Retimer with DFE 10G ASIC FPGA Optical Retimer with DFE Retimer with DFE QSF SFP Passive Copper Cable Retimer with DFE Retimer with DFE QSF SFP Figure 9. Typical Application DS110DF111, 43.
---------	--

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7. Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[c] electrical conductors connecting the first and second DRR devices to convey	TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
electrical transit signals therebetween,	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table. Figure 9. Typical Application DS110DF111, 43.

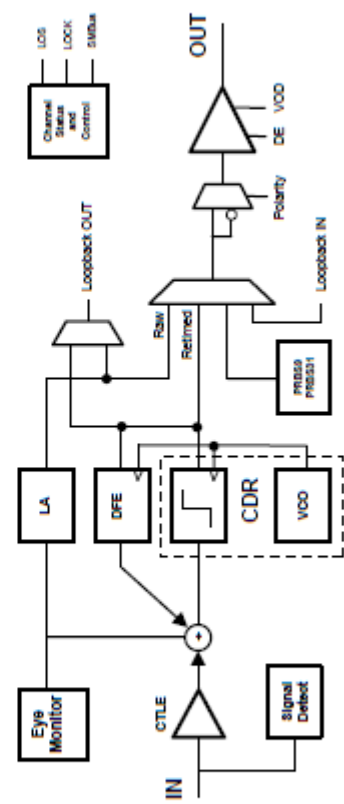
Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent transient Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram illustrates the data path of the DS110DF111. It starts with an 'IN' signal entering a 'CTLE' (Continuous Time Linear Equalizer) block. The output of the CTLE goes to a summing junction. A 'Signal Detect' block also feeds into this junction. The output of the summing junction goes to a 'CDR' (Clock and Data Recovery) block, which is part of a dashed box containing a 'VCO' (Voltage-Controlled Oscillator). The CDR block outputs a 'Refined' signal to a 'DFE' (Decision Feedback Equalizer) block. The DFE block outputs to a 'LA' (Line Attenuator) block. The LA block outputs to a 'Loopback OUT' block. The Loopback OUT block feeds back into the summing junction. The output of the LA block also goes to a 'Channel Status and Control' block, which has inputs for 'LOS' (Loss of Signal), 'LOCK', and 'STATUS'. The output of the LA block goes to an 'OUT' block, which has inputs for 'DE' (De-emphasis) and 'VCO'. The OUT block also feeds back into the summing junction via a 'Loopback IN' block. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[d] the first DRR device converting between said electrical transit signals and said inbound and outbound multilane data streams for the first host interface port, and	TI DS110DF111 discloses and/or renders obvious this limitation.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”) 8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table. Switch Fabric Line Card Back Plane ASIC FPGA Retimer with DFE 10G Retimer with DFE 10G ASIC FPGA Optical Retimer with DFE Retimer with DFE QSF SFP Passive Copper Cable Retimer with DFE Retimer with DFE QSF SFP Figure 9. Typical Application DS110DF111, 43.
---------	--

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.

Exhibit A-4

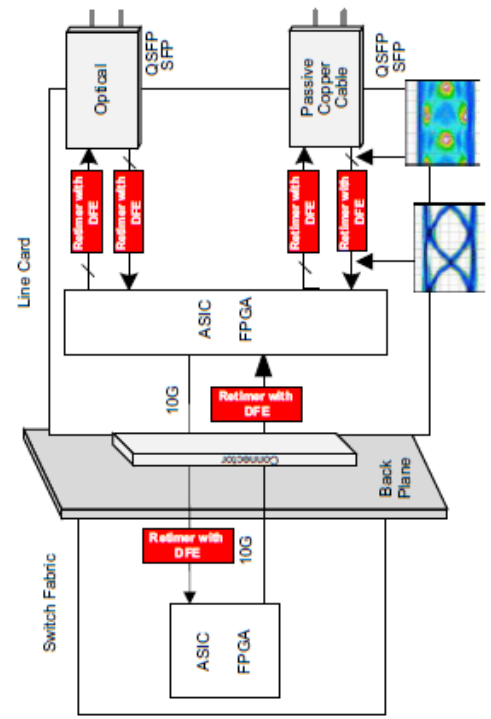
Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7. Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[e] the second DRR device converting between said electrical transit signals and said	TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
inbound and outbound multilane data streams for the second host interface port,	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  Figure 9. Typical Application DS110DF111, 43.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.1 Input Channel Equalization Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium. To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
1[f] the first and second DRR devices providing preequalization	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7. Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
	TI DS110DF111 discloses and/or renders obvious this limitation.

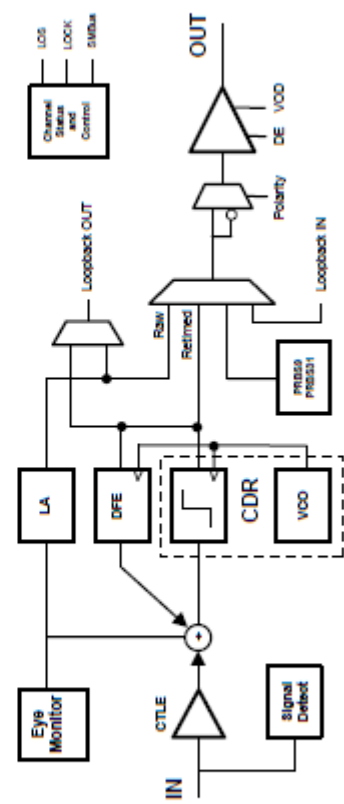
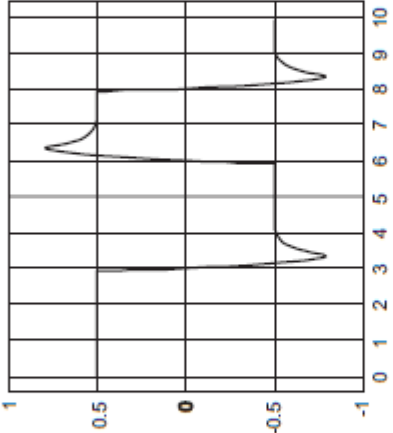
Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent transient Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram illustrates the functional blocks of the DS110DF111. An input signal (IN) enters from the bottom left, passing through a CTLE (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from a 'Signal Detect' block. This sum is then processed by a CDR (Clock and Data Recovery) block, which is part of a larger dashed box containing a VCO (Voltage-Controlled Oscillator) and a PLL (Phase-Locked Loop). The CDR output is fed into a DFE (Decision Feedback Equalizer) block, followed by a LA (Limiting Amplifier) block. The LA output is connected to an 'Eye Monitor' block and also provides a 'Loopback OUT' signal. The 'Loopback OUT' signal is fed back into the CDR block. The CDR block also receives a 'Loopback IN' signal from a 'Phase FREQ' block. The output of the CDR is a 'Raw' signal, which is then processed by a 'Refined' block. The 'Refined' block output is connected to a 'Channel Status and Control' block, which provides 'LOS' (Loss of Signal), 'LOCK', and 'STATUS' signals. The 'Refined' signal is also connected to an output driver block, which provides a 'Polarity' signal and a 'DE' (De-emphasis) signal. The final output (OUT) is connected to a 'VCO' block. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10.

Exhibit A-4

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Claim 1	Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)
	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.

Claim 1

Texas Instruments – DS110DF111 Low-Power, Multirate, 2-Channel Retimer (“DS110DF111”)

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

B. DEPENDENT CLAIM 2

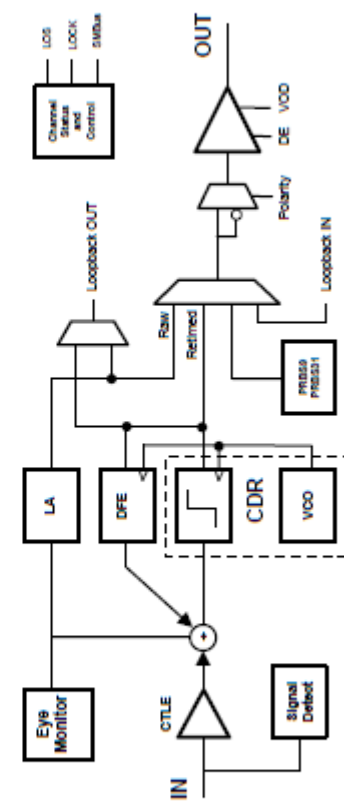
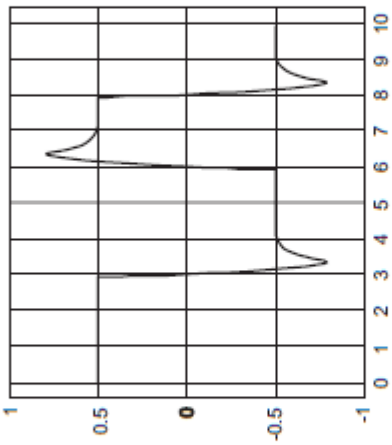
Claim 2 2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.	TI DS110DF111 discloses and/or renders obvious this limitation. 7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram illustrates the data path of the DS110DF111. It starts with an 'IN' signal entering a 'CTLE' (Continuous Time Linear Equalizer) block. The output of the CTLE goes to a summing junction (+). A 'Signal Delay' block also feeds into this junction. The output of the summing junction goes to an 'Eye Monitor' block. The Eye Monitor's output goes to a 'LA' (Linear Amplifier) block. The LA's output goes to a 'DFE' (Decision Feedback Equalizer) block. The DFE's output goes to a 'Raw' signal path. The Raw signal path goes to a 'Refined' signal path. The Refined signal path goes to a 'Loopback IN' block. The Loopback IN block's output goes to a 'Loopback OUT' block. The Loopback OUT block's output goes to a 'Channel Status and Control' block. The Channel Status and Control block has outputs for 'LOS' (Loss of Signal), 'LOCK', and 'STATUS'. The Refined signal path also goes to a 'CDR' (Clock and Data Recovery) block. The CDR block's output goes to a 'VCO' (Voltage-Controlled Oscillator) block. The VCO block's output goes to a 'Polarity' block. The Polarity block's output goes to a 'DE' (De-emphasis) block. The DE block's output goes to an 'OUT' block. The OUT block has a 'VCO' input. The OUT block's output goes to a 'Loopback IN' block. The Loopback IN block's output goes to a 'Loopback OUT' block. The Loopback OUT block's output goes to a 'Channel Status and Control' block. The Channel Status and Control block has outputs for 'LOS', 'LOCK', and 'STATUS'. Figure 6. DS110DF111 Data Path Block Diagram
---	---

Exhibit A-4

Claim 2	
	DS110DF111, 10. 7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Claim 2	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
---------	---

Claim 2

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

C. DEPENDENT CLAIM 3

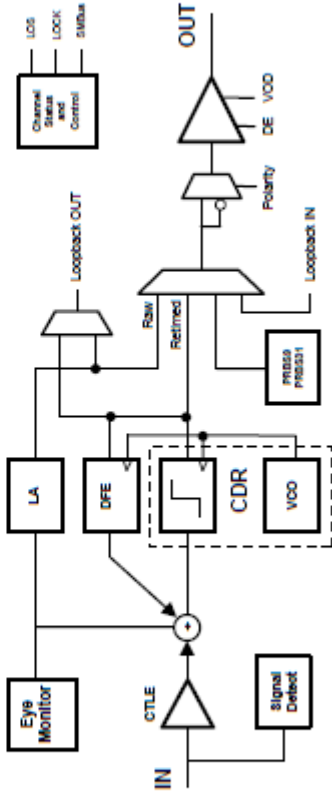
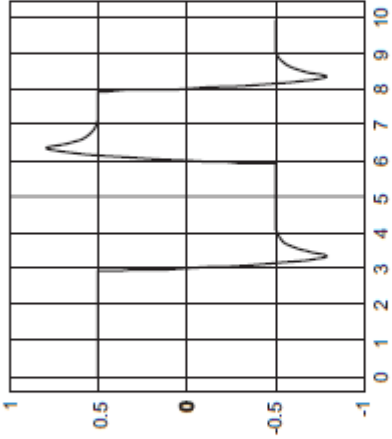
Claim 3 3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.	TI DS110DF111 discloses and/or renders obvious this limitation. 7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram shows the internal components of the DS110DF111. An 'IN' signal enters from the left, passing through a 'Signal Detect' block. It then goes through a 'CTLE' (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from a 'Loopback IN' block. This sum is then processed by a 'CDR' (Clock and Data Recovery) block, which is also connected to a 'VCO' (Voltage-Controlled Oscillator). The CDR output goes through a 'DFE' (Decision Feedback Equalizer) block. The output of the DFE is then processed by a 'LA' (Line Attenuator) block. The output of the LA is connected to an 'Eye Monitor' block and a 'Loopback OUT' block. The 'Loopback OUT' block is connected to a 'Channel Status and Control' block, which has inputs for 'LOS' (Loss of Signal), 'LOCK', and 'STATUS'. The output of the LA is also connected to a 'Polarity' block, which is connected to a 'DE' (De-emphasis) block. The output of the DE block is connected to an 'OUT' block, which is also connected to a 'VCO' block. The 'OUT' block is connected to a 'Loopback IN' block, which provides feedback to the CDR. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10.
---	---

Exhibit A-4

Claim 3	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

Claim 3	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.
	 Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.

Claim 3

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

D. DEPENDENT CLAIM 4

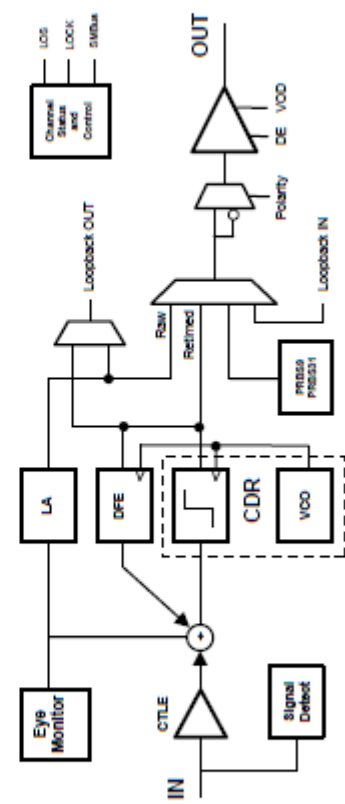
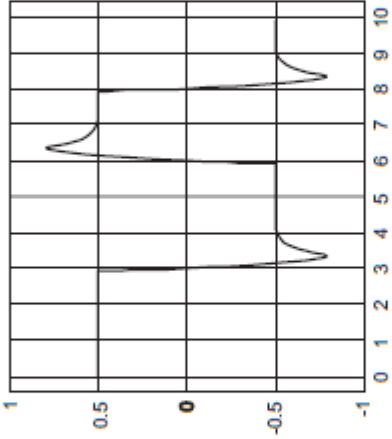
Claim 4 4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.	TI DS110DF111 discloses and/or renders obvious this limitation. 7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram shows the internal components of the DS110DF111. An 'IN' signal enters from the left, passing through a 'Signal Detect' block. It then goes through a 'CTLE' (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from a 'Loopback IN' block. This sum is then processed by a 'CDR' (Clock and Data Recovery) block, which is also connected to a 'VCO' (Voltage-Controlled Oscillator). The CDR output goes through a 'DFE' (Decision Feedback Equalizer) block. The output of the DFE is then processed by a 'LA' (Line Attenuator) block. The LA output is connected to an 'Eye Monitor' block and a 'Loopback OUT' block. The 'Loopback OUT' block is connected to a 'Channel Status and Control' block, which has inputs for 'LOS' (Loss of Signal), 'LOCK', and 'STATUS'. The 'Channel Status and Control' block also outputs 'DE' (De-emphasis) and 'VCO' signals. The final output is 'OUT'. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10.
---	---

Exhibit A-4

Claim 4	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
----------------	---

Exhibit A-4

Claim 4	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.
	 Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.

Claim 4

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

E. DEPENDENT CLAIM 5

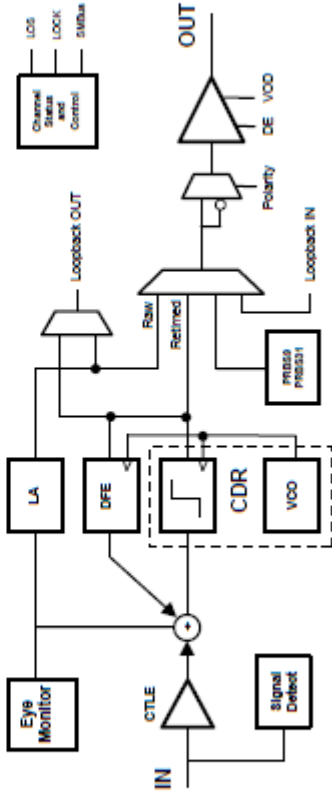
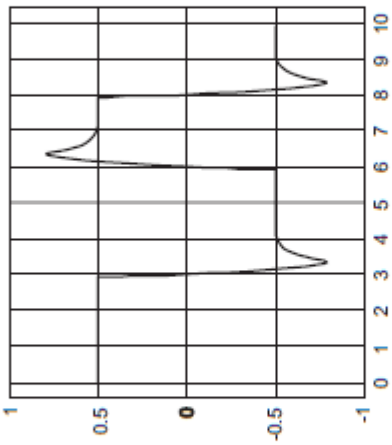
Claim 5 5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.	TI DS110DF111 discloses and/or renders obvious this limitation. 7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram shows the internal components of the DS110DF111. An 'IN' signal enters from the left, passing through a 'Signal Detect' block. It then goes through a 'CTLE' (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from a 'Loopback IN' block. This sum is then processed by a 'CDR' (Clock and Data Recovery) block, which is also connected to a 'VCO' (Voltage-Controlled Oscillator). The CDR output goes through a 'DFE' (Differential Feedback Equalizer) block. The output of the DFE is summed with a feedback signal from a 'Loopback OUT' block. This sum is then processed by a 'LA' (Line Attenuator) block. The output of the LA is connected to an 'Eye Monitor' block. The Eye Monitor output is connected to a 'Channel Status and Control' block, which has inputs for 'LOS' (Loss of Signal), 'LOCK', and 'STATUS'. The output of the LA is also connected to a 'Polarity' block, which is connected to a 'DE' (Differential Emphasis) block. The DE block is connected to the 'OUT' signal. The DE block also has a 'VCO' input. The 'OUT' signal is connected to a 'Loopback OUT' block, which feeds back into the 'Loopback IN' and 'Loopback OUT' blocks. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10.
--	---

Exhibit A-4

Claim 5	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
----------------	---

Exhibit A-4

Claim 5	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
---------	--

Claim 5

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

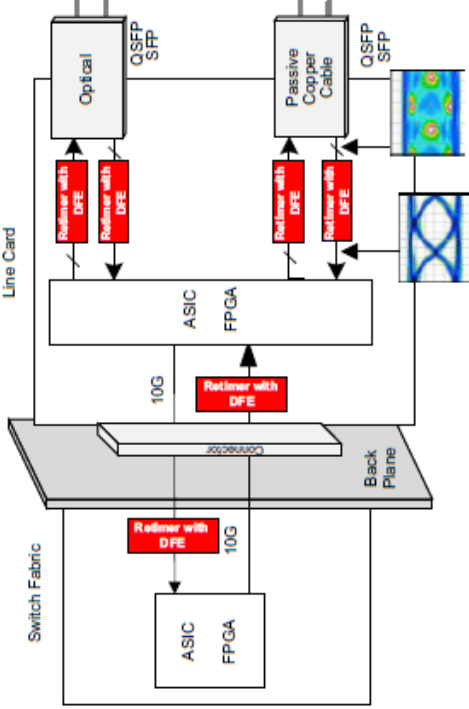
Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

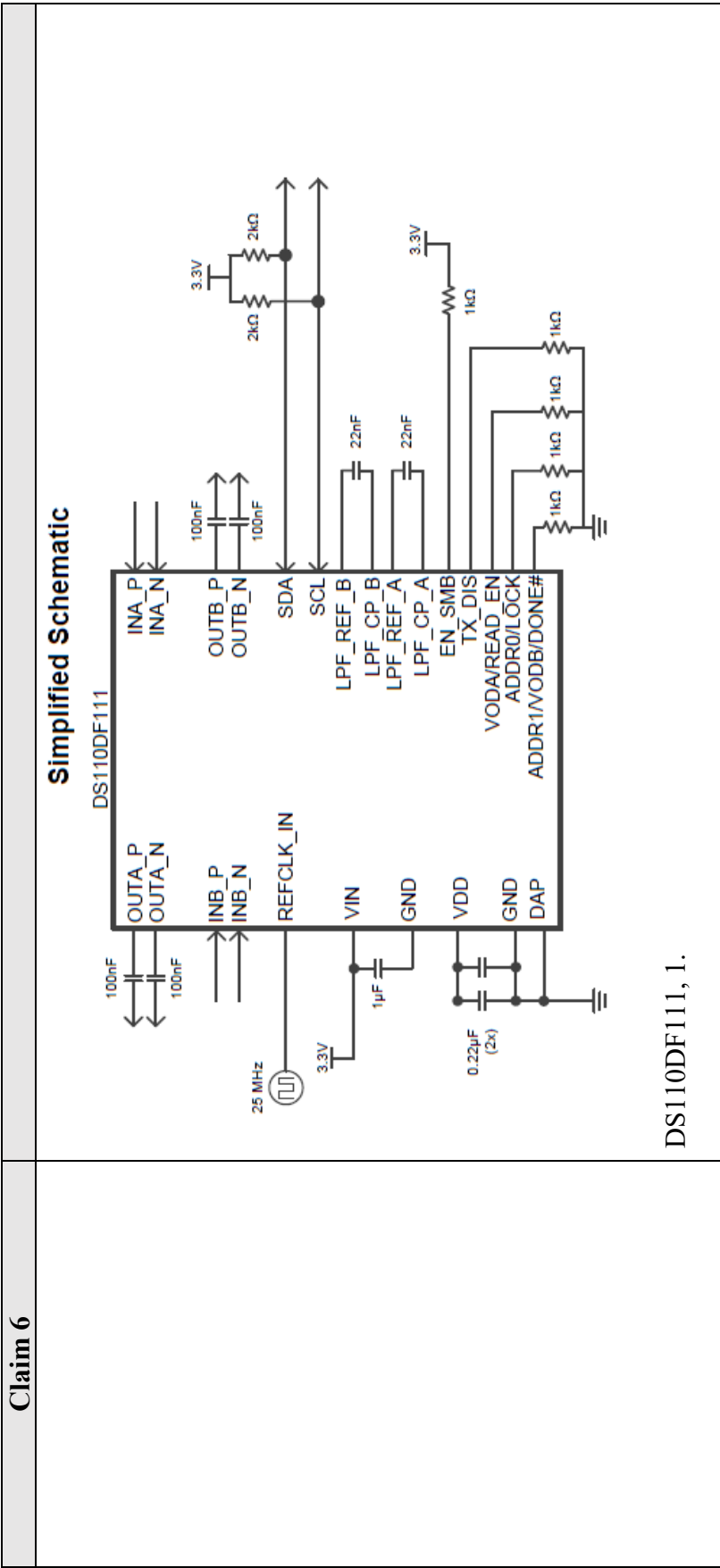
To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

F. DEPENDENT CLAIM 6

Claim 6 6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.	TI DS110DF111 discloses and/or renders obvious this limitation. 8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  Figure 9. Typical Application DS110DF111, 43.
--	--

Claim 6	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram Figure 6. DS110DF111 Data Path Block Diagram
-----------------------	--

DS110DF111, 10.



Claim 6	
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.

Exhibit A-4

Claim 6	
	To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

G. DEPENDENT CLAIM 7

Claim 7	
7. The cable of claim 1, wherein the first and second DDR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 7

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

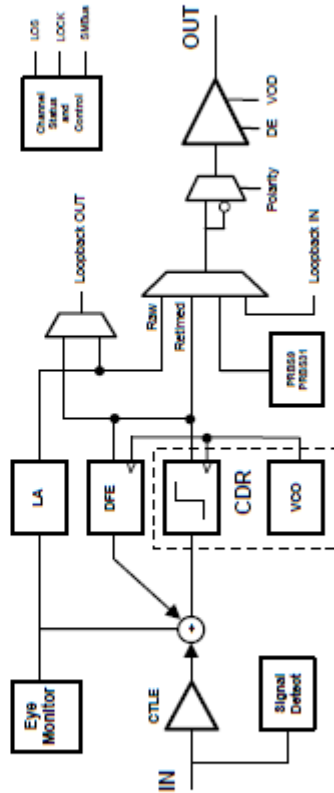


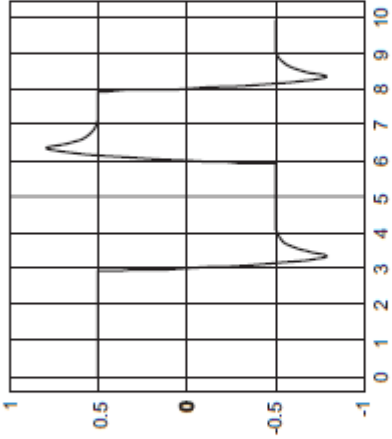
Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 7	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

Claim 7																									
	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7. <table border="1"><caption>Data points for Figure 7</caption><thead><tr><th>Time (x)</th><th>Amplitude (y)</th></tr></thead><tbody><tr><td>0</td><td>-0.5</td></tr><tr><td>1</td><td>0.7</td></tr><tr><td>2</td><td>-0.5</td></tr><tr><td>3</td><td>0.7</td></tr><tr><td>4</td><td>-0.5</td></tr><tr><td>5</td><td>0.7</td></tr><tr><td>6</td><td>-0.5</td></tr><tr><td>7</td><td>0.7</td></tr><tr><td>8</td><td>-0.5</td></tr><tr><td>9</td><td>0.7</td></tr><tr><td>10</td><td>-0.5</td></tr></tbody></table> Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.	Time (x)	Amplitude (y)	0	-0.5	1	0.7	2	-0.5	3	0.7	4	-0.5	5	0.7	6	-0.5	7	0.7	8	-0.5	9	0.7	10	-0.5
Time (x)	Amplitude (y)																								
0	-0.5																								
1	0.7																								
2	-0.5																								
3	0.7																								
4	-0.5																								
5	0.7																								
6	-0.5																								
7	0.7																								
8	-0.5																								
9	0.7																								
10	-0.5																								

Claim 7

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

H. INDEPENDENT CLAIM 8

Claim 8	
8[pre] A cable manufacturing method that comprises:	To the extent the preamble is limiting, TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 8	
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.

Claim 8	Switch Fabric Retimer with DFE ASIC FPGA 10G Retimer with DFE 10G Back Plane Line Card Retimer with DFE Retimer with DFE Optical QSFPP SFP Retimer with DFE Retimer with DFE Passive Copper Cable QSFPP SFP Figure 9. Typical Application DS110DF111, 43.
---------	---

8.1 Application Information
The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

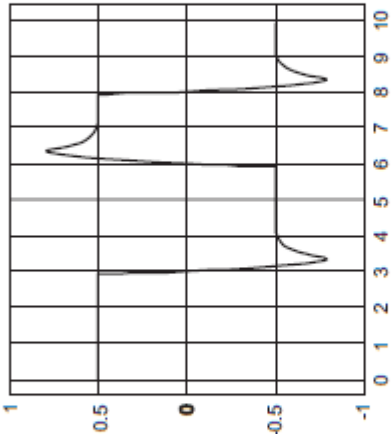
8.2 Typical Application
Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

Exhibit A-4

Claim 8	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
---------	---

Exhibit A-4

Claim 8	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Claim 8	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this preamble is not disclosed, either explicitly or inherently, by TI DS110DF111, this preamble is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading. TI DS110DF111 discloses and/or renders obvious this limitation.
8[a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges	

Claim 8 multi-lane data streams with a first host interface port via the first connector plug;	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.
---	--

Claim 8	Switch Fabric Retimer with DFE ASIC FPGA 10G Retimer with DFE 10G Back Plane Line Card Retimer with DFE Retimer with DFE Optical QSFPP SFP Retimer with DFE Retimer with DFE Passive Copper Cable QSFPP SFP Figure 9. Typical Application DS110DF111, 43.
---------	---

8.1 Application Information
The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application
Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

Claim 8

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

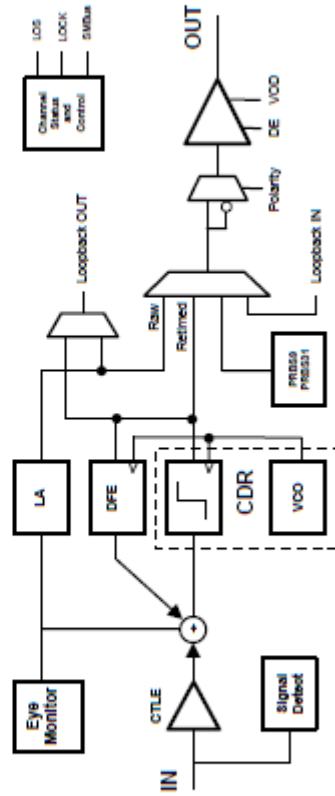


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

7.3.1.1 Input Channel Equalization

Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium.

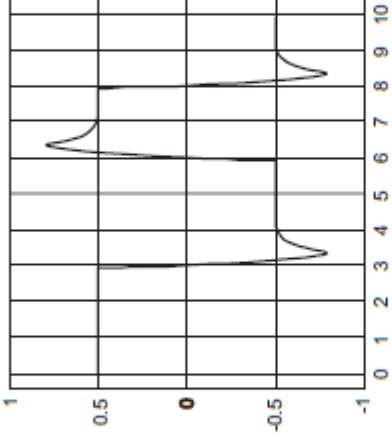
Exhibit A-4

Claim 8	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
---------	---

Exhibit A-4

Claim 8	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
----------------	---

Exhibit A-4

Claim 8	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[b] connecting a second connector plug to a second DRR device that exchanges	TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 8 multi-lane data streams with a second host interface port via the second connector plug;	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported subrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.
---	--

Claim 8	8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table. Figure 9. Typical Application DS110DF111, 43.
----------------	---

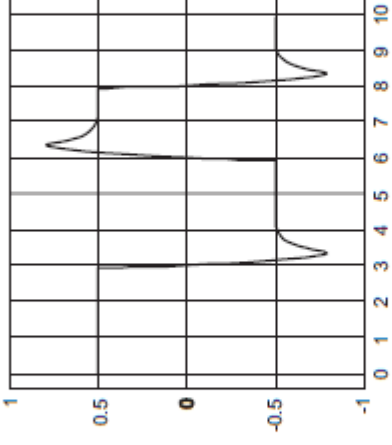
Exhibit A-4

Claim 8	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
---------	---

Exhibit A-4

Claim 8	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
----------------	---

Exhibit A-4

Claim 8	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading. TI DS110DF111 discloses and/or renders obvious this limitation.
8[c] connecting electrical conductors to the first and second DRR devices to convey electrical transit signals	

therebetween,	<table><tr><td data-bbox="228 161 267 1451"> Claim 8 </td><td data-bbox="228 1451 1099 1904"> therebetween, </td></tr><tr><td data-bbox="228 1110 267 1451"> 8.1 Application Information </td><td data-bbox="228 1110 1099 1451"> The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. </td></tr><tr><td data-bbox="228 1060 267 1110"> 8.2 Typical Application </td><td data-bbox="228 1060 1099 1110"> Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table. </td></tr><tr><td data-bbox="228 1010 267 1060"> Figure 9 </td><td data-bbox="228 1010 1099 1060"> Typical Application </td></tr><tr><td data-bbox="228 959 267 1010"> DS110DF111, 43. </td><td data-bbox="228 959 1099 1010"> DS110DF111, 43. </td></tr></table>	Claim 8	therebetween,	8.1 Application Information	The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.	8.2 Typical Application	Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.	Figure 9	Typical Application	DS110DF111, 43.	DS110DF111, 43.
Claim 8	therebetween,										
8.1 Application Information	The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.										
8.2 Typical Application	Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.										
Figure 9	Typical Application										
DS110DF111, 43.	DS110DF111, 43.										

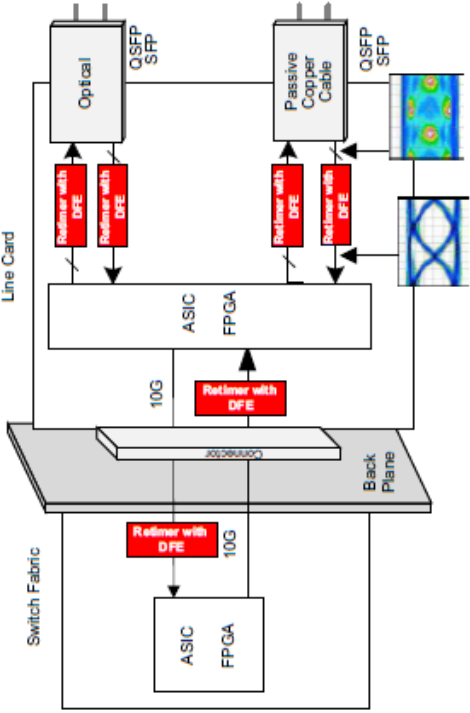


Figure 9. Typical Application

DS110DF111, 43.

Claim 8	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the
-----------------------	--

Exhibit A-4

Claim 8	
8[d] the first DRR device converting between said electrical transit signals and said multi-lane data streams for the first host interface port, and	knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading. TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 8	
	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.

Claim 8	Switch Fabric Retimer with DFE ASIC FPGA 10G Retimer with DFE ASIC FPGA 10G Back Plane Line Card Retimer with DFE Retimer with DFE Optical QSFP SFP Retimer with DFE Retimer with DFE Passive Copper Cable QSFP SFP Figure 9. Typical Application DS110DF111, 43.
---------	---

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

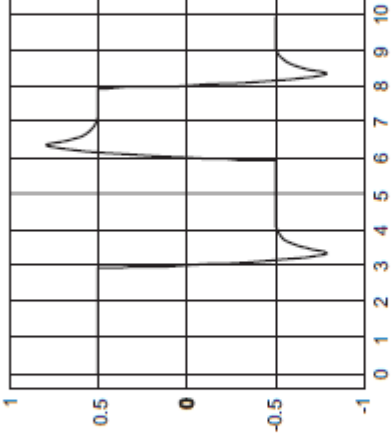
8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

Claim 8	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
-----------------------	---

Claim 8	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
-----------------------	---

Exhibit A-4

Claim 8	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading. TI DS110DF111 discloses and/or renders obvious this limitation.
8[e] the second DRR device converting between said electrical transit signals and said multi-lane data streams	

Claim 8 for the second host interface port,	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.
--	--

Exhibit A-4

Claim 8

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

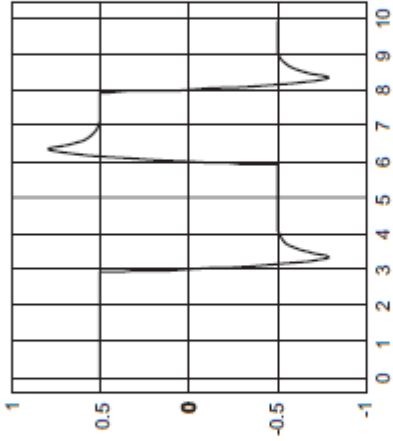
Figure 9. Typical Application

Claim 8	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
-----------------------	---

Exhibit A-4

Claim 8	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

Claim 8	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[f] the first and second DRR devices providing preequalization of the electrical	TI DS110DF111 discloses and/or renders obvious this limitation.

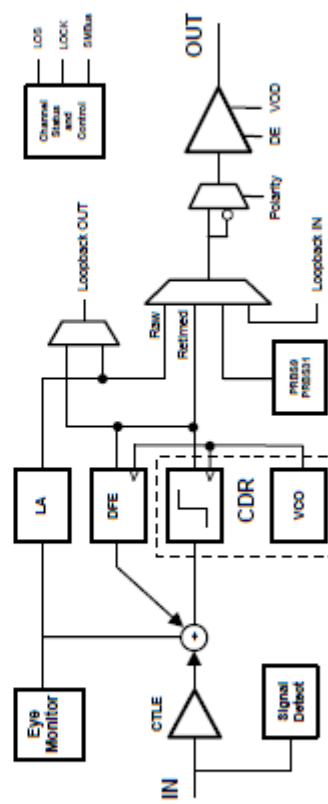
Claim 8 transit signals using transmit filter coefficient values stored in nonvolatile memories.	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram illustrates the functional blocks of the DS110DF111. An 'Eye Monitor' block receives the 'IN' signal and provides feedback to the 'LA' (Linear Amplifier) block. The 'IN' signal also passes through a 'CTLE' (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from the 'LA' block. This summed signal then passes through a 'DFE' (Decision Feedback Equalizer) block. The output of the DFE is fed into the 'CDR' (Clock and Data Recovery) block, which is part of a dashed box containing a 'VCO' (Voltage-Controlled Oscillator). The CDR block outputs a 'Retimed' signal. This 'Retimed' signal is then processed by a 'Polarity' block, which also receives a 'Loopback IN' signal. The output of the Polarity block is fed into an 'OUT' block, which also receives a 'DE' (De-emphasis) signal and a 'VCO' signal. A 'Channel Status and Control' block is shown at the top, with inputs for 'LOS' (Loss of Signal), 'LOCK', and 'STATUS'. A 'Signal Detect' block is also present, receiving the 'IN' signal and providing feedback to the 'LA' block. Figure 6. DS110DF111 Data Path Block Diagram DS110DF111, 10.
---	---

Exhibit A-4

Claim 8	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Exhibit A-4

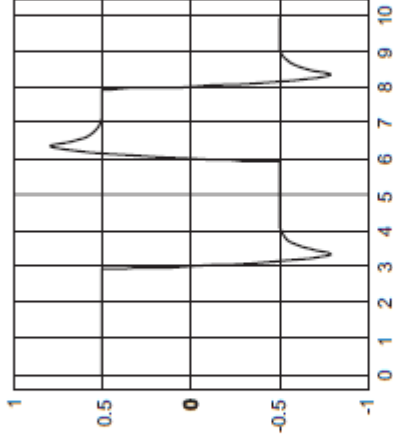
Claim 8	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
---------	---

Exhibit A-4

Claim 8

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

I. DEPENDENT CLAIM 9

Claim 9

9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.

TI DSI10DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

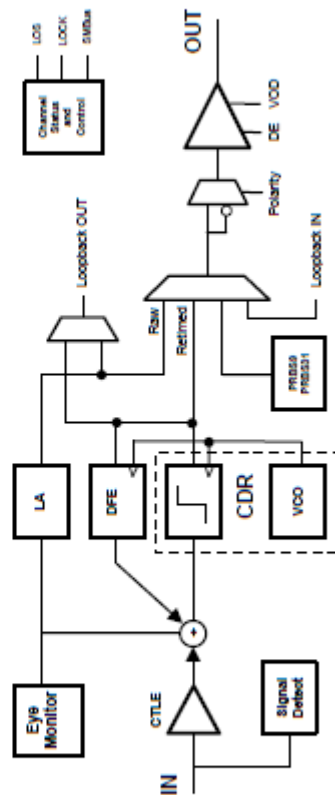
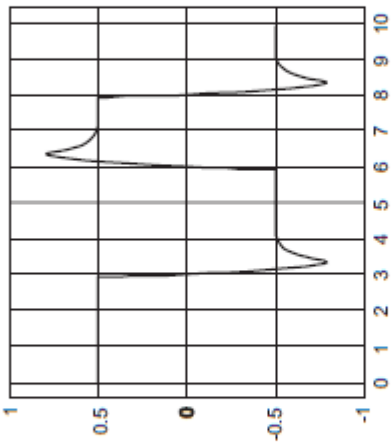


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 9	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Claim 9	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
---------	--

Claim 9

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

J. DEPENDENT CLAIM 10

Claim 10
10. The method of claim 8, further comprising:
programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

Claim 10

TI DS110DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

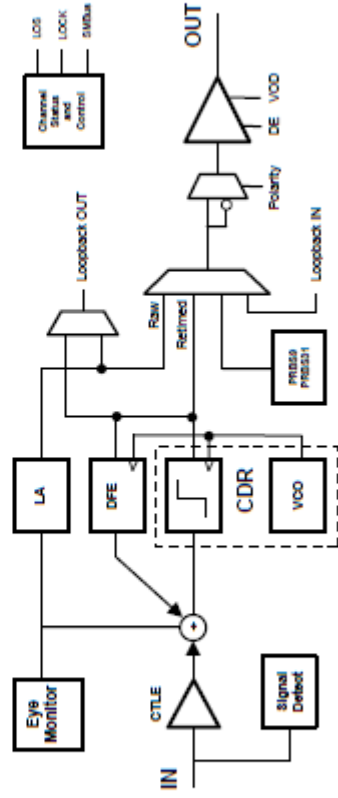


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 10	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Claim 10	
	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7. The graph shows a waveform on a grid. The horizontal axis is labeled from 0 to 10 in increments of 1. The vertical axis is labeled from -1 to 1 in increments of 0.5. The waveform starts at 0, rises to a peak of approximately 0.8 at x=6.5, then falls to a minimum of approximately -0.8 at x=3.5, and finally rises back to 0 at x=10. The peak is labeled '1' and the minimum is labeled '-1'. Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.

Claim 10

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

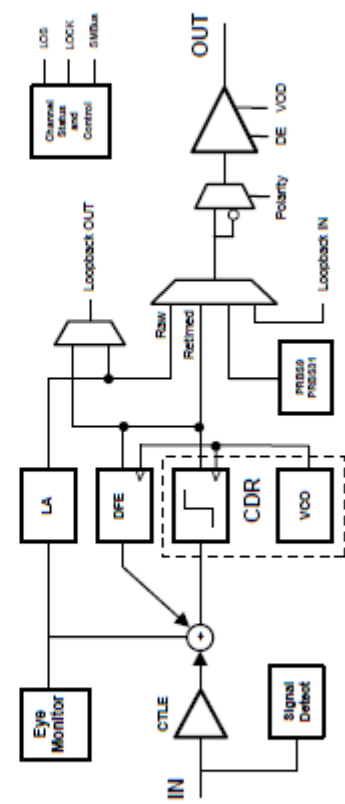
Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

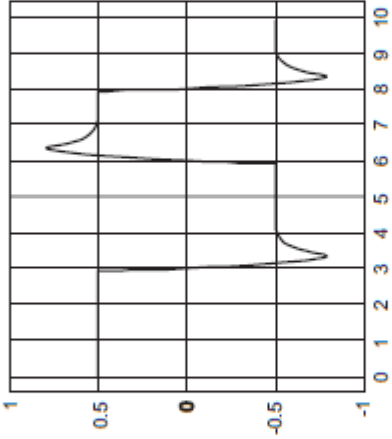
K. DEPENDENT CLAIM 11

Claim 11 11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.	TI DS110DF111 discloses and/or renders obvious this limitation. 7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram illustrates the functional blocks of the DS110DF111. An input signal (IN) enters from the bottom left. It passes through a CTLE (Continuous Time Linear Equalizer) block. The output of the CTLE is summed with a feedback signal from a Signal Detect block. The result is then processed by a LA (Linear Amplifier) block. The output of the LA is fed into a DFE (Decision Feedback Equalizer) block. The output of the DFE is fed into a CDR (Clock and Data Recovery) block. The CDR block is also connected to a VCO (Voltage-Controlled Oscillator) block. The output of the CDR is fed into a PLL (Phase-Locked Loop) block. The output of the PLL is fed into a Polarity block. The output of the Polarity block is fed into an output driver block. The output driver block has two outputs: OUT and DE (Differential Enable). The output driver block is also connected to a Channel Status and Control block. The Channel Status and Control block has three inputs: LOS (Loss of Signal), LOCK, and STATUS. The output of the Channel Status and Control block is fed into the output driver block. The output driver block is also connected to a Feedback block. The Feedback block has two inputs: Loopback IN and Loopback OUT. The output of the Feedback block is fed into the output driver block. Figure 6. DS110DF111 Data Path Block Diagram
--	---

DS110DF111, 10.

Claim 11	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
----------	--

Exhibit A-4

Claim 11	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	--

Claim 11

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

L. DEPENDENT CLAIM 12

Claim 12
12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

TI DS110DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

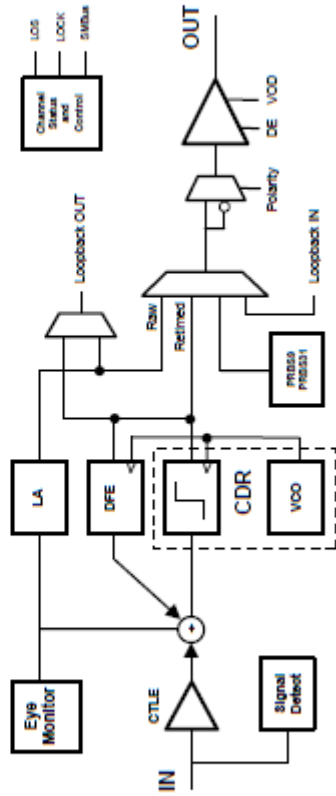
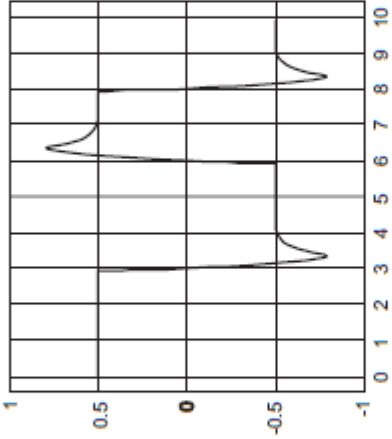


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 12	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
-----------------	---

Claim 12	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	---

Claim 12

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

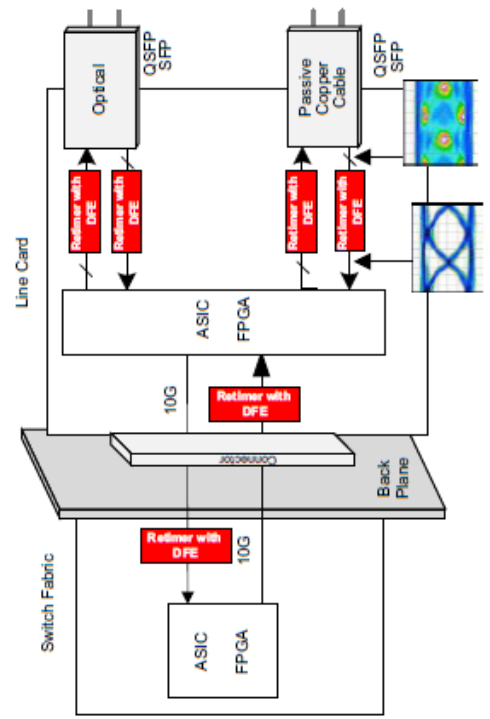
DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

M. DEPENDENT CLAIM 13

Claim 13	13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.
Claim 13	TI DS110DF111 discloses and/or renders obvious this limitation. 8.1 Application Information The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces. 8.2 Typical Application Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.  Figure 9. Typical Application DS110DF111, 43.

Claim 13

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

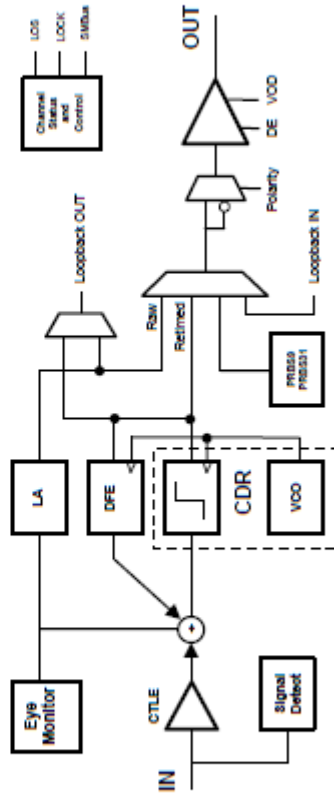


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Claim 13



Claim 13	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI
----------	---

Exhibit A-4

Claim 13	DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
-----------------	---

N. DEPENDENT CLAIM 14

Claim 14	TI DS110DF111 discloses and/or renders obvious this limitation.
14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	

Claim 14

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

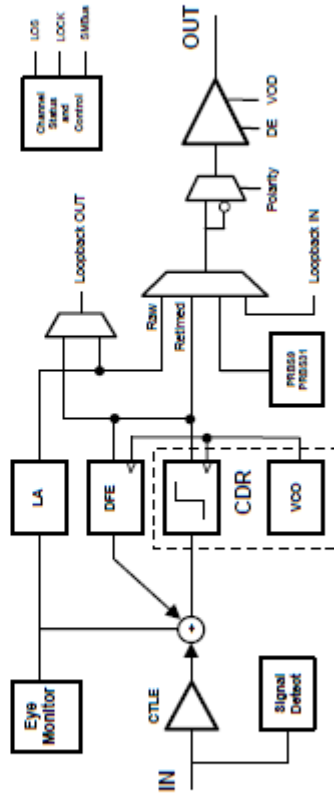
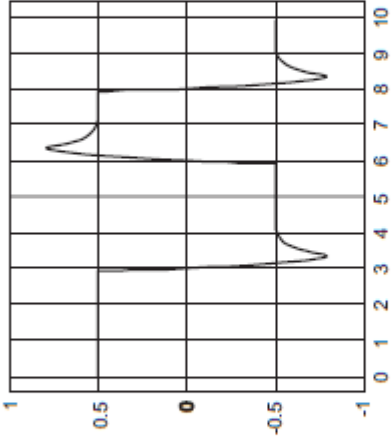


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 14	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
-----------------	---

Claim 14	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	---

Claim 14

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

O. INDEPENDENT CLAIM 15

Claim 15	
15[pre] A communications method that comprises:	To the extent the preamble is limiting, TI DS110DF111 discloses and/or renders obvious this limitation.

Claim 15	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.
----------	--

Claim 15

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

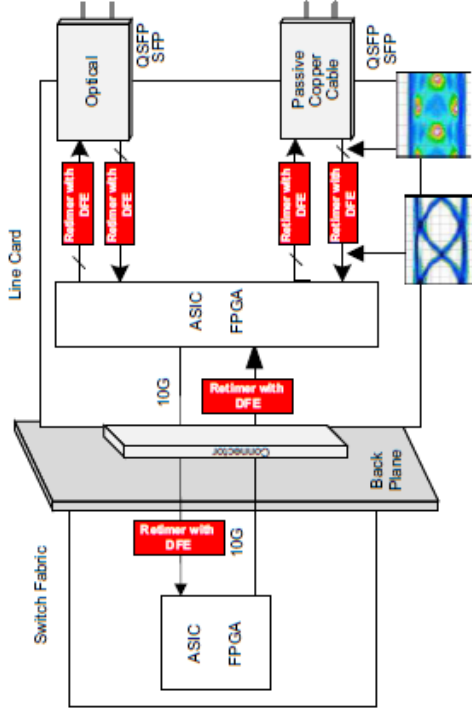


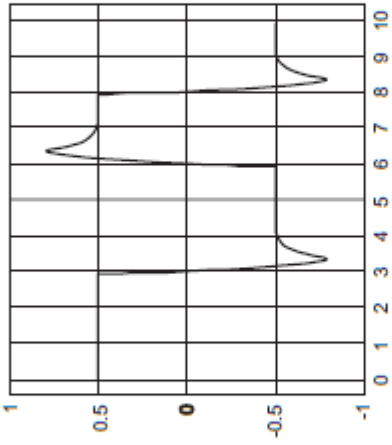
Figure 9. Typical Application

DS110DF111, 43.

Claim 15	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
----------	---

Exhibit A-4

Claim 15	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
------------------------	---

Claim 15	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this preamble is not disclosed, either explicitly or inherently, by TI DS110DF111, this preamble is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading. TI DS110DF111 discloses and/or renders obvious this limitation.
15[a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being	

Claim 15	
connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.

Claim 15

8.1 Application Information

The DS110DF111 is a 2 channel retimer that support many different data rates and application spaces.

8.2 Typical Application

Figure 9 shows a typical implementation for the DS110DF111 in a back plane application. The DS110DF111 can also be used for front port applications. The DS110DF111 supports data rates for CPRI, Infiniband, Ethernet, Interlaken and other custom data rates. For applications which include a lower VCO/4 or VCO/8 data-rate the CTLE value will not adapt automatically. Instead the CTLE value is taken directly from channel register 0x3A. For short, low-loss channels this value should be adjusted as indicated in the Channel Register Table.

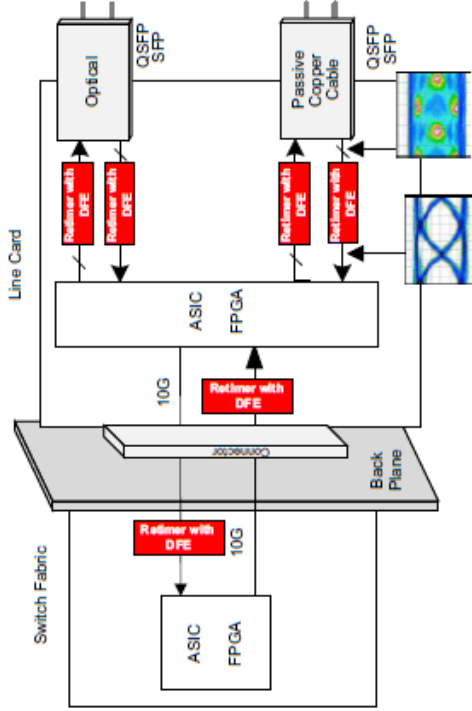


Figure 9. Typical Application

DS110DF111, 43.

Claim 15	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
------------------------	---

Exhibit A-4

Claim 15	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
------------------------	---

Exhibit A-4

Claim 15	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7. Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading. TI DS110DF111 discloses and/or renders obvious this limitation.
15[b] inserting the second end connector plug of the cable into a second host interface	

Claim 15 port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,	3 Description The DS110DF111 is a dual-channel (1-lane bidirectional) retimer with integrated signal conditioning. The DS110DF111 includes an input Continuous-Time Linear Equalizer (CTLE), clock and data recovery (CDR), and transmit driver on each channel. The DS110DF111 with its on-chip Decision Feedback Equalizer (DFE) can enhance the reach and robustness of long, lossy, cross-talk-impaired high speed serial links to achieve $BER < 1 \times 10^{-15}$. For less-demanding applications and interconnects, the DFE can be switched off and achieve the same BER performance. The DS125DF111 and DS110DF111 devices are pin-compatible. Each channel of the DS110DF111 independently locks to serial data at data rates from 8.5 to 11.3 Gbps or to any supported substrate of these data rates. This simplifies system design and lowers overall cost. Programmable transmit de-emphasis driver offers precise settings to meet the SFF-8431 output eye template. The fully adaptive receive equalization (CTLE and DFE) enables longer distance transmission in lossy copper interconnect and backplanes with multiple connectors. The CDR function is ideal for use in front port parallel optical module applications to reset the jitter budget and retime high-speed serial data. DS110DF111, 1.
--	--

Claim 15

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

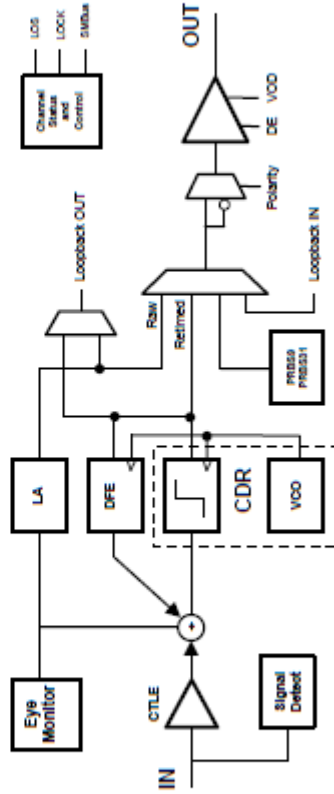


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

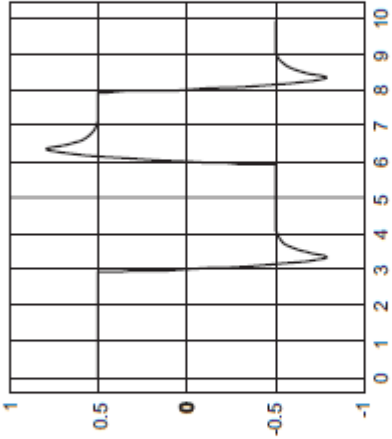
7.3.1.1 Input Channel Equalization

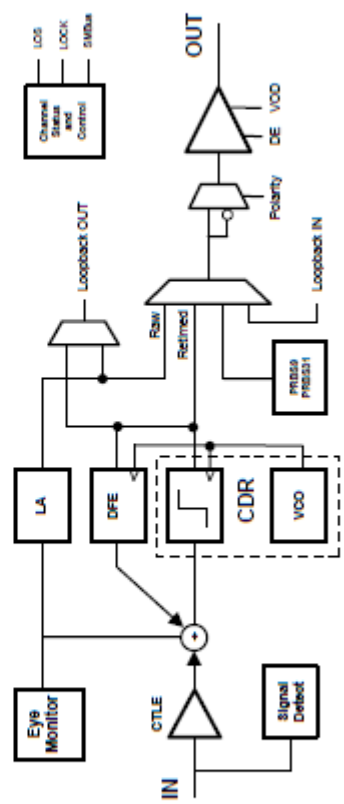
Physical transmission media comprising traces on printed circuit boards (PCBs) or copper cables exhibit a low-pass frequency response characteristic. The magnitude of the high frequency loss varies with the length of the transmission medium and with the loss of the materials which comprise it. This differential high frequency loss and the frequency-dependent group delay of the transmission medium introduce inter-symbol interference in the high-speed broadband signals propagating through the transmission medium.

Claim 15	To make configuration of these settings easier, the DS110DF111 is designed to determine the correct settings for the CTLE autonomously by automatically adapting these equalizations to the input transmission medium. The automatic adaptation takes place when a signal is first detected at the input to the DS110DF111, immediately after the DS110DF111 acquires phase lock. The automatic adaptation is also triggered whenever the CDR circuitry is reset. The DS110DF111 uses its internal eye monitor to generate a figure of merit for the adaptation. The DS110DF111 adjusts its CTLE boost settings in a systematic way to optimize this figure of merit. When 8b/10b encoding is used and the input channels has more than 15 dB of loss, the CTLE table and or adaption algorithm needs to be modified so as to prevent CTLE mal-adaption. This scenario occurs when the CTLE boost is insufficient at lower settings to cause regeneration of the high-frequency content of the K28.5 pattern. As boost is increased, the adaption Figure of Merit (FOM) temporarily observes eye closure as the EQ boost begins to restore the high-frequency content. If the FOM does not improve within the look-beyond counter depth, the CTLE will settle at a lower boost, which is insufficient to equalize the signal and provide good BER. The 5-tap DFE discriminates against input noise and random jitter as well as against crosstalk at the input to the DS110DF111. The DFE tap weights and polarities are adaptive and operate in conjunction with the CTLE to achieve an acceptable BER with more severe channel impairments. DS110DF111, 10-11. 7.3.1.2 Clock And Data Recovery The DS110DF111 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS110DF111 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. DS110DF111, 11.
------------------------	---

Exhibit A-4

Claim 15	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
------------------------	---

Claim 15	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading. TI DS110DF111 discloses and/or renders obvious this limitation.
15[c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit	

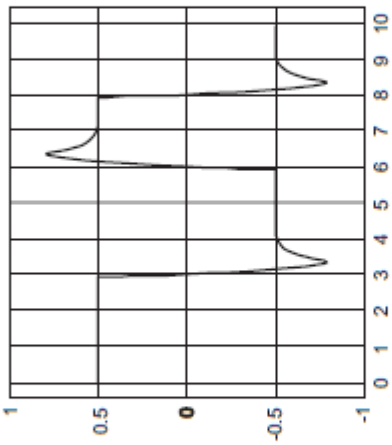
Claim 15 filter coefficient values stored in nonvolatile memories.	7.1 Overview The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer. Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111. 7.2 Functional Block Diagram  The diagram illustrates the functional blocks of the DS110DF111. The input signal (IN) passes through a CTLE (Continuous Time Linear Equalizer) and a signal defect block. The output of the CTLE is fed into a summing junction. The other input to the summing junction is a feedback signal from the CDR (Clock and Data Recovery) block. The output of the summing junction is fed into a DFE (Decision Feedback Equalizer) block. The output of the DFE is fed into a LA (Line Attenuator) block. The output of the LA is fed into an Eye Monitor block. The Eye Monitor block is also connected to a Channel Status and Control block, which provides LOS (Loss of Signal), LOCK, and SIGNAL outputs. The output of the Eye Monitor is fed into a feedback loop that passes through a Raw signal block, a Retimed signal block, and a Loopback IN block. The output of the Retimed signal block is fed into the CDR block. The CDR block is also connected to a VCO (Voltage-Controlled Oscillator) block. The output of the VCO is fed into a Polarity block, which is connected to a DE (De-emphasis) block. The output of the DE block is fed into an OUT block. The OUT block is also connected to a Loopback OUT block, which is connected to the Channel Status and Control block. Figure 6. DS110DF111 Data Path Block Diagram
---	--

DS110DF111, 10.

Exhibit A-4

Claim 15	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
-----------------	---

Exhibit A-4

Claim 15	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	---

Claim 15

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

P. DEPENDENT CLAIM 16

Claim 16

16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.

TI DS110DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

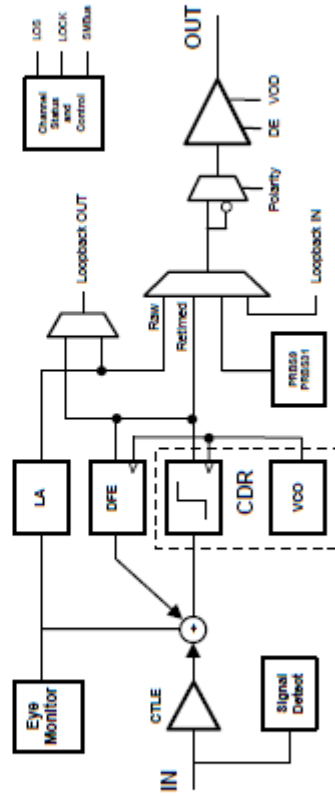
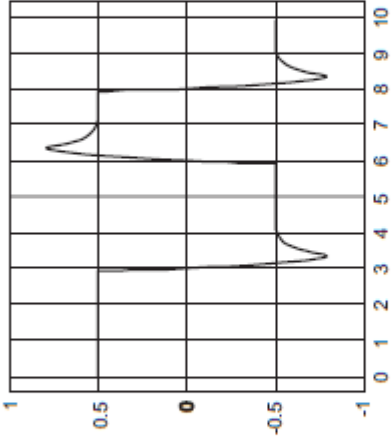


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 16	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
-----------------	---

Claim 16	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	--

Claim 16

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Q. DEPENDENT CLAIM 17

Claim 17
17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.

TI DS110DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

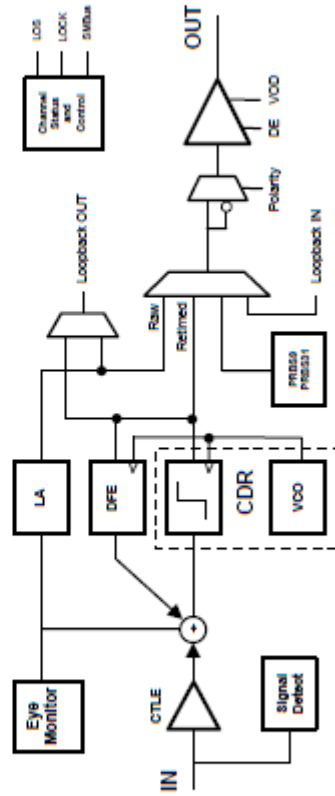
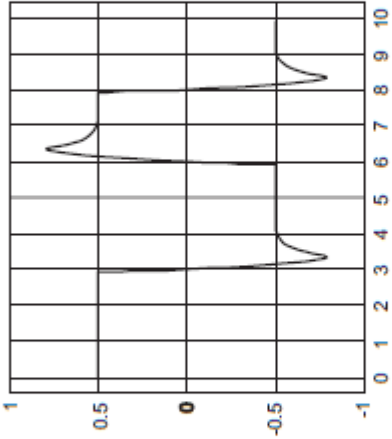


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 17	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
------------------------	---

Claim 17	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12. To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
----------	--

Claim 17

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

R. DEPENDENT CLAIM 18

Claim 18

18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.

TI DSI10DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

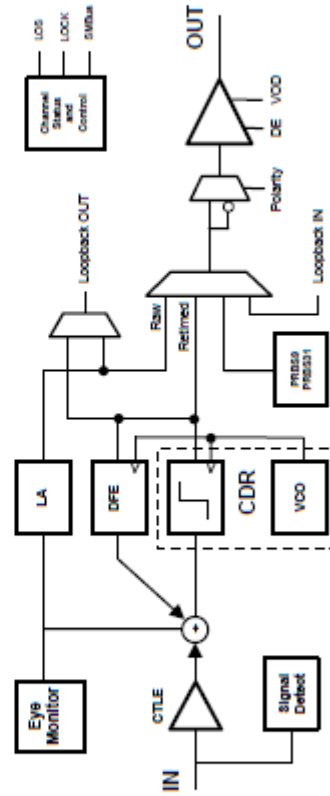
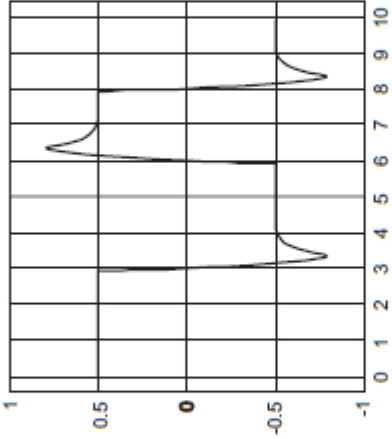


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 18	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
-----------------	---

Claim 18	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	---

Claim 18

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

S. DEPENDENT CLAIM 19

Claim 19

19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.

TI DS110DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

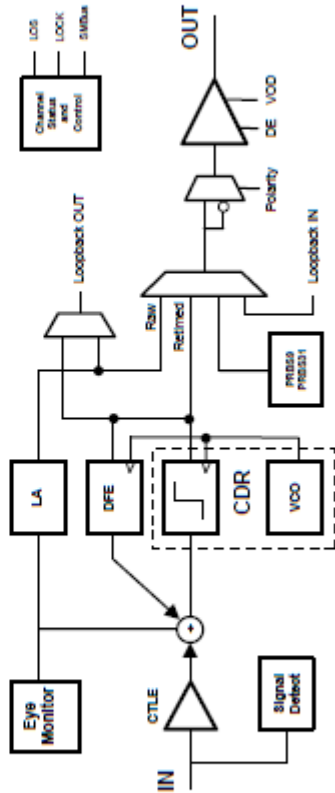
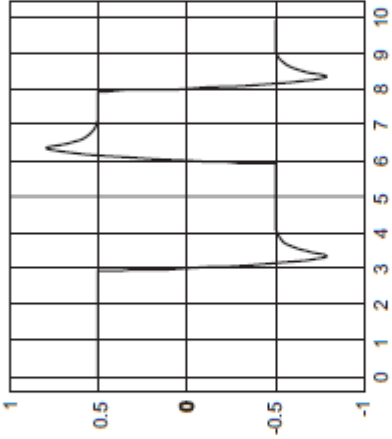


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 19	
	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.

Claim 19	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	---

Claim 19

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

T. DEPENDENT CLAIM 20

Claim 20
20. The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.

TI DS110DF111 discloses and/or renders obvious this limitation.

7.1 Overview

The DS110DF111 is a low-power, multirate, 2-channel retimer. Both channels operate independently. Each channel includes a Continuous Time Linear Equalizer (CTLE) which compensates for the presence of a dispersive transmission channel between the source and the input of the DS110DF111. Each channel includes an independent Voltage-Controlled Oscillator (VCO) and Phase-Locked Loop (PLL) which produce a clean clock. The clean clock produced by the VCO and the PLL is phase-locked to the incoming data clock, but the high-frequency jitter on the incoming data is attenuated by the PLL, producing a clean clock with substantially reduced jitter. This clean clock is used to retime the incoming data, removing high-frequency jitter from the data stream and producing a data output signal with reduced jitter. This provides the Clock and Data Recovery (CDR) function of the retimer.

Each channel of the DS110DF111 features an output driver with settable differential output voltage and settable output de-emphasis. The output de-emphasis compensates for dispersion in the transmission channel at the output of the DS110DF111.

7.2 Functional Block Diagram

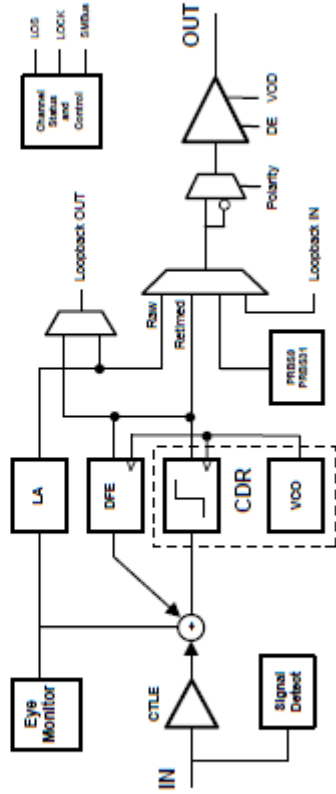
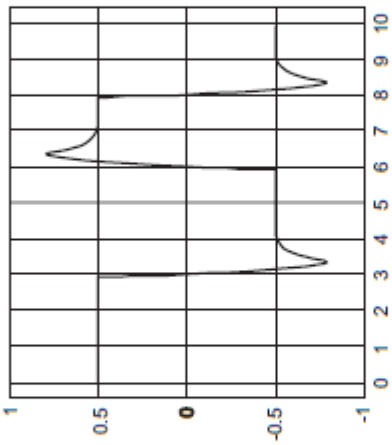


Figure 6. DS110DF111 Data Path Block Diagram

DS110DF111, 10.

Exhibit A-4

Claim 20	7.3.1.4 Datapath Multiplexer and Output Driver The DS110DF111 datapath multiplexer is used to control which internal signal will be presented to the output driver block. Inputs to this multiplexer include raw equalized data without clock recovery, retimed data, PRBS patterns, and Loopback data from the other datapath. The DS110DF111 output driver is used to control specific signal characteristics to enhance transmission quality. The output driver is used to control the following signal features • Amplitude • De-Emphasis • Edge Rate • Polarity The DS110DF111 is commonly used in applications where lossy transmission media exist both at the input and the output of the DS110DF111. The CTLE compensates for lossy transmission media at the input to the DS110DF111. The output de-emphasis compensates for the lossy transmission medium at the output of the DS110DF111. When there is a transition in the output data stream, the output differential voltage reaches its configured maximum value within the configured rise/fall time of the output driver. Following this, the differential voltage rapidly falls off until it reaches the configured VOD level minus the configured de-emphasis level. This accentuates the high-frequency components of the output driver signal at the expense of the low frequency components. The pre-distorted DS110DF111 output signal, with high-frequency components emphasized relative to its low frequency components, exhibits less inter-symbol interference after traveling down a dispersive transmission medium than an undistorted output signal.
-----------------	---

Claim 20	An idealized transmit waveform with analog de-emphasis applied is shown in Figure 7.  Figure 7. Idealized De-Emphasis Waveform The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS110DF111 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. DS110DF111, 11-12.
----------	--

Claim 20

7.5.1.26 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS110DF111, ranging from 0 dB to -12 dB. The de-emphasis values come from register 0x15, bits 2:0 and register 0x15, bit 6, which is the de-emphasis range bit. The available driver de-emphasis settings and the mapping to these bits are shown in Table 25.

Table 25. De-Emphasis Settings

PIN SETTING	REGISTER 0X15 BIT [2], drv_dem[2]	REGISTER 0X15 BIT [1], drv_dem[1]	REGISTER 0X15 BIT [0], drv_dem[0]	REGISTER 0X15 BIT [6], drv_dem_range	DE-EMPHASIS SETTING (dB)
0	0	0	0	0	0.0
	0	0	1	1	-0.9
R	0	0	1	0	-1.5
	0	1	0	1	-2.0
	0	1	1	1	-2.8
	1	0	0	1	-3.3
F	0	1	0	0	-3.5
	1	0	1	1	-3.9
	1	1	0	1	-4.5
	0	1	1	0	-5.0
	1	1	1	1	-5.6
1	1	0	0	0	-6.0
	1	0	1	0	-7.5
	1	1	0	0	-8.0
	1	1	1	0	-12.0

DS110DF111, 32.

To the extent that this limitation is not disclosed, either explicitly or inherently, by TI DS110DF111, this limitation is obvious to a person of ordinary skill in the art based on (1) TI DS110DF111 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.