Exhibit A-5

Invalidity of U.S. Patent No. 10,877,233 (the "'233 Patent") in View of
Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

DS125DF410 was published in February 2018. DS125DF410 qualifies as prior art under at least 35 U.S.C. § 102(a) (AIA).

The Administrative Law Judge has not yet construed the claims and therefore the meaning of the terms in the claims has yet to be resolved. The support identified here for limitations of the Asserted Claims of the '233 Patent is responsive to Complainant's apparent infringement contentions in its Complaint, which Respondents disagree with. As such, nothing in Respondents' claim charts should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Respondents' understanding of the proper scope of the Asserted Claims of the '233 Patent.

All cross-references should be understood to include material that is cross-referenced within the cross-reference. Where a particular Figure is cited, the citation should be understood to encompass the caption and description of the Figure as well as any text relating to or describing the Figure. Conversely, where particular text referring to a Figure is cited, the citation should be understood to include the Figure as well. Respondents reserve the right to rely on additional citations or sources of evidence that also may be applicable, or that may become applicable in light of claim construction, changes in Complainant's infringement and/or domestic industry contentions, and/or information obtained during discovery as the Investigation progresses.

To the extent Complainant alleges that DS125DF410 does not disclose any particular limitation of the Asserted Claims of the '233 Patent, either expressly or inherently, it would have been obvious to a person of ordinary skill in the art as of the priority date of the '233 Patent to modify DS125DF410 and/or to combine the teachings of DS125DF410 with other prior art references, including but not limited to the prior art references cited in the Cover Pleading and the relevant section(s) of claim charts for other prior art references for the '233 Patent in a manner that would have rendered the Asserted Claims invalid as obvious.

Because Complainant has yet to identify any limitation of the Asserted Claims of the '233 Patent that it contends is not fully disclosed by DS125DF410, either alone or in combination with other prior art cited by Respondents, Respondents expressly reserve the right to rebut any such contention, including by identifying additional obviousness combinations, if any such contention is made by Complainant. Respondents further reserve the right to amend or supplement this claim chart at a later date as more fully set forth in the Cover Pleading.

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CREDO 2011
Amphenol v. Credo
IPR2025-00835

A. INDEPENDENT CLAIM 1

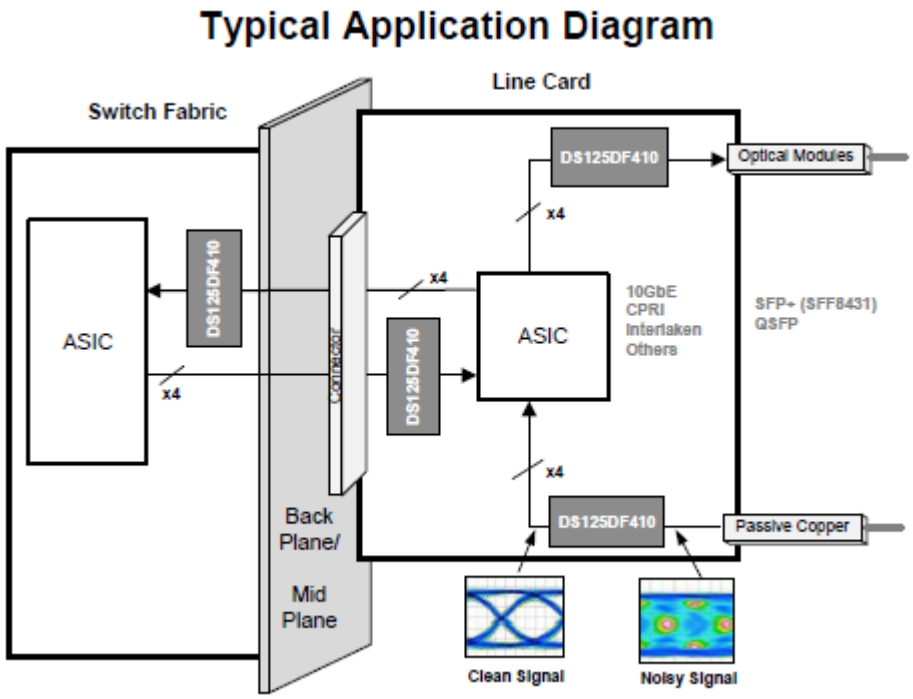
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
1[pre] A cable that comprises:	To the extent the preamble is limiting, DS125DF410 discloses and/or renders obvious this limitation.  DS125DF410, 1.

Exhibit A-5

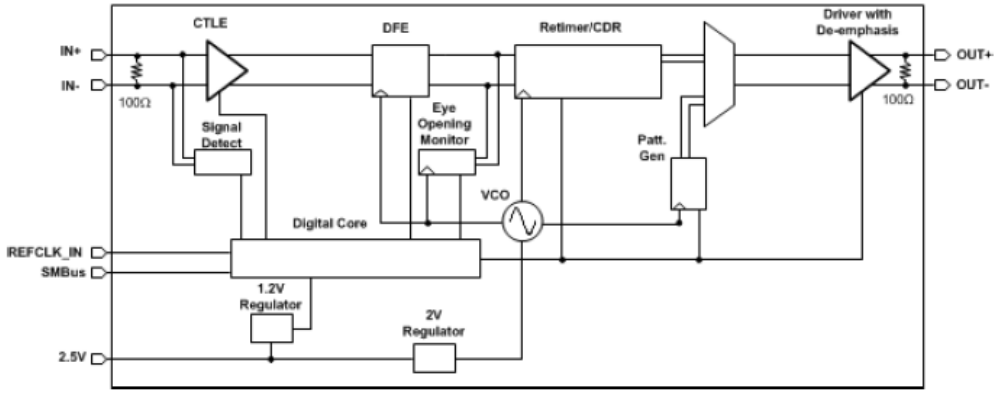
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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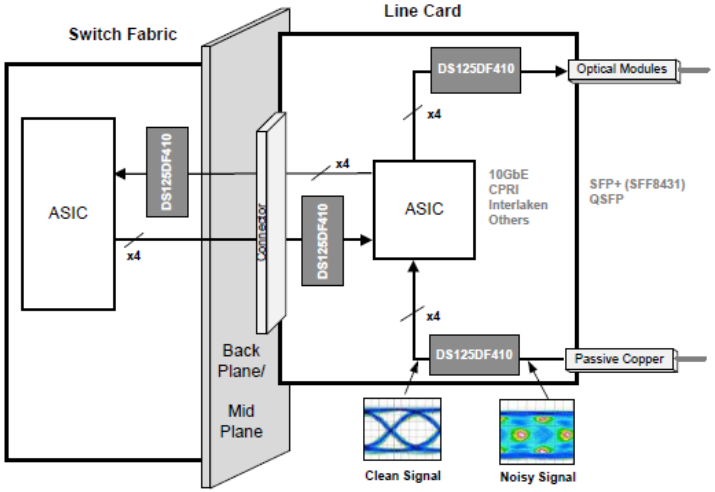
Exhibit A-5

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
9	**7.5.19 Setting the Adaptation/Lock Mode** *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this preamble is not disclosed, either explicitly or inherently, by DS125DF410, this preamble is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[a] a first data recovery and remodulation (DRR) device that	DS125DF410 discloses and/or renders obvious this limitation.

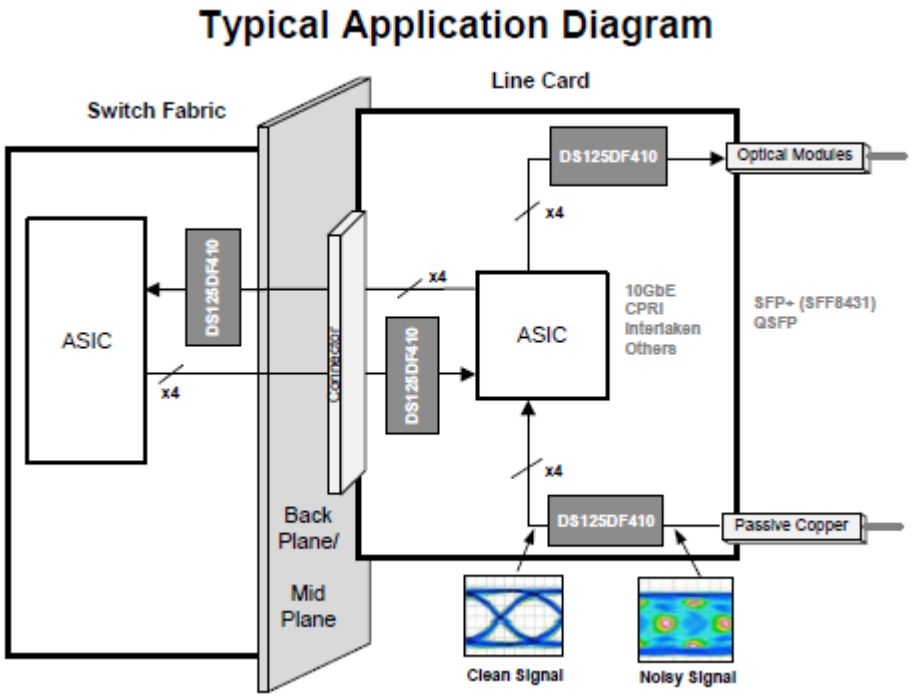
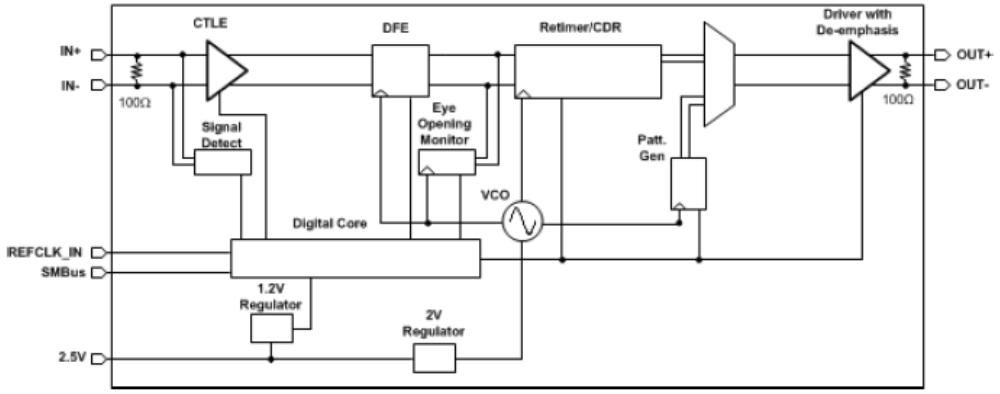
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
exchanges inbound and outbound multi-lane data streams with a first host interface port via a first end connector plug;	 DS125DF410, 1.

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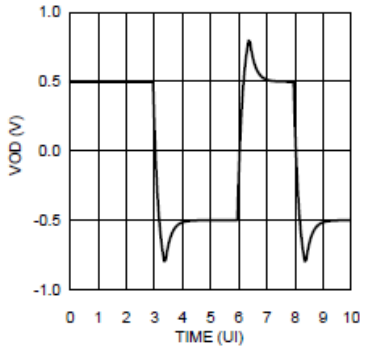
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	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
14	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410. DS125DF410, 31

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Exhibit A-5

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

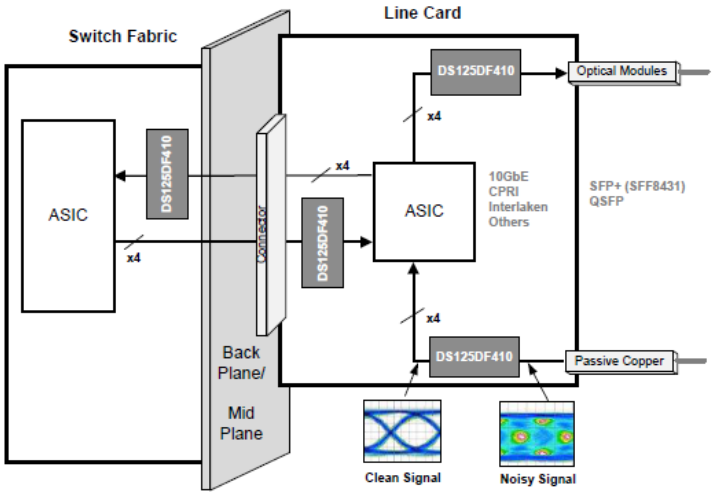
DS125DF410, 41.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[b] a second DRR device that	DS125DF410 discloses and/or renders obvious this limitation.

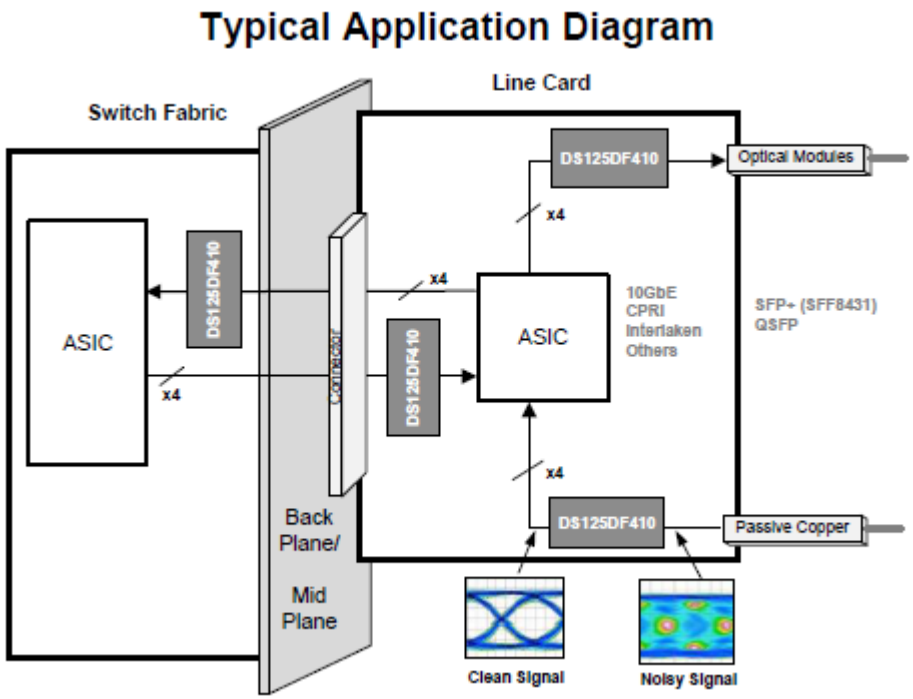
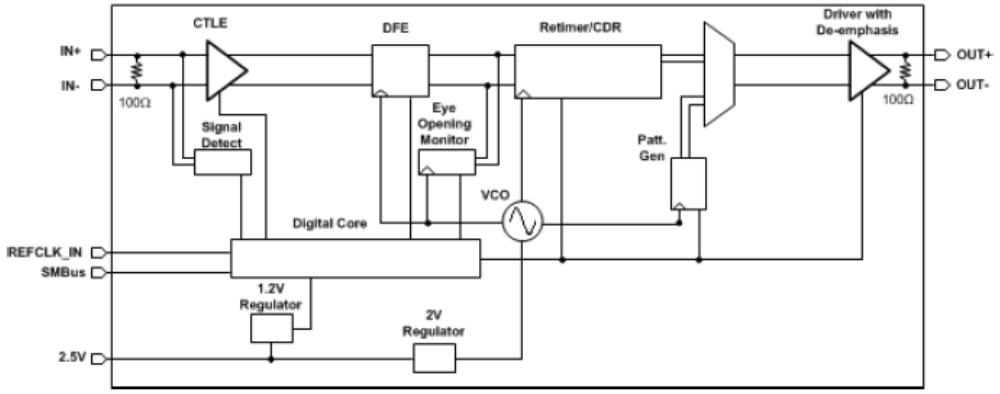
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
exchanges inbound and outbound multi-lane data streams with a second host interface port via a second end connector plug; and	 DS125DF410, 1.

Exhibit A-5

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

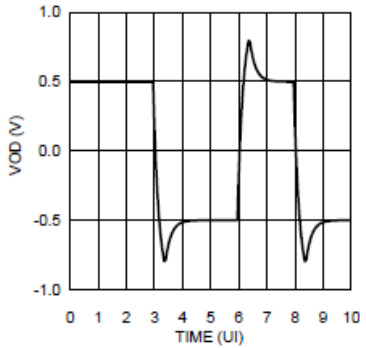
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
35	**7.5.19 Setting the Adaptation/Lock Mode** *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410. DS125DF410, 31

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Exhibit A-5

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

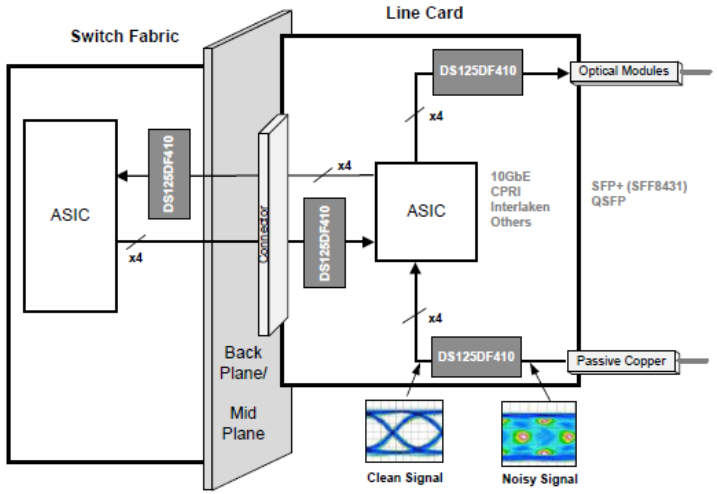
41

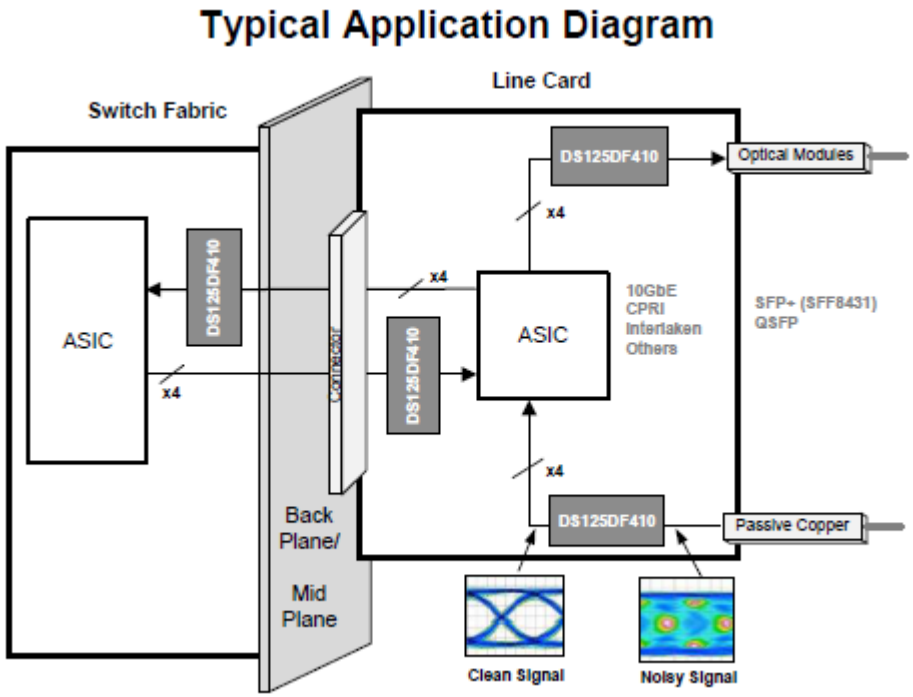
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

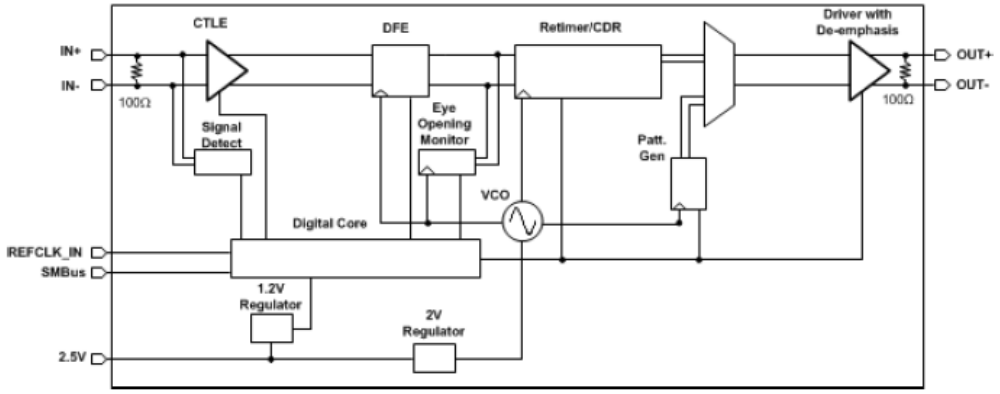
Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[c] electrical conductors	DS125DF410 discloses and/or renders obvious this limitation.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
connecting the first and second DRR devices to convey electrical transit signals therebetween,	 DS125DF410, 1.

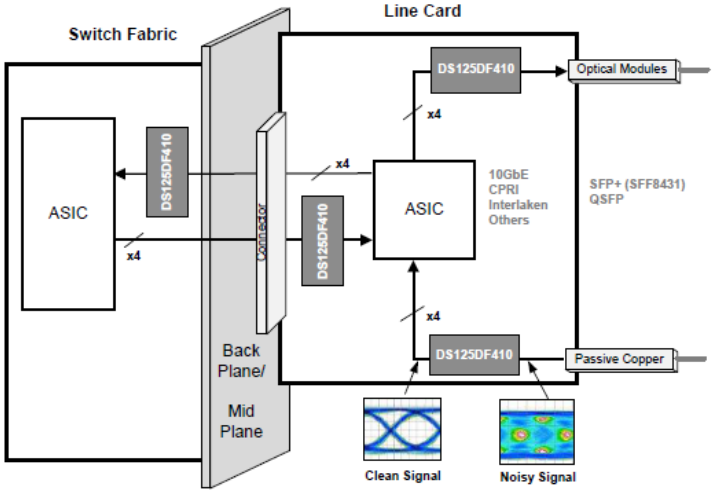
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

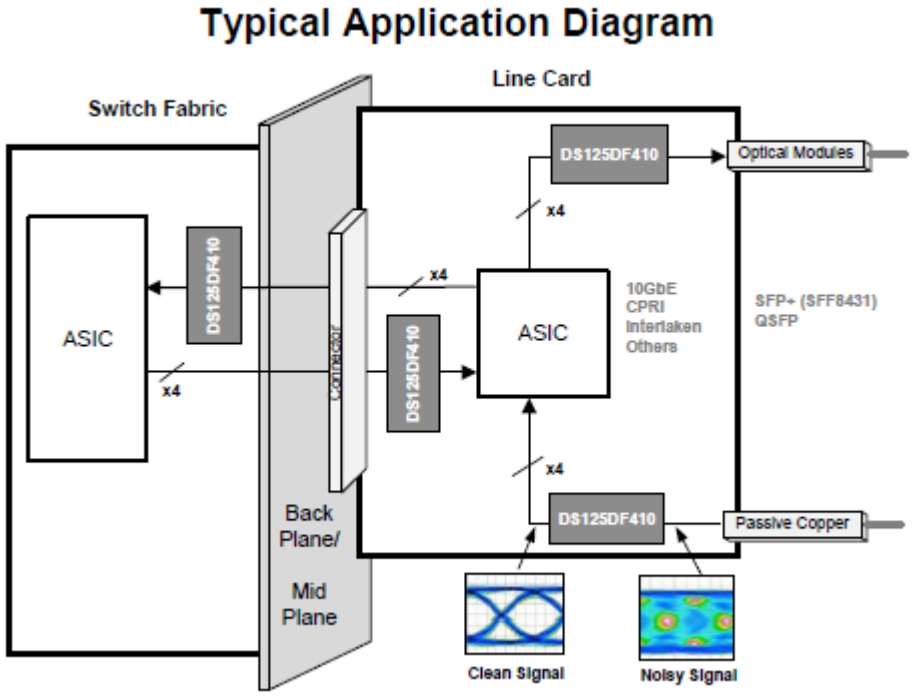
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

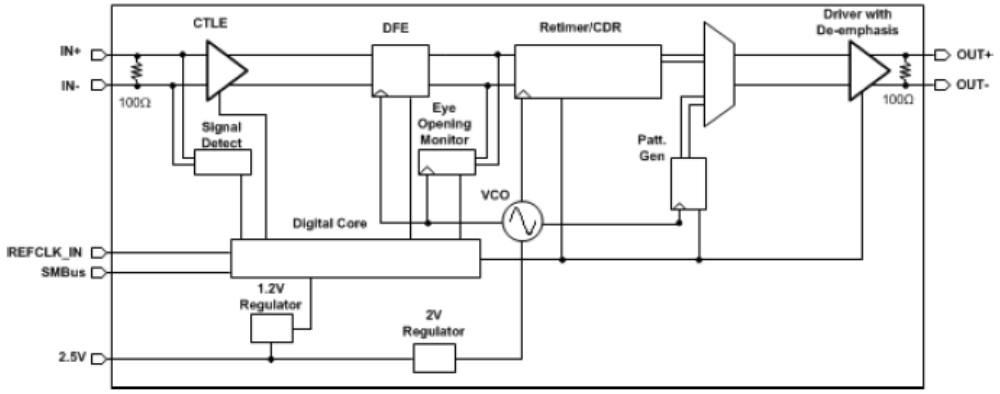
48

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[d] the first DRR device converting between said electrical transit signals and said	DS125DF410 discloses and/or renders obvious this limitation.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
inbound and outbound multilane data streams for the first host interface port, and	 DS125DF410, 1.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

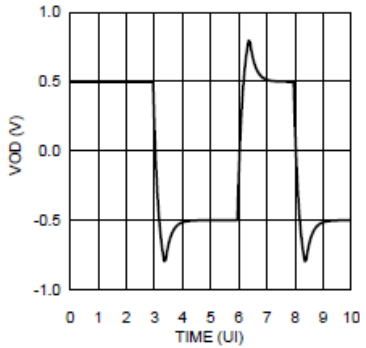
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

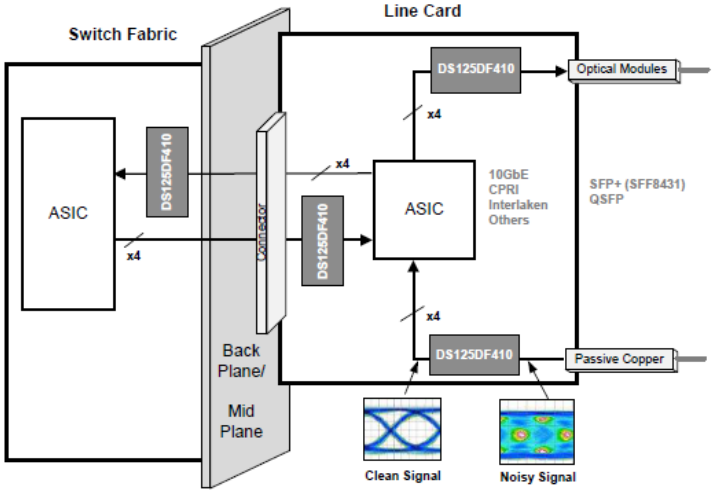
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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Exhibit A-5

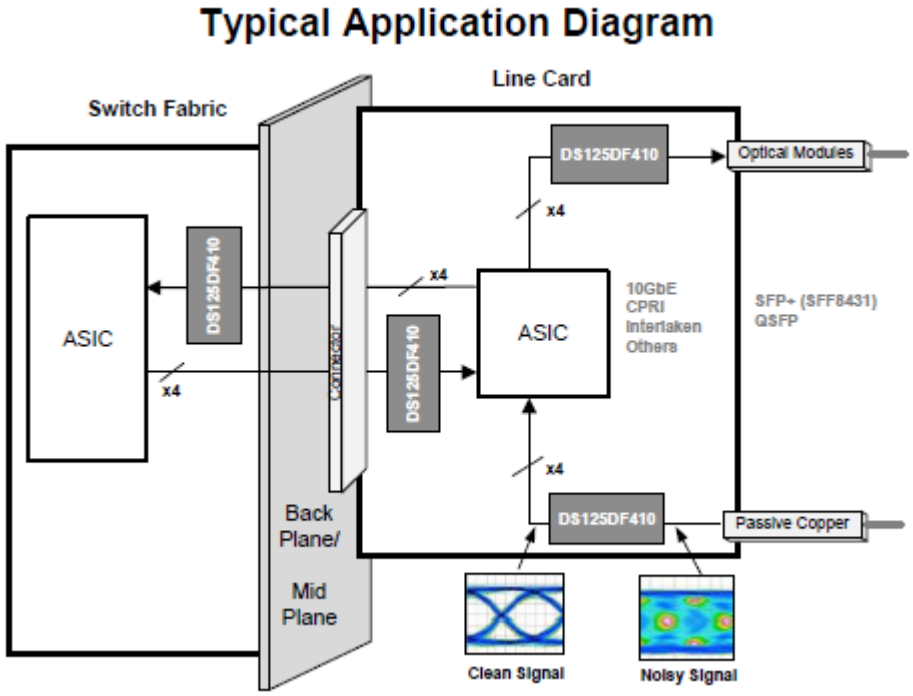
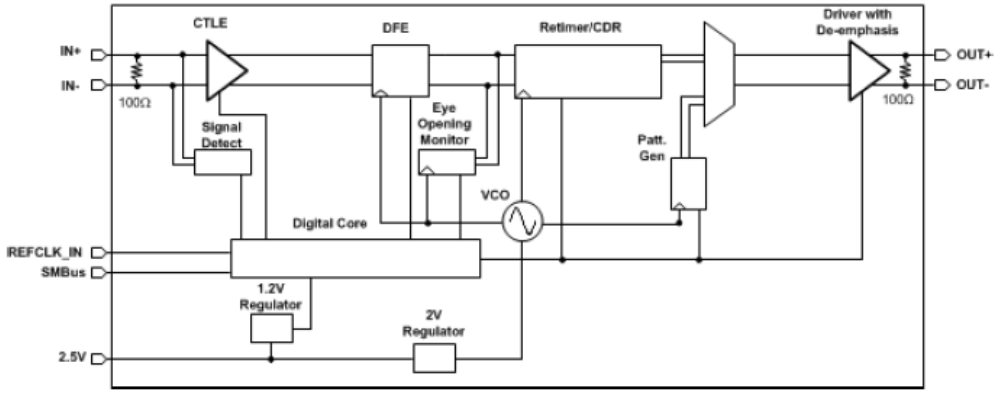
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
1[e] the second DRR device converting between said electrical transit signals and said inbound and outbound multilane data streams for the second host interface port,	 DS125DF410, 1.

Exhibit A-5

Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

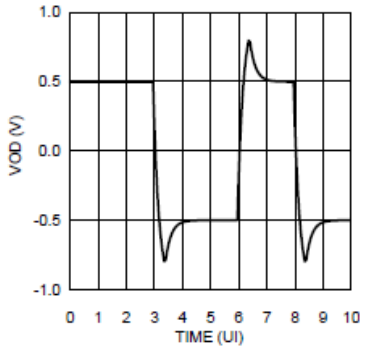
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

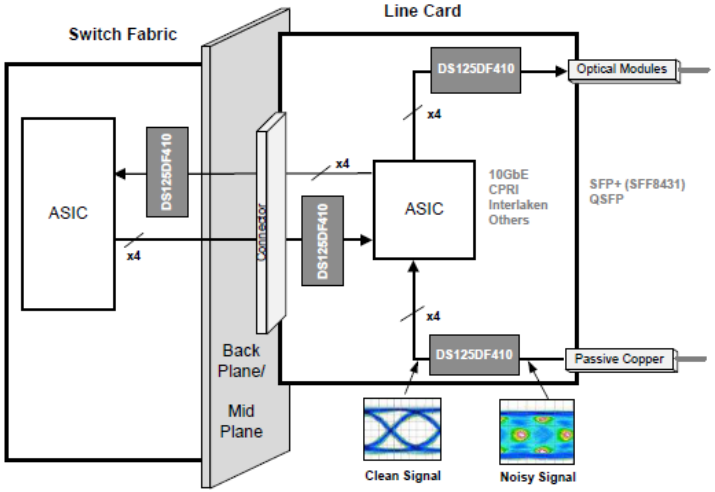
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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
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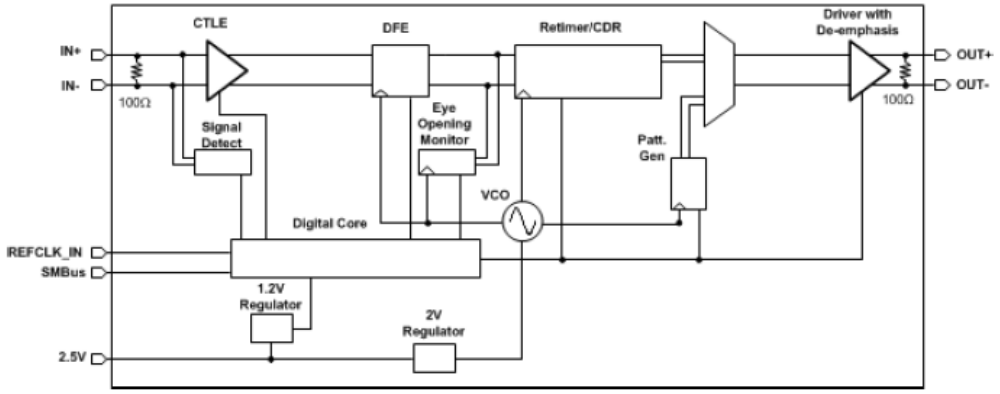
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
64	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
1[f] the first and second DRR devices providing preequalization	DS125DF410 discloses and/or renders obvious this limitation.

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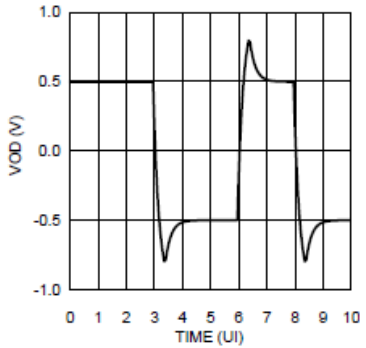
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71	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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	7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410. DS125DF410, 31

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7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

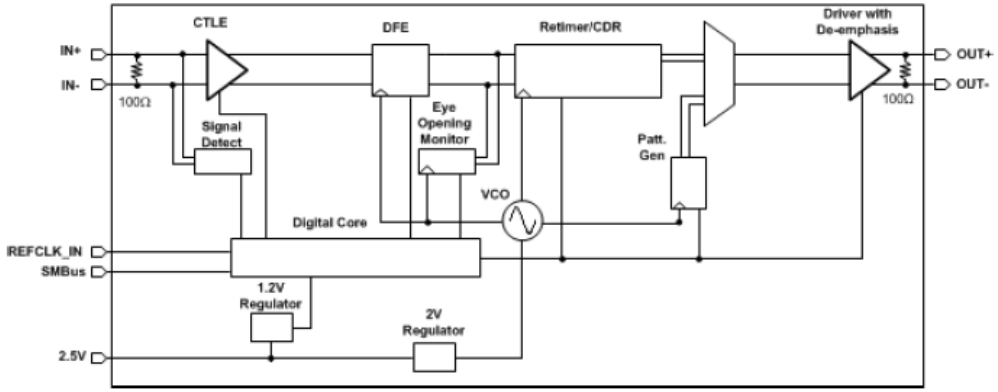
Claim 1	Texas Instruments – DS125DF410 Low Power Multi-Rate Quad Channel Retimer ("DS125DF410")
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

B. DEPENDENT CLAIM 2

Claim 2	
2. The cable of claim 1, further comprising a first controller that configures the first DRR device in response to a power-on event, the first controller retrieving the transmit filter coefficient values from the nonvolatile memories as part of said configuring.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 2	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 2	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

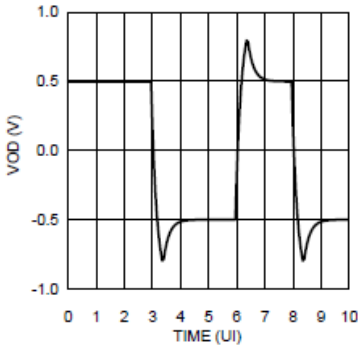
Claim 2	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 2	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 2	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 2	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 2	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 2	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

Claim 2	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

Claim 2	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 2	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 2	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 2	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 2	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 2	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

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Claim 2	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

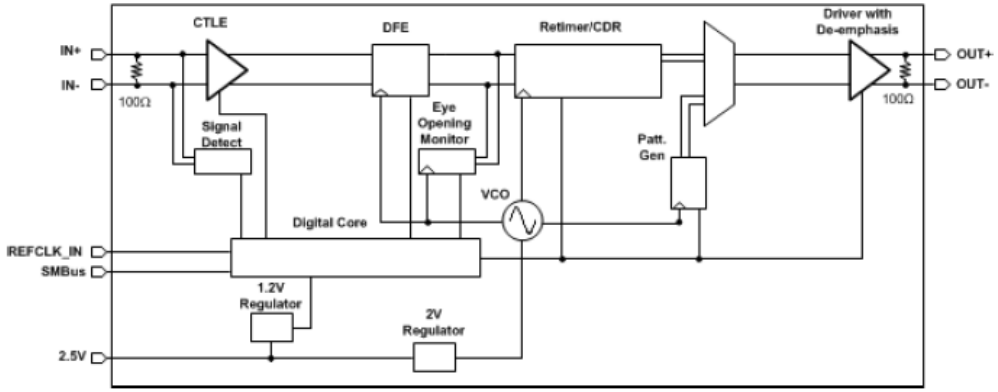
C. DEPENDENT CLAIM 3

Claim 3	
3. The cable of claim 1, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.	DS125DF410 discloses and/or renders obvious this limitation.

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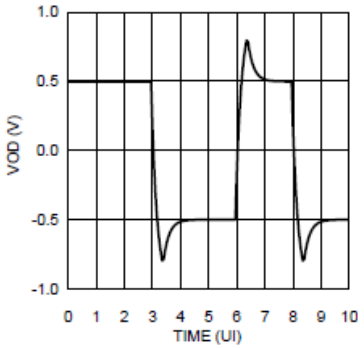
Claim 3	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 3	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 3	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 3	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 3	
103	**7.3.5 Clock and Data Recovery** The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

Claim 3	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 3	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 3	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 3	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 3	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 3	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 3	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

Claim 3	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 3	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

Claim 3	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

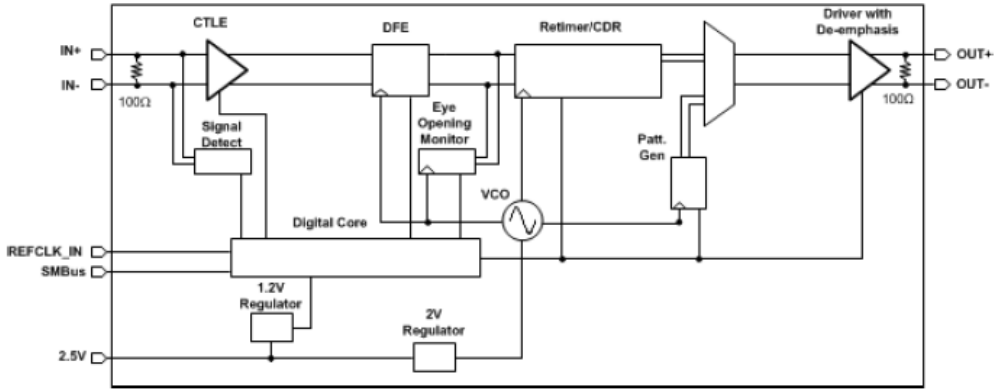
Claim 3	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

D. DEPENDENT CLAIM 4

Claim 4	
4. The cable of claim 3, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 4	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 4	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

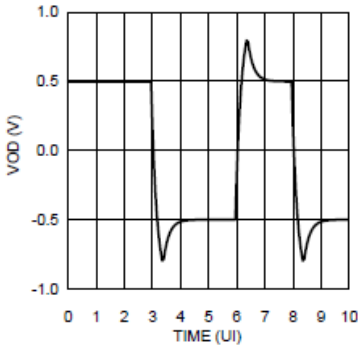
Claim 4	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

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Claim 4	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 4	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 4	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 4	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 4	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 4	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 4	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 4	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 4	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 4	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

Claim 4	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

Claim 4	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

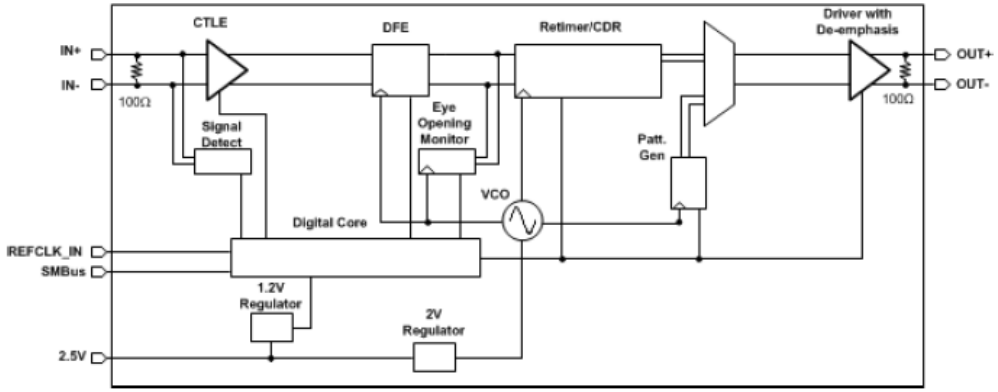
Claim 4	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

E. DEPENDENT CLAIM 5

Claim 5	
5. The cable of claim 4, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 5	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

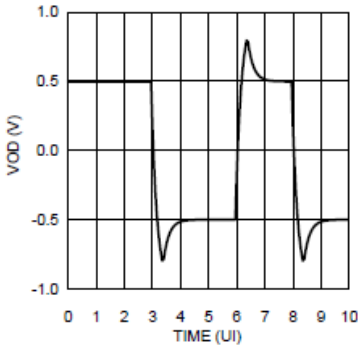
Claim 5	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 5	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 5	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 5	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 5	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 5	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 5	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 5	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 5	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 5	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 5	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 5	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

Claim 5	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

Claim 5	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

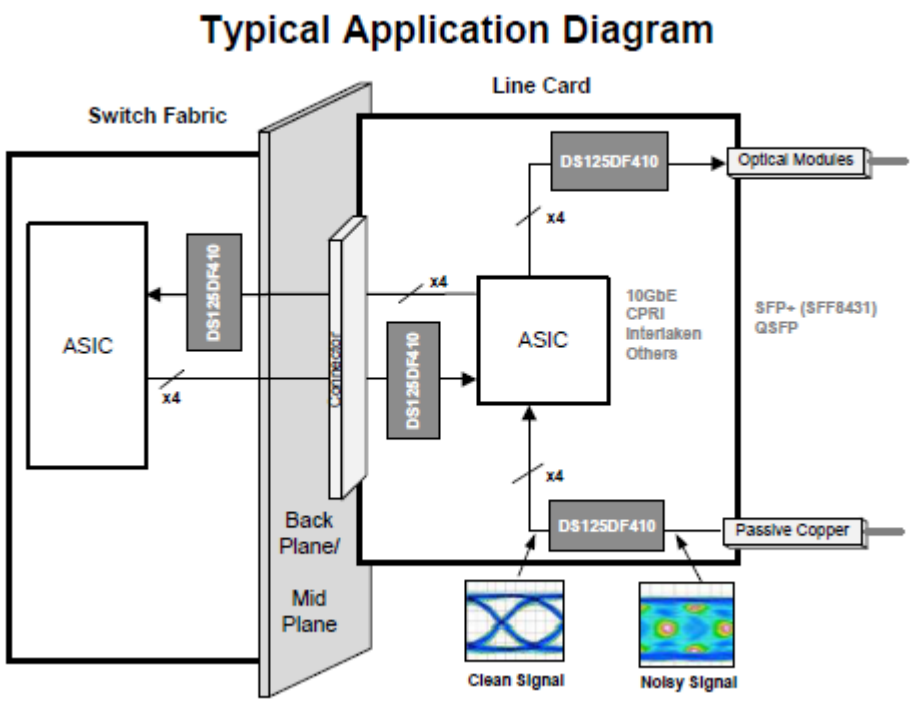
DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 5	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

F. DEPENDENT CLAIM 6

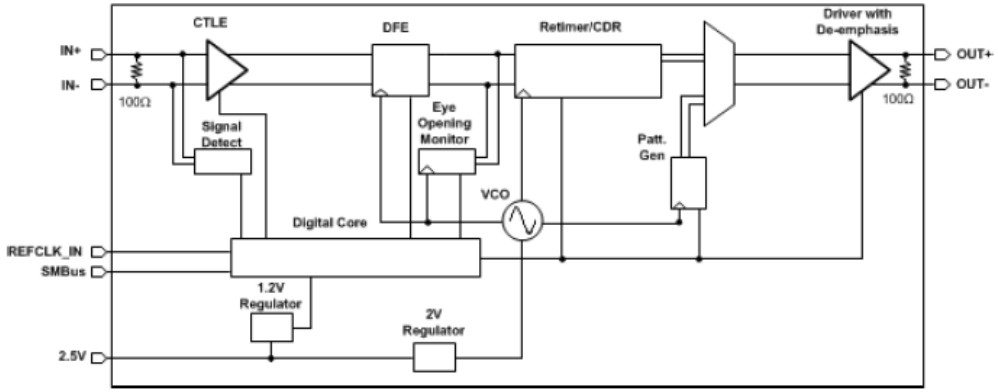
Claim 6	
6. The cable of claim 4, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 6	
	 DS125DF410, 1.

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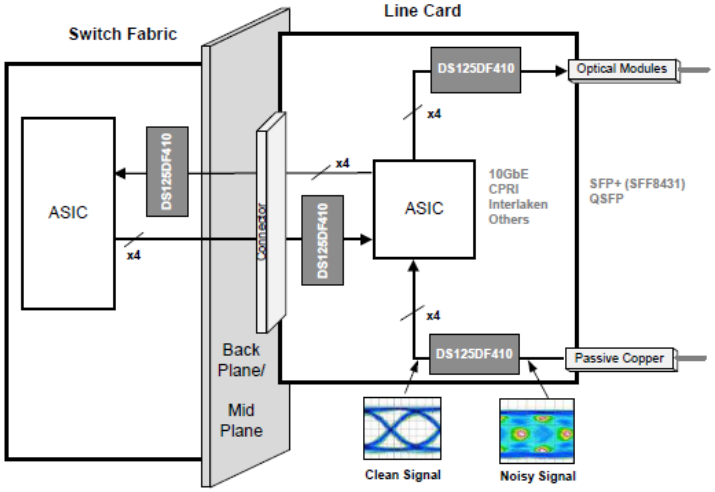
Claim 6	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 6	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 6	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 6	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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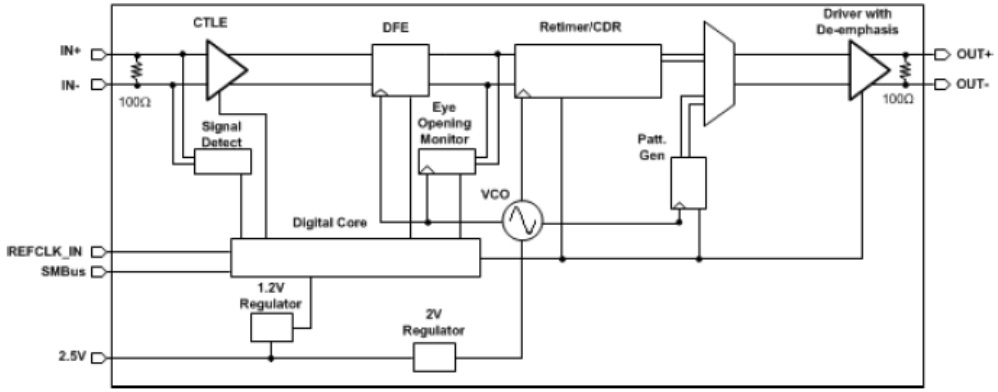
Claim 6	
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50.

G. DEPENDENT CLAIM 7

Claim 7	
7. The cable of claim 1, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 7	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

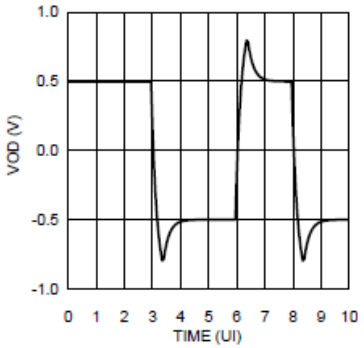
Claim 7	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 7	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 7	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 7	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 7	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 7	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 7	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 7	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 7	

DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 7	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 7	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

Claim 7	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

Claim 7	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 7	

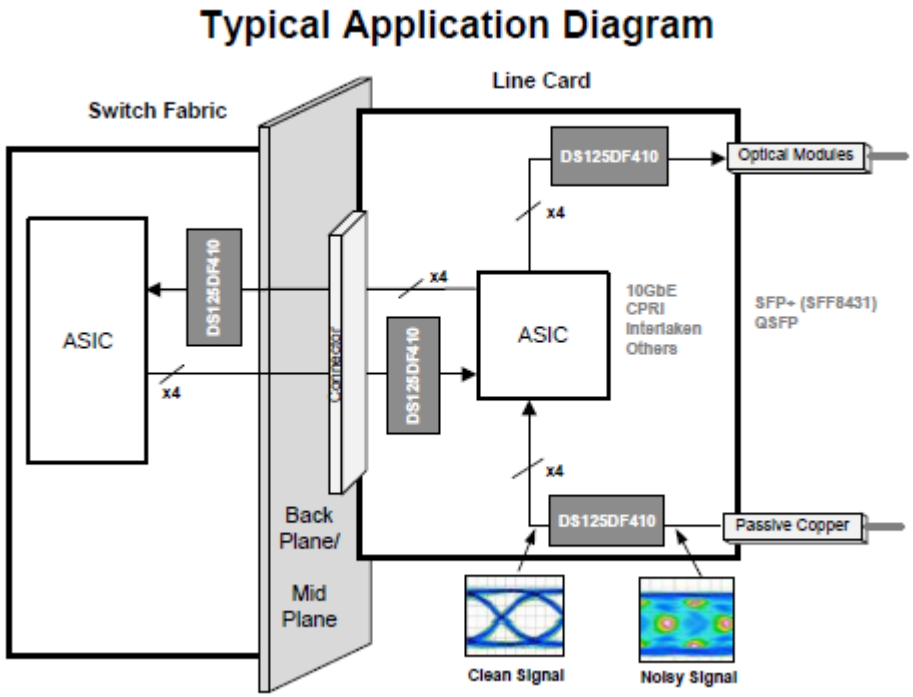
2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 7	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

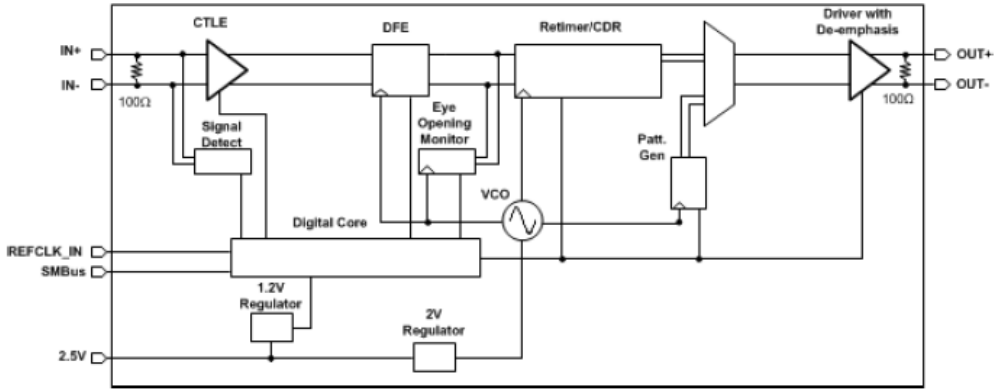
H. INDEPENDENT CLAIM 8

Claim 8	
8[pre] A cable manufacturing method that comprises:	To the extent the preamble is limiting, DS125DF410 discloses and/or renders obvious this limitation.  DS125DF410, 1.

Claim 8	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 8	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

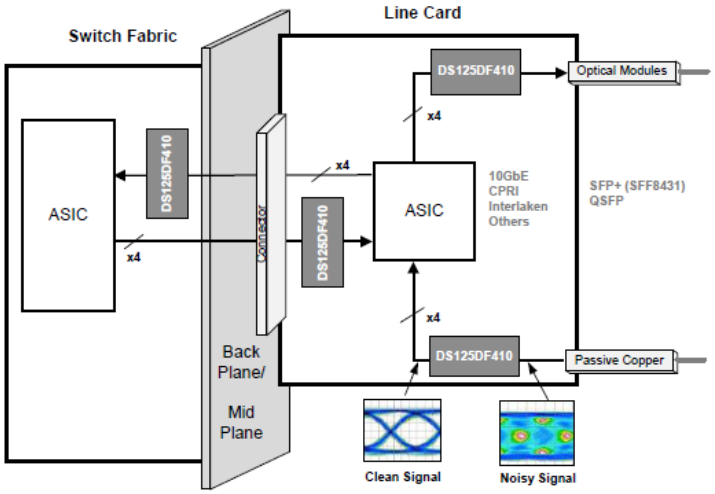
171

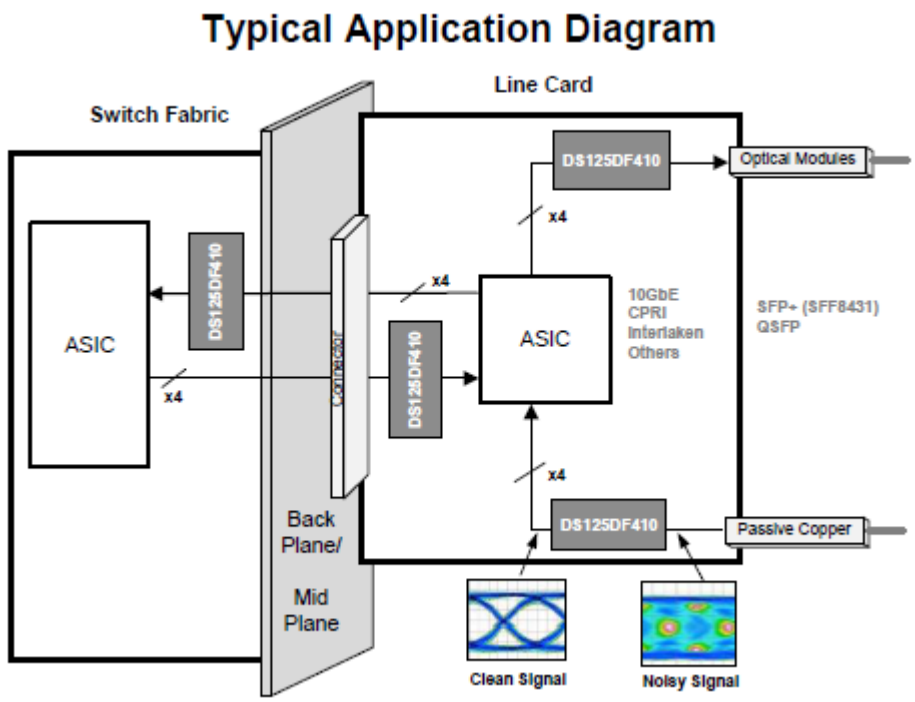
Claim 8	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

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Claim 8	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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Claim 8	
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this preamble is not disclosed, either explicitly or inherently, by DS125DF410, this preamble is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[a] connecting a first connector plug to a first data recovery and re-modulation (DRR) device that exchanges	DS125DF410 discloses and/or renders obvious this limitation.

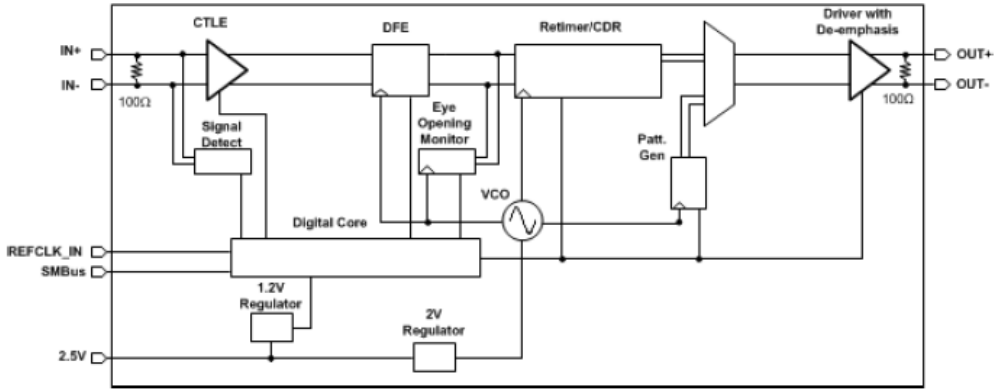
Claim 8	
multi-lane data streams with a first host interface port via the first connector plug;	 DS125DF410, 1.

Claim 8	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 8	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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Claim 8	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

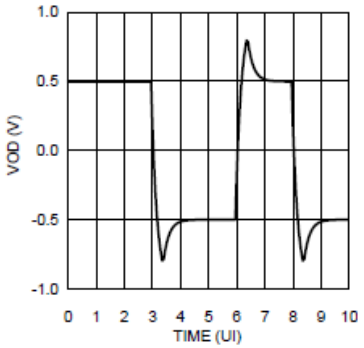
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Claim 8	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 8	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 8	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 8	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 8	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 8	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 8	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 8	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

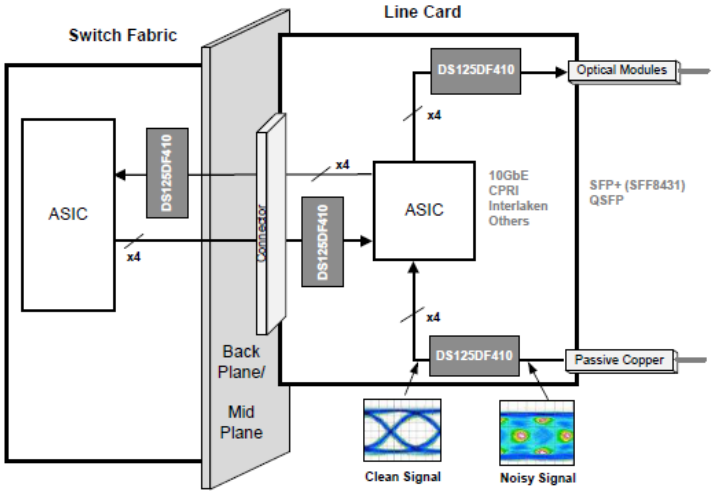
189

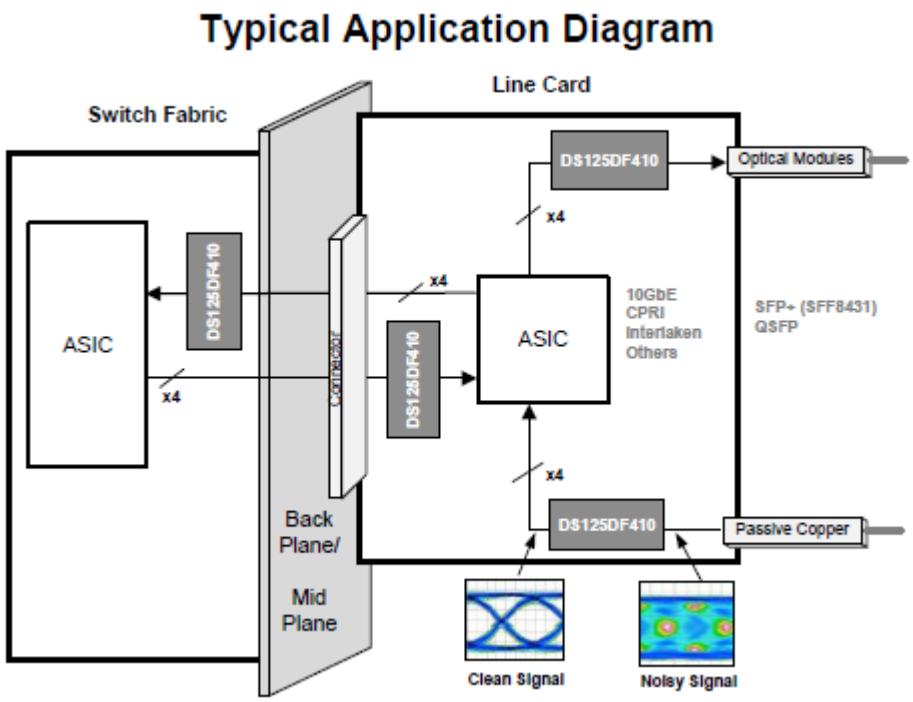
Claim 8	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

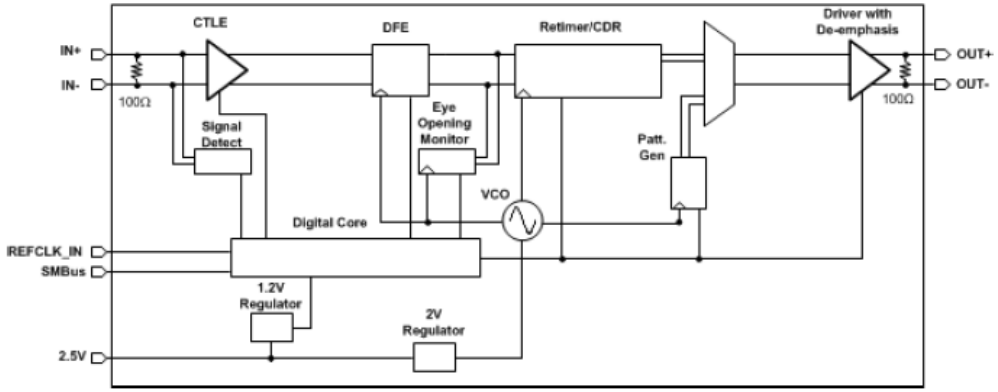
Claim 8	
	DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[b] connecting a second connector plug to a second	DS125DF410 discloses and/or renders obvious this limitation.

Claim 8	
DRR device that exchanges multi-lane data streams with a second host interface port via the second connector plug;	 DS125DF410, 1.

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Claim 8	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 8	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

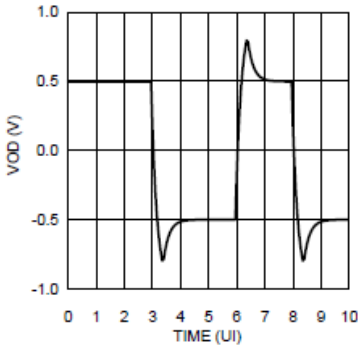
Claim 8	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 8	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 8	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 8	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 8	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 8	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 8	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 8	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 8	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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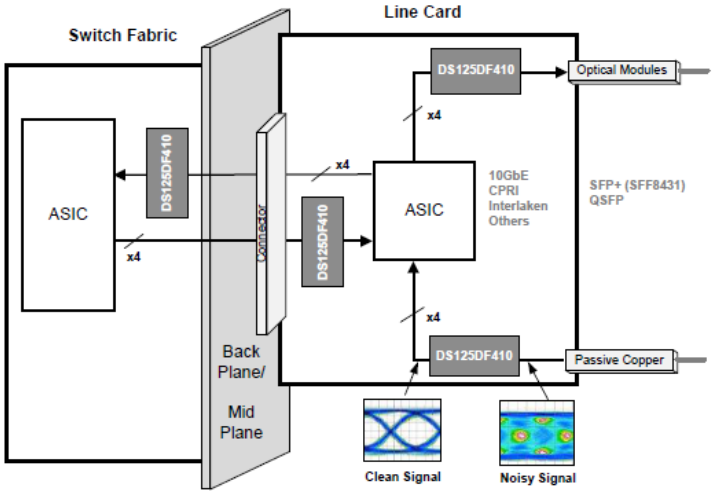
Claim 8	

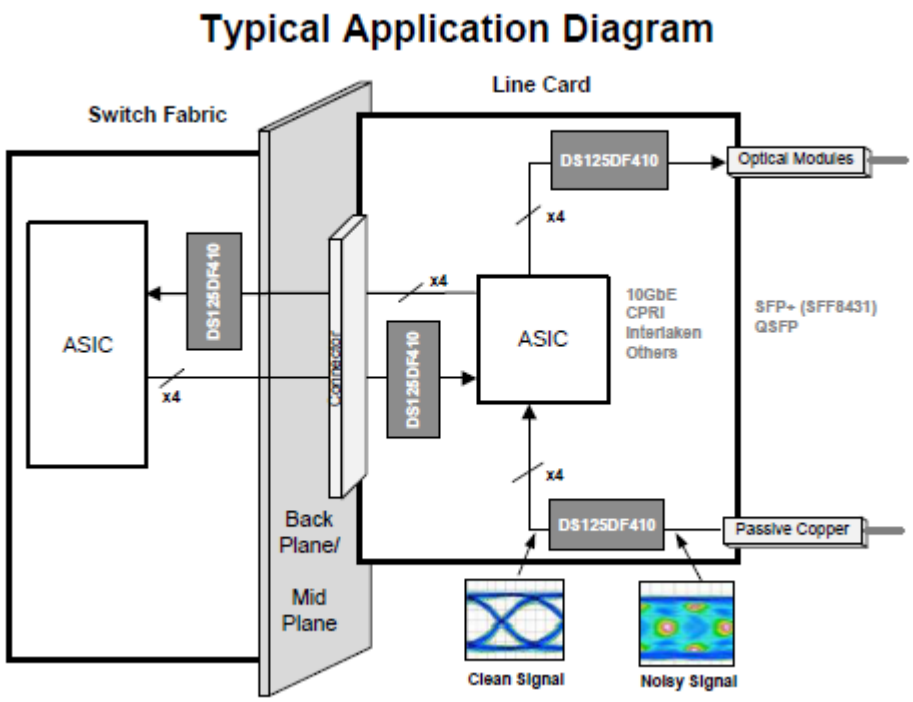
2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

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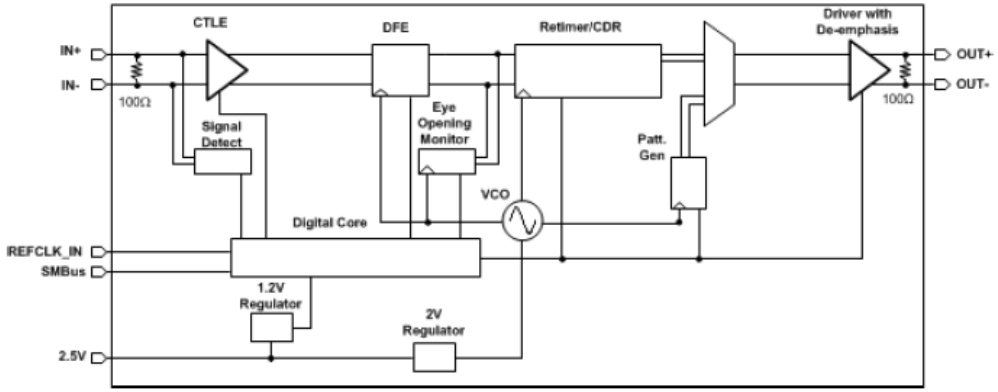
Claim 8	
	DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[c] connecting electrical conductors to the first and	DS125DF410 discloses and/or renders obvious this limitation.

Claim 8	
second DRR devices to convey electrical transit signals therebetween,	 DS125DF410, 1.

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Claim 8	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 8	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

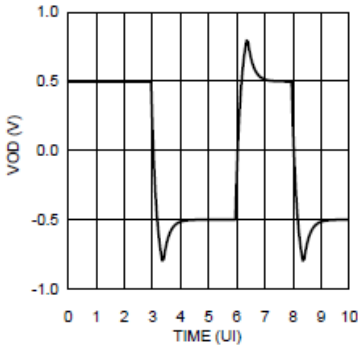
Claim 8	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 8	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 8	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

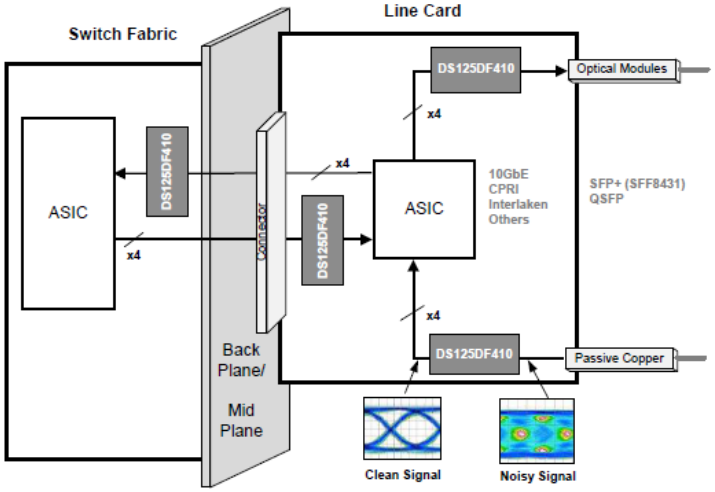
214

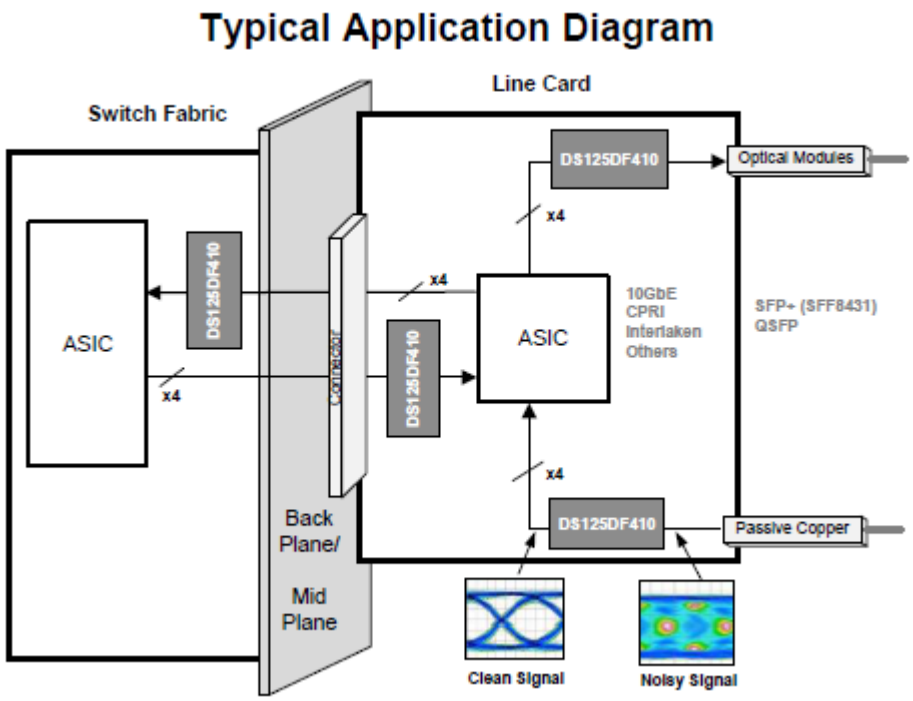
Claim 8	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 8	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

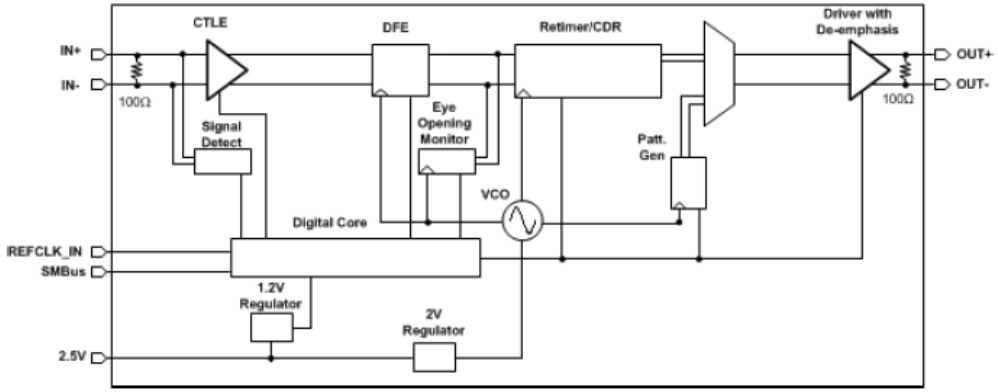
216

Claim 8	
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[d] the first DRR device converting between said electrical transit signals and said multi-lane data streams	DS125DF410 discloses and/or renders obvious this limitation.

Claim 8	
for the first host interface port, and	 DS125DF410, 1.

Claim 8	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

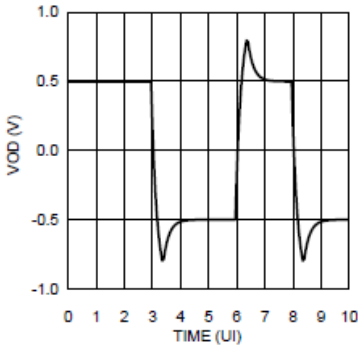
Claim 8	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 8	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 8	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 8	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

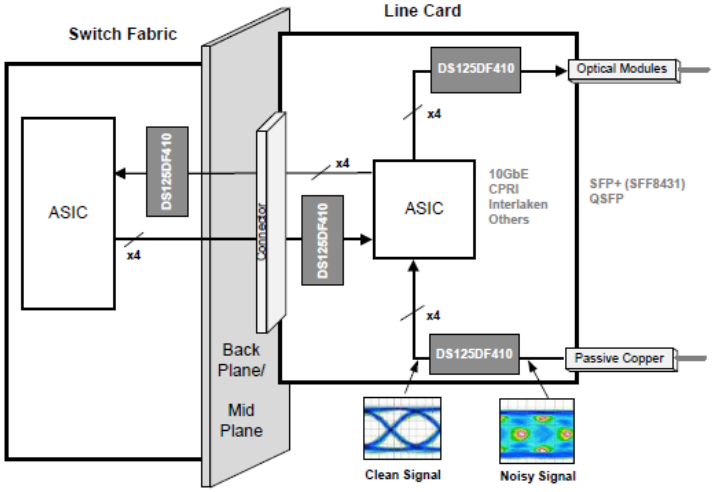
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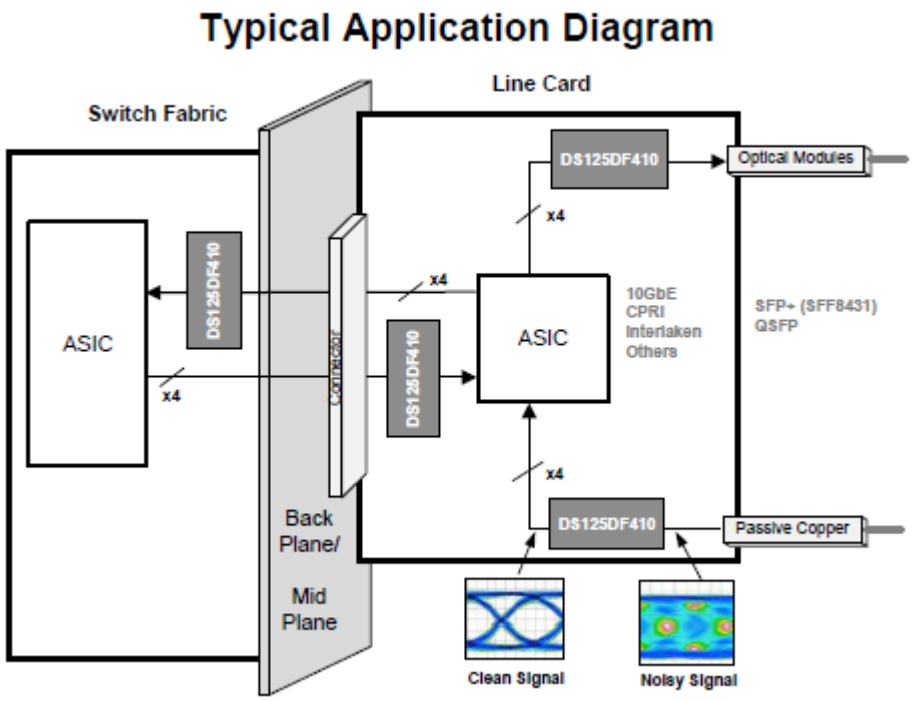
Claim 8	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 8	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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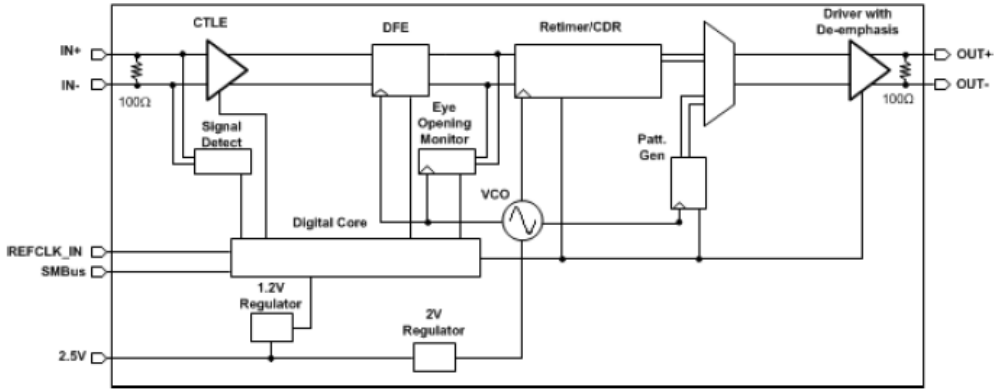
Claim 8	
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[e] the second DRR device converting between said electrical transit signals and said multi-lane data streams	DS125DF410 discloses and/or renders obvious this limitation.

Claim 8	
for the second host interface port,	 DS125DF410, 1.

Claim 8	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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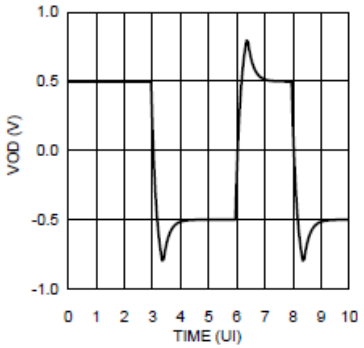
Claim 8	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 8	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 8	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

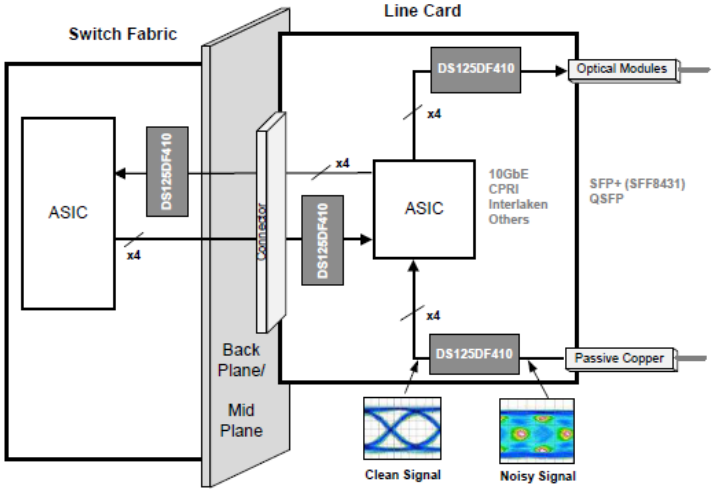
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Claim 8	
232	**7.3.5 Clock and Data Recovery** The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

Claim 8	
233	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

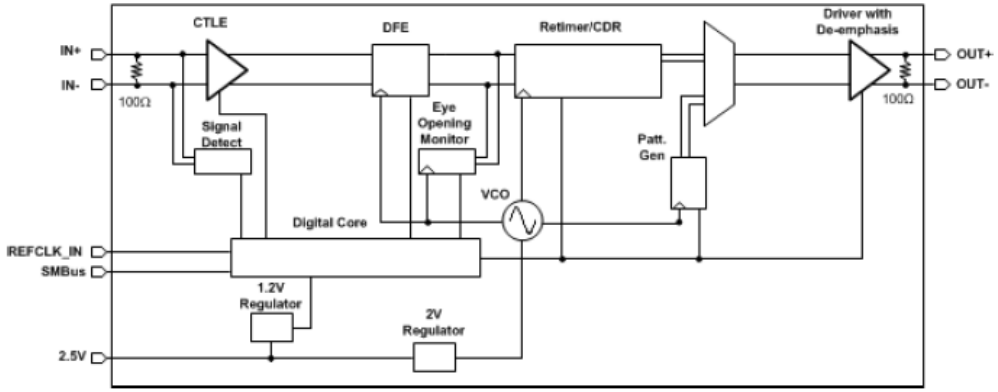
Claim 8	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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Claim 8	
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
8[f] the first and second DRR devices providing preequalization of the electrical	DS125DF410 discloses and/or renders obvious this limitation.

Claim 8	
transit signals using transmit filter coefficient values stored in nonvolatile memories.	**1 Features** • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 8	
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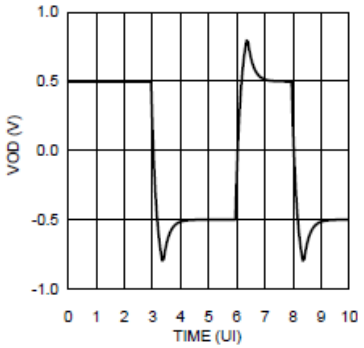
Claim 8	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 8	
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Claim 8	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 8	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 8	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 8	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 8	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 8	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 8	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 8	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

Claim 8	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 8	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

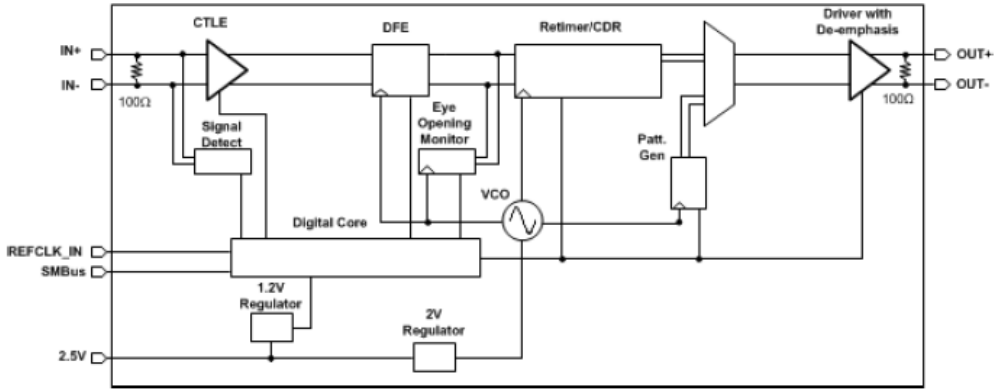
I. DEPENDENT CLAIM 9

Claim 9	
9. The method of claim 8, further comprising: providing a first controller device that configures the first DRR device in response to a power-on event, the first controller device retrieving the transmit filter coefficient values from an internal nonvolatile memory as part of said configuring.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 9	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 9	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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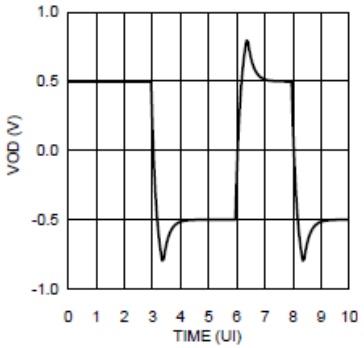
Claim 9	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 9	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 9	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 9	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 9	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 9	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 9	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 9	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 9	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 9	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 9	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

Claim 9	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

Claim 9	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 9	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

J. DEPENDENT CLAIM 10

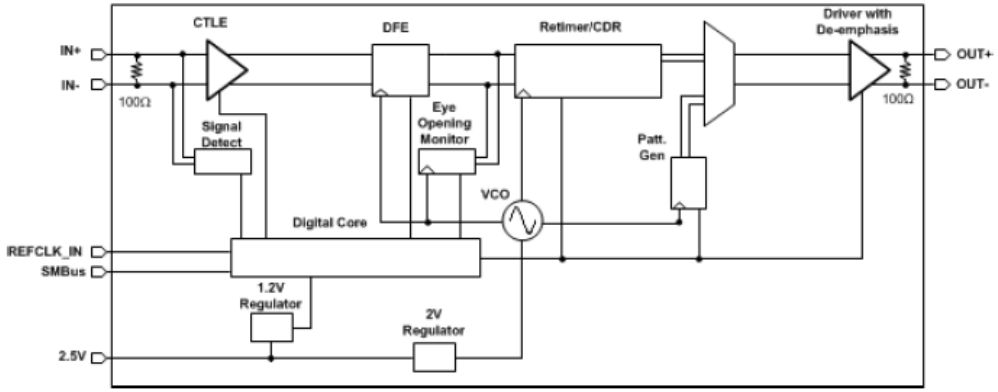
Claim 10	
10. The method of claim 8, further comprising: programming the first and second DRR devices to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 10	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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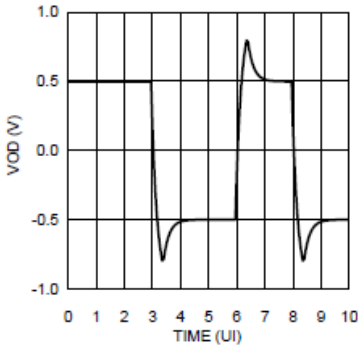
Claim 10	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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Claim 10	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 10	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 10	
272	**7.3.5 Clock and Data Recovery** The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

Claim 10	
273	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

Claim 10	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 10	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 10	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 10	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 10	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 10	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 10	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

Claim 10	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 10	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

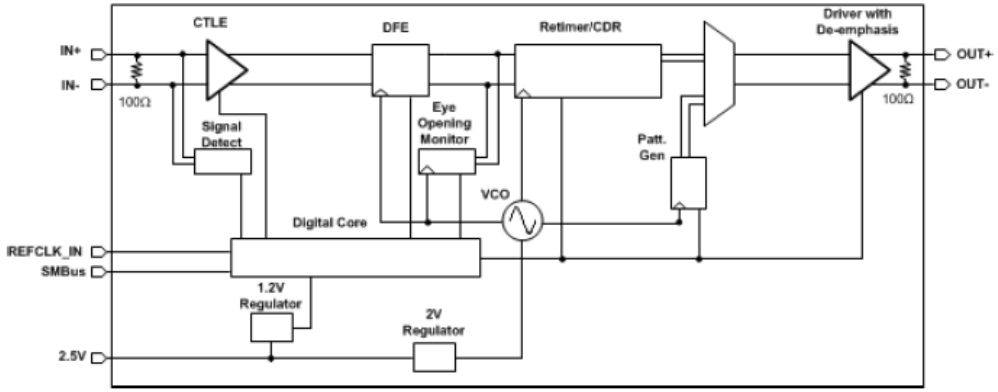
Claim 10	
	DS125DF410, 44.

K. DEPENDENT CLAIM 11

Claim 11	
11. The method of claim 10, further comprising: after connecting the electrical conductors, characterizing channel characteristics of the electrical conductors to determine the transmit filter coefficient values; and storing the transmit filter coefficient values in the nonvolatile memories.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 11	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 11	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

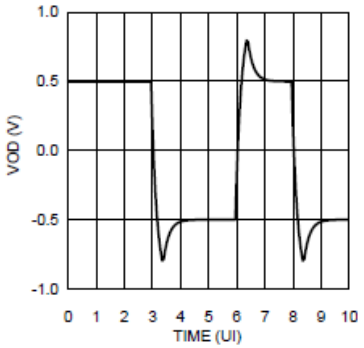
Claim 11	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 11	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 11	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 11	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 11	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 11	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 11	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 11	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 11	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 11	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 11	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 11	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 11	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 11	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

L. DEPENDENT CLAIM 12

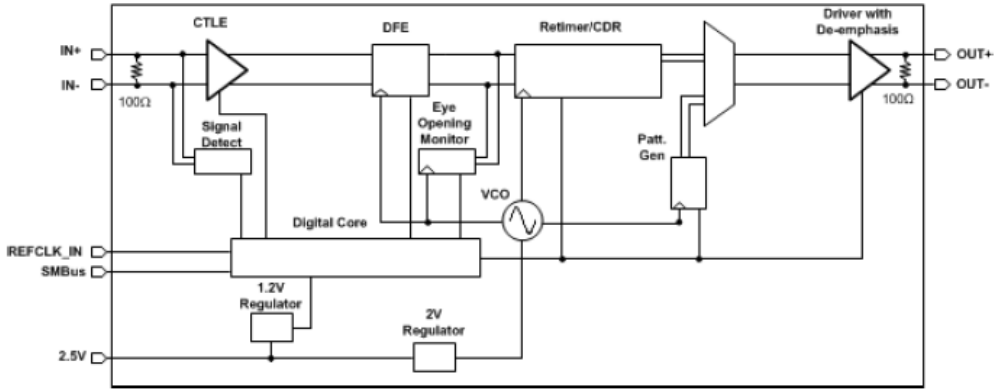
Claim 12	
12. The method of claim 11, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 12	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 12	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

301

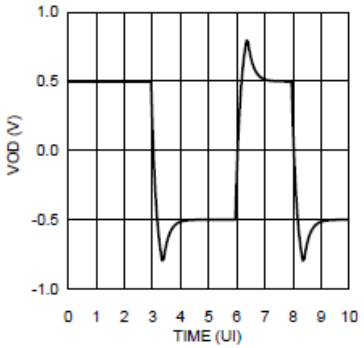
Claim 12	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 12	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 12	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 12	
305	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

Claim 12	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 12	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 12	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 12	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 12	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 12	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 12	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 12	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 12	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

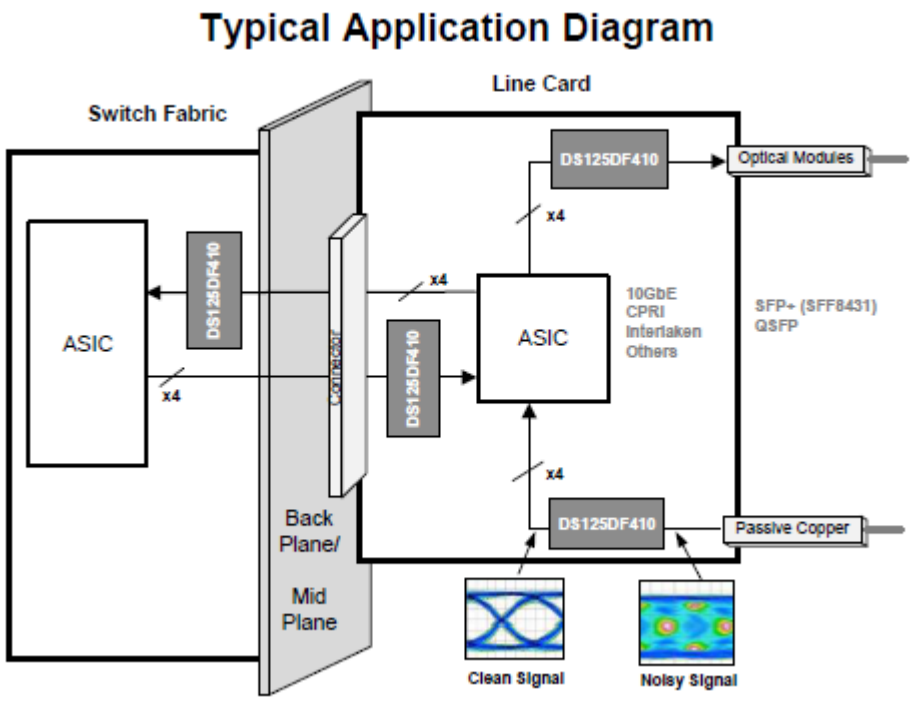
Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 12	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

M. DEPENDENT CLAIM 13

Claim 13	
13. The method of claim 11, wherein the electrical conductors comprise twin-axial conductors that carry each of the electrical transit signals in differential form.	DS125DF410 discloses and/or renders obvious this limitation.

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Claim 13	
	 DS125DF410, 1.

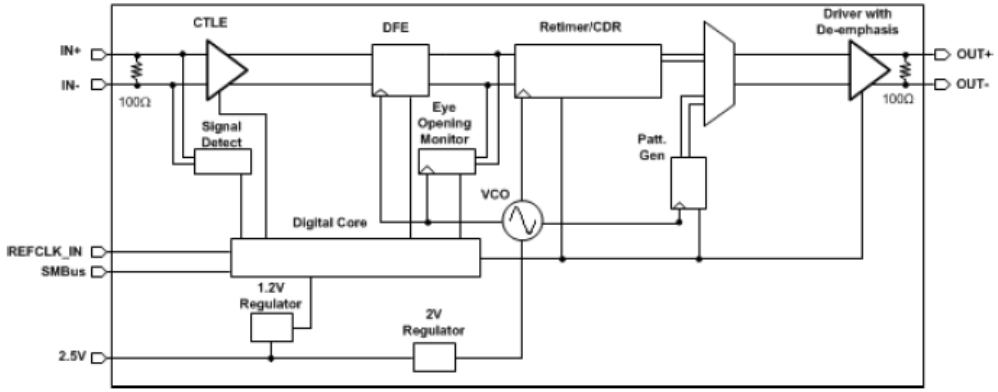
316

Claim 13	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 13	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

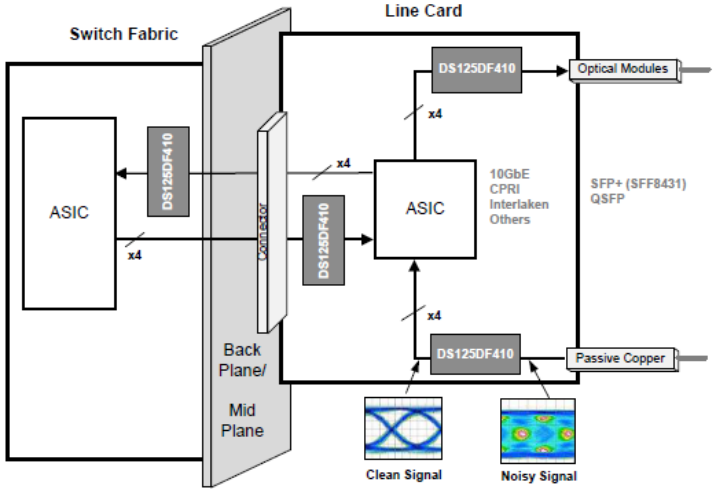
318

Claim 13	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

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Claim 13	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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Claim 13	
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

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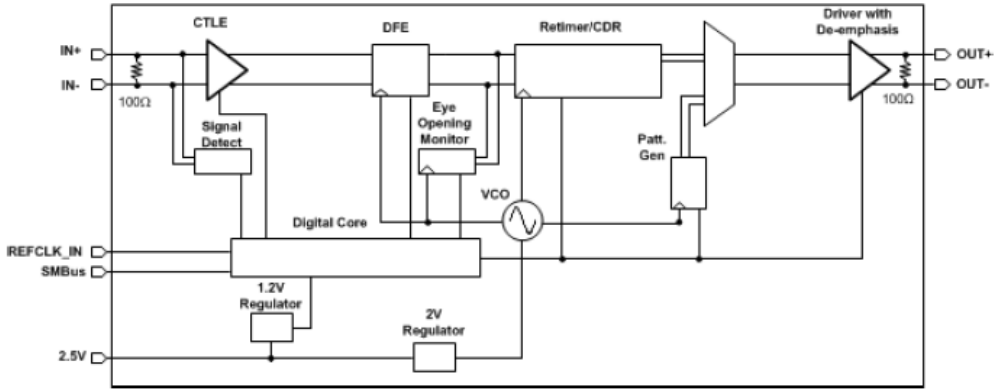
N. DEPENDENT CLAIM 14

Claim 14	
14. The method of claim 8, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 14	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 14	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

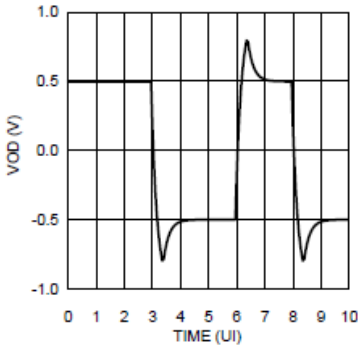
Claim 14	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 14	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 14	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 14	
328	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

Claim 14	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 14	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 14	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 14	

DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 14	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 14	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 14	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 14	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 14	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

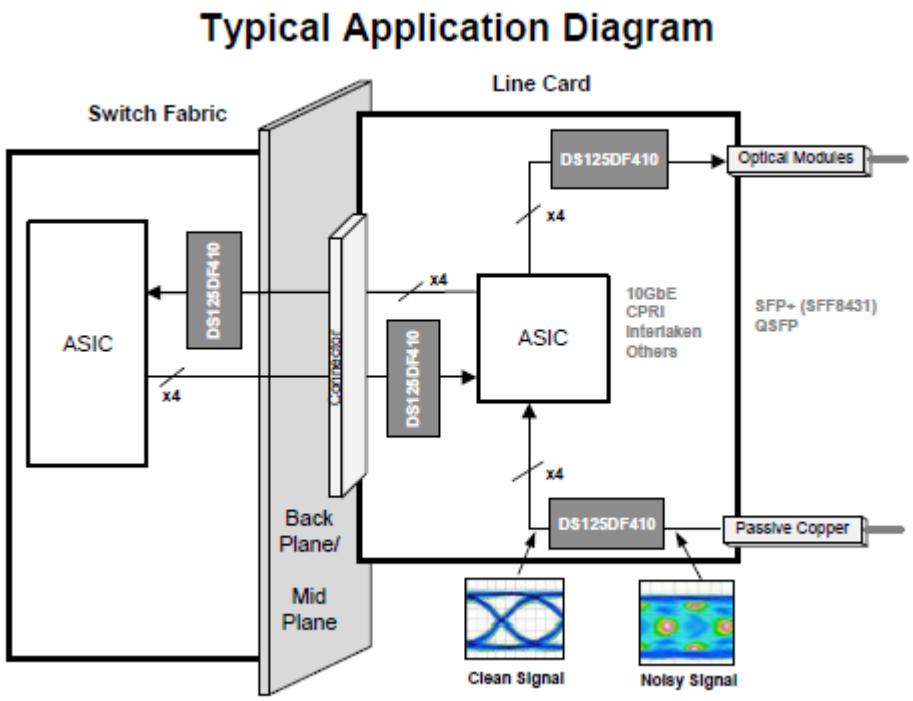
Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 14	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

O. INDEPENDENT CLAIM 15

Claim 15	
15[pre] A communications method that comprises:	To the extent the preamble is limiting, DS125DF410 discloses and/or renders obvious this limitation.

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Claim 15	
	 DS125DF410, 1.

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Claim 15	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 15	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

Claim 15	

7.1 Overview

The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes.

The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM.

The sections below describe the functionality of the various circuits and features within the DS125DF410.

7.2 Functional Block Diagram

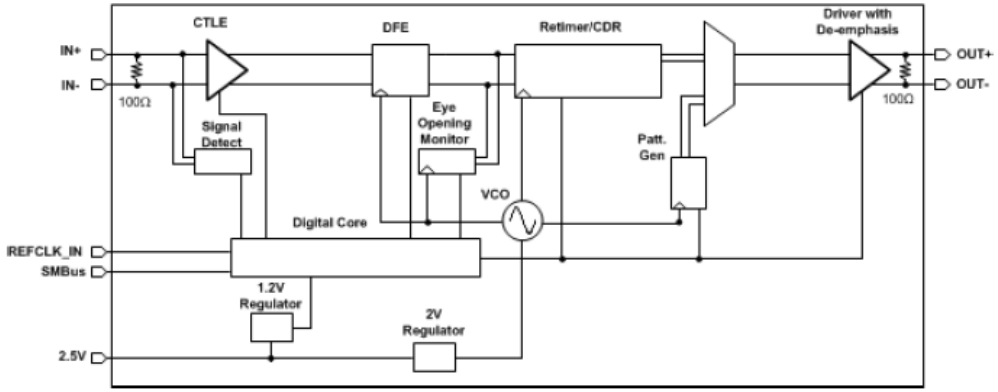


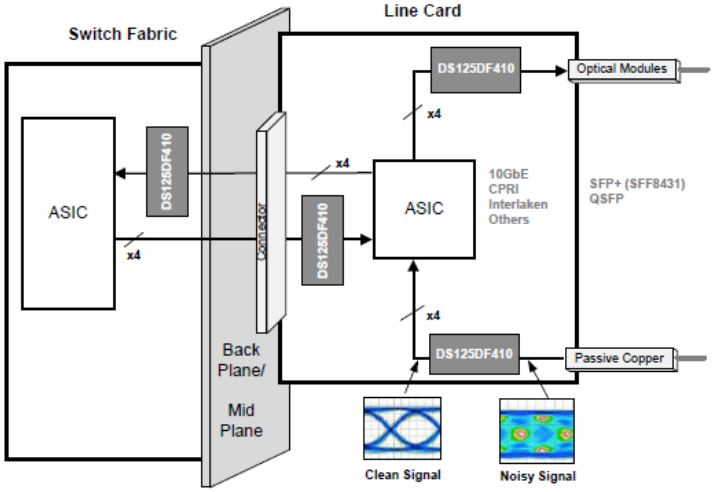
Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels

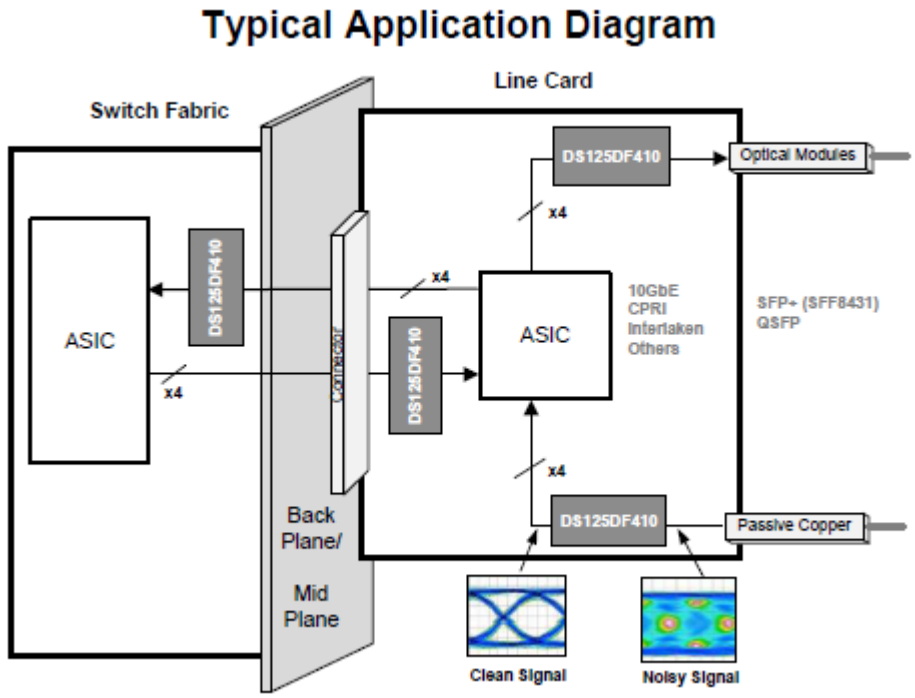
DS125DF410, 8.

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Claim 15	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30.

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Claim 15	
	8.2 Typical Application Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this preamble is not disclosed, either explicitly or inherently, by DS125DF410, this preamble is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.
15[a] inserting a first end connector plug of a cable into a first host interface port, the first end connector plug being	DS125DF410 discloses and/or renders obvious this limitation.

Claim 15	
connected to a first data recovery and re-modulation (DRR) device that converts a multi-lane data stream from the first host interface port into electrical transit signals conveyed by electrical conductors to a second DRR device connected to a second end connector plug of the cable; and	 DS125DF410, 1.

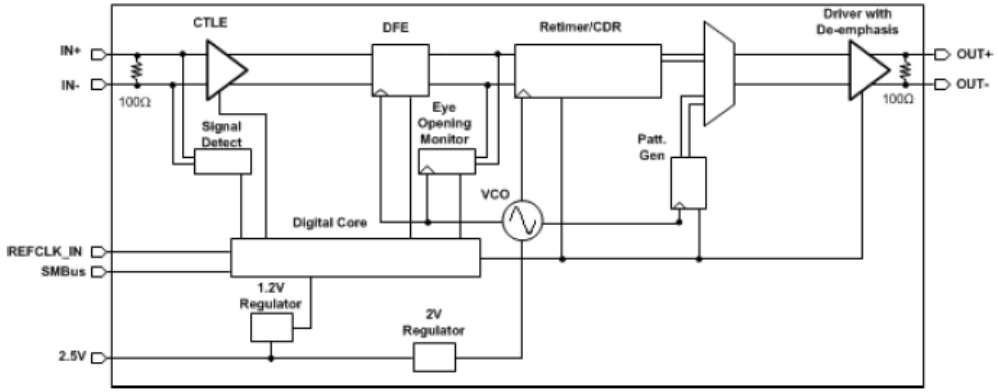
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Claim 15	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 15	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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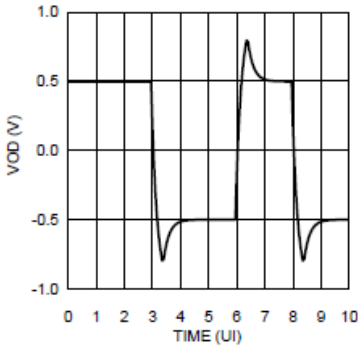
Claim 15	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

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Claim 15	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 15	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 15	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 15	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 15	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 15	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 15	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 15	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

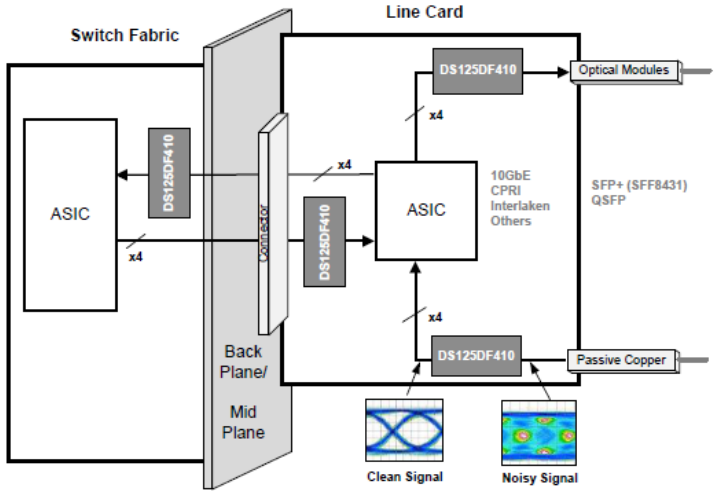
359

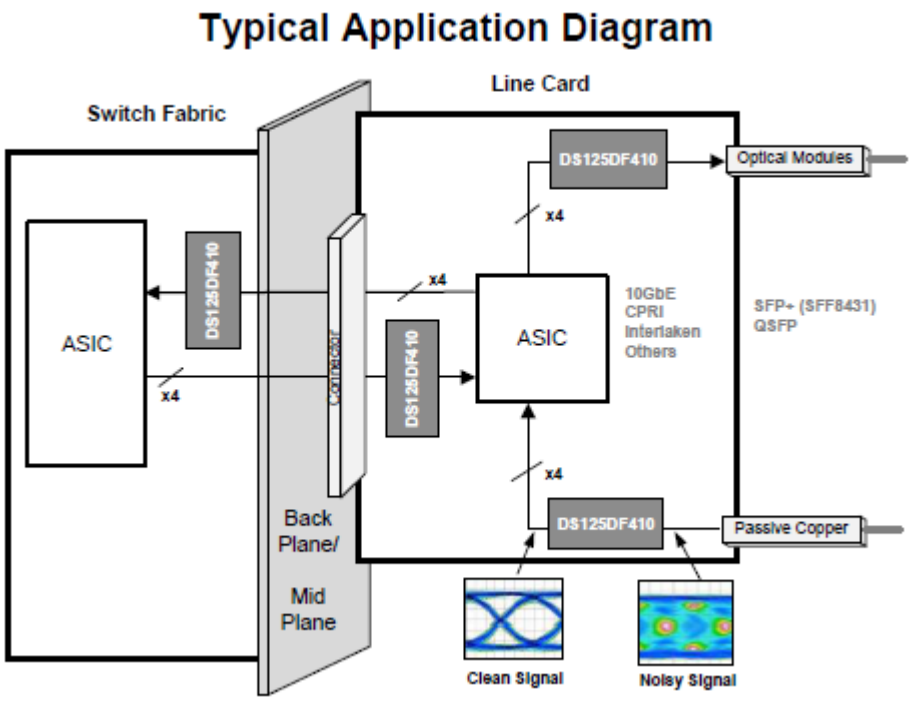
Claim 15	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

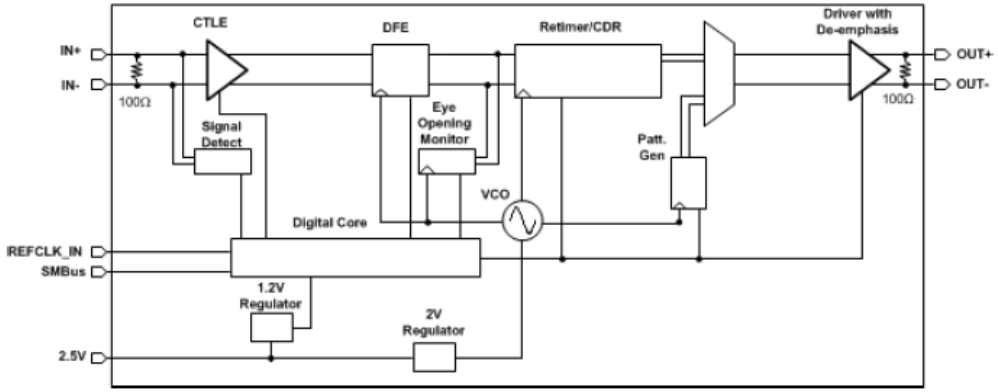
Claim 15	
	DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50.
15[b] inserting the second end connector plug of the cable into a second host interface port, the second DRR device converting a multi-lane data stream from the second host interface port into electrical transit signals conveyed by electrical conductors to the first DRR device,	DS125DF410 discloses and/or renders obvious this limitation.

Claim 15	
	 DS125DF410, 1. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Claim 15	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 15	
	2 Applications • Front Port SFF 8431 (SFP+) Optical and Direct Attach Copper • Backplane Reach Extension, Data Retimer • Ethernet: 10 GbE, 1 GbE • CPRI: Line Bit Rate Options 3–7 • Interlaken: All Lane Bit Rates • InfiniBand • Other Propriety Data Rates up to 12.5 Gbps DS125DF410, 1. **3 Description** The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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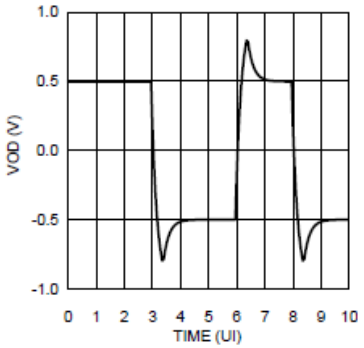
Claim 15	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 15	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 15	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 15	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 15	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 15	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 15	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 15	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 15	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

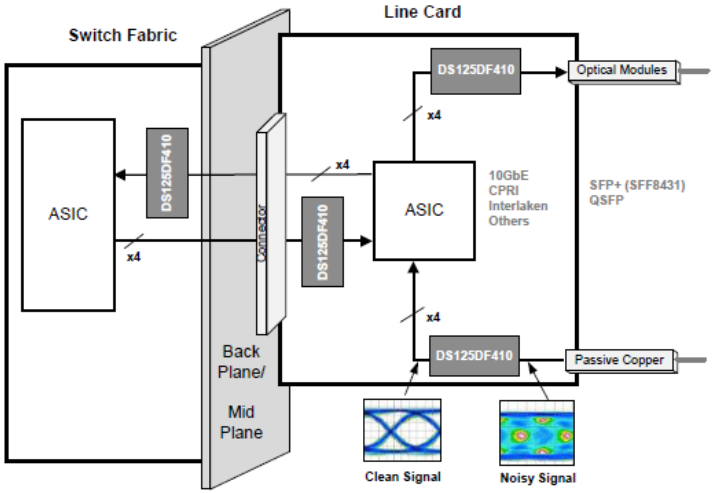
DS125DF410, 41.

Claim 15	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

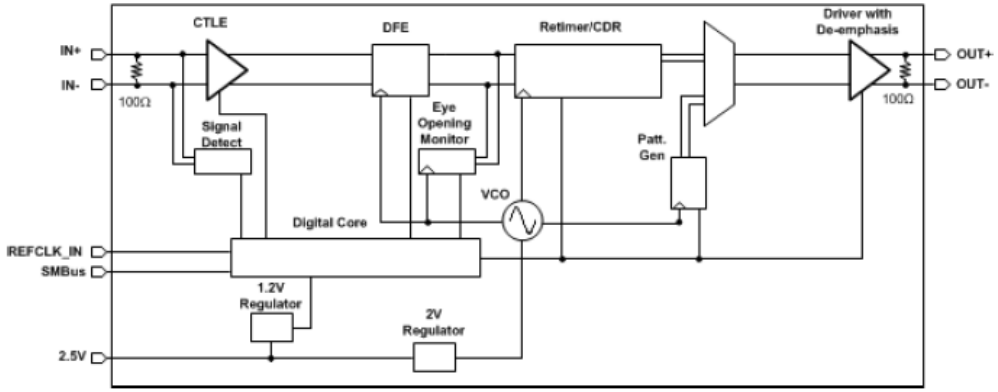
Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 15	
	DS125DF410, 44. **8.2 Typical Application** Figure 6 shows a typical system implementation, where the DS125DF410 is used both on the backplane and port side.  **Figure 6. Typical Application Diagram** DS125DF410, 50. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Claim 15	
15[c] the first and second DRR devices providing pre-equalization of the electrical transit signals using transmit filter coefficient values stored in nonvolatile memories.	**1 Features** • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 15	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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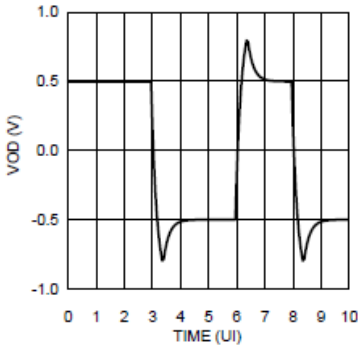
Claim 15	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 15	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 15	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 15	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 15	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 15	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 15	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 15	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 15	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 15	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

Claim 15	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 15	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

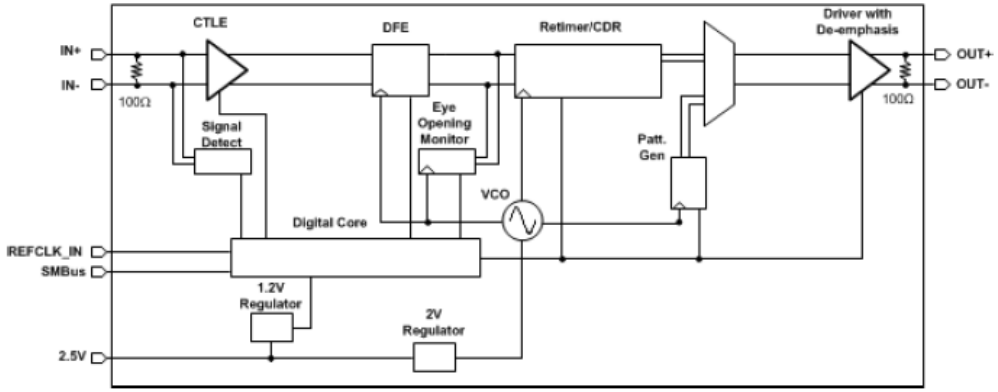
P. DEPENDENT CLAIM 16

Claim 16	
16. The method of claim 15, further comprising: supplying power to the first and second end connector plugs, the first and second end connector plugs being connected to first and second controller devices, respectively, each of the first and second controller devices operating to configure the first and second DRR devices in response to a power-on event, the configuring including retrieving the transmit filter coefficient values from internal nonvolatile memory.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 16	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 16	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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Claim 16	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

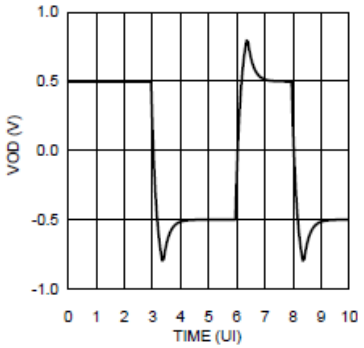
397

Claim 16	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 16	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 16	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 16	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 16	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 16	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 16	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 16	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 16	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 16	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 16	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 16	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

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Claim 16	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

Q. DEPENDENT CLAIM 17

Claim 17	
17. The method of claim 15, wherein the first and second DRR devices are programmed to use the transmit coefficient values each time power is supplied to the first and second end connector plugs.	DS125DF410 discloses and/or renders obvious this limitation.

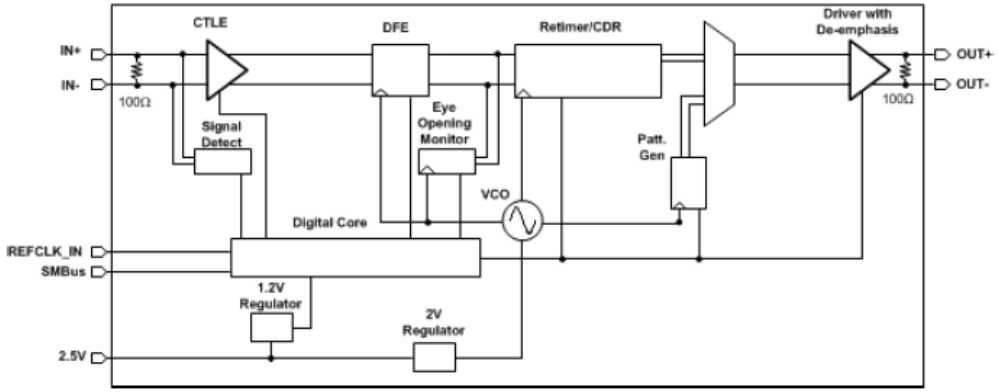
410

Claim 17	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 17	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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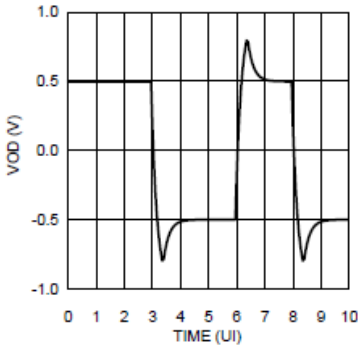
Claim 17	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 17	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 17	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 17	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 17	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

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Claim 17	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 17	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 17	

DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 17	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 17	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 17	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 17	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 17	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 17	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

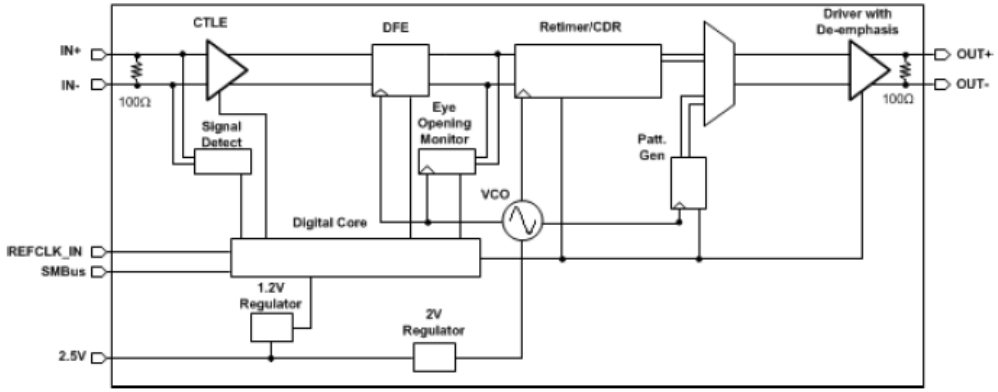
R. DEPENDENT CLAIM 18

Claim 18	
18. The method of claim 17, wherein the transmit filter coefficient values are determined and stored in the nonvolatile memories after assembly of the cable.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 18	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

Claim 18	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

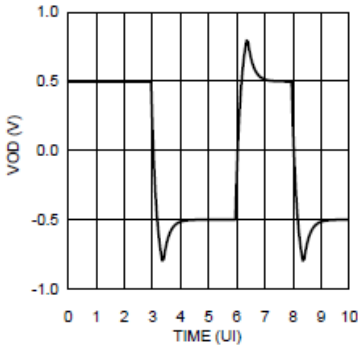
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Claim 18	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

Claim 18	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 18	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 18	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

Claim 18	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 18	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 18	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 18	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 18	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 18	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 18	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Claim 18	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 18	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 18	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

S. DEPENDENT CLAIM 19

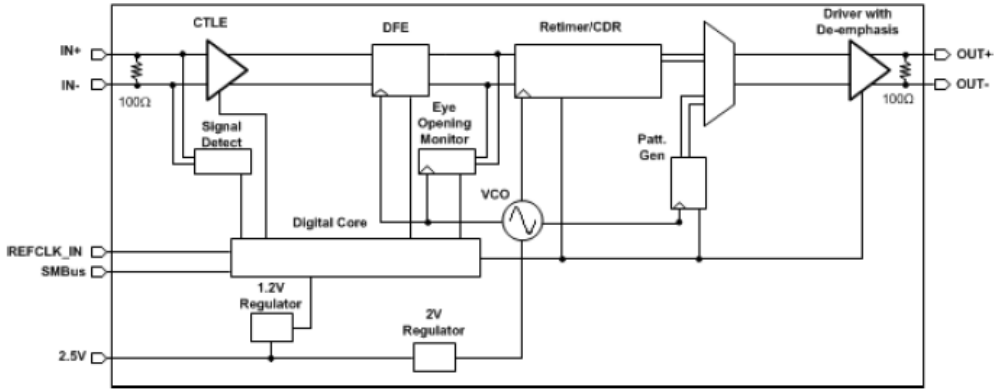
Claim 19	
19. The method of claim 18, wherein the first and second DRR devices employ receiver-based equalization of the electrical transit signals using coefficient values stored in the nonvolatile memories.	DS125DF410 discloses and/or renders obvious this limitation.

Claim 19	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 19	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

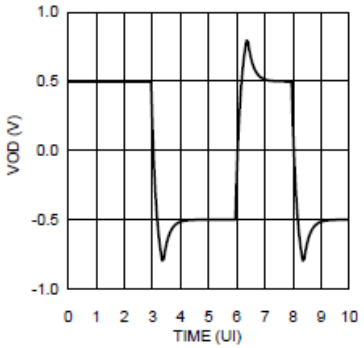
444

Claim 19	
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Claim 19	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

Claim 19	
	7.3.5 Clock and Data Recovery The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

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Claim 19	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 19	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 19	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 19	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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Claim 19	
	DS125DF410, 31

7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

Claim 19	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

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Claim 19	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

DS125DF410, 39.

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Claim 19	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

Claim 19	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

DS125DF410, 41.

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Claim 19	

2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 19	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.

T. DEPENDENT CLAIM 20

Claim 20	
20. The method of claim 15, wherein the first and second DRR devices do not perform pre-equalization of the multi-lane data streams provided to the first and second host interface ports.	DS125DF410 discloses and/or renders obvious this limitation.

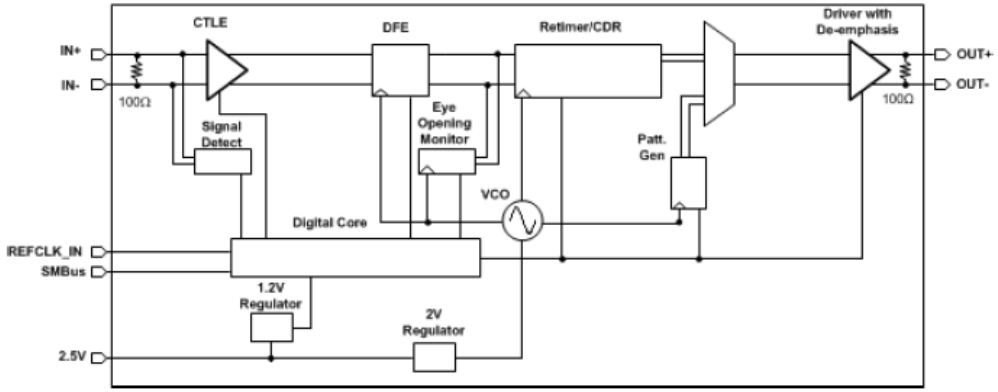
458

Claim 20	
	1 Features • Each Channel Independently Locks to Data Rates from 9.8 to 12.5 Gbps and Submultiples • Fast Lock Operation Based on Protocol-Select Mode • Low Latency (~300ps) • Adaptive Equalization up to 34-dB Boost at 5 GHz • Adjustable Transmit V_{OD}: 600 to 1300 mVp-p • Adjustable Transmit De-emphasis to –15 dB • Typical Power Dissipation (EQ+DFE+CDR+DE): 180 mW/Channel • Programmable Output Polarity Inversion • Input Signal Detection, CDR Lock Detection/Indicator • On-Chip Eye Monitor (EOM), PRBS Generator • Single 2.5-V ± 5% Power Supply • SMBus/EEPROM Configuration Modes • Operating Temperature Range of –40 to 85°C • WQFN 48-Pin 7-mm x 7-mm Package • Easy Pin Compatible Upgrade Between Repeater and Retimers – DS100RT410 (EQ+CDR+DE): 10.3125 Gbps – DS100DF410 (EQ+DFE+CDR+DE): 10.3125 Gbps – DS110RT410 (EQ+CDR+DE): 8.5–11.3 Gbps – DS110DF410 (EQ+DFE+CDR+DE): 8.5–11.3 Gbps – DS125RT410 (EQ+CDR+DE): 9.8–12.5 Gbps – DS125DF410 (EQ+DFE+CDR+DE): 9.8–12.5 Gbps – DS100BR410 (EQ+DE): Up to 10.3125 Gbps DS125DF410, 1.

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Claim 20	
	3 Description The DS125DF410 is four channel retimer with integrated signal conditioning. The device includes a fully adaptive Continuous-Time Linear Equalizer (CTLE), self calibrating 5-tap Decision Feedback Equalizer (DFE), Clock and Data Recovery (CDR), and transmit De-Emphasis (DE) driver to enable data transmission over long, lossy and crosstalk-impaired highspeed serial links to achieve BER < 1×10^{-15}. Each channel can independently lock to data rate from 9.8 to 12.5 Gbps, and associated sub rates (div by 2, 4 and 8) to support a variety of communication protocols. A 25 MHz crystal oscillator clock is used to speed up the CDR lock process. This clock is not used for training the PLL and does not need to be synchronous with the serial data. The programmable settings can be applied using the SMBus (I2C) interface, or they can be loaded via an external EEPROM. An on-chip eye monitor and a PRBS generator allow real-time measurement of high-speed serial data for system bring-up or field tuning. DS125DF410, 1.

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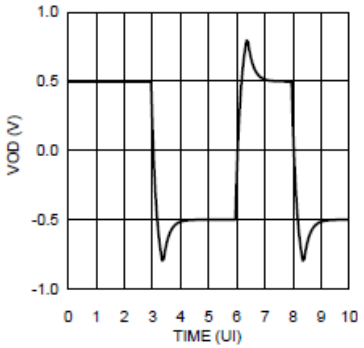
Claim 20	
	7.1 Overview The DS125DF410 is a multi-rate, 4-channel retimer. Each channel in the DS125DF410 operates independently. All channels include a Continuous Time Linear Equalizer (CTLE), Decision Feedback Equalizer (DFE), Clock and Data Recovery circuit (CDR) and a differential driver with programmable output voltage and de-emphasis. Each channel also has its own Eye Opening Monitor (EOM) and configurable Pseudo-Random Bit Sequence (PRBS) pattern generator that can be used for debug purposes. The DS125DF410 is configurable through a single SMBus port. The DS125DF410 can also act as an SMBus master to configure itself from an EEPROM. The sections below describe the functionality of the various circuits and features within the DS125DF410. **7.2 Functional Block Diagram**  **Figure 3. DS125DF410 Data Path Block Diagram — One of Four Channels** DS125DF410, 8.

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Claim 20	
	7.3.3 CTLE The CTLE in the DS125DF410 is a fully adaptive equalizer with optional limiting stage. The CTLE adapts according to a Figure of Merit (FOM) calculation during the lock acquisition process. Once the CDR has locked and the CTLE has been adapted, the CTLE boost level will be frozen until a manual re-adapt command is issued or until the CDR re-enters the lock acquisition state. The CTLE is typically readapted by resetting the CDR. The CTLE consists of 4 stages, with each stage having 2-bit boost control. This allows for 256 different stage-boost combinations. The CTLE adaption algorithm allows the CTLE to adapt through 32 of these stage-boost combinations. These 32 stage-boost combinations comprise the EQ Table in the channel registers; see channel registers 0x40 through 0x5F. This EQ Table can be reprogrammed to support up to 32 of the 256 stage-boost settings. CTLE boost levels are determined by summing the boosts levels of the 4 stages. Different stage-boost combinations that sum to the same number will have approximately the same boost level, but will result in a different shape for the EQ transfer function (boost curve). The fourth stage in the CTLE can be programmed through the SMBus interface to become a limiting stage rather than a linear stage. This is useful in some applications, but it should not be typically used in combination with the DFE. DS125DF410, 10. **7.3.4 DFE** A 5-tap DFE can be enabled within the data path of each channel to assist with reducing the effects of cross talk, reflections, or post cursor inter-symbol interference (ISI). The DFE must be manually enabled, regardless of the selected adapt mode. The DFE can be manually configured to specified tap polarities and tap weights. The DFE taps are all feedback taps with 1UI spacing. Each tap has a specified boost weight range and polarity bit. DS125DF410, 10.

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Claim 20	
463	**7.3.5 Clock and Data Recovery** The DS125DF410 performs its clock and data recovery function by detecting the bit transitions in the incoming data stream and locking its internal VCO to the clock represented by the mean arrival times of these bit transitions. This process produces a recovered clock with greatly reduced jitter at jitter frequencies outside the bandwidth of the CDR Phase-Locked Loop (PLL). This is the primary benefit of using the DS125DF410 in a system. It significantly reduces the jitter present in the data stream, in effect resetting the jitter budget for the system. The DS125DF410 uses the 25 MHz reference to determine the coarse tuning setting for its internal VCO. On power-up, on CDR reset, and when the DS125DF410 loses lock and cannot re-acquire lock after four attempts, the 25 MHz reference is used to calibrate the VCO frequency. The required VCO frequency is set by using the rate/subrate settings (see Table 2) or by manually setting the PPM count and divide ratio. To calibrate the VCO frequency, the DS125DF410 searches through the available VCO coarse tuning settings and counts the divided VCO frequency using the 25 MHz reference as a clock source. The VCO coarse tuning setting which provides the VCO frequency closest to the required frequency is stored, and this coarse tuning setting is used for subsequent operation. This produces a fast, robust phase lock to the input signal. DS125DF410, 10. **7.3.6 Output Driver** The output driver is capable of driving variable output voltages with variable amounts of analog de-emphasis. The output voltage and de-emphasis level can be configured by writing registers over the SMBus. The DS125DF410 cannot determine independently the appropriate output voltage or de-emphasis setting, so the user is responsible for configuring these parameters. They can be set for each channel independently. An idealized transmit waveform with analog de-emphasis applied is shown in Figure 4.

Claim 20	
	 **Figure 4. Idealized De-Emphasis Waveform** DS125DF410, 10-11. ***7.4.4.6 Driver Output De-Emphasis*** The output de-emphasis level of the DS125DF410 can be configured from a nominal setting of 0 dB to a nominal setting of -15 dB depending upon the application. Larger absolute values of the de-emphasis setting provide more pre-distortion of the output driver waveform, accentuating the high-frequency components of the output driver waveform relative to the low-frequency components. Greater values of de-emphasis can compensate for greater dispersion in the transmission media at the output of the DS125DF410. The output de-emphasis level as set is the typical value to which the output signal will settle following the de-emphasis pulse interval in dB relative to the output VOD. DS125DF410, 17.

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Claim 20	
	7.5.8 Overriding the CTLE Boost Setting *Register 0x03, Register 0x13, bit 2, and Register 0x3a* To override the CTLE boost settings, register 0x03 is used. This register contains the currently-applied CTLE boost settings. The boost values can be overridden by using the two-bit fields in this register as shown in the table. The final stage of the CTLE has an additional control bit which sets it to a limiting mode. For some channels, this additional setting improves the bit error rate performance. This bit is bit 2 of register 0x13. If the DS125DF410 loses lock because of a change in the CTLE settings, the DS125DF410 will initiate its lock and adaptation sequence again. Thus, if you write new CTLE boost values to register 0x03 and 0x13 which cause the DS125DF410 to drop out of lock, the DS125DF410 may, in the process of reacquiring the CDR lock, reset the CTLE settings to different values than those you set in register 0x03 and 0x13. If this behavior is not understood, it can appear that the DS125DF410 did not accept the values you wrote to the CTLE boost registers. What's really happening, however, is that the lock and adaptation sequence is overriding the CTLE values you wrote to the CTLE boost registers. This will not happen unless the DS125DF410 drops out of lock. if the adapt mode is set to 0 (bits 6:5 of channel register 0x31), then the CTLE boost values will not be overridden, but the DS125DF410 may still lose lock. If this happens, the DS125DF410 will attempt to reacquire lock. if the reference mode is set appropriately, and if the rate/subrate code is set to permit it, the DS125DF410 will begin searching for CDR lock at the highest allowable VCO divider ratio – that is, at the lowest configured bit rate. At divider values of 4 and 8, the CTLE boost settings used will come not from the values in register 0x03, and 0x13, but rather from register 0x3a, the fixed CTLE boost setting for lower data rates. This setting will be written into boost setting register 0x03 during the lock search process. This value may be different from the value you set in register 0x03, so, again, it may appear that the DS125DF410 has not accepted the CTLE boost settings you set in registers 0x03 and 0x13. The interactions of the lock and adaptation sequences with the manually-set CTLE boost settings can be difficult to understand. To manually override the CTLE boost under all conditions, perform the following steps. 1. Set the DS125DF410 channel adapt mode to 0 by writing 0x0 to bits 6:5 of channel register 0x31. 2. Set the desired CTLE boost setting in register 0x3a. If the DS125DF410 loses lock and attempts to lock to a lower data rate, it will use this CTLE boost setting. 3. Set the desired CTLE boost setting in register 0x03. 4. Set the desired CTLE boost setting in register 0x40. 5. If desired, set the CTLE stage 3 limiting bit, bit 2 of register 0x13. If the DS125DF410 loses lock when the CTLE boost settings are set according to the sequence above, the DS125DF410 will try to reacquire lock, but it will not change the CTLE boost settings in order to do so. DS125DF410, 21.

Claim 20	
	7.5.14 Overriding the DFE Tap Weights and Polarities *Register 0x11, bits 3:0, Register 0x12, bit 7 and bits 4:0, Register 0x15, bit 7, Register 0x1e, bit 3, Register 0x20, Register 0x21, Register 0x23, bit 6, Register 0x2f, bit 0, and Registers 0x71–0x75* For the DS125DF410 the DFE tap weights and polarities are normally set automatically by the adaptation procedure. These values can be overridden by the user if desired. Prior to overriding the DFE tap weights and polarities, the dfe_ov bit, bit 6 of register 0x23, should be set. This bit is set by default. In order for the DFE tap weights and polarities to be applied to the input signal, bit 3 of register 0x1e, the dfe_PD bit, must be set to 0. It is necessary to change the default settings of these registers, because the DFE is powered down by default. It is also necessary to set bit 7 of register 0x15 in order to manually set the DFE tap weights. This bit is cleared by default. Bits 4:0 of register 0x12 set the five-bit weight for DFE tap 1. The first DFE tap has a five-bit setting, while the other taps are set using four bits. Often the first DFE tap has the largest effect in improving the bit error rate of the system, which is why this tap has a five-bit weight setting. DS125DF410, 28. **7.5.17 Overriding the Figure of Merit for Adaptation** *Register 0x2c, bits 5:4, Register 0x31, bits 6:5, Register 0x6b, Register 0x6c, Register 0x6d, and Register 0x6e, bits 7 and 6* The default figure of merit for both the CTLE and DFE adaptation in the DS125DF410 is simple. The horizontal and vertical eye openings are measured for each CTLE boost setting or set of DFE tap weights and polarities. The vertical eye opening is scaled to a constant reference vertical eye opening and the smaller of the horizontal or vertical eye opening is taken as the figure of merit for that set of equalizer settings. The objective is to adapt the equalizer to a point where the horizontal and vertical eye openings are both as large as possible. This usually provides optimum bit error rate performance for most transmission channels. In some systems the adaptation can reach a better setting if only the horizontal or vertical eye opening is used to compute the figure of merit rather than using both. This will be system-dependent and the user must determine through experiment whether this provides better adaptation in the user's system. For the DS125DF410, the DFE figure of merit type can be set using register 0x2c, bits 5:4. The value of this two-bit field versus the configured figure of merit type is shown in Table 9. DS125DF410, 29.

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Claim 20	
	7.5.19 Setting the Adaptation/Lock Mode *Register 0x31, bits 6:5, and Register 0x33, bits 7:4 and 3:0, Register 0x34, bits 3:0, Register 0x35, bits 4:0, Register 0x3e, bit 7, and Register 0x6a* There are four adaptation modes available in the DS125DF410. • Mode 0: The user is responsible for setting the CTLE and DFE values. This mode is used if the transmission channel response is fixed. • Mode 1: Only the CTLE is adapted to equalize the transmission channel. The DFE is enabled, but the tap weights are all set to 0. This mode is primarily used for smoothly-varying high-loss transmission channels such as cables and simple PCB traces. • Mode 2: In this mode, both the CTLE and the DFE are adapted to compensate for additional loss, reflections, and crosstalk in the input transmission channel. – The maximum DFE tap weights can be constrained using register 0x34, bits 3:0, and register 0x35, bits 4:0 as shown in Table 16. • Mode 3: In this mode, both the CTLE and DFE are adapted as in mode 2. However, in mode 3, more emphasis is placed on the DFE setting. This mode may give better results for high crosstalk transmission channels. DS125DF410, 30. **7.5.22 Overriding the CTLE Settings Used for CTLE Adaptation** *Register 0x2c, bits 3:0, Register 0x2f, bit 3, Register 0x39, bits 4:0, and Registers 0x50-0x5f* The CTLE adaptation algorithm operates by setting the CTLE boost stage controls to a set of pre-determined boost settings, each of which provides progressively more high-frequency boost. At each stage in the adaptation process, the DS125DF410 attempts to phase lock to the equalized signal. If the phase lock succeeds, the DS125DF410 measures the horizontal and vertical eye openings using the internal eye monitor circuit. The DS125DF410 computes a figure of merit for the eye opening and compares it to the previous best value of the figure of merit. While the figure of merit continues to improve, the DS125DF410 continues to try additional values of the CTLE boost setting until the figure of merit ceases to improve and begins to degrade. When the figure of merit starts to degrade, the DS125DF410 still continues to try additional CTLE settings for a pre-determined trial count called the "look-beyond" count, and if no improvement in the figure of merit results, it resets the CTLE boost values to those that produced the best figure of merit. The resulting CTLE boost values are then stored in register 0x03. The "look-beyond" count is configured by the value in register 0x2c, bits 3:0. The value is 0x2 by default. The set of boost values used as candidate values during CTLE adaptation are stored as bit fields in registers 0x40-0x5f. The default values for these settings are shown in Table 11. These values may be overridden by setting the corresponding register values over the SMBus. If these values are overridden, then the next time the CTLE adaptation is performed the set of CTLE boost values stored in these registers will be used for the adaptation. Resetting the channel registers by setting bit 2 of channel register 0x00 will reset the CTLE boost settings to their defaults. So will power-cycling the DS125DF410.

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7.5.24 Setting the Output De-Emphasis Setting

Register 0x15, bits 2:0 and bit 6

Fifteen output de-emphasis settings are available in the DS125DF410, ranging from 0 dB to -15 dB. The de-emphasis values come from register 0x15, bits 2:0, which make up the bit field dvr_dem<2:0>, and register 0x15, bit 6, which is the third de-emphasis setting bit.

The available driver de-emphasis settings and the mapping to these bits are shown in Table 13.

Table 13. Driver De-Emphasis Settings

Register 0x15, Bit 2, dvr_dem[2]	Register 0x15, Bit 1, drv_dem[1]	Register 15, Bit 0, drv_dem[0]	Register 0x15, Bit 6, drv_dem_range	De-emphasis Setting (dB)
0	0	0	X	0.0
0	0	1	1	–1.5
0	0	1	0	–2.0
0	1	0	1	–3.5
0	1	0	0	–4.2
0	1	1	1	–5.0
0	1	1	0	–6.0
1	0	0	1	–6.5
1	0	0	0	–7.2
1	0	1	1	–8.0
1	0	1	0	–9.0
1	1	0	1	–9.5
1	1	0	0	–11.0
1	1	1	1	–13.0
1	1	1	0	–15.0

DS125DF410, 33.

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Claim 20	
	7.6.1 Register Information There are two types of device registers in the DS125DF410. These are the control/shared registers and the channel registers. The control/shared registers control or allow observation of settings which affect the operation of all channels of the DS125DF410. They are also used to select which channel of the device is to be the target channel for reads from and writes to the channel registers. The channel registers are used to set all the configuration settings of the DS125DF410. They provide independent control for each channel of the DS125DF410 for all the settable device characteristics. Any registers not described in the tables that follow should be treated as reserved. The user should not try to write new values to these registers. The user-accessible registers described in the tables that follow provide a complete capability for customizing the operation of the DS125DF410 on a channel-by-channel basis. DS125DF410, 33.

Claim 20	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
11	7	0	RW	Y	EOM_SEL_VRANGE[1]	Manually set the EOM vertical range, used with channel register 0x2C[6]: 00: ±100 mV 01: ±200 mV 10: ±300 mV 11: ±400 mV
	6	0	RW	Y	EOM_SEL_VRANGE[0]	
	5	1	RW	Y	EOM_PD	1: Normal operation
	4	0	RW	N	RESERVED	
	3	0	RW	Y	DFE_TAP2_POL	Bit forces DFE tap 2 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	2	0	RW	Y	DFE_TAP3_POL	Bit forces DFE tap 3 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	1	0	RW	Y	DFE_TAP4_POL	Bit forces DFE tap 4 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	0	0	RW	Y	DFE_TAP5_POL	Bit forces DFE tap 5 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
12	7	1	RW	Y	DFE_TAP1_POL	Bit forces DFE tap 1 polarity 1: Negative, boosts by the specified tap weight 0: Positive, attenuates by the specified tap weight
	6	1	RW	N	RESERVED	
	5	1	RW	Y	DFE_SEL_NEG_GM	
	4	0	RW	Y	DFE_WT1[4]	Bits force DFE tap 1 weight, manual DFE operation required to take effect
	3	0	RW	Y	DFE_WT1[3]	
	2	0	RW	Y	DFE_WT1[2]	
	1	0	RW	Y	DFE_WT1[1]	
	0	0	RW	Y	DFE_WT1[0]	

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Claim 20	

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
15	7	0	RW	Y	DFE_FORCE_EN	Enables manual DFE tap settings
	6	0	RW	Y	drv_dem_range	Driver De-emphasis Range
	5	0	RW	Y	RESERVED	
	4	1	RW	Y	RESERVED	
	3	0	RW	N	DRV_PD	1: Powers down the high speed driver 0: Normal operation
	2	0	RW	Y	DRV_DEM2	Driver De-emphasis Setting[2:0]
	1	0	RW	Y	DRV_DEM1	
	0	0	RW	Y	DRV_DEM0	

DS125DF410, 40.

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Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
1F	7	0	RW	Y	RESERVED	
	6	1	RW	Y	LPF_EN_150	When reg_0A[4]=1, this bit will change the loop filter resistance. 1 - 1500 Ω 0 - 750 Ω
	5	0	RW	N	RESERVED	
	4	1	RW	N	lpf_dac_val[4]	lpf_dac_val over-ride
	3	0	RW	N	lpf_dac_val[3]	lpf_dac_val over-ride
	2	1	RW	N	lpf_dac_val[2]	lpf_dac_val over-ride
	1	0	RW	N	lpf_dac_val[1]	lpf_dac_val over-ride
	0	1	RW	N	lpf_dac_val[0]	lpf_dac_val over-ride
20	7	0	RW	Y	DFE_WT5[3]	Bits force DFE tap 5 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT5[2]	
	5	0	RW	Y	DFE_WT5[1]	
	4	0	RW	Y	DFE_WT5[0]	
	3	0	RW	Y	DFE_WT4[3]	Bits force DFE tap 4 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT4[2]	
	1	0	RW	Y	DFE_WT4[1]	
	0	0	RW	Y	DFE_WT4[0]	
21	7	0	RW	Y	DFE_WT3[3]	Bits force DFE tap 3 weight, manual DFE operation required to take effect
	6	0	RW	Y	DFE_WT3[2]	
	5	0	RW	Y	DFE_WT3[1]	
	4	0	RW	Y	DFE_WT3[0]	
	3	0	RW	Y	DFE_WT2[3]	Bits force DFE tap 2 weight, manual DFE operation required to take effect
	2	0	RW	Y	DFE_WT2[2]	
	1	0	RW	Y	DFE_WT2[1]	
	0	0	RW	Y	DFE_WT2[0]	

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2D	7	1	RW	Y	RESERVED	
	6	0	RW	Y	RESERVED	
	5	0	RW	Y	RESERVED	
	4	0	RW	Y	RESERVED	
	3	0	RW	Y	EQ_BST_OV	Allow override control of the EQ setting by writing to channel register 0x03. Not recommended for normal operation.
	2	0	RW	Y	DRV_SEL_VOD2	Controls the VOD levels of the high speed drivers
	1	0	RW	Y	DRV_SEL_VOD1	
	0	0	RW	Y	DRV_SEL_VOD0	
2E	7:00	0	RW	N	RESERVED	
2F	7	0	RW	Y	RATE1	4 bits determine standard. Refer to Table 2.
	6	0	RW	Y	RATE0	
	5	0	RW	Y	SUBRATE1	
	4	0	RW	Y	SUBRATE0	
	3	0	RW	Y	INDEX_OV	If this bit is set to 1, reg 0x13 is to be used as a 5 bit index to the [31:0] array of EQ settings.
	2	1	RW	Y	EN_PPM_CHECK	1: PPM check to be used as a qualifier when performing lock detect
	1	1	RW	Y	EN_FLD_CHECK	For default ref_mode 3: 0: FLD is enabled 1: FLD is disabled
	0	0	RWSC	N	CTLE_ADAPT	Starts CTLE adaption, self-clearing

DS125DF410, 43.

Address (Hex)	BITS	DEFAULT VALUE (Hex)	MODE	EEPROM	FIELD NAME	DESCRIPTION
31	7	0	RW	Y	RESERVED	
	6	0	RW	Y	ADAPT_MODE1	00: no adaption 01: adapt CTLE only 10: adapt CTLE until optimal, then DFE, then CTLE again 11: adapt CTLE until lock, then DFE, then EQ until optimal
	5	1	RW	Y	ADAPT_MODE0	
	4	0	RW	Y	EQ_SM_FOM1	00: not valid 01: SM uses HEO only 10: SM uses VEO only 11: SM uses both HEO and VEO
	3	0	RW	Y	EQ_SM_FOM0	
	2	0	RW	N	RESERVED	
	1	0	RW	N	RESERVED	
	0	0	RW	N	RESERVED	

Claim 20	
	DS125DF410, 44. To the extent that this limitation is not disclosed, either explicitly or inherently, by DS125DF410, this limitation is obvious to a person of ordinary skill in the art based on (1) DS125DF410 alone, (2) the knowledge of a person of ordinary skill in the art; and/or (3) the teachings with respect to this claim element as detailed in the Cover Pleading and/or other invalidity claim charts. The motivations to modify or combine may come from, for example, the knowledge of the person of ordinary skill themselves, or from known problems and predictable solutions as embodied in these references, examples of which are discussed in the Cover Pleading.