

From the previous simulations it was determined that a surface concentration $N_{\text{sur}} \geq 5 \times 10^{20} \text{ cm}^{-3}$ was needed to prevent significant ohmic losses across the light absorbing surface. The junction depth was deemed to not be a critical parameter due to electron diffusion preventing a full depletion all the way to the metallurgical junction (see Fig. 3.15). This was advantageous as it allowed a relaxation of the thermal budget and for all implants to be done at RIT. The use of arsenic as an n-type dopant would have allowed for shallower junction depths to be created using ion implantation however it is unavailable in the RIT SMFL, therefore phosphorous served as the n-type dopant.

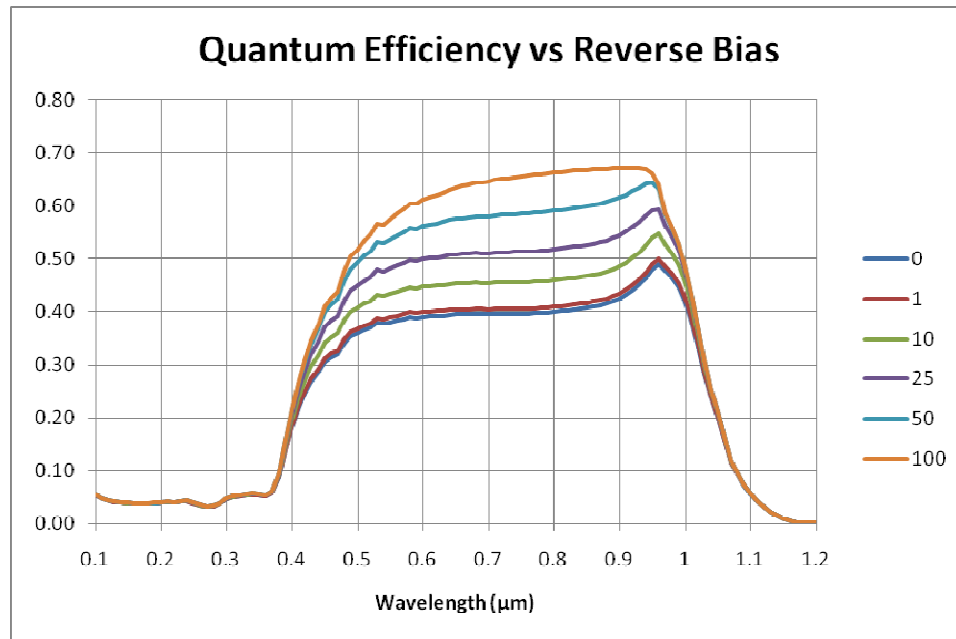


Fig. 3.16 Simulated QE curves for operating biases from 1 to 100 V

With the basic fabrication process parameters for the device determined, the detector operation was explored further by simulating the QE at various biases. Fig. 3.16

shows QE curves for the detector biased at 1, 10, 25, 50, and 100 V. At low voltages the QE in the visible and NIR range is severely degraded. The QE reaches a maximum value at 100 V and simulations at higher voltage showed no additional improvements. The QE at wavelengths less than 400 nm are completely unaffected by the detector bias, again suggesting the carriers are being generated in a region that is not depleted.

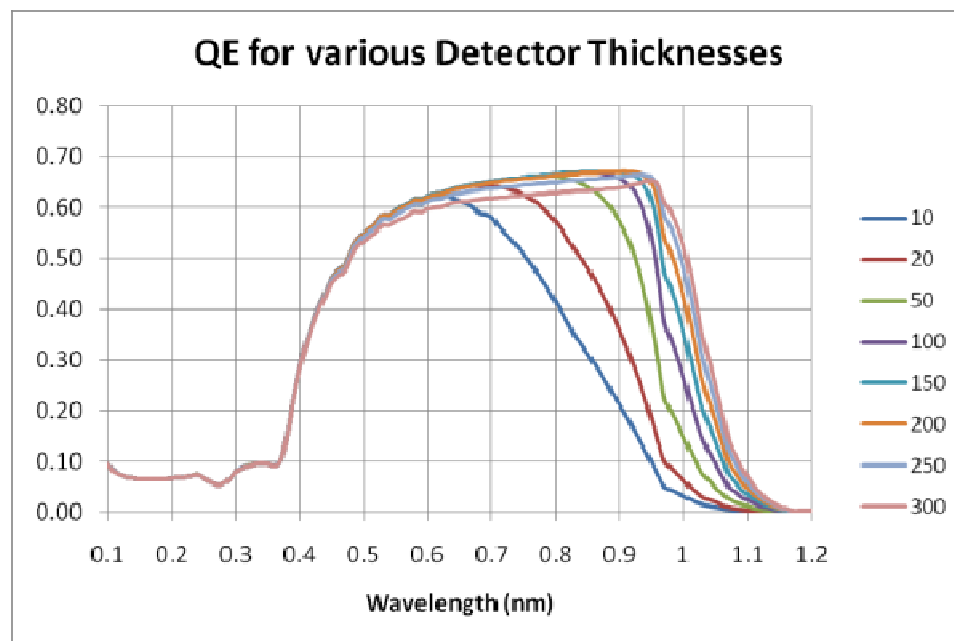


Fig. 3.17 QE curves for detector thicknesses from 10 to 300 μm

Although the thickness of the detector was determined by the substrates ordered for the project, the detector thickness was varied in simulations to demonstrate its effect on QE as shown in Fig. 3.17. The main effect increasing detector thickness has is to provide a greater volume of material for longer wavelength light to be absorbed within. At a thickness of 100 μm the efficiency has reached the maximum efficiency for all

wavelengths less than 900 nm. Further increasing the thickness improves the 1 μm response until larger biases are required to maintain the efficiency.

3.3.3 Point Spread Function

To determine the PSF for a structure in the Atlas simulation program the uniform illumination is split into individual rays. A five pixel wide structure is solved for each of the rays individually and the current is plotted as a function of the position of the light source. A device 75 microns wide was defined in Atlas, the largest structure that could be simulated with adequate resolution due to the limit on the total number of grid points. The uniform monochromatic (600 nm) light was split into 150 rays and the current through each of the 5 pixels is plotted as a function of ray position in Fig. 3.18.

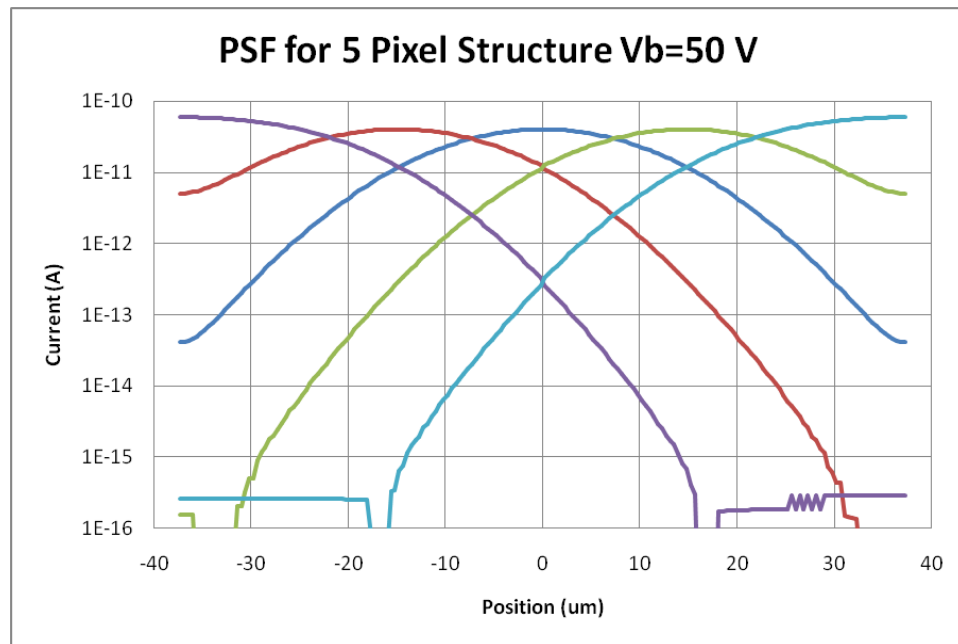


Fig. 3.18 Point spread function simulations showing current through pixels as a function of the source illumination position

The curves can be seen to increase slightly towards the edge of the structure due to diffusion boundary conditions. The simulation software assumes the defined region of silicon is suspended in a vacuum and therefore does not allow any diffusion of carriers into or out of the lateral boundaries. The curve from each of the pixels is shifted to center the maximums in Fig. 3.19 showing this effect is only significant within a few microns of the boundary. This confirms the accuracy of the curve over the vast majority of the simulated region.

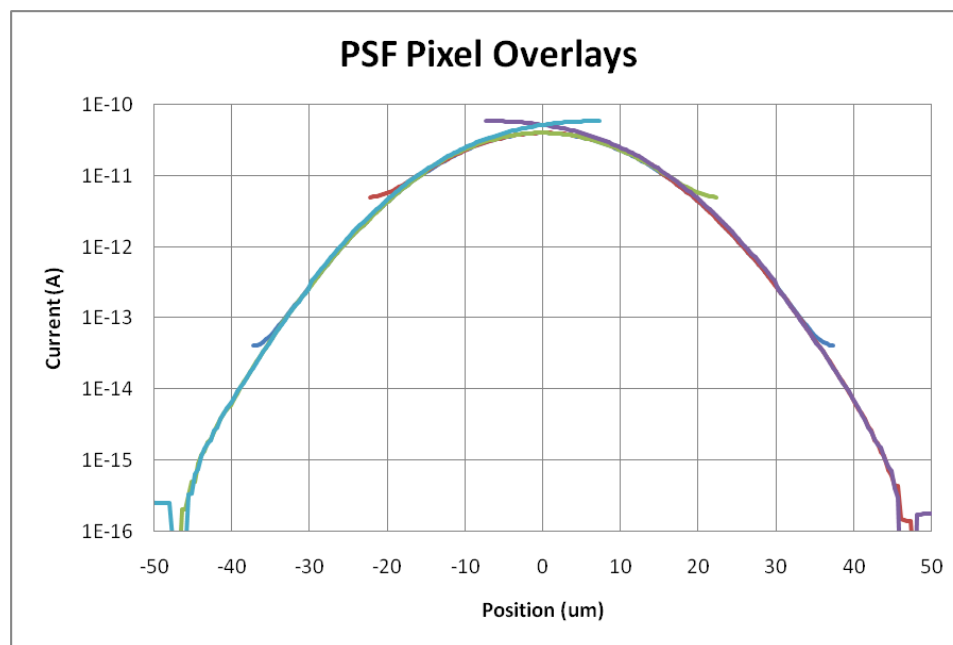


Fig. 3.19 Current through pixels overlaid with maximums centered

The point spread function was simulated as a function of the detector operating bias and the results are shown in Fig 3.20. At the designed operating bias, the full-width half-max (FWHM) of the PSF is significantly larger than the 15 μm pixel pitch. The

consequence is an appreciable charge is expected to leak between adjacent pixels. This result is in line with literature that suggests over-depletion of the detector is required for best performance [25]. The 50 V used here is just enough to deplete the full thickness of the detector. For larger electric fields the FWHM of the PSF decreases rapidly.

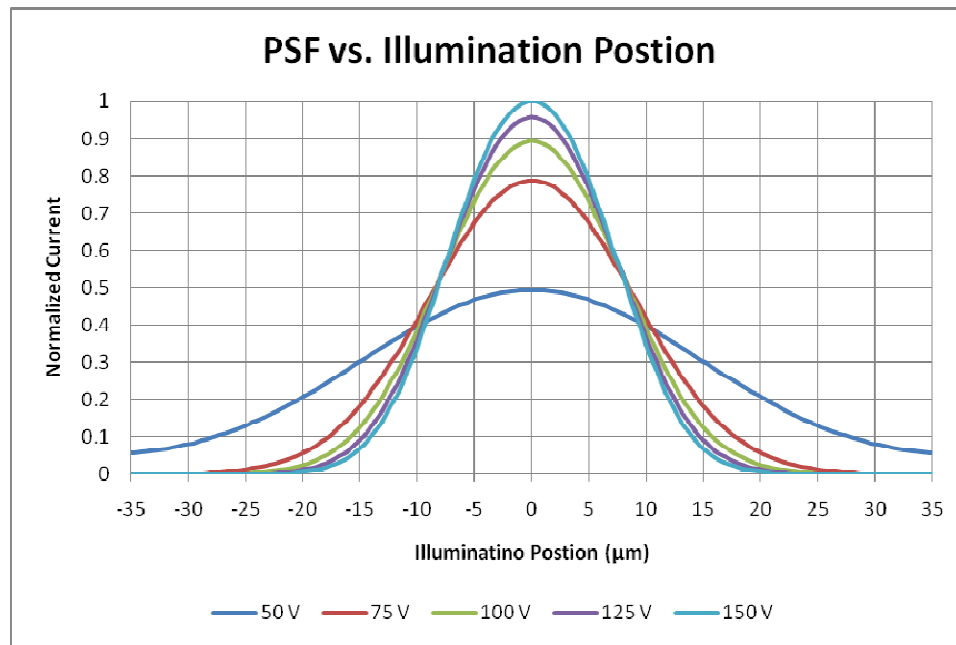


Fig. 3.20 Simulated current vs. illumination position for 50, 75, 100, 125 & 150 V

The amount of lateral diffusion is determined by temperature, electric field, and the depth at which the carriers are generated. Increasing either the electric field or generation depth reduces the transit time, which is the amount of time carriers have to diffuse. The location of carrier generation is determined by the wavelength and the optical properties of the material. Current versus illumination position curves were

generated for wavelengths from 100 to 1200 nm at electric fields of 2 – 6 kV/cm. The FWHM of the curves were extracted and plotted as a surface graph shown in Fig. 3.21.

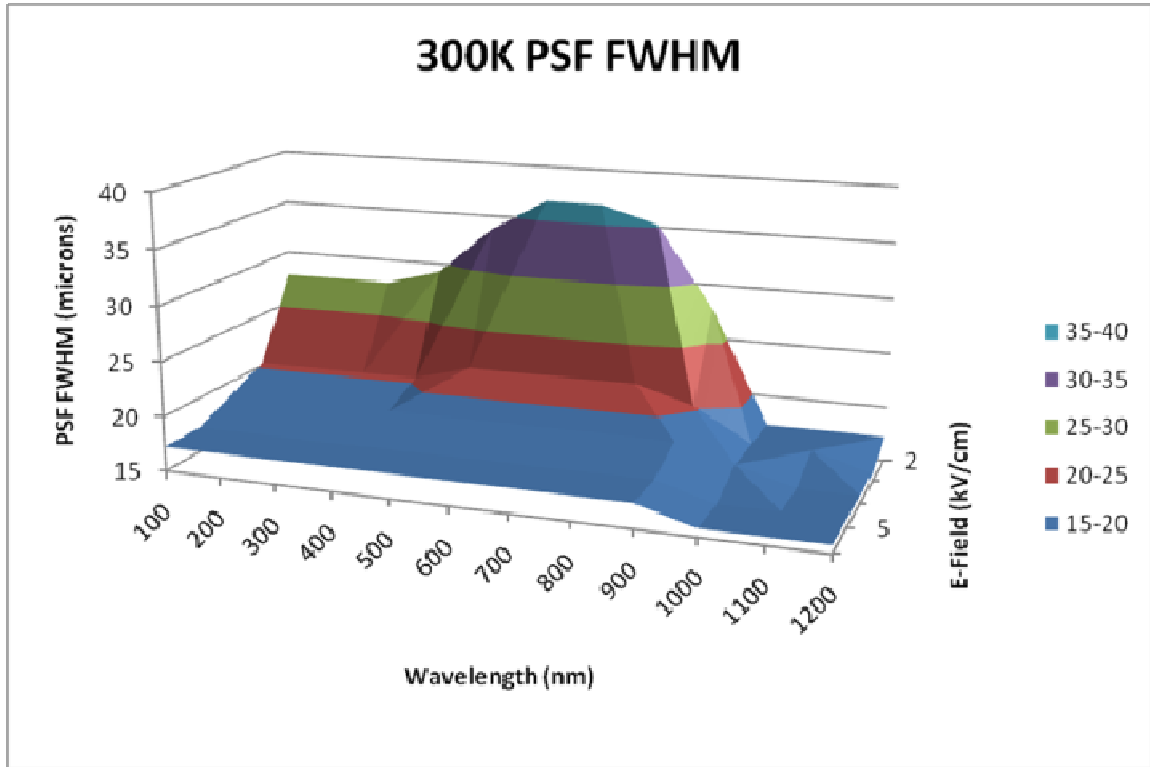


Fig. 3.21 FWHM of Simulated PSF for 100 – 1200 nm and 2 – 6 kV/cm at 300 K

The diffusivity and mobility are both influenced by the temperature of the device, and related by the Einstein relationship. As the temperature is decreased both the mobility and diffusivity increase though at different rates. Diffusivity is directly related to temperature; however the $T^{-3/2}$ dependence nested inside mobility dominates and causes the diffusivity to increase slightly at lower temperatures. The net result of reducing the temperature is an increase in carrier velocities compared to the relative diffusivity, resulting in decreased lateral diffusion.

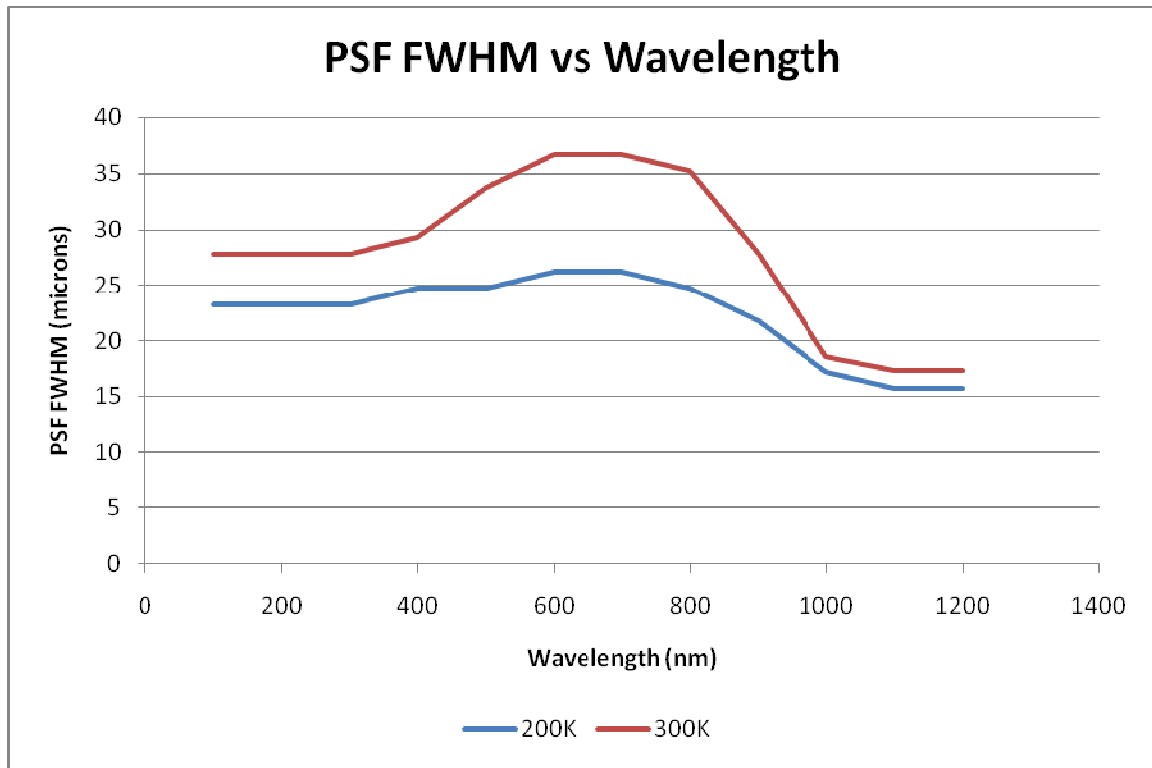


Fig. 3.22 Full width half max of point spread function vs. wavelength at 2 kV/cm for 200 K and 300 K

The effect of temperature is most prominent at lower electric fields and becomes nearly insignificant at fields greater than 4 kV/cm. The FWHM of the PSF is plotted as a function of wavelength at 200 K and 300 K in Fig. 3.22. At longer wavelengths carrier generation occurs throughout the thickness of the device, and again temperature has a subdued impact.

A greater understanding of effect wavelength has on the PSF can be attained by plotting the minority carrier concentration distributions within the device during steady state operation. The distributions are shown in Fig. 3.23 for various wavelengths at the designed operating bias with the point source illumination centered on the device. The

lateral diffusion is most prominent in the 500 – 900 nm range of wavelengths, where most of the light is absorbed within the depletion region. At shorter wavelengths below 400 nm all of the carrier generation occurs within the first 100 nm of silicon, and carrier must diffuse into the depletion region reducing the concentration gradients by the time they arrive. At wavelengths greater than 900 nm the majority of carrier generation moves deeper within the device reducing the time carries have to diffuse laterally.

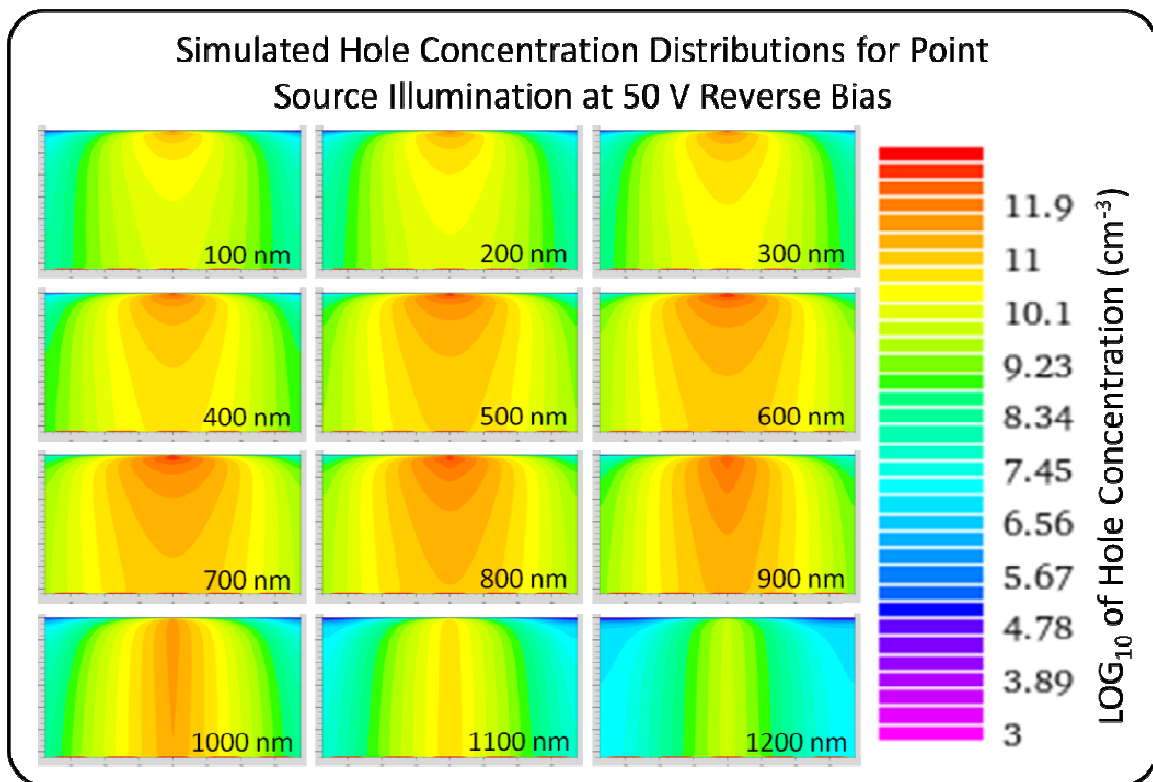


Fig. 3.23 Simulated hole concentration distributions for centered point source illumination at 50 V reverse bias and 300 K for various wavelengths in 5 pixel structure

Chapter 4

Layout and Fabrication

Wafers were fabricated in three process runs that subsequently incorporated the revised process flow, a new mask set, and finally the newly developed processes in each run. Electrical testing was performed to characterize device performance and evaluate process improvements. The first fabrication run used the existing contact mask set with the revised process flow to significantly reduce the number of process steps and related wafer handling in an attempt to limit the introduction of defects and contamination. The second process run incorporated a new mask set using both contact and projection lithography systems with the newly developed contact cut and dry aluminum etch processes. The final process run benefitted from lessons learned during the first two runs and included several process revisions.

4.1. Existing Layout

This thesis builds upon work performed by Kolb during the 2007-2008 academic year [26]. Devices were fabricated using a process by Kolb as part of the capstone project for her Bachelors degree. The layout for the previous work is shown in Fig. 4.1 with all levels of the contact mask set overlaid.

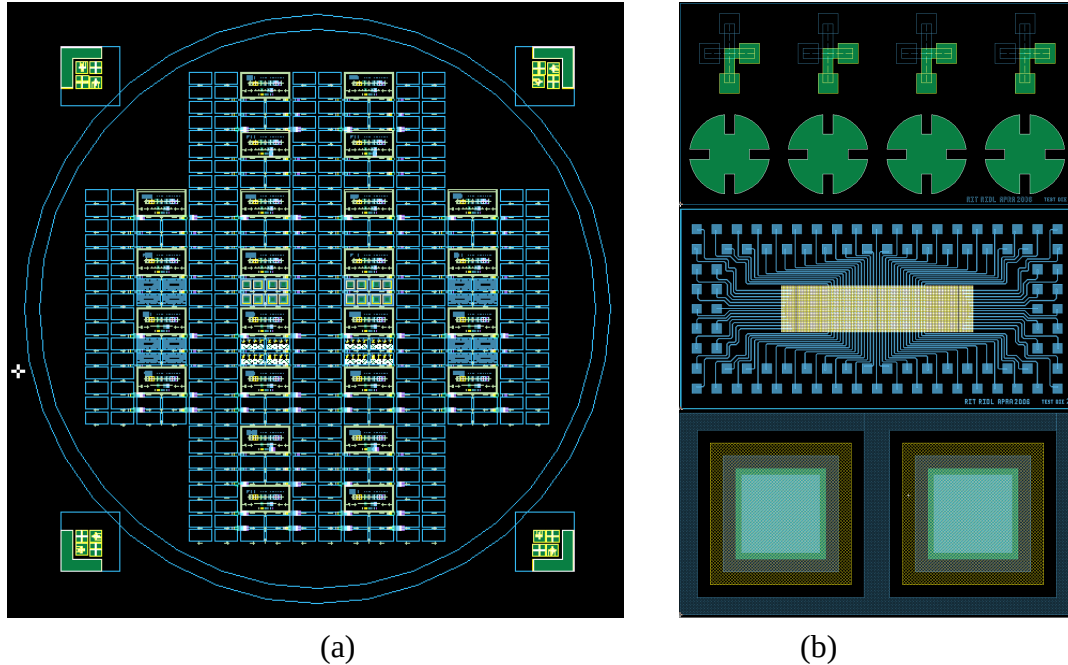


Fig. 4.1 CAD rendering of contact lithography mask layout of (a) entire wafer and (b) close-up of test structures

The process used contact alignment exclusively and relied upon manual alignment of the front and back layers. The test features in the mask set included cross-bridge Kelvin resistors, cloverleaf structures, an array with individually indexed pixels and two large test pixels.

4.2. Mask Design

The need for enhanced resolution and depth of focus on critical mask levels warranted the use of projection lithography and the need to create a new mask set. The lithography tool used was a GCA Automatic Wafer Stepper (AWS) with a g-line illumination source (436 nm) and a 5X reduction system yielding a minimum resolution of ~ 750 nm. A 10 mm x 13.5 mm die shown in Fig. 4.2 (a) was designed that

incorporates 8 diode arrays, 3 test die, and a die that contains alignment marks and resolution features. This die has been arrayed to produce a contact mask shown in Fig. 4.2 (b). Alignment marks have been applied outside the four inch radius where the wafer is positioned to allow the alignment of one mask to another on the contact lithography system enabling the revised front-to-back side alignment process.

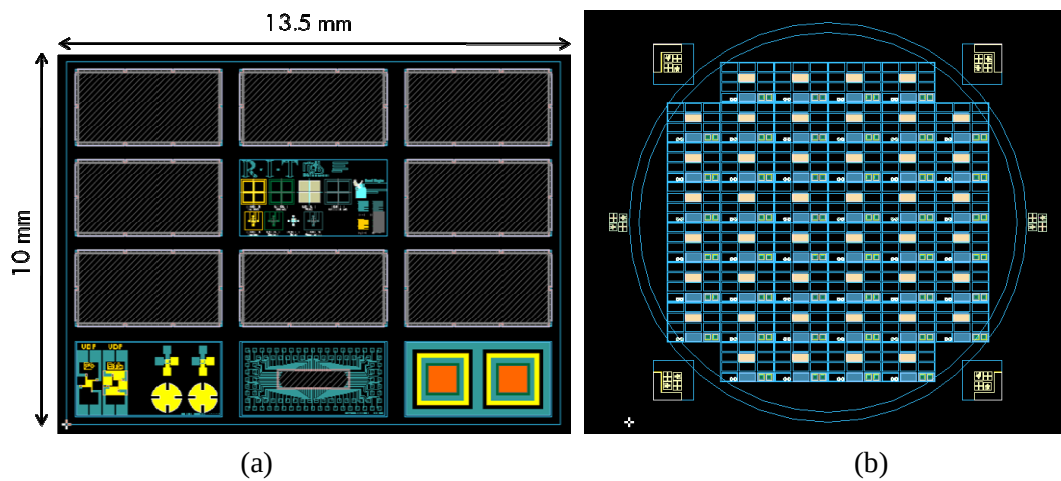


Fig. 4.2 CAD renderings of **(a)** projection die and **(b)** contact mask layout

4.2.1 Revised Test Die

Two of the test die were designed to provide additional process characterization. Additional Van der Pauw structures were included to measure the sheet resistance of the implanted layers through multiple structures. The relative percent of activated dopant can be determined from the conductivity. The cross-bridge Kelvin resistor structures were revised to vary the size and number of contacts between the metal layer and the implanted regions to determine the contact resistance. These test structures are shown in

Fig. 4.3 (a). The pixels in the imaging array are too small to probe manually ($15\text{ }\mu\text{m}$), therefore enlarged versions were created of varying size to allow actual pixel performance to be extrapolated. The scaled pixels, shown in Fig. 4.3 (b) are 10, 15, 18, 25, 50 and 100 times the size of the device pixels. By including pixels of varying size, the area and perimeter contributions to leakage currents are able to be determined.

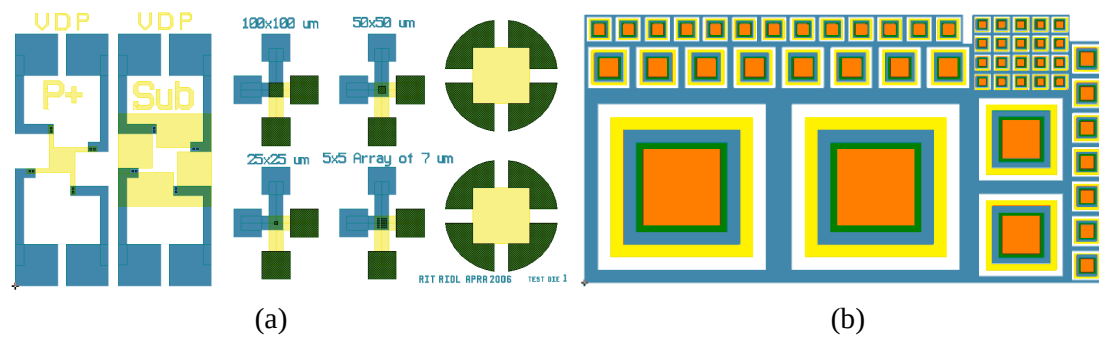


Fig. 4.3 CAD renderings of **(a)** Process characterization test die and **(b)** Pixel characterization test die

4.3. Process Flow

A revised diode fabrication process was designed that dramatically reduced the number of steps and tools the wafers were subjected to. The number of process steps was cut nearly in half to ~ 35 steps and the use of low pressure chemical vapor deposition (LPCVD) and rapid thermal processing (RTP) systems have been eliminated. A thermal oxide grown in the initial steps of the process serves as a protective layer, substrate isolation, and anti-reflective layer. The method for front-to-back-side alignment used was altered to allow alignment to be performed on the contact alignment tool as opposed

to the 'by hand' process under a microscope currently used. Figure 4.4 provides a summary of the key steps in the revised flow and a complete process flow is included in Appendix II.

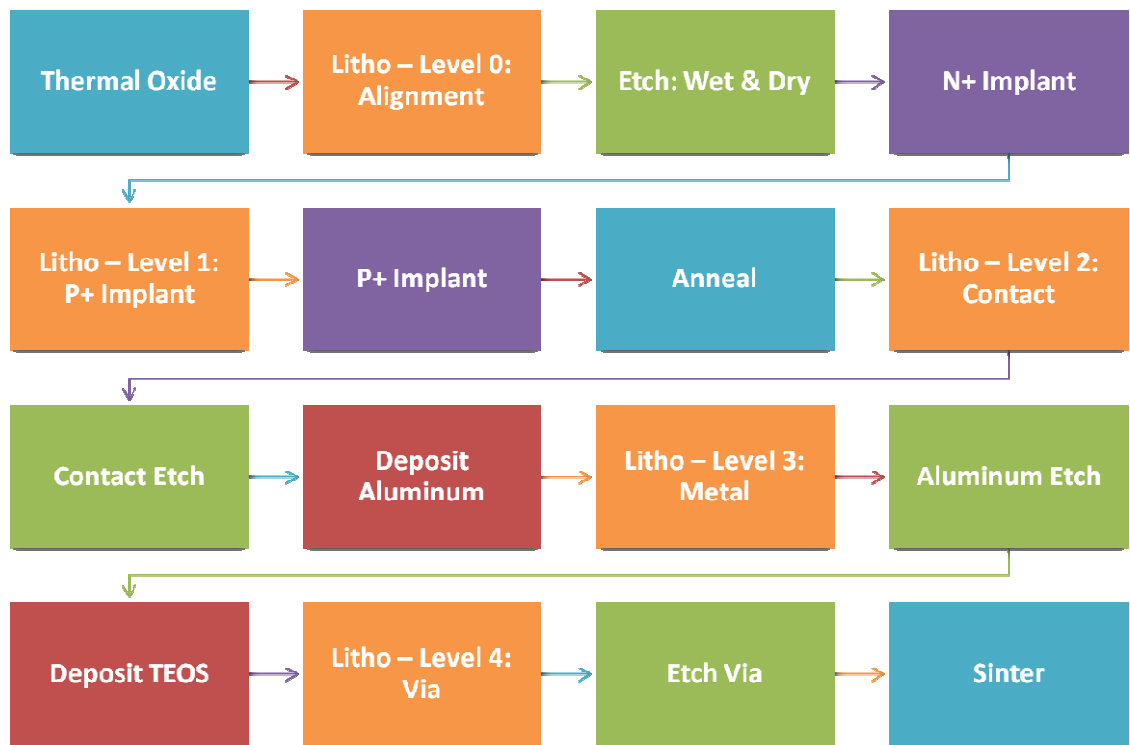


Fig. 4.4 Summary of key steps in revised process flow

First a thermal oxide was grown to serve as a protective layer against contamination as well as an anti-reflective layer. The first lithography step was used to define alignment features on both sides of the wafers. The features were then transferred into the oxide using a wet etch and into the substrates using a dry etch process. The light absorbing side of the wafers then received a blanket phosphorous implant to reduce the resistance of the surface layer to prevent ohmic losses and allow for a suitable contact to

be made. The backside of the devices were patterned and implanted with boron to define the pixels. Next a thermal anneal was performed to activate the dopants and repair the implant damage. The contact lithography level was patterned onto each side of the wafer separately and then the oxide was removed using a wet etch with the opposing side of the wafer protected by a blanket layer of resist. Aluminum was sputtered onto both sides of the wafer and patterned with the metal layout. A TEOS passivation layer was deposited onto the backside of the wafer and vias were etched to open contacts for the bump bonds. Finally a sinter was performed to ensure a good contact between the aluminum and silicon substrate.

4.3.1 Front-to-Backside Alignment

The purpose of the first lithographic levels on both the front and back side of the wafer is to etch features into the silicon that can be used as alignment marks for all subsequent lithographic processes. Therefore the ability to ensure these two layers are aligned to each other is paramount to device performance. The process used to align these two layers has been revised from one which requires the manual alignment of the masks under a microscope to one where the contact lithography tool is utilized for all alignment events. The manual process requires significantly larger tolerances in the

design as mis-alignment of less than 20 μm is difficult to achieve. The revised process can regularly achieve front-to-back side alignment within 5 or less microns.

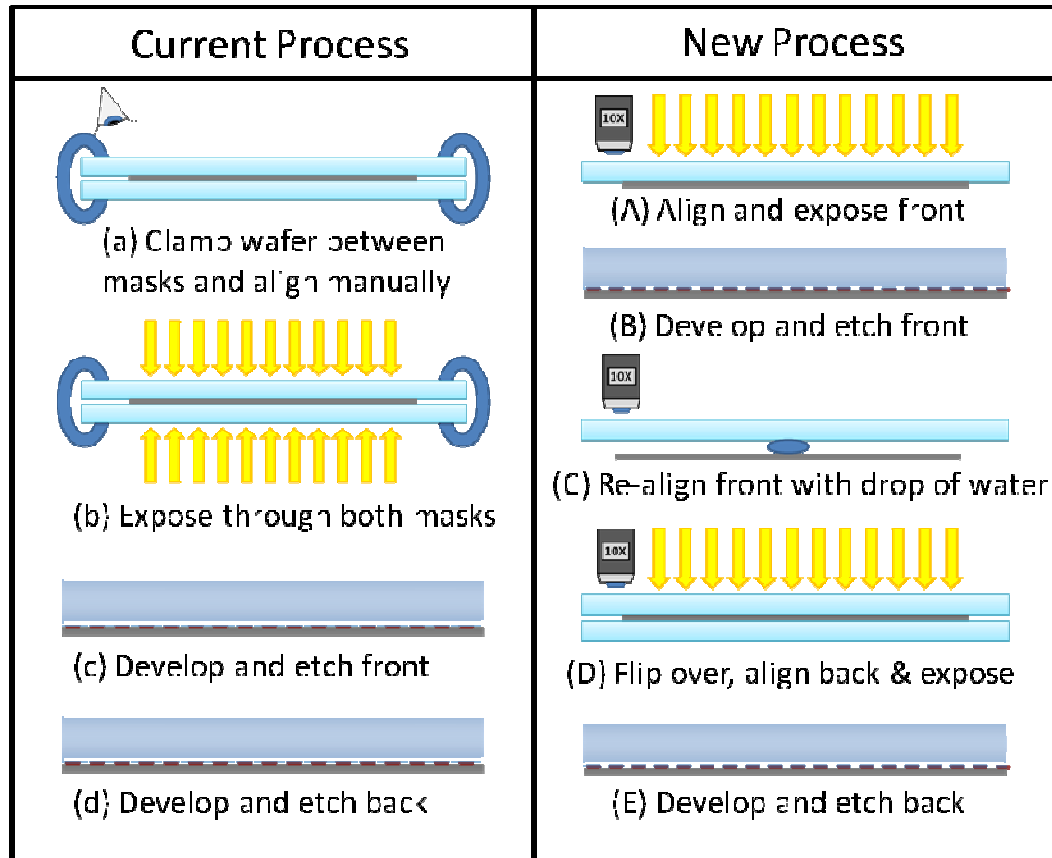


Fig. 4.5 Comparison of current and newly developed front-to-back side alignment process

A comparison of the current and new front-to-back side alignments processes are shown in Fig. 4.4. In the old process the wafer was clamped between the two masks and aligned manually underneath a microscope (Fig. 4.5 (a)). The wafer is then exposed through each mask (Fig. 4.5 (b)) and developed and etched on both sides (Fig. 4.5 (c) & (d)). A newly developed front-to-back side alignment process will allow the alignment of the masks to be performed on the contact alignment tool.

First, the wafer is coated with resist on a single side, and the alignment marks are exposed into the wafer (Fig. 4.5 (A)). The wafer is then developed and the marks are etched into the wafer (Fig. 4.5 (B)). The wafer is loaded back onto the contact tool with a drop of water on the surface and the mask is aligned with the previously etched features (Fig. 4.5 (C)). The drop of water ensures that once the wafer has been aligned to the mask, they can be removed from the system without any movement between the two. They are placed back into the system, flipped over so the mask is in contact with the vacuum chuck and the back side of the wafer is ready for exposure. The second mask is loaded and the two are aligned to each other on the contact tool (Fig. 4.5 (D)). The back side is then exposed, developed and the alignment marks are etched into the wafer (Fig.4.5 (E)). Optical micrographs showing the improvement of the resist image from the metal lithography layer on the bump bond side of the device are shown in Fig 4.6.

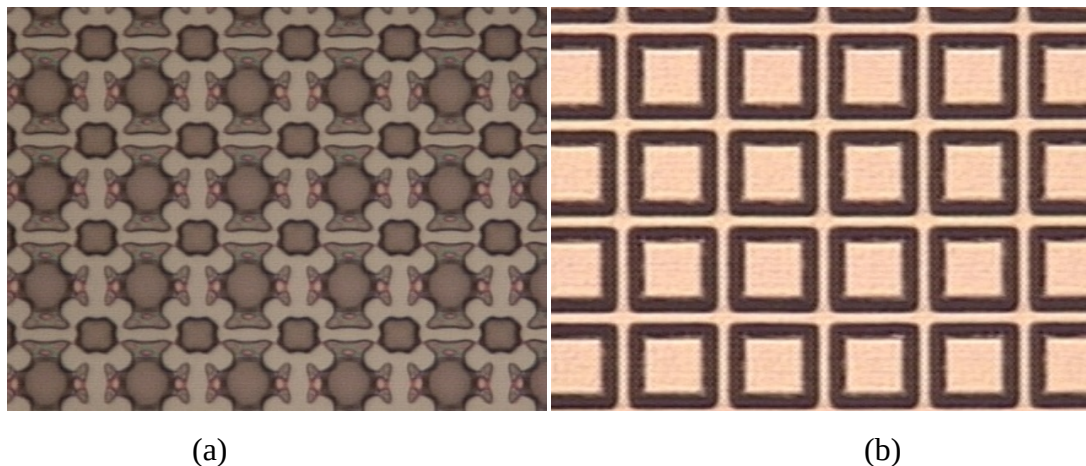


Fig. 4.6 Optical Micrographs of Metal layer pattern after
(a) contact lithography (b) projection lithography

4.3.2 Contact Cut Etch

During initial fabrication runs multiple failure mechanisms were observed during the contact cut etch process. A wet etch in 10:1 buffered oxide etch (BOE) was used and the process of record (POR) called for manual agitation. The method of agitation was defined as lifting the boat of wafers out of the bath and placing them back in.

Two defects were observed as a result of the etch process including an inability to fully clear a contact and a dramatically increased etch rate at the oxide-resist interface. An optical micrograph of the defect can be seen in Fig. 4.7 where the affected contacts exhibit a large colorful ring that is sometimes accompanied by brownish spots in the center. The colorful rings are due to a region of varying oxide thickness and the dark spots are thin regions of oxide most likely ~50 nm thick. It was initially believed that this was the result of an interaction between the two common problems of resist scumming and poor adhesion. Although poor adhesion was an issue at times, the main contributing factor was not discovered until much later while performing experiments for another process.

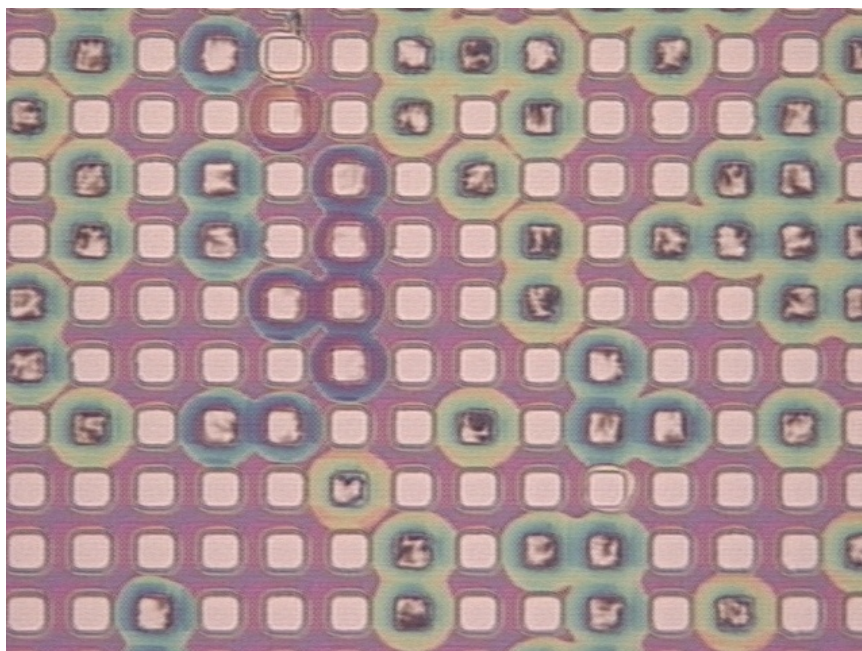


Fig. 4.7 An optical micrograph of the array after contact cut etch where the failure mechanism can be observed

During a wet process a fluid is drawn into a reservoir typically several microns square in size and one or two microns deep with relatively vertical sidewalls. As the fluid reacts with the underlying layer a cavity is formed below the film of resist. The development of the LOR layer used in during hybridization is a similar process, though with slightly thicker layers. It was discovered during the development of this process that if the surface of the wafer was dried after an initial exposure to the developer solution, rewetting the surface caused a very similar defect. An optical micrograph of the defect in the LOR layer can be seen in Fig.4.8.

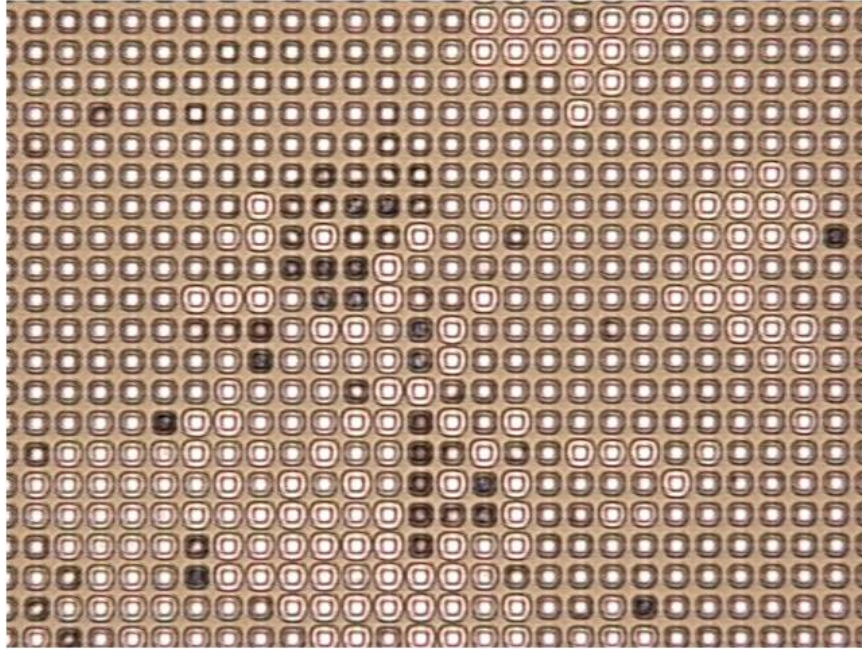


Fig. 4.8 Optical micrograph of features in LOR layer exhibiting blow-out and scumming

The proposed hypothesis for this mechanism is the formation of a cavity affects the ability of the fluid to flow into the feature. Any air trapped in the feature as the wafer is rewet prevents reaction at the bottom and enhances it at the interface. Combined with poor adhesion at the interface this can cause the feature to become severely blown-out and still not fully clear at the bottom.

4.3.3 Aluminum Dry Etch

The metal lithography level on the bump bond side of the wafer is a critical level as it contains the smallest features in the design. A 1 μm border of metal is defined around the outside of each pixel creating a 2 μm wide metal grid between adjacent pixels. The pattern transfer for this level was previously accomplished using a wet etching

process, although significant undercutting led to the erosion of these lines as shown in

Fig. 4.9.

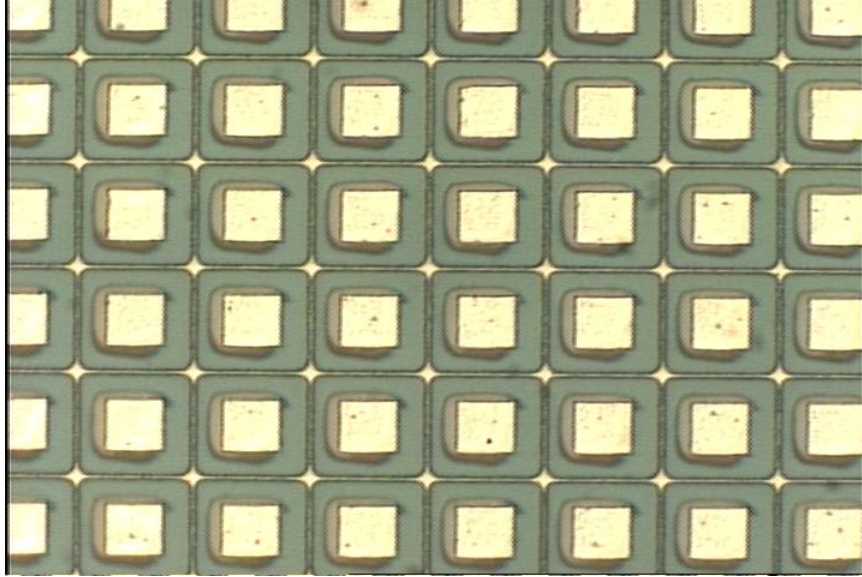


Fig. 4.9 Patterned aluminum layer on bump bond side of device showing thin grid lines due to undercutting during wet etch process

A dry aluminum etch process was developed based on a designed experiment performed a LAM 4600 Metal etcher at Xerox. This is the same model of chlorine dry etch tool available at the SMFL. The tool was designed to process 150 mm wafers and therefore carrier were required to process the 100 mm wafers used in this study. The carriers consist of a 150 mm wafer with a 105 mm circle recess in the center that serves as a pocket to contain the smaller wafer. Although necessary there are several drawbacks associated with the use of a carrier including reduced thermal conduction and capacitive coupling between the substrate and chuck. The recipe from the aforementioned study was used as a starting point for the aluminum dry etch process. An optical micrograph of

resolution features from a test mask after the initial etch was performed is shown in Fig. 4.10.

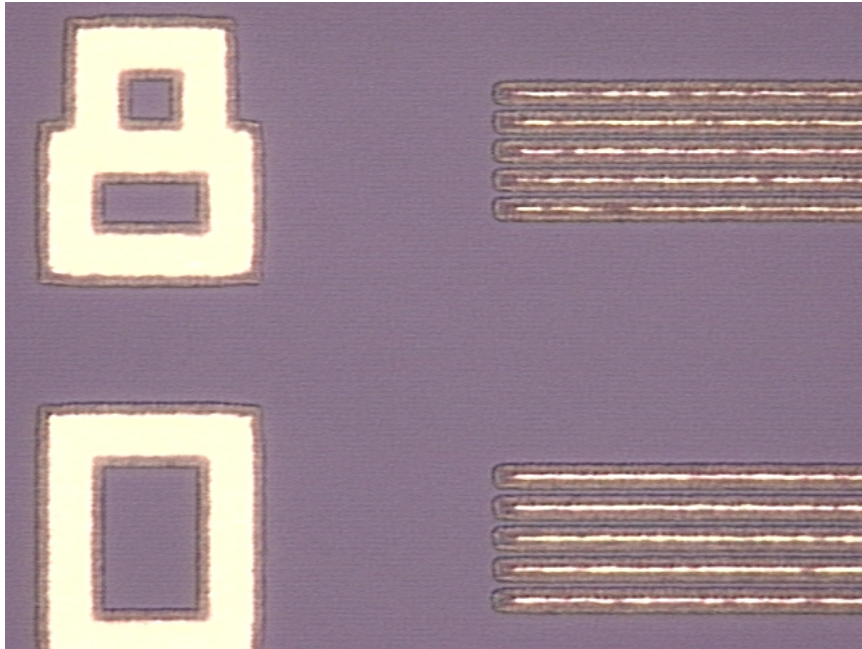


Fig. 4.10 Resolution features etched into aluminum layer using suggested recipe. Note significant undercut of resist features

A significant undercutting of resist features was observed in the initial test wafer, likely due to the introduction of the carrier wafer. The photoresist was also aggressively attacked during the etch and appeared to be shriveling under the intense heat. The inability to use the water passivation system also necessitated the immediate removal of the photoresist to prevent corrosion of the aluminum. Removing the photoresist with an oxygen plasma strip left residues behind so a solvent based process was used.

In order to reduce heat transfer into the wafer and make the etch process more anisotropic several recipe parameters were altered. The experiment found that RF power

had the strongest effect on resist burning with minimal effect on etch rate due to the predominantly chemical nature of the etch and so was reduced significantly. The undercutting was believed to be a result of insufficient sidewall polymer deposition due to the increased temperature of the wafer. Reducing the power and thus heat transfer into the wafer should also help mitigate this problem, however the gas flows were also modified slightly to provide a more polymerizing mixture. A thinner aluminum layer was also used to reduce the total etch time prevent resist burning. The result of the optimized etch recipe can be seen in Fig. 4.11. A significant improvement over the wet process can be seen eliminating the risk of open circuits in the grid.

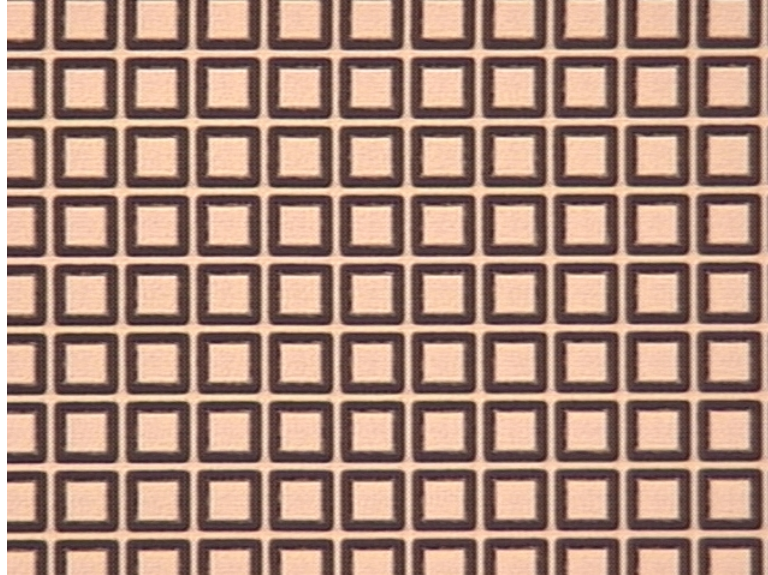


Fig. 4.11 Patterned aluminum pixel contacts dry etched with optimized recipe

Chapter 5

Electrical Testing

Once the fabrication sequence was completed the test diodes structures were measured electrically to determine device performance and quality. The two aspects of device performance evaluated in depth were the on-state ideality factor and off-state leakage. Scaled versions of the diodes were measured to separate area and perimeter effects and extrapolate the performance down to an actual pixel. Carrier lifetimes were determined using the OCVD method and spectral and cryogenic testing was performed.

5.1. Previous Results

The current voltage characteristics of devices fabricated by Kolb are shown below in Fig. 5.1. In forward operation the different modes of current transport are not readily apparent and have rather indistinct transitions. The ideality factor increases rapidly within a couple hundred millivolts, and a large series resistance appears to prevent the device from delivering expected current density levels.

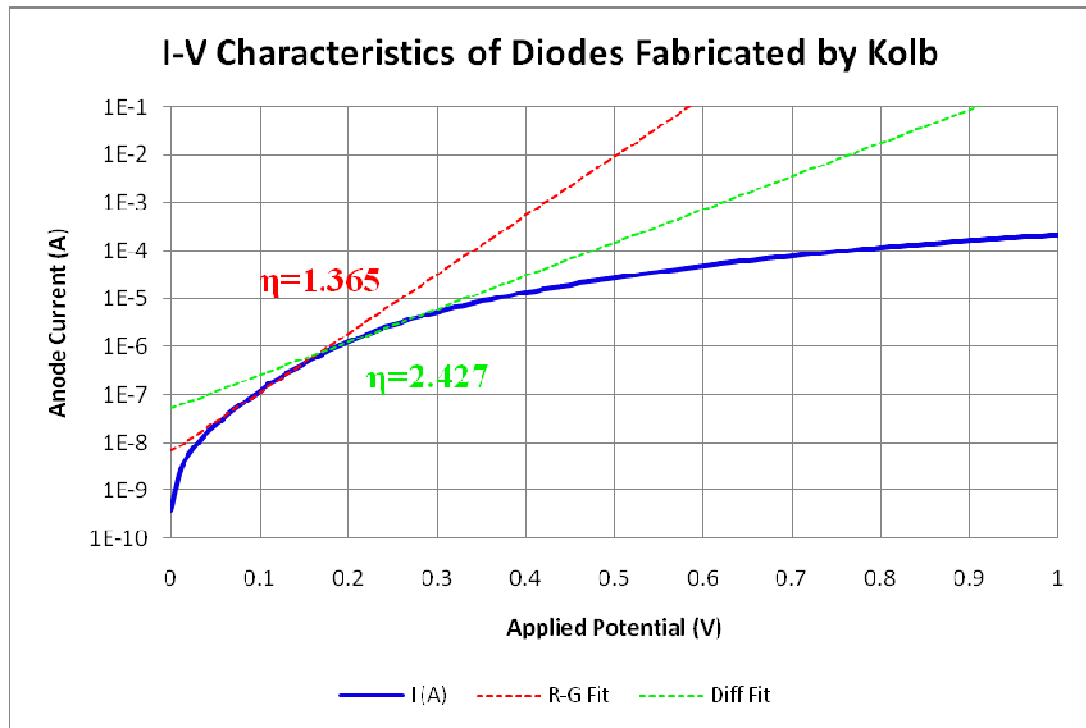


Fig. 5.1 Representative current-voltage characteristics of *p-i-n* diode fabricated by Kolb with ideality fits [26]

The reverse bias current voltage characteristics of several devices are shown in Fig. 5.2. Extremely high leakage current densities are observed as well as non-uniform device behavior. The minimum recorded leakage current of $2 \times 10^{-6} \text{ A/cm}^2$ was almost three orders of magnitude higher than the stated goal. It is believed the use of the LPCVD system for deposition of passivation layers introduced contamination to the devices. The trap centers associated with the contamination resulted in severely degraded on and off-state performance.

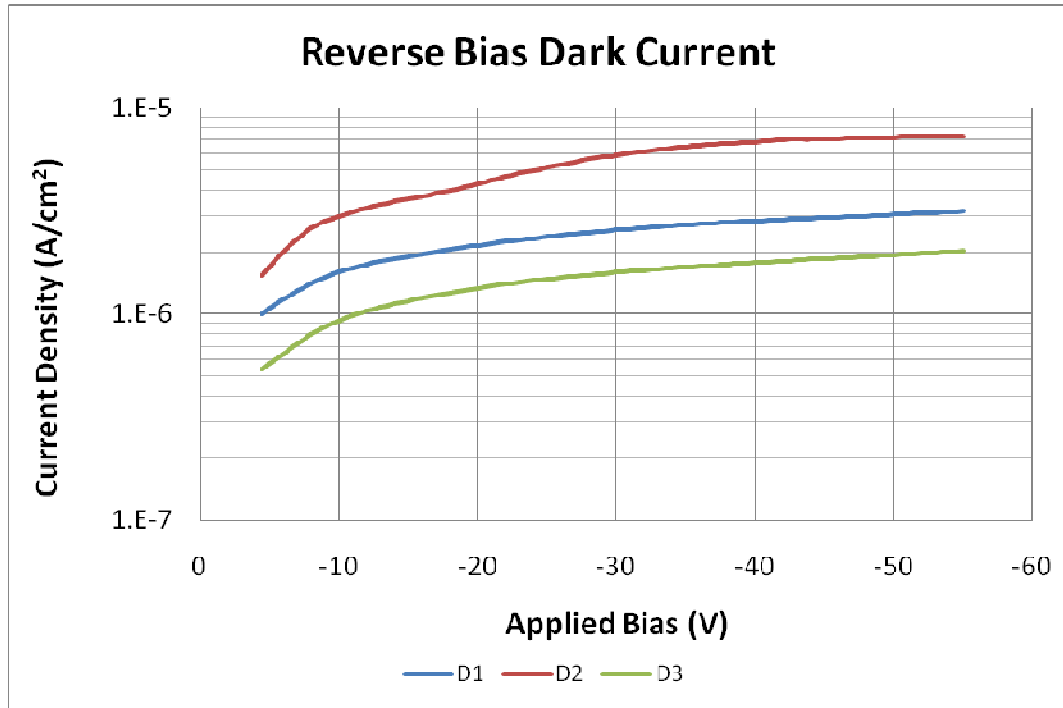


Fig. 5.2 Reverse bias leakage current densities for several devices fabricated by Kolb

5.2. Current-Voltage Characteristics

Electrical testing was performed in a shielded dark box on the 25X test diode structures to determine pixel performance. Current-voltage characteristics were obtained with high voltage resolution in the on-state, and high current resolution in the off state. The devices exhibited high quality diode behavior with low leakage levels. The currents levels at a reverse bias of 50 V were mapped across the wafers to evaluate the uniformity of the leakage currents. Measurements were also performed on a cryogenic testing station to observe the temperature dependence of device operation.

5.2.1 On-State Ideality

A representative forward bias I-V characteristic is shown in Fig. 5.3 selected from one of the wafers sent for bonding. In the forward bias mode the device exhibited several distinct regions of operation. Similar to the simulation results in Chapter 3 an ideality factor of nearly 2 is extracted at lower biases, however a diffusion dominated regime with an ideality factor of ~ 1 is not observed. This is thought to be a soft transition into high-level injection, and series resistance dominating at higher current levels.

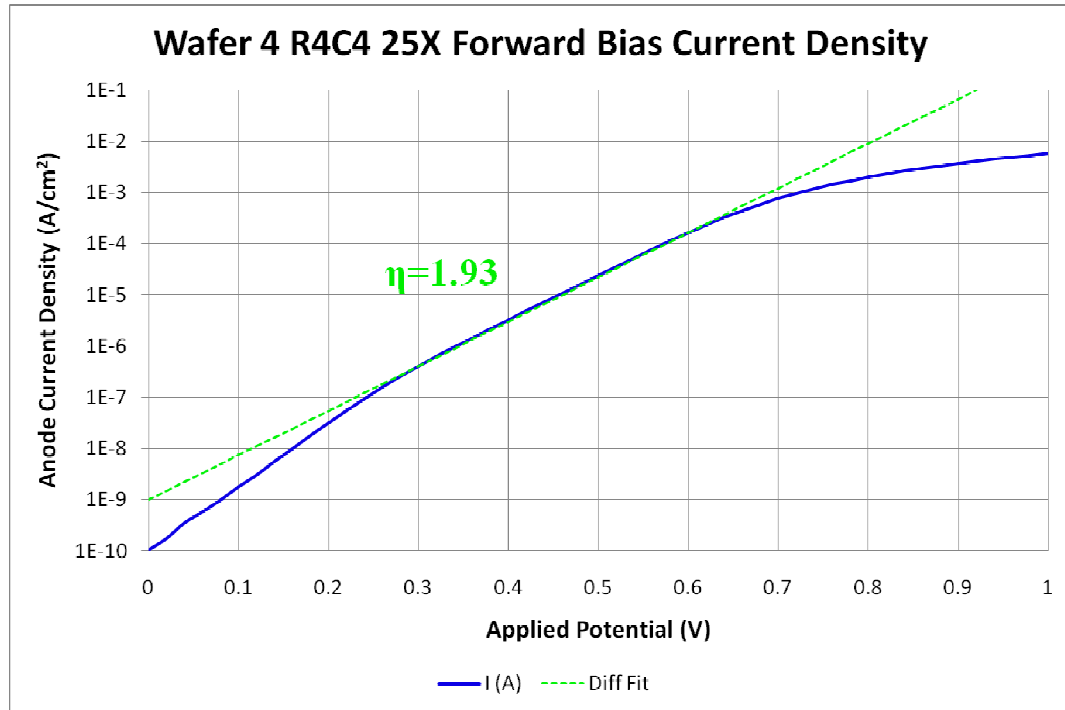


Fig. 5.3 Measured forward bias I-V characteristics of rev3 *p-i-n* diode with exponential fits and resulting ideality factors

Measurements were performed on a cryogenic testing station cooled with liquid nitrogen at temperatures ranging from 250 to 350 K. Unfortunately due to degraded insulation within the cryogenic probes leakage currents from the test set-up dominated

over currents from the device at temperatures below 250 K. Thus although a clear dependence upon temperature is seen at the higher temperatures, no dependence is seen below 250 K. Despite this issue, the relationships observed at the upper temperature range were used to extrapolate device performance at lower current levels.

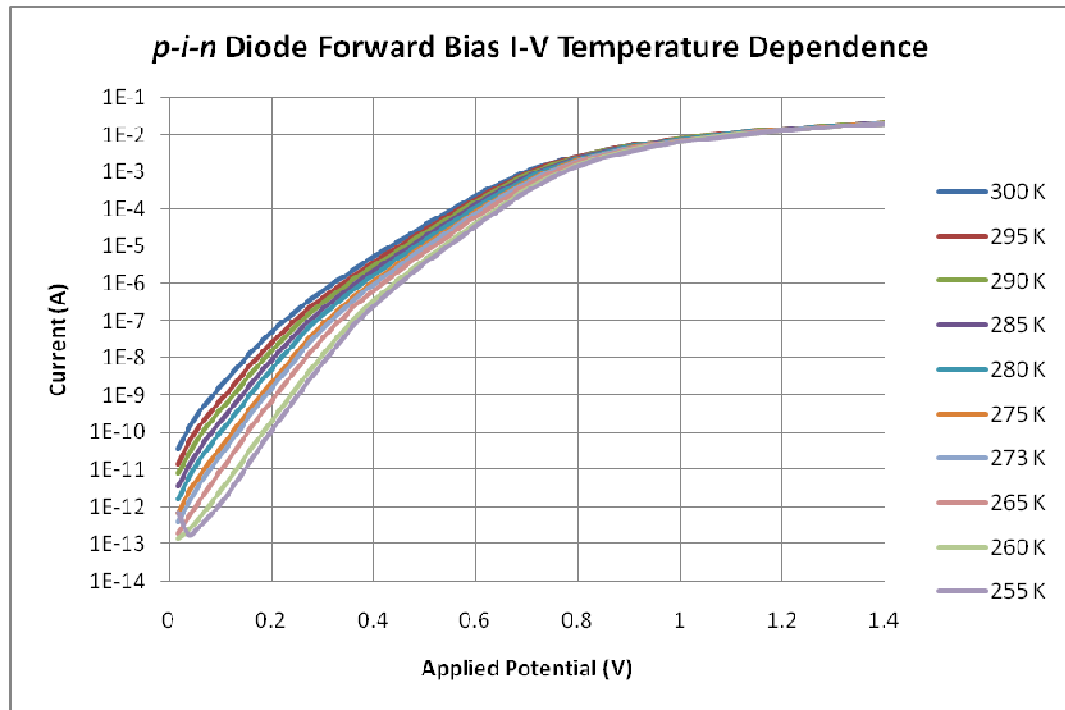


Fig. 5.4 Forward bias I-V characteristics of 25X p-i-n diode measured from 255 K to 300 K showing temperature dependence

The forward bias current-voltage characteristics for a 25X p-i-n diode are shown in Fig. 5.4 for the temperature range of 255 K to 300 K. A dependence on the temperature is seen for applied voltages below 800 mV, although when the device reaches the high-injection/series resistance limited regime temperature no longer has any influence. At the lower applied voltages reducing the temperature increases the ideality

factor but reduces to total current flow. The increase in ideality factor could be due to the lifetime of the carriers increasing faster than the diffusion rate decreases.

5.2.2 Off-State Leakage

The off-state leakage current of test diodes was the primary metric used to determine the quality of the devices. The devices are intended to be used primarily in the reverse bias condition and the leakage current directly attributes to read noise in the final detector. Several sites were sampled from each wafer of the final two fabrication runs and the best wafers from each run were mapped to determine the uniformity and reliability of the process. An interior 25X scaled test diode was used to make all of the reverse bias measurements except for the spectral response.

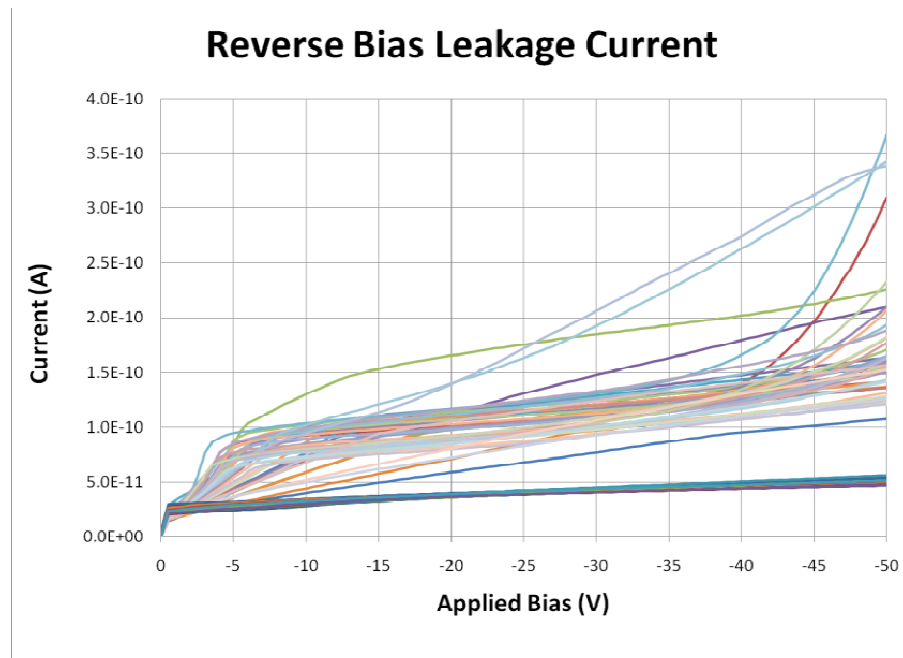


Fig. 5.5 Overlay of reverse bias leakage currents from best wafer of the final two processing runs

An overlay of the leakage current measurements taken from the best wafer of the final two processing runs is shown in Fig. 5.5. Two distinct groups of devices are observed where the group with a larger average leakage and variation was measured on wafer 4 from the second process run and the tightly grouped measurements were made on wafer 1 from the third process run. The devices fabricated in the second process run allow a greater amount of current to flow before stabilizing and continue to show a greater dependence on the applied bias. Soft breakdown mechanisms are observed in several devices and a few other devices appear to simply be resistors with their current varying linearly with applied bias. The final process run significantly reduced both the average leakage currents as well as the variation.

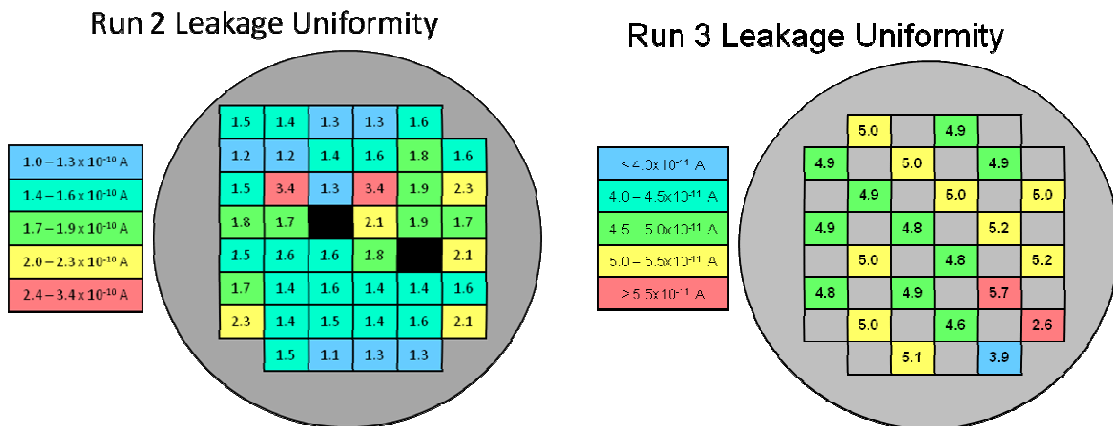


Fig. 5.6 Wafer map of leakage current uniformity for final two processing run.

Wafer maps of the uniformity leakage currents for each of the final two processing runs, shown in Fig. 5.6, were created by selecting the current at the designed operating bias of 50 V. No distinct patterns were observed in the yield of the devices.

Temperature Dependence

The reverse bias characteristics of a high quality device were measured at different operating temperatures using the same cryogenic testing station described earlier. Reverse bias measurements were made at temperatures from 260 to 350 K and are shown in Fig. 5.7. Temperature dependencies below 260 K were unable to be observed due to leakage paths in the test setup introducing too much noise. Leakage currents measured through the probes were at equivalent levels to those generated within from the devices.

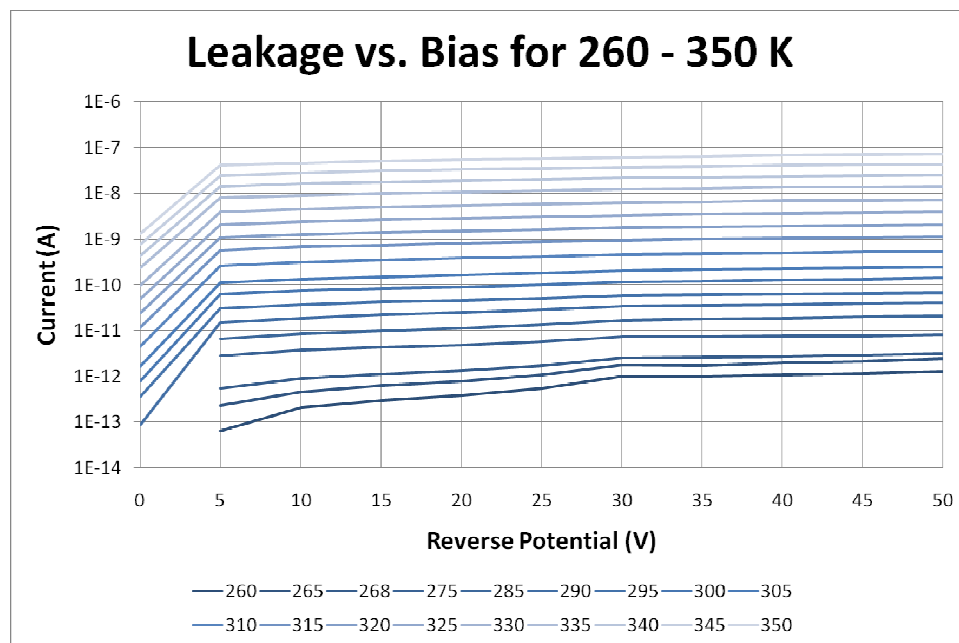


Fig. 5.7 Measure reverse bias leakage current vs. applied potential from 260 to 350 K

The current level at a reverse bias of 50 V was plotted against the temperature the measurement was made at. The observed relationship differs slightly from theory in that an Arrhenius equation was difficult to match with the data. The best fit resulted from a linear extrapolation of the data on a semi-log plot. The extrapolation shown in Fig. 5.8 predicts an additional drop in leakage currents of three orders of magnitude at the designed operating temperature.

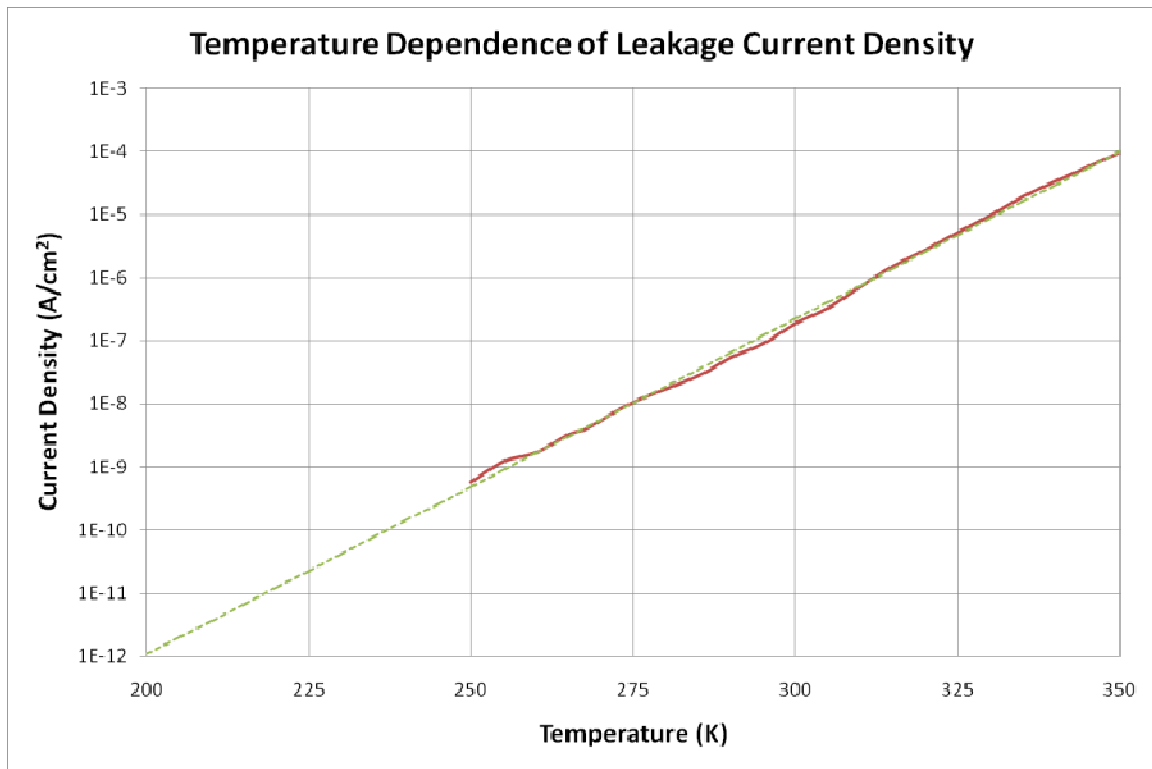


Fig. 5.8 Reverse bias leakage current density at 50 V from 250 to 350 K with exponential extrapolation down to 200 K

TABLE 3 COMPARISON OF REVERSE BIAS LEAKAGE GOALS,
SIMULATIONS AND EXPERIMENTAL RESULTS

	200K Goal	300K Goal	Previous Results	Simulated	Rev3	200K Extrap.	
	1	1.65×10^4	1.14×10^7	5.35×10^5	4.94×10^5	8.08	e/sec/pixel
Current	1.6×10^{-19}	2.64×10^{-15}	3.00×10^{-8}	8.57×10^{-14}	4.95×10^{-11}	8.09×10^{-16}	A/pixel
Current Density	1.32×10^{-13}	2.18×10^{-9}	1.51×10^{-6}	7.09×10^{-8}	6.55×10^{-8}	1.07×10^{-12}	A/cm ²
Side Length	11	11	1408	11	275	275	um

A summary of the previous results, simulated result and experimental results is shown in Table 3 along with a comparison to the goals of the project. The final fabrication sequence came extremely close to meeting the goals. At the designed operating temperature of 200 K it is expected to be a difference of sever electrons per second. The simulated results also demonstrated remarkable similarity to the experimental.

5.3. Junction Lifetime Measurements

Lifetime measurements were performed on fabricated devices using the open circuit voltage decay method. A high speed switch with high input impedance was used to create the open circuit condition. The switch was controlled by a function generator tied to an oscilloscope measuring the junction voltage. A resistor was placed in series with the device to provide a current limiting element. The lifetime is extrapolated by an exponential fit to the experimental data as shown in Fig. 5.9.

The extracted lifetime for the data shown in Fig. 5.9 was about 1 microsecond. This is three orders of magnitude lower than the value specified by the substrate manufacturer although it must be remember this measurement is being made in direct vicinity of the junction. The excess charge creating the junction voltage decays at a faster rate due to high dopant concentrations and defects created during implant. A measurement of the lifetime within the bulk of the device would likely yield different results.

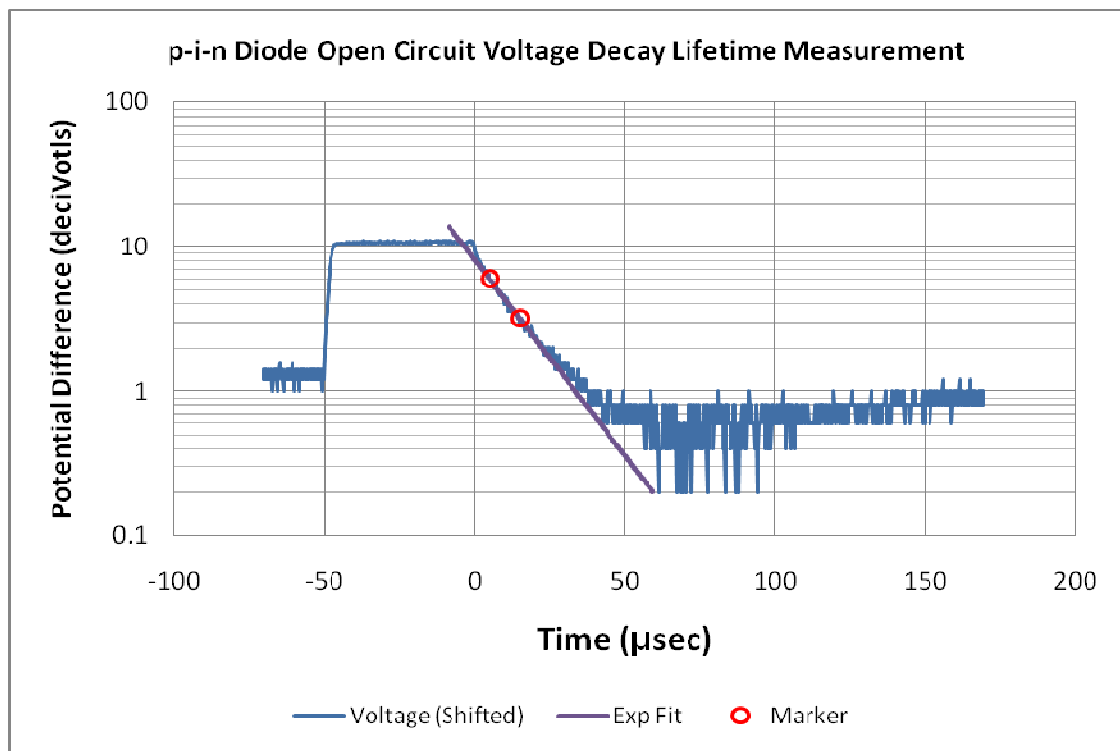


Fig. 5.9 Diode junction voltage decay with exponential fit

5.4. Spectral Response Measurements

The quantum efficiency of fabricated devices was unable to be measured due to a lack of adequate testing equipment, although a similar type of test was able to be performed. The test setup used was designed for solar cell testing and thus allowed for the illumination of specific wavelengths and the ability to measure the current in the device but without an applied bias. The current was measured with the device in a short circuit configuration and the results are shown in Fig. 5.10. A general idea of the spectral response of the device can be observed although no explicit inferences into actual device performance can be made. The device does exhibit a good response all the way up to 1000 nm light.

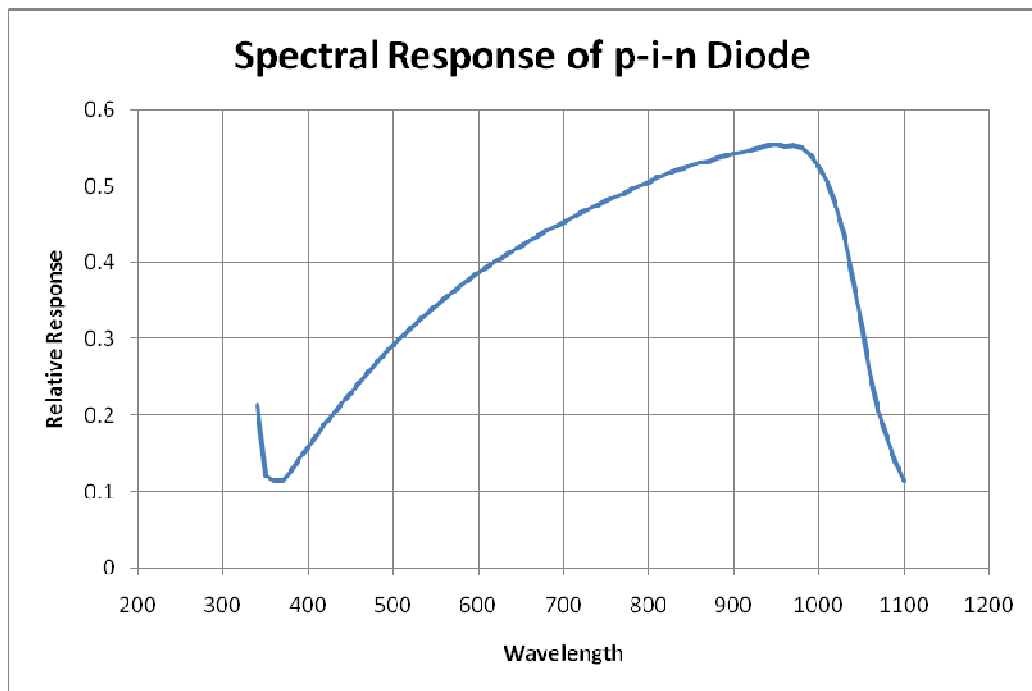


Fig. 5.10 Short circuit spectral response of *p-i-n* diode

Chapter 6

Hybridization

The hybridization technique chosen for this project used a flip chip process with indium bump bonds. A summary of the process is depicted in Fig. 6.1. The wafers were coated with resist and patterned at RIT in the SMFL. The bump bond material was deposited at JPC and the flip chip bonding and packaging took place at STC. The selective deposition of bump bond material was accomplished through a lift-off process. An undercut resist profile is required to create a discontinuous layer for lift-off and several processes were evaluated including negative resists, image reversal, and multilayer stacks. Constraints imposed by the flip chip bonding process and the capillary forces needed for the epoxy under-fill required several microns of spacing between the bonded die. This spacing dictated the required height of the bump bonds, and the thickness of the resist layers needed for the lift-off process. Once coated with indium the lift-off was performed at STC using an N-Methyl-2-pyrrolidone (NMP) solvent stripper with ultrasonic agitation. The parts were then aligned and bonded using the Karl Seuss FC-150. The final step was to fill the space between the chips and bump bonds with an epoxy designed to provide both mechanical stability and protection from moisture and other environmental effects that can lead to corrosion and failure in an under-fill process.

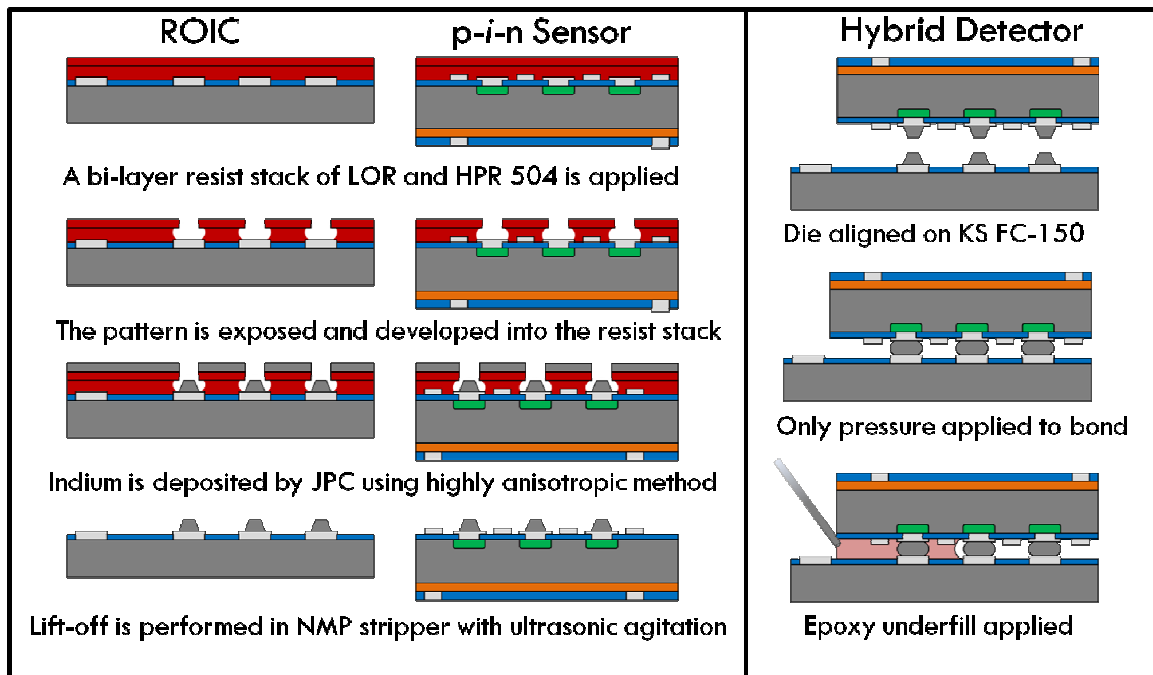


Fig. 6.1 Schematic representation of lift-off and flip chip bump bonding technique used for hybridization process

6.1. Lift-Off Process Development

Metal layers for flip chip bump bonding need to be quite thick relative to the typical thickness of thin films deposited in the semiconductor industry. The bonded die need to be separated by several (~ 3 -5) microns after bonding to allow capillary forces to draw the epoxy in during the under-fill process. The bumps must be even taller than half the die spacing to account for leveling error in the bonding tool, variations in substrate thickness and compression of the bumps during bonding. For this project a bump height of $3\ \mu\text{m}$ was targeted for both diode and ROIC die.

A lift-off process relies upon the ability to create an undercut step height that causes a discontinuity in a deposited material. The discontinuity allows the deposited material to be removed in desired regions where the lift-off material remains. This is easily accomplished for thin layers (up to ~ 500 nm) and there are many standard materials and processes, however thicker layers present unique challenges. A standard rule of thumb in lift-off processing is that resist layers must be ~ 3 -4 times thicker than the material being deposited. To achieve thick resist layers the materials must have a high viscosity and be spin applied at low speeds leading to uniformity issues. The thick layers also pose difficulties for the lithography processes where depth of focus becomes an issue. There is also a tradeoff between the profile of the undercut and the density or proximity of adjacent features

The method of deposition also plays a role in determining the lift-off process. Evaporation is a relatively anisotropic deposition process where the atoms mostly follow a line-of-sight path, although it would be difficult to achieve the desired thicknesses through thermal evaporation. Sputtering is a more isotropic deposition method due to the random collisions that occur in the plasma and requires a more pronounced undercut to ensure the creation of a discontinuity. For these reasons a proprietary process known as Jet Vapor Deposition (JVD) was selected for its high throughput and anisotropy.

Jet Vapor Deposition is a deposition process invented by the Jet Process Corporation that “uses sonic jet nozzles, operating in chambers at ambient temperature (<100° C) and low vacuum (1-5 Torr), to deposit dense, adherent, high quality films at rates far higher than competitive techniques [JPC website].” The process creates a sonic jet of inert gas through a nozzle into which it evaporates the desired material. The material is carried as a vapor to the substrate in a collimated jet with a diameter of about ½”. The jet is then scanned across surface of the substrate by moving either the jet or the substrate. The size of the particles created in the JVD process is relatively large compared to sputtering, and thus their velocities are less affected by random collisions leading to highly anisotropic deposition.

6.1.1 Previous Development Work

A lift-off process was developed by Kolb that utilized a bi-layer resist stack consisting of FujiFilm HPR 504 on Microchem LOR-30A [26]. Microchem LOR is a polymethylglutarimide (PGMI) based ‘lift-off resist’ that acts as the sacrificial layer. The chemical does not contain a photoactive compound and therefore requires a second layer for pattern definition. The solubility of the LOR layer can be tailored by the soft-bake to help achieve the desired profile. Fujifilm HPR504 is the standard g-line photoresist used at RIT for projection lithography on 100 mm substrates.

The LOR-30A was spin coated onto the substrates at 2000 rpm for 45 seconds to achieve a thickness of 4 μm and soft baked at 190 C for 60 sec. The HPR504 was then applied at 2500 rpm for 45 sec and soft-baked at 125 C for 60 sec. The resulting thickness of the total film stack was $\sim 5 \mu\text{m}$. A scanning electron micrograph of a bump bond opening is shown in Fig. 6.2.

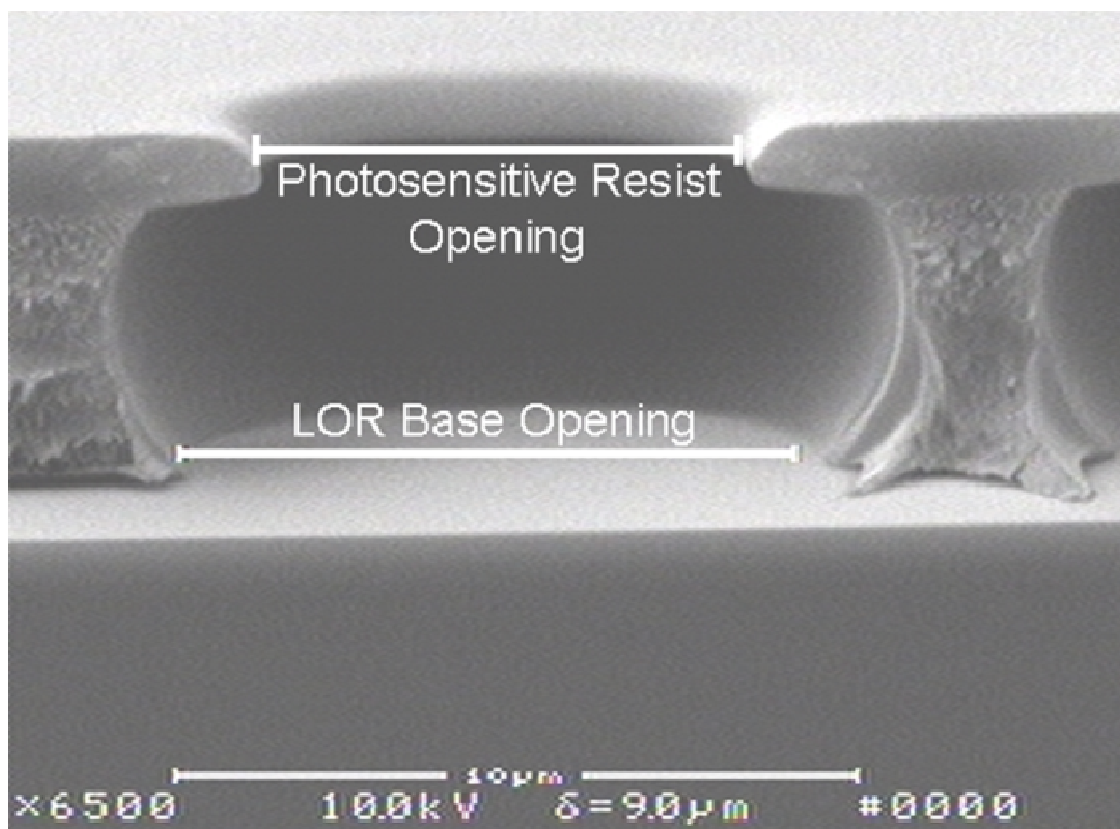


Fig. 6.2 Scanning electron micrograph of bump bond opening in bi-layer resist stack of HPR504 on LOR-30A [26]

The patterned samples were sent to the Jet Process Corporation (JPC) for deposition of the bump bond material. The initial investigation included an evaluation of both indium and gold-tin material systems. The gold-tin alloy provided very low

resistances, oxidation resistance, and the ability to create a eutectic bond and relatively low temperatures, however the presence of gold near the detector poses a contamination concern. The gold-tin alloy also becomes relatively brittle at cryogenic temperatures, and concerns over low temperature operation and contamination led to the selection of indium and the bump bond material.

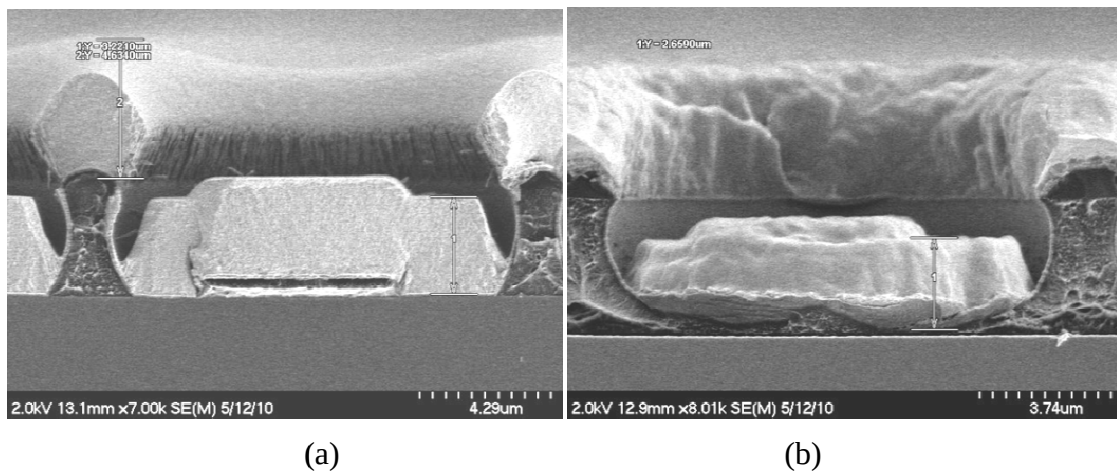


Fig. 6.3 SEM cross-section of bump-bonds after deposition of **(a)** gold-tin **(b)** indium

After deposition, the samples were cleaved along the patterned regions and prepared for imaging. The cross-section SEMs taken through a bump bond are shown in Fig. 6.3 (a) for the gold-tin alloy and Fig. 6.3 (b) for indium. A discontinuous layer of material about three microns thick is achieved with both materials. The size of the features at about ten microns in width is larger than desired due to overdevelopment. The lack of an overhanging structure from the HPR504 is also readily apparent. The absence of this feature contributes to the larger bump size and allows deposition to occur on the

foot of the profile. It is believed these structures were lost during either the pre-clean where the wafers are bombarded with Ar ions or during the subsequent deposition.

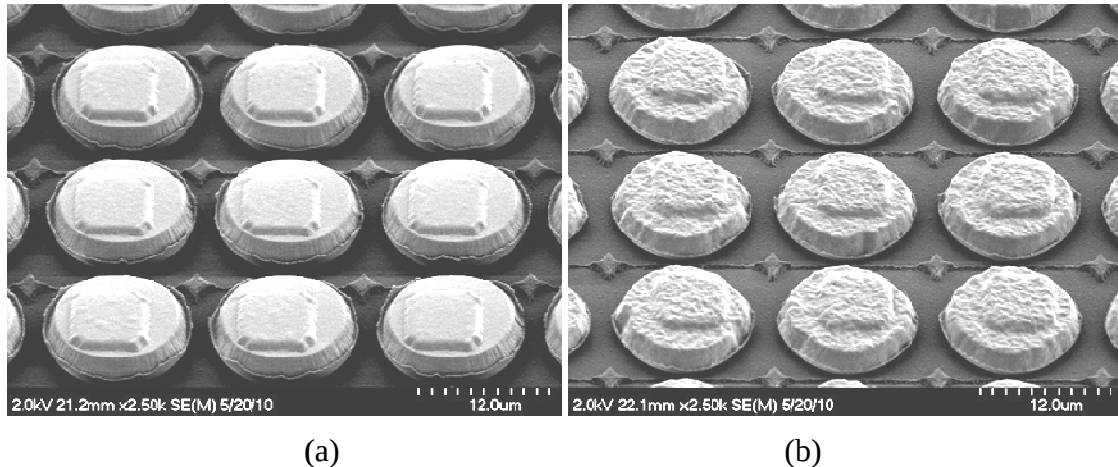


Fig. 6.4 SEM of bump-bond array after lift-off (a) gold-tin(b) indium

The lift-off was successfully performed on several samples aided by the use of ultrasonic agitation. The top down SEMs taken of the bump-bond array are shown in Fig. 6.4 (a) for the gold-tin alloy and Fig. 6.4 (b) for indium. A cupping effect was observed on samples that did not receive the ultrasonic agitation. The work provided an excellent point for further development of the process.

6.1.2 Initial Investigation

Several different processes were initially investigated in an attempt to create an undercut profile that would be mechanically robust enough to withstand the deposition process. Lift-off resists have historically been negative resists as the dissolutions rate are reduced with exposure dose and the exponential decay of absorption readily allowed the

creation of undercut profiles. The resolution limits and need for dangerous solvents as developers phased out their use however the same concept can be applied to positive resists with an image reversal process. The previous process by Kolb, *et al.* was reproduced for comparison, and a bi-layer process with a much thicker top layer was evaluated. SEMs of the resulting resist profiles can be seen in Figure 6.5

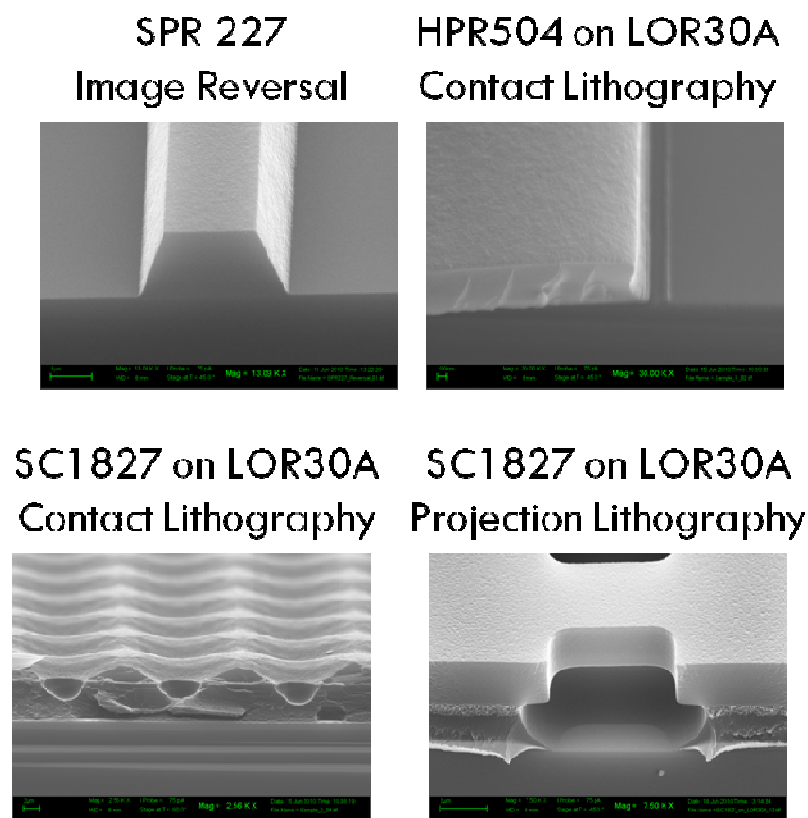


Fig. 6.5 SEM cross-section of resist profile after development for various processes

The image reversal technique involved the use of an ammonia bake and flood exposure process that proved difficult to recreate. The performance of the contact lithography system significantly affected the profile of standard process. The resolution

of the system varied quite dramatically across the wafer, most likely due to variation in the gap between the wafer and reticle. In a new bi-layer process Shipley SC1827 photoresist was used to create a much thicker photoactive layer. This would require a large depth of focus and further drove the need to move to a projection system. The third SEM in Figure 6.5 shows the massive amount of diffraction introduced by the contact system. The profile from the SC1827 on LOR30A process using projection lithography was very promising and displayed all the desired features.

6.1.3 SC 1827 on LOR-30A Development

A simple two factor designed experiment was performed on the lift-off process varying the soft-bake and development time to optimize the resist profile. Several features were identified as key elements evaluated in the profile including the amount of overhang of the top layer beyond the base of the feature, the total undercut and the thickness loss of the top resist layer. The features were evaluated with both optical and scanning electron microscopes. The translucent nature of the materials allowed both layers to be observed with visible light and provided a clear indication of the amount of undercut. The samples were cleaved to allow the SEM to obtain a cross-section of the features. The results for a soft-bake temperature of 190° C at several different development times is shown in Fig. 6.6

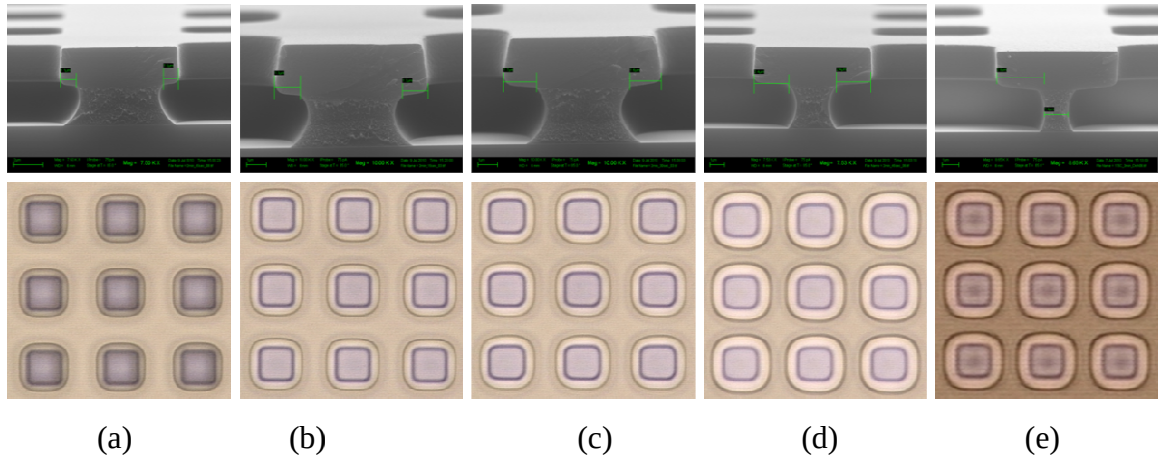


Fig. 6.6 SEM cross-section and correlating optical micrograph of bump-bond opening in bi-layer resist stack for 190 C soft bake and development times of **(a)** 120 sec **(b)** 135 sec **(c)** 150 sec **(d)** 165 sec and **(e)** 180 sec

A two stage soft bake was utilized based on a manufacturer recommendation with an initial temperature of 160° C and a final soft bake temperature of 190° C for 60 sec each. The temperature was found to not have a significant impact on the profile of the LOR layer. The most important factor affecting the profile of the LOR layer was the method of development. A puddle develop process with manual agitation was first used, however this resulted in an extremely slanted profile. This is most likely due to a transport limited mechanism slowing development at the bottom of the feature. The switch to a continuous spray-develop process created much more vertical profiles. The soft-bake temperature was then chosen at the higher end of the defined range to reduce develop times and chemical consumption. A develop time of 150 sec was chosen as the

feature in Fig. 6.6 (c) was determined to have enough undercut to allow for process variations while maintaining the mechanical integrity of the overhang.

6.1.4 Indium Deposition

Samples were prepared with the new process of record and again sent to JPC for indium deposition. The samples were prepared for deposition in the same manner as the previous samples. An argon ion pre-clean was followed by 100 nm of chrome and 1000 nm of gold. Three microns of indium was then deposited on the samples. Some samples were imaged as-deposited while other underwent the lift-off process with ultrasonic agitation before imaging. A SEM of the as deposited sample is shown in Fig. 6.7.

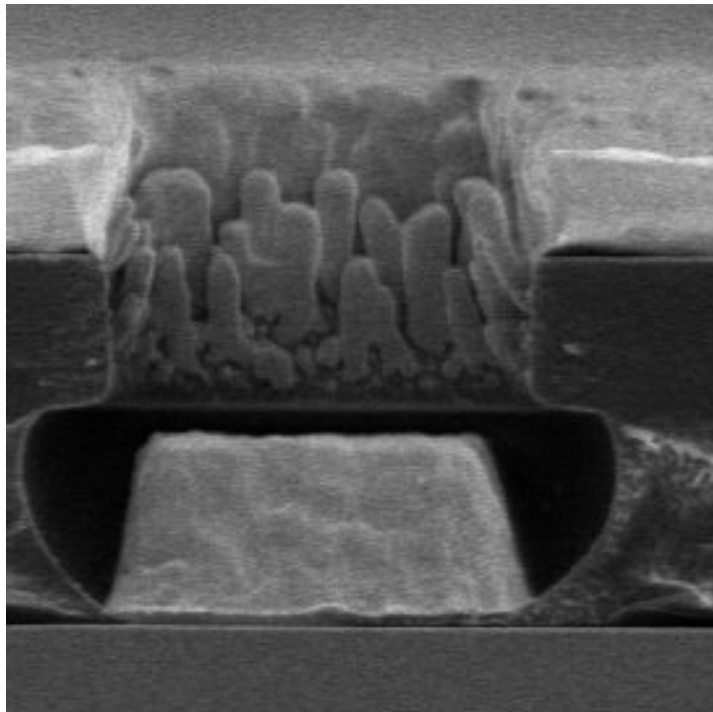


Fig. 6.7 SEM of new thick bi-layer LOR process after deposition of 3 μm of indium

The results were exactly as desired, where a discontinuous indium layer was formed with a bump of the desired size and height. The slight angle to the resist profile caused deposition to occur on this surface creating stalagmite type features. This resulted in a shadowing effect during deposition giving the indium bump a slight taper. The unintended side effect is that it prevents the layers from connecting. This could also allow bumps of even greater heights to be created. The taper also helps to prevent shorting between adjacent bumps as they expand during compression.

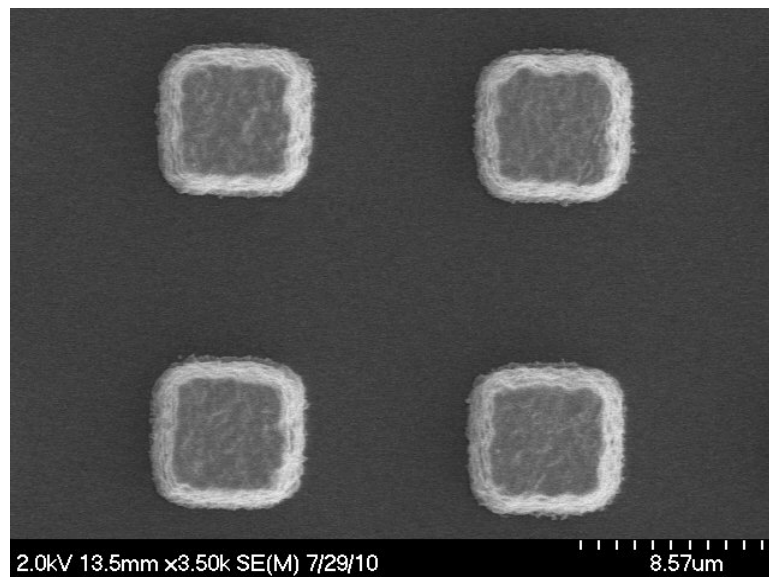


Fig. 6.8 SEM of several 3 μm tall indium bumps after lift-off of excess material

A top-down SEM of several indium bumps is shown in Fig. 6.8. The bumps are six microns wide at the base narrowing to a width of about 4 microns at the top on 15 micron pitch. Although the samples appeared slightly under-developed due

to the foot of the LOR profile extending all the way to the base of the bump, there were no adhesion issues observed during lift-off.

6.1.5 SC 1827 on Double-Coat LOR-30A

During the course of the project the need for a much thicker ($\sim 5\ \mu\text{m}$) indium layer on the detector side of the device arose. The driving factor for this need is discussed at length in Section 6.2. The obvious course of action was to increase the thickness of the sacrificial LOR layer in the bi-layer process. The spin coating was already being performed at the lowest recommended speed, so a second layer had to be applied. The second coating was applied at a much higher speed to achieve the best uniformity. Any irregularities in the initial coating are exaggerated by the second coating.

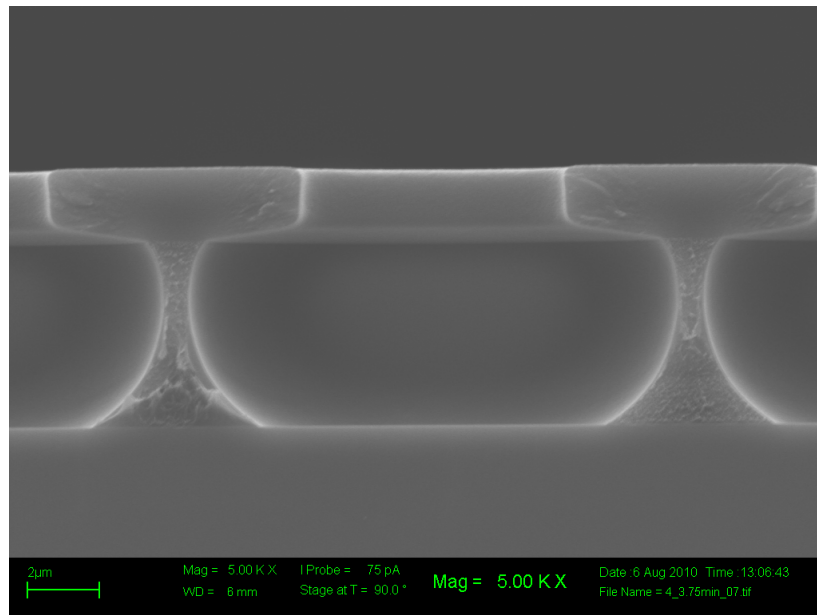


Fig. 6.9 SEM of bi-layer resist process with two LOR layers

The standard two stage soft-bake process was performed after each layer was applied. The thicker sacrificial layer required the develop time be increased to 210 sec. The resulting profile shown in Fig. 6.9 has a 5.8 μm thick LOR layer with a sufficient overhang. It can be noted that the density of the features and the profile of the LOR layer impose a limit on the maximum allowable thickness of this layer. The neck of the feature must remain to prevent the resist layer from collapsing.

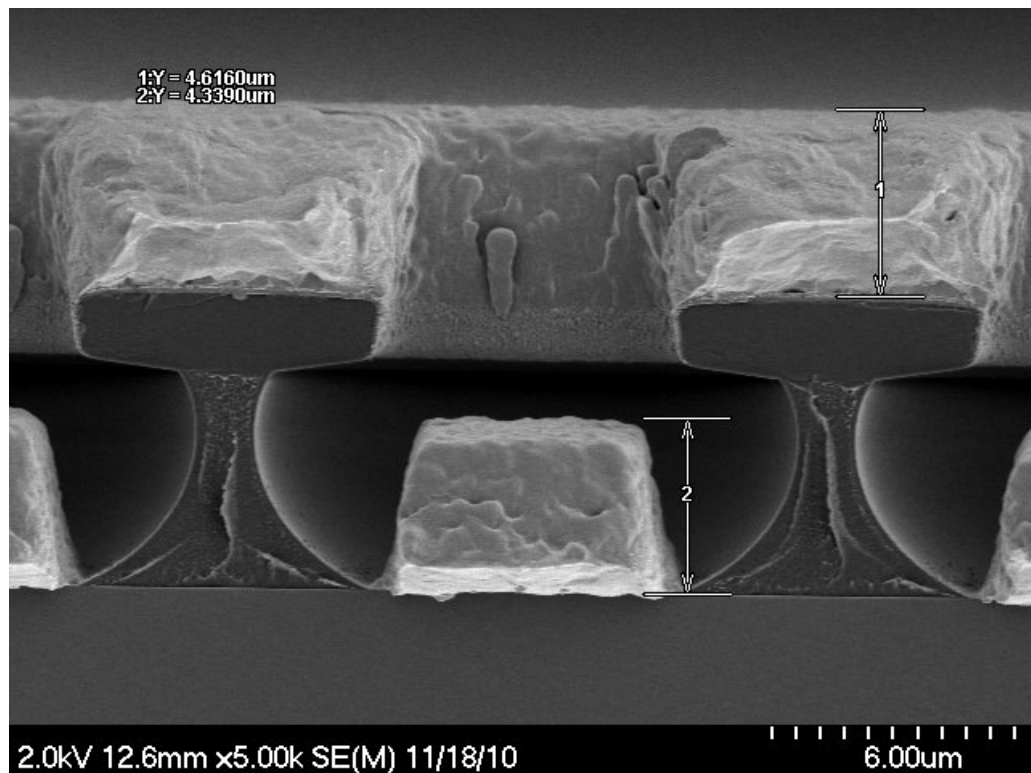


Fig. 6.10 SEM of thick bi-layer resist process after 4.6 μm of indium deposition

The samples prepared with the double LOR coat process were sent to JPC where 4.6 μm of indium was deposited. A cross-section SEM of the sample is shown in Fig. 6.10 through the bump bond array. The taller bump is clearly discontinuous from the

rest of the film by several microns, a promising result. Although the resist sidewall is angled slightly outward in this sample, the feature opening still shrinks slightly as deposition proceeds. This results in a similar tapered profile to the bump, although at a steeper angle than before.

6.2. ROIC Passivation Cut

The read-out integrated circuits (ROIC) for the project were fabricated through the MOSIS service at TSMC using the 4-poly 2-metal process. Due to an oversight in the design, the ROICs were defined with passivation openings on the wire-bond pads, but not the bump bond pads. Since lithography already needed to be performed on the ROIC chips for bump bond metal deposition, a plasma etch was used to open the passivation layer above the bump bond pads before deposition. The locations that needed to be etched were the same as those needing the bump bond metal, so only a single photo-mask was required.

There were many challenges involved with transferring a pattern to a small irregularly shaped substrate. The small size made aligning a pattern to the die difficult and allows only a single point of observation. The irregular shape creates turbulence when spinning the substrate creating large edge beads in viscous coatings. To overcome these challenges several custom vacuum chucks were fabricated. The first was milled out

of plastic with a recessed pocket designed to fit the ROIC die and a vacuum hold to be used for spin coating. The recessed pocket moved the turbulent air away from the edge of the die and significantly reduced the size of the edge beads. The second chuck was designed for the contact lithography tool in tandem with the photo-mask. Two recessed pockets were placed underneath each of the alignment microscopes to allow both to be utilized. A mask was designed with an array of 84x84 openings each 7 microns large at those same locations.

Although no specific details were given as to the thickness or composition of the passivation layer, it was stated to be an oxide, nitride, or oxynitride that was between 0.5 and 2 microns thick. The thickness was confirmed to be very nearly one micron through a profilometer measurement made at the wire-bond pad opening. The composition of the layer was investigated using both ellipsometry and energy dispersive x-ray spectroscopy and was determined to be an oxynitride. This was confirmed by attempting to etch a sample in hydrofluoric acid, which had no effect. A dry etch process was developed in a plasma etch system with fluorine based chemistry. A very low power was used to minimize the amount of resist degradation that occurred during the etch. A thick resist could not be used due to the size of the edge beads when attempting to spin coat the sample.

The samples were spin coated with HPR 504 at 8000 RPM for 45 sec and soft baked at 125 °C for 60 sec. They were aligned and exposed on the contact lithography tool with a dose of 160 mJ/cm². After a 300 sec etch in CF₄ at 10 mTorr the samples were imaged and one was cleaved and prepared for the SEM. An optical micrograph can showing etched bond pads adjacent to dummy bond pads that were not etched can be seen in Fig. 6.11

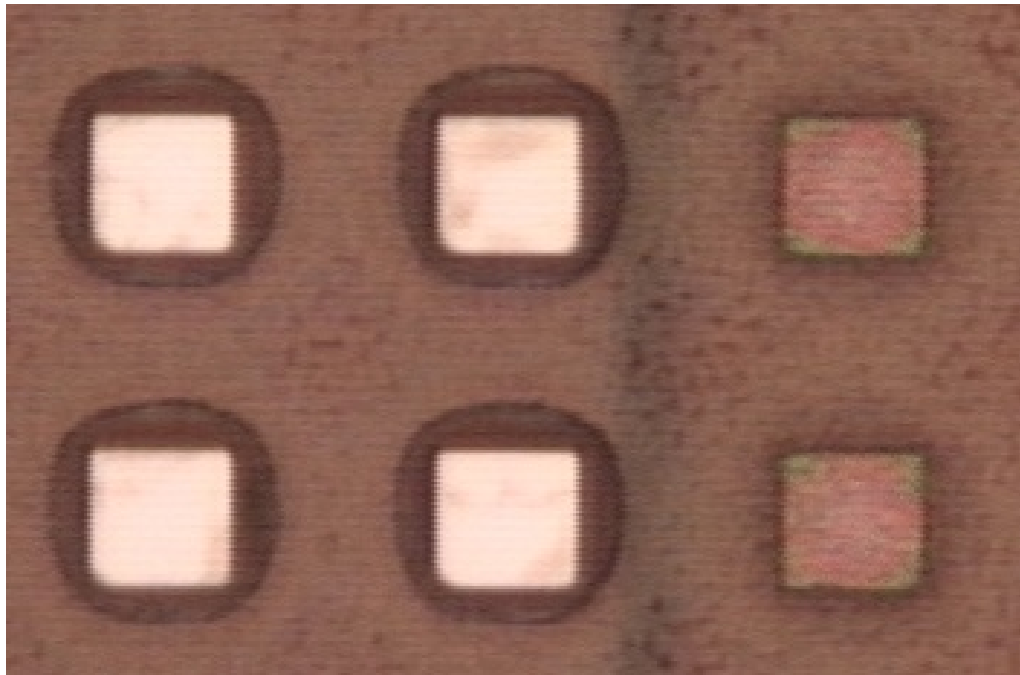


Fig. 6.11 Optical micrograph of etched and un-etched bump bond pads

The surface of the resist became very rough after the etch process, and although a significant thickness loss was not observed the size of the opening was much larger than designed. It was believed several process biases contributed to the enlargement of the feature. The presence of edge beads reduced the focus of the lithography process and the

resulting diffraction enlarged the features slightly. During the plasma etch process the edges of the bond pads magnified the electric fields increasing the etch rates and further bloating the features size. An SEM cross-section through an etched bond pad is shown in Fig. 6.12. The features were sent out for indium deposition and although pictures are unavailable lift-off was successfully performed.

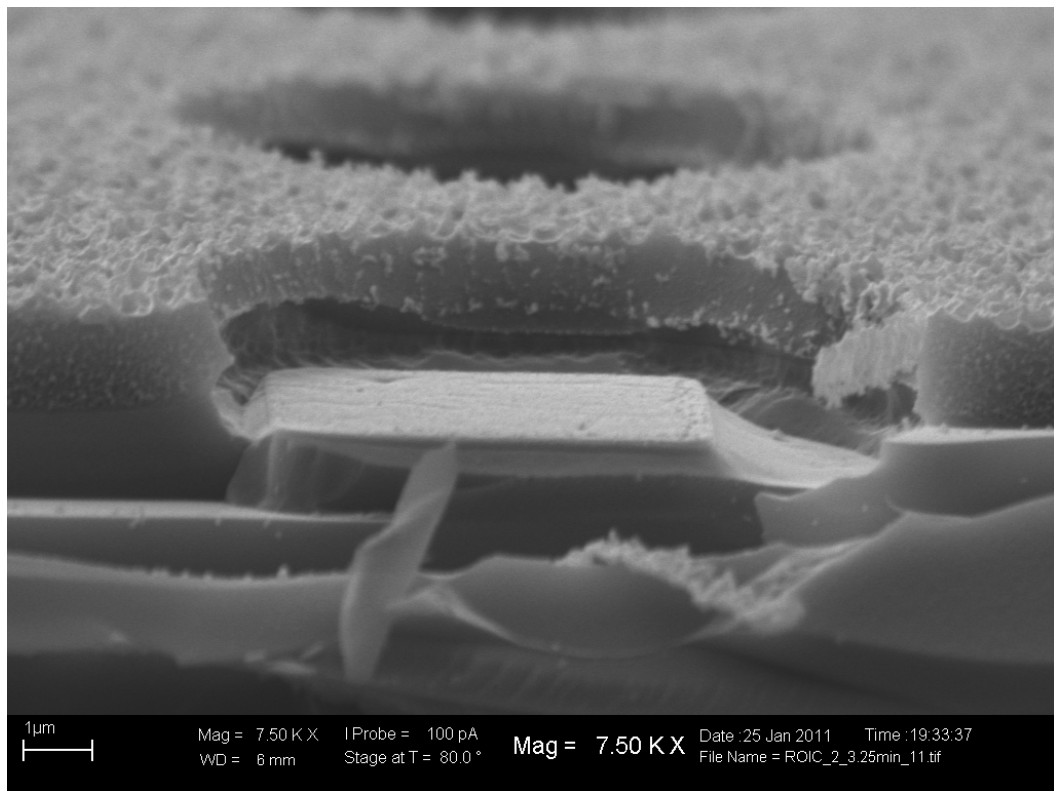


Fig. 6.12 SEM cross-section of ROIC die through etched bond pad

6.3. Bump-Bond Daisy Chain Test Parts

Test parts were created to evaluate the hybridization process and characterize the mechanical and electrical strength of the bonds. The electrical characteristics of the bump bonds were determined by connecting every other bump in the array and shifting

the pattern by one bump on the opposing array in a 'daisy-chain' fashion. At the top and bottom of the array on the fake ROIC die connections are made to each column and connected together in a serpentine fashion. The connections also fan out to arrays of larger pads to be used for manual probing. On the left and right side of the array connections are made to individual bumps allowing any two bumps on the edges to be measured. A screen capture of the bump-bond daisy chain ROIC test part VLSI layout is shown in Fig. 6.13.

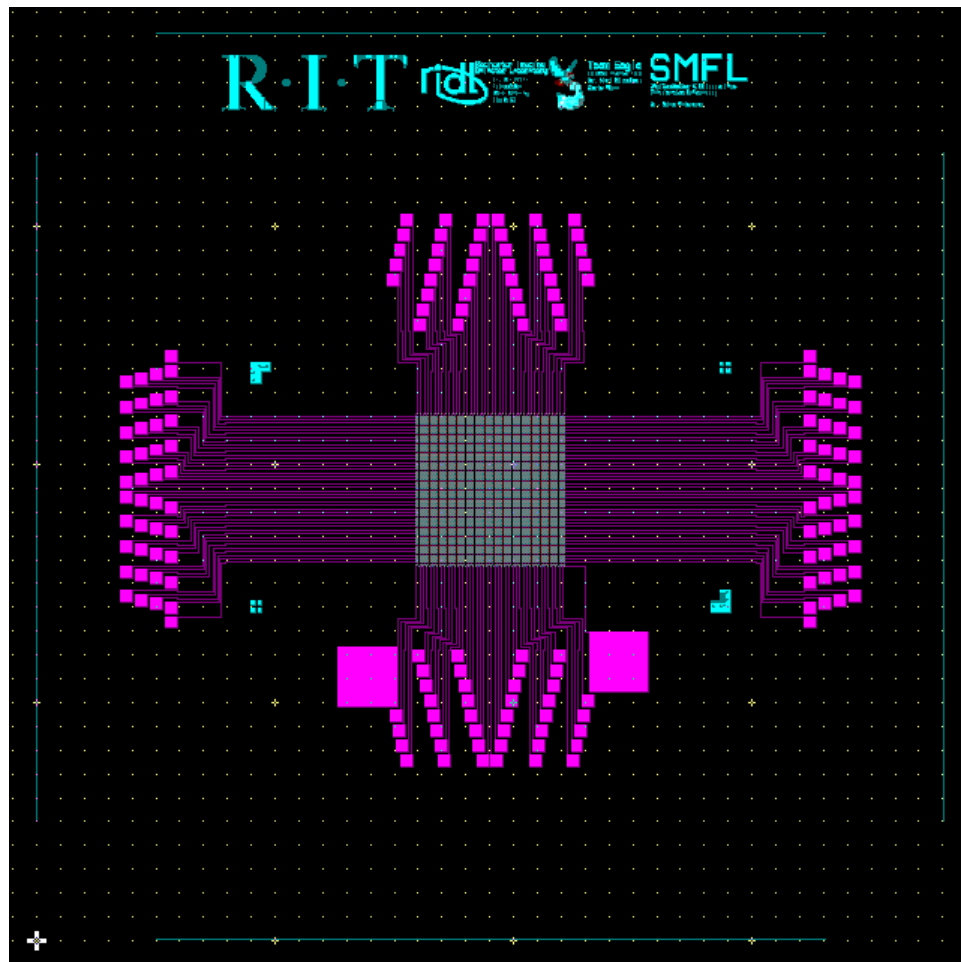


Fig. 6.13 Screen capture of bump-bond daisy chain ROIC test part VLSI layout

A thermal oxide was grown first to electrically insulate the devices from the silicon substrates. An aluminum layer was deposited and patterned with the bump bond and probe connection layer. The test parts were coated with the same passivation layer from the diode fabrication process and patterned with the same contact cut opening design. The samples were wet etched in a pad etch solution and the resist stripped in a heated solvent bath. The ROIC test part wafer received the standard LOR process with a single coating of the LOR layer while the diode test part wafer received the thicker process with the two coatings of the LOR layer. The wafers were sent to JPC and the diode and ROIC parts were deposited with five and one microns of indium respectively. The intention was to mimic the real parts as closely as possible while still ensuring the greatest chance of success.

6.3.1 Physical Testing

The parts were sent to STC where the indium lift-off was performed with the ultra-sonic agitation. A protective coating was applied, the wafers were diced and individual samples were removed and prepared for bonding. A hydrogen peroxide etch was utilized directly before bonding to remove the native oxide. The parts were aligned and bonded in the Karl Seuss FC-150 using only applied pressure. Bonded parts were

observed with infra-red imaging and a few samples were separated and imaged with an SEM. Electrical measurements were also made of bonded test parts.

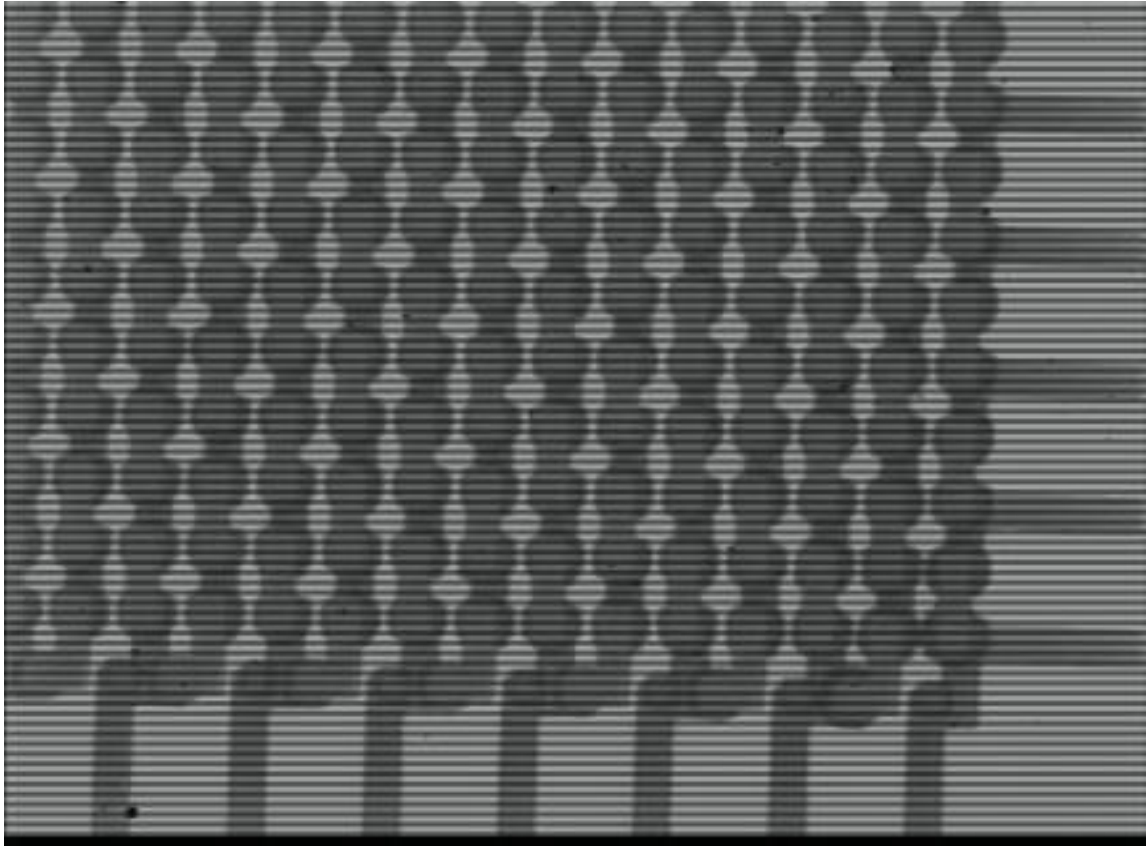


Fig. 6.14 Infra-red optical micrograph of the corner of the bump bond array

The infra-red image of the bump bonds in Fig. 6.14 shows good alignment of the parts and the connections between bumps and to probe pads. Some expansion of the bumps is visible due to the compression when forming the bond. No shorting of adjacent bumps is observed throughout the entire array. This indicates a good mechanical bond was formed between the bumps on the two die.

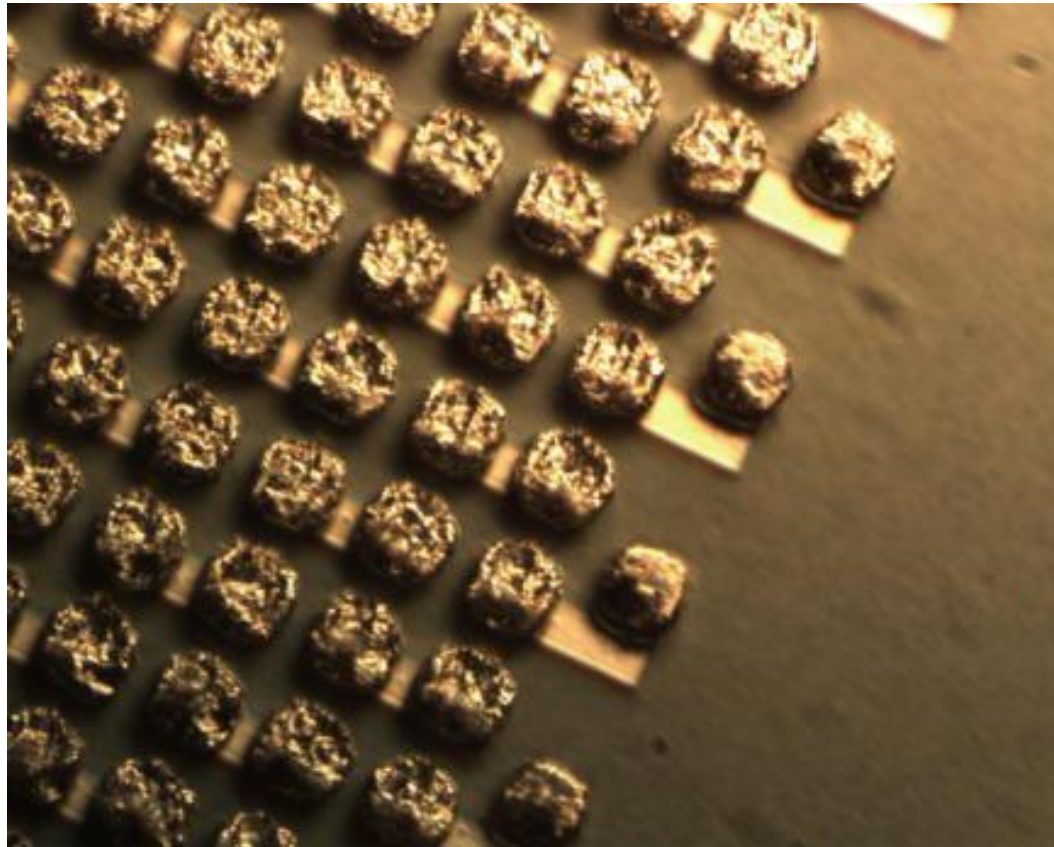


Fig. 6.15 Optical micrograph of 5 μm thick indium bumps after bonding and separation

An optical micrograph of the thicker five micron indium bumps after bonding and separation is shown in Fig. 6.15. A clear depression can be seen in the top of the features as the thicker indium bumps deformed significantly more than the thinner counterparts on the ROIC test die. An SEM image of one of the thinner bumps after bonding and separation is shown in Fig. 6.16.

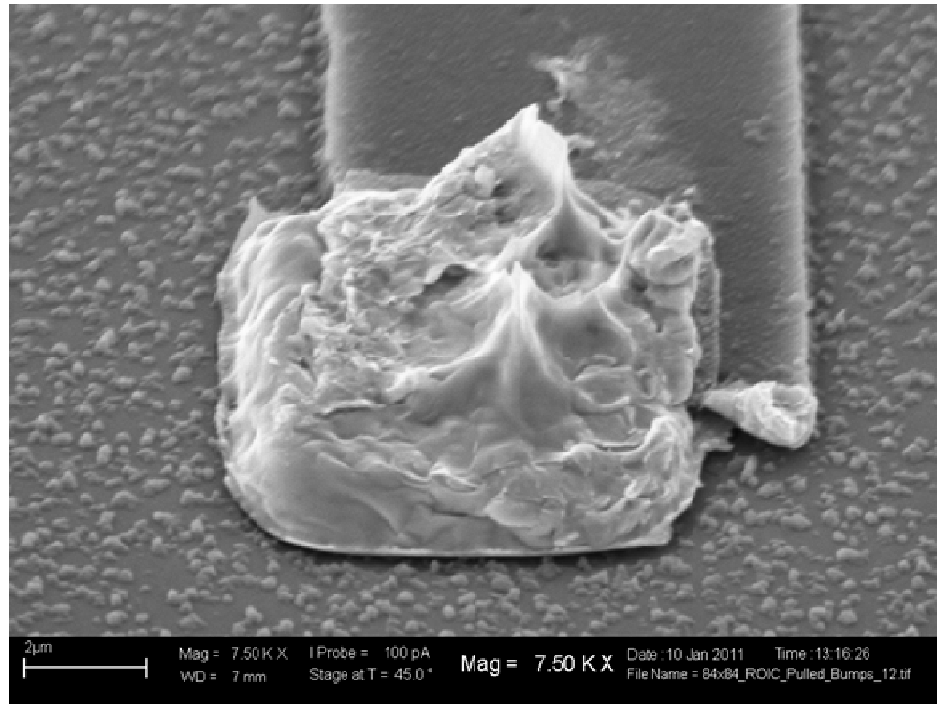


Fig. 6.16 SEM of 1 μm indium bump after bonding and separation

In Fig. 6.16 the indium bump is seen on the aluminum contact pad with pointed features rising out of it. These features are the classic result of the necking and eventual fracture of a piece of metal. The presence of these features indicates a good mechanical bond was formed between the two indium bumps.

6.3.2 Electrical Testing

The resistance of each of the 84 columns in the active array was measured to be about $20\text{ M}\Omega$ as shown in Fig. 6.17. The actual resistances of each column varied slightly but all measurements were many orders of magnitude higher than expected. The results were similar for several tests parts and even when measuring smaller numbers of bumps using the side contacts.

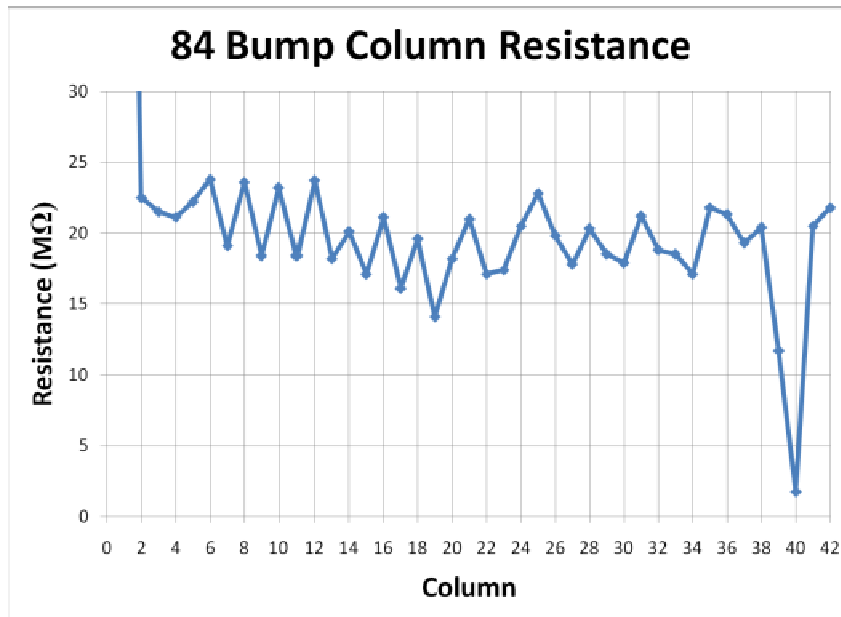


Fig. 6.17 Measured resistance of columns of 84 bump bonds

It was observed however that after the application of a small current through the bumps the current was dramatically reduced. For a pair of bumps the initial resistance of about 200 kΩ could be reduced to about 200 Ω. A current of at least 50 mA was needed to achieve the maximum reduction in resistance. This indicated a contact oxide was present that would breakdown after application of a current. Unfortunately this same type of contact healing through current drive is not available on the experimental devices. This is a major concern for the functionality of the device and an area that requires further development.

6.4. Final Hybridized Devices

Two fully processed *p-i-n* diode wafers patterned with the double layer LOR process were sent to JPC along with five patterned and etched ROIC die. The samples

received five and one micron of indium deposition respectively, and were sent to STC for lift-off and bonding. The two diode wafers sent were the lowest measuring leakage currents from the final two processing runs for which the data was presented in Chapter 5. Unfortunately the wafer from the final run representing the best results to date was determined to be mis-aligned between the front and back.

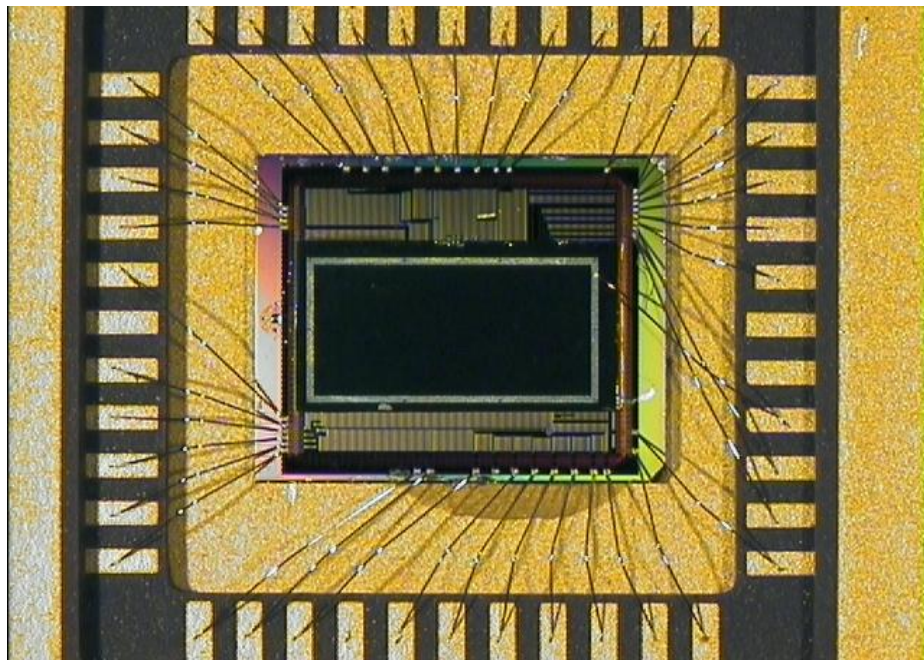


Fig. 6.18 Image of a hybrid *p-i-n* CMOS imaging system wire-bonded in DIP

The lift-off was successfully performed on four of the five etched ROIC die and they were bonded to diode arrays. The bonded die were then affixed to a dual in-line package (DIP) and wire-bonded. An image of the hybrid *p-i-n* CMOS imaging system ready for testing is shown in Fig. 6.18. Testing is currently ongoing at the Center for Detectors laboratory at RIT.

Chapter 7

Final Remarks

In conclusion the project has been deemed largely successful, although there are still many areas that can be improved upon. The leakage measurement results achieving within an order of magnitude of the stated goals are a testament to the quality of devices that can be produced using the manufacturing processes offered at the SMFL. Despite the fact that an imaging system was produced at the completion of the project there were many stumbling blocks and unforeseen issues along the way that could provide beneficial learning opportunities for future projects.

Some of the lessons learned relating to the design of the diode include operating at higher over-depleted biases, incorporating a back side guard ring, and further optimization of passivation and anti-reflection coatings. The simulations performed for project showed in agreement with literature that over-depleted biasing conditions are critical for minimizing pixel cross talk in thick detectors. The incorporation of a guard ring structure on the backside of the devices would help to prevent the depletion region from reaching the edge of diced imagers mitigating surface leakages. The design of the ARC layer could also be further optimized using a nitride passivation layer to further reduce reflections across a broader range of wavelengths.

The hybridization process was quite successful for a prototype device with bonded imagers being produced. The measured bump bond contact resistances were extremely large prohibiting device operation. A further analysis of the deposition pre-clean process is required to investigate possible interfacial layers. The use of under bump metallization layers electrochemically applied has also been shown to be a successful process alternative.

The oversight in ensuring opening in the passivation layer of the ROIC proved to be one of the most difficult challenges of the entire project to overcome. The development a process to pattern an etch individual die was critical to enabling the success of the project. The lesson from this challenge is the constant attention to detail required at every aspect of the project.

Appendix I Typical Atlas Input File

```
#####
#### Rochester Image Detector Laboratory & Team Strongarm
#### APRA Diode
#### Atlas Simulations
#### Reverse Bias Characteristics & Spectral Response
#### revision 5.9
#### 5 Pixel Structure: Wavelength Varied
#### Chris Shea
#### Friday, April 16, 2010
#### cgs4706@rit.edu
#####
go atlas
#
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set W=75
setVb=50
set T=300
set L=0.1
set Tau0=1e-3
set Ns=1e20
setXj=0.5
set rev=5.9
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y.meshloc=20.0 spacing=2.5
y.meshloc=$Th-10 spacing=2.5
y.meshloc=$Th-2 spacing=0.05
y.meshloc=$Th spacing=0.05
#
# SECTION 2: Structure Specification
#
regionnum=1 x.min=-$W/2 x.max=$W/2 y.min=0 y.max=$Th material=Silicon
#
elecnum=1 name=cathode top
elecnum=2 name=anode x.min=-3.5 x.max=3.5 y.min=$Th y.max=$Th
elecnum=3 name=nwellx.min=-18.5 x.max=-11.5 y.min=$Th y.max=$Th
elecnum=4 name=pwellx.min=11.5 x.max=18.5 y.min=$Th y.max=$Th
elecnum=5 name=ndrainx.min=-33.5 x.max=-26.5 y.min=$Th y.max=$Th
elecnum=6 name=pdrainx.min=26.5 x.max=33.5 y.min=$Th y.max=$Th
#
#
doping uniform conc=1e12 n.type
dopinggaus peak=0.0 junction=$Xjconc=$Ns n.typedir=y
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=-3.5 x.max=3.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=-18.5 x.max=-11.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=11.5 x.max=18.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=-33.5 x.max=-26.5
dopinggaus peak=$Th char=0.3 lat.char=0.3 conc=1e20 p.typex.min=26.5 x.max=33.5
regrid region=1 doping ratio=1.25 logarithm max.level=1 smooth.k=4
#
```

```

# SECTION 3: Material Model Specification
#
material taup0=$Tau0 taun0=$Tau0
models temperature=$T srh auger cvtfermibgn
interface optical ar.index=1.45 ar.thick=0.1030 p1.x=0.0 p1.y=0.0 p2.x=0.0 p2.y=0.0
method newton trap clim.dd=1e-5
#
# SECTION 4: Optical source specification
#
beamnum=1      rays=150      x.origin=0      y.origin=-1.0      angle=90.0      wavelength=$L
front.reflambient.index=1.0
beamnum=2      x.origin=0      xmin=-0.25      xmax=0.25      y.origin=-1.0      angle=90.0      wavelength=$L
front.reflambient.index=1.0

#
# SECTION 5: Initial Solution & Reverse Bias IV
#
solveinitoutf=APRA_rev$'rev'_L$L'_Tau$'Tau0'_T$'T'_W$'W'_init.str master
tonyplot
#
log outfile=APRA_IV_rev$'rev'_L$L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log
probe name="Recombination rate" integrated srhx.min=0 x.max=15 y.min=0 y.max=250
solveprevvcathode=0.5 vstep=0.5 vfinal=$Vb/5 name=cathode
tonyplot
solveprevvcathode=$Vb/5 vstep=0.5 vfinal=$Vb name=cathode
log off
tonyplot      APRA_IV_rev$'rev'_L$L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log
structoutf=APRA_rev$'rev'_L$L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.str
tonyplot      APRA_rev$'rev'_L$L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.str
measureu.total
#
# SECTION 6: Spectral Response
#
log outf=APRA_Spectral_rev$'rev'_Ns$'Ns'_Xj$'Xj'_Tau$'Tau0'_T$'T'_V$'Vb'.log master
solveprev b1=1 beam=1 lambda=0.1 wstep=0.01 wfinal=1.3
log off
tonyplot      APRA_Spectral_rev$'rev'_Ns$'Ns'_Xj$'Xj'_Tau$'Tau0'_T$'T'_V$'Vb'.log      -set
APRA_Spectral.set
quit

#
# SECTION 7: Spatial Response
#
log outf=APRA_Spatial_rev$'rev'_L$L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log master
solveprev b1=1 scan.spot=1
log off
tonyplot      APRA_Spatial_rev$'rev'_L$L'_Tau$'Tau0'_T$'T'_W$'W'_V$'Vb'.log
quit

```

Appendix II Process Flow

TABLE I. KEY FOR PROPOSED PROCESS FLOW

Thermal	Lithography	Wet Chemistry	Plasma Deposition & Etch	Implant	Measure
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TABLE II. PROPOSED PROCESS FLOW

#	Step	Process Parameters	Process Details and Comments	Record	Wafers
1	Create Lot Notebook	Obtain a Cleanroom notebook, a previous notebook can be used Update and insert the file located in: \\kgcoe-file\morbo-eagle\RIDL	Tape into the notebook: •Process Flow (this document) •Important Lot Processing Information Sheet •Implant settings		All Device Wafers
2	Scribe	Tool: Diamond Tips Scribe Print out wafer box label and tape it on 4" polypropylene box	The bulk wafer can be found in XXXXXXXX box 5000 ohm-cm		All Device Wafers
3	Grow Oxide	Tool: Bruce Furnace Tube: 4 Recipe: ??? "1000 Å Oxide"	Do Not use dummy wafers	Print Thermal History Include Profiles, N2, & O2	All Device Wafers
4	Oxide Thickness Measurement	Tool: PrometrixSpectramap Recipe: ?	Save Spectramap data to disk and copy to Morbo	M1 Mean: _____ Å Std. Dev: _____ Å Min: _____ Å Max: _____ Å C2	All Device Wafers
5	Coat BBS	Tool: CEE 100 Resist Spinner Recipe: 9 & 0 Do Not use SVG Track (backside resist splattering)	Dehydration Bake: 60 sec @ 150 °C Spin Coat Microprime P20: 15 sec @ 5000 RPM Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
6	Coat LAS	Tool: CEE 100 Resist Spinner Recipe: 9 & 0 Do Not use SVG Track (backside resist splattering)	Spin Coat Microprime P20: 15 sec @ 5000 RPM Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
7	LAS Litho Level I: Alignment	Tool: Karl Seuss MA150 Recipe: adr Level: I Mask: Alignment	Dose: 150 mJ/cm2 Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
8	BBS Litho Level I: Alignment	Tool: Karl Seuss MA150 Recipe: adr Level: I Mask: Alignment	Dose: 150 mJ/cm2 Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
9	Develop BBS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
10	Develop LAS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
11	Oxide Etch	Tool: Manual Wet Bench Bath: MOS Grade 5.2:1 HF:H2O	Thermal Oxide Etch Rate: ~ 1200 Å/min Time: 1 min		
12	Silicon Etch	Tool: Drytek Quad Recipe: ??? Chamber #1 -Al Carrier Power: 50 W Pressure: 100 mT SF₆: 50 sccm Chiller temperature: 38°C Time: 0:20 m:s	Make sure chiller temperature has been set to 38°C Run a clean&season with Al carrier wafer Etch both sides of all wafers		
13	Resist Strip	Tool: Wet Bench Solvent: PRS2000 Temp: 90°C Time: 10 min (each bath)			
14	Implant LAS Side	Tool: Varian 350D Dose: 2e15 cm ⁻³ Energy: 75 keV Species: P ₃₁	Target Peak Depth: 1074 Å		All Device Wafers

15	Coat BBS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Dehydration Bake: 60 sec @ 150 °C Spin Coat Microprime P20: 15 sec @ 5000 RPM Bake: 60 sec @ 150 °C Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
16	BBS Litho Level II: P-Well	Tool: Karl Seuss MA150 Recipe: adr Level: II Mask: P-Well	Dose: 150 mJ/cm2 Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
17	Develop BBS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
18	Implant LAS Side	Tool: Varian 350D Dose: 4e15 cm⁻³ Energy: 35 keV Species: B₁₁	Target Peak Depth: 1455 Å		All Device Wafers
19	Resist Strip	Tool: Branson Asher Recipe: 4" Hard Ash			
20	APM Clean	Tool: Manual Processing Bench# 2 SCA1: 1:3:15 :: NH ₄ OH:H ₂ O ₂ :H ₂ O NH ₄ OH: 300mL H ₂ O ₂ : 900mL H ₂ O: 4500mL Time: 10 min Temp: 75 °C	Spike with 100 mL of H ₂ O ₂ if old	Fill out log Sheet for chemicals added or changed.	All Device Wafers
21	HPM Clean	Tool: Manual Processing Bench# 2 SCA1: 1:3:15 :: HCl:H ₂ O ₂ :H ₂ O HCL: 300mL H ₂ O ₂ : 900mL H ₂ O: 4500mL Time: 10 min Temp: 75 °C	Spike with 100 mL of H ₂ O ₂ if old		All Device Wafers
22	BBS Oxide Dep	Tool: AMat P5000 Thickness: 4000 Å of TEOS Chamber: A Recipe: A6-4000A TEOS LS	Deposit on the Bump Bond Side of the wafer Use TEOS Si Carrier wafer		All Device Wafers
23	Oxide Thickness Measurement	Tool: Prometrix Spectramap Recipe: ?	Save Spectramap data to disk and copy to Morbo	M1 C2 Mean: _____ Å Std. Dev: _____ Å Min: _____ Å Max: _____ Å	All Device Wafers
24	Anneal	Tool: Bruce Furnace Tube: 4 Recipe #: 444 "Shea RIDL Anneal"	Do Not use dummy wafers	Print Thermal History Include Profiles, N2, & O2	All Device Wafers
25	Oxide Thickness Measurement	Tool: Prometrix Spectramap Recipe: ?	Save Spectramap data to disk and copy to Morbo	M1 C2 Mean: _____ Å Std. Dev: _____ Å Min: _____ Å Max: _____ Å	All Device Wafers
26	Coat BBS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Dehydration Bake: 60 sec @ 150 °C Spin Coat Microprime P20: 15 sec @ 5000 RPM Bake: 60 sec @ 150 °C Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
27	Coat LAS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Spin Coat Microprime P20: 15 sec @ 5000 RPM Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
28	LAS Litho Level III: Contact	Tool: Karl Seuss MA150 Recipe: adr Level: III Mask: Contact	Dose: 150 mJ/cm2 Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
29	Develop LAS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
30	Oxide Etch	Tool: Manual Wet Bench Bath: MOS Grade 5.2:1 HF:H2O	Thermal Oxide Etch Rate: ~ 1200 Å/min Annealed TEOS Etch Rate: ~ 2029 Å/min Time: 3:30 min		
31	Resist Strip	Tool: Wet Bench Solvent: PRS2000 Temp: 90°C Time: 10 min (each bath)			

32	Metal Deposition	Tool: CVC601 Target: #2 Aluminum	Power: 2000W Ar Flow: 20 sccms Argon Pressure: 5.0 mTorr Presputter: 300 seconds Dep. Time: 1000 sec	Record Base Pressure and Pump-down time.	All Device Wafers
33	Coat BBS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Dehydration Bake: 60 sec @ 150 °C Spin Coat Microprime P20: 15 sec @ 5000 RPM Bake: 60 sec @ 150 °C Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
34	BBS Litho Level III: Contact	Tool: Karl Seuss MA150 Recipe: adr Level: III Mask: Contact	Dose: 150 mJ/cm2 Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
35	Develop BBS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 150 C		All Device Wafers
36	Oxide Etch	Tool: Manual Wet Bench Bath: MOS Grade 5.2:1 HF:H2O	Thermal Oxide Etch Rate: ~ 1200 Å/min Annealed TEOS Etch Rate: ~ 2029 Å/min Time: 3:30 min		
37	Resist Strip	Tool: Wet Bench Solvent: PRS2000 Temp: 90°C Time: 10 min (each bath)			
38	Metal Deposition	Tool: CVC601 Target: #2 Aluminum	Power: 2000W Ar Flow: 20 sccms Argon Pressure: 5.0 mTorr Presputter: 300 seconds Dep. Time: 1000 sec	Record Base Pressure and Pump-down time.	All Device Wafers
39	Coat BBS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Dehydration Bake: 60 sec @ 150 °C Spin Coat Microprime P20: 15 sec @ 5000 RPM Bake: 60 sec @ 150 °C Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
40	Coat LAS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Spin Coat Microprime P20: 15 sec @ 5000 RPM Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
41	LAS Litho Level IV: Metal	Tool: Karl Seuss MA150 Recipe: adr Level: IV Mask: Metal	Dose: 150 mJ/cm2 Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
42	BBS Litho Level IV: Metal	Tool: Karl Seuss MA150 Recipe: adr Level: IV Mask: Metal	Dose: 150 mJ/cm2 Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
43	Develop BBS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
44	Develop LAS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
45	Aluminum Etch	Tool: LAM 4600 Recipe: ?????	Power: ?? W Pressure: ???mT Gas1: ?? sccm Time: 0:?? m:s		
46	Aluminum Etch	Tool: LAM 4600 Recipe: ?????	Power: ?? W Pressure: ???mT Gas1: ?? sccm Time: 0:?? m:s		
47	Resist Strip	Tool: Wet or Ash???			
48	BBS Oxide Dep	Tool: AMat P5000 Thickness: 4000 Å of TEOS Chamber: A Recipe: A6-4000A TEOS LS	Coat the Bump Bond Side of the wafer Use TEOS Si Carrier wafer		All Device Wafers
49	Coat BBS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Dehydration Bake: 60 sec @ 150 °C Spin Coat Microprime P20: 15 sec @ 5000 RPM Bake: 60 sec @ 150 °C Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers
50	Coat LAS	Tool: CEE 100 Resist Spinner Recipe: 0 Do Not use SVG Track (backside resist splattering)	Spin Coat Microprime P20: 15 sec @ 5000 RPM Spin Coat HPR 504: 3 sec @ 1000 RPM 60 sec @ 5000 RPM Soft Bake: 60 sec @ 105 °C		All Device Wafers

51	LAS Litho Level V: Passivation Cut	Tool: Karl Seuss MA150 Recipe: adr Level: V Mask: Passivation Cut	Dose: 150 mJ/cm ² Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
52	BBS Litho Level V: Passivation Cut	Tool: Karl Seuss MA150 Recipe: adr Level: V Mask: Passivation Cut	Dose: 150 mJ/cm ² Time: Irradiance / Dose Alignment Gap: 20 µm Hard Contact Delay: 60 sec	Measure lamp irradiance to determine exposure time Irradiance: _____	All Device Wafers
53	Develop BBS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
54	Develop LAS	Tool: CEE 100 Developer Recipe: 0 Do Not use SVG Track	Post Exposure Bake: None Hard Bake: 60 sec @ 130 C		All Device Wafers
55	Oxide Etch	Tool: Manual Wet Bench Bath: MOS Grade 5.2:1 HF:H ₂ O	Thermal Oxide Etch Rate: ~ 1200 Å/min Annealed TEOS Etch Rate: ~ 2029 Å/min Time: ??? min		
56	Resist Strip	Tool: Wet Bench Solvent: PRS2000 Temp: 90°C Time: 10 min (each bath)			
57	Sinter	Tool: Bruce Furnace Tube: 2 Recipe: 41 "425C H ₂ /N ₂ 30min"	Do Not use dummy wafers	Print Thermal History Include Profiles, N₂, & O₂	All Device Wafers
58	TEST	Electrical Test			All Device Wafers

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