

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor , I hereby declare that :

I believe I am the sole (if only one name appears below) , or joint (if more than one name appears) , original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled :

"Method of fabricating metal oxide semiconductor transistor"

 + The specification for the above entitled invention is filed herewith.

 The specification for the above entitled invention was filed previously

with application serial number: Filing Date:

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the invention disclosed in this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a). I further acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material to the patentability of the invention disclosed in this application, as defined in 1.56, which became available to me between the filing date of the prior application and the filing date of this application.

PRIORITY CLAIM

 + There is no claim of priority

 Claim of priority is based on the following:

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint the practitioners associated with the Customer Number: 27765 as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to the address associated with the above-mentioned Customer Number.

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

(請發明人務必簽署日期)

Date:	<u>JUN 28 2007</u>	<u>Chu Yin Tseng</u>
	Printed Name:	<u>Chu-Yin Tseng</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shih-Chieh Hsu</u>
	Printed Name:	<u>Shih-Chieh Hsu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Chih-Chiang Wu</u>
	Printed Name:	<u>Chih-Chiang Wu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shyh-Fann Ting</u>
	Printed Name:	<u>Shyh-Fann Ting</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Po-Lun Cheng</u>
	Printed Name:	<u>Po-Lun Cheng</u>
	Citizen of:	<u>R.O.C.</u>

Date: JUN 28 2007

Hsuan-Hsu Chen

Printed Name: Hsuan-Hsu Chen

Citizen of: R.O.C.

NPO#NAU-P0913-USA:0
CUST#UMCD-2007-0007

Combined Declaration and Power of Attorney, Page 3 of 3

F#NPO-P0001E-US
DSB0-096U010242

ABSTRACT

The present invention provides a method for fabricating a metal oxide semiconductor transistor. First, a semiconductor substrate is provided and at least a gate is formed on the semiconductor substrate. A protective layer is then formed on the semiconductor substrate and the gate. Subsequently, at least a recess is formed in the semiconductor substrate adjacent to the gate, and then an epitaxial layer is formed in the recess. A lightly doped region is formed in the semiconductor substrate adjacent to the gate. Finally, a spacer is formed on the sidewall of the gate.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Method of fabricating metal oxide semiconductor transistor		
First Named Inventor/Applicant Name:		Chu-Yin Tseng		
Filer:		Winston Hsu		
Attorney Docket Number:		NAUP0913USA		
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	300	300
Utility Search Fee	1111	1	500	500
Utility Examination Fee	1311	1	200	200
Pages:				
Claims:				
Claims in excess of 20	1202	18	50	900
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1900

Electronic Acknowledgement Receipt	
EFS ID:	2064011
Application Number:	11836772
International Application Number:	
Confirmation Number:	3794
Title of Invention:	Method of fabricating metal oxide semiconductor transistor
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0913USA
Receipt Date:	09-AUG-2007
Filing Date:	
Time Stamp:	23:00:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 1900
RAM confirmation Number	3470
Deposit Account	503105
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	NAUP0913USA0_A1_1_NP 003.PDF	190428 c0c02dd47aff26ee6206df54e36a2c90c 7a8f3b9	no	3
Warnings:					
Information:					
2	Application Data Sheet	NAUP0913USA0_A1_1_NP 075.PDF	1174701 3d4458bb82420ba646fcd0b167984f5 6629d1a5	no	6
Warnings:					
Information:					
3	Claims	321360.PDF	24519 45ef5c4c15b7046e04e1b636d4de4212 f6357bf2	no	6
Warnings:					
Information:					
4	Drawings	321362.PDF	545326 7557085973fe2011ae58bd7dcb4c59b7 4afa2b66	no	14
Warnings:					
Information:					
5	Specification	321359.PDF	42025 5f83ba38f837414571f8995d78c790665 df3e6b8	no	13
Warnings:					
Information:					
6	Power of Attorney	NAUP0913USA0_A1_1_NP 007.PDF	190428 c0c02dd47aff26ee6206df54e36a2c90c 7a8f3b9	no	3
Warnings:					
Information:					
7	Abstract	321361.PDF	15838 7994026a830557ee6572355c2c806fb83 8a2340cd	no	1
Warnings:					
Information:					
8	Fee Worksheet (PTO-06)	fee-info.pdf	8464 c1ae4b377b0907ee6e229e981c2092af 5dad00d3	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2191729		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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(請發明人務必簽署日期)

Date:	<u>JUN 28 2007</u>	<u>Chu Yin Tseng</u>
	Printed Name:	<u>Chu-Yin Tseng</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shih-Chieh Hsu</u>
	Printed Name:	<u>Shih-Chieh Hsu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Chih-Chiang Wu</u>
	Printed Name:	<u>Chih-Chiang Wu</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Shyh-Fann Ting</u>
	Printed Name:	<u>Shyh-Fann Ting</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>JUN 28 2007</u>	<u>Po-Lun Cheng</u>
	Printed Name:	<u>Po-Lun Cheng</u>
	Citizen of:	<u>R.O.C.</u>

Date: JUN 28 2007

Hsuan-Hsu Chen

Printed Name: Hsuan-Hsu Chen

Citizen of: R.O.C.

NPO#NAU-P0913-USA:0
CUST#UMCD-2007-0007

Combined Declaration and Power of Attorney, Page 3 of 3

F#NPO-P0001E-US
DSB0-096U010242

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0913USA
		Application Number	
Title of Invention	Method of fabricating metal oxide semiconductor transistor		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chu-Yin		Tseng		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tainan County		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b)ⁱ		TW			
Mailing Address of Applicant:					
Address 1		No.270, Jiabei Village, Shanhua Township			
Address 2					
City	Tainan County		State/Province		
Postal Code		Countryⁱ	TW		
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Shih-Chieh		Hsu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Hsinchu City		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b)ⁱ		TW			
Mailing Address of Applicant:					
Address 1		No.63, Jinshan 9th St			
Address 2					
City	Hsinchu City		State/Province		
Postal Code		Countryⁱ	TW		
Applicant 3					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chih-Chiang		Wu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Taichung County		Country Of Residenceⁱ	TW	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		NAUP0913USA	
		Application Number			
Title of Invention		Method of fabricating metal oxide semiconductor transistor			

Citizenship under 37 CFR 1.41(b) i		TW			
Mailing Address of Applicant:					
Address 1		No.67-4, Sec. 3, Minzu Rd., Tanzih Township			
Address 2					
City	Taichung County			State/Province	
Postal Code			Countryⁱ	TW	
Applicant 4					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name		Family Name	Suffix
	Shyh-Fann			Ting	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tai-Nan City		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b) i		TW			
Mailing Address of Applicant:					
Address 1		11F., No.2, Lane 6, Chongshan 12th St., East			
Address 2		District			
City	Tai-Nan City			State/Province	
Postal Code			Countryⁱ	TW	
Applicant 5					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name		Family Name	Suffix
	Po-Lun			Cheng	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Kao-Hsiung Hsien		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b) i		TW			
Mailing Address of Applicant:					
Address 1		No. 6, Jui-Chu Rd., Feng-Shan City			
Address 2					
City	Kao-Hsiung Hsien			State/Province	
Postal Code			Countryⁱ	TW	
Applicant 6					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name		Family Name	Suffix
	Hsuan-Hsu			Chen	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tai-Nan City		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b) i		TW			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0913USA
		Application Number	
Title of Invention	Method of fabricating metal oxide semiconductor transistor		

Mailing Address of Applicant:			
Address 1	No.2, Lane 276, Yujhong Rd.		
Address 2			
City	Tai-Nan City	State/Province	
Postal Code		Country	TW
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add 			

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	27765		
Email Address	winstonhsu@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	Method of fabricating metal oxide semiconductor transistor		
Attorney Docket Number	NAUP0913USA	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	14	Suggested Figure for Publication (if any)	
Publication Information:			
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)			
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not been and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.			

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ US Representative (37 CFR 11.9)
Customer Number	027765		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0913USA
		Application Number	
Title of Invention	Method of fabricating metal oxide semiconductor transistor		

Domestic Priority Information:

This section allows for the applicant to claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c). Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
Additional Domestic Priority Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1					Remove
If the Assignee is an Organization check here. ☐					
Prefix	Given Name	Middle Name	Family Name	Suffix	
Mailing Address Information:					
Address 1					
Address 2					
City		State/Province			
Country ⁱ		Postal Code			
Phone Number		Fax Number			
Email Address					
Additional Assignee Data may be generated within this form by selecting the Add button.					Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		NAUP0913USA	
		Application Number			
Title of Invention		Method of fabricating metal oxide semiconductor transistor			
Signature		/WINSTON HSU/		Date (YYYY-MM-DD)	2007-08-07
First Name	WINSTON	Last Name	HSU	Registration Number	41526

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

What is claimed is:

[Claim 1] 1. A method of fabricating a MOS transistor, comprising:

- providing a semiconductor substrate;
- forming at least a gate on the semiconductor substrate;
- forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate;
- forming at least a recess within the semiconductor substrate adjacent to the gate;
- forming an epitaxial layer in the recess;
- forming a lightly doped region within the semiconductor substrate adjacent to the gate; and
- forming a spacer on the sidewall of the gate.

[Claim 2] 2. The method of claim 1, wherein the gate further comprises:

- a dielectric layer;
- a conductive layer, positioned on the dielectric layer; and
- a cap layer, positioned on the conductive layer.

[Claim 3] 3. The method of claim 1, further comprising a step of removing the protective layer after forming the epitaxial layer in the recess.

[Claim 4] 4. The method of claim 1, wherein the protective layer comprises silicon nitride.

[Claim 5] 5. The method of claim 4, wherein the protective layer has a thickness of about 150 to 250 angstroms.

[Claim 6] 6. The method of claim 5, wherein the protective layer has a thickness of about 200 angstroms.

[Claim 7] 7. The method of claim 1, wherein the MOS transistor is a PMOS transistor.

[Claim 8] 8. The method of claim 7, wherein the epitaxial layer comprises SiGe.

[Claim 9] 9. The method of claim 1, wherein the MOS transistor is an NMOS transistor.

[Claim 10] 10. The method of claim 9, wherein the epitaxial layer comprises SiC.

[Claim 11] 11. The method of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.

[Claim 12] 12. The method of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.

[Claim 13] 13. The method of claim 1, further comprising a step of forming a source/drain region within the semiconductor substrate adjacent to the gate after forming the spacer.

[Claim 14] 14. A method of fabricating a CMOS transistor, comprising:

providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area;

forming a gate on the first conductive transistor area and on the second conductive transistor area respectively;

forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate;

forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area;

forming a first epitaxial layer in the recess;

forming a first ion lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area; and

forming a spacer on the sidewall of each gate.

[Claim 15] 15. The method of claim 14, wherein the gate further comprises:

a dielectric layer;

a conductive layer, positioned on the dielectric layer; and

a cap layer, positioned on the conductive layer.

[Claim 16] 16. The method of claim 14, wherein the first protective layer comprises silicon nitride.

[Claim 17] 17. The method of claim 16, wherein the first protective layer has a thickness of about 150 to 250 angstroms.

[Claim 18] 18. The method of claim 17, wherein the first protective layer has a thickness of about 200 angstroms.

[Claim 19] 19. The method of claim 14, wherein each spacer further comprises an oxide liner and a nitride spacer.

[Claim 20] 20. The method of claim 14, wherein each spacer further comprises an offset spacer, positioned between each gate and each spacer.

[Claim 21] 21. The method of claim 14, further comprising a step of removing the first protective layer after forming the first epitaxial layer in the first recess.

[Claim 22] 22. The method of claim 21, after removing the first protective layer, the method further comprises:

- forming a second protective layer on the semiconductor substrate, and the second protective layer covering the surface of each gate;

- forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;

- forming a second epitaxial layer in the second recess;

- removing the second protective layer; and

- forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.

[Claim 23] 23. The method of claim 22, wherein the second protective layer comprises silicon nitride.

[Claim 24] 24. The method of claim 23, wherein the second protective layer has a thickness of about 150 to 250 angstroms.

[Claim 25] 25. The method of claim 24, wherein the second protective layer has a thickness of about 200 angstroms.

[Claim 26] 26. The method of claim 14, after forming the first epitaxial layer, the method further comprises:

- forming at least a second recess within the semiconductor substrate adjacent to the gate in the second conductive transistor area;

- forming a second epitaxial layer in the second recess;

- removing the first protective layer; and

- forming a second ion lightly doped region within the semiconductor substrate adjacent to the gate in the second conductive transistor area before forming the spacer.

[Claim 27] 27. The method of claim 14, wherein the first conductive transistors comprise PMOS transistors and the second conductive transistors comprise NMOS transistors.

[Claim 28] 28. The method of claim 27, wherein the first epitaxial layer comprises SiGe and the second epitaxial layer comprises SiC.

[Claim 29] 29. The method of claim 14, wherein the first conductive transistors comprise NMOS transistors and the second conductive transistors comprise PMON transistors.

[Claim 30] 30. The method of claim 29, wherein the first epitaxial layer comprises SiC and the second epitaxial layer comprises SiGe.

[Claim 31] 31. A MOS transistor structure, comprising:

- a gate formed on a semiconductor substrate;

- two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate;

a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer; and

two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

[Claim 32] 32. The structure of claim 31, wherein the gate further comprises:

a dielectric layer;

a conductive layer, positioned on the dielectric layer; and

a cap layer, positioned on the conductive layer.

[Claim 33] 33. The structure of claim 31, wherein the MOS transistor comprises a PMOS transistor.

[Claim 34] 34. The structure of claim 33, wherein the epitaxial layer comprises SiGe.

[Claim 35] 35. The structure of claim 31, wherein the MOS transistor comprises an NMOS transistor.

[Claim 36] 36. The structure of claim 35, wherein the epitaxial layer comprises SiC.

[Claim 37] 37. The structure of claim 31, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.

[Claim 38] 38. The structure of claim 31, wherein the spacer further comprises an oxide liner and a nitride spacer.

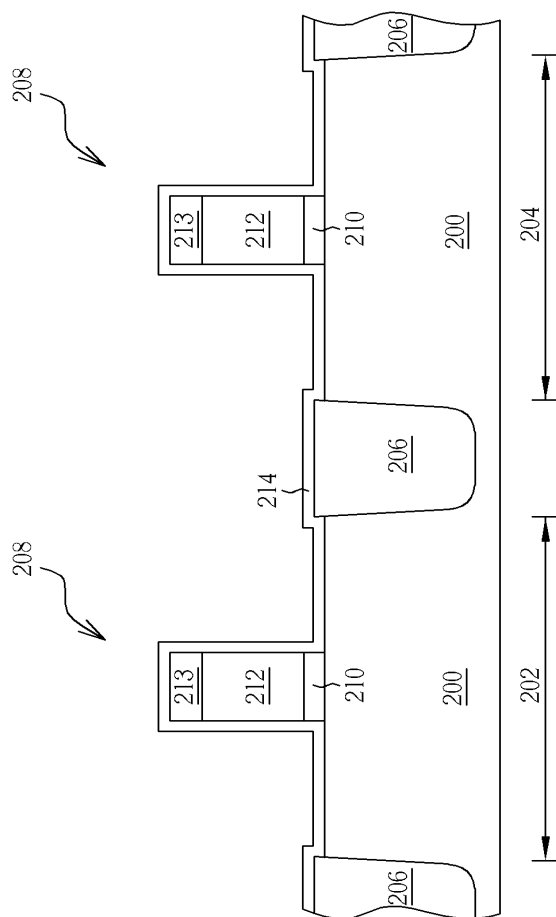


Fig. 1

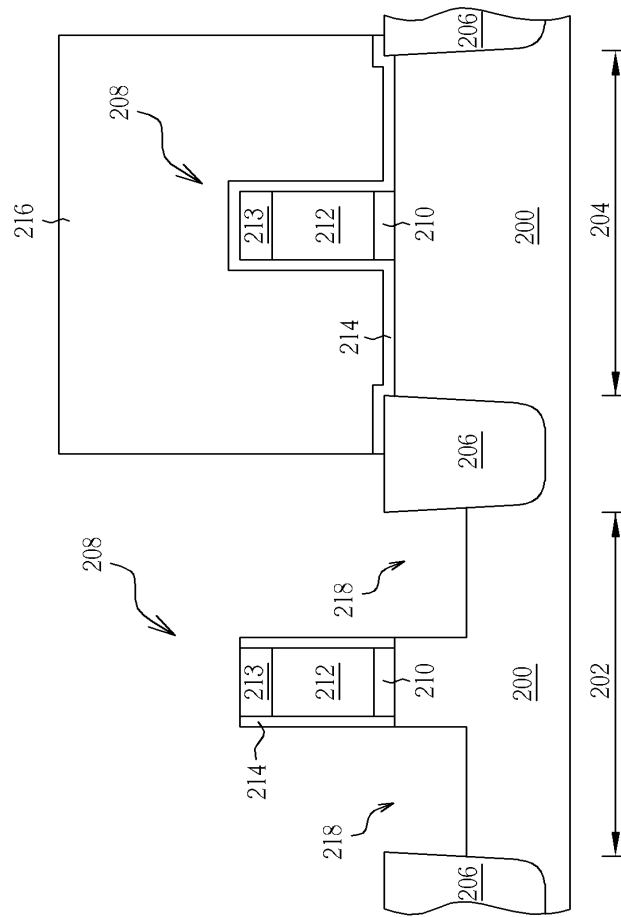


Fig. 2

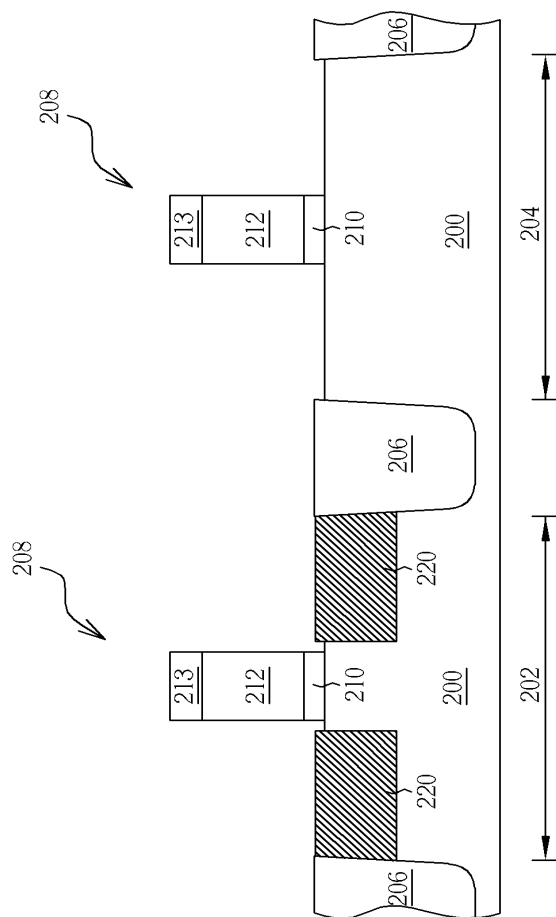


Fig. 3

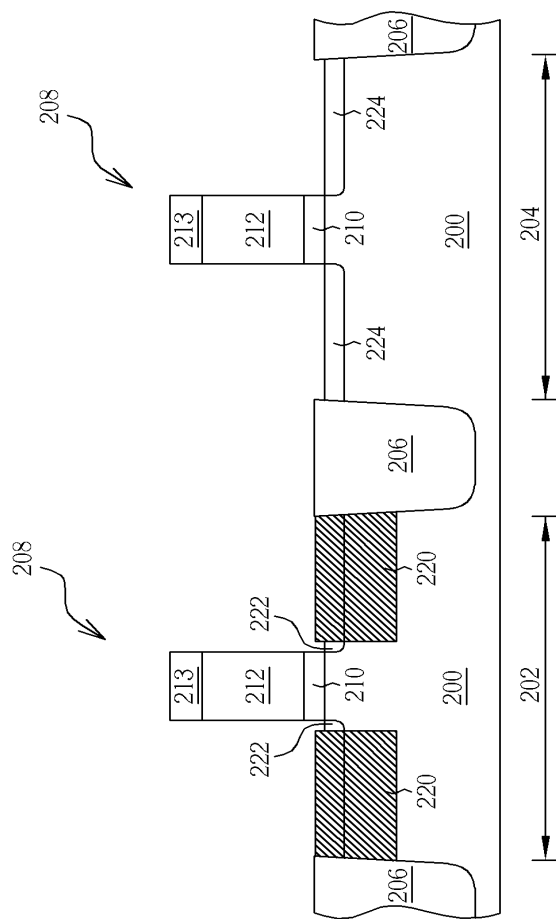


Fig. 4

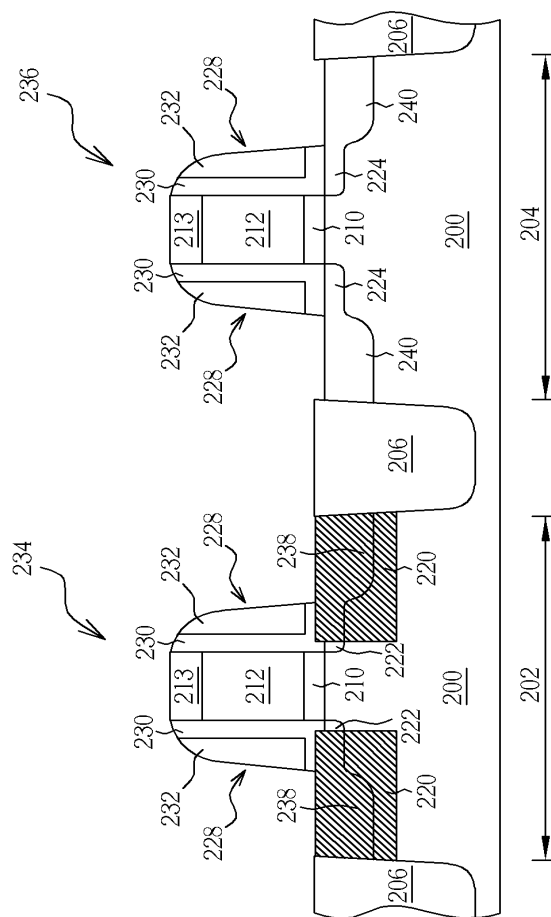


Fig. 5

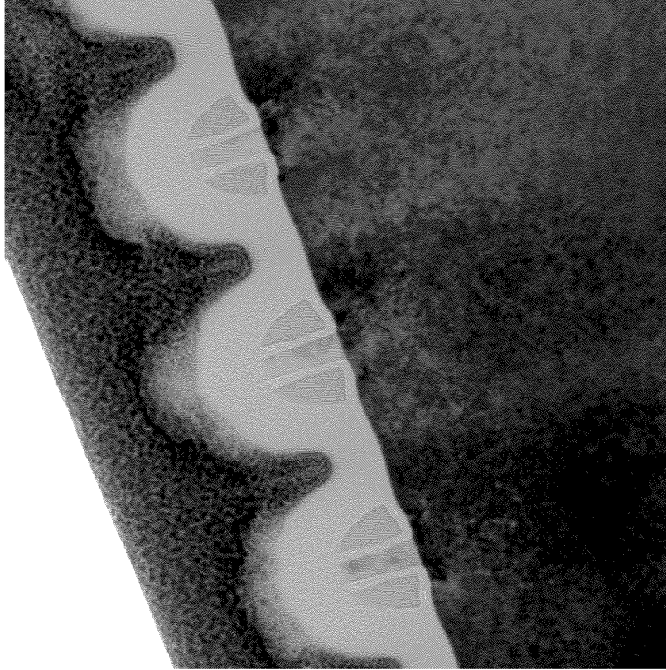


Fig. 6

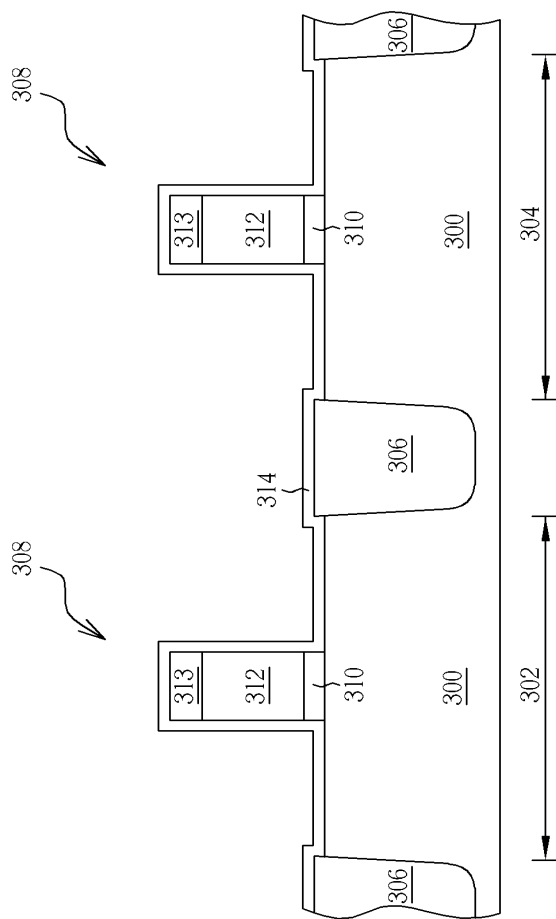


Fig. 7

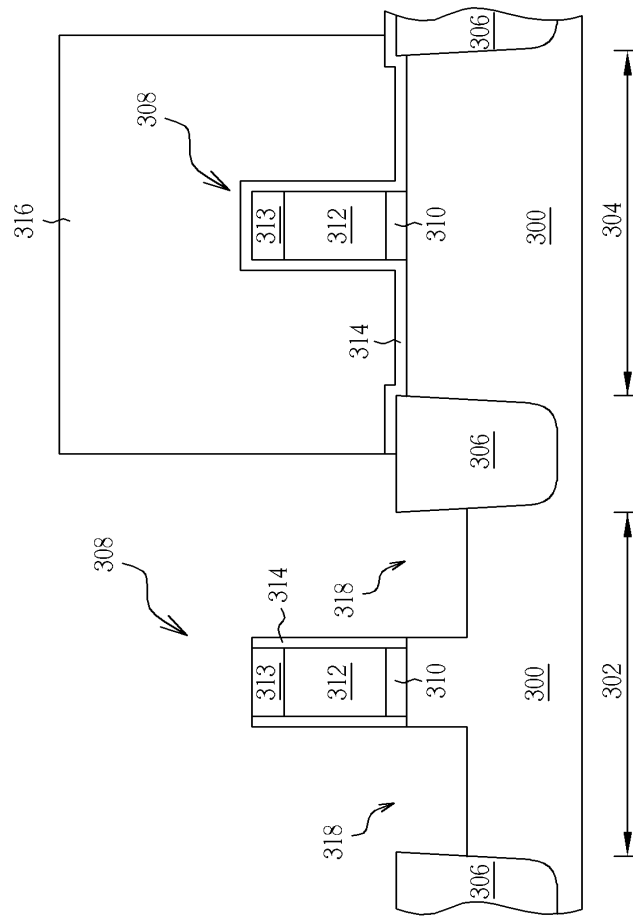


Fig. 8

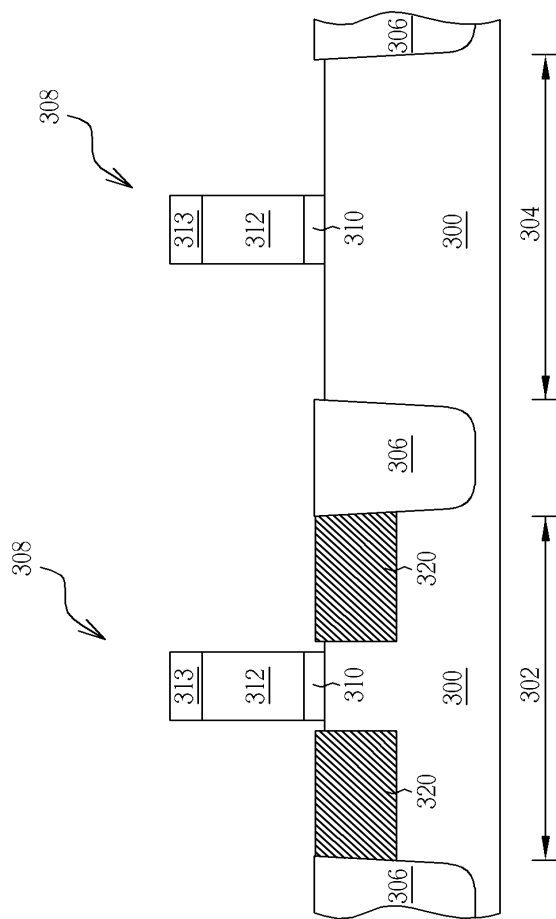


Fig. 9

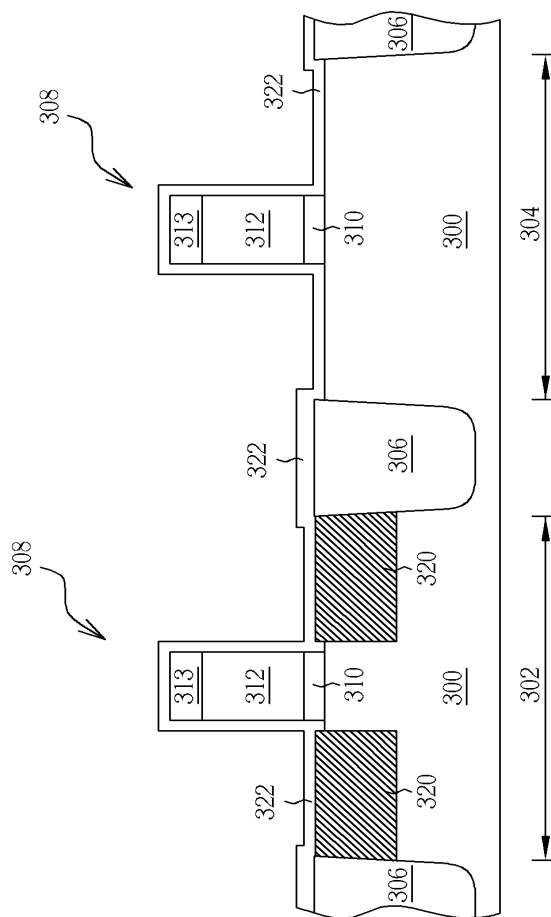


Fig. 10

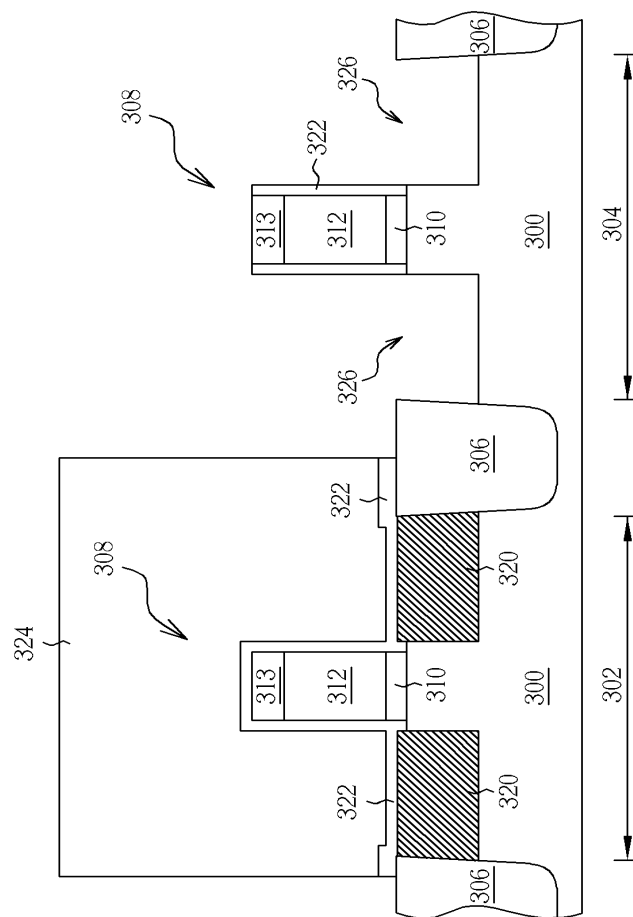


Fig. 11

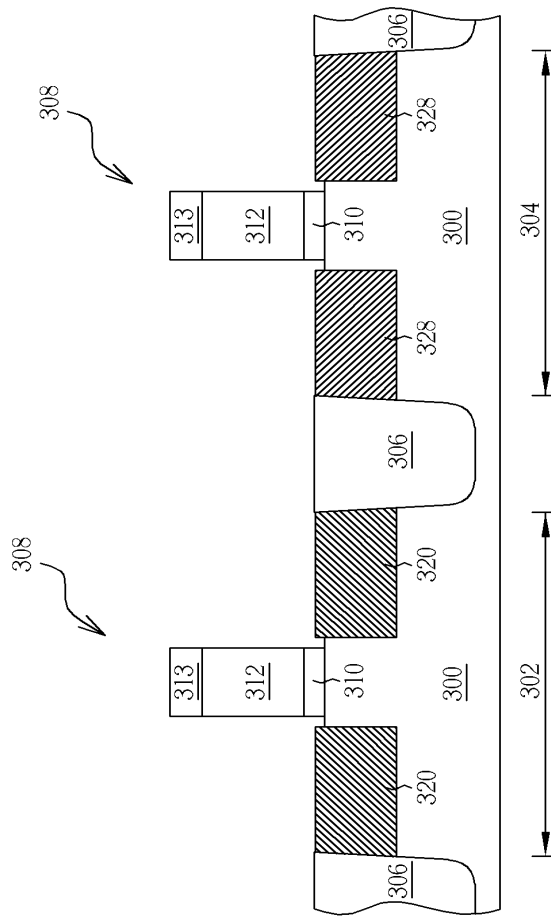


Fig. 12

Method of fabricating metal oxide semiconductor transistor

DESCRIPTION

Background of the Invention

[Para 1] 1. Field of the Invention

[Para 2] The present invention relates to a method for fabricating a metal oxide semiconductor (MOS) transistor, and more particularly, to a method for fabricating a strained silicon channel MOS transistor.

[Para 3] 2. Description of the Prior Art

[Para 4] A conventional MOS transistor generally includes a semiconductor substrate, such as silicon, a source region, a drain region, a channel positioned between the source region and the drain region, and a gate located above the channel. The gate composed of a gate dielectric layer, a gate conductive layer positioned on the gate dielectric layer, and spacers positioned on the sidewalls of the gate conductive layer. Generally, for a given electric field across the channel of a MOS transistor, the amount of current that flows through the channel is directly proportional to a mobility of the carriers in the channel. Therefore, how to improve the carrier mobility so as to increase the speed performance of MOS transistors has become a major topic for study in the semiconductor field.

[Para 5] One way to increase the mobility of the carriers in the channel of an MOS transistor is to produce a mechanical stress in the channel. A compressive strained channel, such as a silicon germanium (SiGe) channel layer grown on silicon, has significant hole mobility enhancement. A tensile strained channel, such as a thin silicon channel layer grown on silicon germanium, achieves significant electron mobility

enhancement. Another prior art method of obtaining a strained channel is to epitaxially grow a SiGe layer adjacent to the spacers within the semiconductor substrate after forming the spacer.

[Para 6] In this type of MOS transistor, a biaxial tensile strain occurs in the epitaxial silicon layer due to the silicon germanium, which has a larger lattice constant than silicon, and, as a result, the band structure alters, and the carrier mobility increases. This enhances the speed performance of the MOS transistor.

[Para 7] The performance of MOS transistors has increased year after year with the diminution of critical dimensions and the advance of very large scale integrated circuits (VLSI); therefore, the demand for the speed performance of the MOS transistor has also greatly increased. However, the compressive or tensile stress obtained according to the conventional method has been hardly achieved the required extent.

[Para 8] Accordingly, the applicants provide a method of fabricating strained silicon channel MOS transistors to improve the shortages from the prior art, and then increase the carrier mobility of MOS transistors.

Summary of the Invention

[Para 9] The present invention relates to a method of fabricating a MOS transistor, and more particularly, to a method of fabricating a strained silicon channel MOS transistor to improve the disadvantages of the prior art.

[Para 10] According to the claims, the present invention provides a method of fabricating a MOS transistor, the method comprising providing a semiconductor substrate; forming

at least a gate on the semiconductor substrate; forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate; forming at least a recess within the semiconductor substrate adjacent to the gate; forming an epitaxial layer in the recess; forming a lightly doped region within the semiconductor substrate adjacent to the gate; and forming a spacer on the sidewall of the gate.

[Para 11] According to the claims, the present invention provides another method for fabricating a CMOS transistor, the method comprising providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area; forming a gate on the first conductive transistor area and on the second conductive transistor area respectively; forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate; forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area; forming a first epitaxial layer in the recess; forming a first ion lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area; and forming a spacer on the sidewall of each gate.

[Para 12] According to the claims, the present invention further provides a MOS transistor structure, the structure comprising a gate formed on a semiconductor substrate; two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate; a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer; and two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

[Para 13] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[Para 14] Fig. 1 to Fig. 5 are cross-sectional diagrams, illustrating a fabricating method of MOS transistors in accordance with the first preferred embodiment of the present invention.

[Para 15] Fig. 6 shows a transmission electron microscopy picture of MOS transistors in accordance with the first preferred embodiment of the present invention.

[Para 16] Fig. 7 to Fig. 14 are cross-sectional diagrams, illustrating a fabricating method of MOS transistors in accordance with the second preferred embodiment of the present invention.

Detailed Description

[Para 17] Please refer to Fig. 1 to Fig. 5, which are cross-sectional diagrams illustrating a method for fabricating a MOS transistor in accordance with the first preferred embodiment of the present invention. For highlighting the characteristic of the present invention and for clarity of illustration, Fig. 1 to Fig. 5 merely show a first conductive transistor area and a second conductive transistor area. As shown in Fig. 1, a semiconductor substrate 200 is provided such as a silicon substrate or a silicon-on-insulator (SOI) substrate, but not limited thereto. The semiconductor substrate 200 comprises a plurality of first conductive transistor areas 202 and a plurality of second

conductive transistor areas 204, and the first conductive transistor areas 202 and the second conductive transistor areas 204 are isolated by isolation structures such as shallow trench isolations (STI) 206. Generally speaking, the STI 206 is formed by etching a trench in the semiconductor substrate 200 and then filling the trench with insulating materials such as silicon oxide. Besides, the semiconductor substrate 200 further comprises a plurality of gates 208, positioned respectively on each first conductive transistor area 202 and each second conductive transistor area 204. Each gate 208 comprises a dielectric layer 210, a conductive layer 212 positioned on the dielectric layer 210 and a cap layer 213 positioned on the conductive layer 212. In general, the dielectric layer 210 comprises isolating materials such as silicon oxide components or silicon nitride components, etc; the conductive layer 212 comprises conductive materials such as polysilicon or metal silicide; and the cap layer 213 comprises dielectric materials such as silicon nitride.

[Para 18] Subsequently, a protective layer 214 is formed on the semiconductor substrate 200, and the protective layer 214 covers the surface of each gate 208. According to the first preferred embodiment of the present invention, the protective layer 214 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 200 and the conductive layer 212: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The protective layer 214 has a thickness of about 150 to 250Å, and is preferably about 200Å.

[Para 19] As shown in Fig. 2, a patterned mask 216 is coated on the second conductive transistor area 204 and a portion of the STI 206. An etching process such as an anisotropic dry etching is then carried out to etch recesses 218 in the first conductive transistor area 202. Thereafter, the patterned mask 216 is removed.

[Para 20] As shown in Fig. 3, after a pre-cleaning step is performed to clean the semiconductor substrate 200 of the first conductive transistor area 202, such as using DHF solution or SPM solution to remove impurities upon the surface of the recesses 218, an epitaxial growth process is carried out to form epitaxial layers 220 in the recesses 218. Then, the protective layer 214 is removed. The epitaxial layer 220 is grown in the recess 218 and it may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the first preferred embodiment of the present invention, when the first conductive transistor area 202 is a PMOS transistor area, the epitaxial layer 220 is composed of SiGe. And when the first conductive transistor area 202 is an NMOS transistor, the epitaxial layer 220 is composed of SiC.

[Para 21] As shown in Fig. 4, a patterned mask (not shown) is coated on the second conductive transistor area 204. A first ion lightly doped process is carried out to form a first ion lightly doped region 222 in the first conductive transistor area 202. Then the patterned mask is removed. Thereafter, another patterned mask (not shown) is coated on the first conductive transistor area 202. A second ion lightly doped process is then carried out to form a second ion lightly doped region 224 in the second conductive transistor area 204. Then the patterned mask is removed.

[Para 22] As shown in Fig. 5, spacers 228 are formed on the sidewalls of each gate 280. According to the first preferred embodiment of the present invention, each spacer 228 comprises an oxide liner 230 and a nitride spacer 232. The spacers 228 cover the sidewalls of each gate 208 and also extend laterally onto the first ion lightly doped region 222 and the second ion lightly doped region 224. Each spacer 228 may also

comprise an offset spacer (not shown) positioned between the gate 208 and the oxide liner 230. Because each spacer 228 in the first conductive transistor area 202 lies over the raised epitaxial layer 220, thus each spacer 228 in the first conductive transistor area 202 is tilted upward. Please refer to Fig. 10, which is a transmission electron microscopy (TEM) picture of the MOS transistors in accordance with the first preferred embodiment of the present invention.

[Para 23] Finally, a patterned mask (not shown) is coated on the second conductive transistor area 204. A first ion source/drain implantation process is then carried out to form a first ion source/drain region 238 in the first conductive transistor area 202; thereby a first conductive transistor 234 such as a PMOS transistor is formed in the first conductive transistor area 202. Thereafter, the patterned mask is removed. Subsequently, another patterned mask (not shown) is coated on the first conductive transistor area 202. A second ion source/drain implantation process is carried out to form a second ion source/drain region 240 in the second conductive transistor area 204; thereby a second conductive transistor 236 such as an NMOS transistor is formed in the second conductive transistor area 204. Thereafter, the patterned mask is removed.

[Para 24] It should be noticed that the process of forming the source/drain regions 238 as shown in Fig. 5 is an optional step depending on the method used in the epitaxial growth process. Because the epitaxial growth process as shown in Fig. 3 may be an in-situ doped epitaxial growth process, therefore, while the epitaxial layer 200 is formed, the demanded doped ions can also be implanted into the semiconductor substrate 200 or the grown epitaxial layer 200, as a result, the corresponding source/drain regions are formed. Thus, the source/drain implantation process as shown in Fig. 5 can be skipped. According to the first preferred embodiment of the present invention, when the first conductive transistor area 202 is a PMOS transistor area, the epitaxial growth process,

which is carried out to form the epitaxial layer 220 composed of silicon germanium, may be an in-situ doped boron epitaxial growth process. Accordingly, the corresponding source/drain regions are formed by implanting the demanded boron ions within the semiconductor substrate 200 while the epitaxial layer 220 is formed.

[Para 25] Please refer to Fig. 7 to Fig. 14, which are cross-sectional diagrams illustrating a method for fabricating a MOS transistor in accordance with the second preferred embodiment of the present invention. For highlighting the characteristic of the present invention and for clarity of illustration, Fig. 7 to Fig. 14 merely show a first conductive transistor area and a second conductive transistor area. As shown in Fig. 7, a semiconductor substrate 300 is provided such as a silicon substrate or a silicon-on-insulator (SOI) substrate, but not limited thereto. The semiconductor substrate 300 comprises a plurality of first conductive transistor areas 302 and a plurality of second conductive transistor areas 304, and the first conductive transistor areas 302 and the second conductive transistor areas 304 are isolated by isolation structures such as shallow trench isolations (STI) 306. Generally speaking, STI 306 is formed by etching a trench in the semiconductor substrate 300 and then filling the trench with insulating materials such as silicon oxide. Besides, the semiconductor substrate 300 further comprises a plurality of gates 308, positioned respectively on each first conductive transistor area 302 and each second conductive transistor area 304. Each gate 308 comprises a dielectric layer 310, a conductive layer 312 positioned on the dielectric layer 310 and a cap layer 313 positioned on the conductive layer 312. In general, the dielectric layer 310 comprises isolating materials such as silicon oxide components or silicon nitride components, etc; the conductive layer 312 comprises conductive materials such as polysilicon or metal silicide; and the cap layer 313 comprises dielectric materials such as silicon nitride.

[Para 26] Subsequently, a first protective layer 314 is formed on the semiconductor substrate 300, and the first protective layer 314 covers the surface of each gate 308. According to the second preferred embodiment of the present invention, the first protective layer 314 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 300 and the conductive layer 312: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The first protective layer 314 has a thickness of about 150 to 250Å, and is preferably about 200Å.

[Para 27] As shown in Fig. 8, a first patterned mask 316 is coated on the second conductive transistor area 304 and a portion of the STI 306. An etching process such as an anisotropic dry etching is carried out to form first recesses 318 in the first conductive transistor area 302. Thereafter, the first patterned mask 316 is removed.

[Para 28] As shown in Fig. 9, after a pre-cleaning step is performed to clean the semiconductor substrate 300 of the first conductive transistor area 302, such as using DHF solution or SPM solution to remove impurities upon the surface of the first recesses 318, an epitaxial growth process is carried out to form first epitaxial layers 320 in the first recesses 318. Then, the first protective layer 314 is removed. The first epitaxial layer 320 is grown in the first recess 318 and it may be grown higher than the surface of the semiconductor substrate 300, so as to form a raised epitaxial layer. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the second preferred embodiment of the present invention, when the first conductive transistor area 302 is a PMOS transistor area, the first epitaxial layer 320 is composed of SiGe.

[Para 29] As shown in Fig. 10, a second protective layer 322 is formed on the semiconductor substrate 300 and the second protective layer 322 covers the surface of each gate 308. According to the second preferred embodiment of the present invention, the second protective layer 322 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 300 and the conductive layer 312: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The second protective layer 322 has a thickness of about 150 to 250Å, and is preferably about 200Å.

[Para 30] As shown in Fig. 11, a second patterned mask 324 is coated on the first conductive transistor area 302 and a portion of the STI 306. An etching process such as an anisotropic dry etching is carried out to form second recesses 326 in the second conductive transistor area 304. Thereafter, the second patterned mask 324 is removed.

[Para 31] It should be noticed that the steps of forming the second recess 326 shown in Fig. 10 to Fig. 11 might be performed without using the second protective layer 322. Namely, after forming the first epitaxial layer 320 as shown in Fig. 9, the first protective layer 314 is not removed and then the second patterned mask 324 is coated directly on the first conductive transistor area 302 and a portion of the STI 306. Subsequently, an etching process such as that shown in Fig. 11 is carried out to form the second recesses 326 in the second conductive transistor area 304. Thereafter, the second patterned mask 324 and the first protective layer 314 are removed. Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention.

[Para 32] As shown in Fig. 12, after a pre-cleaning step is performed to clean the semiconductor substrate 300 of the second conductive transistor area 304, such as using

DHF solution or SPM solution to remove impurities upon the surface of the second recesses 326, an epitaxial growth process is carried out to form second epitaxial layers 328 in the second recesses 326. Then, the second protective layer 322 is removed. The second epitaxial layer 328 is grown in the second recess 326 and it may be grown higher than the surface of the semiconductor substrate 300, so as to form a raised epitaxial layer. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the second preferred embodiment of the present invention, when the second conductive transistor area 304 is an NMOS transistor area, the second epitaxial layer 328 is composed of SiC. It should be noticed that the process of forming the first epitaxial layer 320 as shown in Fig.7 to Fig. 9 might be performed after the process of forming the second epitaxial layer 328 as shown in Fig. 10 to Fig. 12. Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention.

[Para 33] As shown in Fig. 13, a patterned mask (not shown) is coated on the second conductive transistor area 304. A first ion lightly doped process is carried out to form a first ion lightly doped region 330 in the first conductive transistor area 302. Then the patterned mask is removed. Thereafter, another patterned mask (not shown) is coated on the first conductive transistor area 302. A second ion lightly doped process is then carried out to form a second ion lightly doped region 332 in the second conductive transistor area 304. Then the patterned mask is removed.

[Para 34] As shown in Fig. 14, spacers 334 are formed on the sidewalls of each gate 308. According to the second preferred embodiment of the present invention, each spacer 334 comprises an oxide liner 336 and a nitride spacer 338. The spacers 334 cover the sidewalls of each gate 308 and extend laterally onto the first ion lightly doped region 330 and the second ion lightly doped region 332. The spacers 334 also cover a portion

of the first epitaxial layer 320 and a portion of the second epitaxial layer 328. Additionally, each spacer 334 may further comprise an offset spacer (not shown) positioned between the gate 308 and the oxide liner 336.

[Para 35] Finally, a patterned mask (not shown) is coated on the second conductive transistor area 304. A first ion source/drain implantation process is then carried out to form a first ion source/drain region 344 in the first conductive transistor area 302; thereby a first conductive transistor 340 such as a PMOS transistor is formed in the first conductive transistor area 302. Thereafter, the patterned mask is removed. Subsequently, another patterned mask (not shown) is coated on the first conductive transistor area 302. A second ion source/drain implantation process is carried out to form a second ion source/drain region 346 in the second conductive transistor area 304; thereby a second conductive transistor 342 such as an NMOS transistor is formed in the second conductive transistor area 304. Thereafter, the patterned mask is removed.

[Para 36] It should be noticed that the processes of forming the first source/drain regions 334 and the second source/drain regions 346 as shown in Fig. 14 is an optional step depending on the method used in the epitaxial growth process. Because the epitaxial growth process as shown in Fig. 9 may be an in-situ doped epitaxial growth process, therefore, while the first epitaxial layer 320 or the second epitaxial layer 328 is formed, the demanded doped ions can also be implanted into the semiconductor substrate 300 or the grown epitaxial layers 320, 328, as a result, the corresponding source/drain regions are formed. Accordingly, source/drain implantation as shown in Fig. 14 can be skipped.

[Para 37] Since the characteristic of the present invention is to form the epitaxial layer before forming the spacer, thus the distance between the gate and the epitaxial layer is

no longer limited by the width of the spacer. Besides, the process of etching the recess is carried out before forming the spacer. At this moment, the pattern density on the semiconductor substrate is lower than the time when the spacer is formed, thus the micro-loading effect caused by the pattern density can be reduced, and then the uniformity in etching the recess is increased. Additionally, the lightly doped regions and the source/drain regions are doped after forming the epitaxial layer, thus the doped ions will not be affected by the high temperature epitaxial growth process, which leads the doped ions to diffuse. Finally, since the present invention provides a protective layer to cover the semiconductor substrate and the shallow trench isolation (STI), the problem of the STI thickness loss will be reduced.

[Para 38] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention.

8/9/2007

PTO/SB/06 (12-04)

Approved for use through 7/31/2006. OMB 0651-0032

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PATENT APPLICATION FEE DETERMINATION RECORD					Application or Docket Number	
Substitute for Form PTO-875					11/836,772	
APPLICATION AS FILED – PART I						
(Column 2)			SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A			N/A	500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A	200
TOTAL CLAIMS (37 CFR 1.16(i))	38	minus 20 = 18	X	25=	X	50= 900
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *	X	100=	X	200=
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					N/A	
					TOTAL	1900
* If the difference in column 1 is less than zero, enter "0" in column 2.						
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			
	Total (37 CFR 1.16(i))	Minus	**	=		
	Independent (37 CFR 1.16(h))	Minus	***	=		
	Application Size Fee (37 CFR 1.16(s))					
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
				TOTAL ADD'T FEE		
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			
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	Independent (37 CFR 1.16(h))	Minus	***	=		
	Application Size Fee (37 CFR 1.16(s))					
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
				TOTAL ADD'T FEE		
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11/836,772	08/09/2007	2811	1900	NAUP0913USA	38	3

CONFIRMATION NO. 3794

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FILING RECEIPT

Date Mailed: 08/20/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Chu-Yin Tseng, Tainan County, TAIWAN;
Shih-Chieh Hsu, Hsinchu City, TAIWAN;
Chih-Chiang Wu, Taichung County, TAIWAN;
Shyh-Fann Ting, Tai-Nan City, TAIWAN;
Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN;
Hsuan-Hsu Chen, Tai-Nan City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 08/20/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/836,772**

Projected Publication Date: 02/12/2009

Non-Publication Request: No

Early Publication Request: No

Title

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/836,772	08/09/2007	Chu-Yin Tseng	NAUP0913USA

CONFIRMATION NO. 3794

PUBLICATION NOTICE

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116



OC000000034530073

Title:Method of fabricating metal oxide semiconductor transistor

Publication No.US-2009-0039389-A1

Publication Date:02/12/2009

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/836,772	08/09/2007	Chu-Yin Tseng	NAUP0913USA	3794
27765 7590 08/11/2009 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER DANG, PHUC T	
			ART UNIT 2892	PAPER NUMBER
			NOTIFICATION DATE 08/11/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No. 11/836,772	Applicant(s) TSENG ET AL.	
	Examiner Phuc T. Dang	Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 09 August 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☐ Claim(s) _____ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☒ Claim(s) 1-38 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

Election/Restriction

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Group I, Claims 1-30, drawn to a method of fabricating a MOS transistor, classified in class 438, subclass 204.
- II. Group II, Claims 31-38, drawn to a MOS transistor, classified in class 257, subclass 190.

The inventions are distinct, each from the other because of the following reasons:

- 1. Inventions I and II are related as method of making and product made.

The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the Group II invention would not necessarily imply unpatentability of the Group I invention, since the device of Group II invention could be made by a product different from those of the Group I invention. For example, a semiconductor device of Group II can be made is different ways and does not have exactly follow the process of the claims of Group I.

However, the issues of method and product claims are divergent.

Furthermore, there may be some overlap in the searches of the two groups, but there is no reason to believe that the searches would be identical. Therefore, based on the additional work involved in searching and examination of the two inventions together, restriction of distinct inventions is clearly proper.

- 2. Applicant is advised that the response to this requirement to be complete must include an election of the invention to be examined eventhough the requirement be traverse (37 CFR 1.143).
- 3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).
- 4. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Phuc T. Dang whose telephone number (571) 272-1776. The examiner can normally be reached on Monday through Friday from 8:00am to 5:00pm.

Application/Control Number: 11/836,772
Art Unit: 2892

Page 3

/Phuc T Dang/
Primary Examiner, Art Unit 2892

<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant										☐ CPA										☐ T.D.										☐ R.1.47									
CLAIM			DATE																																				
Final	Original	08/03/2009																																					
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	2	÷																																					
	3	÷																																					
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<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	08/03/2009								
	37	÷								
	38	÷								

Method of fabricating metal oxide semiconductor transistor

Appl. No. : 11/836,772 Confirmation No. 3794
Applicant : Chu-Yin Tseng et al.
Filed : August 9, 2007
TC/A.U. : 2892
Examiner : DANG, PHUC T
Docket No. : NAUP0913USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

- 5 In response to the Office action of August 11, 2009, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

10

REMARKS/ARGUMENTS

5 In response to the Election/Restriction requirement in the above-identified Office
action, species II (claims 31-38) is elected as the subject matter to be examined in the
present application. Claims 1-30 are canceled accordingly. Consideration of the
elected claims 31-38 is politely requested. The inventorship is not changed.

10 Applicant respectfully requests that a timely Notice of Allowance be issued in this
case.

Sincerely yours,

15 _____/Winston Hsu/_____ Date: _____08/24/2009_____
Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

20 Note: Please leave a message in my voice mail if you need to talk to me. (The time in
D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Electronic Acknowledgement Receipt	
EFS ID:	5929046
Application Number:	11836772
International Application Number:	
Confirmation Number:	3794
Title of Invention:	Method of fabricating metal oxide semiconductor transistor
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0913USA
Receipt Date:	24-AUG-2009
Filing Date:	09-AUG-2007
Time Stamp:	02:30:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Claims	684447.PDF	53626 7988015f1e80c6b7e4e3008c77cd269d335d d737	no	2

Warnings:

Information:

2	Response to Election / Restriction Filed	684448.PDF	59256 38b867318797d5fc5968114668f599ae407951f2	no	1
Warnings:					
Information:					
3	Applicant Arguments/Remarks Made in an Amendment	684450.PDF	56902 3d6692e818a56ad4e88d136c53395c6dfa58484f	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			169784		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

5

Listing of Claims:

Claims 1-30 (canceled)

- 10 Claim 31 (original): A MOS transistor structure, comprising:
a gate formed on a semiconductor substrate;
two raised epitaxial layers positioned respectively in the semiconductor substrate
next to the relative sides of the gate;
a spacer formed on the sidewall of the gate and extending laterally upon a portion
15 of the raised epitaxial layer; and
two doped region formed respectively in the semiconductor substrate next to the
relative sides of the gate.

- Claim 32 (original): The structure of claim 31, wherein the gate further comprises:
20 a dielectric layer;
a conductive layer, positioned on the dielectric layer; and
a cap layer, positioned on the conductive layer.

- Claim 33 (original): The structure of claim 31, wherein the MOS transistor comprises
25 a PMOS transistor.

Claim 34 (original): The structure of claim 33, wherein the epitaxial layer comprises
SiGe.

- 30 Claim 35 (original): The structure of claim 31, wherein the MOS transistor comprises

an NMOS transistor.

Claim 36 (original): The structure of claim 35, wherein the epitaxial layer comprises SiC.

5

Claim 37 (original): The structure of claim 31, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.

Claim 38 (original): The structure of claim 31, wherein the spacer further comprises
10 an oxide liner and a nitride spacer.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/836,772		Filing Date 08/09/2007		☐ To be Mailed	
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APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A		N/A		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR	X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL				

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	08/24/2009	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 8	Minus	** 38	= 0	X \$ =		OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$ =		OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	

(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Legal Instrument Examiner:
/RAMONA D. WILSON/



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/836,772	08/09/2007	Chu-Yin Tseng	NAUP0913USA	3794
27765 7590 09/09/2009 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER DANG, PHUC T	
			ART UNIT 2892	PAPER NUMBER
			NOTIFICATION DATE 09/09/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No. 11/836,772	Applicant(s) TSENG ET AL.	
	Examiner Phuc T. Dang	Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on election filed on 08/24/2009.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 31-38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 31-38 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 09 August 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.	4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) ☐ Notice of Informal Patent Application 6) ☐ Other: _____.
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DETAILED ACTION

Election/Restrictions

1. Applicant's election of Species II (claims 31-38) filed on 08/24/2009 and canceled Species I (claims 1-30) has been acknowledged and considered.

Because Applicants did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP 818.03(a)).

Claims 31-38 are currently pending in the application.

Oath/Declaration

2. The oath/declaration filed on 08/09/2007 is acceptable.

Specification

This application is objected to be cause of the following:

3. A title such as -- METAL OXIDE SEMICONDUCTOR TRANSISTOR -- is suggested.

Note that, the claims are directed to semiconductor device instead of to a method of making a semiconductor device.

A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP 606.01).

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to

Art Unit: 2892

the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 31-32 and 34 are rejected under 35 U.S.C. 102 (e) as being anticipated by Luo et al., hereafter “Luo” (U.S. Publication No. 2008/0006818 A1).

Regarding claim 31, Luo discloses a MOS transistor structure, comprising:

a gate 22 formed on a semiconductor substrate 12;

two raised epitaxial layers 28 & 30 positioned respectively in the semiconductor substrate 12 next to the relative sides of the gate 22;

a spacer 36 formed on the sidewall of the gate 22 and extending laterally upon a portion of the raised epitaxial layer 28 & 30; and

two doped region 34 formed respectively in the semiconductor substrate 12 next to the relative sides of the gate 22 (Fig. 5).

Regarding claim 32, Luo discloses wherein the gate further comprises a dielectric layer 20; a conductive layer 22, positioned on the dielectric layer 20; and a cap layer 24, positioned on the conductive layer 22 (Fig. 5).

Regarding claim 34, Luo discloses wherein the epitaxial layer comprises SiGe (para [0049]-[[0052]]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject

Art Unit: 2892

matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 33 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luo et al., hereafter “Luo” (U.S. Publication No. 2008/0006818 A1).

Regarding claims 34-35, Luo discloses the features of the claimed invention as discussed above, but does not disclose the MOS transistor comprises PMOS and NMOS.

It would have been an obvious matter of the design choice to modify the MOS transistor comprises PMOS and NMOS in order to improve the performance of the MOS transistor, since it has been held to be within the general skill of the worker in the art to select any type of the transistor on the basis of its suitability for the intended use as a matter of obvious design choice.

In re Leshin, 125 USPQ 416.

Regarding claim 36, Luo discloses wherein the epitaxial layer comprises SiGe (para [0049]-[0052]).

6. Claims 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Luo in view Chien et al., hereafter “Chien” (U.S. Patent No. 6,815,770 B1).

Regarding claims 37-38, Luo discloses the features of the claimed invention as discussed above, but does not disclose wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer.

However, Chien, in the same field of endeavor, discloses the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer (Fig. 1).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Luo to provide the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer as taught by Chien for a purpose of controlling the step of doping.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cheng et al. (U.S. Publication No. 2008/0032468 A1) and YAMAUCHI et al. (U.S. Publication No. 2007/0298558 A1).
8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 571-272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.
9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and Final communications.
10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

/Phuc T Dang/

Primary Examiner, Art Unit 2892

Application/Control Number: 11/836,772
Art Unit: 2892

Page 6

Notice of References Cited	Application/Control No. 11/836,772		Applicant(s)/Patent Under Reexamination TSENG ET AL.	
	Examiner Phuc T. Dang		Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0006818 A1	01-2008	Luo et al.	257/19
*	B	US-6,815,770 B1	11-2004	Chien et al.	257/344
*	C	US-2007/0298558 A1	12-2007	YAMAUCHI et al.	438/197
*	D	US-2008/0032468 A1	02-2008	Cheng et al.	438/197
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 3794

SERIAL NUMBER 11/836,772	FILING or 371(c) DATE 08/09/2007 RULE	CLASS 257	GROUP ART UNIT 2892	ATTORNEY DOCKET NO. NAUP0913USA		
APPLICANTS Chu-Yin Tseng, Tainan County, TAIWAN; Shih-Chieh Hsu, Hsinchu City, TAIWAN; Chih-Chiang Wu, Taichung County, TAIWAN; Shyh-Fann Ting, Tai-Nan City, TAIWAN; Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN; Hsuan-Hsu Chen, Tai-Nan City, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/20/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged /PHUC T DANG/ Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 14	TOTAL CLAIMS 38	INDEPENDENT CLAIMS 3
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE Method of fabricating metal oxide semiconductor transistor						
FILING FEE RECEIVED 1900	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
257	19,190,192,197	09/03/2009	PD

SEARCH NOTES		
Search Notes	Date	Examiner
INVENTOR SEARCH	09/03/2009	PD
EAST SEARCH	09/03/2009	PD

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	08/03/2009	09/03/2009						
	1	÷	-						
	2	÷	-						
	3	÷	-						
	4	÷	-						
	5	÷	-						
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	28	÷	-						
	29	÷	-						
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	31	÷	✓						
	32	÷	✓						
	33	÷	✓						
	34	÷	✓						
	35	÷	✓						
	36	÷	✓						

<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47									
CLAIM		DATE							
Final	Original	08/03/2009	09/03/2009						
	37	÷	✓						
	38	÷	✓						

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"11836772"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 18:49
L2	1	((gate) and (substrate) and (raised near epitaxial) and (spacer sidewall side-wall) and (dop\$3 near region\$1)). clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 18:57
L3	33	((gate) and (substrate) and (raised near epitaxial) and (spacer sidewall side-wall) and (dop\$3 near region\$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 18:57
L4	0	((gate) and (substrate) and (raised near epi) and (spacer sidewall side-wall) and (dop\$3 near region\$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:07
L5	7104	((gate) and (substrate) and (epi epitaxial) and (spacer sidewall side-wall) and (dop \$3 near region\$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:08
L6	119	5 and ((epi epitaxial) with (recess\$3) with (substrate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:08
L7	108	6 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:09

L8	44	7 and PMOS	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:17
L9	19	8 and (epi epitaxial) with (sige)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:18
L10	19	8 and ((epi epitaxial) with (sige))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:18
L11	26	7 and ((epi epitaxial) with (sige))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:21
L12	1	tseng near chu-yin.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:25
L13	22	hsu near shih-chieh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:25
L14	11	wu near chih-chiang.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:25
L16	44	ting near shyh-fann.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:26

L18	23	cheng near po-lun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:27
L19	5	chen near hsuan-hsu.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/08/31 19:27

8/ 31/ 2009 7:27:35 PM**C:\ Documents and Settings\ PDang1\ My Documents\ EAST\ Workspaces\ today062609.wsp**

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"20080006818"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:45
L2	26228	((cmos) (mos)) with ((pmos) (p-mos))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:49
L3	14298	((cmos) (mos)) with ((pmos) near5 (nmos))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:49
L4	4701	((mos) with (pmos) near5 (nmos))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:50
L6	367	4 and epitaxial near layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:50
L7	2	1 and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:51
L8	365	6 and (substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:52

L9	29	8 and cap near layer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 17:52
L10	2	1 and sige	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:12
L11	184	(offset near spacer) with (between) with (gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:14
L12	21	11 and cmos near transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:14
L13	131	(offset near spacer) with (between) with (gate near5 spacer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:17
L14	15	13 and cmos near transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:17
L15	210	(spacer) with (oxide near2 lin \$3) with (nitride near spacer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:22
L16	199	15 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:23

L17	25	16 and offset near spacer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:23
L18	13	17 and mos	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:25
L19	11	17 and mos near transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/09/01 18:25

9/ 1/ 2009 6:36:15 PM**C:\ Documents and Settings\ PDang1\ My Documents\ EAST\ Workspaces\ today062609.wsp**

Method of fabricating metal oxide semiconductor transistor

Appl. No. : 11/836,772 Confirmation No. 3794
Applicant : Chu-Yin Tseng et al.
Filed : August 9, 2007
TC/A.U. : 2892
Examiner : DANG, PHUC T
Docket No. : NAUP0913USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

- 5 In response to the Office action of September 09, 2009, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

- 10 **Remarks/Arguments** begin on page 5 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

5

Listing of Claims:

Claims 1-30 (canceled)

- 10 Claim 31 (currently amended): A MOS transistor structure, comprising:
a gate formed on a semiconductor substrate;
two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;
- 15 a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer; and
two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.
- 20 Claim 32 (original): The structure of claim 31, wherein the gate further comprises:
a dielectric layer;
a conductive layer, positioned on the dielectric layer; and
a cap layer, positioned on the conductive layer.
- 25 Claim 33 (original): The structure of claim 31, wherein the MOS transistor comprises a PMOS transistor.

Claim 34 (original): The structure of claim 33, wherein the epitaxial layer comprises SiGe.

30

Claim 35 (original): The structure of claim 31, wherein the MOS transistor comprises an NMOS transistor.

5 Claim 36 (original): The structure of claim 35, wherein the epitaxial layer comprises SiC.

Claim 37 (original): The structure of claim 31, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.

10 Claim 38 (original): The structure of claim 31, wherein the spacer further comprises an oxide liner and a nitride spacer.

Claim 39 (new): The structure of claim 31, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.
15

Claim 40 (new): The structure of claim 31, wherein the spacer further comprises a L-shaped spacer.

Claim 41 (new): The structure of claim 31, further comprising a lightly doped drain
20 disposed in the semiconductor substrate and outside the raised epitaxial layers.

Appl. No. 11/836,772
Amdt. dated October 26, 2009
Reply to Office action of September 09, 2009

Amendments to the Specification:

Please replace the title of the invention with the following:

- 5 ~~Method of fabricating metal oxide semiconductor transistor~~

Metal oxide semiconductor transistor

Electronic Acknowledgement Receipt	
EFS ID:	6316495
Application Number:	11836772
International Application Number:	
Confirmation Number:	3794
Title of Invention:	Method of fabricating metal oxide semiconductor transistor
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0913USA
Receipt Date:	26-OCT-2009
Filing Date:	09-AUG-2007
Time Stamp:	04:27:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	718415.PDF	73908 b9d19316a11df6c78828385675bad7c4d7f131ce	no	3

Warnings:

Information:

2	Amendment/Req. Reconsideration-After Non-Final Reject	718414.PDF	59901 cb1ade15424e3fd93567e431cfd8b068d4f54578b	no	1
Warnings:					
Information:					
3	Claims	718413.PDF	54239 c460aa1ef328803eb545d98fde6a36a4402ee4f	no	2
Warnings:					
Information:					
4	Specification	718412.PDF	49939 e7998a6db365861d4239a8f166ddc6b2990a3f05	no	1
Warnings:					
Information:					
Total Files Size (in bytes):				237987	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Objection of the Specification

- 5 The title of the invention has been amended to “Metal oxide semiconductor transistor”,
as requested by the Examiner. Acceptance of the new title is respectfully requested.

Rejection of claims 31-32 and 34 under 35 U.S.C. 102(e) as being anticipated by
10 **Luo et al., hereafter “Luo” (U.S. Publication No. 2008/0006818 A1).**

Claim 31 is amended to specify that the raised epitaxial layers are positioned in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate.

- 15 Luo in Fig. 5 of the cited reference recites two epitaxial layers 28/30. These two epitaxial layers 28/30 however are not disposed above the surface of the substrate 12, as recited in the amended claim 31. Instead, the two epitaxial layers 28/30 are formed evenly with the surface of the substrate 12.

- 20 As the limitation of the raised epitaxial layers disposed above the surface of the semiconductor substrate is clearly not satisfied by Luo’s invention, applicants submit that the MOS transistor structure of the present invention is patentable over the cited reference. Reconsideration of the amended claim 31 is respectfully requested. As
25 claims 32 and 34 are dependent upon claim 31, applicants submit that if claim 31 is found allowable, claims 32 and 34 should additionally be found allowable.

Rejection of claims 33 and 35-36 under 35 U.S.C. 103(a) as being unpatentable
30 **over Luo et al., hereafter “Luo” (U.S. Publication No. 2008/0006818 A1).**

Claims 33 and 35-36 are dependent upon the amended claim 31, applicants submit that if claim 31 is found allowable, claims 33 and 35-36 should additionally be found allowable.

5

Rejection of claims 37-38 under 35 U.S.C. 103(a) as being unpatentable over Luo in view of Chien et al., hereafter “Chien” (U.S. Patent No. 6,815,770 B1).

10 Claims 37-38 are dependent upon the amended claim 31, applicants submit that if claim 31 is found allowable, claims 37-38 should additionally be found allowable.

New Claims

15

Dependent claims 39-41 are added to describe additional embodiments of the present invention. Specifically, claim 39 recites that the edge of the raised epitaxial layers is not aligned with the edge of the spacer, claim 40 recites that the spacer further comprises a L-shaped spacer, and the claim 41 recites a lightly doped drain is
20 disposed in the semiconductor substrate and outside the raised epitaxial layers.

It is respectfully suggested that none of the cited references teaches these limitations and as claims 39-41 are dependent upon claim 31, applicants submit that if claim 31 is found allowable, claims 39-41 should additionally be found allowable.

25

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

30

Appl. No. 11/836,772
Amdt. dated October 26, 2009
Reply to Office action of September 09, 2009

Sincerely yours,

_____/Winston Hsu/

Date: 10/26/2009

Winston Hsu, Patent Agent No. 41,526

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

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e-mail : winstonhsu@naipo.com

10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/836,772		Filing Date 08/09/2007		☐ To be Mailed	
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APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A				N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =				X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =				X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL		TOTAL	

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	10/26/2009	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 11	Minus	** 20	= 0	X \$ =				X \$52=	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$ =				X \$220=	0
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE	0	

(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =				X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =				X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR		TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/KIM WATSON SAUNDERS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/836,772	08/09/2007	Chu-Yin Tseng	NAUP0913USA	3794
27765 7590 12/09/2009 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER DANG, PHUC T	
			ART UNIT 2892	PAPER NUMBER
			NOTIFICATION DATE 12/09/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No. 11/836,772	Applicant(s) TSENG ET AL.	
	Examiner Phuc T. Dang	Art Unit 2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 10/26/2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 31-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 31-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 August 2007 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Amendment

1. The amendment filed on 10/26/2009 has been acknowledged and considered.

In amendment, applicant amended claim 31 and added claims 39-41 and remained claims 32-38.

Claims 31-41 are currently pending in the application.

Drawings

2. The drawings are objected to because there is no figure showing the two raised epitaxial layers positioned in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate as claimed in claim 31. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any

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required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections-35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 31-40 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(S), at the time the application was filed, had possession of the claimed invention.

In claim 31, “the two raised epitaxial layers positioned in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate” is a new matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maszara (U.S. Publication No. 2006/0211245 A1).

Regarding claim 31, Maszara, Figs. 1-4 and related text, discloses a MOS transistor structure, comprising:

- a gate 106 formed on a semiconductor substrate 102;

- two raised epitaxial layers 402 & 404 positioned respectively in the semiconductor substrate 102 next to the relative sides of the gate 106 and above the surface of the semiconductor substrate 102;

- a spacer 200 formed on the sidewall of the gate 16 and extending laterally upon a portion of the raised epitaxial layer 402 & 404 (Figs. 1-4).

Figs. 1-4 of Maszara discloses the features of the claimed invention as discussed above but does not disclose two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

However, as shown in the background of the Maszara specification in paragraph [0006]-[0007], the substrate on both sides of the gate is doped by ion implantation into the surface of the substrate. These doped regions of the substrate are referred as “shallow source/drain junctions” which are referred as two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

Then, it would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Figures 1-4 of Maszara to provide two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate as

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taught by the background of Maszara for a purpose of improving the semiconductor structure of the transistor.

5. Claims 31, 33-36 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Natzle (U.S. Patent No. 6,774,000 B2) in view of Murthy et al., hereafter “Murthy” (U.S. Patent No. 7,195,985 B2).

Regarding claim 31, Natzle, Figs. 1A-1F and related text, discloses a MOS transistor structure, comprising:

- a gate 16 formed on a semiconductor substrate 12;

- two raised epitaxial layers 22D & 22S positioned respectively in the semiconductor substrate 12 next to the relative sides of the gate 16 and above the surface of the semiconductor substrate 12;

- a spacer 22G formed on the sidewall of the gate 16; and

- two doped region 12D & 12S formed respectively in the semiconductor substrate 12 next to the relative sides of the gate 16 (Figs. 1A-1F).

Figs. 1A-1F of Natzle discloses a spacer 22G formed on the sidewall of the gate 16, but does not disclose extending upon a portion of the raised epitaxial layer 22D & 22S.

However, Murthy, in the same field of endeavor, discloses a spacer 112 & 114 formed on the sidewall of the gate 190 and extending upon a portion of the raised epitaxial layer 370 & 380 (Fig. 3A).

Then, it would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Figures 1A-1F of Natzle to provide the spacer formed on the sidewall of the gate and extending upon a portion of the raised epitaxial layer as

taught by the background of Murthy for a purpose of improving the performance of the circuit on the semiconductor substrate.

Regarding claims 33-36 and 39, Murthy discloses the MOS transistor comprises a PMOS and a NMOS transistor (col. 2, lines 59-64) and the epitaxial layer comprises SiGe (col. 7, lines 47-51) and SiC (col. 7, lines 53-64).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Natzle to provide the MOS transistor comprises a PMOS and a NMOS transistor and the epitaxial layer comprises SiGe and SiC as taught by the background of Murthy for a purpose of improving the performance of the circuit on the semiconductor substrate.

Regarding claim 39, Natzle discloses wherein the edge of the raised epitaxial layers 22D & 22S is not aligned with the edge of the spacer 22G (Fig. 1E-1F).

6. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maszara or Natzle and Murthy in view of Luo et al., hereafter "Luo" (U.S. Publication No. 2008/0006818 A1).

Regarding claim 32, Maszara or Natzle and Murthy discloses the features of the claimed invention as discussed above, but does not disclose the gate further comprises a dielectric layer, a conductive layer, positioned on the dielectric layer; and a cap layer, positioned on the conductive layer.

However, Luo, in the same field of endeavor, discloses the gate further comprises a dielectric layer 20, a conductive layer 22, positioned on the dielectric layer; and a cap layer 24, positioned on the conductive layer (Fig. 5).

Then, it would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Maszara or Natzle and Murthy to provide the gate further comprises a dielectric layer, a conductive layer, positioned on the dielectric layer; and a cap layer, positioned on the conductive layer as taught by the background of Murthy for a purpose of improving the performance of the MOS transistor.

7. Claims 37-38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maszara or Natzle and Murthy in view Chien et al., hereafter "Chien" (U.S. Patent No. 6,815,770 B1).

Regarding claims 37-38, Maszara or Natzle and Murthy discloses the features of the claimed invention as discussed above, but does not disclose wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer.

However, Chien, in the same field of endeavor, discloses the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer (Fig. 1).

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Maszara or Natzle and Murthy to provide the spacer further comprises an offset spacer, positioned between the gate and the spacer, wherein the spacer further comprises an oxide liner and a nitride spacer as taught by Chien for a purpose of controlling the step of doping.

Regarding claim 41, Maszara or Natzle and Murthy discloses the features of the claimed invention as discussed above, but does not disclose further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers.

However, Chien, in the same field of endeavor, discloses further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers (Figs. 1 & 4 and Abstract).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Maszara or Natzle and Murthy to provide a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers as taught by Chien for a purpose of improving the performance of the MOS transistor.

8. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maszara or Natzle and Murthy in view of Chidambarrao et al., hereafter "Chidambarrao" (U.S. Publication No. 2008/0179636 A1).

Regarding claim 40, Maszara or Natzle and Murthy discloses the features of the claimed invention as discussed above, but does not disclose the spacer further comprises a L-shaped spacer.

However, Chidambarrao, in the same field of endeavor, discloses the spacer further comprises a L-shaped spacer 26 (Fig. 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Maszara or Natzle and Murthy to provide the spacer further comprises a L-shaped spacer as taught by Chidambarrao for a purpose of improving the performance of the transistor.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on M-F (9-6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le, can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Phuc T Dang/

Primary Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 11/836,772	Applicant(s)/Patent Under Reexamination TSENG ET AL.	
	Examiner Phuc T. Dang	Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0211245 A1	09-2006	Maszara, Witold P.	438/683
*	B	US-6,774,000 B2	08-2004	Natzle et al.	438/300
*	C	US-7,195,985 B2	03-2007	Murthy et al.	438/341
*	D	US-2008/0179636 A1	07-2008	Chidambarao et al.	257/255
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	N					
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	R					
	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant					☐ CPA					☐ T.D.					☐ R.1.47				
CLAIM		DATE																	
Final	Original	08/03/2009	09/03/2009	11/30/2009															
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	2	÷	-	-															
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	27	÷	-	-															
	28	÷	-	-															
	29	÷	-	-															
	30	÷	-	-															
	31	÷	✓	✓															
	32	÷	✓	✓															
	33	÷	✓	✓															
	34	÷	✓	✓															
	35	÷	✓	✓															
	36	÷	✓	✓															

<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant										☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE													
Final	Original	08/03/2009	09/03/2009	11/30/2009											
	37	÷	✓	✓											
	38	÷	✓	✓											
	39			✓											
	40			✓											
	41			✓											

Search Notes 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
257	19,190,192,197	09/03/2009	PD
same	as above	11/30/2009	PD

SEARCH NOTES		
Search Notes	Date	Examiner
INVENTOR SEARCH	09/03/2009	PD
EAST SEARCH	09/03/2009	PD
EAST SEARCH	11/30/2009	PD

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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CONFIRMATION NO. 3794

SERIAL NUMBER 11/836,772	FILING or 371(c) DATE 08/09/2007 RULE	CLASS 257	GROUP ART UNIT 2892	ATTORNEY DOCKET NO. NAUP0913USA		
APPLICANTS Chu-Yin Tseng, Tainan County, TAIWAN; Shih-Chieh Hsu, Hsinchu City, TAIWAN; Chih-Chiang Wu, Taichung County, TAIWAN; Shyh-Fann Ting, Tai-Nan City, TAIWAN; Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN; Hsuan-Hsu Chen, Tai-Nan City, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/20/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/PHUC T DANG/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 14	TOTAL CLAIMS 38	INDEPENDENT CLAIMS 3
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE METAL OXIDE SEMICONDUCTOR TRANSISTOR						
FILING FEE RECEIVED 1900	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	"20080006818"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 12:47
L2	3570	((raised vertical\$2) with (epi epitaxial) with (substrate wafer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 12:48
L3	471	((raised vertical\$2) with (epi epitaxial) with (substrate wafer)) with (gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 12:49
L4	208	3 and mos	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 12:49
L5	195	4 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 12:49
L6	124	5 and ((dop\$3) with (gate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 13:13
L7	45	5 and ((dop\$3 near region) with (gate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 13:45

L8	20	"6774000" "20070224766" "20080179636"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 14:14
L9	9	8 and (pmos p-mos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 14:15
L10	4	9 and sige	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 14:16
L11	4	10 and (epi epitaxial)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 14:20
L12	9	8 and (nmos n-mos)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 14:35
L13	2	8 and ((lidd) (lightly near dop \$4) (lightly-dop\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 14:43
L14	3	8 and ((sic) (silicon near carbon))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 14:50
L15	38	((lidd) (lightly-doped) (lightly near doped)) with (raised vertical) near3 (((epi) (epitaxial\$2)) near2 (layer)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 15:03

L16	38	15 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 15:04
L17	38	((doped doping) with (raised vertical) near3 (((epi) (epitaxial\$2)) near2 (layer)) with (substrate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 15:07
L18	36	17 and @ad<="20070809"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/30 15:08
S1	1115	((tungsten near nitride) and ((tungsten near2 layer) with (substrate wafer)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:08
S2	218	((tungsten with precursor) with ((nitrogen) ("n. sub.2"))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:09
S3	63	S1 and S2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:09
S4	15	S3 and @ad<="20020226"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:09
S5	255	(tungsten near layer) with ((physical near vapor near deposition) (pvd))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:53

S6	53	(tungsten with precursor) with (diborane)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:55
S7	7	S5 and S6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:55
S8	0	S7 and @ad<="20020226"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:55
S9	78	S5 and @ad<="20020226"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:55
S10	4	(tungsten near layer) with ((physical near vapor near deposition) (pvd)) with (improv\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:57
S11	7	(tungsten near layer) with ((physical near vapor near deposition) (pvd)) with (enhanc\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 10:58
S12	24	((tungsten near layer) with ((physical near vapor near deposition) (pvd)) with ((atomic near layer near deposition) (ald)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 11:00
S13	1	S12 and @ad<="20020226"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 11:00

S14	175	(tungsten near hexafluoride) with (diborane)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 11:26
S15	16	(tungsten near layer) with (tungsten near hexafluoride) with (diborane)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 11:27
S16	4	S15 and @ad<="20020226"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 11:27
S17	175	(tungsten) with (tungsten near hexafluoride) with (diborane)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 11:28
S18	48	S17 and @ad<="20020226"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/11/19 11:28

11/ 30/ 2009 3:14:47 PM

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Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (09-08)

Approved for use through 10/31/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL **(Submitted Only via EFS-Web)**

Application Number	11/836,772	Filing Date	2007-08-09	Docket Number (if applicable)	NAUP0913USA	Art Unit	2892
First Named Inventor	Chu-Yin Tseng			Examiner Name	DANG, PHUC T		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
 (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
 The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
 Deposit Account No 503105

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (09-08)

Approved for use through 10/31/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Signature of Registered U.S. Patent Practitioner			
Signature	/WINSTON HSU/	Date (YYYY-MM-DD)	2010-03-05
Name	Winston Hsu	Registration Number	41526

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		11836772		
Filing Date:		09-Aug-2007		
Title of Invention:		METAL OXIDE SEMICONDUCTOR TRANSISTOR		
First Named Inventor/Applicant Name:		Chu-Yin Tseng		
Filer:		Winston Hsu/Karen Chen		
Attorney Docket Number:		NAUP0913USA		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD (\$)				810

Electronic Acknowledgement Receipt	
EFS ID:	7136994
Application Number:	11836772
International Application Number:	
Confirmation Number:	3794
Title of Invention:	METAL OXIDE SEMICONDUCTOR TRANSISTOR
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu/Karen Chen
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP0913USA
Receipt Date:	05-MAR-2010
Filing Date:	09-AUG-2007
Time Stamp:	02:05:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$810
RAM confirmation Number	5976
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	798824.PDF	119454	no	5
			14b870072b2666881f85e3c158bace498d866eb0		
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	798823.PDF	67273	no	1
			d82184ea1b17fd2ac7ce95025b13c866278bb1d		
Warnings:					
Information:					
3	Claims	798822.PDF	62031	no	2
			e0b0784dc0b18ca0776e44042aeb8b43cdb37f26		
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	798819.PDF	339541	no	3
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Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	30340	no	2
			9170bc9afd826d17e8597e06f5426433b24e786d		
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Information:					
Total Files Size (in bytes):			618639		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Request for Continued Examination:

- 5 The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Objection of the drawings

- 10 Regarding the objection of the drawings, the applicants would like to direct the Examiner's attention to Figs. 3-5 of the instant application. In Fig. 3-5, the limitation recited in claim 31 is fully satisfied by the PMOS transistor 234 shown on left hand side of the CMOS structure.

- 15 For instance, the feature of "two raised epitaxial layers 220 positioned in the semiconductor substrate 200 next to the relative sides of the gate 212 and above the surface of the semiconductor substrate 200" is clearly revealed in Figs. 3-5.

- 20 **Rejection of claims 31-40 under 35 U.S.C. 112, first paragraph.**

- Similar the above arguments made for the drawings, the applicants would like to direct the Examiner's attention to Figs. 3-5 and paragraphs [0020] to [0022] of the specification. In these paragraphs, the limitation of "two raised epitaxial layers 220
25 positioned in the semiconductor substrate 200 next to the relative sides of the gate 212 and above the surface of the semiconductor substrate 200" is clearly addressed.
Hence claims 31-40 already contain subject matter which was described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed
30 invention. Reconsideration of claims 31-40 is respectfully requested.

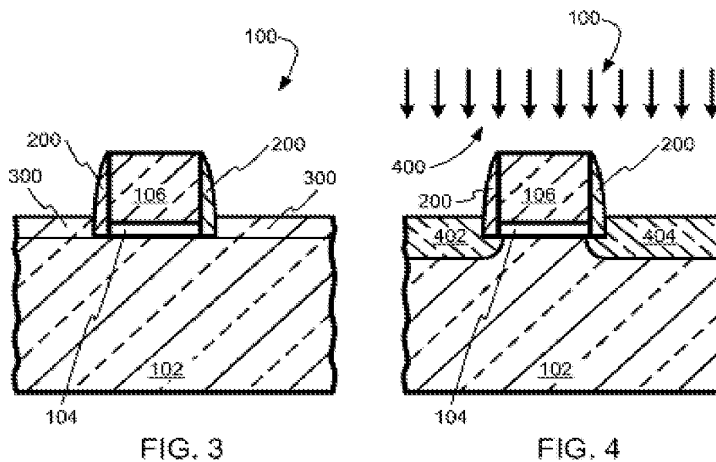
Rejection of claim 31 under 35 U.S.C. 103(a) as being unpatentable over Maszara (US Publication No. 2006/0211245 A1).

5

Claim 31 has been amended to specify that a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.

Maszara in Fig. 4 (shown below) of the cited reference recites two regions 402/404.

10 However, these two regions 402/404 are source/drain regions formed by ion implantation and could not be construed as the raised epitaxial layers of the present invention. The epitaxial layers suggested by Maszara in paragraph [0035] of the cited reference are the layers 300 shown in Fig. 3. As the epitaxial layers 300 are formed on surface of the substrate 102 after the formation of the spacer 200, the spacer 200
15 could not have been formed on the epitaxial layers 300 and the limitation of the spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers as recited in claim 31 of the present invention is clearly not satisfied.



20

In addition, as no recess is formed in the substrate 102 of Maszara, none of the

epitaxial layer 300 is formed in the substrate 102. Instead, the entire epitaxial layer 300 is disposed above the surface of the semiconductor substrate 102 and the limitation of the raised epitaxial layers positioned in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate as recited in claim 31 of the present invention is again not satisfied.

Lastly, as the spacer 200 is not extended on a portion of the epitaxial layers 300, the limitation of a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate is also not satisfied.

As the above features are clearly absent in Maszara's invention, applicants submit that the MOS transistor structure of the present invention is clearly patentable over the cited reference. Reconsideration of claim 1 is respectfully requested.

Rejection of claims 31, 33-36 and 39 under 35 U.S.C. 103(a) as being unpatentable over Natzle (U.S. Patent No. 6,774,000 B2) in view of Murthy (U.S. Patent No. 7,195,985 B2).

Claim 31 has been amended to specify that a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.

Natzle in Figs. 1A-1F of the cited reference recites a spacer 22G formed on the sidewall of the gate 16 but fails to teach that the spacer 22G extends upon a portion of the raised epitaxial layer 22D and 22S, as pointed out by the Examiner.

Murthy in Fig. 3A (shown below) of the cited reference recites two epitaxial layers 370 and 380 positioned in the semiconductor substrate and above the surface of the substrate. However, as the epitaxial layers 370 and 380 are deposited in the recess after the formation of the spacer and that the recess is formed well below the spacer,

Rejection of claims 37-38 and 41 under 35 U.S.C. 103(a) as being unpatentable over Maszara or Natzle and Murthy in view of Chien et al (U.S. Patent No. 6,815,770 B1).

- 5 As claims 37-38 and 41 are dependent upon claim 31, applicants submit that if claim 31 is found allowable, claims 37-38 and 41 should additionally be found allowable.

Rejection of claim 40 under 35 U.S.C. 103(a) as being unpatentable over Maszara or Natzle and Murthy in view of Chidambarrao et al (U.S. Publication No. 2008/0179636 A1).

- 10 As claim 40 is dependent upon claim 31, applicants submit that if claim 31 is found allowable, claim 40 should additionally be found allowable.

15

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

- 20 Sincerely yours,

_____/Winston Hsu/

Date: 03/05/2010

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.

- 25 Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

- Note: Please leave a message in my voice mail if you need to talk to me. (The time in
30 D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

Metal oxide semiconductor transistor

Appl. No. : 11/836,772 Confirmation No. : 3794
Applicant : Chu-Yin Tseng et al.
Filed : August 9, 2007
TC/A.U. : 2892
Examiner : DANG, PHUC T
Docket No. : NAUP0913USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

Sir:

- 5 In response to the Office action of December 9, 2009, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

5

Listing of Claims:

Claims 1-30 (canceled)

- 10 Claim 31 (currently amended): A MOS transistor structure, comprising:
a gate formed on a semiconductor substrate;
two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;
15 a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and
two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

20

Claim 32 (original): The structure of claim 31, wherein the gate further comprises:
a dielectric layer;
a conductive layer, positioned on the dielectric layer; and
a cap layer, positioned on the conductive layer.

25

Claim 33 (original): The structure of claim 31, wherein the MOS transistor comprises a PMOS transistor.

Claim 34 (original): The structure of claim 33, wherein the epitaxial layer comprises
30 SiGe.

Claim 35 (original): The structure of claim 31, wherein the MOS transistor comprises an NMOS transistor.

- 5 Claim 36 (original): The structure of claim 35, wherein the epitaxial layer comprises SiC.

Claim 37 (original): The structure of claim 31, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.

10

Claim 38 (original): The structure of claim 31, wherein the spacer further comprises an oxide liner and a nitride spacer.

- 15 Claim 39 (previously presented): The structure of claim 31, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.

Claim 40 (previously presented): The structure of claim 31, wherein the spacer further comprises a L-shaped spacer.

- 20 Claim 41 (previously presented): The structure of claim 31, further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers.

Electronic Acknowledgement Receipt	
EFS ID:	7136994
Application Number:	11836772
International Application Number:	
Confirmation Number:	3794
Title of Invention:	METAL OXIDE SEMICONDUCTOR TRANSISTOR
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu/Karen Chen
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP0913USA
Receipt Date:	05-MAR-2010
Filing Date:	09-AUG-2007
Time Stamp:	02:05:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$810
RAM confirmation Number	5976
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	798824.PDF	119454 14b870072b2666881f85e3c158bace498d866eb0	no	5
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	798823.PDF	67273 d82184ea1b17fd2ac7ce95025b13c866278bb1d	no	1
Warnings:					
Information:					
3	Claims	798822.PDF	62031 e0b0784dc0b18ca0776e44042aeb8b43cdeb37f26	no	2
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	798819.PDF	339541 cea6ce6d3c675c54d4914d2f3d4d44ee65e87032a	no	3
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	30340 9170bc9afd826d17e8597e06f5426433b24e786d	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			618639		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/836,772		Filing Date 08/09/2007		☐ To be Mailed	
---	--	--	--	--	---	--	----------------------------------	--	---------------------------------------	--

APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A		N/A		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR	X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL				

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	03/05/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 11	Minus	** 20	= 0	X \$ =		OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$ =		OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))							OR			
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Legal Instrument Examiner:
/Theresa Dawkins/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 03/24/2010

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

DANG, PHUC T

ART UNIT

PAPER NUMBER

2892

DATE MAILED: 03/24/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/836,772	08/09/2007	Chu-Yin Tseng	NAUP0913USA	3794

TITLE OF INVENTION: METAL OXIDE SEMICONDUCTOR TRANSISTOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	06/24/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27765 7590 03/24/2010

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Certificate of Mailing or Transmission

hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/836,772 08/09/2007 Chu-Yin Tseng NAUP0913USA 3794

TITLE OF INVENTION: METAL OXIDE SEMICONDUCTOR TRANSISTOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	06/24/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
DANG, PHUC T	2892	257-190000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/836,772	08/09/2007	Chu-Yin Tseng	NAUP0913USA	3794
27765	7590	03/24/2010	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			DANG, PHUC T	
			ART UNIT	PAPER NUMBER
			2892	
DATE MAILED: 03/24/2010				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 306 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 306 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/836,772	TSENG ET AL.	
	Examiner	Art Unit	
	Phuc T. Dang	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to RCE filed on 03/05/2010.

2. ☒ The allowed claim(s) is/are 31-41 (renumbered as in new claims 1-11).

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
--	--

/Phuc T Dang/ Primary Examiner, Art Unit 2892	
--	--

DETAILED ACTION

Continued Examination under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after Final. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114.

Applicant's submission filed on 03/05/2010 has been entered.

In the request for continued examination, the applicants canceled claims 1-30 and amended claim 1 and remained claims 31-41.

Claims 31-41 are currently pending in the application.

Oath/Declaration

2. The oath/declaration filed on 08/09/2007 is acceptable.

Examiner's Statement of Reasons for Allowance

3. Claims 31-41 are allowed.

Claims 31-41 are renumbered as in new claims 1-11.

4. The following is an examiner's statement of reasons for allowance:

None of the prior art teaches a MOS transistor structure, comprising a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of

Art Unit: 2892

the semiconductor substrate, in combination with the other structures in the independent claim

31.

Claims 32-41 are directly or indirectly depend on the independent claim 31.

Cited Prior Arts

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Park et al. (U.S. Patent No. 6,429,084 B1), Chan et al. (U.S. Patent No. 6,110,787) and Zhu et al. (U.S. Publication No. 2005/0156154 A1).

Conclusion

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submission should be clearly labeled "Comments on Statement of Reasons for Allowance".

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300 for regular communications and After Final communications.

9. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Application/Control Number: 11/836,772
Art Unit: 2892

Page 4

/Phuc T Dang/

Primary Examiner, Art Unit 2892

Notice of References Cited	Application/Control No. 11/836,772		Applicant(s)/Patent Under Reexamination TSENG ET AL.	
	Examiner Phuc T. Dang		Art Unit 2892	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,429,084 B1	08-2002	Park et al.	438/305
*	B	US-6,110,787	08-2000	Chan et al.	438/300
*	C	US-2005/0156154 A1	07-2005	Zhu et al.	257/019
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 3794

SERIAL NUMBER 11/836,772	FILING or 371(c) DATE 08/09/2007 RULE	CLASS 257	GROUP ART UNIT 2892	ATTORNEY DOCKET NO. NAUP0913USA		
APPLICANTS Chu-Yin Tseng, Tainan County, TAIWAN; Shih-Chieh Hsu, Hsinchu City, TAIWAN; Chih-Chiang Wu, Taichung County, TAIWAN; Shyh-Fann Ting, Tai-Nan City, TAIWAN; Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN; Hsuan-Hsu Chen, Tai-Nan City, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/20/2007						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/PHUC T DANG/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 14	TOTAL CLAIMS 38	INDEPENDENT CLAIMS 3
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE METAL OXIDE SEMICONDUCTOR TRANSISTOR						
FILING FEE RECEIVED 1900	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3070	(raised near epitaxial epi) and (substrate) and ((spacer \$1) (sidewall\$1) (side-wall \$1)) and (gate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 15:35
L2	476495	"257"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 15:36
L3	2646	1 and 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 15:36
L4	873	257/190.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 15:36
L5	32	1 and 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 15:36
L6	3	"20060211245"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 15:56
L7	28	"6774000" "7195985"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 15:57

L8	1776	257/192.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:07
L9	43	1 and 8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:07
L10	1498	257/197.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:14
L11	18	1 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:15
L12	484	257/19.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:15
L13	32	1 and 12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:15
L14	2551	1 and @ad<="20070609"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:25
L15	14	14 and (raised near (epi epitaxial)) with (substrate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/03/15 16:26

3/ 15/ 2010 4:27:50 PM

C:\ Documents and Settings\ PDang1\ My Documents\ EAST\ Workspaces\ today022110.wsp

<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
Final	Original	08/03/2009	09/03/2009	11/30/2009	03/17/2010						
	1	÷	-	-	-						
	2	÷	-	-	-						
	3	÷	-	-	-						
	4	÷	-	-	-						
	5	÷	-	-	-						
	6	÷	-	-	-						
	7	÷	-	-	-						
	8	÷	-	-	-						
	9	÷	-	-	-						
	10	÷	-	-	-						
	11	÷	-	-	-						
	12	÷	-	-	-						
	13	÷	-	-	-						
	14	÷	-	-	-						
	15	÷	-	-	-						
	16	÷	-	-	-						
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	27	÷	-	-	-						
	28	÷	-	-	-						
	29	÷	-	-	-						
	30	÷	-	-	-						
1	31	÷	✓	✓	=						
2	32	÷	✓	✓	=						
3	33	÷	✓	✓	=						
4	34	÷	✓	✓	=						
5	35	÷	✓	✓	=						
6	36	÷	✓	✓	=						

<i>Index of Claims</i> 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE									
Final	Original	08/03/2009	09/03/2009	11/30/2009	03/17/2010						
7	37	÷	✓	✓	=						
8	38	÷	✓	✓	=						
9	39			✓	=						
10	40			✓	=						
11	41			✓	=						

Search Notes 	Application/Control No. 11836772	Applicant(s)/Patent Under Reexamination TSENG ET AL.
	Examiner Phuc T Dang	Art Unit 2892

SEARCHED			
Class	Subclass	Date	Examiner
257	19,190,192,197	09/03/2009	PD
438	218,285	09/03/2009	PD
same	as above	11/30/2009	PD
same	as above	03/17/2010	PD

SEARCH NOTES		
Search Notes	Date	Examiner
INVENTOR SEARCH	09/03/2009	PD
EAST SEARCH	09/03/2009	PD
EAST SEARCH	11/30/2009	PD
EAST SEARCH (Interference Search History Printout)	03/17/2010	PD

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
same	as above	03/17/2010	PD

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
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Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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27765 7590 03/24/2010

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Stephanie Lai	(Depositor's name)
/Stephanie Lai/	(Signature)
05/19/2010	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/836,772	08/09/2007	Chu-Yin Tseng	NAUP0913USA	3794

TITLE OF INVENTION:

Metal oxide semiconductor transistor

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$1510	\$300	\$1810	06/24/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
DANG, PHUC T	2892	257-190000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Winston Hsu
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

UNITED MICROELECTRONICS CORP.

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

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- ☐ A check in the amount of the fee(s) is enclosed.
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☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-3105.

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /WINSTON HSU/

Date 05/19/2010

Typed or printed name Winston Hsu

Registration No. 41,526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:		11836772		
Filing Date:		09-Aug-2007		
Title of Invention:		METAL OXIDE SEMICONDUCTOR TRANSISTOR		
First Named Inventor/Applicant Name:		Chu-Yin Tseng		
Filer:		Winston Hsu		
Attorney Docket Number:		NAUP0913USA		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt	
EFS ID:	7630311
Application Number:	11836772
International Application Number:	
Confirmation Number:	3794
Title of Invention:	METAL OXIDE SEMICONDUCTOR TRANSISTOR
First Named Inventor/Applicant Name:	Chu-Yin Tseng
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0913USA
Receipt Date:	19-MAY-2010
Filing Date:	09-AUG-2007
Time Stamp:	03:34:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1810
RAM confirmation Number	17422
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NAUP0913-0-E2-1-PTOL85b-PTO.pdf	165359 8f20fd2b406dfe2bef83a10c5e16a4f6daa328d6	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	31955 027ae1bc2dff647a863f7467f6ae95d7d46cca9f	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			197314		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/836,772	06/29/2010	7745847	NAUP0913USA	3794

27765 7590 06/09/2010
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 306 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Chu-Yin Tseng, Tainan County, TAIWAN;
Shih-Chieh Hsu, Hsinchu City, TAIWAN;
Chih-Chiang Wu, Taichung County, TAIWAN;
Shyh-Fann Ting, Tai-Nan City, TAIWAN;
Po-Lun Cheng, Kao-Hsiung Hsien, TAIWAN;
Hsuan-Hsu Chen, Tai-Nan City, TAIWAN;