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(54) **METHOD AND STRUCTURE FOR SECOND SPACER FORMATION FOR STRAINED SILICON MOS TRANSISTORS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 409 days.

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(57) **ABSTRACT**

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438/300

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438/297, 230, 231, 300
See application file for complete search history.

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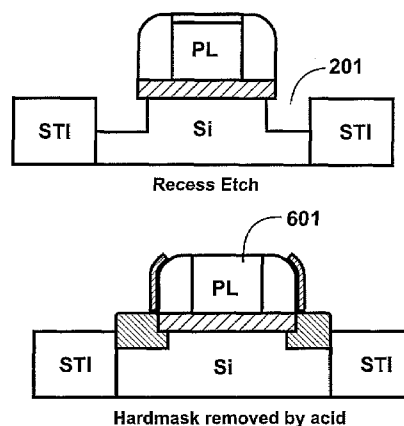
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A method for forming a CMOS semiconductor wafer. The method includes providing a semiconductor substrate (e.g., silicon wafer) and forming a dielectric layer (e.g., silicon dioxide, silicon oxynitride) overlying the semiconductor substrate. The method includes forming a gate layer overlying the dielectric layer and patterning the gate layer to form a gate structure including edges. The method includes forming a dielectric layer overlying the gate structure to protect the gate structure including the edges. Preferably, the dielectric layer has a thickness of less than 40 nanometers. The method includes etching a source region and a drain region adjacent to the gate structure using the dielectric layer as a protective layer and depositing silicon germanium material into the source region and the drain region to fill the etched source region and the etched drain region. The method causes a channel region between the source region and the drain region to be strained in compressive mode from at least the silicon germanium material formed in the source region and the drain region. The method includes forming a second protective layer overlying surfaces and performing an anisotropic etching process to form spacer structures to seal the gate structure.

18 Claims, 3 Drawing Sheets



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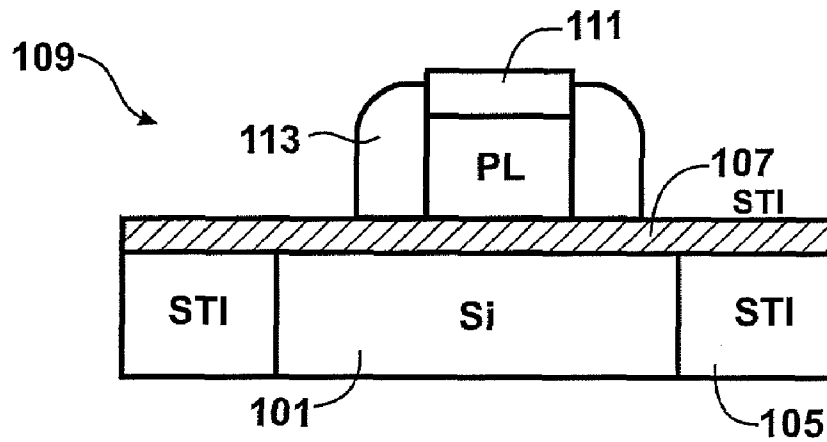
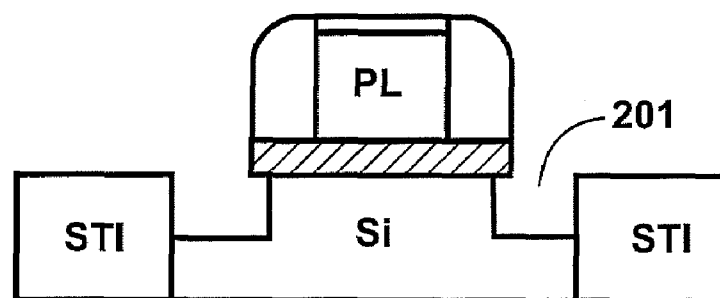


FIGURE 1



Recess Etch

FIGURE 2

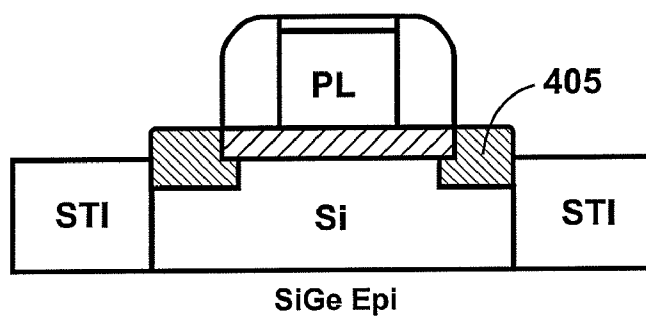


FIGURE 3

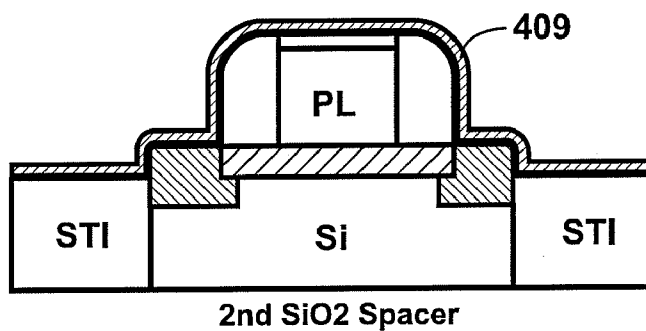


FIGURE 4

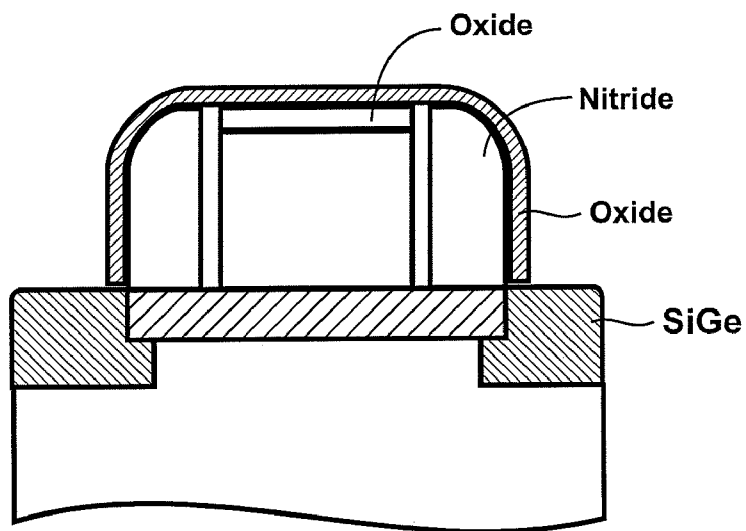


FIGURE 4A

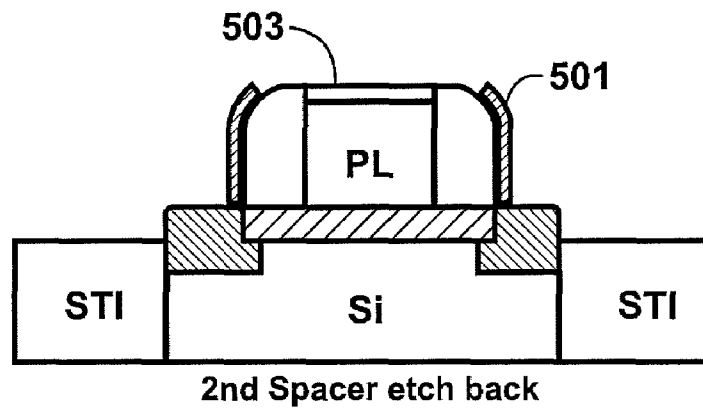


FIGURE 5

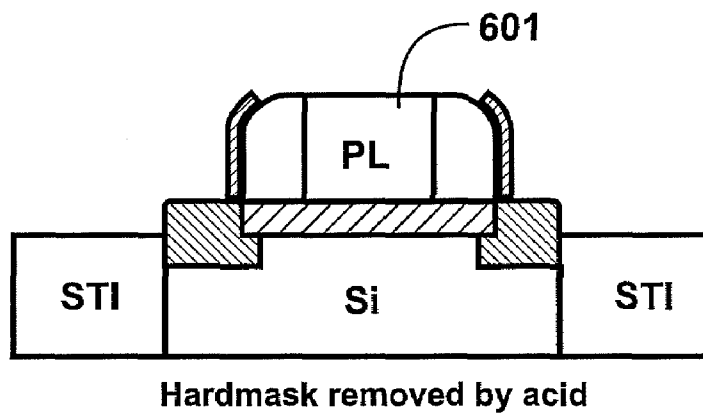


FIGURE 6

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METHOD AND STRUCTURE FOR SECOND SPACER FORMATION FOR STRAINED SILICON MOS TRANSISTORS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority to Chinese Patent Application No. 200510029992.1, filed on Sep. 19, 2005, commonly assigned, incorporated by reference herein for all purposes.

BACKGROUND OF THE INVENTION

The present invention is directed to integrated circuits and their processing for the manufacture of semiconductor devices. More particularly, the invention provides a method and structures for manufacturing MOS devices using strained silicon structures for advanced CMOS integrated circuit devices. But it would be recognized that the invention has a much broader range of applicability.

Integrated circuits have evolved from a handful of interconnected devices fabricated on a single chip of silicon to millions of devices. Conventional integrated circuits provide performance and complexity far beyond what was originally imagined. In order to achieve improvements in complexity and circuit density (i.e., the number of devices capable of being packed onto a given chip area), the size of the smallest device feature, also known as the device "geometry", has become smaller with each generation of integrated circuits.

Increasing circuit density has not only improved the complexity and performance of integrated circuits but has also provided lower cost parts to the consumer. An integrated circuit or chip fabrication facility can cost hundreds of millions, or even billions, of U.S. dollars. Each fabrication facility will have a certain throughput of wafers, and each wafer will have a certain number of integrated circuits on it. Therefore, by making the individual devices of an integrated circuit smaller, more devices may be fabricated on each wafer, thus increasing the output of the fabrication facility. Making devices smaller is very challenging, as each process used in integrated fabrication has a limit. That is to say, a given process typically only works down to a certain feature size, and then either the process or the device layout needs to be changed. Additionally, as devices require faster and faster designs, process limitations exist with certain conventional processes and materials.

An example of such a process is the manufacture of MOS devices itself. Such device has traditionally become smaller and smaller and produced faster switching speeds. Although there have been significant improvements, such device designs still have many limitations. As merely an example, these designs must become smaller and smaller but still provide clear signals for switching, which become more difficult as the device becomes smaller. Additionally, these designs are often difficult to manufacture and generally require complex manufacturing processes and structures. These and other limitations will be described in further detail throughout the present specification and more particularly below.

From the above, it is seen that an improved technique for processing semiconductor devices is desired.

BRIEF SUMMARY OF THE INVENTION

According to the present invention, techniques for processing integrated circuits for the manufacture of semiconductor devices are provided. More particularly, the invention pro-

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vides a method and structures for manufacturing MOS devices using strained silicon structures for CMOS advanced integrated circuit devices. But it would be recognized that the invention has a much broader range of applicability.

In a specific embodiment, the present invention provides a method for forming a CMOS semiconductor wafer. The method includes providing a semiconductor substrate, e.g., silicon substrate. The method includes forming a dielectric layer (e.g., oxide, silicon oxynitride) overlying the semiconductor substrate. The method includes forming a gate layer (e.g., doped polysilicon layer) overlying the dielectric layer. The method includes patterning the gate layer to form a gate structure including edges and forming a dielectric layer overlying the gate structure to protect the gate structure including the edges. In a specific embodiment, the dielectric layer has a thickness of less than 40 nanometers, but can be other dimensions. The method includes forming sidewall spacer structures from a portion of the dielectric layer and etching a source region and a drain region adjacent to the gate structure using the sidewall spacer structures made from a portion of the dielectric layer as a protective layer. The method includes depositing silicon germanium material into the source region and the drain region to fill the etched source region and the etched drain region. The method causes a channel region between the source region and the drain region to be strained in compressive mode from at least the silicon germanium material formed in the source region and the drain region. The method includes forming a second protective layer overlying surfaces including the silicon germanium material and performing an anisotropic etching process to form spacer structures to seal the gate structure.

In an alternative specific embodiment, the invention provides a method for forming a CMOS semiconductor wafer. The method includes providing a semiconductor substrate (e.g., silicon wafer) and forming a dielectric layer (e.g., silicon dioxide, silicon oxynitride) overlying the semiconductor substrate. The method includes forming a gate layer overlying the dielectric layer and patterning the gate layer to form a gate structure including edges. The method includes forming a dielectric layer overlying the gate structure to protect the gate structure including the edges. Preferably, the dielectric layer has a thickness of less than 40 nanometers. The method includes etching a source region and a drain region adjacent to the gate structure using the dielectric layer as a protective layer and depositing silicon germanium material into the source region and the drain region to fill the etched source region and the etched drain region. The method causes a channel region between the source region and the drain region to be strained in compressive mode from at least the silicon germanium material formed in the source region and the drain region. The method includes forming a second protective layer overlying surfaces and performing an anisotropic etching process to form spacer structures to seal the gate structure.

In a specific embodiment, the present invention provides a method using a silicon germanium fill material, which has a larger lattice spacing than single crystal silicon material. Such larger lattice spacing of silicon germanium fill material causes a channel region of an MOS transistor to be in a slightly compressive mode, when such material has been deposited in recessed regions adjacent to the channel region. Although the lattice spacing is slightly larger, silicon germanium still grows within the recessed regions, which are substantially single crystal silicon bearing material. Of course, there may be other variations, modifications, and alternatives.

Many benefits are achieved by way of the present invention over conventional techniques. For example, the present technique provides an easy to use process that relies upon con-

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ventional technology. In some embodiments, the method provides higher device yields in dies per wafer. Additionally, the method provides a process that is compatible with conventional process technology without substantial modifications to conventional equipment and processes. Preferably, the invention provides for an improved process integration for design rules of 90 nanometers and less. Additionally, the invention provides for increased mobility of holes using a strained silicon structure for CMOS devices. Depending upon the embodiment, one or more of these benefits may be achieved. These and other benefits will be described in more throughout the present specification and more particularly below.

Various additional objects, features and advantages of the present invention can be more fully appreciated with reference to the detailed description and accompanying drawings that follow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1 through 6 are simplified cross-sectional view diagram of a method for fabricating a CMOS device according to an embodiment of the present invention.

FIG. 4A is a simplified cross-sectional view structure of a double sidewall structure according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

According to the present invention, techniques for processing integrated circuits for the manufacture of semiconductor devices are provided. More particularly, the invention provides a method and structures for manufacturing MOS devices using strained silicon structures for CMOS advanced integrated circuit devices. But it would be recognized that the invention has a much broader range of applicability.

A method for fabricating a CMOS integrated circuit device according to an embodiment of the present invention may be outlined as follows:

1. Provide a semiconductor substrate, e.g., silicon wafer, silicon on insulator;
2. Form a dielectric layer (e.g., gate oxide or nitride) overlying the semiconductor substrate;
3. Form a gate layer (e.g., polysilicon, metal) overlying the dielectric layer;
4. Pattern the gate layer to form a gate structure including edges (e.g., a plurality of sides or edges);
5. Form a dielectric layer (e.g. hard mask) overlying the gate structure to protect the gate structure including the edges;
6. Etch a source region and a drain region adjacent to the gate structure using the dielectric layer as a protective layer;
7. Deposit silicon germanium material into the source region and the drain region to fill the etched source region and the etched drain region;
8. Cause a channel region between the source region and the drain region to be strained in compressive mode from at least the silicon germanium material formed in the source region and the drain region, wherein the channel region is about the same width as the patterned gate layer;
9. Form sidewall spacers overlying the patterned gate layer;
10. Expose hard mask on the patterned gate layer;

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11. Selectively remove the hard mask on patterned gate layer while maintaining the sidewall spacers overlying the patterned gate layer; and
12. Perform other steps, as desired.

The above sequence of steps provides a method according to an embodiment of the present invention. As shown, the method uses a combination of steps including a way of forming a CMOS integrated circuit device. Other alternatives can also be provided where steps are added, one or more steps are removed, or one or more steps are provided in a different sequence without departing from the scope of the claims herein. Further details of the present method can be found throughout the present specification and more particularly below.

FIGS. 1 through 6 are simplified cross-sectional view diagram of a method for fabricating a CMOS device according to an embodiment of the present invention. These diagrams are merely examples, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, alternatives, and modifications. In a specific embodiment, the method forms a shallow trench isolation region or regions 105 within a portion of the semiconductor substrate 101. The shallow trench isolation regions are formed using patterning, etching, and deposition of a dielectric fill material within the trench region. The dielectric fill material is often oxide or a combination of oxide and nitride depending upon the specific embodiment. The isolation regions are used to isolate active regions within the semiconductor substrate.

The method forms a gate dielectric layer 107 overlying the surface of the substrate. Preferably, the gate dielectric layer is oxide or silicon oxynitride depending upon the embodiment. The gate dielectric layer is preferably 10-20 nanometers and less than 40 nanometers depending upon the specific embodiment. The method forms a gate layer overlying the semiconductor substrate. The gate layer is preferably polysilicon that has been doped using either in-situ doping or ex-situ implantation techniques. The impurity for doping is often boron, arsenic, or phosphorus having a concentration ranging from about 1×10^{19} to about 1×10^{20} atoms/cm³. Of course, one of ordinary skill in the art would recognize many variations, modifications, and alternatives.

Preferably, the method forms a hard mask layer overlying the gate structure. The hard mask layer can be made of any suitable material such as a dielectric material or a metal material, or any combination of these. The hard mask layer is deposited to a suitable thickness to protect the underlying gate structure during etching and deposition steps, which will be further described below. In a specific embodiment, the present method forms sidewall spacers on edges of the patterned gate layer, as shown. The sidewall spacers are often made of a dielectric material, such as silicon dioxide, silicon nitride, or any combination of these, and the like.

As shown, the method patterned the gate layer to form an NMOS gate structure (not shown) including edges and patterns a PMOS gate structure 109 including edges. As shown, the hard mask 111 remains on the gate structure. The method forms lightly doped drain regions and sidewall spacers 113 on edges of patterned gate layer. The lightly doped drain regions are often formed using implantation techniques. For the PMOS device, the lightly doped drain region uses Boron or BF₂ impurity having a concentration ranging from about 1×10^{18} to about 1×10^{19} atoms/cm³. For the NMOS device, the lightly doped drain region uses arsenic impurity having a concentration ranging from about 1×10^{18} to about 1×10^{19} atoms/cm³. Depending upon the embodiment, the method forms a dielectric layer overlying the NMOS gate structure to

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protect the NMOS gate structure including the edges. The method also forms a dielectric protective layer overlying the PMOS gate structure to protect the PMOS gate structure including the edges. Preferably, the dielectric protective layer is the same layer for PMOS and NMOS devices. Alternatively, another suitable material can be used to protect the NMOS and PMOS gate structures, including lightly doped drain regions.

Referring to FIG. 2, the method simultaneously etches a first source region and a first drain region adjacent to the NMOS gate structure and etches a second source region and a second drain region **201** adjacent to the PMOS gate structure using the dielectric layer as a protective layer. The method uses reactive ion etching techniques including a SF_6 or CF_4 bearing species and plasma environment. In a preferred embodiment, the method performs a pre-treatment process on etched source/drain regions, which preserves the etched interfaces to maintain substantially high quality silicon bearing material. According to a specific embodiment, the each of the etched regions has a depth of ranging from about 100 Angstroms ($\text{\AA}$) to about 1000 $\text{\AA}$ and a length of about 0.1 μm to about 10 μm , and a width of about 0.1 μm to about 10 μm for a 90 nanometer channel length. Each of the etched regions has a depth of ranging from about 100 $\text{\AA}$ to about 1,000 $\text{\AA}$ and a length of about 0.1 μm to about 10 μm , and a width of about 0.1 μm to about 10 μm for a 65 nanometer channel length according to an alternative specific embodiment. Preferably, the hard mask remains on the gate structure and does not expose any of the gate structure during the etching process.

The method masks NMOS regions, while exposing the PMOS etched regions. Referring to FIG. 3, the method deposits silicon germanium material **405** into the first source region and the first drain region to cause a channel region between the first source region and the first drain region of the PMOS gate structure to be strained in a compressive mode. The silicon germanium is epitaxially deposited using in-situ doping techniques. That is, impurities such as boron are introduced while the silicon germanium material grows. A concentration ranges from about 1×10^{19} to about 1×10^{20} atoms/ cm^3 of boron according to a specific embodiment. As shown, the hard mask **401** still remains in tact to selectively grow the silicon germanium material into the etched regions without depositing on the top of the gate structure. Of course, there can be other variations, modifications, and alternatives.

The method strips the mask from NMOS regions. The method masks PMOS regions, while exposing the NMOS etched regions. The method deposits silicon carbide material into the second source region and second drain region to cause the NMOS channel region between the second source region and the second drain region of the NMOS gate structure to be strained in a tensile mode. The silicon carbide is epitaxially deposited using in-situ doping techniques. That is, impurities such as phosphorous (P) or arsenic (As) are introduced while the silicon carbide material grows. A concentration ranges from about 1×10^{19} to about 1×10^{20} atoms/ cm^3 of the above impurities according to a specific embodiment. Of course, there can be other variations, modifications, and alternatives.

Referring to FIG. 4, the method includes depositing a protective layer **409** overlying the entirety of the patterned structure. The patterned structure includes silicon germanium fill material, shallow trench isolation, sidewall spacers, and hard mask material, and others depending upon the embodiment. The protective layer can be a silicon nitride layer, a silicon oxide layer, or any combination of these depending upon the specific embodiment. In a preferred embodiment, the protec-

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tive layer seals phosphorous bearing impurities in the gate layer. In a preferred embodiment, protective layer comprises silicon nitride. Preferably, the final spacer structure comprises an ONO structure, as shown in FIG. 4A. The first oxide is about 200 $\text{\AA}$, nitride 500 to 800 $\text{\AA}$, second oxide 900 $\text{\AA}$ in the ONO, which is oxide on nitride on oxide structure. Depending upon the embodiment, the protective layer comprises PECVD oxide, or TEOS CVD, or thermal CVD, and others. Of course, one of ordinary skill in the art would recognize many variations, modifications, and alternatives.

To finish the device according to an embodiment of the present invention, the method forms sidewall spacers **501** from the second protective layer, as illustrated by FIG. 5. The sidewall spacers exposes an upper portion **503** of the hard mask, while sealing regions on the edges of the gate layer. In a preferred embodiment, the method removes the hard mask to expose **601** the top surface of the gate structures, as shown in FIG. 6. Such gate structures are substantially free from any silicon germanium and/or silicon carbide bearing impurities. The gate structures are also substantially smooth and damage free. The method forms a silicide layer overlying gate layer and source/drain regions. Preferably, the silicide layer is a nickel bearing layer such as nickel silicide overlying the exposed source/drain regions and upper surface of the patterned gate layer. Other types of silicide layers can also be used. Such silicide layers include titanium silicide, tungsten silicide, nickel silicide, and the like. The method forms an interlayer dielectric layer overlying NMOS and PMOS transistor devices. The method then performs electrical contacts. Other steps include performing a back end processes and other steps, as desired.

The above sequence of steps provides a method according to an embodiment of the present invention. As shown, the method uses a combination of steps including a way of forming a CMOS integrated circuit device. In a preferred embodiment, the method provides a protective layer that is used for protecting a top portion of the gate structure during etching of recessed regions and selectively depositing silicon germanium material and/or silicon carbide material only on exposed surfaces of the recessed source/drain regions. Other alternatives can also be provided where steps are added, one or more steps are removed, or one or more steps are provided in a different sequence without departing from the scope of the claims herein.

It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

What is claimed is:

1. A method for forming a CMOS semiconductor wafer comprising:
 - providing a semiconductor substrate;
 - forming a dielectric layer overlying the semiconductor substrate;
 - forming a gate layer overlying the dielectric layer;
 - patterning the gate layer to form a gate structure including edges;
 - forming a dielectric layer overlying the gate structure to protect the gate structure including the edges, the dielectric layer having a thickness of less than 40 nanometers;
 - etching a source region and a drain region adjacent to the gate structure using the dielectric layer as a protective layer;

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depositing silicon germanium material into the source region and the drain region to fill the etched source region and the etched drain region;

causing a channel region between the source region and the drain region to be strained in compressive mode from at least the silicon germanium material formed in the source region and the drain region;

forming a second protective layer overlying surfaces including the silicon germanium material and an entirety of the gate structure to seal any impurities in the patterned gate layer, wherein the second protective layer is formed after the silicon germanium material is formed in the source region and the drain region; and

performing an anisotropic etching process on the second protective layer to form spacer structures to seal the gate structure, wherein the spacer structures are formed after the silicon germanium material is formed in the source region and the drain region; and

exposing a top surface of the gate structure while sealing the edges of the gate structure using the spacer structures, wherein the exposing occurs after formation of the spacer structures.

2. The method of claim 1 wherein the effective channel region has a length of a width of the gate structure.

3. The method of claim 1 wherein the semiconductor substrate is essential silicon material.

4. The method of claim 1 wherein the silicon germanium material is single crystalline.

5. The method of claim 1 further comprising forming a spacer layer overlying the semiconductor substrate including silicon germanium, gate structure, and edges.

6. The method of claim 5 further comprising anisotropic etching the spacer layer to form sidewall spacers on edges of the gate layer.

7. The method of claim 1 wherein the second protective layer seals phosphorous bearing impurities in the gate layer.

8. The method of claim 1 wherein the depositing of the silicon germanium material is provided using an epitaxial reactor.

9. The method of claim 1 wherein the compressive mode in the PMOS device increases a mobility of holes in the channel region.

10. The method of claim 1 wherein the second protective layer comprises silicon nitride.

11. The method of claim 1 wherein the spacer structures comprise an ONO structure.

12. The method of claim 11 wherein the ONO structure comprises first oxide of about 200 Å, nitride of about 500 to 800 Å, and second oxide of about 900 Å.

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13. The method of claim 1 wherein the second protective layer comprises PECVD oxide.

14. The method of claim 1 wherein the second protective layer comprises TEOS CVD.

15. The method of claim 1 wherein the second protective layer comprises thermal CVD.

16. The method of claim 1 wherein the second protective layer comprises LPCVD.

17. The method of claim 1 wherein the second protective layer comprises ALD nitride.

18. A method for forming a CMOS semiconductor wafer comprising:

- providing a semiconductor substrate;
- forming a dielectric layer overlying the semiconductor substrate;
- forming a gate layer overlying the dielectric layer, the gate layer comprises a plurality of impurities therein;
- patterning the gate layer to form a gate structure including edges;
- forming a dielectric layer overlying the gate structure to protect the gate structure including the edges, the dielectric layer having a thickness of less than 40 nanometers;
- forming first sidewall spacer structures from a portion of the dielectric layer;
- etching a source region and a drain region adjacent to the gate structure using the first sidewall spacer structures;
- depositing silicon germanium material into the source region and the drain region to fill the etched source region and the etched drain region;
- causing a channel region between the source region and the drain region to be strained in compressive mode from at least the silicon germanium material formed in the source region and the drain region;
- forming a second protective layer overlying surfaces including the silicon germanium material and an entirety of the gate structure to seal any impurities in the patterned gate layer, wherein the second protective layer is formed after the silicon germanium material is formed in the source region and the drain region; and
- performing an anisotropic etching process on the second protective layer to form second sidewall spacer structures to seal the gate structure, wherein the second spacer structures are formed after the silicon germanium material is formed in the source region and the drain region; and
- exposing a top surface of the gate structure while sealing the edges of the gate structure using the second sidewall spacer structures, wherein the exposing occurs after formation of the second sidewall spacer structures.

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