

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd. And Apple Inc.,

Petitioners

v.

Marlin Semiconductor Ltd.

Patent Owner

Patent No. 7,745,847 B2
Filing Date: August 9, 2007
Issue Date: June 29, 2010

Title: METAL OXIDE SEMICONDUCTOR TRANSISTOR

Inter Partes Review No. IPR2025-00847

**DECLARATION OF PROF. EUGENE FITZGERALD, PH.D.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 7,745,847**

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Declaration of Prof. Eugene Fitzgerald, Ph.D.

I, Prof. Eugene Fitzgerald, Ph.D., declare as follows:

I. Introduction

1. My name is Eugene Fitzgerald. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in connection with a petition for *inter partes* review of U.S. Patent No. 7,745,847 (“’847 Patent”), which I have been told is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-11 of the ’847 Patent (“Challenged Claims”).

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the basis for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the ’847 Patent is unpatentable for at least the reasons I discuss below.

II. Background and Qualifications

A. Education and Career

5. I have summarized in this section my educational background, career history, and other relevant qualifications.

6. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing, and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of transistors.

7. I received a B.S. in Materials Science and Engineering from the Massachusetts Institute of Technology (“MIT”) in 1985, a M.S. in Materials Science and Engineering from Cornell University in 1987, and a Ph.D. in Materials Science and Engineering from Cornell University in 1989.

8. From 1988 to 1994, I worked as a research scientist at AT&T Bell Laboratories in Murray Hill, N.J., in the Materials Science and Engineering Department. While at AT&T Bell Laboratories, I conducted fundamental research in semiconductor materials and devices, specifically the use epitaxial layers in field effect transistors (“FETs”).

9. From 1994 to 2000, I was an Associate Professor at MIT. From 2000 to the present, I have been a Professor of Materials Science at MIT, in the Materials Science and Engineering Department. I am currently the Merton C. Flemings-

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Singapore-MIT-Alliance Professor of Materials Engineering and the Lead Principal Investigator of MIT SMART LEES (Singapore- MIT Alliance for Research and Technology, MIT's Research Center in Singapore, Low Energy Electronic Systems), where I managed the ninety- million-dollar research program (2011-2025).

10. Of specific relevance to this case, my research involves studying semiconductor structures with strained materials, and specifically the use of epitaxially grown germanium alloys—such as silicon germanium (“SiGe”)—to strain semiconductor devices. The use of epitaxial SiGe to form source/drain regions that strain the channel in Metal-Oxide-Semiconductor (“MOS”) transistors, was technology developed by at least the year 2000 (about seven years before the earliest claimed priority date for the '847 Patent).

11. Early on my research group studied (and we continue to work on) epitaxy growth of SiGe on silicon substrates. (See, for example, Z. Cheng, E.A. Fitzgerald & D.A. Antoniadis, “SiGe-On-Insulator (SGOI) Technology and MOSFET Fabrication,” Advanced Materials for Micro- and Nano-Systems (AMMNS) (2002); O. Kwon, J.J. Boeckl, M.L. Lee, A.J. Pitera, E.A. Fitzgerald & S.A. Ringel, “Monolithic Integration of AlGaInP Laser Diodes on SiGe/Si Substrates By Molecular Beam Epitaxy,” Journal of Applied Physics, vol. 100, no. 1 (2006); J. Wang, C. Heidelberger, E.A. Fitzgerald & N.J. Quitoriano, “Liquid Phase Epitaxy

SiGe Films on a CVD-Grown SiGe/Si (001) Graded Film,” Journal of Crystal Growth, vol. 535, 125541 (2020).)

12. I have received numerous honors and awards for my work. For example, I was a co-recipient of the Institute of Electrical and Electronics Engineers (“IEEE”) 2011 Andrew S. Grove Award for outstanding contributions to solid state devices and technology including “seminal contributions to the demonstration of Si/Ge lattice mismatch strain engineering for enhanced carrier transport properties in MOSFET devices,” the IEEE 2004 EDS George Smith Award for Best Paper for a paper I co-authored entitled “Fully Depleted Strained-SOI n- and p- MOSFETs on Bonded SGOI Substrates and Study of the SiGe/BOX Interface,” and the TMS 1994 Robert Lansing Hardy Medal Award for exceptional promise of a successful career in the field of metallurgy and materials science.

13. I am the founder, co-founder, or a founding team member of the following companies and organizations: AmberWave Systems Corporation (a company focused on strained silicon semiconductor technology); Contour Semiconductor (a company focused on a unique semiconductor fabrication process for non-volatile memory); 4Power LLC (manufacturer of high efficiency, low cost solar cells using III-V thin films on silicon substrates); Paradigm Research LLC (commercializing true monolithic III-V/Si CMOS integrated circuits); The Innovation Interface (a not-for-profit organization that trains future innovators

through university-corporate innovation projects); The Water Initiative (creating customized point-of-drinking water solutions and scaling those solutions through micro-entrepreneurs, developers and government entities), and New Silicon Corporation Pte. Ltd. (III-V+CMOS integrated circuit company).

14. A full list of my research and professional experience, my expert witness or consultant experience, and other activities and awards is further detailed in my curriculum vitae, which I understand is being included as Exhibit 1004.

15. As a co-founder, professor, and inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

B. Publications

16. A list of the publications that I have authored and patents I have been awarded during my technical career can be found in my Google Scholar Profile <https://scholar.google.com/citations?hl=en&user=YsZ6EjkAAAAJ>.

17. I am a named inventor on over 100 granted United States patents and have authored over 700 peer-reviewed academic journal publications. I have coauthored several publications on strained silicon transistors. For example, I co-authored the book *Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy*, published in 2018 by CRC press. I also have patents specifically discussing SiGe/silicon strain technology, gate sidewall spacer formation, and lightly doped drains, metal gate

electrodes, and MOSFET transistors, all of which are relevant technologies in this case. Some examples of my relevant patents and publications that predate the '847

Patent are:

- Y.J. Mii, Y.H. Xie, E.A. Fitzgerald, D. Monroe, F.A. Thiel, B.E. Weir & L.C. Feldman, "Extremely High Electron Mobility in Si/Ge_xSi_{1-x} Structures Grown by Molecular Beam Epitaxy," Applied Physics Letters, vol. 59, no. 13, pp. 1611-13 (1991).
- M.L. Lee & E.A. Fitzgerald, "Optimized Strained Si/Strained Ge Dual-Channel Heterostructures for High Mobility P-and N-MOSFETs," Technical Digest of the 2003 IEEE International Electron Devices Meeting ("IEDM"), pp. 18.1.1-4 (2003).
- M.L. Lee, E.A. Fitzgerald, M.T. Bulsara, M.T. Currie & A. Lochtefeld, "Strained Si, SiGe, and Ge Channels for High-Mobility Metal-Oxide-Semiconductor Field-Effect Transistors," Journal of Applied Physics, vol. 97, no. 1 (2005).
- E.A. Fitzgerald, R. Hammond & M. Currie, "Gate Technology for Strained Surface Channel and Strained Buried Channel MOSFET Devices," U.S. Patent No. 6,583,015 (filed Aug. 6, 2001).
- T.A. Langdo, M.T. Currie, R. Hammond, A.J. Lochtefeld & E.A. Fitzgerald, "Strained-Semiconductor-On-Insulator Device Structures," U.S. Patent No. 6,995,430 (filed June 6, 2003).

C. Compensation

18. I am being compensated for services provided in this matter at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of my work in this matter. My compensation is not contingent upon the results of my study or analysis, the substance of my opinions, or the outcome of any

proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '847 Patent.

III. Materials Reviewed

19. In forming my opinions regarding the '847 Patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the page number of the original reference, not the stamped exhibit page numbers.

IV. Legal Standards

20. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '847 Patent are patentable, I have been told that I am obliged to follow existing law.

A. Anticipation

21. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

22. I have been told that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

23. I have been told that under 35 U.S.C. §103(a), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in §102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I have been told that, in inter partes review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

24. When considering the issues of obviousness, I have been told that I am to do the following:

- a. Determine the scope and content of the prior art;
- b. Ascertain the differences between the prior art and the claims at issue;
- c. Resolve the level of ordinary skill in the pertinent art; and

d. Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

25. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have been asked to assume is just before the earliest claimed priority date of the '847 Patent (i.e., August 9, 2007).

26. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '847 Patent).

27. I have been told that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

28. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another

reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

29. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

30. I have been told the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

31. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing

so, that variation was likely to have been obvious. I have been told that in many fields, there may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

32. I have been told that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine them. But I also understand that any “teaching, suggestion, or motivation” present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told this “teaching, suggestion, or motivation” test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

33. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

34. I have been told that when there is a known technique to address a known problem using prior art elements according to their established functions, then a person of ordinary skill in the art would have had a motivation to combine.

35. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. Level of Ordinary Skill in the Art

36. I have been informed that a person of ordinary skill in the art (“person of ordinary skill in the art”) is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

37. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

38. In my opinion, a person having ordinary skill in the art in reference to the '847 Patent would have had a master's degree in electrical engineering, physics,

chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal education.

39. I have not analyzed the priority date of the '847 Patent, but I note that the earliest claim of priority listed on the face of the '847 Patent is its filing date, August 9, 2007. Because all the prior art discussed in this declaration predates August 9, 2007, I have been asked for simplicity to treat **August 9, 2007**, as the priority date for the '847 Patent. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

VI. Technological Background

40. The '847 Patent describes Metal Oxide Semiconductor ("MOS") transistors with epitaxial source/drain regions to provide mechanical stress and boost transistor performance. ('847 Patent at Title, 1:7-10.)

41. For my analysis of the technical background and the knowledge of the person of ordinary skill in the art, I was asked to consider the filing date of the '847 Patent (i.e., **August 9, 2007**) as the patent's priority date. As I further discuss below, in my opinion, the elements described and claimed in the '847 Patent were well

known before this date—in fact, already commonplace, even in high-volume commercial production.

42. Further, to the extent the Patent Owner claims an earlier priority date (e.g., a priority in 2006), such change in priority would not materially change my analysis of the technical background or the knowledge of the person of ordinary skill in the art because all the elements in the '847 Patent were well known before then as well.

43. The '847 Patent generally relates to a technology that is known in the field as “strained silicon channel MOS transistor[s]”—i.e., MOS transistors using SiGe source/drain stressors. ('847 Patent, 1:7-10.) That technology was known and had been developed at least since the early 2000s. For example, as I explain below in more detail, MOS transistors using strained silicon SiGe source/drain stressors was widespread by the mid-2000s. In fact, two generations of high-volume commercial devices (i.e., 90nm devices, released 2003, and 65nm devices, released 2005) used strained-silicon channel MOS transistors.

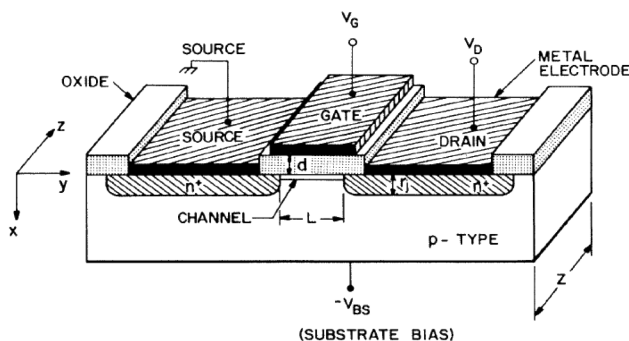
44. During the timeframe relevant to the '847 Patent, the person of ordinary skill in the art would have been familiar with the background information I describe below in subsections A through C.

A. MOS Transistors

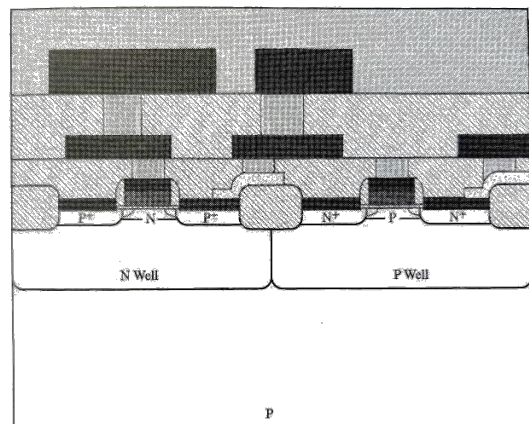
45. By the priority of the '847 Patent, MOS transistors had been known for decades. Introduced in 1960s, MOS transistors had been a cornerstone of modern electronics for many decades. (Size at 431.)

46. MOS transistors, and specifically MOS field-effect transistors (“MOSFETs”) like the ones at issue here, include four main regions: *source* and *drain* regions allow for current input and output, and a *gate* overlies a *channel* region located between the source/drain regions. (Size at 433-34, Fig. 3.)

47. The gate comprises a gate electrode (which is normally made of a metal or doped polysilicon) and a thin gate dielectric layer (which is an electrically insulating film) that separates the gate from the semiconductor channel underneath it, as the figures below illustrate. (Size at 433-34, Fig. 3.) These figures show typical MOSFET arrangements as described in textbooks. (Size at 433-34, Fig. 3; Plummer at 71-90, Figs. 1-11, 2-2, 2-22 to 2-44.)



Size, Fig. 3



Plummer, Fig. 1-11

48. The *source* and *drain* regions are generally *doped* with impurities that modify the conductivity or resistivity of the region. (Plummer at 60-63.) More specifically, source/drain regions are usually doped with *p-type* or *n-type* impurities, and channel regions are doped with impurities of the opposite type. (Sze at 433-34; Plummer at 76-82.)

49. Generally, the terms *PMOS* and *NMOS* refer to MOSFETs with p-type or n-type source/drain regions, respectively. (Plummer at 12-13, 50-51, Figs. 1-11, 2-2.) Most typical devices are *CMOS* (“Complementary MOS”), which include both PMOS and NMOS. (Plummer at Fig. 1-11.)

50. Applying voltage to the gate electrode controls the channel underneath to connect or disconnect the source and drain. (Sze at 433-34, 438, Figs. 3, 6.) In an enhancement-mode transistor (which is normally “off”), applying a voltage to the gate can induce a conducting channel between the source and drain (what is known as turning “on” the transistor). On the other hand, applying no voltage to the gate destroys the conducting channel (what is known as turning “off” the transistor). In a depletion-mode transistor (which is normally “on”), the situation is reversed.

B. Strained Channel Technology

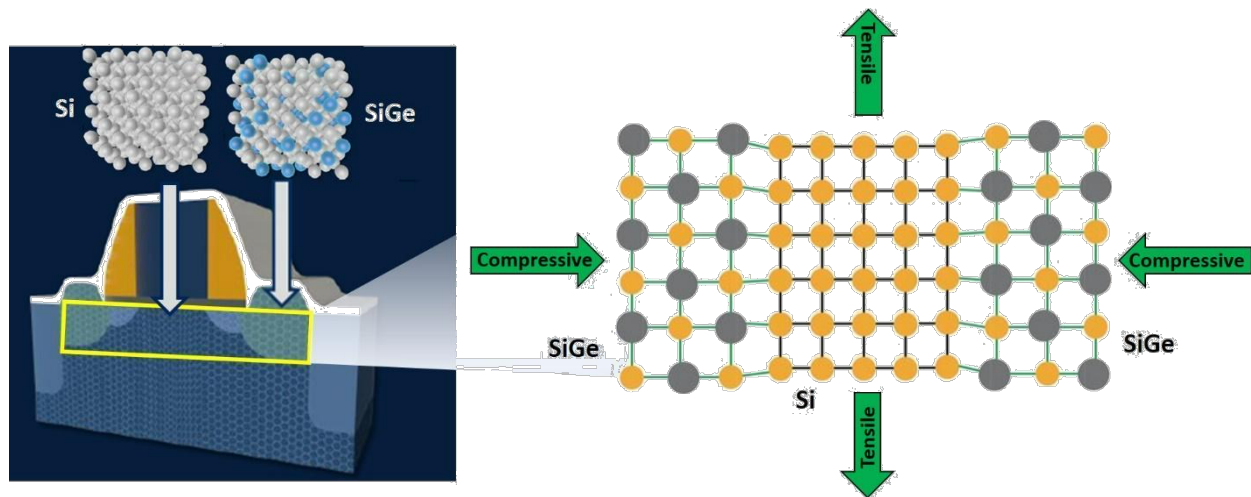
51. Strained-silicon channel MOSFETs with SiGe source/drain stressors predate the '847 Patent, finding use in even high-volume commercial devices. (See Thompson at 1790-71; Bai at 657-58.) Manufacturers found that using stressor

films or epitaxy layers in the source/drains in MOSFETs could increase the channel mobility of charge carriers (electrons in NMOS and holes in PMOS). (James at 2.) Stressing the channel modifies the band structure of the silicon and reduces phonon scattering, which allows the charge carriers to move more easily through the channel, enhancing the transistor's switching speed and drive current. (James at 2; Thompson at 1790-96; Murthy ¶[0005].) Manufacturers understood that using compressive source/drain stressors improved carrier mobility in PMOS (hole mobility), whereas tensile stress improved carrier mobility in NMOS (electron mobility). (James at 2; Thompson at 1790-96; Murthy ¶[0005].)

52. The first high-volume strained-channel MOSFETs included epitaxial SiGe layers in the source/drain regions. By 2005, using SiGe source/drain stressors to compress high-volume manufactured PMOS devices was common, and reverse-engineering reports on such commercial devices had showed that SiGe had increased PMOS "hole mobility by as much as 50%." (James at 2.)

53. SiGe stressor layers strain the channel because germanium atoms are *larger* than silicon atoms, leading to a germanium lattice constant (i.e., inter-atomic spacing in the crystal) that is roughly 4% larger than in silicon. Thus, adding SiGe source/drain regions near the silicon channel *compressively* strains the silicon channel region along the current flow direction (left-to-right in the graphic below). (James at 2; Thompson at 1790-96; Murthy ¶¶[0046]-[0047]; Bohr ¶[0024], FIG. 4.)

The graphic below exemplifies how SiGe source/drain stressors compress a silicon channel. The Ge atoms (shown in gray in the graphic on the right) are larger than the silicon atoms (shown in yellow in the graphic on the right). This increases the inter-atomic spacing of the lattice, which compresses the silicon channel.



54. Ensuring adequate strain transfer commonly involved growing epitaxial source/drain regions that extended above the substrate (protruding over the silicon surface) to provide sufficient SiGe to effectively compress the silicon channel. (See Ghani at 978, Figs. 1-4; Wang906 ¶¶[0030]-[0032], FIG. 9; Bohr at FIGS. 4-7; Kavalieros at Abstract, ¶[0025], ¶[0043], FIGS. 5, 13.) These “raised” SiGe regions also improve PMOS performance by reducing contact resistance in the source and drain regions. (See James at 2.)

55. Compressive strain does not benefit NMOS devices because the charge carriers in NMOS devices are electrons, not holes as in PMOS devices. Electron carrier mobility benefits from *tensile* strain, not compressive strain. In the first high-

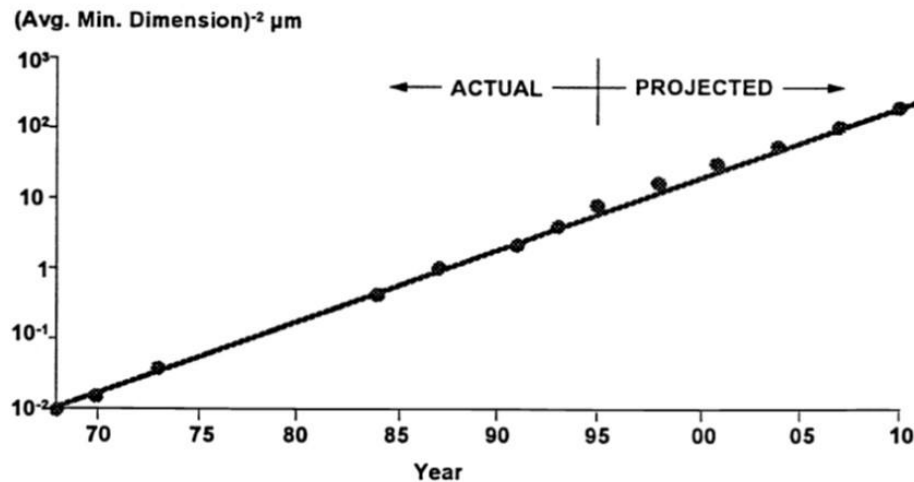
volume, strain-enhanced commercial NMOS devices, manufacturers used tensile-strained silicon nitride layers to impart tensile strain to the NMOS channel, thereby enhancing electron mobility. (James at 4.) A further evolution of strained-channel NMOS devices, to induce more tensile strain, involved using epitaxial source/drain stressors (similar to PMOS devices). To achieve tensile stress, the material in the source/drain requires a smaller atom than silicon (unlike the larger atom Ge used for compression). For example, by growing silicon carbide (SiC) in the source/drain regions, carbon—being a *smaller* than silicon—tends to create a smaller lattice spacing than silicon, inducing a tensile strain to the silicon channel region of an NMOS device. (Murthy ¶¶[0005], ¶¶[0048], ¶¶[0072]; Bohr ¶¶[0045].)

56. By the priority date of the '847 Patent (August 9, 2007), epitaxial SiGe source/drain stressors already had been used in two generations of high-volume commercial MOSFET devices. (Thompson at 1790-91 (Intel 90nm devices); Bai at 657-58 (Intel 65nm devices).)

C. Gate Sidewall Spacers

57. Since the invention of MOS transistors, there has always been a drive to shrink individual transistors and increase their density. This trend is known as device “scaling.” (Chang at xviii-xxi; Wolf2 at 1 at Fig. 1-1(b).) Device scaling was such a well-established trend that it followed a predictable cadence, known as “Moore’s Law.” (See Moore at 1-16; Wolf2 at 1.) Although not technically a “law,”

Gordon Moore's prediction that the number of transistors in a single integrated circuit would double every two years held true for many decades. The figure below shows one aspect of Moore's law—the rate at which the average minimum device dimension shrank. (Moore at Fig. 14.)



Moore at Fig. 14

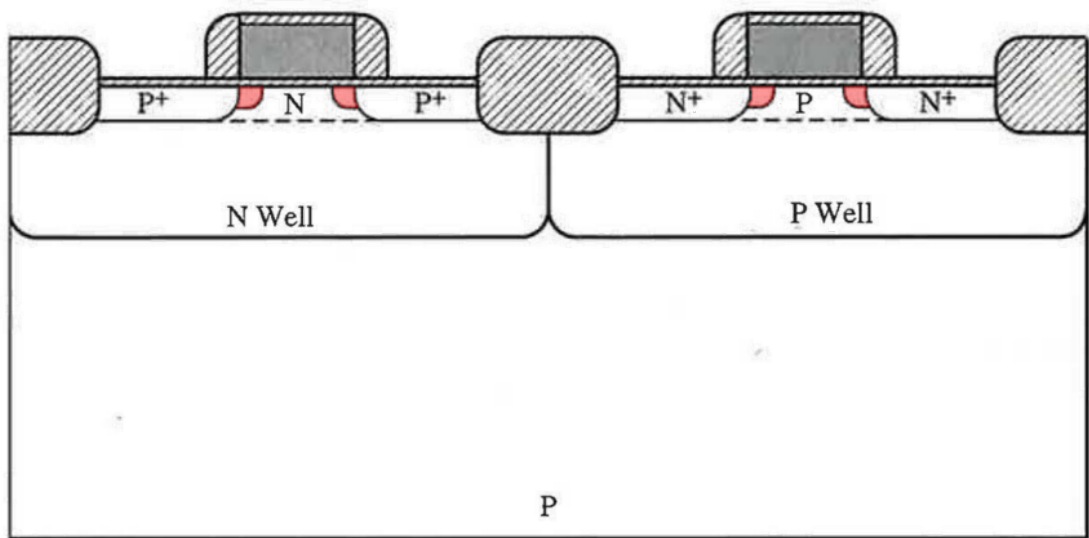
58. When shrinking a MOSFET, the channel must become shorter, which brings the source and drain regions closer to one other. (Wolf3 at 205, 233-34; Wolf2 at 338.) This also brings the source/drain regions closer to the channel/gate regions. As this occurs, the electric field from the drain may eventually “penetrate into the source region” and cause unwanted increases in current. (Wolf2 at 341.) This phenomenon is called *punchthrough*, which is an example of what are known as short-channel effects (“SCEs”). (Wolf3 at 233; Sze at 433; Quirk at 211; Plummer at 77-78.)

59. Researchers and engineers discovered punchthrough and other SCEs as early as the 1970s, and they developed a variety of techniques to mitigate those effects. (Plummer at 77-78.) By the 1990s, one very common technique to mitigate SCEs in high-volume commercial semiconductor fabrication was to use lightly doped drain (“LDD”) regions.¹ (Plummer at 76-82; Quirk at 211-13.) Because source and drain regions generate an electric field that can affect the channel of the transistors, it was found that introducing LDD regions alleviated punchthrough by positioning more heavily doped source/drain regions (and their larger electric fields) further away from the channel, thereby controlling electric fields near the channel and improving the transistor’s performance. (Plummer at 77-78; Quirk at 211-13.)

60. As early as 1980s, researchers found they could better control electric fields near the channel, improve transistor performance, and minimize SCEs by controlling the source/drain doping. The LDD approach, illustrated below, uses a sequence of doping implantations that “carefully tailor the doping profile near the drain junction (and the source junction) in order to minimize short channel effects.” (Plummer at 78.) For example, as Plummer shows in Fig. 2-33 (reproduced below),

¹ Although the last “D” in “LDD” stands for “drain,” a person of ordinary skill in the art would have known that LDD regions were almost always formed in both source and drain regions. Accordingly, LDD regions may be more accurately be understood as lightly doped source and drain regions.

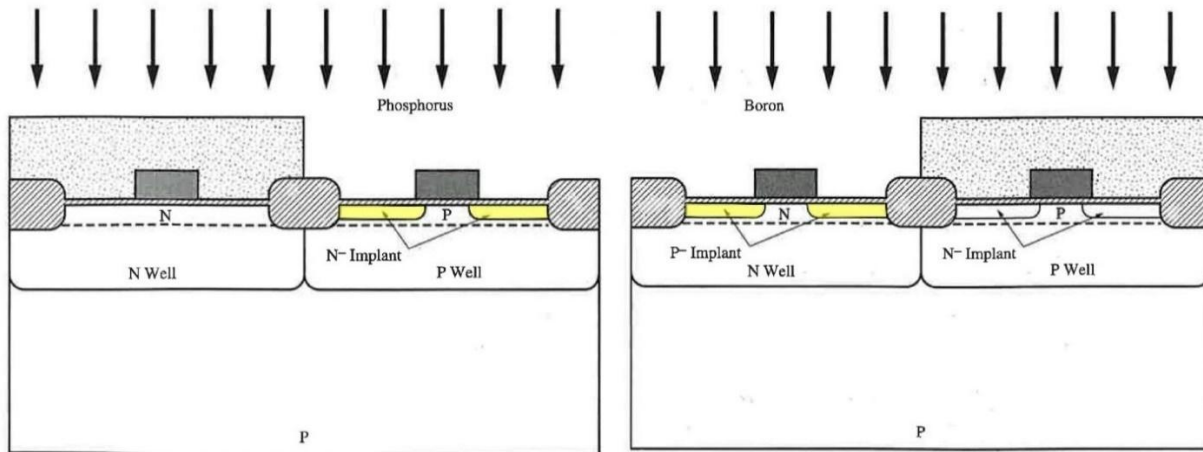
LDD regions (annotated in red) are introduced close to the channel to facilitate control of electric fields there. (Plummer at 76-78.)



Plummer at Fig. 2-33^[2]

61. Plummer's Figs. 2-27 through 2-32 illustrate a typical method of forming and the LDD regions by using "sidewall spacers." (See Plummer at 76-82.) Impurities like boron or phosphorus are used to create lightly doped implant regions on the sides of the gate (the rectangle between the yellow regions). (See Plummer at 76-77.) As shown below, ion implantation forms lightly doped source/drain regions (yellow) using the gate as a mask to block the ions from the channel region.

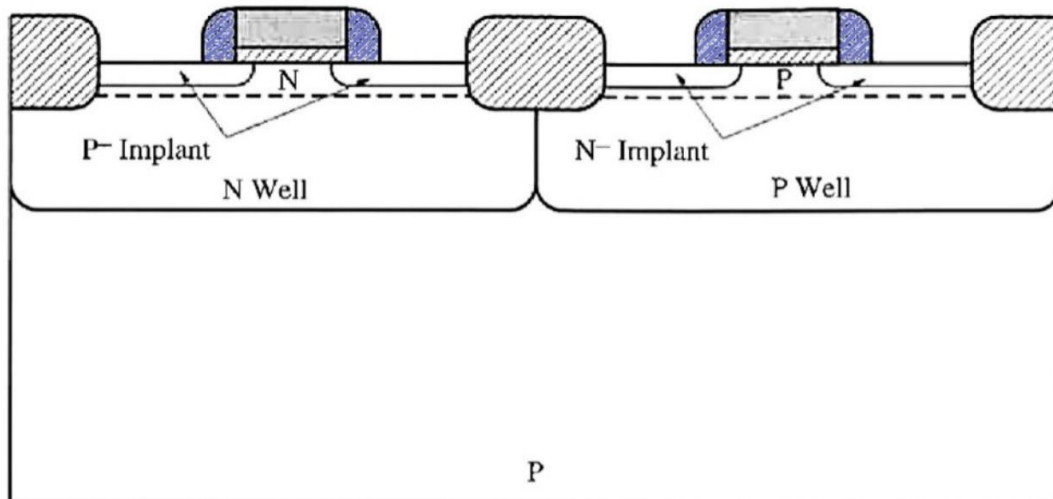
² All color annotations from here through the end of this declaration have been added unless I note otherwise.



Plummer at Fig. 2-27

Plummer at Fig. 2-28

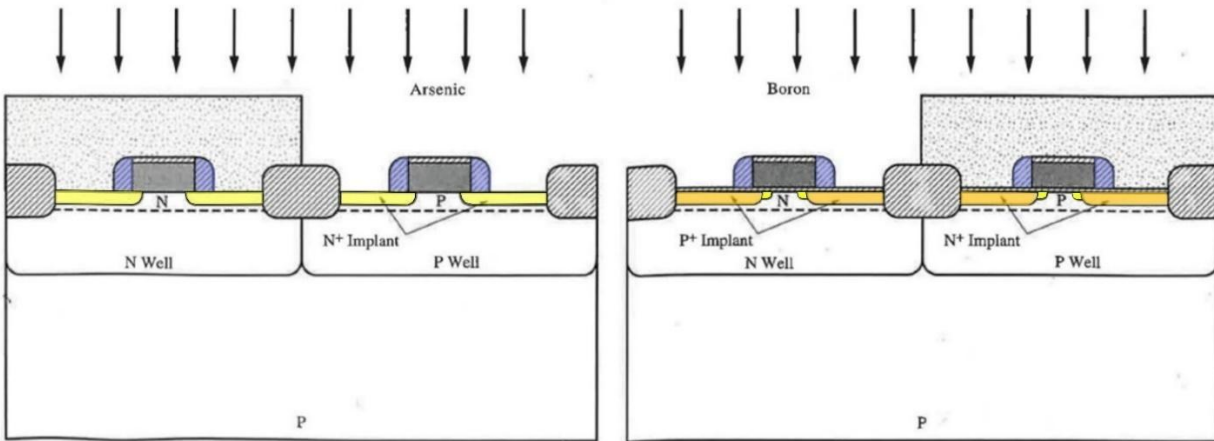
62. Then the “sidewall spacers” (purple) are formed on gate edges. (See Plummer at 78-80.)



Plummer at Fig. 2-30

63. As shown below, such sidewall spacers act as masks near the edge of the channel during subsequent ion implantation to more heavily dope part of the substrate. The sidewall spacers protect the LDD regions (yellow) and help position the more heavily doped regions (orange) further away from the channel edge.

(Plummer at 80-82 at Figs. 2-31 to 2-33; Quirk at 213 at Fig. 9.17; Wolf3 at 595-96 at Fig. 9-31(f).) This reduces the electric field near the channel to mitigate SCEs.



Plummer at Fig. 2-31

Plummer at Fig. 2-32

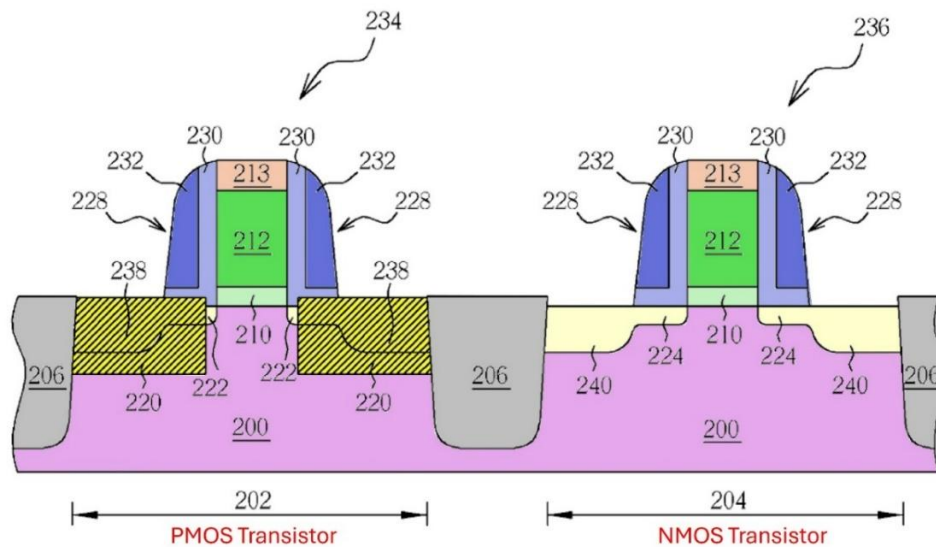
64. This way of forming LDD regions, gate sidewall spacers, and source/drain regions was very well-known by the priority date of the '847 Patent. For example, Plummer published his book in 2000. Even back then, this process was a routine part of undergraduate courses on semiconductor design and manufacturing. By the time of the '847 Patent, the use of gate sidewall spacers to form LDD regions in this way had been fundamental in semiconductor manufacturing for more than a decade. Sidewall spacers, including those extending onto epitaxial source/drain regions, were common and a routine device element, as illustrated by the references I analyze in this declaration below.

VII. THE '847 PATENT

65. To perform my analysis, I reviewed the '847 Patent and its prosecution history. Below, I provide a brief overview of both.

A. Overview

66. The '847 patent describes a "MOS transistor structure." ('847 Patent at 2:21-29.) The embodiment in Fig. 5 below shows the different elements of the MOS transistor structure described in the patent. The table beneath Fig. 5 summarizes the elements depicted in Fig. 5. (See '847 Patent at 2:50-4:35.)



'847 Patent, Fig. 5 (annotated)

PMOS

220: Epitaxial layer
222: First ion lightly doped region
234: First conductive transistor
238: First ion source/drain regions

NMOS

224: Second ion lightly doped region
236: Second conductive transistor
240: Second ion source/drain regions

NMOS & PMOS

200: Semiconductor substrate	213: Cap layer
206: Shallow trench isolation (STI)	228: Spacers
210: Dielectric layer	230: Oxide liner
212: Conductive layer	232: Nitride spacer

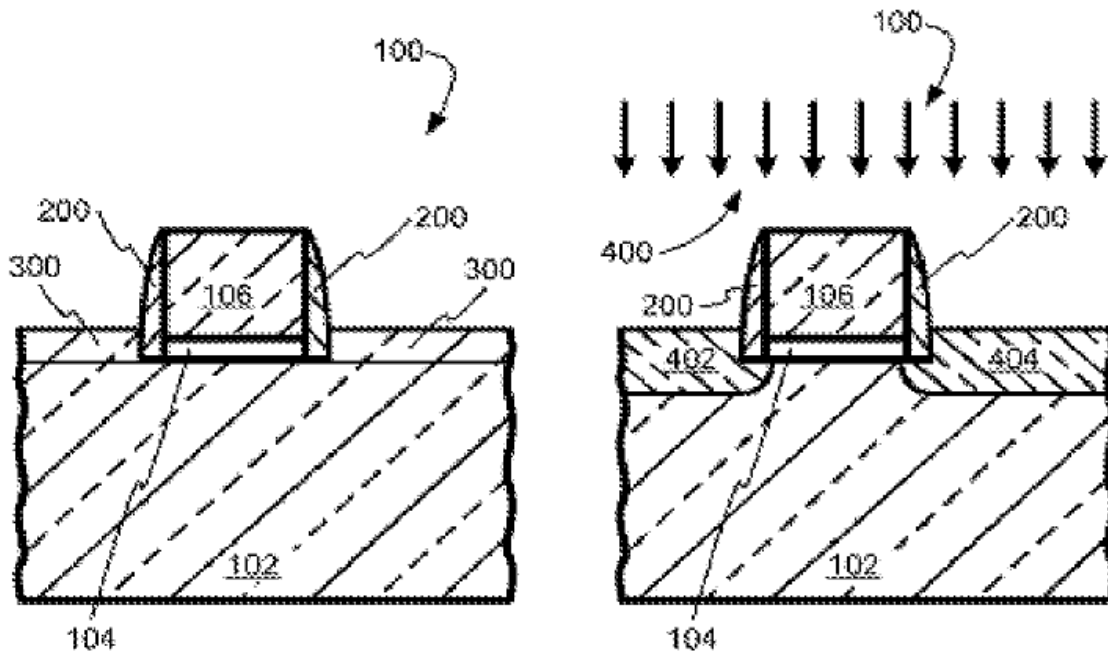
67. As Fig. 5 shows above, this exemplary MOS structure described in the '847 Patent includes “a first conductive transistor 234” (e.g., PMOS) formed “in the first conductive transistor area 202” and “a second conductive transistor 236” (e.g., NMOS) formed “in the second conductive transistor area 204.” ('847 Patent at 4:7-15.) Each transistor also comprises a gate that includes a dielectric layer 210, a conductive layer 212, and a cap layer 213. ('847 Patent at 3:3-6.) And each gate is flanked by a pair of sidewall spacers 228 comprising “an oxide liner 230 and a nitride spacer 232.” ('847 Patent at 3:57-61.)

68. As Fig. 5 shows, the PMOS device additionally includes two epitaxial layers 220 formed “next to the relative sides of the gates.” ('847 Patent at 2:23-25, 3:33-37.) Those epitaxial layers “may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.” ('847 Patent at 3:35-38.) According to the '847 Patent, “the characteristic of the present invention is to form the epitaxial layer before forming the spacer, thus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer.” ('847 Patent at 6:64-67.)

B. Prosecution History

69. Based on my review of the prosecution file history for the '847 Patent, I understand that the Examiner first rejected the claims as anticipated or rendered obvious by the prior art, depicted in part below. (Prosecution History at 71-75.) In

response, the Applicant amended the independent claim by adding the following underlined language: “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate.” (Prosecution History at 88-91.)



Prosecution History at 128

70. The Examiner again rejected again the claims based on the prior art, shown in part above. (Prosecution History at 99-108.) In response, the Applicant amended the independent claim again, this time adding the following underlined language: “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.” (Prosecution History at 132-34.)

71. The Applicant argued that “the spacer 200 could not have been formed on the epitaxial layers 300” because “the epitaxial layers 300 are formed on surface of the substrate 102 after the formation of the spacer 200.” (Prosecution History at 128.) The Applicant also argued that the prior art did not satisfy newly added “contact surface” requirement because “the spacer 200 is not extended on a portion of the epitaxial layers 300.” (Prosecution History at 129.)

72. After this, the Examiner issued a notice of allowability. (Prosecution History at 142-45.) In it, the Examiner stated:

None of the prior art teaches a MOS transistor structure, comprising a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.

(Prosecution History at 143-44 (underlining in original).) But the Examiner appears to have overlooked the prior art I discuss below. Such an arrangement was actually quite common before the '847 Patent.

C. Claim Construction

73. I have been told that claim terms are construed with the meanings they would have to a person of ordinary skill in the art in the context of the patent and prosecution history. Except for claim 7 of the '847 Patent, that is how I have applied the claim language.

74. For Claim 7 I tried to apply the meaning of the claim as understood by the person of ordinary skill, but I was unable because I find that claim 7 is confusing as written. Claim 7 recites: “The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.” Therefore, claim 7 requires the “offset spacer” to be part of the “spacer.” But claim 7 also requires the “offset spacer” to be located between the “spacer” and the gate. Those two requirements seem to conflict.

75. Instead of applying the literal language of claim 7 as written, I was asked to analyze claim 7 by analogy to the examples in the '847 Patent. Specifically, I was asked to assume claim 7 may be satisfied so long as one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the claimed “gate.”

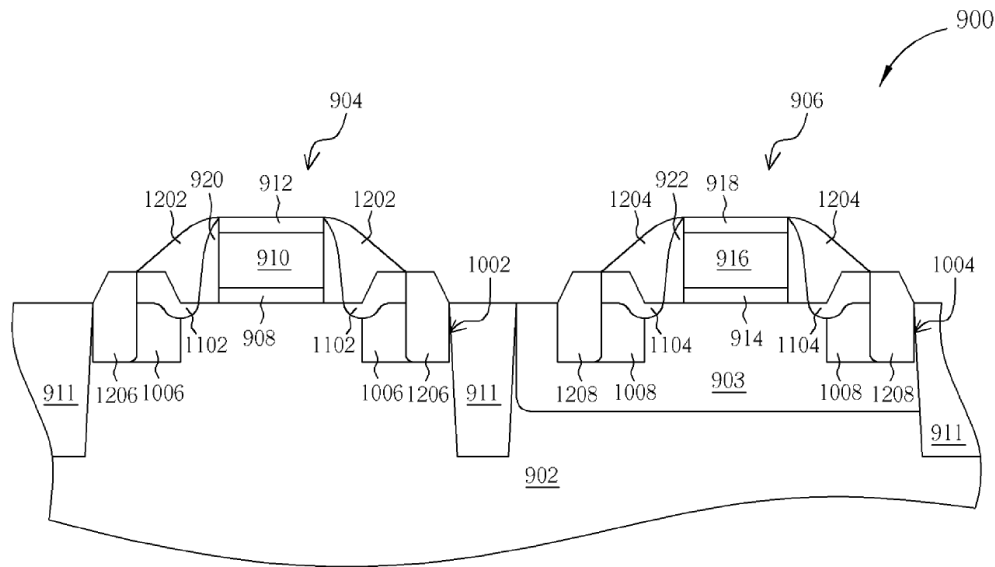
76. If the Patent Owner offers constructions of any terms, I reserve the right to address those constructions at an appropriate time in the future.

VIII. REVIEW OF THE PRIOR ART

A. The Lan Reference

77. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Lan qualifies as prior art to the '847 Patent. I note, however, that Lan seems to have been filed on May 11, 2006. (Lan at cover page.)

78. Lan is in the same field of endeavor as the '847 Patent (MOSFETs and their fabrication), and Lan is reasonably pertinent to a problem the '847 Patent purports to address (fabricating strained silicon channel MOS transistors). (See Lan at Title, 1:53-63; '847 Patent at 1:6-10, 1:49-52.) Applying the standard for “analogous art” stated in the final paragraph of Section IV.B, it is my opinion that a person of ordinary skill in the art would have considered Lan to be analogous art to the '847 Patent.



Lan, Fig. 12

79. Lan describes “a method of manufacturing a metal oxide semiconductor transistor.” (Lan at 1:9-15.) Lan’s transistors include a gate that (as Lan’s Fig. 12 shows above) comprises gate insulating layers 908 and 914, doped polysilicon layers 910 and 916, and cap layers 912 and 918. (Lan at 4:54-58.)

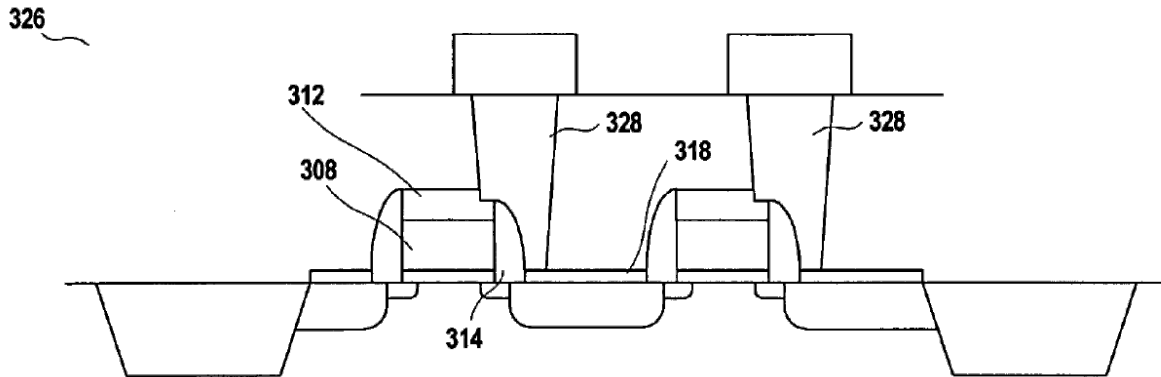
80. Lan's disclosed process also "forms source/drain extension areas before forming epitaxial layers." (Lan at 1:9-15.) After forming the source/drain extensions, Lan uses disposable spacers to delimit substrate recesses 1002 and 1004 on either side of the gate. (Lan at 4:59-5:3, Figs. 10-12.) A selective epitaxial growth ("SEG") process then forms raised source/drain regions in substrate recesses 1002 and 1004. (See Lan at 4:59-5:3, Figs. 10-12.) As Lan's Fig. 12 illustrates above, after stripping the "disposable spacer[s]," Lan teaches to form "main spacers" 1202 and 1204 that extend onto the raised epitaxial source/drain regions. (Lan at 5:4-5, 5:22-24, Figs. 11-12.)

B. The Liaw Reference

81. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Liaw qualifies as prior art to the '847 Patent. I note, however, that Liaw seems to have been filed on August 27, 2004, and that it seems to have issued as a patent on April 11, 2006. (Liaw at cover page.)

82. Liaw is in the same field as the '847 Patent (MOSFETs and their fabrication), and Liaw is reasonably pertinent to a problem the '847 Patent purports to address (fabricating silicon MOS transistors). (See Liaw, Abstract, 1:6-9, 1:58-2:2; '847 Patent at 3:3-11.) Applying the standard for "analogous art" stated in the final paragraph of Section IV.B, it is my opinion that a person of ordinary skill

in the art would have considered Liaw to be analogous art to the '847 Patent. '847 Patent.



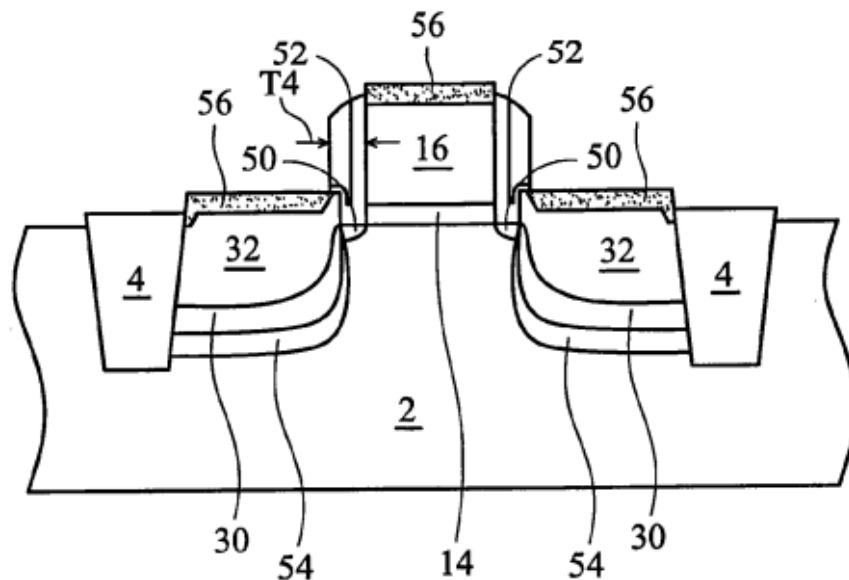
Liaw, FIG. 3B

83. As FIG. 3B shows above, Liaw describes “a metal oxide semiconductor (MOS) device with a metal gate and a cap layer.” (Liaw at 1:5-9.) Liaw’s devices include gates with a metal gate conductor (e.g., gate conductor 308) and an insulating cap layer (e.g., cap layer 312). (Liaw at 4:63-66, 3:50-4:31, FIG. 3B.) According to Liaw, “by keeping the cap layer 312 atop the metal gate conductor 308, the MOS device 300 is able to tolerate a slight misalignment of the conductive plug 322.” (Liaw at 5:5-8.) This is possible because, even when conductive plugs 328 are misaligned to the source/drain regions as shown above, “[e]lectrical contact is, as intended, only made to the salicide source/drain contact 318, since the insulating cap layer 312 insulates the metal gate conductor 308 from being exposed.” (Liaw at 5:18-22.)

C. The Wang407 Reference

84. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Wang407 qualifies as prior art to the '847 Patent. I note, however, that Wang407 seems to have been filed on September 6, 2006. (Wang407 at cover page.)

85. Wang407 is in the same field of endeavor as the '847 Patent (MOSFETs and MOSFET fabrication), and Wang407 is reasonably pertinent to a problem the '847 Patent purports to address (fabricating strained silicon channel MOS transistors). (See Wang407 at Title, 1:65-2:2; '847 Patent at 1:6-10, 1:49-52.) Applying the standard for “analogous art” stated in the final paragraph of Section IV.B, it is my opinion that a person of ordinary skill in the art would have considered Wang407 to be analogous art to the '847 Patent.



Wang407, Fig. 9

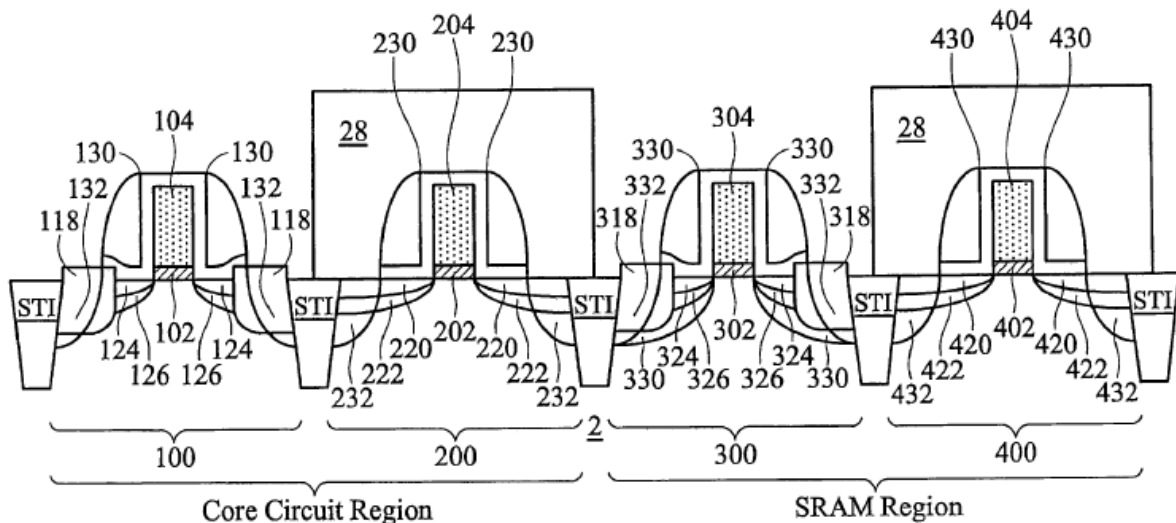
86. Like the '847 Patent, Wang407 describes a “method for forming stressors in metal-oxide-semiconductor (MOS) devices.” (Wang407 at 3:15-16.) And, like the '847 Patent, Wang407 recognized that to “further enhance the performance of MOS devices, stress may be introduced in the channel region of a MOS transistor to improve carrier mobility.” (Wang407 at 1:28-30.) With the goal of improving carrier mobility, Wang407 describes NMOS and PMOS transistors that include raised epitaxial “stressors” adjacent to the gate to strain the channel. (Wang407 at 4:4-21 & Figs. 1-9 (PMOS), 5:58-6:4 & Fig. 11 (NMOS).)

87. As Fig. 9 shows above, the Wang407 device structure includes multi-layered sidewall spacers 52, as well as “a semiconductor substrate [2], a gate stack [including gate dielectric 14 and gate electrode 16] on the semiconductor substrate, and a stressor [32] adjacent the gate stack and having at least a portion in the semiconductor substrate.” (Wang407 at Abstract, 4:61-67, Fig. 9.)

D. The Wang753 Reference

88. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Wang753 qualifies as prior art to the '847 Patent. I note, however, that Wang753 seems to have been filed on April 10, 2006. (Wang753 at cover page.)

89. Wang753 is in the same field as the '847 Patent (MOSFETs and their fabrication), and Wang753 is reasonably pertinent to a problem the '847 Patent purports to address (fabricating strained silicon channel MOS transistors). (See Wang753 at Title, Abstract, 1:6-9, 2:29-35; '847 Patent at 1:6-10, 1:49-52.) Applying the standard for “analogous art” stated in the final paragraph of Section IV.B, it is my opinion that a person of ordinary skill in the art would have considered Wang753 to be analogous art to the '847 Patent.



Wang753, FIG. 13

90. As FIG. 13 shows above, Wang753 describes a “semiconductor structure [that] includes a core circuit and an SRAM [static random access memory] cell.” (Wang753 at 1:51-56, 2:24-29.) Wang753 explains that this semiconductor structure includes active region 100 for the core PMOS devices and active region 300 for the SRAM PMOS devices. (Wang753 at 3:43-49, FIG. 13.)

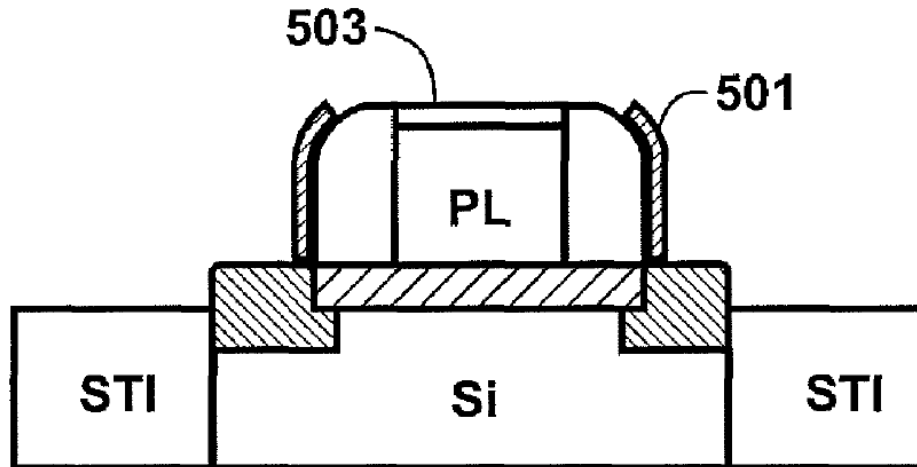
91. The core PMOS device structure, which is the primary structure I analyze, includes “a gate dielectric 102 on substrate 2 and a gate electrode 104 on gate dielectric 102.” (Wang753 at 3:49-52.) The core PMOS also includes raised “SiGe stressors 118” and “spacers 130,” formed with “a liner oxide layer 25 and a nitride layer 27.” (Wang753 at 4:14-18, 5:19-26.) Additionally, the core PMOS device structure includes “LDD regions 124 and halo regions 126 in active region 100” that are formed by introducing p-type and n-type impurities, respectively. (Wang753 at 4:45-51.) The SRAM cell includes similar PMOS devices in region 300. (Wang753 at 3:52-59, 4:14-18, 4:45-51, 4:56-58.)

E. The Chen Reference

92. I am not an attorney and am not qualified to assess whether a particular reference qualifies as prior art, but I have been asked to assume that Chen qualifies as prior art to the '847 Patent. I note, however, that Chen seems to have been filed on October 4, 2005. (Chen at cover page.)

93. Chen is in the same field of endeavor as the '847 Patent (MOSFETs and their fabrication), and Chen is reasonably pertinent to a problem the '847 Patent purports to address (fabricating strained silicon channel MOS transistors). (See Chen at Title, Abstract, 3:30-37, 5:32-36; '847 Patent at 1:6-10, 1:49-52.) Applying the standard for “analogous art” stated in the final paragraph of Section IV.B above, it

is my opinion that a person of ordinary skill in the art would have considered Chen to be analogous art to the '847 Patent.



Chen, FIG. 5

94. Chen describes “a method and structures for manufacturing MOS devices using strained silicon structures for advanced CMOS integrated circuit devices.” (Chen at 1:15-20.) As Fig. 5 shows, Chen’s devices include a gate structure with a conductive gate layer (“PL”) sandwiched between a gate dielectric layer underneath and a hard mask layer above (the upper surface of which is labeled 503). (Chen at 4:30-46, Fig. 5.)

95. As Fig. 5 also shows, Chen’s devices include sidewall spacers. (Chen at 3:60-4:4, 4:43-59, 5:60-6:19.) After patterning the gate structure, Chen (A) forms first spacers around the gate (Chen at 4:57-59), then (B) grows raised, strained epitaxial SiGe layers in trenches adjacent to the gate (Chen at 5:9-13, 5:32-39), and

(C) forms second spacers around the first spacers and overlying the strained SiGe layers (Chen at 6:11-15).

IX. THE CHALLENGED CLAIMS ARE ANTICIPATED AND/OR OBVIOUS IN VIEW OF THE PRIOR ART

96. By August 9, 2007, and even in the proceeding years, structures like the ones described in the '847 Patent were already known and used throughout the semiconductor industry. Because the relevant principles, fabrication methods, and MOS structures were already thoroughly established and widely known, a person of ordinary skill in the art would have found the claimed structures in the '847 Patent were already known or at least obvious. The following sections explain why I reach that conclusion in greater detail, and the chart below summarizes the grounds I address in my analysis.

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A / 1B	1, 3-9, 11	102 / 103	Lan
1C / 1D	2	103	Lan / Lan & Liaw
2A / 2B	1, 3-11	102 / 103	Wang407
3A / 3B	1, 10	102 / 103	Wang753
4A / 4B	1-2, 7-8	102 / 103	Chen

A. Grounds 1A and 1B: Lan Anticipates (Ground 1A) and Renders Obvious (Ground 1B) Claims 1, 3-9, and 11

97. Lan teaches, suggests, and renders obvious all the elements of claims 1, 3-9, and 11 of the '847 Patent.

98. Through the analysis below, I conclude that Lan anticipates claims 1, 3-9, and 11 (Ground 1A) because Lan discloses every limitation of those claims when viewed from the perspective of a person of ordinary skill in the art.

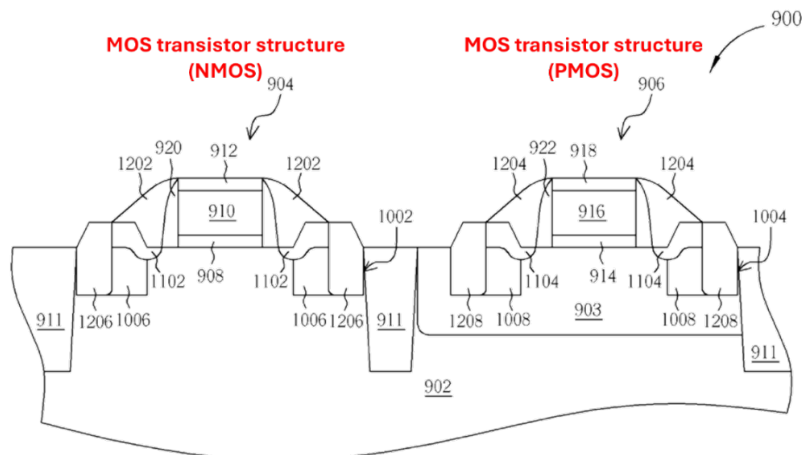
99. For the same reasons stated in my analysis below, I also conclude that Lan renders claims 1, 3-9, and 11 obvious (Ground 1B) because the differences between claims 1, 3-9, and 11 and Lan are such that claims 1, 3-9, and 11 would have been obvious to a person of ordinary skill in the art.

1. Independent Claim 1

a. [1pre]: “[a] MOS transistor structure”

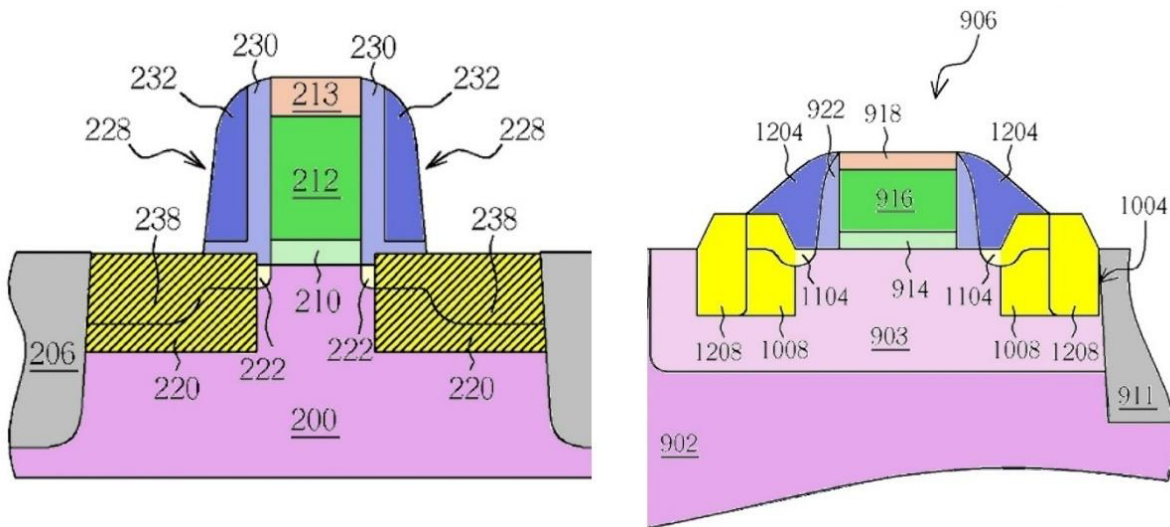
100. Lan discloses “[a] MOS transistor structure,” as recited in [1pre].

101. Lan discloses “a method of manufacturing ... a complementary metal oxide semiconductor transistor” comprising PMOS and NMOS devices, as Fig. 12 shows below. (Lan at 1:9-15, 1:53-54, 5:47-53, Figs. 1-12.) Lan thus discloses NMOS and PMOS transistor structures (each being MOS transistor structures).



Lan, Fig. 12 (annotated)

102. As the side-by-side comparison shows below, Lan's PMOS device has the same basic arrangement as the one the '847 Patent describes. For example, both include the same basic arrangement of gate, spacers, source/drain epitaxy layers, lightly doped regions, and substrate.

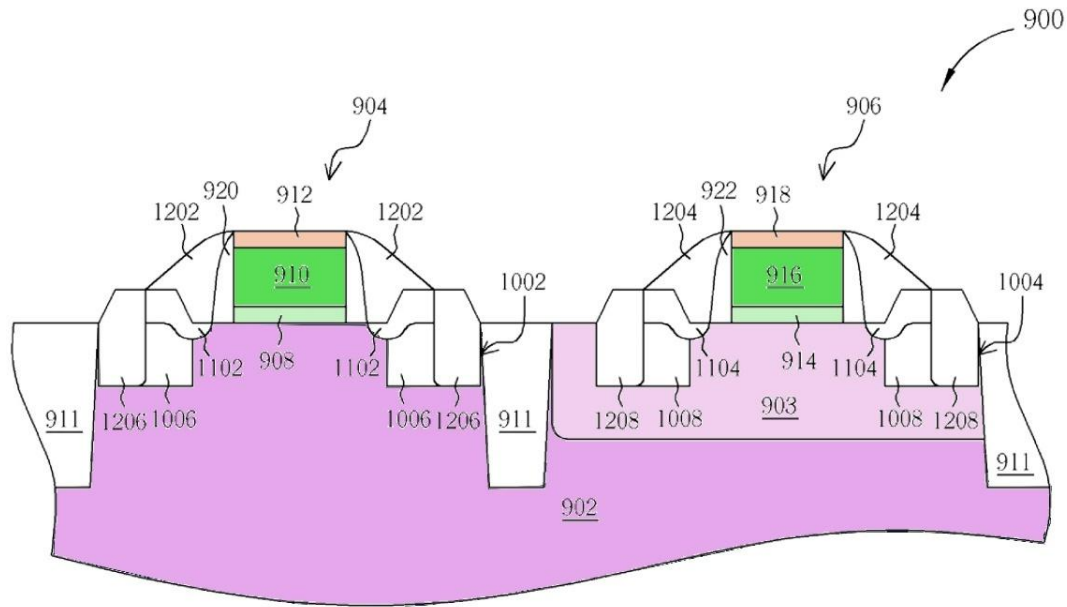


'847 Patent, Fig. 5 (PMOS excerpted) Lan, Fig. 12 (PMOS excerpted)

b. [1a]: "a gate formed on a semiconductor substrate"

103. Lan discloses "a gate formed on a semiconductor substrate," as recited in [1a].

104. Lan's disclosed method "provides a substrate, and a gate is formed on the substrate." (Lan at 1:56-57.) For example, Lan discloses "[g]ates 904, 906 . . . formed on the substrate 902," as Fig. 12 shows. (Lan at 4:54-56, 3:30-32, Figs. 1, 9.)



Lan, Fig. 12

105. Lan specifies that the “substrate can be silicon,” for example—which is a semiconductor material. (Lan at 5:54-56.)

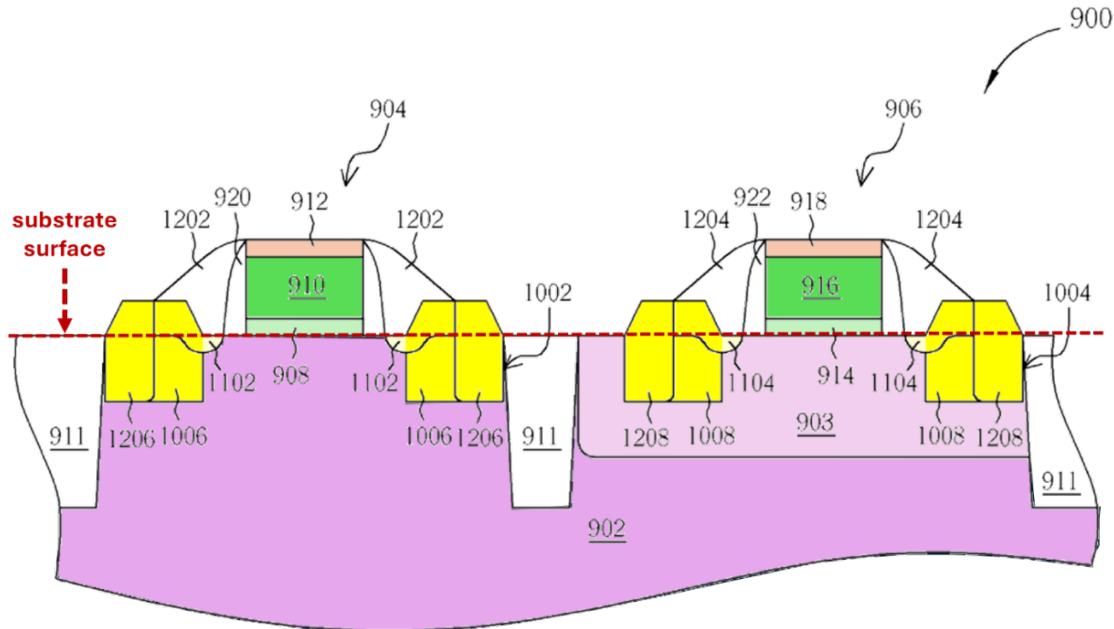
106. Lan explains that “[t]he gates 904, 906 include gate insulating layers 908, 914, doped poly-silicon layers 910, 916, and cap layers 912, 918.” (Lan at 4:56-58, 2:51-52, 3:32-34.)

107. Therefore, Lan discloses a gate (e.g., gates 904 and 906) formed on a semiconductor substrate (e.g., substrate 902).

- c. **[1b]: “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate”**

108. Lan discloses (Ground 1A), or at least renders obvious (Ground 1B), “two raised epitaxial layers positioned respectively in the semiconductor substrate

next to the relative sides of the gate and above the surface of the semiconductor substrate,” as recited in [1b].



Lan, Fig. 12 (annotated)

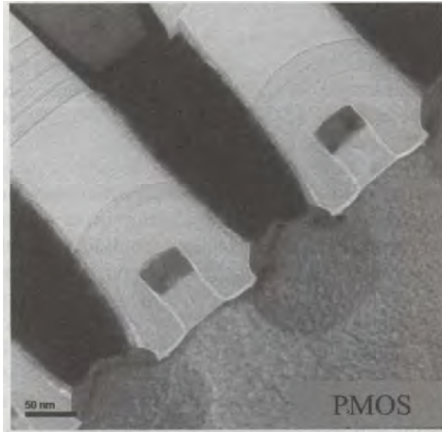
109. Lan discloses “a plurality of epitaxial layers . . . on the two sides of the gate.” (Lan at 1:59-60.) For example, Lan discloses that “a SEG [selective epitaxial growth] process is performed to form epitaxial layers 1006, 1008 in the recesses 1002, 1004.” (Lan at 4:67-5:2; *see also* Lan at Abstract, 2:59-65, 3:55-58.) Lan’s recesses are formed “in the substrate” on “the two sides of the gate,” then filled by growing “SiGe or SiC.” (Lan at 3:49-58; *see also* Lan at 2:59-65, 4:67-5:3, Figs. 2, 5-6, 10.) As Lan’s Fig. 12 illustrates above, a person of ordinary skill in the art would have understood (Ground 1A), or at least found obvious (Ground 1B), that

Lan's epitaxial layers 1006 and 1008 (highlighted yellow above) extend above the surface of the substrate 902 (marked with the red dashed line above).

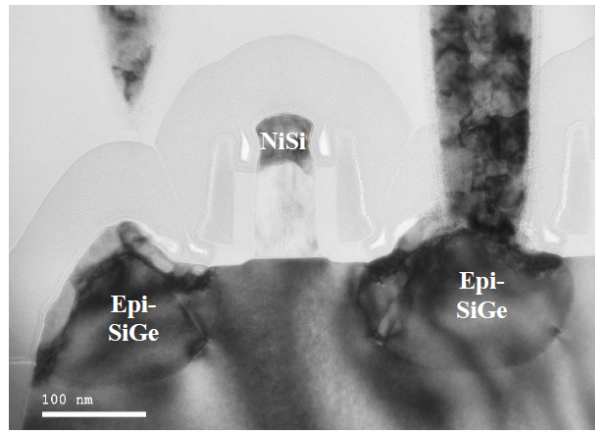
110. As of the priority date of the '847 Patent, a person of ordinary skill in the art would have been very familiar with cross-sectional figures like the one Lan presents in Fig. 12. These types of figures are frequently used to illustrate the basic structure of MOS transistor structures, and they have been a staple in the field for many decades. Although not always drawn to scale, such drawings, including Lan's Fig. 12 specifically, are often useful to illustrate the general shapes of elements and their spatial relationships to one another. For example, if such a figure shows one structural feature being higher than another, especially extending above the substrate, a person of ordinary skill in the art would have understood that positional relationship to be a relevant detail. Similarly, as another example, if two layers or elements are drawn in contact with one another, a person of ordinary skill in the art would have understood that positional relationship to be a relevant detail.

111. Further, as I discuss in Section VI.B, epitaxial source/drain stressors extending above the substrate surface (as Lan shows) was a typical and expected feature of prior-art strained channel technology. The epitaxial layers grow in substrate recesses and protrude above the substrate to reduce contact resistance and ensure adequate strain transfer to the channel. (As just a few examples, *see* James at 2, Fig. 6; Thompson at 1790-93, Figs. 2-5; Ghani at 978, Figs. 1-4; Bai at 657-58,

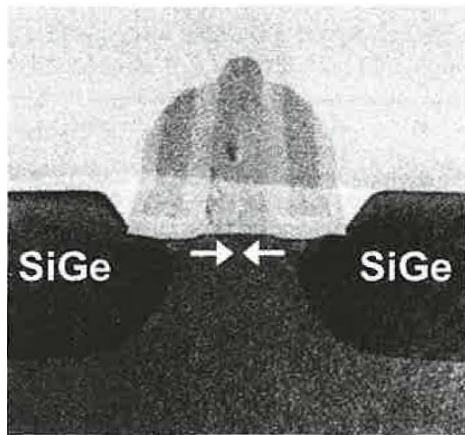
Fig. 4; Wang906 ¶¶[0030]-[0032], FIG. 9; Bohr at FIGS. 4-7; Kavalieros at Abstract, ¶[0025], ¶[0043], FIGS. 5, 13.) Those in the art would have known this.



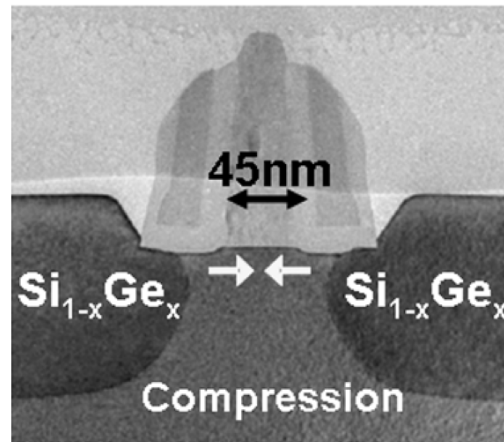
Bai, Fig. 4



James, Fig. 6



Ghani, Fig. 1



Thompson, Fig. 2

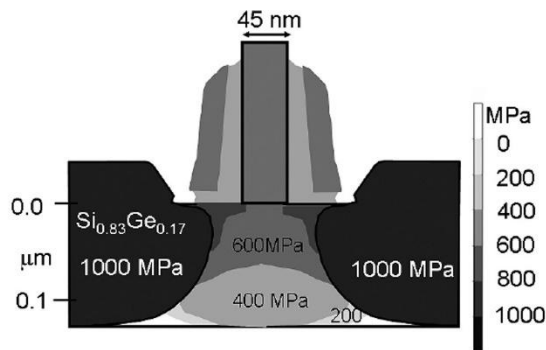


Fig. 4. Stress simulations for SiGe source/drain structure and gate length of 45 nm. Dominate stress is uniaxial along the direction of current flow. Contours of stress in MPa.

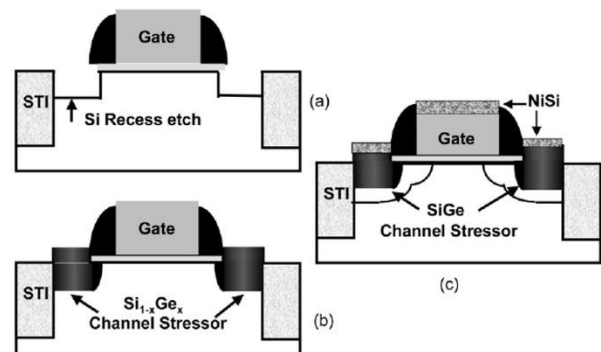
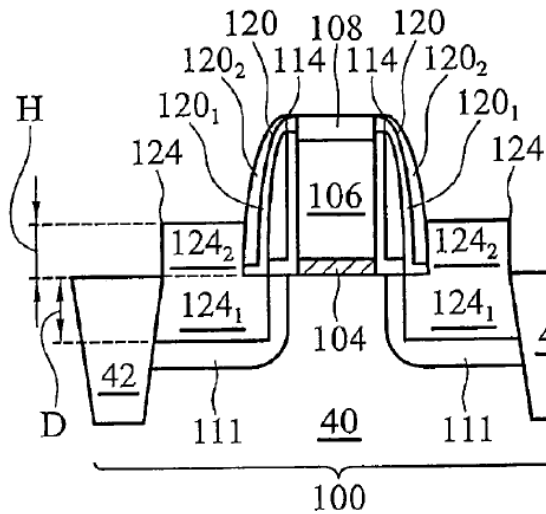


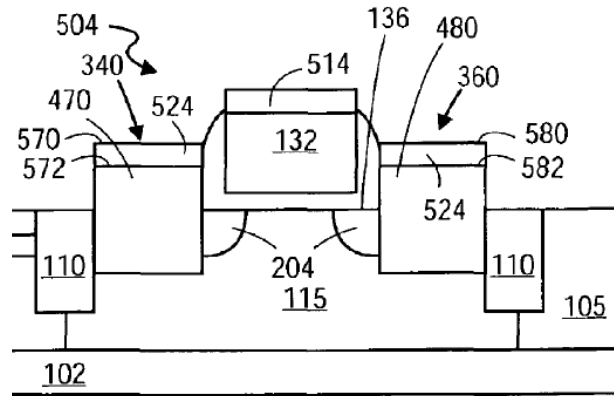
Fig. 3. Novel uniaxial strained-Si process flow use in this paper.

Thompson, Fig. 4

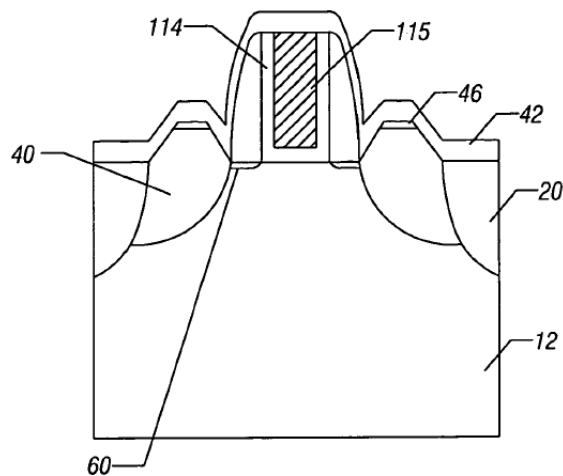


Wang906, FIG. 9 (excerpted)

Thompson, Fig. 3



Bohr, FIG. 5 (excerpted)



Kavalieros, FIG. 13

112. Accordingly, Lan discloses (Ground 1A), or at least renders obvious (Ground 1B), two raised epitaxial layers (e.g., epitaxial layers 1006 and 1008) positioned respectively in the semiconductor substrate (e.g., substrate 902) next to the relative sides of the gate (e.g., gates 904 and 906) and above the surface of the semiconductor substrate.

d. [1c]: “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer”

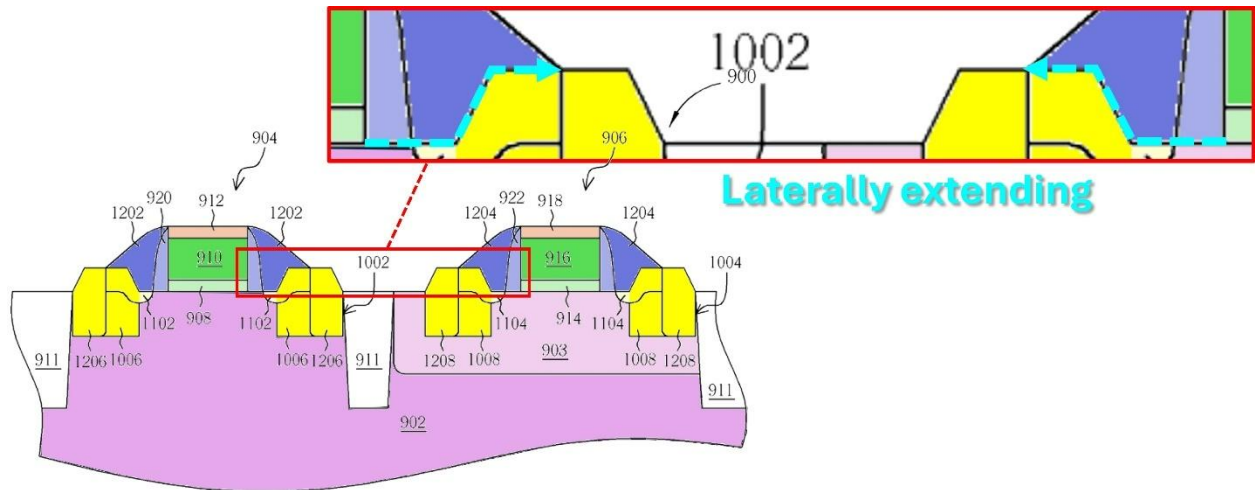
113. Lan discloses (Ground 1A), or at least renders obvious (Ground 1B), “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer,” as recited in [1c].

114. Lan discloses a “main spacer” and an “offset spacer,” including “main spacers 1202, 1204” and “offset spacers 920, 922.” (Lan at 4:59-65, 5:22-24; *see also* Lan at 3:4-8, 4:13-17.) Lan explains that the “offset spacer is formed around the gate.” (Lan at 1:57-59.) For example, “[a] deposition process and an anisotropic etching process are performed to form offset spacers 920, 922 around the gates 904, 906.” (Lan, 4:59-61; *see also* Lan at 2:53-55, 3:35-37, 4:13-15, Figs. 1, 5, 9.)

115. After growing epitaxial layers 1006 and 1008, the main spacer is formed around the offset spacer. For example, Lan teaches to deposit “[a] nitride silicon layer” and perform “[a]n anisotropic etching process ... to form main spacers 1202, 1204.” (Lan at 5:22-24; *see also* Lan at 3:4-8, 4:15-17, Figs. 4, 8, 12.) As an alternative to single-layer main spacers, Lan also explains they can be formed with multiple layers: “[T]he main spacer[s] are made by OO, ON, OON, ONO, ONONO.” (Lan at 5:61-63.) A person of ordinary skill in the art would have understood (Ground 1A), or at least found obvious (Ground 1B), that this refers to multiple sidewall layers of silicon oxide (“O”) and silicon nitride (“N”) formed in

the order listed. (*See*, for example, Chen at 6:3-10 (“The first oxide is about 200 Å, nitride 500 to 800 Å, second oxide 900 Å in the ONO, which is oxide on nitride on oxide structure.”), Fig. 4A; Thei at 12:2-14 (disclosing spacers “comprising oxide nitrides as shown (ON), oxide nitride oxide layers (ONO), oxide nitride nitride layers (ONN), [and] oxide nitride oxide nitride layers (ONON)”), 14:53-56 (“[I]n this illustrative preferred embodiment an alternative to the ON structure is shown, here an ONO structure is shown as the sidewall spacer”); Huang ¶[0024] (“[T]he spacers 80 and 82 can also be a multi-layer structure, such as an oxide-nitride (ON) dielectric layer, an oxide-nitride-oxide (ONO) dielectric layer, an oxide-nitride-oxide-nitride (ONON) dielectric layer, and so on.”).) Any of these main spacer embodiments, alone or together with the offset spacers, satisfies [1c].

116. As Lan’s Fig. 12 illustrates below, person of ordinary skill in the art would have understood (Ground 1A), or at least found obvious (Ground 1B), that Lan’s main spacers 1202 and 1204 extend laterally onto epitaxial layers 1006 and 1008. Consistent with the figure, Lan’s claim 5 recites “forming a main spacer . . . on part of the epitaxial layers.” (Lan at 6:51-53.) Lan teaches, for example, “to form source/drain 1206 in the epitaxial layers 1006 outside the two sides of the main spacer 1202 of the gate 904,” such that that the main spacers would cover a portion of the epitaxial layers. (Lan at 5:26-35.)



Lan, Fig. 12 (annotated & magnified)

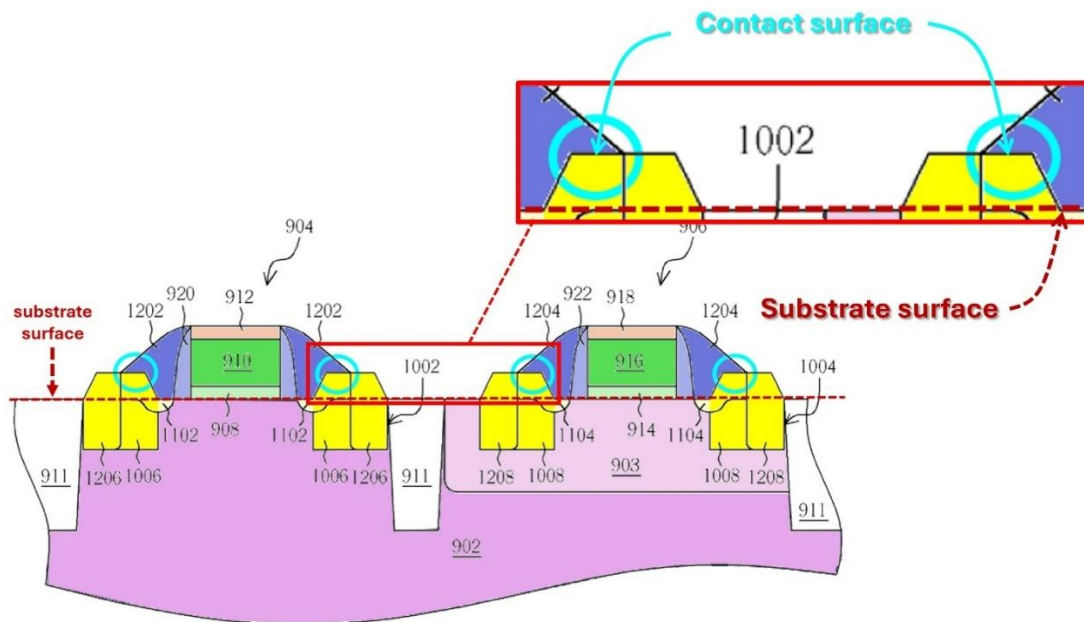
117. Therefore, Lan discloses (Ground 1A), or at least renders obvious (Ground 1B), a spacer (e.g., main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922) formed on the sidewall of the gate (e.g., gates 904 and 906) and extending laterally upon a portion of the raised epitaxial layer (e.g., epitaxial layers 1006 and 1008).

- e. **[1d]: “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate”**

118. Lan discloses (Ground 1A), or at least renders obvious (Ground 1B),
 “a contact surface of the raised epitaxial layers and a bottom of the spacer is above
 the surface of the semiconductor substrate,” as recited in [1d].

119. As I explain in Section IX.A.1.d, the preceding subsection for [1c], a person of ordinary skill in the art would have understood, or at least found obvious, that Lan's spacers (e.g., main spacers 1202 and 1204 alone or in combination with

offset spacers 920 and 922) extend onto a portion of Lan's epitaxial layers 1006 and 1008. The region where Lan's spacers and epitaxial layers overlap define contact surfaces. (See Lan at Fig. 12.) As I explain in Section IX.A.1.c for [1b], a person of ordinary skill in the art would have understood, or at least found obvious, that the upper surfaces of Lan's epitaxial layers 1006 and 1008 also extend above Lan's substrate surface. (See Lan at Fig. 12.) The annotated version of Fig. 12 below shows these features.



Lan, Fig. 12 (annotated & magnified)

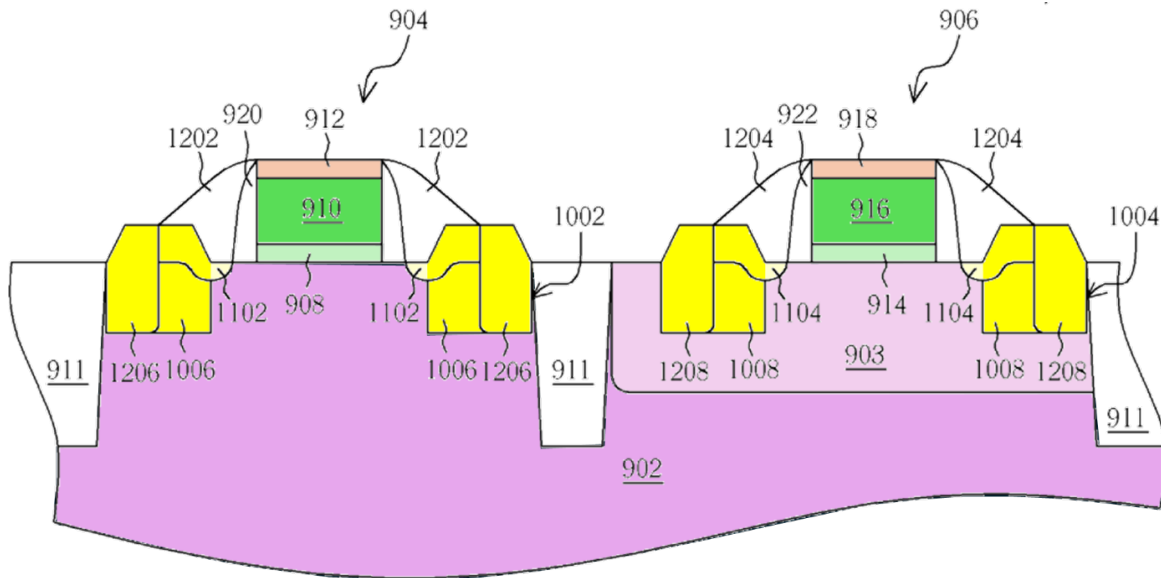
120. Therefore, as Fig. 12 illustrates above, Lan discloses (Ground 1A), or at least renders obvious (Ground 1B), a contact surface of the raised epitaxial layers (e.g., Lan's epitaxial layers 1006 and 1008) and a bottom of the spacer (e.g., the bottom of Lan's main spacers 1202 and 1204) is above the surface of the semiconductor substrate (e.g., Lan's substrate 902).

f. [1e]: “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate”

121. Lan discloses “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate,” as recited in [1e].

122. Lan’s source/drain regions are doped and comprise (A) “source/drain extension areas” 1102 and 1104 and (B) “source/drain” regions 1206 and 1208. (Lan at 5:7-10, 5:13-17, 5:26-29, 5:32-35; *see also* Lan at 1:9-49, 1:61-63, 2:3-9, 2:17-29, 3:8-11, 3:16-24, 3:63-4:46, Figs. 3-4, 7-8, 11-12.) Lan explains that “source/drain extension areas [1102 and 1104] are formed in the substrate outside . . . the epitaxial layers [1006 and 1008]” using “[a] light dopant implanting process.” (Lan at 1:61-63, 2:66-3:3; *see also* Lan at 5:7-10, 5:13-17.) Meanwhile, source/drain regions 1206 and 1208 are formed “in the epitaxial layers” 1006 and 1008, also using “[a]n ion implanting process.” (Lan at 5:26-29, 5:32-35.) Epitaxial layers 1006 and 1008 also may be doped *in situ* during epitaxial growth. (Lan at 5:41-43.)

123. All the source/drain regions Lan discloses (e.g., epitaxial layers 1006 and 1008, source/drain extension regions 1102 and 1104, and source/drain regions 1206 and 1208) (highlighted yellow below) are doped, and they are formed next to the sides of gates 904 and 906, as Fig. 12 illustrates below. (*See* Lan at Fig. 12.)



Lan, Fig. 12

124. Therefore, Lan discloses two doped regions (e.g., at least source/drain extension regions 1102 or 1104) formed respectively in the semiconductor substrate (e.g., substrate 902) next to the relative sides of the gate (e.g., gates 904 and 906).

125. Moreover, if a doped epitaxial region qualifies as a “doped region formed . . . in the semiconductor substrate,” then any combination of Lan’s epitaxial layers (e.g., 1006 and 1008), source/drain extension regions (e.g., 1102 and 1104), and/or source/drain regions (e.g., 1206 and 1208) would qualify as the claimed “two doped regions” in [1e]. (Lan at 4:59-5:54, Fig. 12.) Like Lan’s source/drain extension regions, Lan’s epitaxial layers and source/drain regions are formed next to the relative sides of gates 904 and 906, as Fig. 12 above shows. (See Lan at 5:7-10, 5:13-17, 5:26-31, 5:32-35, Fig. 12.)

2. Dependent Claims

a. Claim 3: “The structure of claim 1, wherein the MOS transistor comprises a PMOS transistor.”

126. As I explain in Section IX.A.1, Lan discloses and renders obvious the structure of claim 1.

127. Lan also discloses the MOS structure “wherein the MOS transistor comprises a PMOS transistor,” as recited in claim 3.

128. Lan discloses that the device in Fig. 12 is a “CMOS transistor” (Lan at 5:37-38), which means that it includes both NMOS and PMOS transistors. (*See* Section VI.A above.) Lan further specifies that the “PMOS ha[s] the epitaxial layer in a CMOS” and refers to “the etched recesses of the PMOS” when discussing CMOS fabrication. (Lan at 4:45-46, 5:47-53.) Therefore, Lan discloses that the MOS transistor of claim 1 comprises a PMOS transistor.

b. Claim 4: “The structure of claim 3, wherein the epitaxial layer comprises SiGe.”

129. As I explain in Section IX.A.2.a, Lan discloses and renders obvious the structure of claim 3.

130. Lan further discloses the structure “wherein the epitaxial layer comprises SiGe,” as recited in claim 4.

131. Lan discloses that epitaxial layers 1008 “are made from . . . SiGe.” (Lan at 5:2-3; *see also* Lan at 2:62-65; 3:55-58.) As I explain above in Section VI.B,

a person of ordinary skill in the art would have known SiGe is used in PMOS devices to provide compressive stress to the silicon channel and improve device performance. Accordingly, Lan discloses the structure of claim 3 wherein the epitaxial layers (e.g., Lan's PMOS epitaxial layers 1008) comprise SiGe.

c. Claim 5: “The structure of claim 1, wherein the MOS transistor comprises an NMOS transistor.”

132. As I explain in section IX.A.1, Lan discloses and renders obvious the structure of claim 1.

133. Lan also discloses the MOS transistor structure “wherein the MOS transistor comprises a NMOS transistor,” as recited in claim 5.

134. Lan discloses that the device in Fig. 12 is a “CMOS transistor,” meaning it includes both NMOS and PMOS transistors. (Lan at 5:37-38.) Lan further discloses that the “NMOS ha[s] the epitaxial layer in a CMOS” and refers to “the etched recesses of . . . the NMOS.” (Lan at 4:46-48, 5:47-53.) Therefore, Lan discloses that the MOS transistor of claim 1 comprises an NMOS transistor.

d. Claim 6: “The structure of claim 5, wherein the epitaxial layer comprises SiC.”

135. As I explain in section IX.A.2.c, Lan discloses and renders obvious the structure of claim 5.

136. Lan also discloses the MOS structure “wherein the epitaxial layer comprises SiC,” as recited in claim 6.

137. Lan discloses that epitaxial layers 1006 “are made from . . . SiC.” (Lan at 5:2-3; *see also* Lan at 2:62-65, 3:55-58.) As I explain in Section VI.B, a person of ordinary skill in the art would have known that SiC is used in NMOS and to provide tensile stress to the silicon channel and improve NMOS performance. Therefore, Lan discloses the structure of claim 5 wherein the epitaxial layers (e.g., Lan’s NMOS epitaxial layers 1006) comprise SiC.

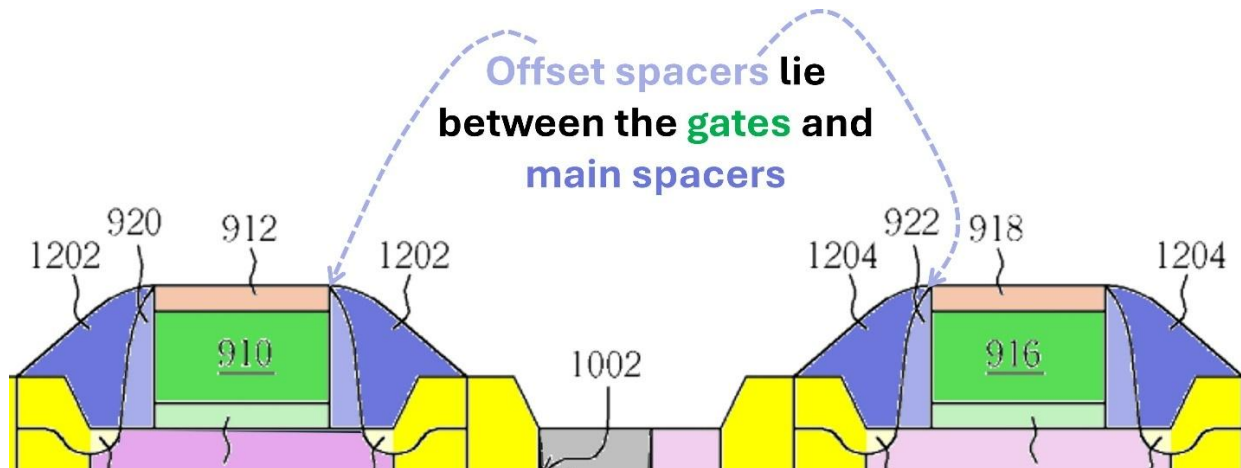
e. Claim 7: “The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.”

138. As I explain in section IX.A.1, Lan discloses and renders obvious the structure of claim 1.

139. For the reasons I explain in section VII.C, here I analyze claim 7 assuming that the claim can be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the claimed “gate.” Under such interpretation, Lan discloses claim 7.

140. As I explain in Section IX.A.1.d, Lan’s main spacers 1202 and 1204, alone or together with Lan’s offset spacers 920 and 922, satisfy the requirements of the claimed “spacer.” Lan’s offset spacers 920 and 922 are “formed around the gate.” (Lan at 1:57-59; *see also* Lan at 2:53-55, 3:35-37, 4:59-61.) Lan’s main spacers 1202 and 1204 are then “formed around the offset spacer.” (Lan at 4:15-17; *see also* Lan at 3:6-8, 5:22-24, Fig. 12.) Therefore, Lan discloses an offset spacer (e.g., offset

spacers 920 and 922) positioned between the gate (e.g., gates 904 and 906) and a portion of the “spacer” (e.g., main spacers 1202 and 1204 of the claimed spacer), as Fig. 12 shows below.



Lan, Fig. 12 (excerpted, annotated)

- f. **Claim 8: “The structure of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.”**

141. As I explain in section IX.A.1, Lan discloses and renders obvious the structure of claim 1.

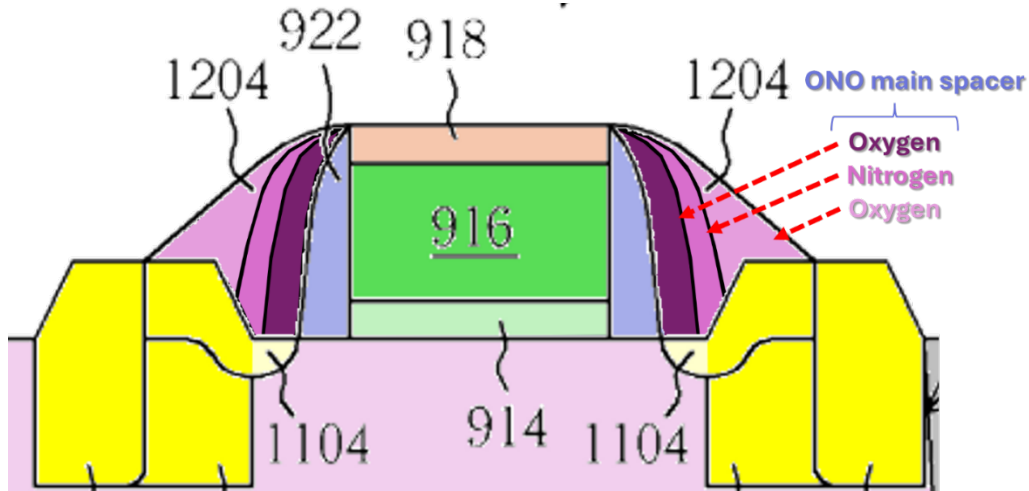
142. Lan also discloses, and at least renders obvious, the MOS transistor structure “wherein the spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 8.

143. As I explain in Section IX.A.1.d, Lan discloses a “spacer—i.e., main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922. As I also explain there, Lan’s main spacers may be “made by OO, ON, OON, ONO,

ONONO,” which a person of ordinary skill in the art would have understood (Ground 1A), and at least found obvious (Ground 1B), refers to multiple sidewall layers of silicon oxide (“O”) and silicon nitride (“N”) formed in the order listed. (Lan at 5:61-62; *see also* Chen at 6:3-10 (“The first oxide is about 200 Å, nitride 500 to 800 Å, second oxide 900 Å in the ONO, which is oxide on nitride on oxide structure.”), Fig. 4A; Thei at 12:2-14 (disclosing spacers “comprising oxide nitrides as shown (ON), oxide nitride oxide layers (ONO), oxide nitride nitride layers (ONN), [and] oxide nitride oxide nitride layers (ONON)”), 14:53-56 (“[I]n this illustrative preferred embodiment an alternative to the ON structure is shown, here an ONO structure is shown as the sidewall spacer”); Huang ¶[0024] (“[T]he spacers 80 and 82 can also be a multi-layer structure, such as an oxide-nitride (ON) dielectric layer, an oxide-nitride-oxide (ONO) dielectric layer, an oxide-nitride-oxide-nitride (ONON) dielectric layer, and so on.”).)

144. When Lan’s main spacers 1202 and 1204 comprise ONO, for example, a person of ordinary skill in the art would have understood (Ground 1A), and at least found obvious (Ground 1B), that they comprise an oxide liner (the interior “O” layer) and a nitride spacer (the central “N” layer), as shown below in modified Fig. 12. (Lan at 5:61-62.) Accordingly, as the modified version of Lan’s Fig. 12 shows below, Lan discloses, and at least renders obvious, that the spacer (e.g., main

spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922) further comprises an oxide liner and a nitride spacer.



Alternative Lan, Fig. 12 (modified to show exemplary ONO embodiment)

145. Additionally, Lan discloses that main spacers 1202 and 1204 may be silicon nitride and that offset spacers 920 and 922 must have etch selectivity relative to silicon nitride. (Lan at 4:59-67, 5:22-24.) A person of ordinary skill in the art would have understood (Ground 1A), and at least found obvious (Ground 1B), that silicon oxide would be, by far, the clearest option with the required etch selectivity for offset spacers 920 and 922.

146. A person of ordinary skill in the art would have understood (Ground 1A), and at least found obvious (Ground 1B), that certain etch chemistries may etch different materials different etch rates, and the ratio of those etch rates is called the “selectivity.” (Plummer at 612-13.) The relationship between materials, etchants, and relative etch rates (i.e., etch selectivities) were well-known to those in

the field of semiconductor processing. It was taught in textbooks. (*See*, for example, Plummer at 618 & Tbl. 10-1, 645 & Tbl. 10-3.) In particular, the use of silicon oxide and silicon nitride layers for forming gate sidewall spacers due to their relative etch selectivities was known and common. (*See*, for example, Hachimine, 12:23-26 (explaining insulating film 13 is made of silicon oxide), 18:3-6 (“The silicon nitride films (14a, 14b) are etched under conditions permitting these films to have an etching selectivity over the insulating film 13.”), FIG. 19; Plummer at 618 & Tbl. 10-1, 645 & Tbl. 10-3.)

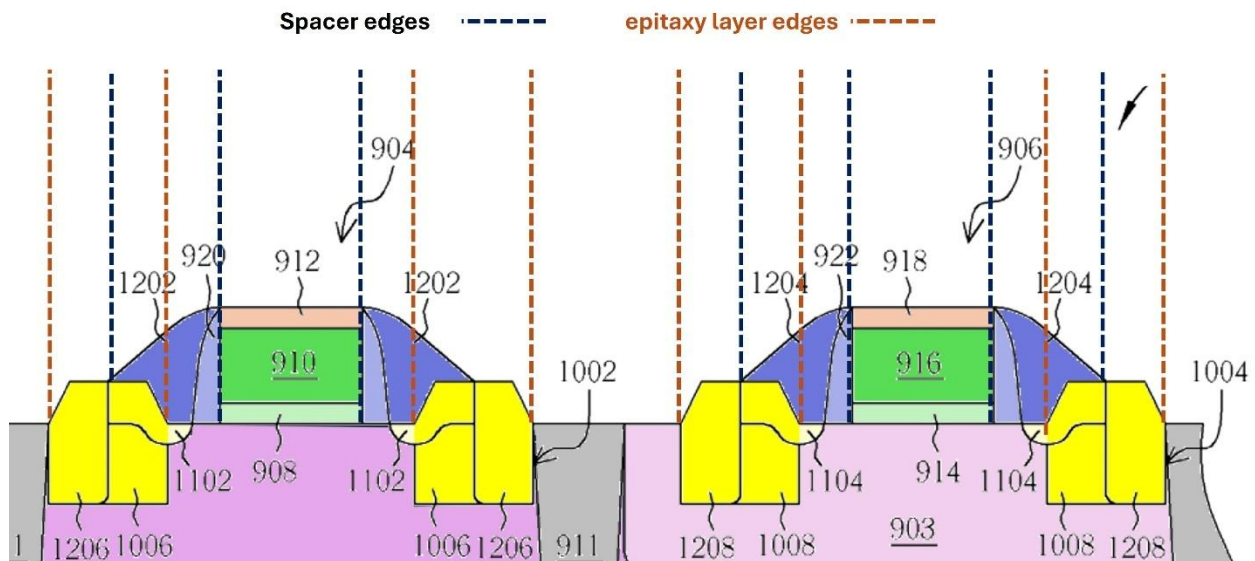
147. From this prior training, a person of ordinary skill in the art would have understood (Ground 1A), and at least found it obvious (Ground 1B), to make Lan’s offset spacers 920 and 922 using silicon oxide. Therefore, a person of ordinary skill in the art would have recognized Lan also discloses (Ground 1A), and at least renders obvious (Ground 1B), that the spacer comprises an oxide liner (e.g., offset spacers 920 and 922) and a nitride spacer (e.g., main spacers 1202 and 1204).

g. Claim 9: “The structure of claim 1, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.”

148. As I explain in section IX.A.1, Lan discloses discloses and renders obvious the structure of claim 1.

149. Lan also discloses the MOS transistor structure “wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer,” as recited in claim 9.

150. Lan discloses that the edges of the raised epitaxial layers (Lan’s epitaxial layers 1006 and 1008) are not aligned with the edges of the spacer (e.g., Lan’s main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922), as Lan’s Fig. 12 shows below. This is a natural consequence of how Lan uses offset spacers, disposable spacers, and main spacers to define lightly doped source/drain extension regions 1102 and 1104, source/drain epitaxial regions 1006 and 1008, and source/drain regions 1206 and 1208, respectively. (Lan at 2:65-3:11, 3:59-4:28, 5:4-35.)



Lan, Fig. 12 (excerpted, annotated)

151. In Lan, the edges of spacers cannot align with the edges of the epitaxial layers because: (A) while offset spacers 920/922 contact the edges of gates 910/916, the epitaxial layers 1006/1008 are specifically formed not to be aligned with the gate separated from the gate (*see* Fig. 12), and (B) the main spacers 1202/1204 are formed over only a portion of the epitaxial layers 1006/1008, so their edges cannot align. (Lan at 5:4-24, Figs. 10-12; *see also* Lan at 3:45-4:28.) Therefore, Lan discloses the edge of the raised epitaxial layers (e.g., Lan's epitaxial layers 1006 and 1008) is not aligned with the edge of the spacer (e.g., main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922).

h. Claim 11: "The structure of claim 1, further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers."

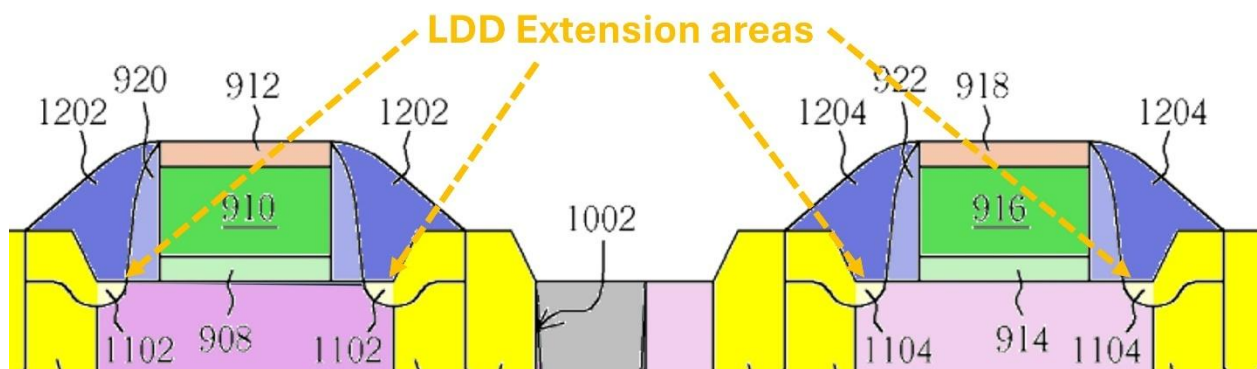
152. As I explain in section IX.A.1, Lan discloses discloses and renders obvious the structure of claim 1.

153. Lan also discloses the MOS transistor structure "further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers," as recited in claim 11.

154. Lan discloses that "source/drain extension areas [1102 and 1104] are formed in the substrate outside . . . the epitaxial layers [1006 and 1008]" using "[a] light dopant ion implanting process." (Lan at 1:61-63, 2:66-3:3; *see also* Lan at 5:7-10, 5:13-17.) This process Lan describes is the same process the '847 Patent

describes for LDD formation. (See '847 Patent at 3:29-54, Figs. 3-4.) And Lan specifically refers to source/drain extension areas 1102 and 1104 as “LDDs,” which stands for “lightly doped drain” regions. (Lan at 5:17-19; *see also* Lan at 2:66-3:3.)

155. Therefore, Lan discloses that the structure of claim 1 further includes a lightly doped drain (e.g., source/drain extension areas 1102 and 1104) disposed in the semiconductor substrate (e.g., substrate 902) and outside the raised epitaxial layers (e.g., epitaxial layers 1006 and 1008), as Fig. 12 shows below. This is the same arrangement the '847 Patent specifies for its “lightly doped region[s].” (See '847 Patent at 3:29-54, 6:17-26, Figs. 3-4, 11-13.)



Lan, Fig. 12 (excerpted, annotated)

B. Grounds 1C and 1D: Lan Alone (Ground 1C) and Lan combined with Liaw (Ground 1D) Render Claim 2 Obvious

1. [2pre]: “[t]he structure of claim 1”

156. As I explain in Section IX.A.1, Lan discloses and renders obvious the structure of claim 1.

2. [2a]: “wherein the gate further comprises: a dielectric layer”

157. Lan further discloses “wherein the gate further comprises: a dielectric layer,” as recited in [2a].

158. Lan discloses that gates 904 and 906 comprise “gate insulating layers 908, 914.” (Lan at 4:56-57.) Lan’s “gate insulating layer is made by materials having high-K, such as oxide, nitric oxide, nitride, silica, or hafnium silicates,” which are well-known dielectric materials. (Lan at 5:56-58.) Therefore, Lan discloses that the gates (e.g., gates 904 and 906) further comprise a dielectric layer (e.g., insulating layers 908 and 914).

3. [2b]: “a conductive layer, positioned on the dielectric layer”

159. Lan further discloses the gate in its transistors structure comprises “a conductive layer, positioned on the dielectric layer, ” as recited in [2b].

160. Lan discloses that gates 904 and 906 comprise “doped poly-silicon layers 910, 916.” (Lan at 4:56-58.) When Lan refers to “doped polysilicon layers” it is disclosing a conductive layer. Polysilicon in MOSFETs, and specifically doped polysilicon, is considered conductive. (*See*, for example, Quirk at 302 & Tbl. 12.1 (resistivity of doped polysilicon is “ ≈ 500 to $525 [\mu\Omega\cdot\text{cm}]$ ”).) Lan also discloses that “[t]he gate is not limited by the above poly-silicon.” (Lan at 5:58-60.) Lan’s layers 910 and 916 “also can be made by . . . any conductive material, such as metal,” which is also conductive. (Lan at 5:58-60.)

161. As Lan's Fig. 12 shows, conductive layers 910 and 916 are positioned on insulating layers 908 and 914, respectively. Therefore, Lan discloses that the gates (e.g., gates 904 and 906) comprise a conductive layer (e.g., polysilicon or metal layers 910 and 916) positioned on the dielectric layer (e.g., insulating layers 908 and 914).

4. [2c]: "a cap layer, positioned on the conductive layer"

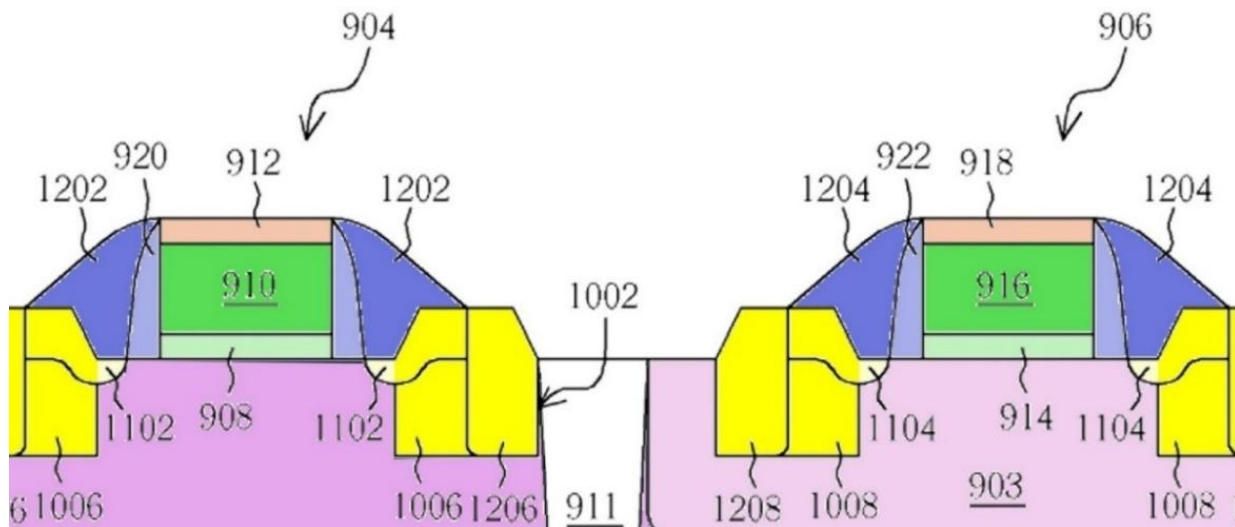
162. A person of ordinary skill in the art would have found it obvious for Lan's gates (e.g., gates 904 and 906) to comprise "a cap layer, positioned on the conductive layer," as recited in [2c]. For example, a person of ordinary skill in the art would have found it obvious for Lan's gates 904 and 906 to include cap layers 912 and 918 positioned on the conductive layer (e.g., metal gate layers 910 and 916) based on prior training (Ground 1C) and also further in view of Liaw (Ground 1D). I explain both rationales in the subsections below.

a. Ground 1C: Lan renders claim 2 obvious

163. Lan's gates 904 and 906 comprise "cap layers 912, 918," as Lan's Fig. 12 illustrates. (Lan at 4:56-58; *see also* Lan at 2:51-62, 3:8-11, 3:32-34, 3:49-53.) When etching recesses in the substrate for the epitaxial source/drain layers, Lan's cap layers "serve as etching masks." (Lan at 2:49-61; *see also* Lan at 3:49-53, Fig. 5.)

164. A person of ordinary skill in the art would have understood this means Lan's cap layers are made of a material, such as an oxide or nitride insulator, that provides etch selectivity over the silicon substrate. (*See*, for example, Plummer at 645 & Tbl. 10-3; Lan at 5:54-56 (silicon substrate); Liaw, 4:6-20 ("Appropriate materials of the cap layer 312 include oxide, silicon oxynitride, silicon nitride, ..."), 5:37-39 ("The cap layer 412, typically oxide, is deposited on top of the metal gate conductor 408."); Wang407, 3:38-40 ("Hard mask 18 preferably comprises silicon nitride, although other materials such as oxides, oxynitrides, and silicon carbide can also be used."); Wang753, 3:56-59 ("The gate stacks are preferably masked by hard masks 106, 206, 306 and 406, respectively, which are preferably formed of materials such as oxide, silicon nitride, silicon oxynitride, and combinations thereof."); Chen, 4:43-48 ("The hard mask layer can be made of any suitable material such as a dielectric material").)

165. Lan's Fig. 12 below confirms that Lan's cap layers 912 and 918 are positioned on Lan's conductive layers 910 and 916. (Lan at 4:56-58.) Accordingly, Lan's gates (e.g., gates 904 and 906) comprise a cap layer (e.g., cap layers 912 and 918) positioned on the conductive layer (e.g., Lan's metal gate layers 910 and 916).



Lan, Fig. 12 (excerpted)

166. After completing the structure shown in FIG. 12 above, Lan states that “a self-aligned silicide process is performed to silicide ... the gates 904, 906, and the source/drain 1206, 1208.” (Lan at 3:12-14.) A self-aligned silicide process is also known in the industry as a “salicide” process.

167. A person of ordinary skill in the art would have understood that performing a salicide process on the gate in Lan's FIG. 12 only makes sense if Lan's conductive layers 910 and 916 are made of polysilicon. A person of ordinary skill in the art also would have understood that the salicide process can be applied to polysilicon layers 910 and 916 in Lan's FIG. 12 only if cap layers 912 and 918 are first removed.

168. As I explain for [2b] in Section IX.B.3, Lan’s conductive gate layers 910 and 916 are “not limited [to] poly-silicon” and, alternatively, “can be

made by . . . any conductive material, such as metal.” (Lan at 5:58-60.) In an embodiment of Lan’s FIG. 12 where gate conductor layers 910 and 916 are made of metal, a person of ordinary skill in the art would have found it obvious to retain cap layers 912 and 918 because siliciding metal gate conductors is unworkable and unnecessary.

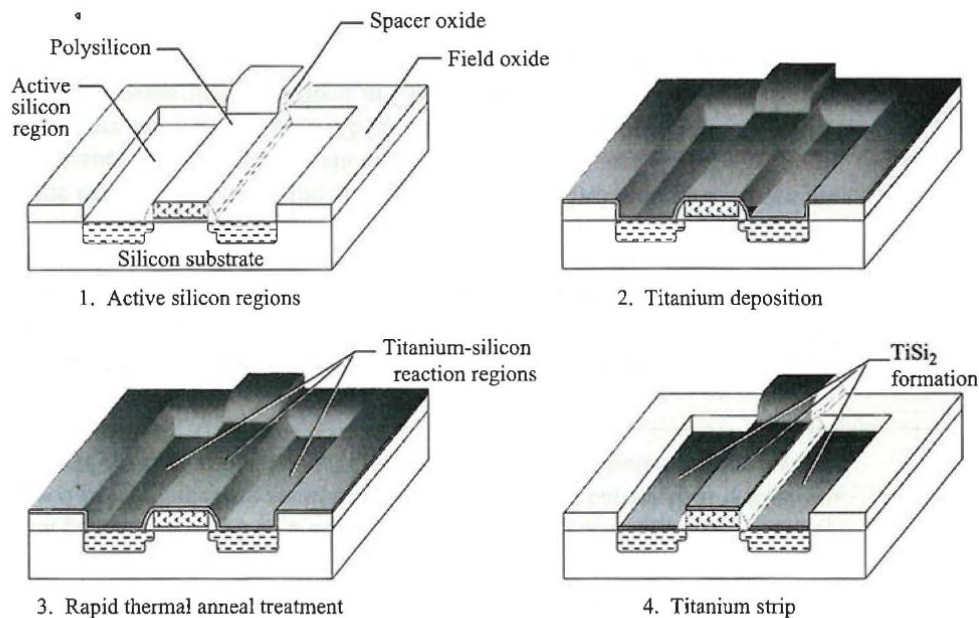


FIGURE 12.13 Formation of Self-Aligned Metal Silicide (Salicide)

Quirk, Fig. 12.13

169. The textbook illustrations above illustrate the three basic stages of the salicide process. (Quirk at 311-12, Fig. 12.13.) First, a metal (in this example, titanium) is deposited over the entire substrate, which includes exposed silicon regions. Second, the structure is heated to a temperature sufficient to cause the metal atoms to react with the exposed silicon. This is typically achieved by a rapid thermal annealing process. As a result of this heat treatment, a metallic silicide compound

selectively forms where the metal and silicon are in direct contact (e.g., in the titanium-silicon reaction regions shown below). Third, the unreacted metal is selectively stripped away using a selective chemical etchant (e.g., a titanium strip below), which leaves behind the silicide (TiSi_2 below) in the reacted areas and removes the metal everywhere else.

170. Applying this introductory textbook knowledge to Lan's FIG. 12, a person of ordinary skill in the art would have understood Lan's cap layers 912 and 918 must be removed in order to perform the silicide process on the polysilicon gate layers 910 and 916. Otherwise, Lan's cap layers 912 and 918 would block the silicide reaction in the gate region. (*See*, for example, Fischer at 9:28-38 (explaining that such a cap layer will "shield the gate stack" from silicidation); Quirk at Fig. 12.13 (showing how silicide does not form in non-silicon regions).)

171. By applying this same textbook knowledge to Lan's metal-gate embodiment—that is, Lan's FIG. 12, wherein gate conductor layers 910 and 916 are made of a metal rather than polysilicon (*see* Lan at 5:58-60)—a person of ordinary skill in the art would have understood it would be unworkable and unnecessary to perform a silicide process on Lan's gate conductor layers 910 and 916. There are at least three reasons for this.

172. First, a person of ordinary skill in the art would have understood that a silicide process would not work when Lan's conductive gate layers 910 and 916 are

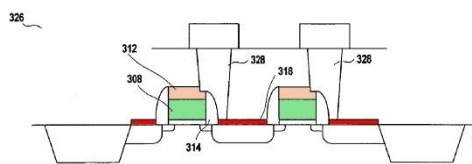
made of metal. When layers 910 and 916 are made of metal, there would be no silicon in the gate for the salicide metal layer to react with. The reaction between the silicide metal and an underlying silicon layer is fundamental to the salicide process. (Quirk at 214, 312, Fig. 12.13.) When Lan's conductive gate layers 910 and 916 are made of metal, there is no silicon layer on the gate.

173. Second, a person of ordinary skill in the art would have understood that there is no need for a gate silicide when Lan's conductive gate layers 910 and 916 are made of metal. The reason for performing a salicide process on polysilicon is to reduce resistivity. Doped polysilicon has a resistivity of about $500\ \mu\Omega\cdot\text{cm}$, whereas silicides have a resistivity of about $10\ \mu\Omega\cdot\text{cm}$. (See Quirk at 302 & Tbl. 12.1 (doped polysilicon has a resistivity of " ≈ 500 to $525\ [\mu\Omega\cdot\text{cm}]$ "), 311 & Fig. 12.11 (C54 phase of TiSi_2 has a resistivity of " $10\text{-}15\ \mu\Omega\cdot\text{cm}$ ").) A person of ordinary skill in the art would have understood metals already have resistivities of about $10\ \mu\Omega\cdot\text{cm}$, making silicide unnecessary. (See Quirk at 302 & Tbl. 12.1 (metal resistivities ranging from about 1 to $15\ \mu\Omega\cdot\text{cm}$); Liaw at 4:66-5:2 (explaining that "no salicide layer is needed" when "the gate conductor . . . is made of metal").)

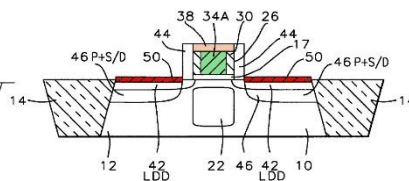
174. Third, a person of ordinary skill in the art would have understood that when layers 910 and 916 are made of metal, it would be beneficial to retain cap layers 912 and 918 on top of the gate. If Lan's cap layers 912 and 918 were removed, then metal gate layers 910 and 916 underneath would be exposed to the chemicals

used to strip the unreacted metal used to make the silicide on source/drain regions 1206 and 1208. (*See* Lan at 5:35-37 (“[A] self-aligned silicide process is performed to silicide . . . the source/drain 1206, 1208.”).) A person of ordinary skill in the art would have understood such exposure is undesirable because it can remove, corrode, or damage metal layers 910 and 916. A person of ordinary skill in the art thus would have understood the beneficial protection offered by cap layers 912 and 918 when Lan’s gate layers 910 and 916 are made of metal.

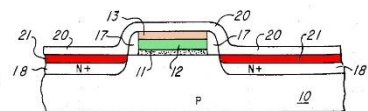
175. Examples from the prior art confirm that a person of ordinary skill in the art would have understood to retain Lan’s cap layers 912 and 918 when gate conductors 906 and 910 are made of metal. For example, Liaw explains that “no salicide layer is needed” when “the gate conductor . . . is made of metal.” (Liaw at 4:66-5:2.) In the examples below, the gate conductor (green) is metal (Liaw at 3:58-65; Tsai at 5:56-59; McDavid at 2:24-26), and the cap layer (peach) is retained during the salicide process used to form silicide source/drain electrodes (red) (Liaw at 4:63-5:23; Tsai at 5:66-6:2, 6:30-31; McDavid at 2:26-28, 3:13-19).



Liaw, Fig. 3B

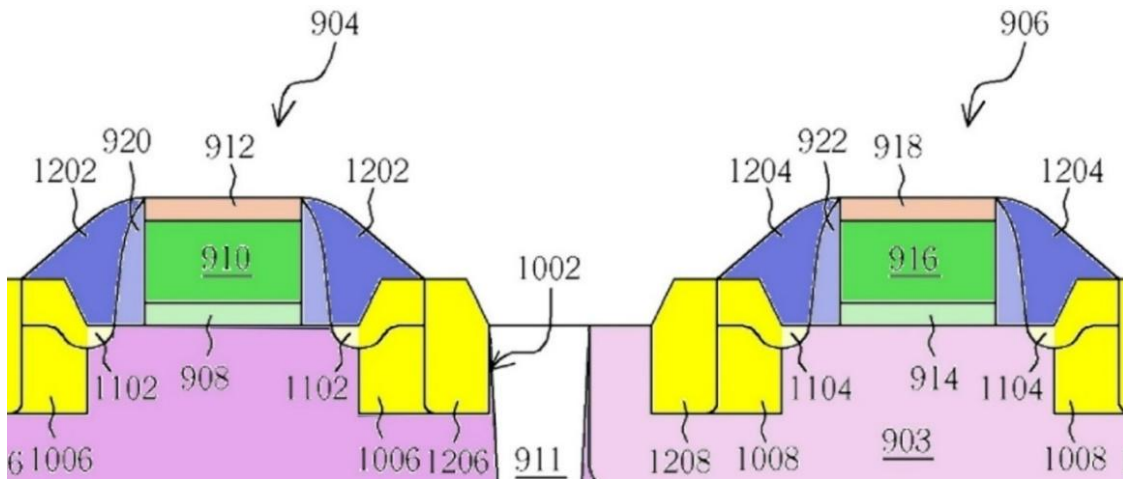


Tsai, Fig. 7



McDavid, Fig. 5

176. For all the reasons above, a person of ordinary skill in the art would have understood, and found it obvious, from prior training to retain cap layers 912 and 918 when Lan's conductive gate layers 910 and 916 are made of metal.



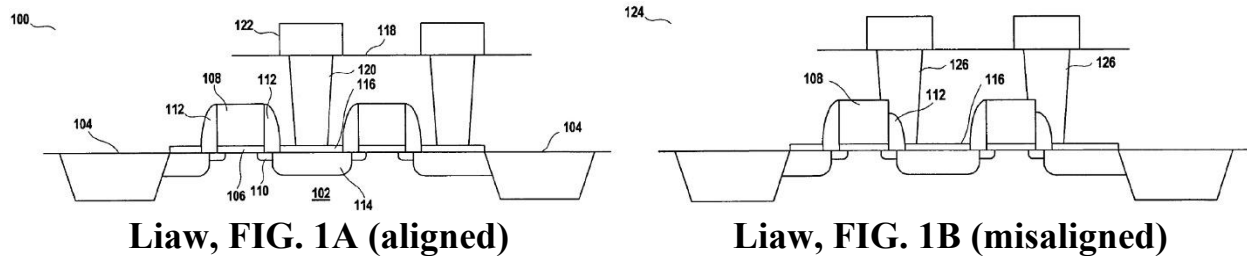
Lan, Fig. 12 (excerpted)

177. By retaining Lan's cap layers 912 and 918 when conductive gate layers 910 and 916 are made of metal, a person of ordinary skill in the art would have understood that Lan's gates (e.g., gates 904 and 906) include a cap layer (e.g., cap layers 912 and 918) positioned on the conductive layer (e.g., metal layers 910 and 916), as in Fig. 12 above.

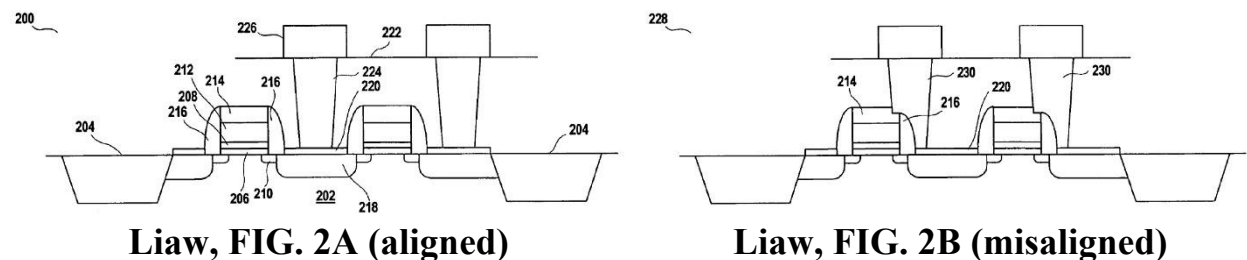
b. Ground 1D: The combination of Lan and Liaw renders claim 2 obvious

178. By further applying Liaw's teachings to Lan, a person of ordinary skill in the art also would have found it obvious to retain Lan's cap layers 912 and 918 when layers 910 and 916 are made of metal. (*See* Lan at 5:58-60.)

179. Liaw explains: “[T]o avoid an undesired electrical connection between the gate conductor and the source/drain regions through the self-aligned contact, a cap layer is usually formed atop the gate conductor as a protection layer.” (Liaw at 1:45-48.) Without such a cap layer, misalignment of the source/drain contact plugs (features 126 below) can cause “the circuit [to] be shorted, thereby causing failure.” (Liaw at 2:50-59.) Comparing Liaw’s FIGS. 1A and 1B illustrates this concept.



180. A cap layer, such as Liaw’s cap layer 214 in FIG. 2B below, prevents short-circuiting between the gate and source/drain region. This added tolerance for misalignment when forming the source/drain contacts results in what are called “self-aligned” source/drain contacts. (Liaw at 3:19-29, FIGS. 2A-2B; *see also* Lan at 4:48-51.)



181. When the gate conductor layer is made of polysilicon, forming a gate cap layer to allow for self-aligned source/drain contacts can be challenging. When

paired with silicidation of the source/drain regions of the substrate, Liaw explains that the source/drain silicide “must be formed before the cap layer.” (Liaw at 3:30-40.) As a result, two separate silicide processes are required—one for the gate electrode and one for the source/drain electrodes. (Liaw at 3:40-46.) And that “significantly increases the fabrication overhead” because “it complicates the fabrication process and increases costs.” (Liaw at 3:46-49.) Liaw refers to this additional overhead as “the dilemma of choosing between a salicide layer on the poly-silicon gate conductor and a self-aligned contact on the source/drain regions.” (Liaw at 4:63-66.) To avoid this dilemma, Liaw teaches to use a metal gate conductor layer. (See, for example, Liaw at Title, 1:51-54.)

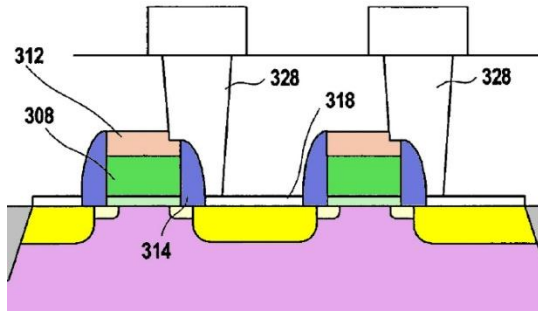
182. Lan’s illustrated embodiment uses “doped poly-silicon layers 910, 916.” (Lan at 4:56-58.) For that embodiment, Lan teaches to perform a salicide process “on the gates 904, 906, and the source/drain 1206, 1208.” (Lan at 4:56-58, 5:35-37.) As I explain in the preceding subsection, a person of ordinary skill in the art would have understood this involves **removing** cap layers 912 and 918. (See Section IX.B.4.a above.) Because of this, Lan’s polysilicon-gate embodiment faces Liaw’s “dilemma of choosing between a salicide layer on the poly-silicon gate conductor and a self-aligned contact on the source/drain regions.” (Liaw at 4:63-66.) In other words, Lan can either forego self-aligned source/drain contact plugs in its polysilicon-gate embodiment, thereby risking short-circuits due to misalignment, or

else the process would need to be modified as described in Liaw. (*See* Liaw at 3:30-49.) As Liaw explains, this would both “significantly increase[] the fabrication overhead” and “complicate[] the fabrication process and increases costs.” (Liaw at 3:44-49.) Liaw’s capped metal-gate approach does not suffer from this drawback.

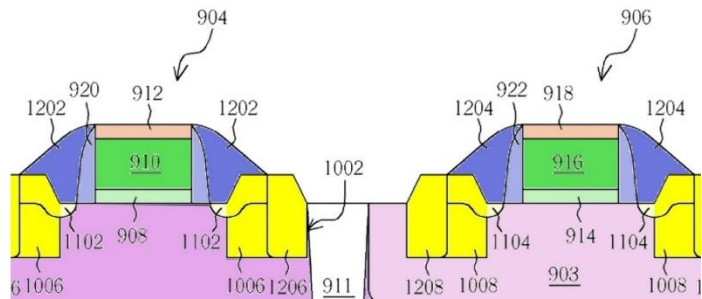
183. Lan’s disclosures, however, are not limited to polysilicon gates. Lan explains that “[t]he gate is not limited [to] poly-silicon, and it also can be made by . . . any conductive material, such as metal.” (Lan at 5:58-60.) Such an embodiment is consistent with Liaw’s solution to the “dilemma of choosing between a salicide layer on the poly-silicon gate conductor and a self-aligned contact on the source/drain regions.” (Liaw at 4:63-66; *see also* Liaw at 4:63-5:23, FIG. 3B.)

184. Liaw’s disclosed structure uses a metal gate conductor, consistent with Lan’s metal-gate embodiment. (*See* Lan at 5:58-60 (“The gate . . . can be made by . . . any conductive material, such as metal.”); Liaw, 1:58-67 (“[T]he gate structure includes . . . a metal gate conductor disposed on the gate dielectric layer, [and] a cap layer disposed on the metal gate conductor”).) Lan’s MOS transistors and Liaw’s MOS transistors have the same gate configuration. (*See* Liaw at 4:6-20; Lan at 4:56-58, 5:58-60.) Both use a gate conductor layer made of metal. (*See* Lan at 5:58-60; Liaw at 3:58-65.) Additionally, both include a cap layer. Thus, when Lan states that “[t]he gate . . . can be made by . . . any conductive material, such as metal,” it is my opinion that a person of ordinary skill in the art would have

Declaration of Prof. Eugene Fitzgerald, Ph.D.



Liaw, FIG. 3B (excerpted)

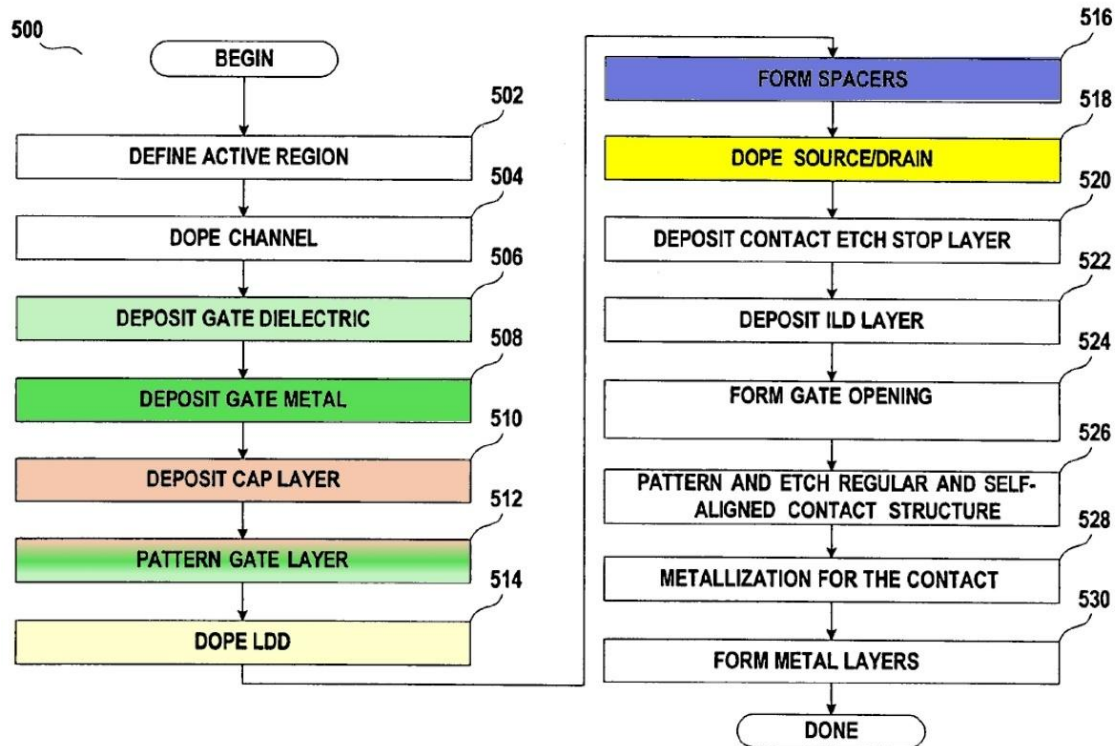


Lan, Fig. 12 (excerpted)

185. For example, Liaw's cap layer may be "an oxide layer or a layer of oxide covered by a layer of silicon nitride." (Liaw at 4:15-20.) A person of ordinary skill in the art would have understood that using such a material for Lan's cap layers 912 and 918 would satisfy Lan's requirement that the cap layer must provide etch selectivity over the semiconductor substrate during source/drain recess etching. (See Lan at 4:65-67; Plummer at 645 & Tbl. 10-3 (providing exemplary plasma etch chemistries for selectively etching silicon over silicon oxide, for instance).)

186. As the flow chart in Liaw's FIG. 5 illustrates below, a person of ordinary skill in the art would have understood that Lan's process flow and Liaw's process flow are also very similar. Both deposit and pattern gate dielectric, gate conductor, and cap layers to form a gate structure. (*See* Lan at 4:49-58, Fig. 9; Liaw at 3:50-4:5, 6:25-30.) Both also form LDD regions, gate sidewall spacers, and deep source/drain regions, in that order. (*See* Lan at 5:6-35, Figs. 9-12; Liaw at FIG. 5.)

And both Lan and Liaw disclose a subsequent salicide process performed on the source/drain regions. (See Lan at 5:35-37; Liaw at 4:36-38.)



Liaw, FIG. 5

187. Given these similarities in both structure and process flow between Lan and Liaw, a person of ordinary skill in the art would have understood Lan's metal-gate embodiment (*see* Lan at 5:58-60, Fig. 12) implements Liaw's solution (*see* Liaw at 4:63-5:23, FIG. 3B) simply by retaining cap layers 912 and 918.

188. In view of Liaw's teachings, a person of ordinary skill in the art would have been motivated to make Lan's gate conductor layers 910 and 916 using metal and to retain cap layers 912 and 918 when doing so. According to Liaw, such an approach avoids the increased fabrication overhead, added complexity, and

increased costs that would be necessary to achieve self-aligned source/drain contacts in Lan's polysilicon-gate embodiment. (Liaw at 3:44-49.) It "avoids the dilemma of choosing between a salicide layer on the poly-silicon gate conductor and a self-aligned contact on the source/drain regions." (Liaw at 4:63-66.) Liaw explains:

[S]ince the gate conductor 308 is made of metal, *no salicide layer is needed* for improving its interface quality with a metal interconnection structure. This naturally solves the dilemma by choosing to form the self-aligned contact 318 atop the source/drain regions 316, without sacrificing the contact quality of the metal gate conductor 308. In addition, *by keeping the cap layer 312 atop the metal gate conductor 308*, the MOS device 300 is able to tolerate a slight misalignment of the conductive plug 322.

(Liaw at 4:66-5:8 (emphases added).) A person of ordinary skill in the art thus would have understood from Liaw that, by retaining Lan's cap layer, "[e]lectrical contact is, as intended, only made to the salicide source/drain contact 318, since the insulating cap layer 312 insulates the metal gate conductor 308 from being exposed." (Liaw at 5:18-21.) A person of ordinary skill in the art would have understood, as Liaw teaches, the resulting benefit is improved misalignment tolerance for the source/drain contacts. (Liaw at 5:22-23 ("Thus, a slight misalignment of the [source/drain] conductive plug . . . can be tolerated.").)

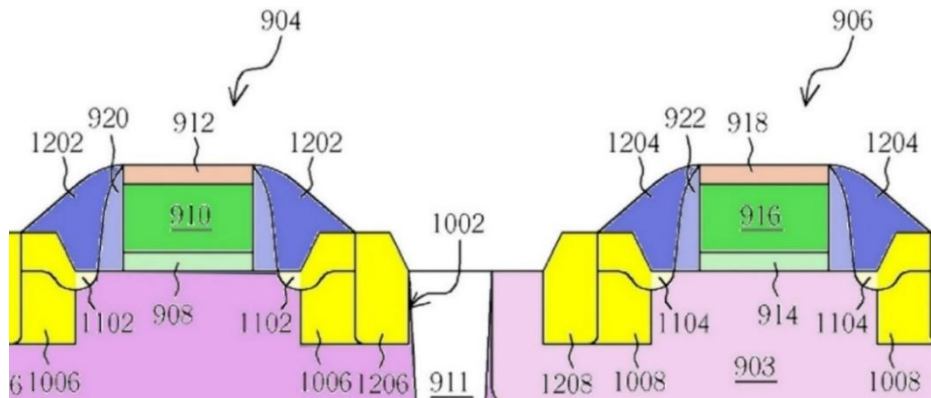
189. A person of ordinary skill in the art also would have been motivated to retain cap layers 912 and 918 when Lan's gate conductor layers 910 and 916 are metal for the reasons I explain in the subsection immediately above. To reiterate, removing the cap layers for source/drain silicidation would be unnecessary and could damage gate conductor layers 910 and 916. (*See* Section IX.B.4.a above.)

190. A person of ordinary skill in the art would have reasonably expected success when applying Liaw's teachings to Lan because, as Liaw demonstrates, doing so requires no structural or process changes other than simply retaining Lan's cap layers. (*See* Liaw at 4:63-5:23, 6:16-42, FIGS. 3B, 5.) In fact, as I explain above, Liaw's gate structure is what a person of ordinary skill in the art would have envisioned when Lan states that the gate conductor may be a metal, and Liaw discloses cap layer materials consistent with Lan's requirement to provide selectivity over the substrate during source/drain recess etching. (*See* Lan at 3:48-54, 5:58-60.)

191. Applying the legal standards explained to me, as summarized above in Section IV.B, it is my opinion that a person of ordinary skill in the art would have viewed the combination of Lan and Liaw described above to be: (1) a simple adoption of one disclosed element (a metal gate conductor) instead of another (a polysilicon gate conductor) to obtain predictable results; (2) using a known technique (using a cap layer to protect a metal gate conductor) to improve similar devices in the same way; (3) applying a known technique (using a cap layer to protect

a metal gate conductor) to a known device ready for improvement to yield predictable results; and (4) a teaching, suggestion, or motivation in the prior art (Liaw's teachings to use a metal gate conductor in a device like Lan's) that would have led one of ordinary skill to modify Lan to arrive at the claimed invention.

192. In Lan's metal-gate embodiment (*see* Lan at 5:58-60), retaining Lan's cap layers according to Liaw's teachings (*see* Liaw at 4:63-5:23), cap layers 912 and 918 are positioned on Lan's metal layers 910 and 916, as Fig. 12 shows below. Accordingly, a person of ordinary skill in the art would have found it obvious, as in the combination of Lan and Liaw, to implement Lan's device structure with a cap layer (e.g., Lan's cap layers 912 and 918) positioned on the conductive layer (e.g., Lan's metal gate layers 910 and 916).



Lan, Fig. 12 (excerpted)

C. Grounds 2A and 2B: Wang407 Anticipates (Ground 2A) or at Least Renders Obvious (Ground 2B) Claims 1 and 3-11

193. Wang407 teaches, suggests, and renders obvious all the elements of claims 1 and 3-11 of the '847 Patent.

194. Through the analysis below, I conclude that Wang407 anticipates claims 1 and 3-11 (Ground 2A) because Wang407 discloses every limitation of those claims when viewed from the perspective of a person of ordinary skill in the art.

195. For the same reasons stated in my analysis below, I also conclude that Wang407 renders claims 1 and 3-11 obvious (Ground 2B) because the differences between claims 1 and 3-11 and Wang407 are such that claims 1 and 3-11 would have been obvious to a person of ordinary skill in the art.

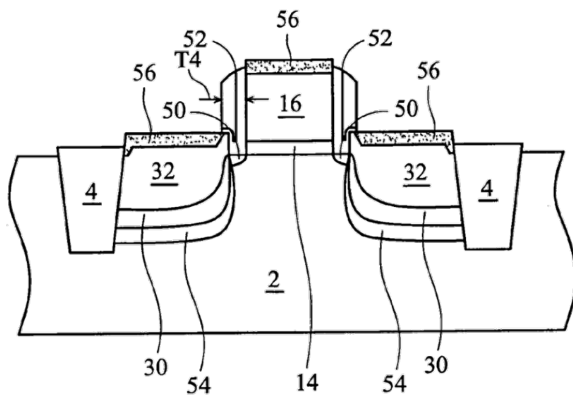
1. Independent Claim 1

a. [1pre]: “[a] MOS transistor structure”

196. Wang407 discloses “[a] MOS transistor structure,” as recited in [1pre].

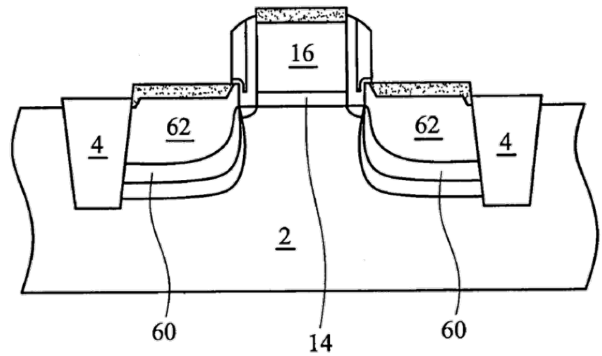
197. Wang407 discloses methods “for forming stressors in metal-oxide-semiconductor (MOS) devices,” such as the PMOS and NMOS devices shown in Figs. 9 and 11 below. (Wang407 at 3:15-16; *see also* Wang407 at 1:7-9, 2:59-3:2, 3:15-22, 5:58-62, Figs. 1-11.)

**MOS transistor structure
(PMOS)**



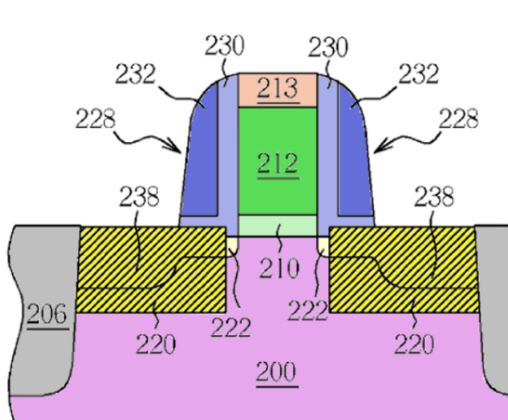
Wang407, Fig. 9 (annotated)

**MOS transistor structure
(NMOS)**

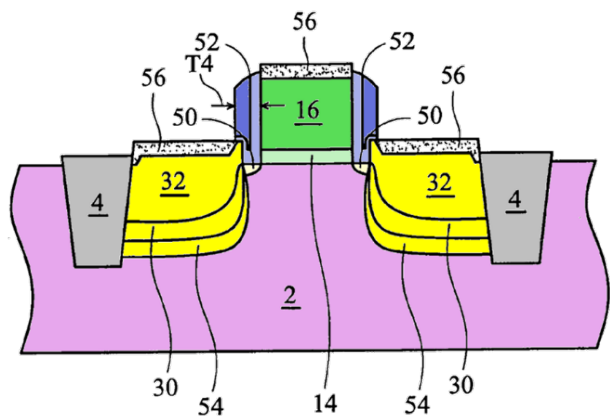


Wang407, Fig. 11 (annotated)

198. Based on my review Wang407 and the devices in the '847 patent have very similar structures. The figure below compares one of Wang407's transistors with one in the '847 patent. As shown, Wang407's device has the same basic arrangement as the one from '847 Patent describes. For example, both include the same arrangement of gate, spacers, source/drain epitaxy layers, lightly doped regions, and substrate.



'847 Patent, Fig. 5 (excerpted)



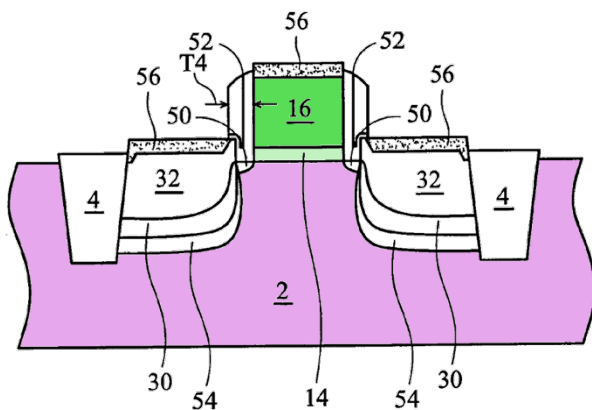
Wang407, Fig. 9

b. [1a]: “a gate formed on a semiconductor substrate”

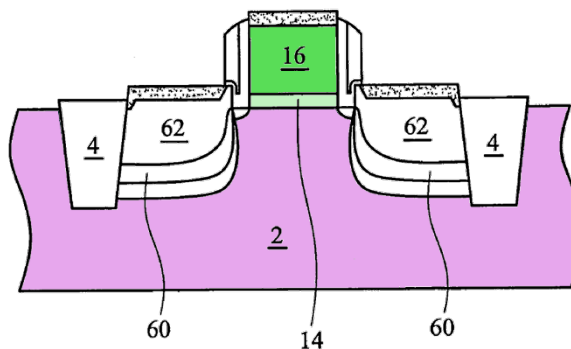
199. Wang407’s MOS transistor structures include “a gate formed on a semiconductor substrate,” as recited in [1a].

200. Wang407 discloses “[a] gate stack 12 comprising a gate dielectric 14 [and] a gate electrode 16 ... formed on substrate 2.” (Wang407 at 3:31-33.) Substrate 2 may be “bulk silicon,” for example, which is a semiconductor substrate. (Wang407 at 3:23-25.)

201. Accordingly, Wang407 discloses a gate (e.g., gate stack 12 comprising gate dielectric 14 and gate electrode 16) formed on a semiconductor substrate (e.g., substrate 2), as Figs. 9 and 11 show below.



Wang407, Fig. 9 (PMOS)



Wang407, Fig. 11 (NMOS)

c. [1b]: “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate”

202. Wang⁴⁰⁷ discloses (Ground 2A), and at least renders obvious (Ground 2B), that its MOS transistor structures include “two raised epitaxial layers

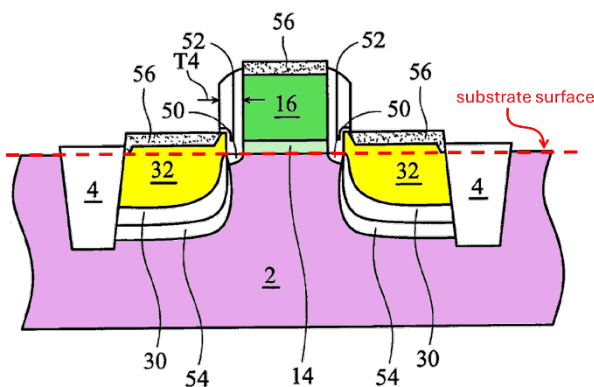
positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate,” as recited in [1b].

203. Wang407’s structures include “SiGe regions 30” and “SiGe regions 32” (PMOS) and “SiC regions 60” and “SiC regions 62” (NMOS). (Wang407 at 4:34-38, 5:60-65.) According to Wang407, these regions comprise epitaxial layers. A person of ordinary skill in the art would have understood epitaxial growth refers to crystal growth. For example, Wang407 describes “process conditions for epitaxial growth . . . to form [PMOS] SiGe regions 32.” (Wang407 at 4:34-38.) It also explains how the same concept “may also be used with the formation of NMOS” using SiC, and it describes the SiC “lattice constant” (Wang407 at 5:58-67), which a person of ordinary skill in the art would have understood refers to the atomic spacing in a crystal lattice. Wang407’s SiGe regions 30 and 32 and SiC regions 60 and 62 are thus epitaxial layers.

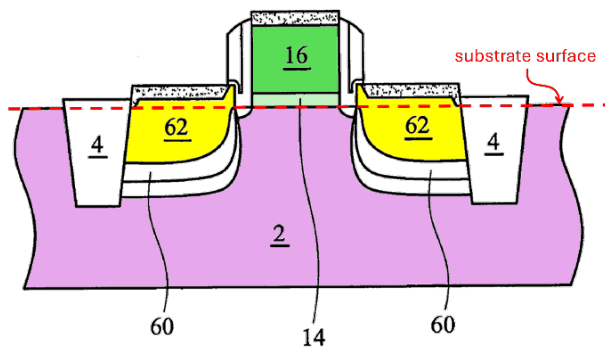
204. Wang407 also explains that these epitaxial SiGe and SiC regions are grown in recesses etched into the substrate next to the sides of the gates. Wang407, 3:63-4:6 (“[R]ecesses 26 are formed along the edges of dummy spacers 24, preferably by isotropically or anisotropically etching substrate 2. . . . FIG. 6 illustrates the formation of epitaxy regions 30, often referred to as SiGe stressors or regions, preferably by selective epitaxial growth (SEG) in recesses 26.”), 4:33-38 (“After the formation of SiGe regions 30, process conditions for epitaxial growth are

changed to form SiGe regions 32 on SiGe regions 30 . . .”), 5:47-60 (“The concept of the preferred embodiments of the present invention may also be used with the formation of NMOS devices.”), Figs. 5-7.) Wang407 describes the resulting structures in the cross-sectional figure of Figs. 9 and 11, reproduced and annotated below.

205. As Figs. 9 and 11 below illustrate, a person of ordinary skill in the art would have understood (Ground 2A), and at least found obvious (Ground 2B), that SiGe and SiC regions (highlighted in yellow) each have the structure recited in [1b]. For example, each of regions 32 and 62 (and also the combined regions 30+32 and 60+62) constitute a pair of raised epitaxial layers positioned (A) in the substrate (substrate 2); (B) next to the relative sides of the gate stack (gate stack 12 comprising gate dielectric 14 and gate electrode 16); and (C) above the surface of the substrate (substrate 2) (as annotated in red). (See Wang407 at Figs. 9, 11.)



Wang407, Fig. 9 (annotated, PMOS)



Wang407, Fig. 11 (annotated, NMOS)

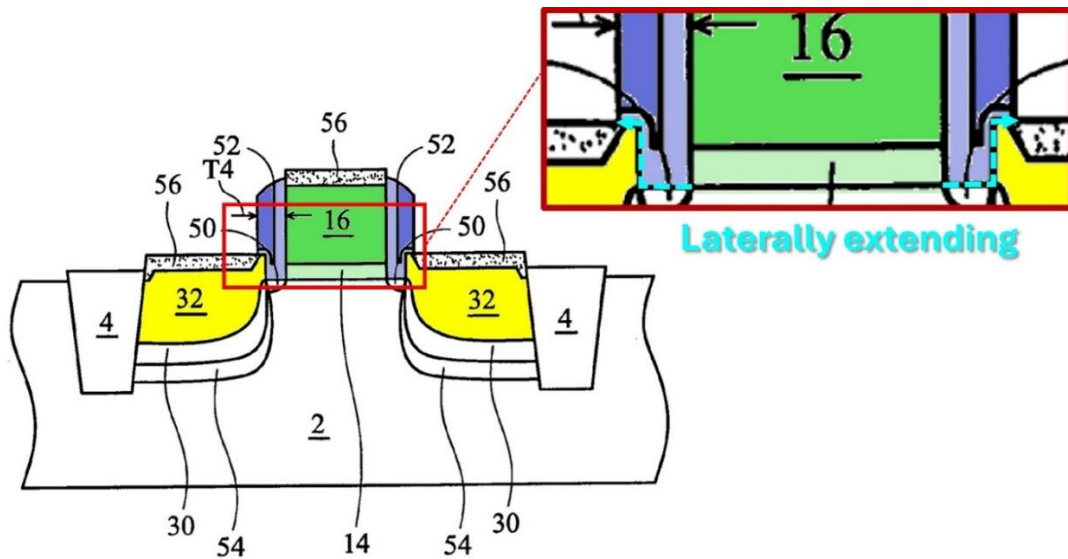
206. Further, a person of ordinary skill in the art would have understood that having the epitaxy layers above the surface of the substrate (as Wang407 shows) was a typical and expected feature of the prior art strained channel technology. As I discuss in Section VI.B, raised source/drain epitaxy was well known and common in devices incorporating epitaxial source/drain stressors. The epitaxial layers grow in substrate recesses and protrude above the substrate to reduce contact resistance and ensure adequate strain transfer to the channel region. (As just a few examples, from which I reproduce images in Section IX.A.1.c above, *see* James at 2, Fig. 6; Thompson at 1790-93, Figs. 2-5; Ghani at 978, Figs. 1-4; Bai at 657-58, Fig. 4; Wang906 ¶¶[0030]-[0032], FIG. 9; Bohr at FIGS. 4-7; Kavalieros at Abstract, ¶[0025], ¶[0043], FIGS. 5, 13.)

d. [1c]: “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer”

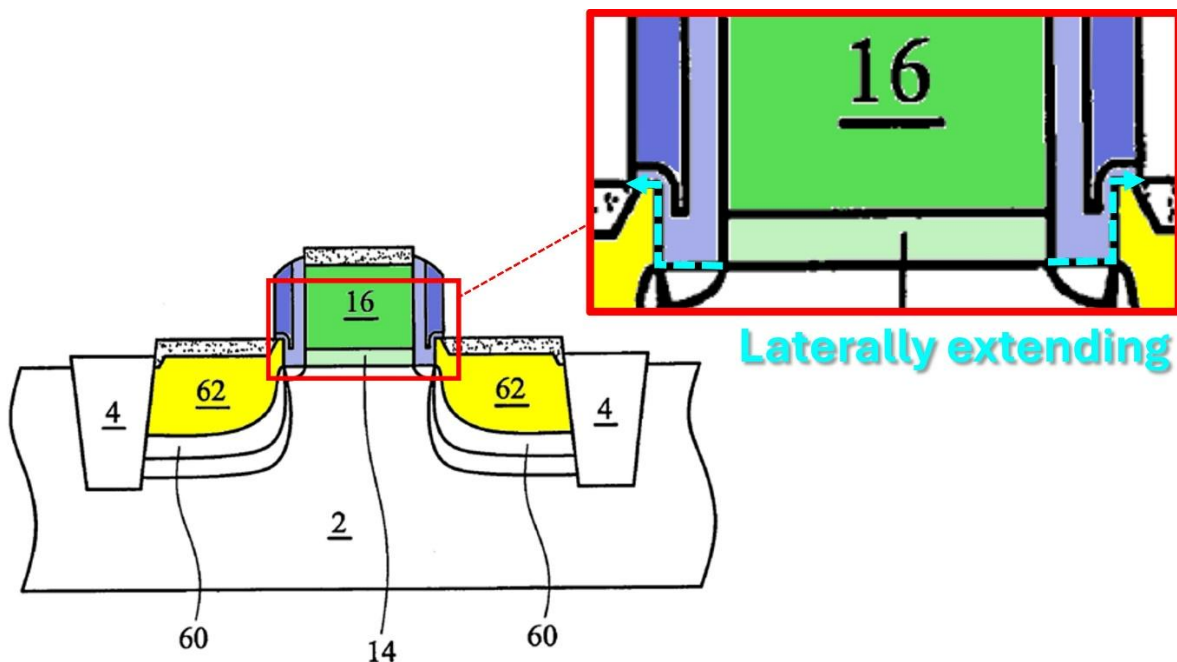
207. Wang407 discloses “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer,” as recited in [1c].

208. Wang407 discloses “a liner oxide layer and a nitride layer [that] are blanket formed” and “then patterned to form spacers 52.” (Wang407 at 4:61-64.) As Figs. 9 and 11 show below (in which I have magnified the bottom of the spacers 52 and colored the two different layers dark and light purple), a person of ordinary skill in the art would have understood that Wang407’s spacers 52 are (A) formed on the

sidewall of the gate (gate stack 12 comprising gate dielectric 14 and gate electrode 16) and (B) extend laterally upon a portion of the raised epitaxial layer (SiGe region 32 and SiC region 62).

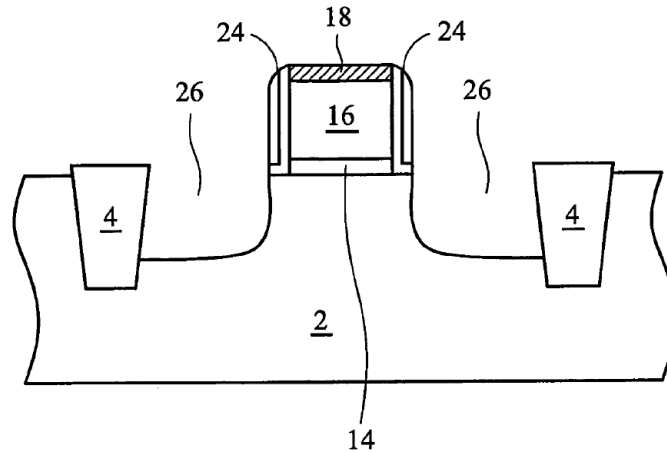


Wang407, Fig. 9 (annotated & magnified)



Wang407, Fig. 11 (annotated & magnified)

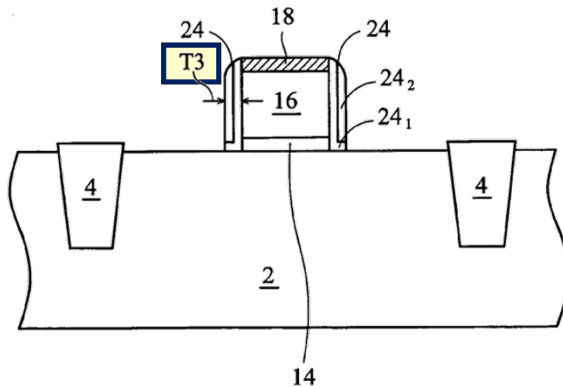
209. Wang407 explains that recesses 26 (shown in Fig. 5), where epitaxial growth of SiGe regions 30/32 and SiC regions 60/62 takes place, “are formed along the edges of dummy spacers.” (Wang407 at 3:63-65; *see also* Wang407 at 4:33-40, Figs. 5-7.)



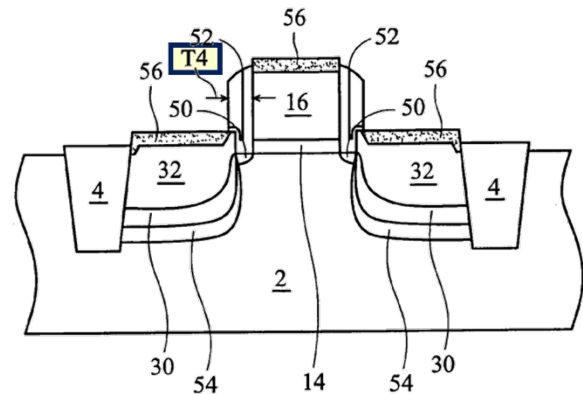
Wang407, Fig. 5

210. Wang407 further discloses that dummy spacers 24 have a thickness T3, as Fig. 4 shows below. (Wang at 4:64-67.) Because “recesses 26 are formed along the edges of dummy spacers 24,” SiGe regions 30/32 and SiC regions 60/62 are spaced a distance T3 away from the sidewalls of gate stack 12. (Wang407 at 3:63-65, Figs. 4-9.) Subsequently, those dummy spacers “are removed.” (Wang407 at 4:49-54.) After ion implantation, new spacers 52 “are formed.” (Wang407 at 4:61-67.) “[S]pacers 52 have a thickness T4 greater than a thickness T3 of dummy spacers 24.” (Wang407 at 4:64-67.) Wang407’s Fig. 9 shows the thicknesses T4 of spacers 52. Because T4 is **greater** than the T3, a person of ordinary skill in the art

would have understood Wang407's fabrication process necessary results in spacers 52 extending laterally onto a portion of SiGe regions 32 and SiC regions 62.



Wang407, Fig. 4



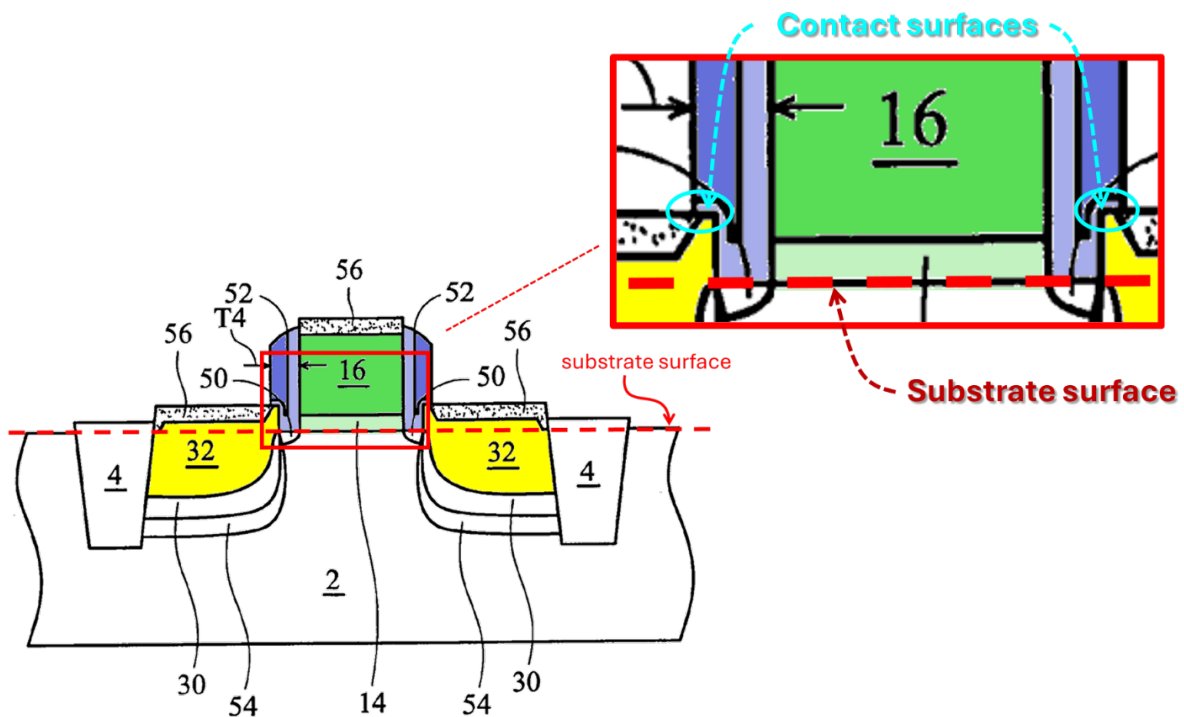
Wang407, Fig. 9

- e. [1d]: “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate”

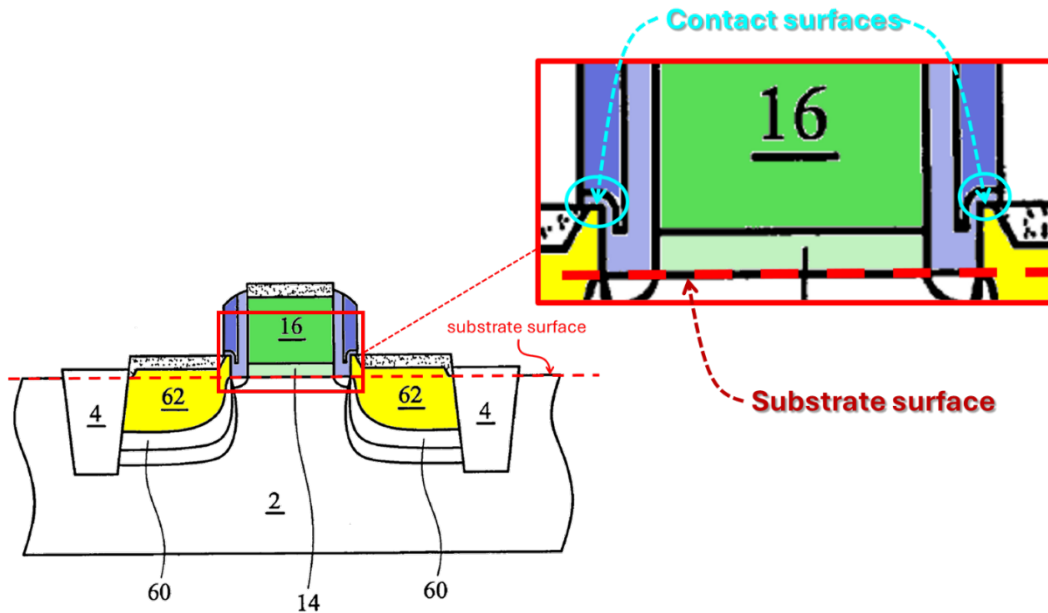
211. Wang407 discloses (Ground 2A), and at least renders obvious (Ground 2B), that “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate,” as recited in [1d].

212. As I explain in Section IX.C.1.d above for [1c], Wang407's spacers 52 extend onto a portion of SiGe regions 32 and SiC regions 62. As evident from the cross-sectional figures in Figs. 9 and 11, the bottom surfaces of spacers 52 and top surfaces of SiGe regions 32 and SiC regions 62 intersect to define contact surfaces, each having a width equal to approximately $T4 - T3$. (See Wang407 at 4:64-67, Figs. 4-7, 9, 11.) As I explain in section IX.C.1.c above for [1b], a person of ordinary

skill in the art would have understood (Ground 2A), and at least found obvious (Ground 2B), that Wang407's SiGe regions 32 and SiC regions 62 also protrude and extend above the substrate surface. From this, as annotated Figs. 9 and 11 confirm below, a person of ordinary skill in the art would have understood (Ground 2A), and at least found obvious (Ground 2B), that contact surfaces between the epitaxial layers (e.g., SiGe regions 32 or SiC regions 62) and a bottom of the spacer (e.g., spacers 52) lie above the surface of the semiconductor substrate (substrate 2).



Wang407, Fig. 9 (annotated & magnified)



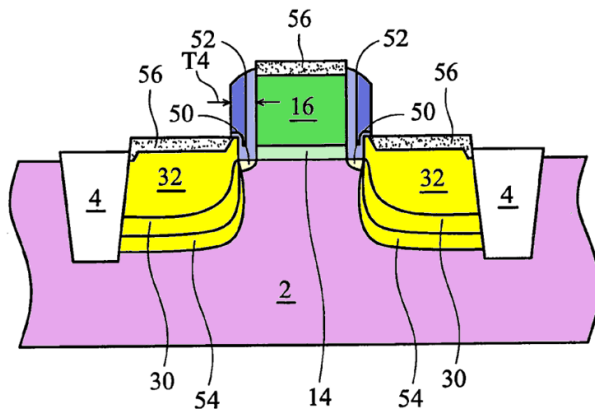
Wang407, Fig. 11 (annotated & magnified)

213. Further, although Wang407 describes forming “silicide regions 56” on SiGe regions 32 and SiC regions 62, Wang407 discloses (both in the drawings and in the text) that the silicide is formed only on their “exposed surfaces”—i.e., not on the contact surfaces indicated above. (Wang407 at 5:3-7; *see also* Wang407 at Figs. 9, 11.) As I explain in Section IX.B.4.a above, silicides are formed by placing a metal layer in contact with a semiconductor region and annealing. (Quirk at 311-12, Fig. 12.13.) Wang407’s spacers 52 shield the contact surfaces from the silicide metal layer, as Figs. 9 and 11 indicate. (*See* Quirk at 312, Fig. 12.13.)

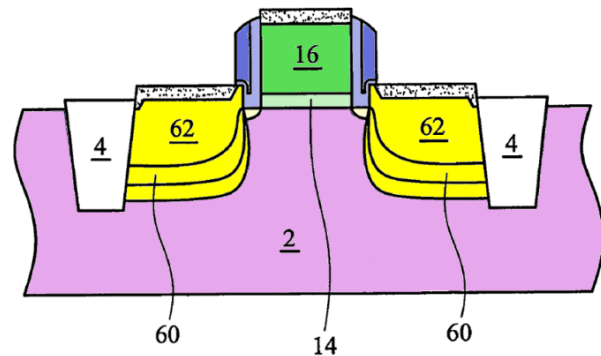
- f. [1e]: “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate”**

214. Wang407 discloses “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate,” as recited in [1e].

215. Wang407's PMOS transistors include source/drain regions with various parts on both sides of the PMOS gate stack: SiGe epitaxy regions 30 and 32 (Wang407 at 4:4-6, 4:34-38), lightly doped source/drain (LDD) regions 50 (Wang407 at 4:55-58), and deep source/drain regions 54 (Wang407 at 5:1-3). (*See also* Wang407 at Figs. 8-9.) A person of ordinary skill in the art would have understood that the NMOS transistors are the same, except they contain SiC epitaxy regions 60 and 62, and the doping type would be the opposite. (*See* Wang407 at (explaining the same concept "may also be used with the formation of NMOS").)



Wang407, Fig. 9

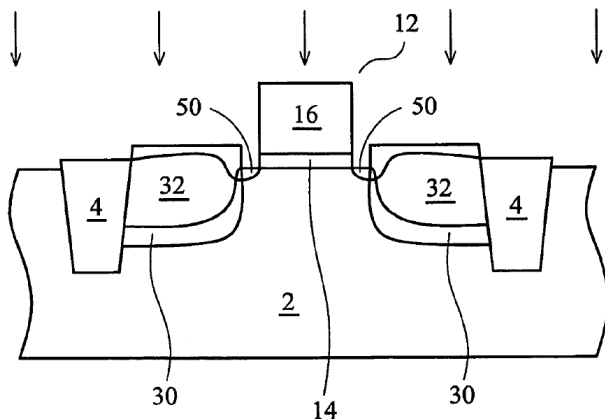


Wang407, Fig. 11

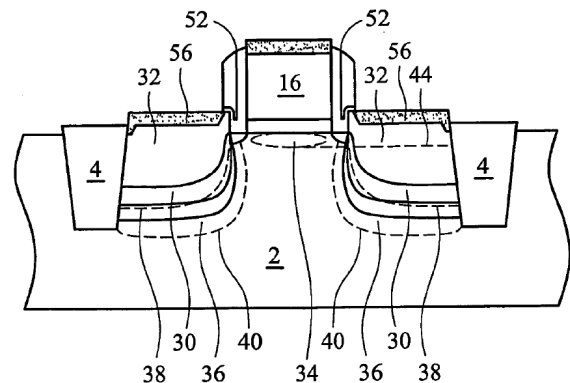
216. Wang407's LDD regions 50 and deep source/drain regions 54 are formed by implanting p-type impurities. (Wang407 at 4:55-56, 5:1-3.) These regions extend beyond SiGe epitaxial regions 30 and 32 into substrate 2, as Fig. 9 shows above. LDD regions 50, for example, are implanted immediately next to the gate stack. (Wang407 at 4:56-58 ("LDD regions 50 are substantially aligned with the respective edge of gate stack 12."); *see also* Wang407 at Fig. 8.) Although not

labeled in Fig. 11, Wang407 explains that the same concepts “may also be used with the formation of NMOS devices.” (Wang407 at 5:58-62; *see also* Wang407 at claims 6, 13.)

217. Wang407’s LDD regions 50 are formed after dummy spacers 24 have been removed, as in Fig. 8 below. (*See* Wang407 at 4:49-58.) When implanting the LDD p-type dopants, only “[g]ate stack 12 acts as a mask,” such that LDD regions 50 form in both SiGe epitaxial regions 32 and substrate 2. (Wang407 at 4:56-58.) After forming spacers 52 in Wang407, deep source/drain regions 54 are formed by implanting p-type impurities into SiGe epitaxial regions 30 and 32 and portions of substrate 2 underneath, as Fig. 9 illustrates above. (*See* Wang407 at 5:1-3.)



Wang407, Fig. 8



Wang407, Fig. 10

218. Wang407’s Fig. 10 describes the effects of this source/drain configuration. (*See* Wang407 at 5:13-46.) A person of ordinary skill in the art would have understood that depletion regions 36 between dotted lines 38 and 40 are characteristic of MOSFET source/drain regions, forming near the boundary between

the source/drain regions and the rest of the substrate. (*See* Sze at 438-39, Fig. 6; Wolf2 at 338-39, Fig. 5-17; Wolf3 at 232-34, Figs. 5-21, 5-22.)

219. From these various disclosures, a person of ordinary skill in the art would have understood that Wang407 discloses two doped regions (e.g., LDD regions 50 and/or deep source/drain regions 54) formed respectively in the semiconductor substrate (substrate 2) next to the relative sides of the gate (gate stack 12 comprising gate dielectric 14 and gate electrode 16).

220. Additionally, if a doped epitaxial region qualifies as a “doped region formed . . . in the semiconductor substrate,” then any combination of Wang407’s epitaxial source/drain regions 32/62, LDD regions 50, and/or the deep source/drain regions 54 would qualify as the claimed “two doped regions” in [1e]. Like LDD regions 50 and deep source/drain regions 54, Wang407’s epitaxial SiGe regions 30/32 and SiC regions 60/62 are doped and formed next to the relative sides of the gate, as Figs. 9 and 11 show above. (*See* Wang407 at 3:63-65, 4:33-40, Figs. 5-9, 11.)

2. Dependent Claims

a. Claim 3: “The structure of claim 1, wherein the MOS transistor comprises a PMOS transistor.”

221. As I explain in Section IX.C.1, Wang407 discloses and renders obvious the structure of claim 1.

222. Wang407 also discloses the structure “wherein the MOS transistor comprises a PMOS transistor,” as recited in claim 3.

223. Wang407 discloses that the embodiment in Fig. 9 is a PMOS transistor. Specifically, it discloses that “FIGS. 1 through 9 are cross-sectional views of intermediate stages in the manufacture of a *PMOS* embodiment.” (Wang407 at 2:63-64 (emphasis added).) Wang407 also claims a “semiconductor device [that] comprises a *PMOS* device.” (Wang407 at claims 8, 18 (emphasis added).)

b. Claim 4: “The structure of claim 3, wherein the epitaxial layer comprises SiGe.”

224. As I explain in Section IX.C.2.a, Wang407 discloses and renders obvious the structure of claim 3.

225. Wang407 also discloses the structure “wherein the epitaxial layer comprises SiGe,” as recited in claim 4.

226. Wang407 discloses that the PMOS epitaxial layer in Fig. 9 (e.g., SiGe regions 32) comprises SiGe. (Wang407 at 4:4-6, 4:34-38.) As I explain in Section VI.B, SiGe was frequently used to strain the channel of PMOS devices. Because Ge atoms are bigger than Si atoms and SiGe has a larger lattice constant than Si, SiGe compressively strains the Si channel. Wang407 expressly discusses this as well: “A commonly used method for applying compressive stress to the channel regions of PMOS devices is to grow SiGe stressors in the source and drain regions.” (Wang407 at 1:36-38.)

c. Claim 5: “The structure of claim 1, wherein the MOS transistor comprises an NMOS transistor.”

227. As I explain in Section IX.C.1, Wang407 discloses and renders obvious the structure of claim 1.

228. Wang407 also discloses the structure “wherein the MOS transistor comprises a NMOS transistor,” as recited in claim 5.

229. Wang407 discloses that the embodiment in Fig. 11 is an NMOS transistor. Wang407 states that “FIG. 11 illustrates an *NMOS* device.” (Wang407 at 5:60-62 (emphasis added).) Wang407 also claims a “semiconductor device [that] comprises a *NMOS* device.” (Wang407 at claims 9, 19.)

d. Claim 6: “The structure of claim 5, wherein the epitaxial layer comprises SiC.”

230. As I explain in section IX.C.2.c, Wang407 discloses and renders obvious the structure of claim 5.

231. Wang407 also discloses the structure “wherein the epitaxial layer comprises SiC,” as recited in claim 6.

232. Wang407 discloses that the NMOS epitaxial layer in Fig. 11 (e.g., SiC regions 62) comprises SiC. (Wang407 at 5:60-67.) As I explain in Section VI.B, SiC was used to strain the channel of NMOS devices. Because C atoms are smaller than Si and SiC has a smaller lattice constant than Si, SiC creates tensile strain in the Si channel. Wang407 expressly discusses this as well: “[S]tresses can be introduced

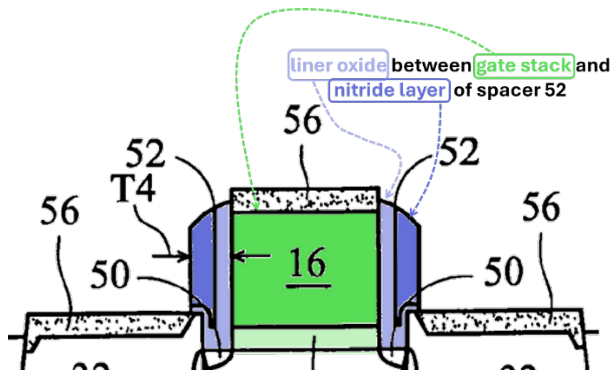
to the channel regions of NMOS devices by forming SiC stressors. Since SiC has a smaller lattice constant than silicon has, it contracts after annealing and applies a tensile stress to the channel region.” (Wang407 at 1:47-51.)

e. Claim 7: “The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.”

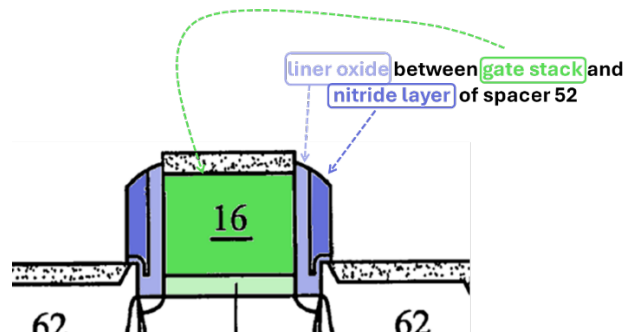
233. As I explain in section IX.C.1, Wang407 discloses and renders obvious the structure of claim 1.

234. For the reasons I explain in section VII.C, here I analyze claim 7 assuming that the claim can be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the claimed “gate.” Under such interpretation, Wang407 discloses claim 7.

235. Wang407’s spacer (spacer 52) comprises “a liner oxide layer and a nitride layer.” (Wang407 at 4:61-64.) “Preferably, a liner oxide layer and a nitride layer are blanket formed. The liner oxide layer and the nitride layer are then patterned to form spacers 52.” (Wang407 at 4:61-64.) Wang407 thus discloses an offset spacer (liner oxide of spacer 52) positioned between the gate (gate stack 12 comprising gate dielectric 14 and gate electrode 16) and another portion of the “spacer” (nitride layer of spacer 52), as Figs. 9 and 11 show.



Wang407, Fig. 9 (excerpted)



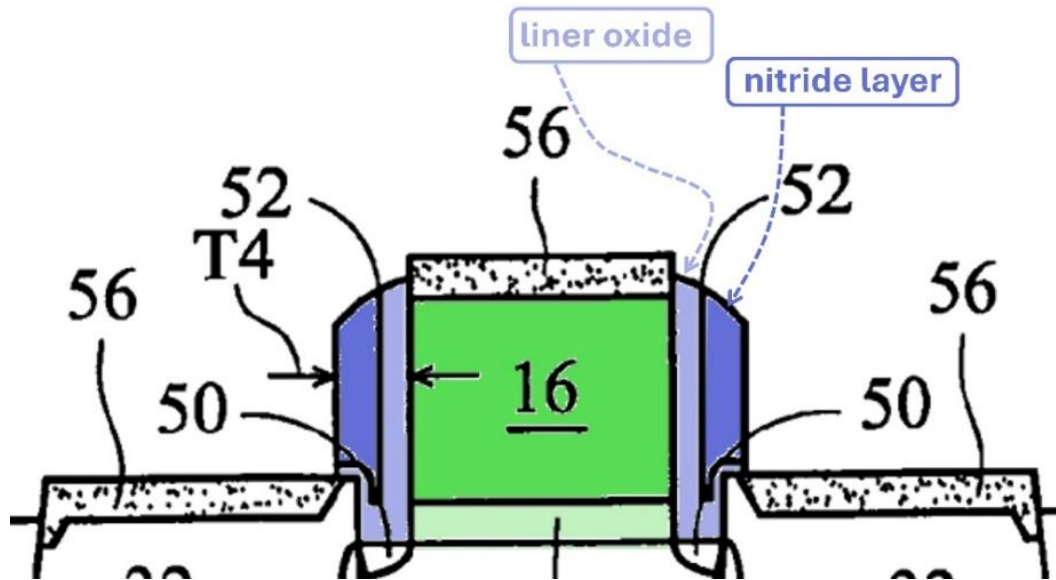
Wang407, Fig. 11 (excerpted)

- f. **Claim 8: “The structure of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.”**

236. As I explain in section IX.C.1, Wang407 discloses and renders obvious the structure of claim 1.

237. Wang407 also discloses the structure “wherein the spacer further comprises an oxide liner and a nitride spacer,” as recited in claim 8.

238. Wang407’s spacer (spacer 52) comprises “a liner oxide layer and a nitride layer.” (Wang407 at 4:61-64.) “Preferably, a liner oxide layer and a nitride layer are blanket formed. The liner oxide layer and the nitride layer are then patterned to form spacers 52.” (Wang407 at 4:61-64.) Therefore, Wang407’s spacer (spacer 52) comprises an oxide liner (liner oxide layer) and a nitride spacer (nitride layer), as Figs. 9 and 11 show.



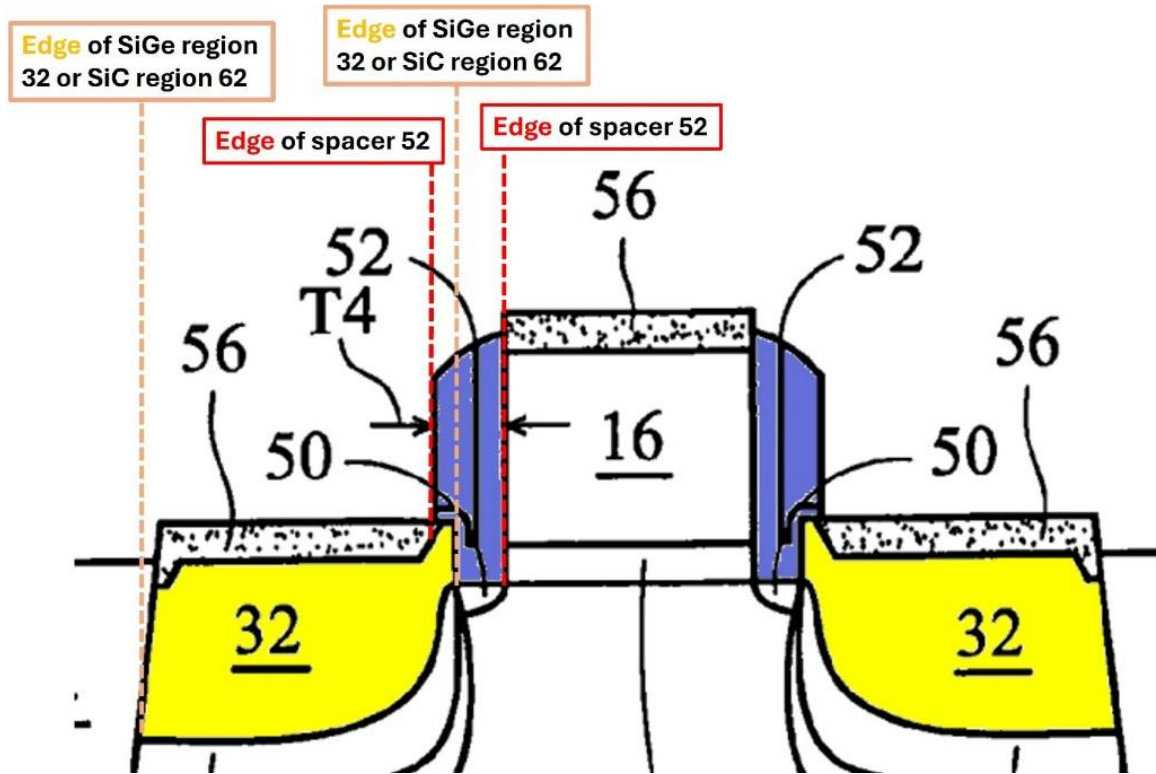
Wang407, Fig. 9 (excerpted)

- g. **Claim 9: “The structure of claim 1, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.”**

239. As I explain in section IX.C.1, Wang407 discloses and renders obvious the structure of claim 1.

240. Wang407 also discloses the structure “wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer,” as recited in claim 9.

241. In Wang407’s device the edges of the raised epitaxial layers (e.g., SiGe regions 32 or SiC regions 62) are not aligned with the edges of Wang407’s spacers (spacers 52), as Fig. 9 shows below.



Wang407, Fig. 9 (annotated, excerpted)

242. As I explain in Section IX.C.1.d, Wang407's spacers 52 are thicker than the dummy spacers 24 used to define the location of epitaxial layers 32 and 62. As a result, spacers 52 overlap SiGe regions 32 and SiC regions 62 (by an amount approximately equal to $T4 - T3$ wide). (See Wang407 at 4:64-67.) With such a configuration, the edges of the spacers and epitaxial regions cannot be aligned, because the distance from Wang407's gate stack 12 to the edge of the spacers 52 ("T4" in Fig. 9) is necessarily larger than the distance from Wang407's gate stack 12 to the inner edge of Wang407's SiGe regions 32 or SiC regions 62 (where the sidewall of SiGe region 32 meets the spacer 52 in Fig. 9 above, which is equal to

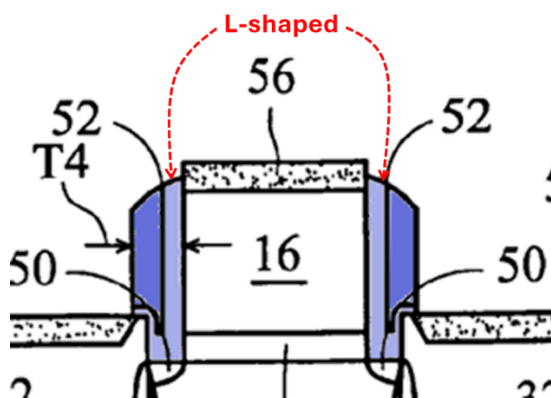
“T3” in Fig. 4). Wang407’s fabrication thus yields a MOS device structure in which the edges of SiGe regions 32 / SiC regions 62 and spacers 52 are misaligned.

h. Claim 10: “The structure of claim 1, wherein the spacer further comprises a [sic] L-shaped spacer.”

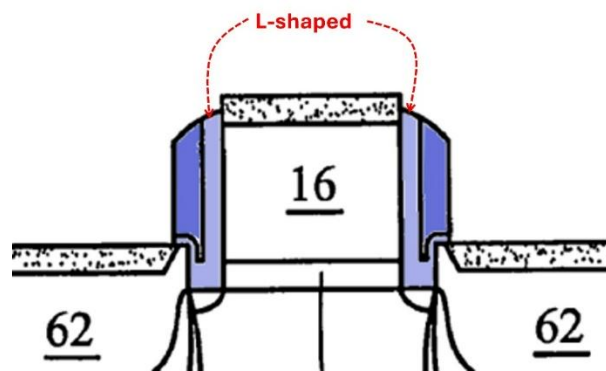
243. As I explain in section IX.C.1, Wang407 discloses and renders obvious the structure of claim 1.

244. Wang407 also discloses the structure “wherein the spacer further comprises a [sic] L-shaped spacer,” as recited in claim 10.

245. As Figs. 9 shows below, Wang407’s spacers 52 comprise an L-shaped spacer (liner oxide layer) with a vertical portion along the gate sidewall and a substantially horizontal portion along the substrate. The analogous oxide liner in Fig. 11 has a similar “L” shaped configuration. Accordingly, Wang407’s spacer (spacer 52) further comprises an L-shaped spacer (liner oxide layer).



Wang407, Fig. 9 (excerpted)



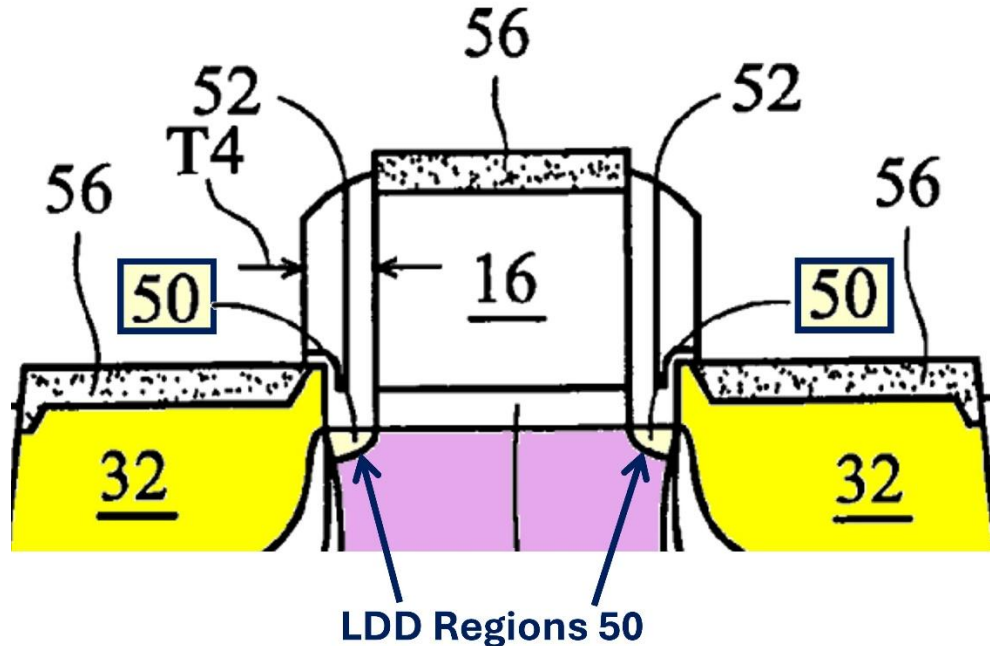
Wang407, Fig. 11(excerpted)

i. Claim 11: “The structure of claim 1, further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers.”

246. As I explain in section IX.C.1, Wang407 discloses and renders obvious the structure of claim 1.

247. Wang407 also discloses the structure “further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers,” as recited in claim 11.

248. For example, Wang407 discloses “[l]ightly doped source/drain (LDD) regions 50” formed “by implanting a p-type impurity.” (Wang407 at 4:55-56.) Wang407 explains this process takes place after dummy spacers have been removed, such that only Wang407’s “gate stack 12 acts as a mask” and “LDD regions 50 are substantially aligned with the respective edge of gate stack 12.” (Wang407 at 4:56-58, 4:49-54, Fig. 8.) This process Wang407 describes for forming LDD regions 50 (i.e., making and removing a dummy spacer to implant LDD regions outside the epitaxial source/drain regions) is the same process the ’847 Patent describes for forming its “lightly doped region.” (See ’847 Patent at 3:29-54, 6:17-26, Figs. 3-4, 11-13.) Thus, as shown in Figs. 9 below (and also in Fig. 11), Wang407 discloses a lightly doped drain (LDD regions 50) disposed in the semiconductor substrate (substrate 2) outside the raised epitaxial layers (SiGe regions 32 or SiC regions 62).



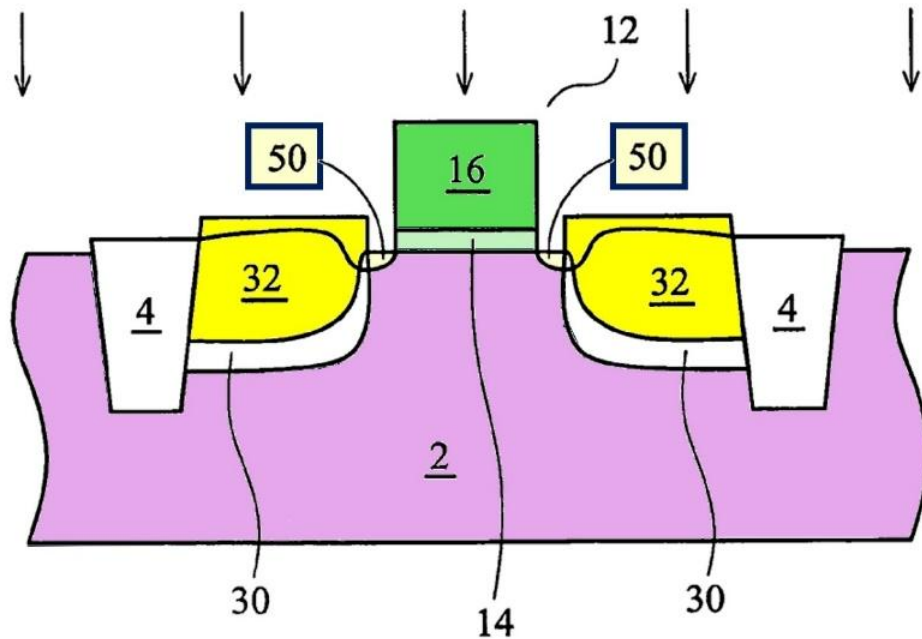
Wang407, Fig. 9 (excerpted)

249. Wang407 explains that epitaxial SiGe regions 32 and epitaxial SiC regions 62 grow selectively in recesses 26 delimited by dummy spacers 24. (See Wang407 at 3:63-65 (“[R]ecesses 26 are formed along the edges of dummy spacers 24, preferably by isotropically or anisotropically etching substrate 2.”), 4:34-48 (“SiGe regions 30 preferably only occupy bottom portions of the recesses 26. After the formation of SiGe regions 30, process conditions for epitaxial growth are changed to form SiGe regions 32 on SiGe regions 30”), Figs. 5, 7.) Removing dummy spacers 24, as Fig. 8 shows, creates a gap between the epitaxial regions and gate stack 12. (See Wang407 at 4:49-54, Fig. 8.) This exposes a portion of substrate 2 to the p-type ion implantation process used to form LDD regions 50. (See Wang407 at 4:55-58, Fig. 8.) As a result of this exposure, LDD regions 50 form

in a region that is necessarily both in substate 2 and outside of the epitaxial regions.

This is the same arrangement the '847 Patent describes for its “lightly doped region.”

(See '847 Patent at 3:29-54, 6:17-26, Figs. 3-4, 11-13.)



Wang407, Fig. 8

D. Grounds 3A and 3B: Wang753 Anticipates (Ground 3A) and Renders Obvious (Ground 3B) Claims 1 and 10

250. Wang753 teaches, suggests, and renders obvious all the elements of claims 1 and 10 of the '847 Patent.

251. Through the analysis below, I conclude that Wang753 anticipates claims 1 and 10 (Ground 3A) because Wang753 discloses every limitation of those claims when viewed from the perspective of a person of ordinary skill in the art.

252. For the same reasons stated in my analysis below, I also conclude that Wang753 renders claims 1 and 10 obvious (Ground 3B) because the differences

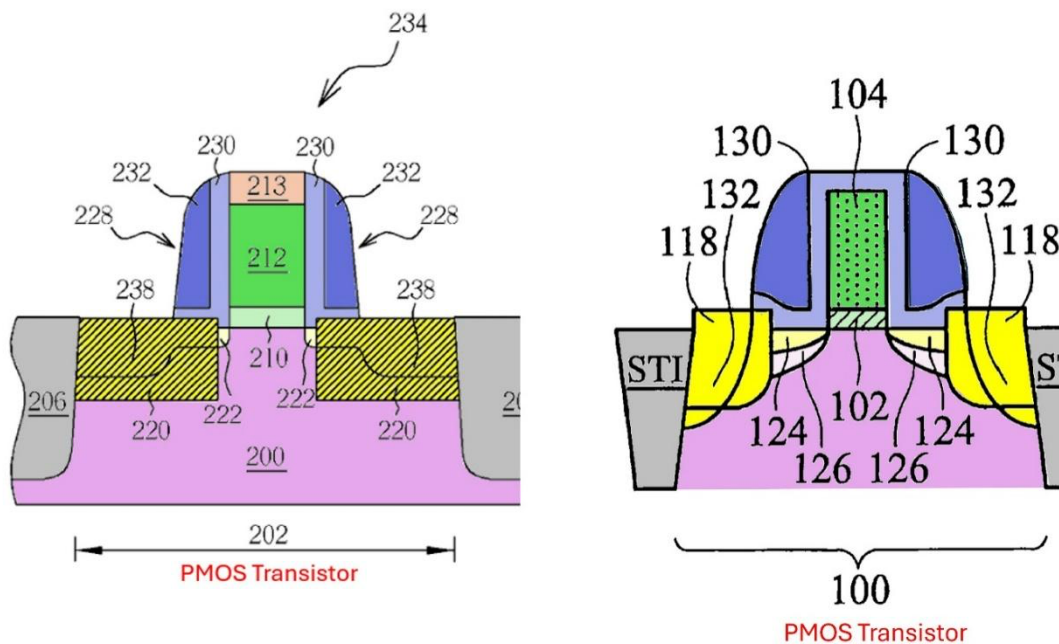
between claims 1 and 10 and Wang753 are such that claims 1 and 10 would have been obvious to a person of ordinary skill in the art.

1. Independent Claim 1

a. [1pre]: “[a] MOS transistor structure”

253. Wang753 discloses “[a] MOS transistor structure,” as recited in [1pre].

254. Wang753 discloses a semiconductor structure that “combines the formation of PMOS and NMOS devices for core circuits and SRAM cells.” (Wang753 at 3:33-36, 3:43-49, FIG. 13.) Wang753’s PMOS devices (e.g., the PMOS device in core region 100) are MOS transistor structures.



’847 Patent, Fig. 5 (PMOS excerpt) Wang753, FIG. 13^[3] (PMOS excerpt)

³ Wang753 explains that a liner oxide layer 25 (in light purple above) is “patterned to form spacers 130 . . . as shown in FIG. 11.” (Wang753 at 5:19-22.) Although it does not meaningfully affect my analysis of Wang753, liner oxide layer 25 would

255. As shown in the side-by-side comparison above, Wang's PMOS device has the same basic arrangement the '847 Patent describes. For example, both include the same basic arrangement of gate dielectric, gate electrode, spacers, source/drain epitaxy layers, lightly doped regions, and substrate.

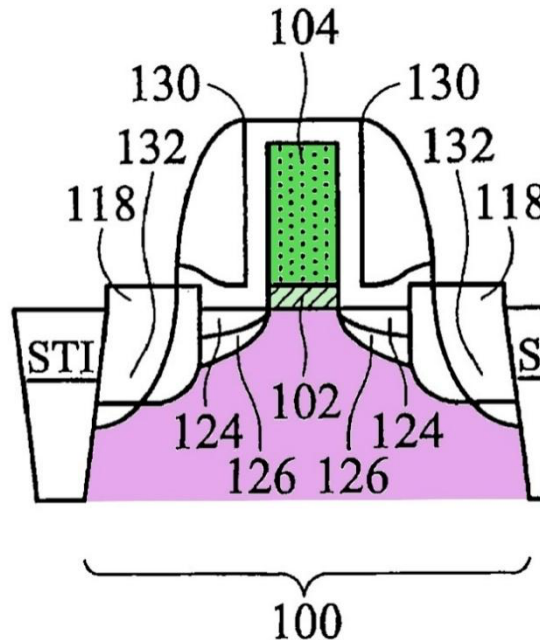
b. [1a]: "a gate formed on a semiconductor substrate"

256. Wang753 discloses "a gate formed on a semiconductor substrate," as recited in [1a].

257. Wang753's PMOS devices include "a gate stack formed on the substrate 2" (fuchsia below). (Wang753 at 3:49-52.) For example the PMOS device in core region 100, shown below in FIG. 13, includes "a gate dielectric 102 on substrate 2 and a gate electrode 104 on gate dielectric 102." (Wang753 at 3:49-52.) Wang753 explains that "[s]ubstrate 2 preferably comprises bulk silicon," which is a well-known semiconductor substrate. (Wang753 at 3:41-43.)

258. Accordingly, Wang753 discloses a gate (e.g., Wang753's "gate stack" comprising gate dielectric 102 and gate electrode 104) formed on a semiconductor substrate (silicon substrate 2).

not extend over gate electrode 104 in FIG. 13. Rather, it would appear as in Wang753's FIGS. 11 and 12. A person of ordinary skill in the art would have identified this as a drawing error in FIG. 13. (See Wang753 at 5:19-42, FIGS. 11-13.)



Wang753, FIG. 13 (excerpted)

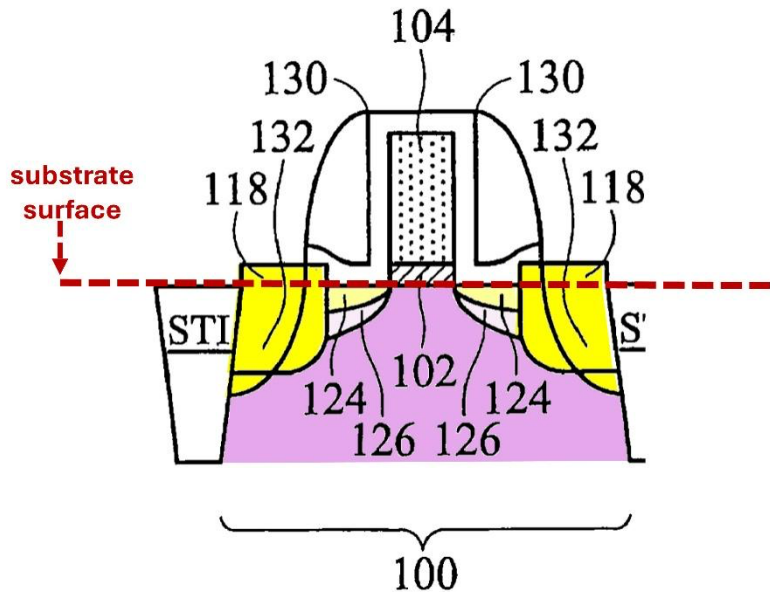
- c. [1b]: “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate”

259. Wang753 discloses (Ground 3A), and at least renders obvious (Ground 3B), “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate,” as recited in [1b].

260. Wang753’s PMOS devices include “SiGe stressors 118” in source/drain regions adjacent to the gate stack. (See Wang753 at 4:14-18.) According to Wang753, forming SiGe stressors 118 involves making “disposable spacers” (gate spacers 114, shown in Wang753’s FIG. 4) that define “recesses 116” etched in the substrate. (Wang753 at 4:10-13, 4:23-27, FIGS. 4-6.) Wang753’s

“SiGe stressors [are] epitaxially grown in the recesses 116.” (Wang753 at 4:14-17.)

As Wang753’s FIG. 13 shows, a person of ordinary skill in the art would have understood (Ground 3A), and at least found obvious (Ground 3B), that SiGe stressors 118 extend above the substrate. (Wang753 at 4:14-22.)



Wang753, FIG. 13 (excerpted, annotated)

261. Thus, Wang753 discloses (Ground 3A), and at least renders obvious (Ground 3B), two raised epitaxial layers (e.g., SiGe stressors 118) positioned respectively in the semiconductor substrate (substrate 2) next to the relative sides of the gate (e.g., Wang753’s gates stack comprising gate dielectric 102 and gate electrode 104) and above the surface of the semiconductor substrate.

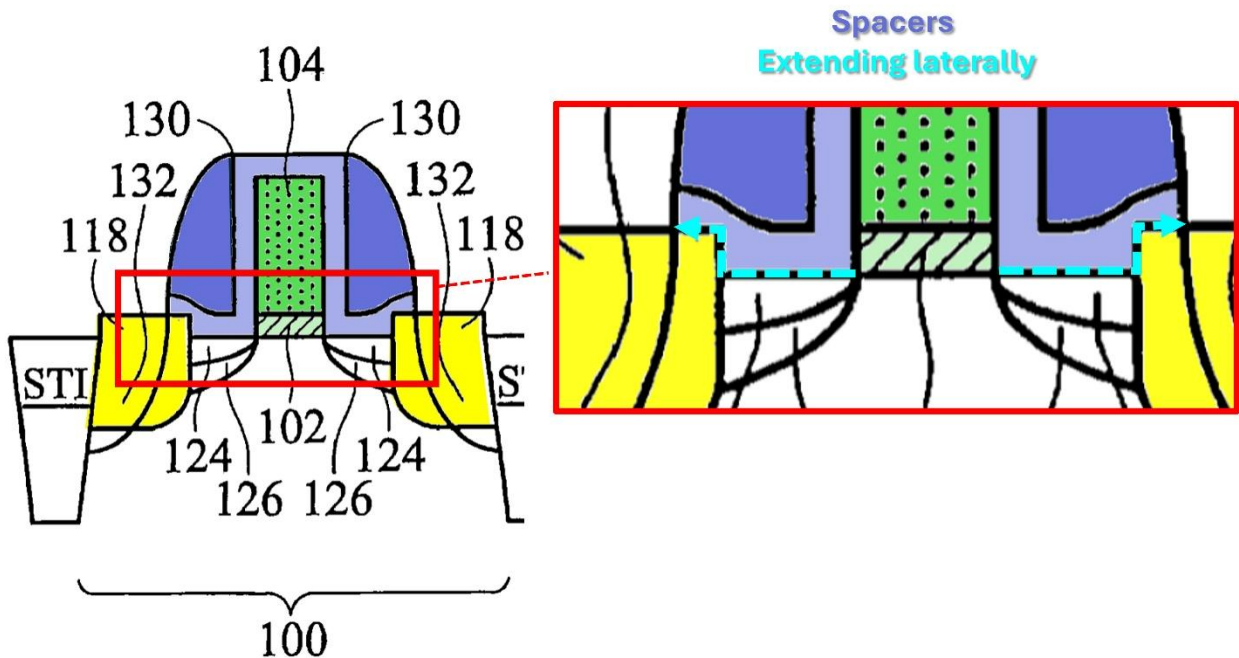
262. Further, a person of ordinary skill in the art would have understood having the epitaxy layers above the surface of the substrate (as Wang753 shows) was a typical and expected feature of the prior art strained channel technology. As I

discuss in Section VI.B, raised source/drain epitaxy was well known and common in devices incorporating epitaxial source/drain stressors. The epitaxial layers grow in substrate recesses and protrude above the substrate to reduce contact resistance and ensure adequate strain transfer to the channel region. (As just a few examples, from which I reproduce images in Section IX.A.1.c above, *see* James at 2, Fig. 6; Thompson at 1790-93, Figs. 2-5; Ghani at 978, Figs. 1-4; Bai at 657-58, Fig. 4; Wang906 ¶¶[0030]-[0032], FIG. 9; Bohr at FIGS. 4-7; Kavalieros at Abstract, ¶[0025], ¶[0043], FIGS. 5, 13.)

d. [1c]: “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer”

263. Wang753 discloses “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer,” as recited in [1c].

264. Wang753 discloses “a liner oxide layer 25 and a nitride layer 27 [that] are blanket formed” on the PMOS device. (Wang753 at 5:19-21, FIG. 10.) Wang753 further explains that “[t]he two layers are then patterned to form spacers 130 . . . as shown in FIG. 11.” (Wang753 at 5:21-22; *see also* Wang753 at FIG. 11.) According to Wang753, spacers 130 “have a thickness greater than that of” the disposable spacers 114 used to define the distance between the gate and epitaxial SiGe stressors 118. (Wang753 at 5:22-25.) “As a result, spacers 130 . . . have portions on SiGe stressors 118,” as FIG. 13 confirms below. (Wang753 at 5:25-27.)



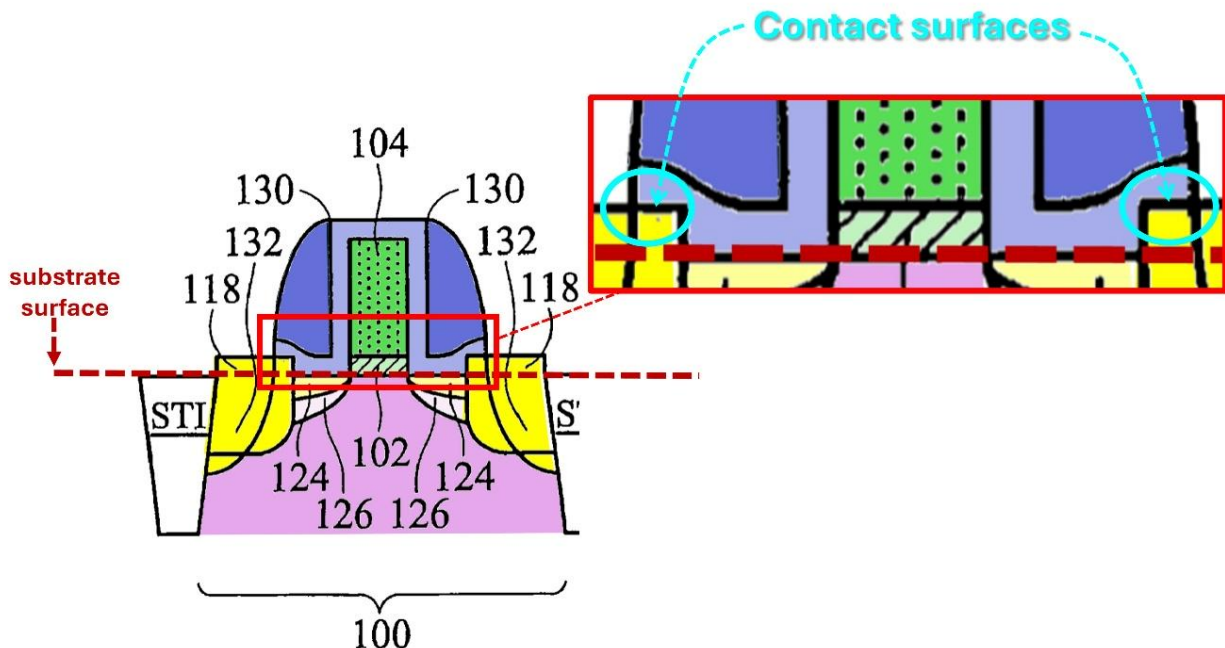
Wang753, Fig. 13 (magnified, annotated)

265. Therefore, Wang753 discloses a spacer (spacers 130) formed on the sidewall of the gate (Wang753's gate stack comprising gate dielectric 102 and gate electrode 104) and extending laterally upon a portion of the raised epitaxial layer (SiGe stressors 118 adjacent to the gate stack).

- e. [1d]: “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate”

266. Wang753 discloses (Ground 3A), and at least renders obvious (Ground 3B), “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate,” as recited in [1d].

267. As I explain in section IX.D.1.d for [1c], Wang's spacers 130 extend laterally onto a portion of SiGe stressors 118. As evident from the cross-section in FIG. 13, the bottom surfaces of spacers 130 and top surfaces of epitaxial SiGe stressors 118 intersect to define contact surfaces. (See Wang753 at FIG. 13.) As I further explain in Section IX.D.1.c for [1b], a person of ordinary skill in the art would have understood (Ground 3A), and at least found obvious (Ground 3B), that the upper surfaces of SiGe stressors 118 are above the substrate surface. Therefore, as FIG. 13 shows, those contact surfaces between the raised epitaxial layers (SiGe stressors 118) and bottom of the spacer (spacers 130) are above the semiconductor substrate surface (of substrate 2, fuchsia).



Wang753, FIG. 13 (excerpted, annotated, magnified)

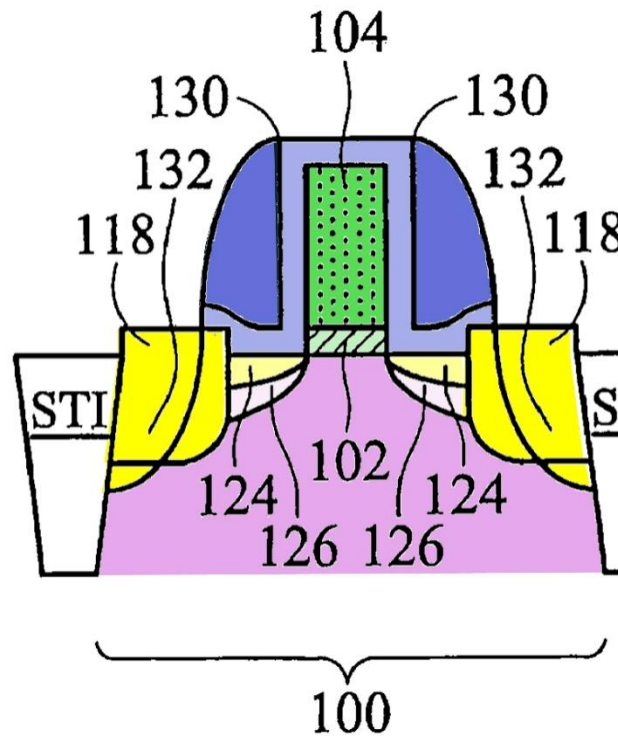
f. [1e]: “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate”

268. Wang753 discloses “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate,” as recited in [1e].

269. Wang753’s PMOS devices, such as the PMOS device in core region 100, include source/drain regions with several components on both sides of the gate stack: SiGe stressors 118, LDD regions 124, and deep source/drain regions 132. (*See* Wang753 at FIG. 13.) Wang753 explains the following:

- SiGe stressors 118 are preferably doped with “P-type impurities such as boron . . . during epitaxial growth.” (Wang753 at 4:14-18.)
- “LDD regions 124 are formed by introducing p-type impurities” into the substrate.” (Wang753 at 4:49-51; *see also* Wang753 at 4:29-37, 4:46-51, FIG. 8.)
- “[D]eep source/drain regions 132,” which are “substantially aligned with edges of the spacers 130,” are formed by “implanting p-type impurities.” (Wang753 at 5:36-42.)

As FIG. 13 shows below, Wang753’s LDD regions 124, for example, lie next to the gate stack (light and dark green). They are also “substantially aligned with the edges of the gate electrodes.” (Wang753 at 4:34-36.)



Wang753, FIG. 13 (excerpted)

270. Therefore, Wang753 discloses two doped regions (e.g., LDD regions 124) formed respectively in the semiconductor substrate (substrate 2) next to the relative sides of the gate (Wang753's gate stack comprising gate dielectric 102 and gate electrode 104).

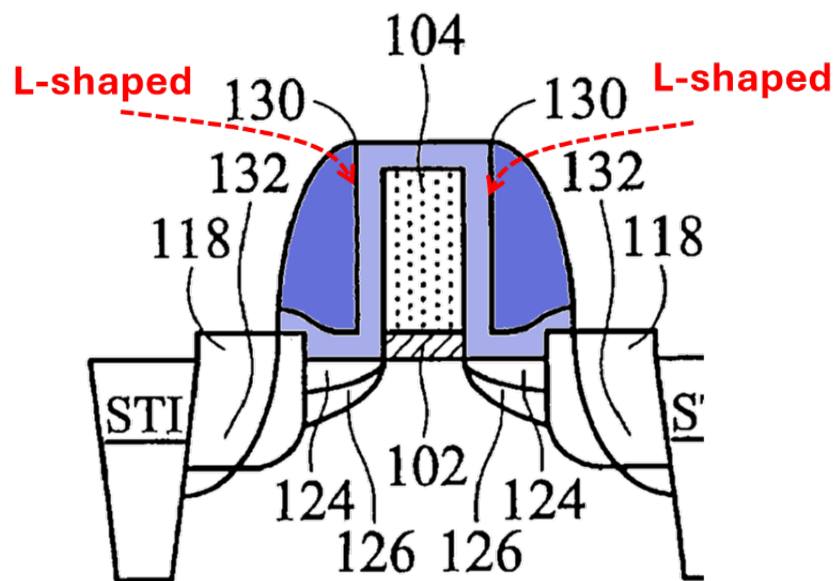
271. Additionally, if a doped epitaxial region qualifies as a "doped region formed ... in the semiconductor substrate," then any combination of SiGe stressors 118, LDD regions 124, and/or deep source/drain regions 132 would qualify as the claimed "two doped regions" in [1e]. As FIG. 13 confirms, SiGe stressors 118, LDD regions 124, and deep source/drain regions 132 all are formed next to the relative sides of Wang753's gate stack.

2. Dependent Claim 10: “The structure of claim 1, wherein the spacer further comprises a [sic] L-shaped spacer.”

272. As I explain in section IX.D.1, Wang753 discloses and renders obvious the structure of claim 1.

273. Wang753 also discloses (Ground 3A) and renders obvious (Ground 3B), the structure “wherein the spacer further comprises a [sic] L-shaped spacer,” as recited in claim 10.

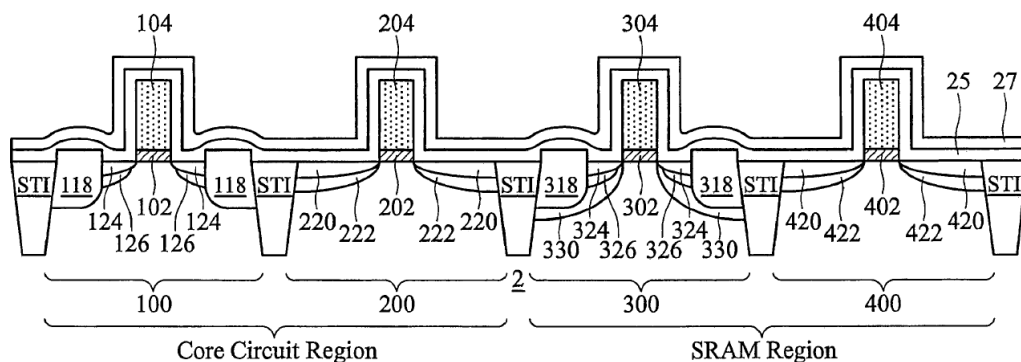
274. As FIG. 13 shows below, a person of ordinary skill in the art would have understood (Ground 3A), and at least found obvious (Ground 3B), that spacers 130 include an L-shaped “liner oxide layer 25” (light purple) with a vertical portion along the sidewall of the gate stack and a substantially horizontal portion along the substrate. (See Wang753 at FIG. 13.)



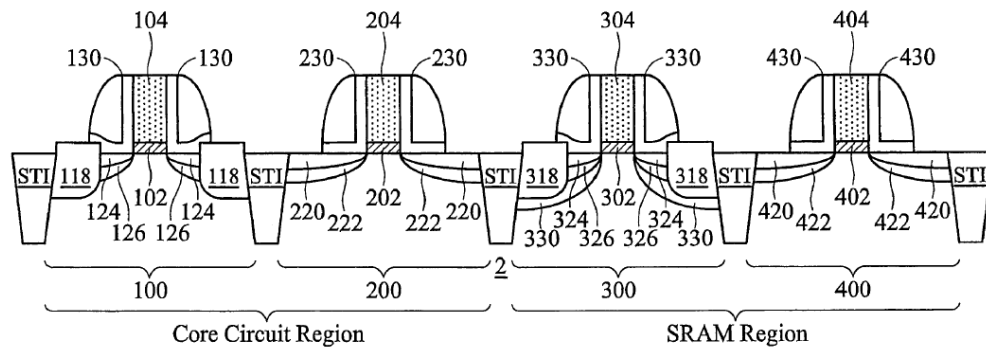
Wang753, Fig. 13 (excerpted)

275. As I explain in footnote 5 above (in Section IX.D.1.a), liner oxide layer 25 (light purple) would not extend over gate electrode 104 in FIG. 13. It would instead appear as in Wang753's FIGS. 11 and 12. (*See* Wang753 at 5:19-22.) Although this does not meaningfully affect my analysis, a person of ordinary skill in the art would have identified this as a drawing error in FIG. 13. (*See* Wang753 at 5:19-42, FIGS. 11-13.)

276. As FIGS. 10 and 11 show below, “[r]eferring to FIG. 10, a liner oxide layer 25 and a nitride layer 27 are blanket formed” and “then patterned to form spacers 130, 230, 330 and 430, as shown in FIG. 11.” (Wang753 at 5:19-22.) A person of ordinary skill in the art would have understood, and at least found obvious, that the same etching step that removes liner oxide layer 25 from the horizontal surfaces of the substrate between the gate stacks would also remove it from the horizontal surfaces on top of gate electrodes 104, 204, 304, and 404, as FIG. 11 shows. (*See, e.g.*, Quirk at 212, Fig. 9.16; Wolf3 at 595-96, Fig. 9-31; Plummer at 78-80, Figs. 2-29, 2-30.)

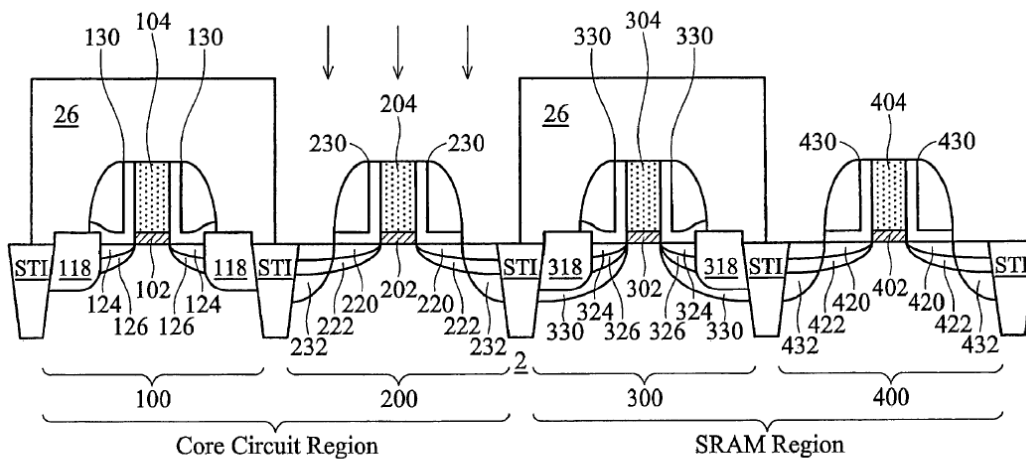


Wang753, FIG. 10



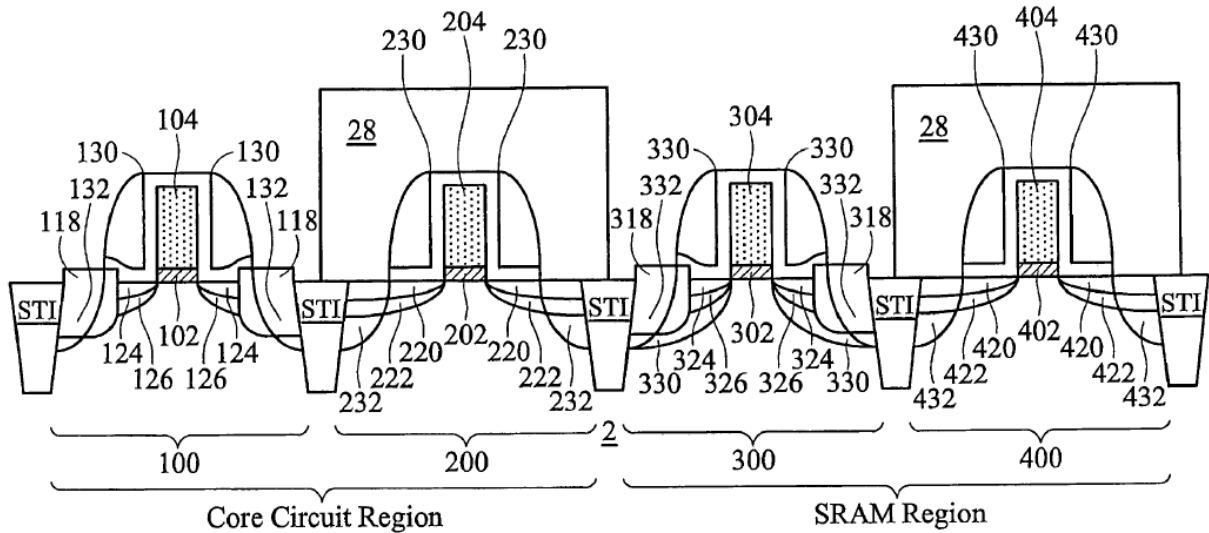
Wang753, FIG. 11

277. The liner oxide layer 25 is also shown as being etched away from the tops of gate electrodes 104, 204, 304, and 404 in FIG. 12.



Wang753, FIG. 12

278. Then, in FIG. 13, with no explanation and in the context of nothing that would form a layer on top of the gate electrodes, the liner oxide inexplicably appears on top of gate electrodes 104, 204, 304, and 404. (See Wang753 at 5:36-42.)



Wang753, FIG. 13

279. Although this does not meaningfully affect my analysis regarding Wang753, in my opinion a person of ordinary skill in the art would have identified the liner oxide layer 25 on top of gate electrodes in FIG. 13 as a drawing error. In the context of Wang753, there is no rationale or process disclosed to explain the presence of oxide layer 25 over the gate electrodes at this stage of processing.

280. In any event, Wang753 discloses (Ground 3A), and at least renders obvious (Ground 3B), a spacer (spacers 130) comprising an L-shaped spacer (liner oxide layer 25, as patterned by etching).

E. Grounds 4A and 4B: Chen Anticipates (Ground 4A) or at Least Renders Obvious (Ground 4B) Claims 1-2 and 7-8

281. Chen teaches, suggests, and renders obvious all the elements of claims 1-2 and 7-8 of the '847 Patent.

282. Through the analysis below, I conclude that Chen anticipates claims 1-2 and 7-8 (Ground 4A) because Chen discloses every limitation of those claims when viewed from the perspective of a person of ordinary skill in the art.

283. For the same reasons stated in my analysis below, I also conclude that Chen renders claims 1-2 and 7-8 obvious (Ground 4B) because the differences between claims 1 and 10 and Chen are such that claims 1-2 and 7-8 would have been obvious to a person of ordinary skill in the art.

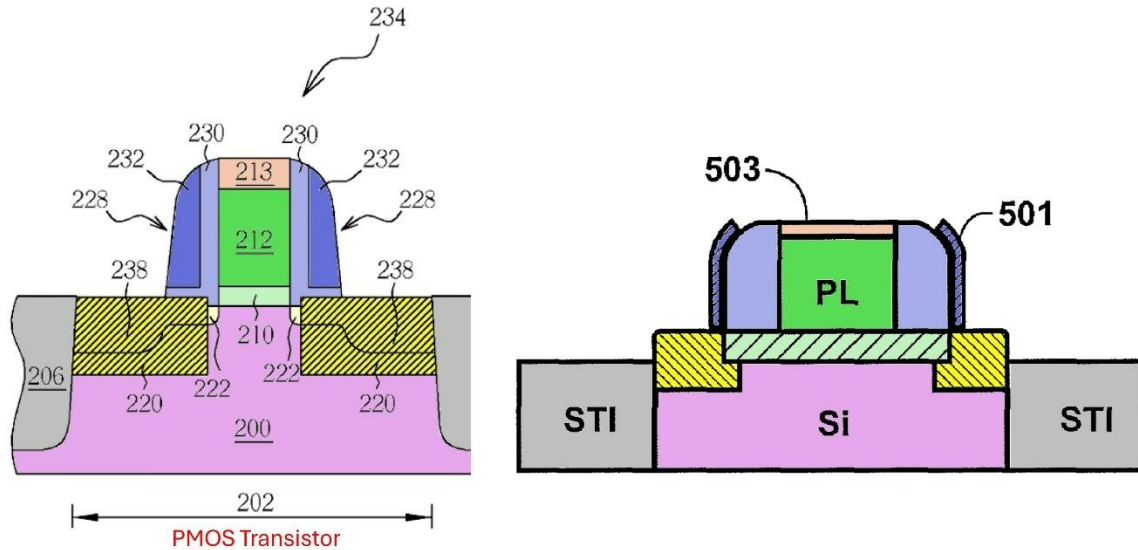
1. Independent Claim 1

a. [1pre]: “[a] MOS transistor structure”

284. Chen discloses “[a] MOS transistor structure,” as recited in [1pre].

285. Chen discloses “a method and structures for manufacturing MOS devices using strained silicon structures.” (Chen at 1:17-20.) The method includes the fabrication of a “CMOS device” with “NMOS gate structure (not shown)” and “PMOS gate structure 109.” (Chen at 4:15-56.) Chen’s PMOS structure in FIG. 5, for example, is a MOS transistor structure.

286. As shown below, Chen’s device has the same basic arrangement as the one the ’847 Patent describes. For example, both include the same arrangement of gate, spacers, source/drain epitaxy layers, lightly doped regions, and substrate.



'847 Patent, Fig. 5 (PMOS excerpted)

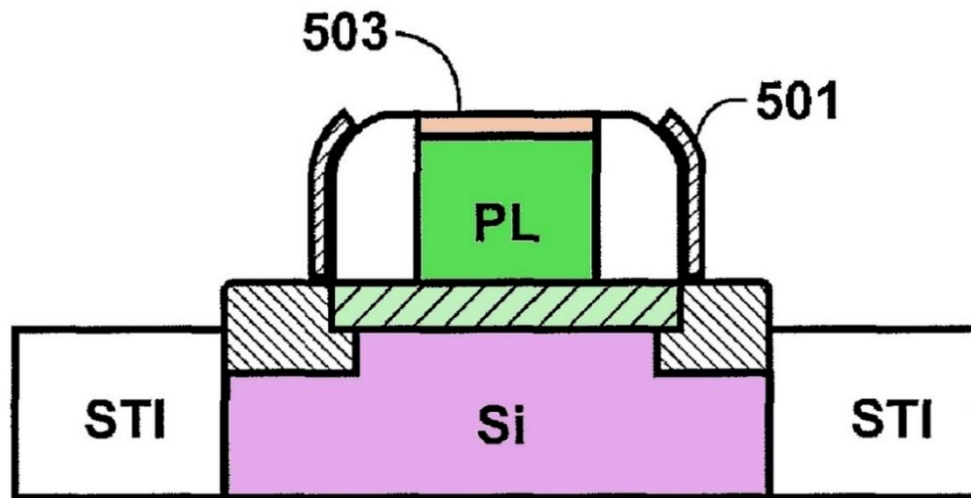
Chen, FIG. 5 (PMOS)

b. [1a]: “a gate formed on a semiconductor substrate”

287. Chen discloses “a gate formed on a semiconductor substrate,” as recited in [1a].

288. Chen discloses “a semiconductor substrate 101” (fuchsia below). (Chen at 4:19-23.) Chen also discloses “a gate dielectric layer 107 [light green below] overlying the surface of the substrate.” (Chen at 4:30-35.) Chen further discloses “a gate layer [dark green below] overlying the semiconductor substrate.” (Chen at 4:35-38.) In one embodiment, Chen’s PMOS transistor further includes a “hard mask” (peach below) overlying the gate layer. (Chen at 4:43-57, 6:11-15.) Chen explains that the gate dielectric layer, gate layer, and hard mask layer are patterned into “a PMOS gate structure 109.” (Chen at 4:44-57; 5:9-30, FIGS. 1-2.)

289. Therefore, Chen discloses a gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask) formed on a semiconductor substrate (semiconductor substrate 101).



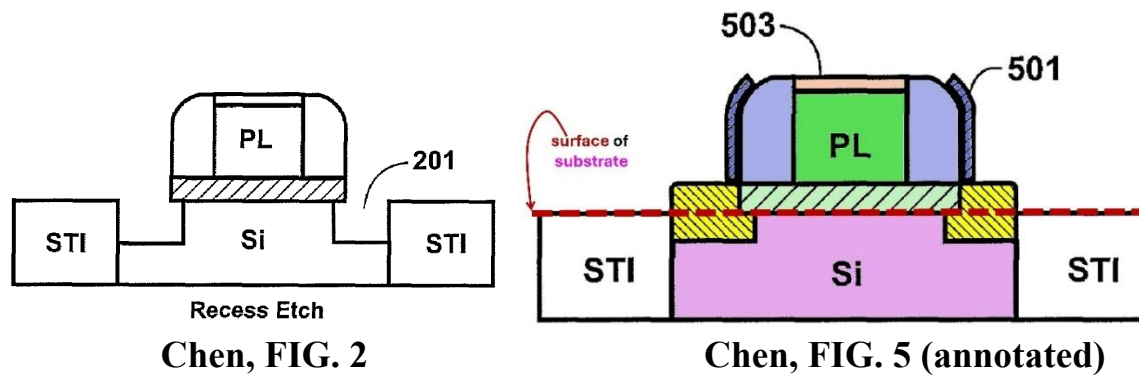
Chen, FIG. 5

- c. [1b]: “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate”

290. Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate” as recited in [1b].

291. Chen discloses a process for etching source/drain regions 201 “adjacent to the PMOS gate structure” to form recesses, as FIG. 2 shows below. (Chen at 5:9-30.) “[S]ilicon germanium material 405” is then grown in those recesses to

compress the channel. (Chen at 5:31-41.) Chen explains that the “silicon germanium is epitaxially deposited using in-situ doping techniques.” (Chen at 5:36-38; *see also* Chen at 3:52-57.) Thus, Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), two raised epitaxial layers (silicon germanium material 405) positioned respectively in the semiconductor substrate (semiconductor substrate 101) next to the relative sides of the gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask) and above the surface of the semiconductor substrate.



292. Further, having the epitaxy layers above the surface of the substrate (as Chen shows) was a typical and expected feature of the prior art strained channel technology. As I discuss in Section VI.B, raised source/drain epitaxy was well known and common in devices incorporating epitaxial source/drain stressors. The epitaxial layers grow in substrate recesses and protrude above the substrate to reduce contact resistance and ensure adequate strain transfer to the channel region. (As just a few examples, from which I reproduce images in Section IX.A.1.c above, *see*

James at 2, Fig. 6; Thompson at 1790-93, Figs. 2-5; Ghani at 978, Figs. 1-4; Bai at 657-58, Fig. 4; Wang906 ¶¶[0030]-[0032], FIG. 9; Bohr at FIGS. 4-7; Kavalieros at Abstract, ¶[0025], ¶[0043], FIGS. 5, 13.)

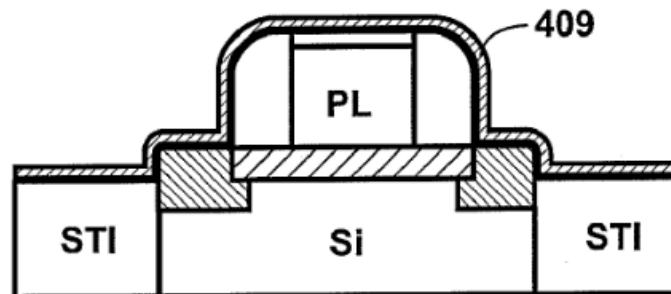
d. [1c]: “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer”

293. Chen discloses “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer,” as recited [1c].

294. Chen discloses “sidewall spacers on edges of the patterned gate layer.” (Chen at 4:49-51; *see also* Chen at 3:65-66, 4:57-59, 6:11-13.) Chen’s sidewalls may be “made of a dielectric material, such as silicon dioxide, silicon nitride, or any combination of these, and the like.” (Chen at 4:49-53.) According to Chen, “[p]referably, the final spacer structure comprises an ONO structure, as shown in FIG. 4A.” (Chen at 6:3-4.) This refers to a three-layer spacer with a silicon nitride layer sandwiched between two silicon oxide layers. (Chen at 6:4-6 (“The first oxide is about 200 Å, nitride 500 to 800 Å, second oxide 900 Å in the ONO, which is oxide on nitride on oxide structure.”).)

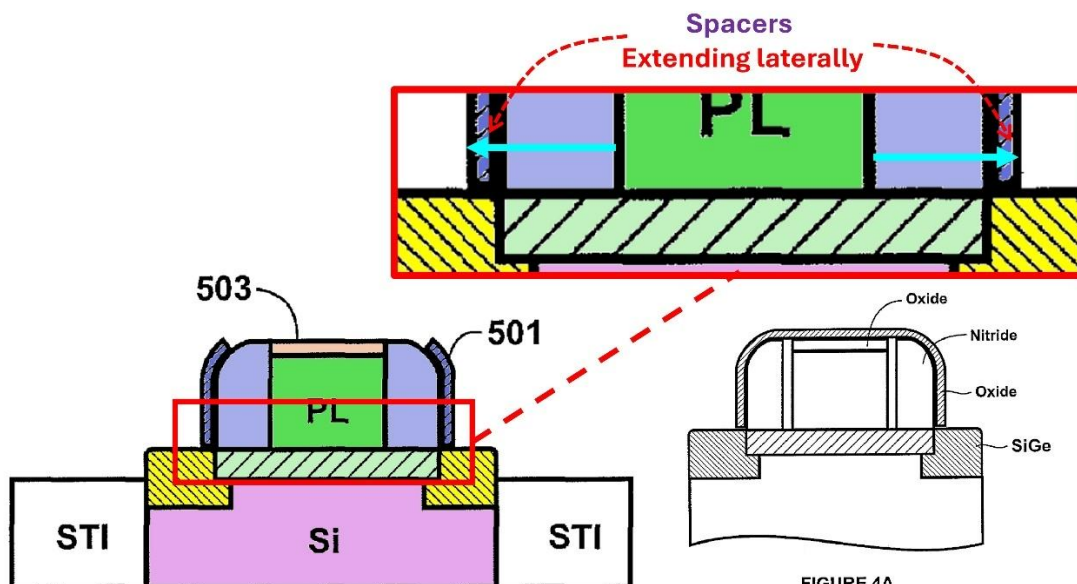
295. Chen’s “sidewall spacers 113” (which are the spacers directly contacting the gate structure) are formed “on edges of [the] patterned gate layer.” (Chen at 4:49-53; *see also* Chen at FIG. 1.) After etching trenches 201 and growing silicon germanium material 405, Chen discloses a process that involves “depositing

a protective layer 409 overlying the entirety of the patterned structure,” including silicon germanium material 405, as in FIG. 4. (Chen at 5:60-64.)



Chen, FIG. 4

296. Chen then states: “To finish the device according to an embodiment of the present invention, the method forms sidewall spacers 501” by etching protective layer 409 to “expose[] an upper portion 503 of the hard mask, while sealing regions on the edges of the gate layer.” (Chen at 6:11-15.) Chen’s FIG. 5 below shows this embodiment.



Chen, FIG. 5 (annotated, magnified)

FIGURE 4A

Chen, Fig. 4A

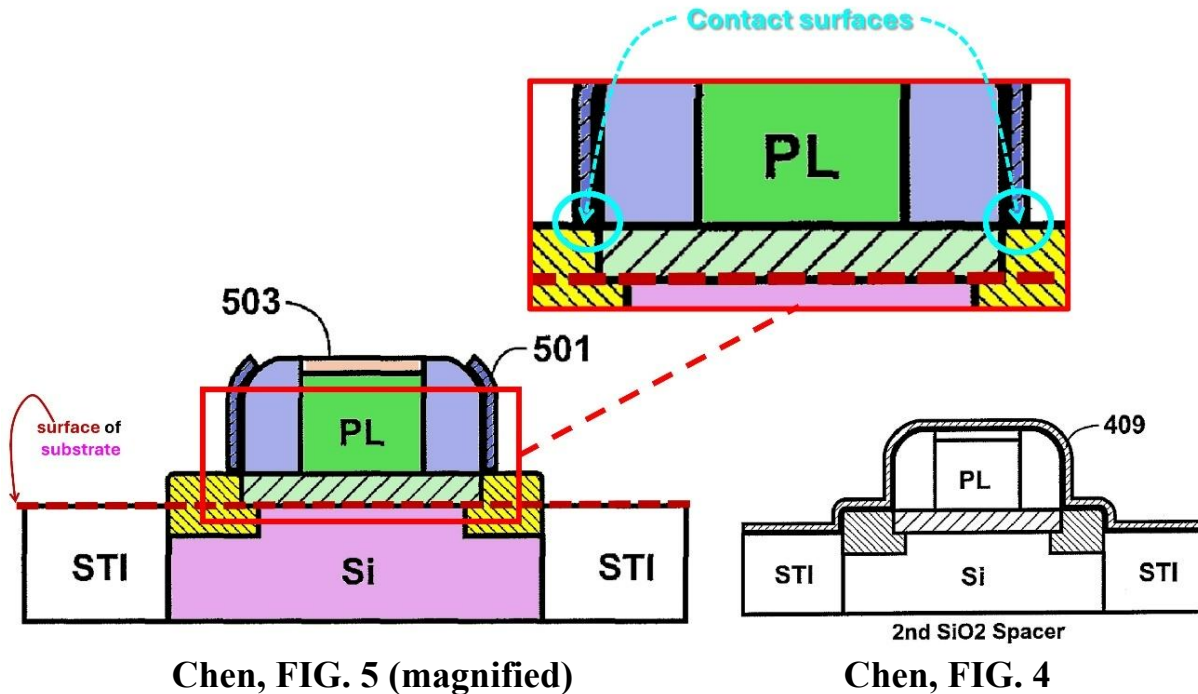
297. Therefore, as FIG. 5 illustrates above, Chen discloses a spacer (Chen's sidewall spacer 501 together with Chen's sidewall spacer 113) formed on the sidewall of the gate (Chen's gate stack comprising the gate dielectric layer, gate layer, and the hard mask) and extending laterally upon a portion of the raised epitaxial layer (silicon germanium material 405).

e. [1d]: “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate”

298. Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate” as recited [1d].

299. As I explain in Section IX.E.1.d for [1c], Chen's sidewall spacer structures extend onto a portion of silicon germanium material 405. (*See* Chen at FIG. 5.) As evident in the cross-section of FIG. 5, the bottom surface of Chen's sidewall spacer 501 and the top surface of Chen's silicon germanium material 405 intersect to define contact surfaces. (*See* Chen at FIGS. 4-5.) As I also explain in Section IX.E.1.c for [1b], a person of ordinary skill in the art would have understood (Ground 4A), and at least found obvious (Ground 4B), that the upper surfaces of silicon germanium material 405 extend above the substrate surface. (*See* Chen at Fig. 5.) Thus, as FIG. 5 indicates below, a person of ordinary skill in the art would have understood (Ground 4A), and at least found obvious (Ground 4B), that a

contact surface of the raised epitaxial layers (silicon germanium material 405) and a bottom of the spacer (e.g., bottom of sidewall spacer layer 501) is above the surface of the semiconductor substrate (semiconductor substrate 101).



300. According to Chen, spacers 501 are formed by depositing, and then etching, a “protective layer 409.” (Chen at 5:60-64, 6:11-15.) Chen specifies that protective layer 409 is deposited after and on top of silicon germanium material 405. (Chen at 5:60-62; *see also* Chen at FIG. 4.) After etching protective layer 409, a person of ordinary skill in the art would have understood that the bottom of spacer 501 remains in direct contact with silicon germanium material 405, as Chen’s FIGS. 4-5 illustrate.

301. Therefore, Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), a contact surface of the raised epitaxial layers (silicon germanium material 405) and a bottom of the spacer (e.g., a bottom of spacer layer 501) is above the surface of the semiconductor substrate.

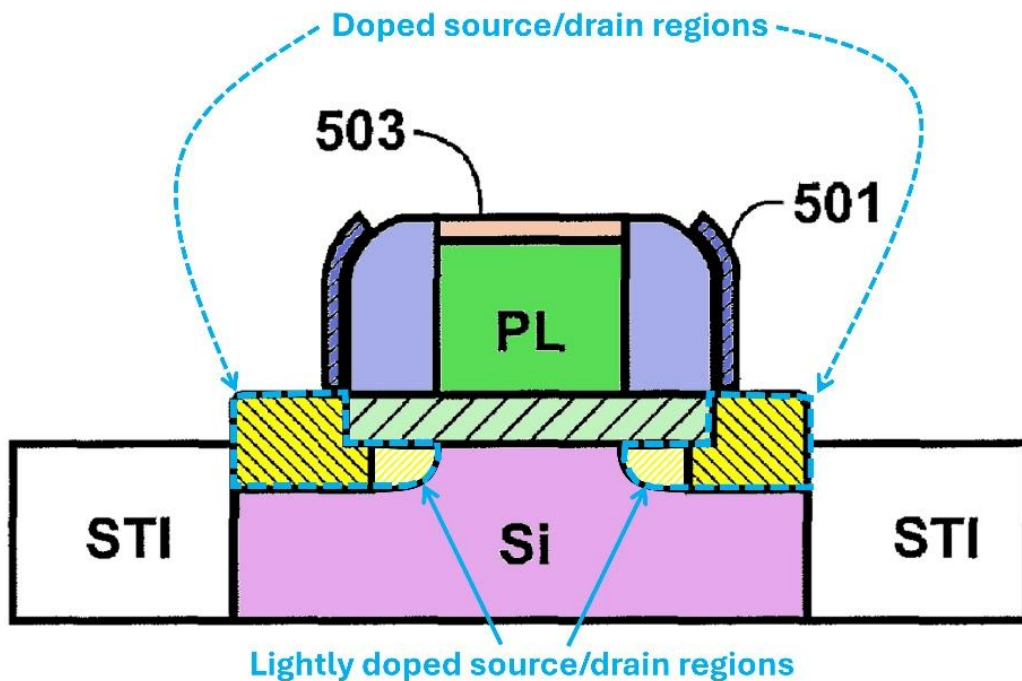
f. [1e]: “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate”

302. Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate,” as recited in [1e].

303. Chen’s silicon germanium material 405 in source/drain regions 201 is doped “using in-situ doping techniques” by introducing “impurities such as boron . . . while the silicon germanium material grows.” (Chen at 5:31-44.)

304. Chen further discloses “form[ing] lightly doped drain regions . . . on edges of [the] patterned gate layer.” (Chen at 4:57-5:8.) For PMOS devices, “the lightly doped drain region uses Boron or BF₂” introduced using “[ion] implantation techniques.” (Chen at 4:59-63.) Because Chen’s LDD regions are disclosed as being formed “on edges of [the] patterned gate layer” (Chen at 4:57-59), a person of ordinary skill in the art would have understood (Ground 4A), and at least found obvious (Ground 4B), that they are formed on the edges of the gate and in the substrate. Although Chen does not illustrate these lightly doped drain (i.e., “LDD”)

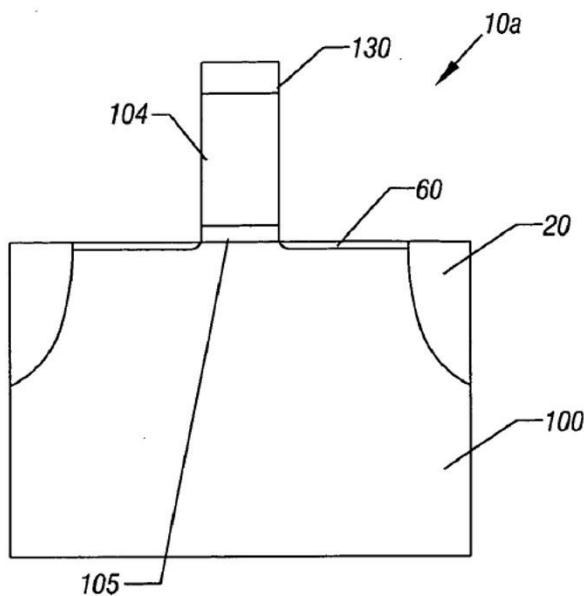
regions in the figures, a person of ordinary skill in the art would have understood (Ground 4A), and at least found obvious (Ground 4B), that Chen is describing the textbook LDD process with which anyone in the art would have been familiar, and which I discuss in Section VI.C above. A person of ordinary skill in the art would have understood (Ground 4A), and at least found obvious (Ground 4B), that Chen's LDD regions would be positioned, as shown below, near the edges of Chen's gate stack and under the interior spacer layer (sidewall spacers 113).



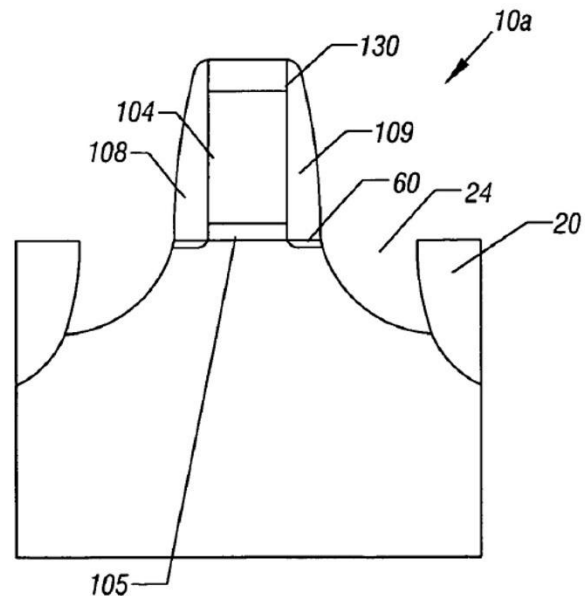
Chen, Fig. 5 (annotated, LDD added)

305. After forming Chen's LDD regions, the substrate is etched to form recessed regions 201 in which to grow silicon germanium material 405. (Chen at 5:9-30, FIG. 2.) A person of ordinary skill in the art would have understood (Ground 4A), and at least found obvious (Ground 4B), that this etching process

removes portions of the LDD-doped substrate, leaving the portion of the LDD-doped regions closer to the channel intact. Kavalieros, for instance, discloses the same process as Chen. First, as FIG. 1 shows below, “[a] tip or lightly doped source drain 60 may be formed using the gate structure as a mask” by using “[i]on implantation.” (Kavalieros ¶[0031]; *see also* Chen at 4:57-63 (describing the same).) Then, after forming a sidewall spacer 108, “[a] trench 24 is formed into the substrate 100, as shown in FIG. 4.” (Kavalieros ¶[0023]-[0024]; *see also* Chen at 5:9-13 (describing the same).) As Kavalieros’s FIG. 4 confirms, this process “leav[es] a portion of the lightly doped source drain 60” underneath the sidewall spacers. (Kavalieros ¶[0024].)



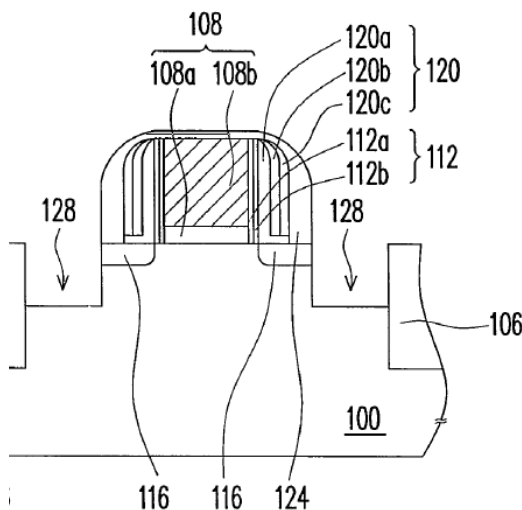
Kavalieros, FIG. 1



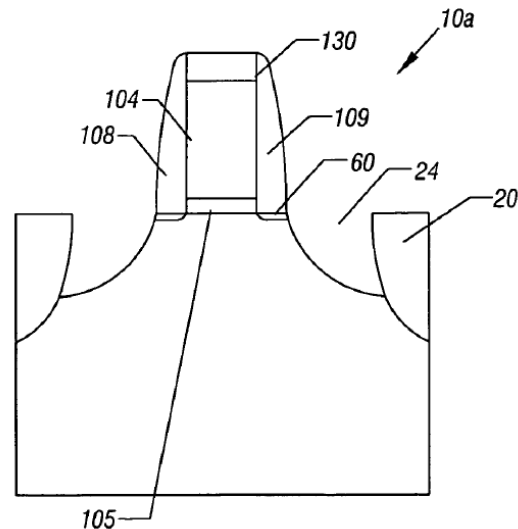
Kavalieros, FIG. 4

306. Additionally, as I explain in Section VI.C, such LDD regions reduce the electric field close to the channel to mitigate SCEs. For the LDD regions Chen

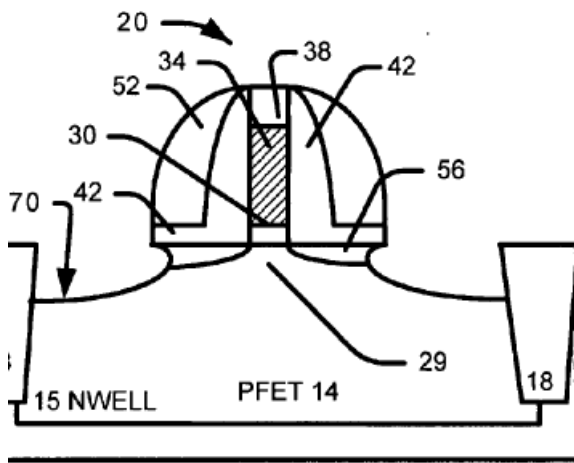
describes to serve that purpose, a person of ordinary skill in the art would have understood (Ground 4A), and at least found obvious (Ground 4B), that the portions of the LDD regions close to the channel must remain in place, or else the LDD regions would not serve their intended purpose. This is well supported in the literature, which describes the formation of the LDD regions and later etch that is set to leave the LDD region close the channel in the substrate. (Several examples include the following: Liu at 5:52-64, 6:59-7:15, FIGS. 1A-1F; Chong ¶[0032], ¶[0039], ¶[0042], Figs. 1-5B; Orlowski at 3:33-47, 4:31-44, 4:58-5:3, 5:15-18, FIGS. 1-5; Zhang ¶[0014], ¶¶[0017]-[0018], FIGS. 3-7; Kavalieros at ¶[0021], ¶¶[0023]-[0025], FIGS. 1-5; Lee at ¶¶[0034]-[0038], ¶[0052], FIGS. 4-8.)



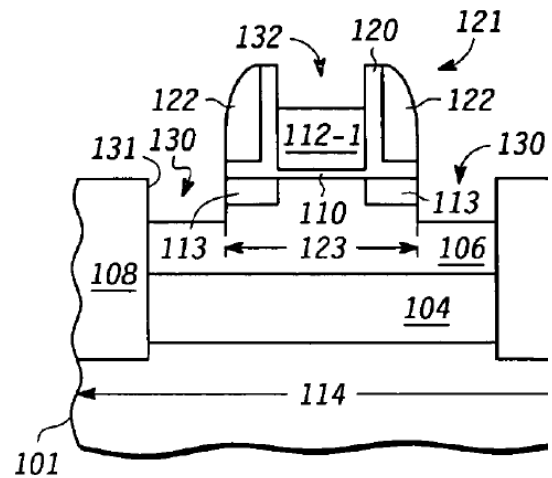
Liu, FIG. 1E (PMOS excerpted)



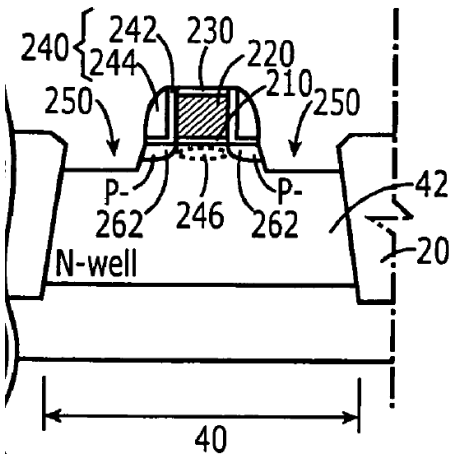
Kavalieros, FIG. 4



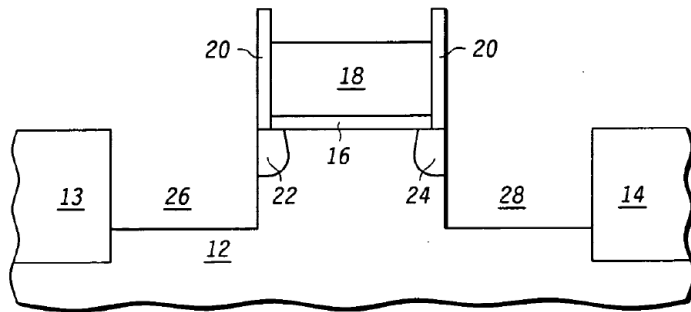
Chong, FIG. 4 (PMOS excerpted)



Orlowski, FIG. 4 (PMOS excerpted)



Lee, Fig. 7 (PMOS excerpted)



Zhang, FIG. 5

307. Thus, Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), two doped regions (Chen's lightly doped drain regions) formed respectively in the semiconductor substrate (substrate 101) next to the relative sides of the gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask).

308. Additionally, if an epitaxial region qualifies as a region “formed in the semiconductor substrate,” then any combination of Chen’s lightly doped regions and/or silicon germanium material 405 would qualify as the claimed “two doped regions” in [1e]. Like Chen’s lightly doped regions, Chen’s silicon germanium material regions 405 are doped and formed next to the relative sides of the gate, as FIG. 5 confirms. (*See* Chen at 5:9-13 (teaching to etch source/drain recesses 201), 5:32-36 (teaching to grow epitaxial SiGe in recessed regions 201), FIG. 5.)

2. Dependent Claims

a. Dependent claim 2

i. [2pre]: “[t]he structure of claim 1”

309. As I explain in Section IX.E.1, Chen discloses and renders obvious the structure of claim 1.

ii. [2a]: “wherein the gate further comprises: a dielectric layer”

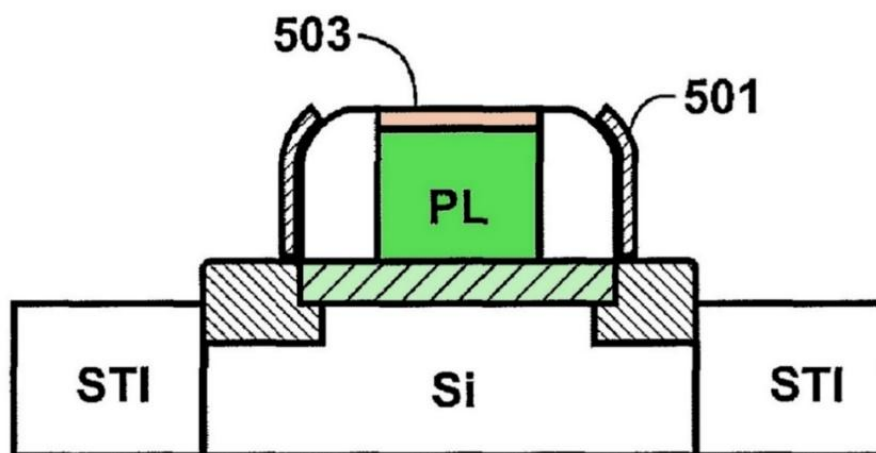
310. Chen’s gate comprises “a dielectric layer,” as recited in [2a].

311. Chen’s gate stack includes “a dielectric layer 107,” described as “oxide or silicon oxynitride depending upon the embodiment.” (Chen at 4:30-35.) Thus, Chen discloses that the gate (Chen’s gate stack comprising the gate dielectric layer, gate layer, and hard mask) further comprises a dielectric layer (dielectric layer 107).

iii. [2b]: “a conductive layer, positioned on the dielectric layer”

312. Chen’s gate comprises “a conductive layer, positioned on the dielectric layer” as recited in [2b].

313. Chen discloses “a gate layer . . . overlying the dielectric layer.” (Chen at 3:45-46; *see also* Chen at 2:10-11, FIG. 5.) Chen also describes the “gate layer [as] overlying the semiconductor substrate.” (Chen at 4:35-38.) As Chen’s FIG. 5 confirms, gate layer “PL” (dark green below) thus overlies dielectric layer 107 (light green below). Chen’s gate layer PL is made of metal or doped polysilicon, which are both conductive. (Chen, 3:45-46 (“a gate layer (e.g., polysilicon, metal)”); Quirk at 302 & Tbl. 12.1 (listing resistivities for such materials).) Chen’s gate structure thus includes a conductive layer (gate layer PL (dark green)), positioned on the dielectric layer (gate dielectric layer 107 (light green)).

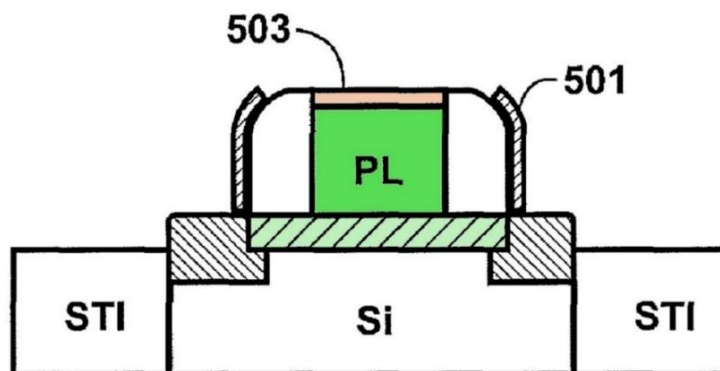


Chen, FIG. 5

iv. [2c]: “a cap layer, positioned on the conductive layer”

314. Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), that the gate structure comprises “a cap layer, positioned on the conductive layer” as recited in [2c].

315. Chen discloses an embodiment in which the gate stack further includes an optional “hard mask” (peach below) overlying the gate layer (PL, dark green). (See Chen at 4:43-59 (“Preferably, the method forms a hard mask layer overlying the gate structure. . . . [S]idewall spacers [are formed] on edges of [the] patterned gate.”), 6:11-15 (“To finish the device according to an embodiment of the present invention, the method . . . exposes an upper portion 503 of the hard 15 mask, while sealing regions on the edges of the gate layer.”).) Chen explains that the “hard mask layer can be made of any suitable material such as a dielectric material.” (Chen at 4:44-46; *see also* Chen at 3:49-51.)



Chen, FIG. 5

316. Chen's "dielectric layer (e.g. hard mask)" is formed, as shown above, "overlying the gate structure to protect the gate structure including the edges." (Chen at 3:49-51; *see also* Chen at 4:46-49 ("The hard mask layer is deposited to a suitable thickness to protect the underlying gate structure during etching and deposition steps"), FIG. 5.) Chen's hard mask is therefore positioned on the conductive layer, as claimed. Additionally, Chen's hard mask may be made of the same type of material the '847 Patent associates with the claimed cap layer. The '847 Patent explains that "cap layer 213 comprises dielectric materials." ('847 Patent at 3:3-11.) Similarly, Chen states that the hard mask may be formed with "any suitable material such as a dielectric material." (Chen, 4:44-46; *see also* Chen at 3:49-51 ("dielectric layer (e.g., hard mask) overlying the gate structure").) Therefore, despite the difference in nomenclature, a person of ordinary skill in the art would have understood that Chen's hard mask is a "cap layer" as recited in [2c].

317. Although the Chen's FIG. 6 may be a "preferred embodiment," Chen also explains that FIG. 5 shows another embodiment:

To finish the device according to an embodiment of the present invention, the method forms sidewall spacers 501 from the second protective layer, *as illustrated by FIG. 5*. The sidewall spacers exposes an upper portion 503 of the hard mask, while sealing regions on the edges of the gate layer. *In a preferred embodiment*, the method removes

the hard mask to expose 601 the top surface of the gate structures, *as shown in FIG. 6.*

(Chen at 6:11-18 (emphases added).) In the quoted passage above, Chen makes clear that FIG. 5 represents a “finish[ed] . . . device,” in which the hard mask remains part of the gate structure. Chen’s FIG. 6, on the other hand, represents a different embodiment.

318. In the embodiment of FIG. 5 above, Chen expressly discloses (Ground 4A) that the gate (Chen’s gate stack, comprising at least gate dielectric layer 107 and gate layer PL) also comprises a cap layer (Chen’s hard mask) positioned on the conductive layer (Chen’s gate layer PL).

319. Although Chen expressly discloses [2c] (Ground 4A, as described above), in my opinion a person of ordinary skill in the art also would have found it obvious to leave the hard mask on the gate structure as a cap layer in the final device structure (Ground 4B).

320. In Chen’s FIG. 6 embodiment, Chen teaches to form silicide on the gate layer (PL) by “remov[ing] the hard mask to expose 601 the top surface of the gate structures.” (Chen at 6:15-27.) Removing the hard mask to expose the gate layer (PL) permits a salicide process to take place on the gate layer, assuming it is made of polysilicon. I explain this in greater detail in Section IX.B.4.a above. But, as the

passage I quoted above from Chen makes clear, removing the hard mask is only “preferred,” not required. (Chen at 6:11-18.)

321. A person of ordinary skill in the art would have understood that removing Chen’s hard mask was optional and would have had several reasons to leave the hard mask in place (as Chen already discloses in FIG. 5).

322. First, Chen specifies that it “is directed to integrated circuits.” (Chen at 1:15-21.) A person of ordinary skill in the art would have known that integrated circuits typically include device regions where silicide is not needed or desired. A person of ordinary skill in the art would have known that integrated circuits typically include different types of transistors. For example, the Alvarez reference explains that “many different types of transistors 122 and 124 are formed across a workpiece 102 surface, with the different types of transistors 122 and 124 having different operating parameters and requirement.” (Alvarez ¶[0027].) Examples might include input-out transistors, processing transistors, logic core transistors, analog transistors, high frequency transistors, and low frequency transistors.

323. Depending on the transistor type and its function, a MOSFET would need to meet different design requirements (e.g., threshold voltage, breakdown voltage, contact resistivity, etc.) As a result, different types of MOSFETs on the integrated circuit might have different doping levels, or some may not use silicide source/drain or gate electrodes. For example, to protect the integrated circuit from

electrostatic discharge (“ESD”) and provide larger drive currents, engineers targeted high gate impedance in input-out MOSFETs. In core logic MOSFETs, on the other hand, engineers targeted a low gate impedance to facilitate faster signal transfer and lower power consumption. Because of that variability in parameters, a person of ordinary skill in the art would have understood it was desirable to avoid silicide formation in certain regions of an integrated circuit (e.g., where higher impedance is preferred). (*See*, for example, Alvarez ¶[0028] (teaching “to block the formation of silicide . . . in some regions . . . of the semiconductor device”).)

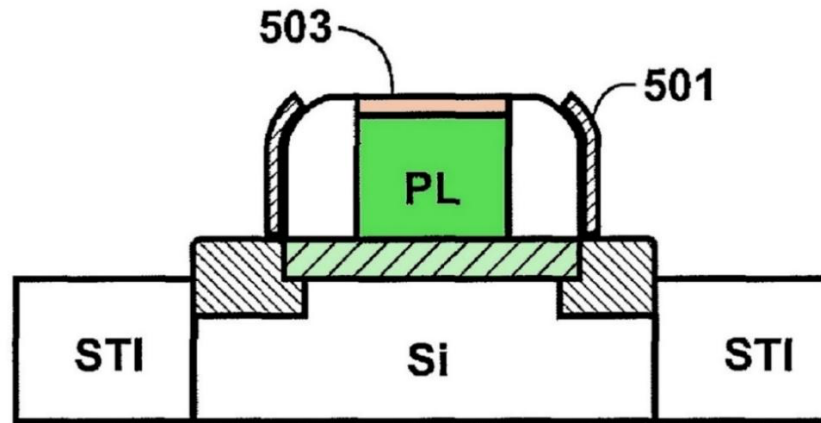
324. In device regions where silicide is unwanted on the gate, a person of ordinary skill in the art would have found it obvious to retain Chen’s hard mask because there is no need to form a silicide on the gate polysilicon. (*See* Chen at 6:15-27 (explaining that the hard mask is removed only “to expose 601 the top surface of the gate structures” to enable “form[ing] a silicide layer overlying gate layer”).) This is one reason why, for example, a person of ordinary skill in the art would have wanted to implement Chen’s embodiment of FIG. 5, which retains the hard mask, as opposed to the embodiment of FIG. 6, which removes the hard mask to form a silicide. (*See* Chen at 6:11-18, FIGS. 5-6.)

325. Second, like the Lan reference I discuss above in Section IX.B.4, Chen teaches that its conductive gate layer (PL) may be made of metal. (Chen at 3:45-46 (“[f]orm a gate layer (e.g., polysilicon, *metal*) overlying the dielectric layer”

(emphasis added)).) For the same reasons a person of ordinary skill in the art would have found it obvious to retain Lan's cap layer when using a metal gate, a person of ordinary skill in the art also would have found it obvious to retain Chen's cap layer (hard mask) when Chen's gate layer (PL) is made of metal. (See Section IX.B.4.a above.) Although it would be needlessly repetitive to restate those details from Section IX.B.4.a here, to summarize briefly, a person of ordinary skill in the art would have found it obvious that siliciding a gate metal conductive layer is unworkable and unnecessary because: (1) a salicide process would not work on a metal gate (because there is no silicon for the silicide reaction); (2) there would be no need (since the gate metal already has a low resistance); and (3) if the cap layer were removed when forming silicide on source/drain regions, the metal gate layer could be removed, corroded, or otherwise damaged when stripping the unreacted silicide metal. (See Section IX.B.4.a above.) Therefore, a person of ordinary skill in the art would have understood that retaining Chen's cap layer (hard mask) beneficially protects a metal gate layer during the salicide process to form silicide on the source/drain regions.

326. Therefore, to a person of ordinary skill in the art viewing Chen's disclosures in view of prior training, it would have been obvious that the gate (Chen's gate stack, comprising at least gate dielectric layer 107 and gate layer PL)

further comprises a cap layer (Chen's hard mask) positioned on the conductive layer (Chen's gate layer PL), as FIG. 5 shows below.

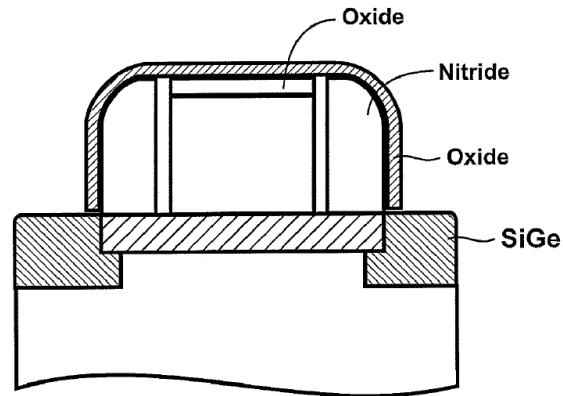


Chen, FIG. 5

- b. **Claim 7: “The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.”**

327. As I explain in Section IX.E.1, Chen discloses and renders obvious the structure of claim 1.

328. For the reasons I explain in section VII.C, here I analyze claim 7 assuming that the claim can be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the claimed “gate.” Under such interpretation, Chen discloses claim 7.



Chan, FIG. 4A

329. In Chen's preferred embodiment, "the final spacer structure comprises an ONO structure, as shown in FIG. 4A." (Chen at 6:3-10). For example, "[t]he first oxide is about 200 Å, nitride 500 to 800 Å, second oxide 900 Å in the ONO, which is oxide on nitride on oxide structure." (Chen at 6:4-6.) After forming the structure in Chen's FIG. 4A, Chen teaches to "form[] sidewall spacers 501" by etching the outer oxide layer to "expose[] an upper portion 503 of the hard mask, while sealing regions on the edges of the gate layer." (Chen at 6:11-15.)

330. Such layered spacers were common in the art. (*See*, for example, Lan at 5:61-62 ("[T]he main spacer [is] made by OO, ON, OON, ONO, ONONO."); Thei at 12:2-14 (disclosing spacers "comprising oxide nitrides as shown (ON), oxide nitride oxide layers (ONO), oxide nitride nitride layers (ONN), [and] oxide nitride oxide nitride layers (ONON)"), 14:53-56 ("[I]n this illustrative preferred embodiment an alternative to the ON structure is shown, here an ONO structure is shown as the sidewall spacer"); Huang ¶[0024] ("[T]he spacers 80 and 82 can

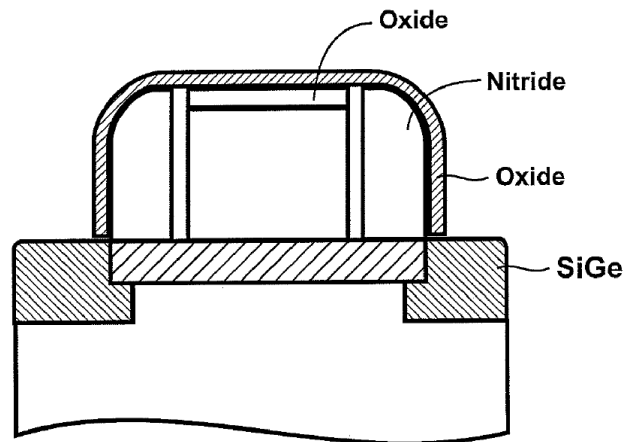
also be a multi-layer structure, such as an oxide-nitride (ON) dielectric layer, an oxide-nitride-oxide (ONO) dielectric layer, an oxide-nitride-oxide-nitride (ONON) dielectric layer, and so on.”.)

331. In view of the foregoing, Chen discloses an offset spacer (the “first oxide” in the ONO spacer) positioned between Chen’s gate stack and a portion of the spacer (e.g., the “nitride” and the “second oxide” of the ONO spacer).

c. Claim 8: “The structure of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.”

332. As I explain in section IX.E.1, Chen discloses and renders obvious the structure of claim 1.

333. As I explain in Section IX.E.2.b, Chen discloses a preferred embodiment wherein “the final spacer structure comprises an ONO structure.” (Chen art 6:3-6.) In that embodiment, the “first oxide” layer of Chen’s ONO spacer is an oxide liner. (Chen at 6:3-6; *see also* Chen at FIGS. 4A, 5.) Chen’s ONO spacer also includes a “nitride” layer. (Chen at 6:3-6; *see also* Chen at FIGS. 4A, 5.) As FIG. 4A confirms below, the “first oxide” of Chen’s ONO spacer lines the gate structure, and the “nitride” layer is sandwiched between the “first oxide” and the “second oxide.” (Chen at 6:3-6, FIG. 4A.)



Chen, FIG. 4A

334. Therefore, the spacer (Chen's ONO spacer) comprises an oxide liner (the "first oxide" of the ONO spacer) and a nitride spacer (the "nitride" of the ONO spacer).

X. Conclusion

335. As discussed above, it is my opinion that the Challenged Claims of the '847 Patent are unpatentable because they are anticipated by the prior art, because they would have been obvious to a person of ordinary skill in view of the prior art, or both.

336. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for

Declaration of Prof. Eugene Fitzgerald, Ph.D.

cross-examination within the United States during the time allotted for cross-examination.

337. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

338. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 17th day of April, 2025.

By:  _____

Prof. Eugene Fitzgerald, Ph.D.

Appendix A

Exhibit	Description
Ex-1001	U.S. Patent No. 7,745,847 B2 to Tseng et al. (“’847 Patent”).
Ex-1002	Prosecution File History of the ’847 Patent (“Prosecution History”).
Ex-1004	Curriculum Vitae of Dr. Eugene Fitzgerald, Ph.D.
Ex-1005	U.S. Pat. No. 7,935,590 B2 to Lan et al. (“Lan”).
Ex-1006	U.S. Pat. No. 7,026,689 B2 to Liaw (“Liaw”).
Ex-1007	U.S. Pat. No. 7,605,407 B2 to Wang (“Wang407”).
Ex-1008	U.S. Pat. No. 7,449,753 B2 to Wang et. al. (“Wang753”)
Ex-1009	U.S. Pat. No. 7,591,659 B2 to Chen et al. (“Chen”).
Ex-1010	S.M. Sze, <i>Physics of Semiconductor Devices</i> . (2d ed. 1981) (excerpted) (“Sze”).
Ex-1011	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted) (“Plummer”).
Ex-1012	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-76 (2005) (“James”).
Ex-1013	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained-Silicon,” <i>IEEE Transactions on Electron Devices</i> , vol. 51. No. 11, pp. 1790-97 (Nov. 2004) (“Thompson”).
Ex-1014	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al. (“Murthy”)
Ex-1015	U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al. (“Bohr”).

Exhibit	Description
Ex-1016	T. Ghani et al., “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors,” Technical Digest of the 2003 IEEE International Electron Devices Meeting (“IEDM”), pp. 978-80 (Dec. 10, 2003) (“Ghani”).
Ex-1017	U.S. Pat. Pub. No. 2007/0034906 A1 to Wang et al. (“Wang906”).
Ex-1018	U.S. Pat. Pub. No. 2006/0286729 A1 to Kavalieros et al. (“Kavalieros”)
Ex-1019	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) (“Bai”).
Ex-1020	Excerpts from C.Y. Chang & S.M Sze, <i>ULSI Technology</i> (1996) (“Chang”).
Ex-1021	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 2: Process Integration</i> (1990) (“Wolf2”).
Ex-1022	G.E. Moore, <i>Lithography and the Future of Moore’s Law</i> , Proceedings of the Society of Photo-Optical Instrumentation Engineers (SPIE) 2437, pp. 2-17 (May 19, 1995) (“Moore”).
Ex-1023	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET</i> (1995) (“Wolf3”).
Ex-1024	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> , Ch. 12: Metallization (2001) (excerpted) (“Quirk”).
Ex-1025	U.S. Pat. No. 7,364,957 to Thei et al. (“Thei”).

Exhibit	Description
Ex-1026	U.S. Pat. Pub. No. 2007/0042584 A1 to Huang et al. (“Huang”).
Ex-1027	U.S. Pat. No. 7,105,394 to Hachimine et al. (“Hachimine”).
Ex-1028	U.S. Pat. No. 7,968,952 to Fischer et al. (“Fischer”).
Ex-1029	U.S. Pat. No. 6,232,164 to Tsai et al. (“Tsai”).
Ex-1030	U.S. Pat. No. 4,641,417 to McDavid (“McDavid”).
Ex-1031	U.S. Pat. No. 7,402,496 to Liu et al. (“Liu”).
Ex-1032	U.S. Pat. Pub. No. 2007/0132038 A1 to Chong et al. (“Chong”).
Ex-1033	U.S. Pat. No. 7,238,580 B2 to Orlowski et al. (“Orlowski”).
Ex-1034	U.S. Pat. Pub. No. 2006/0228863 A1 to Zhang et al. (“Zhang”).
Ex-1035	U.S. Pat. Pub. No. 2007/0048907 A1 to Lee et al. (“Lee”).
Ex-1036	U.S. Pat. Pub. No. 2007/0249069 A1 to Alvarez et al. (“Alvarez”).

Appendix B

Claim 1	
[1pre]	A MOS transistor structure, comprising:
[1a]	a gate formed on a semiconductor substrate;
[1b]	two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;
[1c]	a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer, and
[1d]	a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and
[1e]	two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate.
Claim 2	
[2pre]	The structure of claim 1,
[2a]	wherein the gate further comprises: a dielectric layer;
[2b]	a conductive layer, positioned on the dielectric layer; and
[2c]	a cap layer, positioned on the conductive layer.
Claim 3	
The structure of claim 1, wherein the MOS transistor comprises a PMOS transistor.	
Claim 4	
The structure of claim 3, wherein the epitaxial layer comprises SiGe.	

Claim 5
The structure of claim 1, wherein the MOS transistor comprises an NMOS transistor.
Claim 6
The structure of claim 5, wherein the epitaxial layer comprises SiC.
Claim 7
The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.
Claim 8
The structure of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.
Claim 9
The structure of claim 1, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.
Claim 10
The structure of claim 1, wherein the spacer further comprises a [sic] L-shaped spacer.
Claim 11
The structure of claim 1, further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers.