

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd. and Apple Inc.,

Petitioners,

v.

Marlin Semiconductor Ltd.

Patent Owner.

Patent No. 7,745,847 B2
Filing Date: August 9, 2007
Issue Date: June 29, 2010

Title: METAL OXIDE SEMICONDUCTOR TRANSISTOR

Inter Partes Review No. IPR2025-00847

PETITION FOR *INTER PARTES* REVIEW

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Exhibit	Description
Ex-1001	U.S. Patent No. 7,745,847 B2 to Tseng et al. (“’847 Patent”).
Ex-1002	Prosecution File History of the ’847 Patent.
Ex-1003	Declaration of Dr. Eugene Fitzgerald, Ph.D.
Ex-1004	Curriculum Vitae of Dr. Eugene Fitzgerald, Ph.D.
Ex-1005	U.S. Pat. No. 7,935,590 B2 to Lan et al. (“Lan”).
Ex-1006	U.S. Pat. No. 7,026,689 B2 to Liaw (“Liaw”).
Ex-1007	U.S. Pat. No. 7,605,407 B2 to Wang (“Wang407”).
Ex-1008	U.S. Pat. No. 7,449,753 B2 to Wang et. al. (“Wang753”)
Ex-1009	U.S. Pat. No. 7,591,659 B2 to Chen et al. (“Chen”).
Ex-1010	S.M. Sze, <i>Physics of Semiconductor Devices</i> . (2d ed. 1981) (excerpted).
Ex-1011	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted).
Ex-1012	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-76 (2005).
Ex-1013	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained-Silicon,” IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004).

Exhibit	Description
Ex-1014	U.S. Pat. Pub. No. 2006/0148151 A1 to Murthy et al.
Ex-1015	U.S. Pat. Pub. No. 2004/0262683 A1 to Bohr et al.
Ex-1016	T. Ghani et al., “A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors,” Technical Digest of the 2003 IEEE International Electron Devices Meeting (“IEDM”), pp. 978-80 (Dec. 10, 2003).
Ex-1017	U.S. Pat. Pub. No. 2007/0034906 A1 to Wang et al.
Ex-1018	U.S. Pat. Pub. No. 2006/0286729 A1 to Kavalieros et al.
Ex-1019	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004).
Ex-1020	Excerpts from C.Y. Chang & S.M Sze, <i>ULSI Technology</i> (1996).
Ex-1021	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 2: Process Integration</i> (1990).
Ex-1022	G.E. Moore, <i>Lithography and the Future of Moore’s Law</i> , Proceedings of the Society of Photo-Optical Instrumentation Engineers (SPIE) 2437, pp. 2-17 (May 19, 1995).
Ex-1023	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET</i> (1995).
Ex-1024	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> , Ch. 12: Metallization (2001) (excerpted).

Exhibit	Description
Ex-1025	U.S. Pat. No. 7,364,957 to Thei et al.
Ex-1026	U.S. Pat. Pub. No. 2007/0042584 A1 to Huang et al.
Ex-1027	U.S. Pat. No. 7,105,394 to Hachimine et al.
Ex-1028	U.S. Pat. No. 7,968,952 to Fischer et al.
Ex-1029	U.S. Pat. No. 6,232,164 to Tsai et al.
Ex-1030	U.S. Pat. No. 4,641,417 to McDavid
Ex-1031	U.S. Pat. No. 7,402,496 to Liu et al.
Ex-1032	U.S. Pat. Pub. No. 2007/0132038 A1 to Chong et al.
Ex-1033	U.S. Pat. No. 7,238,580 B2 to Orlowski et al.
Ex-1034	U.S. Pat. Pub. No. 2006/0228863 A1 to Zhang et al.
Ex-1035	U.S. Pat. Pub. No. 2007/0048907 A1 to Lee et al.
Ex-1036	U.S. Pat. Pub. No. 2007/0249069 A1 to Alvarez et al.

***NOTE: All citations herein to page numbers identify the stamped page numbers of the cited exhibit, not the page numbers of the original reference.**

LIST OF CHALLENGED CLAIMS

Claim 1	
[1pre]	A MOS transistor structure, comprising:
[1a]	a gate formed on a semiconductor substrate;
[1b]	two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;
[1c]	a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer, and
[1d]	a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and
[1e]	two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate.
Claim 2	
[2pre]	The structure of claim 1,
[2a]	wherein the gate further comprises: a dielectric layer;
[2b]	a conductive layer, positioned on the dielectric layer; and
[2c]	a cap layer, positioned on the conductive layer.
Claim 3	
The structure of claim 1, wherein the MOS transistor comprises a PMOS transistor.	
Claim 4	
The structure of claim 3, wherein the epitaxial layer comprises SiGe.	

Claim 5
The structure of claim 1, wherein the MOS transistor comprises an NMOS transistor.
Claim 6
The structure of claim 5, wherein the epitaxial layer comprises SiC.
Claim 7
The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.
Claim 8
The structure of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.
Claim 9
The structure of claim 1, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.
Claim 10
The structure of claim 1, wherein the spacer further comprises a [sic] L-shaped spacer.
Claim 11
The structure of claim 1, further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers.

I. RELIEF REQUESTED

Applying the following grounds, Co-Petitioners request *inter partes* review of the '847 Patent¹ and cancellation of claims 1-11:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A/1B	1, 3-9, 11	102/103	Lan
1C	2	103	Lan
1D	2	103	Lan, Liaw
2A/2B	1, 3-11	102/103	Wang407
3A/3B	1, 10	102/103	Wang753
4A/4B	1-2, 7-8	102/103	Chen

II. STATE OF THE ART

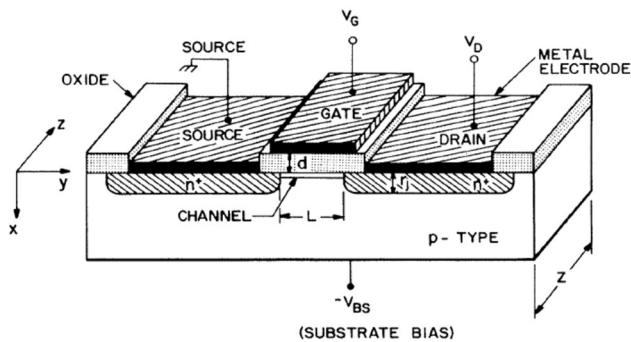
The '847 Patent describes Metal Oxide Semiconductor (“MOS”) transistors with epitaxial source/drain regions. By August 2007, when the '847 Patent was filed, such transistors were already well-known.

A. MOS Transistors

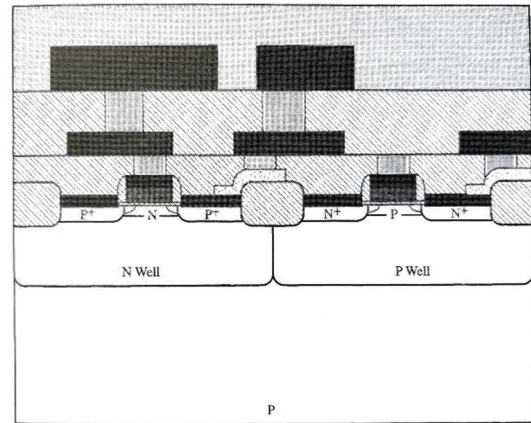
Introduced in 1960s, MOS transistors have been a cornerstone of electronics for decades. (Ex-1003 ¶45; Ex-1010, 7.) MOS field-effect transistors (“FETs”) like the ones at issue here include four main regions: *source* and *drain* regions allow for current input and output, and a *gate* overlies a *channel* region located between the source/drain regions. (Ex-1003 ¶46; Ex-1010, 9-10, Fig. 3.) The gate comprises a

¹ U.S. Patent No. 7,745,847 (Ex-1001).

conductive gate electrode and an electrically insulating gate dielectric layer that separates the gate from the semiconductor channel underneath. (Ex-1003 ¶47; Ex-1010, 9-10, Fig. 3.) Applying voltage to the gate electrode controls the channel to connect or disconnect the source and drain. (Ex-1003 ¶50; Ex-1010, 9-10, 14-15, Figs. 3, 6.) The figures below show typical MOSFET arrangements. (Ex-1003 ¶47; *see generally* Ex-1010, 9-10, Fig. 3; Ex-1011, 39-58, Figs. 1-11, 2-2, 2-22 to 2-44.)



Ex-1010, Fig. 3



Ex-1011, Fig. 1-11

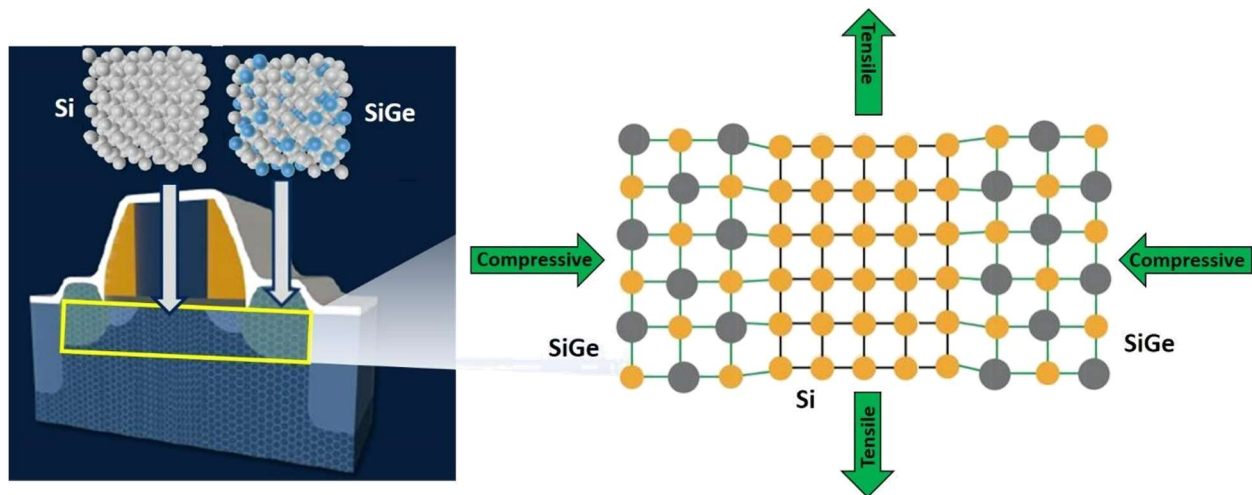
Generally, source/drain regions are *doped* with *p-type* or *n-type* impurities, and channel regions are oppositely doped. (Ex-1003 ¶48; Ex-1010, 9-10; Ex-1011, 44-50.) The terms **PMOS** and **NMOS** refer to MOSFETs with p-type or n-type source/drain regions, respectively. (Ex-1003 ¶49; Ex-1011, 16-19, Figs. 1-11, 2-2.) Typical devices are **CMOS** (“Complementary MOS”), which include both PMOS and NMOS devices. (Ex-1003 ¶49; Ex-1011, Fig. 1-11.)

B. Strained-Channel Technology

Well before the '847 patent, researchers found that mechanically stressing the silicon in the MOSFET channel increased the mobility of charge carriers (electrons in NMOS or holes in PMOS). Stressing the channel allowed the charge carriers to move more easily through the channel, enhancing switching speed and drive current. (Ex-1003 ¶51; Ex-1012, 2; Ex-1013, 1-7; Ex-1014 ¶[0005].)

To mechanically stress the channel, researchers introduced epitaxial source/drain regions comprising crystalline materials with different lattice spacings than the neighboring silicon channel. (Ex-1003 ¶51.) Compressive strain improved PMOS mobility, whereas tensile strain improved NMOS mobility. (Ex-1003 ¶51; Ex-1012, 2; Ex-1013, 1-7; Ex-1014 ¶[0005].)

Silicon-germanium ("SiGe") was the most common source of *compressive* channel stress. Because germanium atoms are *larger* than silicon atoms, growing SiGe source/drain regions compressively strains the silicon channel along the current flow direction (left-to-right below). (Ex-1003 ¶53; Ex-1012, 2; Ex-1013, 1-7; Ex-1014 ¶¶[0046]-[0047]; Ex-1015 ¶[0024], FIG. 4.) By 2005, use of SiGe had increased PMOS "hole mobility by as much as 50%." (Ex-1012, 2; Ex-1003 ¶52.)



Ex-1003 ¶53

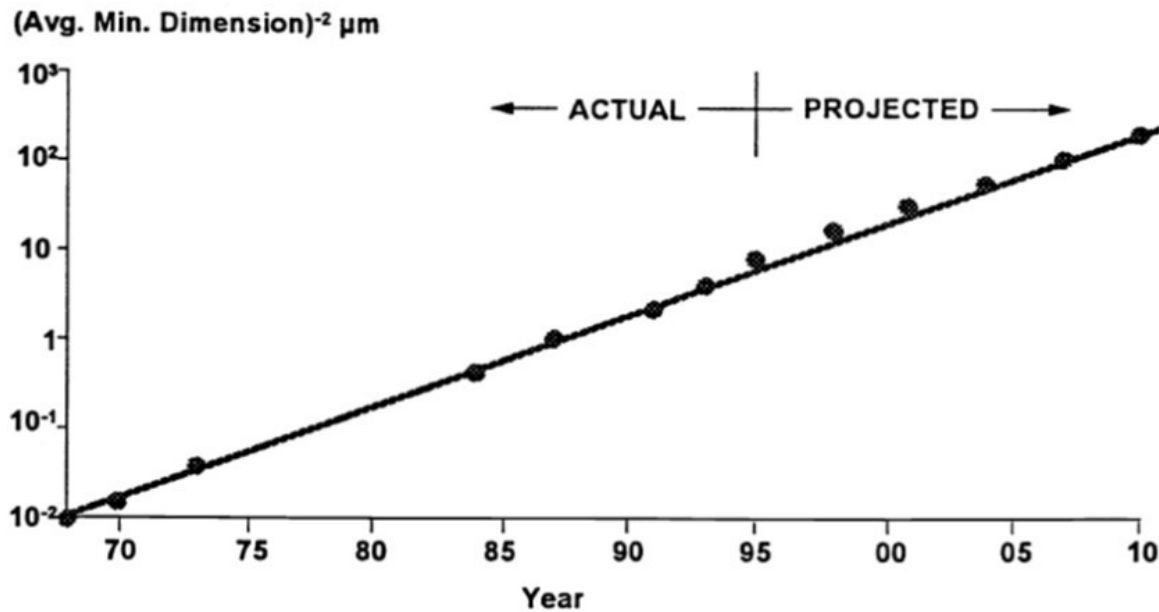
To ensure adequate strain transfer, it was common to grow epitaxial source/drain regions extending above the substrate surface. (Ex-1016, 4, Figs. 1-4; Ex-1017 ¶¶[0030]-[0032], FIG. 9; Ex-1015, FIGS. 4-7; Ex-1018, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13; Ex-1003 ¶54.) Raised epitaxy regions further improved performance by reducing contact resistance. (Ex-1012, 2-3, Fig. 6; Ex-1003 ¶54.)

Same principles were also commonly applied to NMOS, except improving NMOS carrier mobility requires *tensile* strain, not compressive. (Ex-1003 ¶55.) Creating tensile strain with source/drain regions requires growing a material like silicon carbide (SiC) with an atom (e.g., carbon) *smaller* than silicon. (Ex-1003 ¶55; Ex-1014 ¶[0005], ¶[0048], ¶[0072]; Ex-1015 ¶[0045].)

By August 2007, strained-silicon technology was well-known. The industry had been using it in the two most recent generations of high-volume commercial devices. (Ex-1013, 1-2 (90nm); Ex-1019, 4-5 (65nm); Ex-1003 ¶56.)

C. Gate Sidewall Spacers

There has always been a drive to make transistors smaller and increase their density, a trend called “scaling.” (Ex-1003 ¶57; Ex-1020, 8-11; Ex-1021, 24, Fig. 1-1(b).) For decades, scaling followed a predictable trend called Moore’s Law. (See generally Ex-1022; Ex-1003 ¶57.) The figure below shows one aspect of that trend—the rate at which the average minimum device dimension shrank. (Ex-1022, Fig. 14.)



Ex-1022, Fig. 14

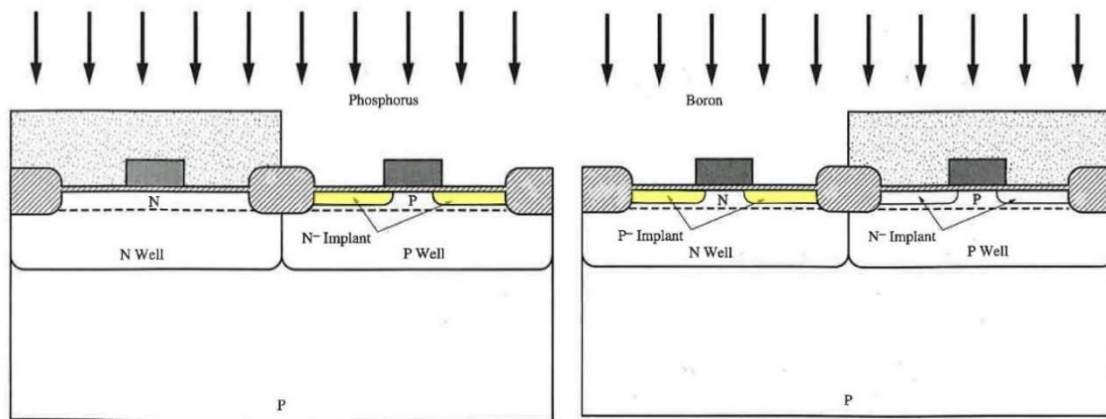
To shrink a MOSFET, the channel must become shorter, bringing the source and drain regions closer. (Ex-1003 ¶58, Ex-1023, 20, 24-25; Ex-1021, 28.) Consequently, the drain’s electric field may “penetrate into the source region” and cause unwanted current increase. (Ex-1021, 31; see Ex-1003 ¶58.) This is called

punchthrough, an example of a “short-channel effect” (“SCE”). (Ex-1003 ¶58; Ex-1023, 24; Ex-1010, 9; Ex-1024, 17; Ex-1011, 45-46.)

Researchers recognized such issues as early as the 1970s and developed a variety of techniques to mitigate SCEs. (Ex-1003 ¶59.) By the 1990s, one ubiquitous technique used in commercial semiconductor fabrication was to use so-called lightly doped drain (“LDD”) regions.² (Ex-1011, 44-50; Ex-1024, 17-19; Ex-1003 ¶59.)

With LDDs, “[t]he objective is to carefully tailor the doping profile near the drain junction (and the source junction) in order to minimize short channel effects.” (Ex-1011, 46.) The textbook figures below depict a typical method of forming LDD regions. (Ex-1011, 44-45; Ex-1003 ¶61.) As shown below, a lightly doped ion implant (yellow) is performed using the gate as a mask to block the ions from the channel region.

² Although called lightly doped *drains*, they might be more accurately described as lightly doped *sources* and *drains* since LDDs are usually formed in both regions. (Ex-1003 ¶59 n.1.)



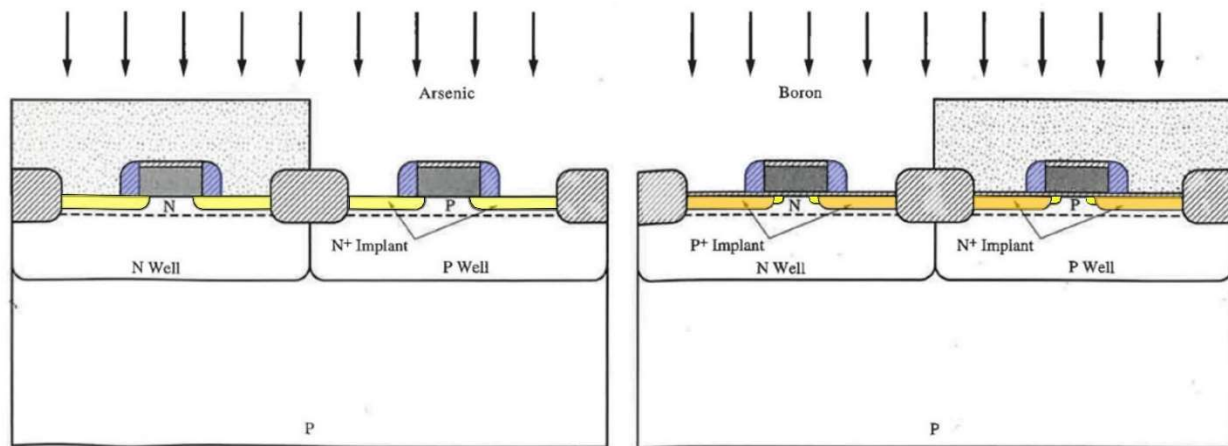
Ex-1011, Fig. 2-27^[3]

Ex-1011, Fig. 2-28

Source/drain regions generate an electric field that can affect the channel. (Ex-1003 ¶59.) By positioning more heavily doped source/drain regions (and their larger electric fields) farther away from the channel, LDD regions can mitigate those kinds of effects. (Ex-1003 ¶¶59-60; Ex-1011, 44-50; Ex-1024, 17-19.)

Such configurations are often achieved by using sidewall spacers. (Ex-1003 ¶¶61-63; Ex-1011, 46-48.) As shown below, sidewall spacers (purple) act as masks near the edge of the channel to protect the LDD regions (yellow) when performing a subsequent, heavier doping process. This spaces the more heavily doped regions (orange) farther from the channel. (Ex-1011, 48-50, Figs. 2-31 to 2-33; *see* Ex-1024, 19, Fig. 9.17; Ex-1023, 32-33, Fig. 9-31(f); Ex-1003 ¶63.)

³ Color annotations have been added throughout this Petition for emphasis.



Ex-1011, Fig. 2-31

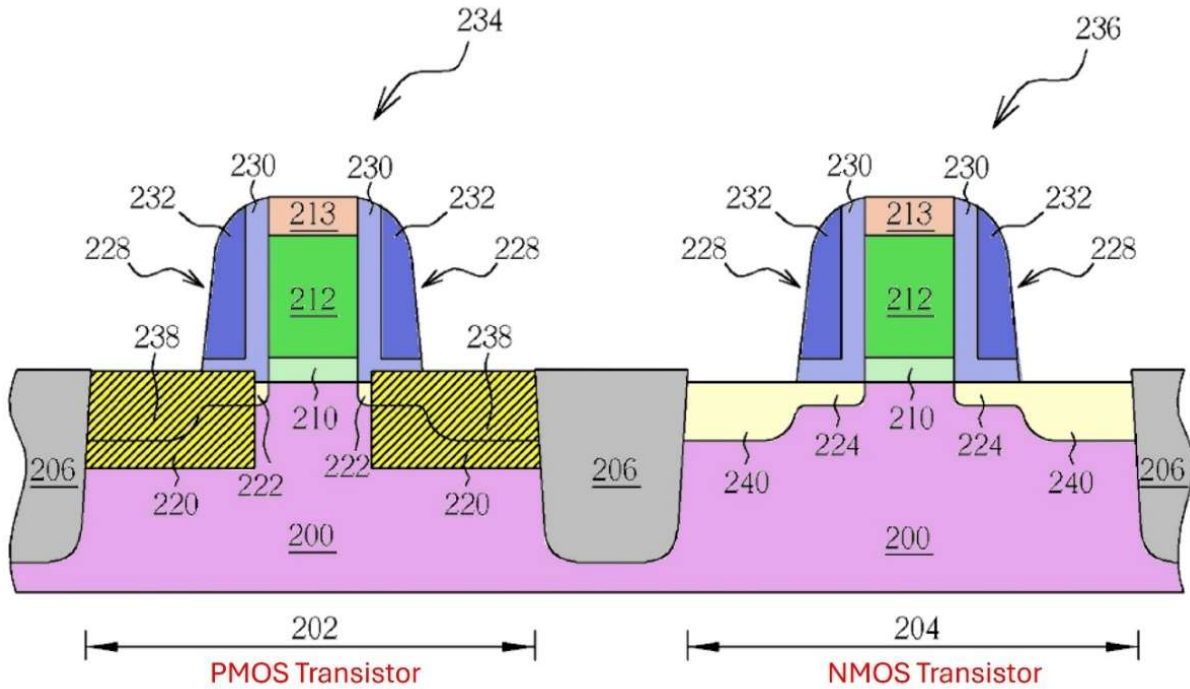
Ex-1011, Fig. 2-32

By August 2007, this type of source/drain engineering and had been commonplace for more than a decade, and sidewall spacers were a routine device element. (Ex-1003 ¶64.) And, as the prior art discussed herein illustrates, sidewall spacers that extend onto epitaxial source/drain regions were well-known. (*Id.*)

III. THE '847 PATENT

A. Overview

The '847 patent describes and claims a “MOS transistor structure” like the exemplary embodiment in Fig. 5 below. (Ex-1001, 2:21-29.) As Fig. 5 shows, the '847 Patent's exemplary transistor includes “a first conductive transistor 234” (e.g., PMOS) formed “in the first conductive transistor area 202” and “a second conductive transistor 236” (e.g., NMOS) formed “in the second conductive transistor area 204.” (*Id.*, 4:7-15.) Each transistor comprises a gate with a dielectric layer 210, a conductive layer 212, and a cap layer 213 (*id.*, 3:3-6), each flanked by sidewall spacers 228 comprising “an oxide liner 230 and a nitride spacer 232” (*id.*, 3:57-61).



Ex-1001, Fig. 5 (annotated)

PMOS

220: Epitaxial layer
222: First ion lightly doped region
234: First conductive transistor
238: First ion source/drain regions

NMOS

224: Second ion lightly doped region
236: Second conductive transistor
240: Second ion source/drain regions

NMOS & PMOS

200: Semiconductor substrate
206: Shallow trench isolation (STI)
210: Dielectric layer
212: Conductive layer
213: Cap layer
228: Spacers
230: Oxide liner
232: Nitride spacer

The PMOS device additionally includes two epitaxial layers 220 formed “next to the relative sides of the gates.” (*Id.*, 2:23-25; *see id.*, 3:33-37.) According to the ’847 Patent, those epitaxial layers “may be grown higher than the surface of the

semiconductor substrate 200, so as to form a raised epitaxial layer 220” as Fig. 5 shows. (Ex-1001, 3:35-38.) According to the specification, “the characteristic of the present invention is to form the epitaxial layer before forming the spacer, thus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer.” (*Id.*, 6:64-67.) As shown below, this allegedly inventive characteristic was not inventive at all.

B. Prosecution History

The prosecution history includes two office actions and narrowing amendments. (*See generally* Ex-1002.) In a statement of reasons for allowance, the Examiner emphasized that the prior art of record did not disclose “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.” (Ex-1002, 143-44.) But the prior art is replete with such device configurations.

C. Claim Construction

Claim terms receive their ordinary meaning as understood by a POSITA. (*See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc).) This Petition implicates only one issue of claim scope for the Board.⁴ (*Nidec Motor Corp.*

⁴ Other terms may require construction to resolve disputes elsewhere, but not here.

v. Zhongshan Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (claims only construed to the extent necessary to resolve a controversy).)

Claim 7 recites: “the spacer further comprises an offset spacer, positioned between the gate and the spacer,” which seems to require the “offset spacer” to be both part of, and not part of, the claimed “spacer.” Despite this, Patent Owner’s litigation allegations include claim 7 in the ITC. Patent Owner is expected to argue claim 7 may be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the “spacer” and the gate. For purposes of this Petition, Co-Petitioners analyze the validity of claim 7 by applying that interpretation.⁵

IV. ORDINARY SKILL

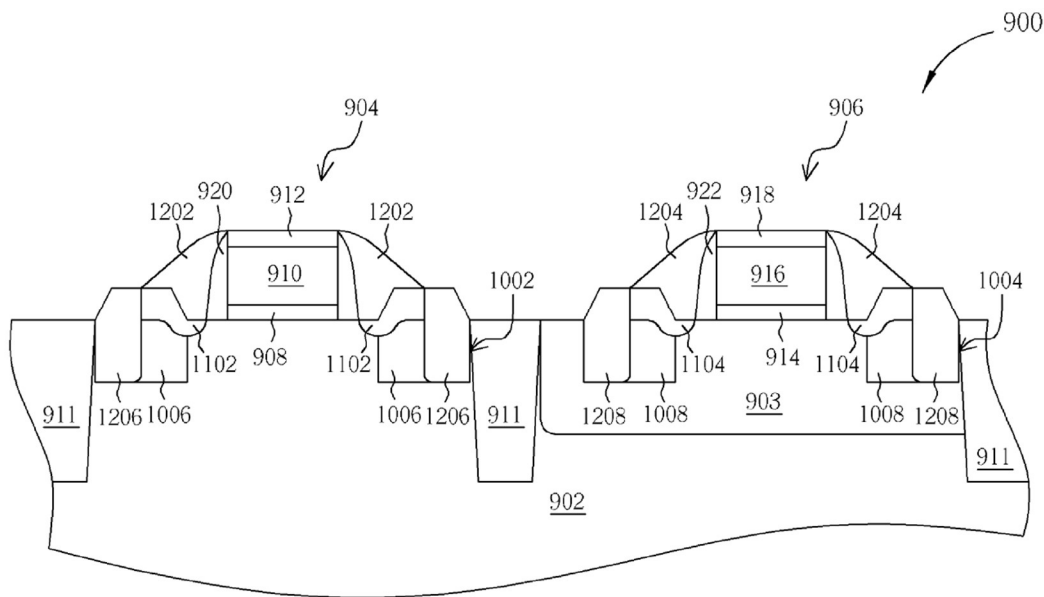
A person of ordinary skill in the art (“POSITA”) would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing as of August 9, 2007. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for formal education. (Ex-1003 ¶38.)

⁵ Co-Petitioners reserve the right to raise the indefiniteness of claim 7 in other fora.

V. PRIOR ART

A. Lan (Ex-1005)

Lan (filed May 11, 2006, and issued May 3, 2011) is prior art under pre-AIA §102(e). Because Lan is in the same field (MOSFETs) and reasonably pertinent to a problem the '847 Patent purports to address (fabricating strained silicon channel MOS transistors), Lan is analogous art. (*Compare* Ex-1001, 1:6-10, 1:49-52, *with* Lan, Title, 1:53-63; *see* Ex-1003 ¶78.)



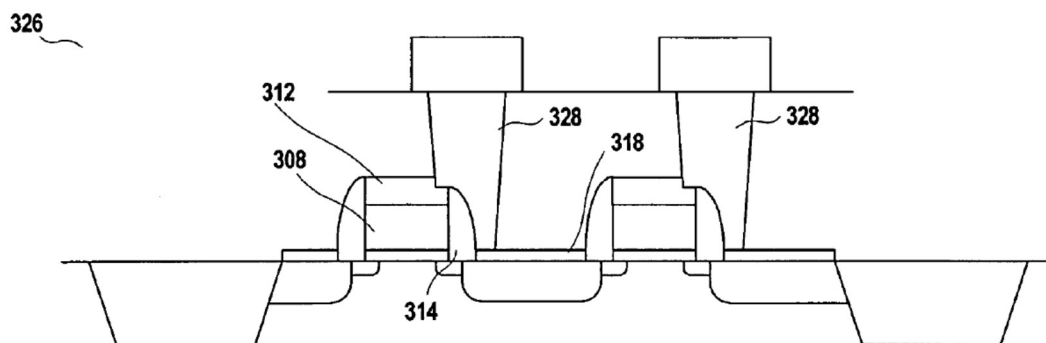
Lan, Fig. 12

Lan describes “a method of manufacturing a metal oxide semiconductor transistor.” (Lan, 1:9-15.) The gate comprises gate insulating layers 908 and 914, doped polysilicon layers 910 and 916, and cap layers 912 and 918. (*Id.*, 4:54-58.) Lan’s disclosed process “forms source/drain extension areas before forming epitaxial layers.” (*Id.*, 1:9-15.) After forming the source/drain extensions, sacrificial

spacers are used to delimit substrate recesses 1002 and 1004 on either side of the gate. (*Id.*, 4:59-5:3, Figs. 10-12.) A selective epitaxial growth (“SEG”) process then forms raised source/drain regions in substrate recesses 1002 and 1004. (*Id.*) As Fig. 12 illustrates above, after stripping the sacrificial spacers, Lan teaches to form main spacers 1202 and 1204 that extend laterally onto the raised epitaxial source/drain regions. (*Id.*, 5:4-24, Fig. 12.)

B. Liaw (Ex-1006)

Liaw (filed August 27, 2004, and issued April 11, 2006) is prior art under pre-AIA §§102(a), (b), and (e). Because Liaw is in the same field (MOSFETs) and reasonably pertinent to a problem the ’847 Patent purports to address (fabricating silicon MOS transistors, including the use of a gate capping layer), Liaw is analogous art. (*Compare* Ex-1001, 3:3-11, with Liaw, Abstract, 1:6-9, 1:58-2:2; *see* Ex-1003 ¶82.)



Liaw, FIG. 3B

Liaw describes “a metal oxide semiconductor (MOS) device with a metal gate and a cap layer.” (Liaw, 1:5-9.) Using a metal gate conductor (e.g., gate

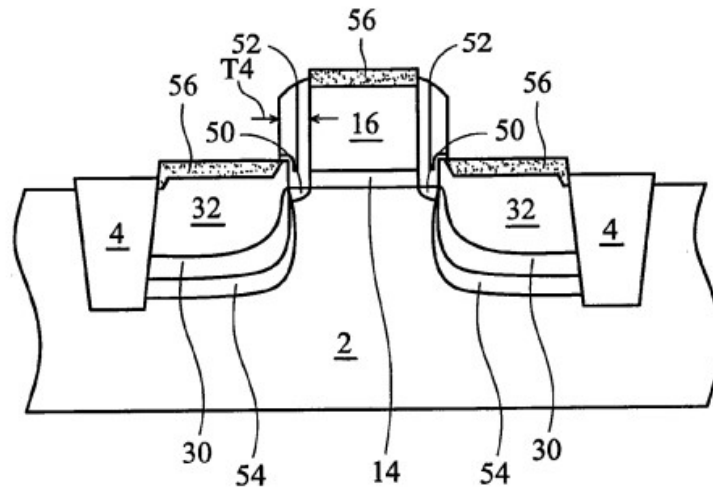
conductor 308) and an insulating cap layer (e.g., cap layer 312) “avoids the dilemma of choosing between a salicide layer on the poly-silicon gate conductor and a self-aligned contact on the source/drain regions.” (*Id.*, 4:63-66; *id.*, 3:50-4:31, FIG. 3B.) Liaw explains: “[B]y keeping the cap layer 312 atop the metal gate conductor 308, the MOS device 300 is able to tolerate a slight misalignment of the conductive plug 322.” (*Id.*, 5:5-8.) Even when conductive plugs 328 are misaligned to the source/drain regions, as FIG. 3B illustrates above, “[e]lectrical contact is, as intended, only made to the salicide source/drain contact 318, since the insulating cap layer 312 insulates the metal gate conductor 308 from being exposed.” (*Id.*, 5:18-21.)

C. Wang407 (Ex-1007)

Wang407 (filed September 6, 2006, and issued October 20, 2009) is prior art under pre-AIA §102(e). Because Wang407 is in the same field (MOSFETs) and reasonably pertinent to a problem the ’847 Patent purports to address (fabricating strained silicon channel MOS transistors), Wang407 is analogous art. (*Compare* Ex-1001, 1:6-10, 1:49-52, *with* Wang407, Title, 1:65-2:2; *see* Ex-1003 ¶85.)

Like the ’847 Patent, Wang407 describes a “method for forming stressors in metal-oxide-semiconductor (MOS) devices.” (Wang407, 3:15-16.) Also like the ’847 Patent, Wang407 recognized that to “further enhance the performance of MOS devices, stress may be introduced in the channel region of a MOS transistor to improve carrier mobility.” (*Id.*, 1:28-30.) To that end, Wang407 describes NMOS

and PMOS transistors with raised epitaxial “stressors” adjacent to the gate to strain the channel. (*Id.*, 4:4-21, Figs. 1-9 (PMOS), 5:58-6:4, Fig. 11 (NMOS).) As Fig. 9 illustrates below, Wang407’s device structure includes multi-layered sidewall spacers 52, as well as “a semiconductor substrate [2], a gate stack [comprising gate dielectric 14 and gate electrode 16] on the semiconductor substrate, and a stressor [32] adjacent the gate stack and having at least a portion in the semiconductor substrate.” (*Id.*, Abstract; *see id.*, 4:61-67, Fig. 9.)

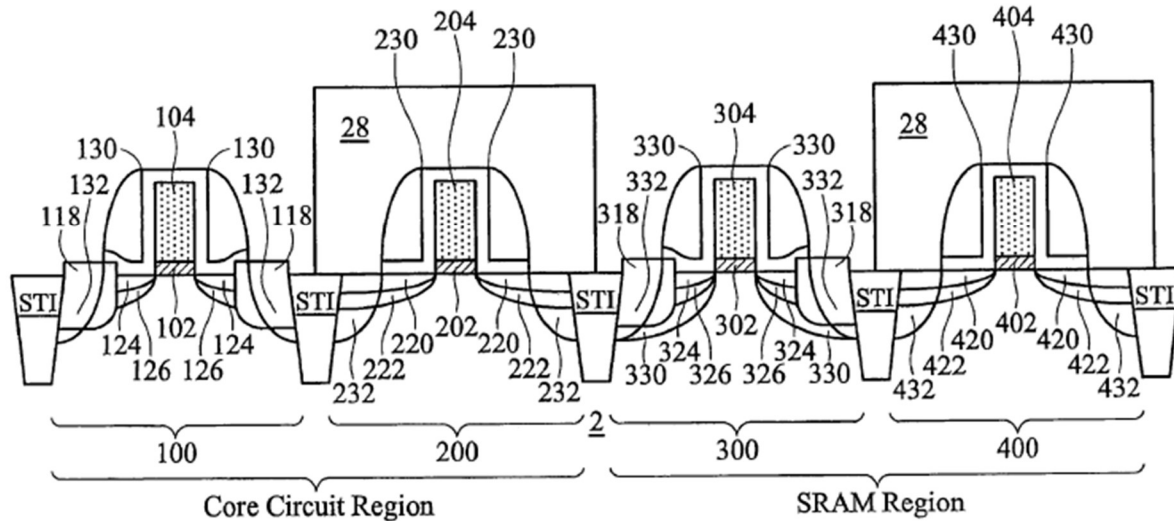


Wang407, Fig. 9

D. Wang753 (Ex-1008)

Wang753 (filed April 10, 2006, and issued November 11, 2008) is prior art under pre-AIA §102(e). Because Wang753 is in the same field (MOSFETs) and reasonably pertinent to a problem the '847 Patent purports to address (fabricating strained silicon channel MOS transistors), Wang753 is analogous art. (*Compare*

Ex-1001, 1:6-10, 1:49-52, *with* Wang753, Title, Abstract, 1:6-9, 2:29-35; *see* Ex-1003 ¶89.)

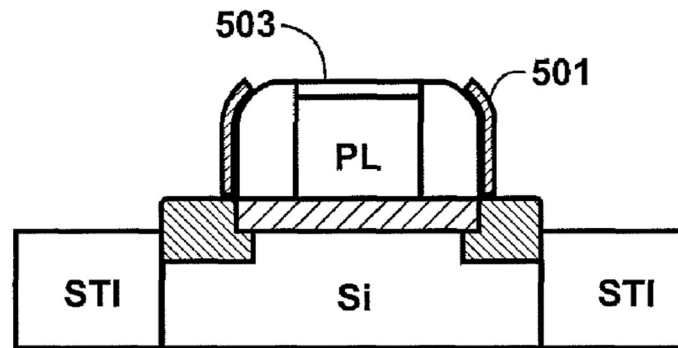


Wang753, FIG. 13

As FIG. 13 shows above, Wang753 describes a “semiconductor structure [that] includes a core circuit and an SRAM cell.” (Wang753, 1:51-56, 2:24-29.) The semiconductor structure includes active region 100 for the core PMOS devices. (*Id.*, 3:43-49, FIG. 13.) The core PMOS devices include “a gate dielectric 102 on substrate 2 and a gate electrode 104 on gate dielectric 102” (*id.*, 3:49-52), raised “SiGe stressors 118” (*id.*, 4:14-18), and “spacers 130,” formed with “a liner oxide layer 25 and a nitride layer 27” (*id.*, 5:19-26). Additionally, they include “LDD regions 124” that are formed by introducing p-type and n-type impurities, respectively. (*Id.*, 4:45-51.) The SRAM PMOS devices are similar and further include current-tuning regions 330. (*Id.*, 3:52-59, 4:14-18, 4:45-51, 4:56-58.)

E. Chen (Ex-1009)

Chen (filed October 4, 2005, and issued September 22, 2009) is prior art under pre-AIA §102(e). Because Chen is in the same field (MOSFETs) and reasonably pertinent to a problem the '847 Patent purports to address (fabricating strained silicon channel MOS transistors), Chen is analogous art. (*Compare* Ex-1001, 1:6-10, 1:49-52, *with* Chen, Title, Abstract, 3:30-37, 5:32-36; *see* Ex-1003 ¶¶93.)



Chen, Fig. 5

Chen describes “structures for manufacturing MOS devices using strained silicon structures for advanced CMOS integrated circuit devices.” (Chen, 1:15-20.) Chen’s gate structure comprises a gate dielectric layer, a conductive gate layer, and a hard mask layer. (*Id.*, 4:30-46, Fig. 5.) After the gate structure is patterned, Chen’s process (a) forms a first spacer around the gate (*id.*, 4:57-59), (b) grows raised, strained SiGe layers in trenches adjacent to the gate (*id.*, 5:9-13, 5:32-39), and (c) forms a second spacer around the first spacer and overlying the SiGe layer (*id.*, 6:11-15).

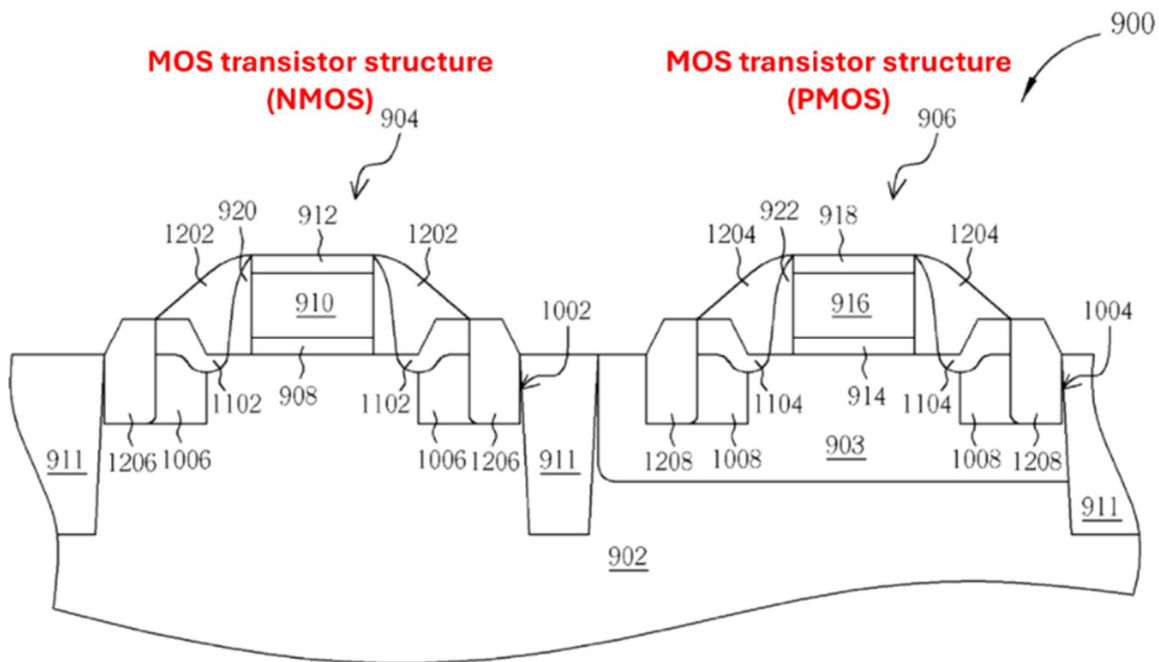
VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Grounds 1A and 1B: Lan Anticipates (Ground 1A) and Renders Obvious (Ground 1B) Claims 1, 3-9, and 11

1. Independent Claim 1

a. [1pre]: “[a] MOS transistor structure”

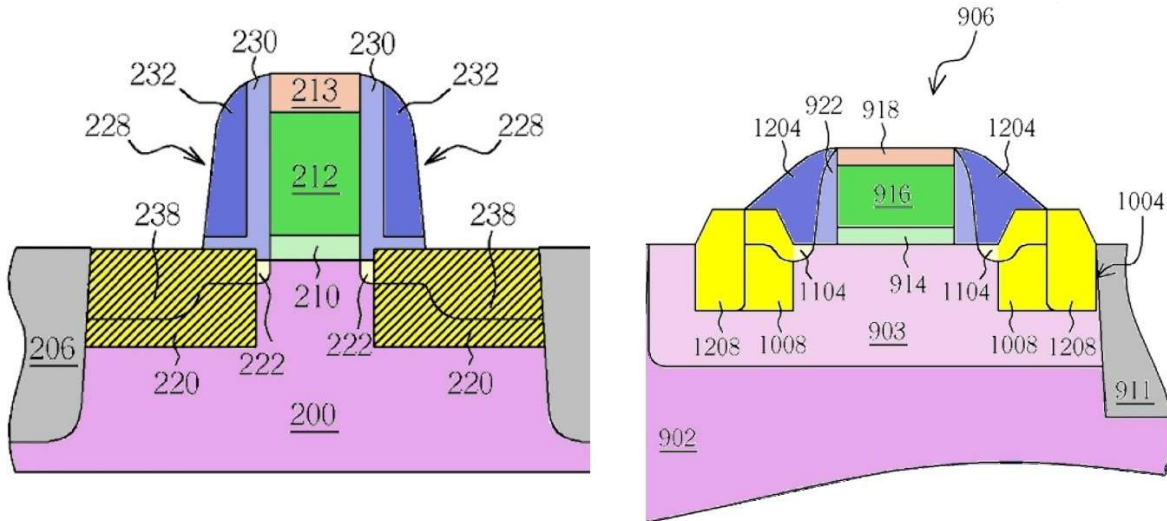
Lan discloses “a method of manufacturing ... a complementary metal oxide semiconductor transistor” comprising PMOS and NMOS devices, as Fig. 12 shows below. (Lan, 1:9-15; *see id.*, 1:53-54, 5:47-53, Figs. 1-12.) Lan thus discloses NMOS and PMOS transistor structures (MOS transistor structures). (Ex-1003 ¶¶100-102.)



Lan, Fig. 12

As the comparison below demonstrates, Lan’s PMOS transistors have the same basic arrangement as in the ’847 Patent. For example, both include the same

basic arrangement of gate, spacers, source/drain epitaxy layers, lightly doped regions, and substrate. (Ex-1003 ¶102.)

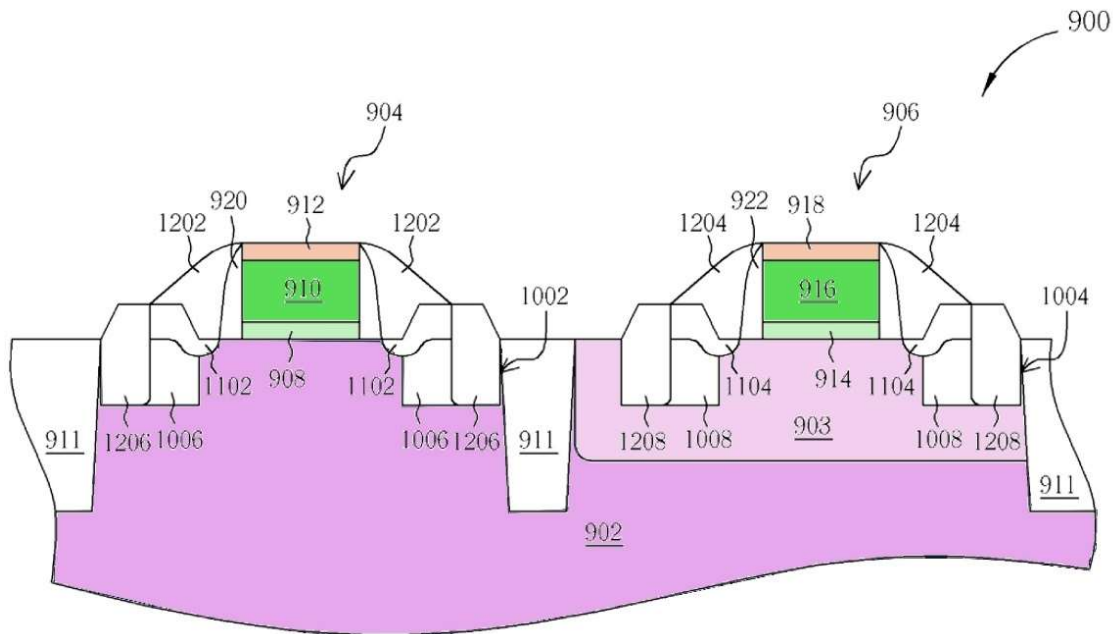


'847 Patent, Fig. 5 (PMOS excerpted)

Lan, Fig. 12 (PMOS excerpted)

b. [1a]: “a gate formed on a semiconductor substrate”

Lan’s disclosed method “provides a substrate, and a gate is formed on the substrate.” (Lan, 1:56-57.) For example, Lan discloses “[g]ates 904, 906 ... formed on [a] substrate 902” as Fig. 12 shows below. (*Id.*, 4:54-56; *see also id.*, 3:30-32, Figs. 1, 9.) Lan’s “substrate can be silicon,” which is a semiconductor material. (*Id.*, 5:55; Ex-1003 ¶105.) “The gates 904, 906 include gate insulating layers 908, 914, doped poly-silicon layers 910, 916, and cap layers 912, 918.” (Lan, 4:56-58; *see id.*, 2:51-52, 3:32-34.) Accordingly, Lan discloses a gate (e.g., gates 904 and 906) formed on a semiconductor substrate (e.g., substrate 902). (Ex-1003 ¶¶103-107.)



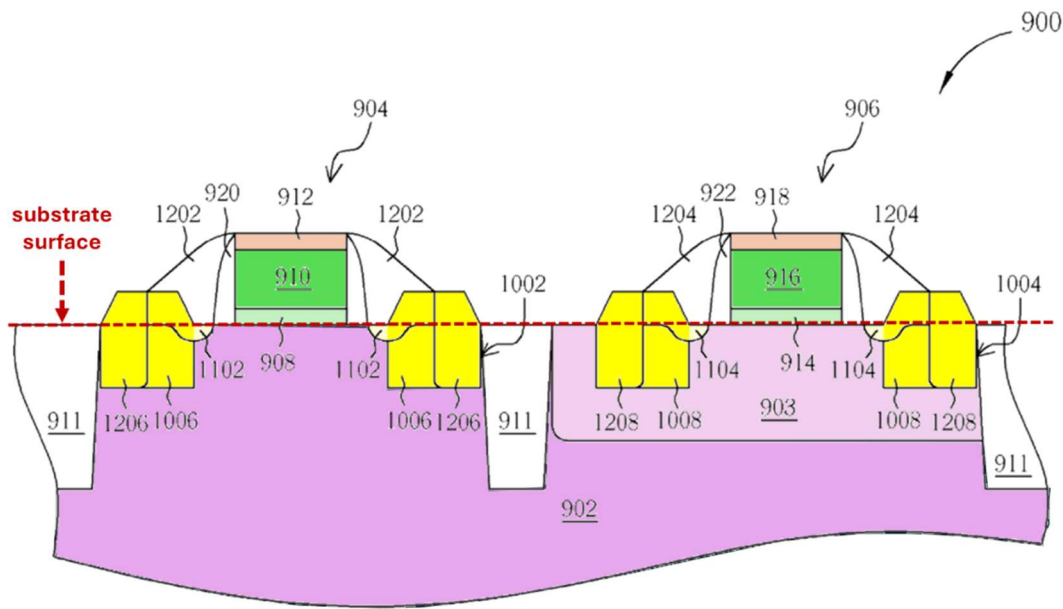
Lan, Fig. 12

- c. **[1b]: “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate”**

Lan discloses “a plurality of epitaxial layers ... on the two sides of the gate.”

(Lan, 1:59-60.) For example, Lan discloses that “a SEG [selective epitaxial growth] process is performed to form epitaxial layers 1006, 1008 in the recesses 1002, 1004.”

(*Id.*, 4:67-5:2; *see id.*, Abstract, 2:59-65, 3:55-58.) Lan’s recesses are formed “in the substrate” on “the two sides of the gate,” then filled by growing “SiGe or SiC.” (*Id.*, 2:59-65; *see id.*, 3:49-54, 4:67-5:3, Figs. 2, 5-6, 10.)



Lan, Fig. 12 (annotated)

As Fig. 12 illustrates, a POSITA would have understood (Ground 1A), and at least found obvious (Ground 1B), that Lan’s epitaxial layers extend above the surface of the substrate. (*Id.*, Fig. 12; Ex-1003 ¶¶109-110; *see Regents of Univ. of Cal. v. Satco Prods., Inc.*, No. 2023-1356, 2024 WL 4972639, at *3 (Fed. Cir. Dec. 4, 2024) (nonprecedential) (“[P]atent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their spatial relations to one another.”).)

Accordingly, Lan discloses (Ground 1A), and at least renders obvious (Ground 1B), two raised epitaxial layers (e.g., epitaxial layers 1006 and 1008) positioned respectively in the semiconductor substrate (e.g., substrate 902) next to the relative sides of the gate (e.g., gates 904 and 906) and above the surface of the semiconductor substrate—a typical and expected prior-art feature. (*Id.*, Fig. 12;

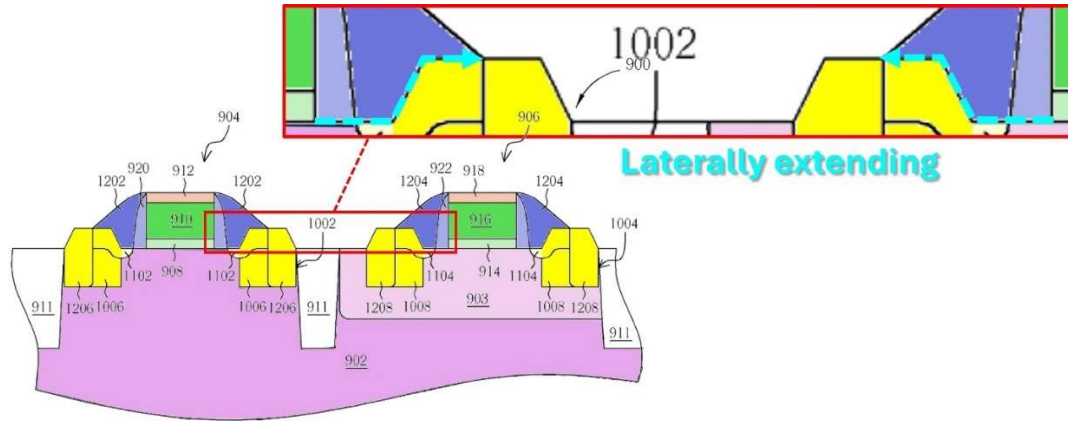
supra §II.B; Ex-1003 ¶¶108-112 (discussing Ex-1012, 2, Fig. 6; Ex-1013, 1-3, Figs. 2-5; Ex-1016, 4, Fig. 1; Ex-1019, 4-5, Fig. 4; Ex-1017 ¶¶[0030]-[0032], FIG. 9; Ex-1015, FIGS. 4-7; Ex-1018, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13).)

d. [1c]: “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer”

Lan discloses a “main spacer” and an “offset spacer,” including “main spacers 1202, 1204” and “offset spacers 920, 922.” (Lan, 3:4-8, 4:13-17, 4:59-65, 5:22-24.) The “offset spacer is formed around the gate.” (*Id.*, 1:57-59.) Lan explains that “[a] deposition process and an anisotropic etching process are performed to form offset spacers 920, 922 around the gates 904, 906.” (*Id.*, 4:59-61; *see id.*, 2:53-55, 3:35-37, 4:13-15, Figs. 1, 5, 9.)

Subsequently, after growing the epitaxial layers in the recesses, the main spacer is formed around the offset spacer. Lan explains to deposit “[a] nitride silicon layer” and perform “[a]n anisotropic etching process ... to form main spacers 1202, 1204.” (Lan, 5:22-24; *see id.*, 3:4-8, 4:15-17, Figs. 4, 8, 12; *supra* §II.C.) Alternatively, Lan explains that “the main spacer[s] are made by OO, ON, OON, ONO, ONONO,” which a POSITA would have understood (Ground 1A), and at least found obvious (Ground 1B), refers to multiple layers of silicon oxide (“O”) and silicon nitride (“N”) sidewalls in the orders listed. (Lan, 5:61-62; *see* Chen, 6:3-10, Fig. 4A; Ex-1025, 12:2-14, 14:53-56; Ex-1026 ¶[0024]; Ex-1003 ¶115.) Any of

these main spacer embodiments, alone or together with the offset spacers, satisfies [1c]. (Ex-1003 ¶115.)



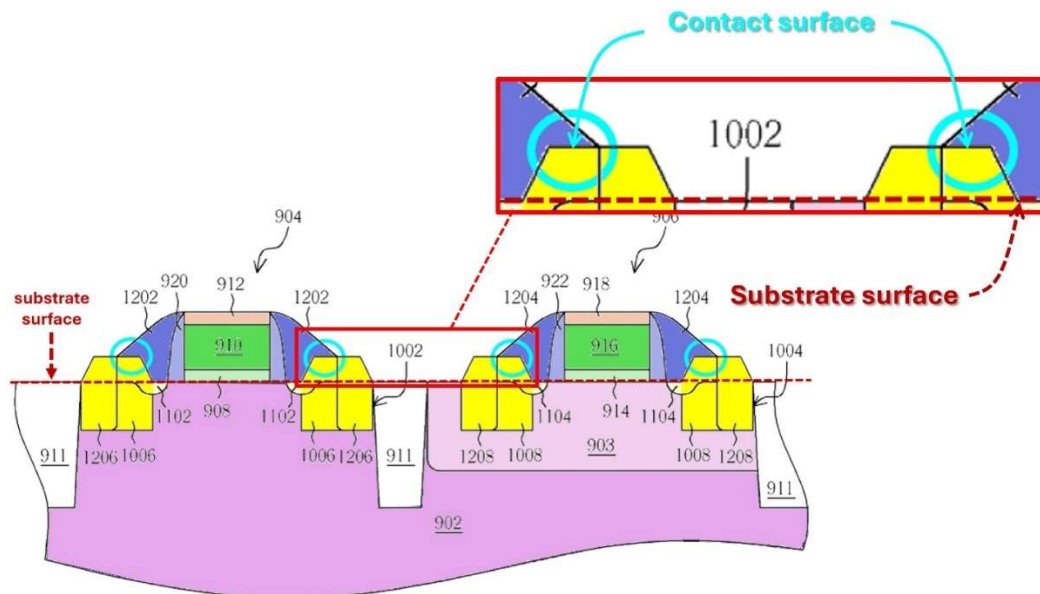
Lan, Fig. 12 (magnified, annotated)

As Lan’s Fig. 12 illustrates, main spacers 1202 and 1204 extend laterally onto epitaxial layers 1006 and 1008. (Lan, Fig. 12; *see* Ex-1003 ¶116.) Lan’s claim 5 specifically recites, “forming a main spacer ... on part of the epitaxial layers.” (Lan, 6:51-53; *see id.*, 5:26-35 (teaching “to form source/drain [1206 / 1208] in the epitaxial layers [1006 / 1008] outside the two sides of the main spacer [1202 / 1204],” such that that the main spacers cover portions of the epitaxial layers); Ex-1003 ¶116.)

Accordingly, Lan discloses (Ground 1A), and at least renders obvious (Ground 1B), a spacer (e.g., main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922) formed on the sidewall of the gate (e.g., gates 904 and 906) and extending laterally upon a portion of the raised epitaxial layer (e.g., epitaxial layers 1006 and 1008). (Ex-1003 ¶¶113-117.)

- e. [1d]: “a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate”

As explained for [1c], Lan’s spacers (e.g., main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922) extend onto a portion of Lan’s epitaxial layers 1006 and 1008. The portions of epitaxial layers 1006 and 1008 onto which Lan’s spacers extend define contact surfaces. (Lan, Fig. 12; *supra* §VI.A.1.d; Ex-1003 ¶119.) Moreover, as explained for [1b], a POSITA would have understood (Ground 1A), and at least found obvious (Ground 1B), that the upper surfaces of Lan’s epitaxial layers 1006 and 1008 extend above Lan’s substrate surface. (Lan, Fig. 12; *supra* §VI.A.1.c; Ex-1003 ¶119.)



Lan, Fig. 12 (magnified, annotated)

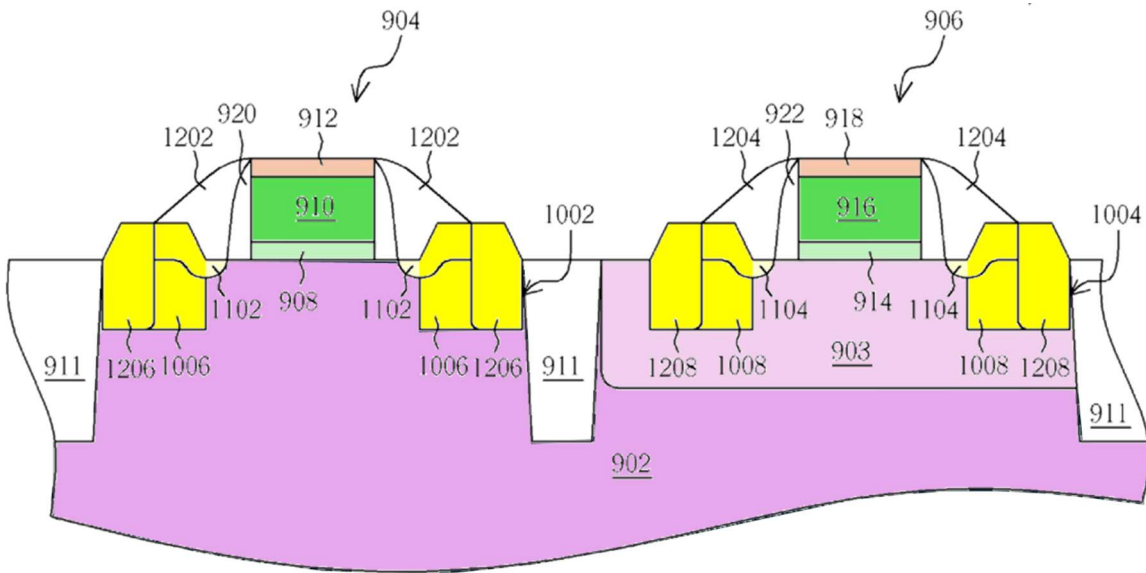
As Fig. 12 confirms above, a POSITA thus would have understood (Ground 1A), and at least found obvious (Ground 1B), that the contact surfaces

between Lan's epitaxial layers 1006 and 1008 (raised epitaxial layers) and the bottoms of Lan's main spacers 1202 and 1204 (bottom of the spacers) lie above the surface of Lan's substrate 902 (semiconductor substrate). (Ex-1003 ¶¶118-120.)

f. [1e]: “two doped region [sic] formed respectively in the semiconductor substrate next to the relative sides of the gate”

Lan discloses doped source/drain regions comprising (a) “source/drain extension areas” 1102 and 1104 and (b) “source/drain” regions 1206 and 1208. (Lan, 5:7-10, 5:13-17, 5:26-35; *see id.*, Abstract, 1:9-49, 1:61-63, 2:3-9, 2:17-29, 3:8-24, 3:63-4:46, 5:7-47, Figs. 3-4, 7-8, 11-12.) “[S]ource/drain extension areas [1102 and 1104] are formed in the substrate outside ... the epitaxial layers” using “[a] light dopant implanting process.” (*Id.*, 1:61-63, 2:66-3:3; *see id.*, 5:7-10, 5:13-17.) Meanwhile, source/drain regions 1206 and 1208 are formed “in the epitaxial layers” using “[a]n ion implanting process.” (*Id.*, 5:26-29, 5:32-35.) Epitaxial layers 1006 and 1008 also may be doped during epitaxial growth. (*Id.*, 5:41-43.)

All these source/drain regions (e.g., epitaxial layers 1006 and 1008, source/drain extension regions 1102 and 1104, and source/drain regions 1206 and 1208)) (yellow) are thus doped and formed next to the sides of gates 904 and 906, as Fig. 12 confirms below. (*See id.*, Fig. 12; *see* Ex-1003 ¶¶122-123.)



Lan, Fig. 12 (annotated)

Accordingly, Lan discloses two doped regions (e.g., at least source/drain extension regions 1102 or 1104) formed respectively in the semiconductor substrate (substrate 902) next to the relative sides of the gate (gates 904 and 906). (Ex-1003 ¶¶121-124.)

Additionally, if a doped epitaxial region qualifies as a “doped region formed ... in the semiconductor substrate,” then the claimed “two doped regions” may be mapped to any combination of Lan’s epitaxial layers (e.g., 1006 and 1008), source/drain extension regions (e.g., 1102 and 1104), and source/drain regions (e.g., 1206 and 1208). (Ex-1003 ¶125.) Like Lan’s source/drain extension regions, Lan’s epitaxial layers and source/drain regions are doped and formed next to the relative sides of gates 904 and 906, as Fig. 12 confirms. (Lan, 5:7-10, 5:13-17, 5:26-31, 5:32-35, Fig. 12; Ex-1003 ¶125.)

2. Dependent Claims

a. Claim 3: “The structure of claim 1, wherein the MOS transistor comprises a PMOS transistor.”

Lan discloses and renders obvious the structure of claim 1. (*Supra* §VI.A.1.) Lan also discloses that the device in Fig. 12 is a “CMOS transistor,” meaning it includes NMOS and PMOS transistors. (Lan, 5:37-38; *see id.*, 4:45-46 (noting the “PMOS ha[s] the epitaxial layer in a CMOS”), 5:47-53 (referencing “the etched recesses of the PMOS”); *supra* §II.A; Ex-1003 ¶128.) Accordingly, Lan discloses that the MOS transistor of claim 1 comprises a PMOS transistor. (Ex-1003 ¶¶126-128.)

b. Claim 4: “The structure of claim 3, wherein the epitaxial layer comprises SiGe.”

Lan discloses and renders obvious the structure of claim 3. (*Supra* §VI.A.2.a.) Lan further discloses that “[t]he epitaxial layers 1006, 1008 are made from ... SiGe,” which was known to improve PMOS performance. (Lan, 5:2-3; *see id.*, 2:62-65; 3:55-58, *supra* §II.B; Ex-1003 ¶131.) Accordingly, Lan discloses the structure of claim 3 wherein the epitaxial layers (PMOS epitaxial layers 1008) comprise SiGe. (Ex-1003 ¶¶129-131.)

c. Claim 5: “The structure of claim 1, wherein the MOS transistor comprises an NMOS transistor.”

Lan discloses and renders obvious the structure of claim 1. (*Supra* §VI.A.1.) Lan also discloses that the device in Fig. 12 is a “CMOS transistor,” meaning it

includes NMOS and PMOS transistors. (Lan, 5:37-38; *see id.*, 4:46-48 (noting the “NMOS ha[s] the epitaxial layer in a CMOS”), 5:47-53 (referencing “the etched recesses of ... the NMOS”); *supra* §II.A; Ex-1003 ¶134.) Accordingly, Lan discloses that the MOS transistor of claim 1 comprises an NMOS transistor. (Ex-1003 ¶¶132-134.)

d. Claim 6: “The structure of claim 5, wherein the epitaxial layer comprises SiC.”

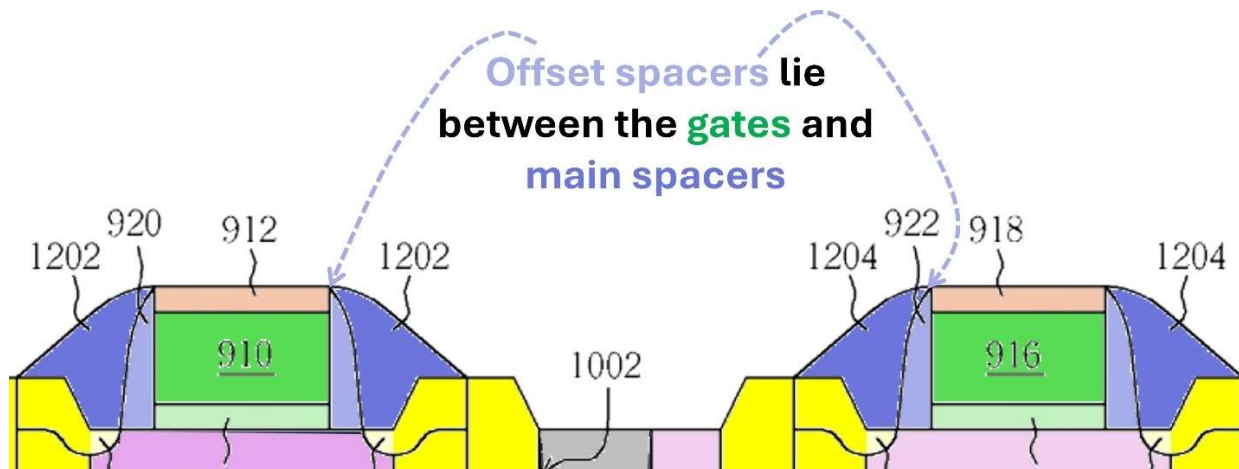
Lan discloses and renders obvious the structure of claim 5. (*Supra* §VI.A.2.c.) Lan further discloses “[t]he epitaxial layers 1006, 1008 are made from ... SiC,” which was known to improve NMOS performance. (Lan, 5:2-3; *see id.*, 2:62-65, 3:55-58; *supra* §II.B; Ex-1003 ¶137.) Accordingly, Lan discloses the structure of claim 5 wherein the epitaxial layers (NMOS epitaxial layers 1006) comprise SiC. (Ex-1003 ¶¶135-137.)

e. Claim 7: “The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.”

Lan discloses and renders obvious the structure of claim 1. (*Supra* §VI.A.1.)

Co-Petitioners expect Patent Owner to argue claim 7 may be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the gate. (*See supra* §III.C.) Lan discloses such an embodiment.

Lan's main spacers 1202 and 1204, alone or together with Lan's offset spacers 920 and 922, constitute a "spacer." (*Supra* §VI.A.1.d ([1c]); Ex-1003 ¶140.) Lan's offset spacers are "formed around the gate" (Lan, 1:57-59; *see id.*, 2:53-55, 3:35-37, 4:59-61), and Lan's main spacers are "formed around the offset spacer" (*id.*, 4:15-17; *see id.*, 3:6-8, 5:22-24). Thus, Lan discloses an offset spacer (e.g., offset spacers 920 and 922) positioned between the gate (e.g., gates 904 and 906) and at least a portion of the claimed "spacer" (e.g., main spacers 1202 and 1204). (See Lan, Fig. 12; Ex-1003 ¶¶138-140.)



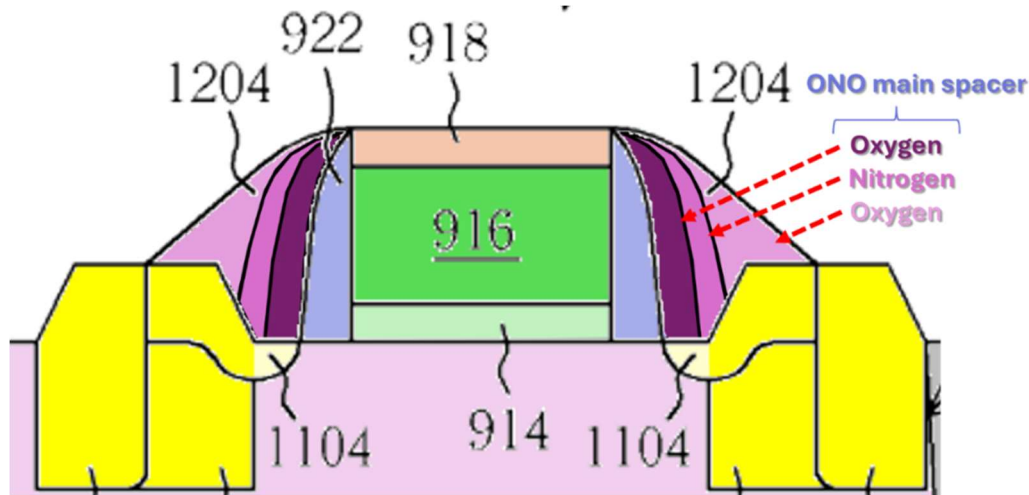
Lan, Fig. 12 (excerpted, annotated)

- f. **Claim 8: "The structure of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer."**

Lan discloses and renders obvious the structure of claim 1. (*Supra* §VI.A.1.) Lan's spacer comprises main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922. (*Supra* §VI.A.1.d ([1c]).) Lan's main spacers may be "made by OO, ON, OON, ONO, ONONO," which a POSITA would have

understood (Ground 1A), and at least found obvious (Ground 1B), refers to multiple layers of silicon oxide (“O”) and silicon nitride (“N”) sidewalls in the order listed. (Lan, 5:61-62; *see* Chen, 6:3-10; Ex-1025, 12:2-14, 14:53-56; Ex-1026 ¶[0024]; Ex-1003 ¶143.)

When Lan’s main spacers 1202 and 1204 comprise ONO, for example, they comprise an oxide liner (the interior “O” layer) and a nitride spacer (the central “N” layer). (Ex-1003 ¶144.) Accordingly, as the modified version of Lan’s Fig. 12 shows below, Lan discloses (Ground 1A), and at least renders obvious (Ground 1B), that the spacer (e.g., main spacers 1202 and 1204 alone or in combination with offset spacers 920 and 922) further comprises an oxide liner and a nitride spacer. (Ex-1003 ¶¶141-144.)



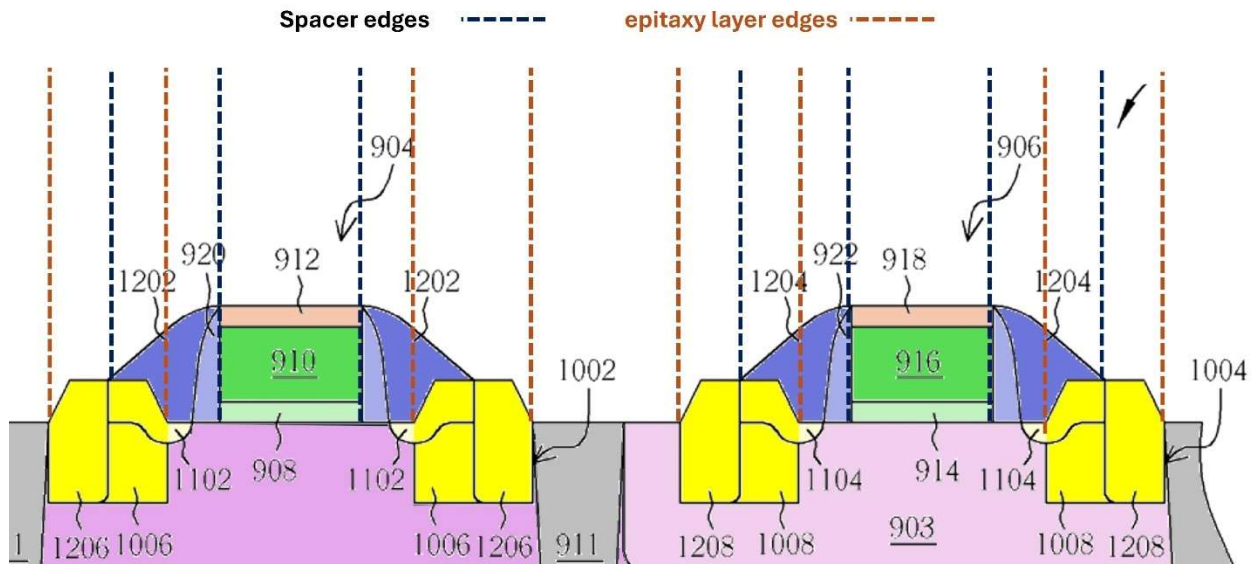
Alternative Fig. 12 (modified to show exemplary ONO embodiment)

Additionally, Lan discloses that main spacers 1202 and 1204 may be silicon nitride and that offset spacers 920 and 922 must have etch selectivity relative to

silicon nitride. (Lan, 4:59-67, 5:22-24.) A POSITA would have understood (Ground 1A), and at least found obvious (Ground 1B), that silicon oxide would be, by far, the clearest option with the required etch selectivity for offset spacers 920 and 922. (Ex-1003 ¶¶145-147 (discussing Ex-1027, 12:23-26, 18:3-6, FIG. 19; Ex-1011, 65 & Tbl. 10-1, 68 & Tbl. 10-3.) For this additional reason, Lan discloses (Ground 1A), and at least renders obvious (Ground 1B), that the spacer further comprises an oxide liner (e.g., offset spacers 920 and 922) and a nitride spacer (e.g., main spacers 1202 and 1204). (Ex-1003 ¶147.)

g. Claim 9: “The structure of claim 1, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.”

Lan discloses and renders obvious the structure of claim 1. (*Supra* §VI.A.1.) Additionally, Lan discloses that the edges of the raised epitaxial layers (Lan’s epitaxial layers 1006 and 1008) are not aligned with the edges of the spacer (e.g., Lan’s main spacers 1202/1204 alone or in combination with offset spacers 920/922), as Fig. 12 confirms below. (*See* Ex-1003 ¶¶148-151.) This is a natural consequence of how Lan uses the offset spacers, disposable spacers, and main spacers to define lightly doped source/drain extension regions 1102 and 1104, source/drain epitaxial regions 1006 and 1008, and source/drain regions 1206 and 1208, respectively. (*See* Lan, 2:65-3:11, 3:59-4:28, 5:4-35; Ex-1003 ¶150.)



Lan, Fig. 12 (excerpted, annotated)

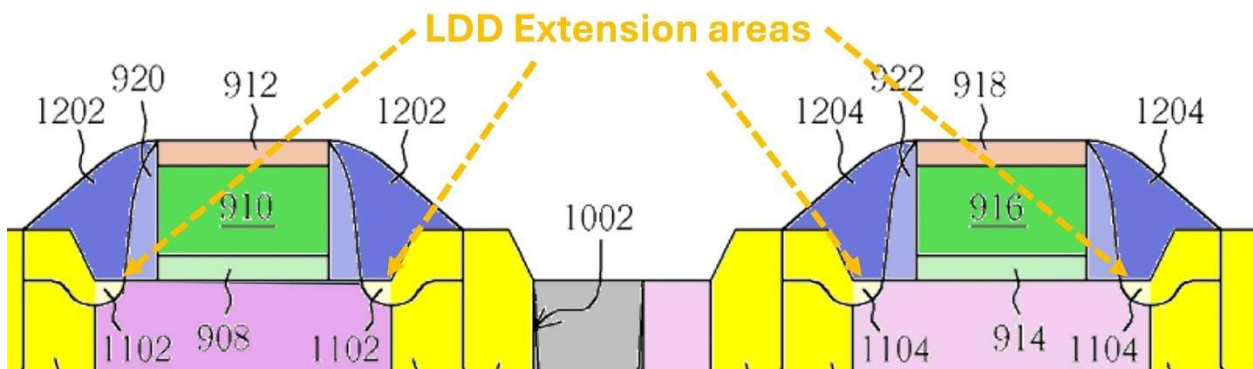
As shown above, the edges of Lan’s sidewall spacers are misaligned to the edges of the epitaxial layers. Offset spacers 920/922 contact the edges of gates 904/906, whereas epitaxial layers 1006/1008 are spaced away from the gate edge. (Lan, 4:49-5:5, Figs. 10-11.) The inner edges of the spacers and epitaxial layers thus cannot be aligned. Moreover, main spacers 1202/1204 are formed over only a portion of epitaxial layers 1006/1008, so their outer edges cannot be aligned either. (Lan, 5:4-24, Figs. 10-12; *see id.*, 3:45-4:28; Ex-1003 ¶151.)

h. Claim 11: “The structure of claim 1, further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers.”

Lan discloses and renders obvious the structure of claim 1. (*Supra* §VI.A.1.) Additionally, Lan discloses that “source/drain extension areas [1102 and 1104] are formed *in the substrate outside* the offset spacer and *the epitaxial layers*” using “[a]

light dopant ion implanting process.” (Lan, 1:61-63 (emphasis added), 2:66-3:3; *see id.*, 1:21-25, 5:7-17.) This process is the same process the ’847 Patent describes for LDD formation. (See Ex-1001, 3:29-54, Figs. 3-4). And Lan refers to source/drain extension areas 1102 and 1104 as “LDDs,” which stands for “lightly doped drain” regions. (*Id.*, 5:17-19, 2:66-3:3; *see supra* §II.C; Ex-1003 ¶154.)

Accordingly, Lan discloses a lightly doped drain (e.g., source/drain extension areas 1102 and 1104) disposed in the semiconductor substrate (e.g., substrate 902) and outside the raised epitaxial layers (e.g., epitaxial layers 1006 and 1008), as Fig. 12 confirms below. (Ex-1003 ¶¶152-155.)



Lan, Fig. 12 (excerpted, annotated)

B. Grounds 1C and 1D: Lan Alone (Ground 1C) and Lan Combined With Liaw (Ground 1D) Render Claim 2 Obvious

1. [2pre]: “[t]he structure of claim 1”

Lan discloses and renders obvious the structure of claim 1. (*Supra* §VI.A.1.)

2. [2a]: “wherein the gate further comprises: a dielectric layer”

Lan’s gates 904 and 906 comprise “gate insulating layers 908, 914.” (Lan, 4:56-57.) “The gate insulating layer is made by materials having high-K, such as oxide, nitric oxide, nitride, silica, or hafnium silicates,” which are well-known dielectrics. (*Id.*, 5:56-58; *see* Ex-1003 ¶158.) Accordingly, Lan discloses that the gates (e.g., gates 904 and 906) further comprise a dielectric layer (e.g., insulating layers 908 and 914). (Ex-1003 ¶¶157-158.)

3. [2b]: “a conductive layer, positioned on the dielectric layer”

Lan’s gates 904 and 906 comprise “doped poly-silicon layers 910, 916.” (Lan, 4:56-58.) Doped polysilicon layers are conductive. (Ex-1003 ¶160; *see* Ex-1024, 30, Tbl. 12.1.) But “[t]he gate is not limited by the above poly-silicon.” (Lan, 5:58-60.) Layers 910 and 916 “also can be made by ... any conductive material, such as metal.” (*Id.*) Lan’s conductive layers 910 and 916 are positioned on insulating layers 908 and 914, respectively, as Fig. 12 shows. Accordingly, Lan discloses that the gates (e.g., gates 904 and 906) comprise a conductive layer (e.g., doped polysilicon or metal layers 910 and 916) positioned on the dielectric layer (e.g., insulating layers 908 and 914). (Ex-1003 ¶¶159-161.)

4. [2c]: “a cap layer, positioned on the conductive layer”

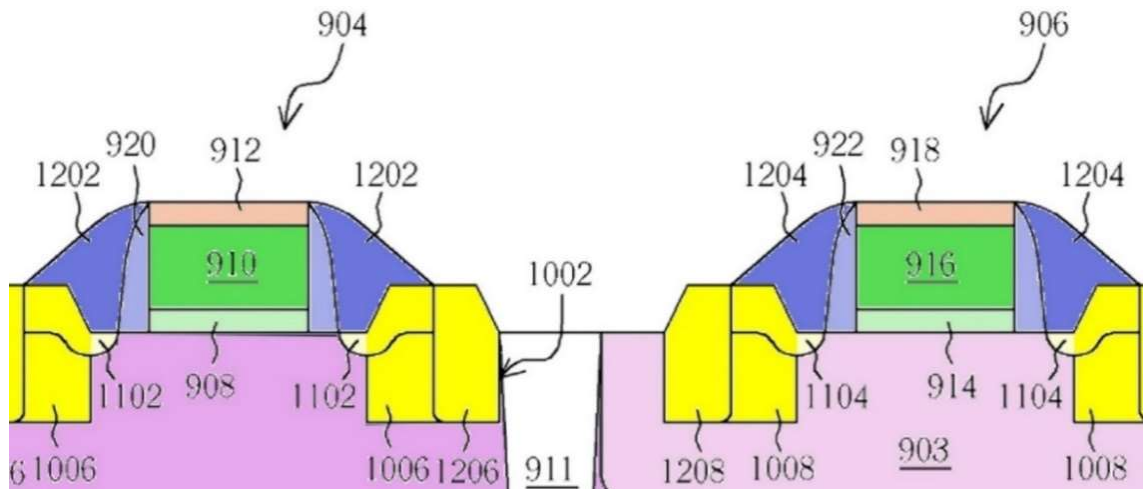
Whether viewing Lan’s disclosures based on prior training (Ground 1C) or further in view of Liaw (Ground 1D), a POSITA would have found it obvious that

Lan's gates (e.g., gates 904 and 906) include a cap layer (e.g., cap layers 912 and 918) positioned on the conductive layer (e.g., metal layers 910 and 916). (Ex-1003 ¶162.)

a. Ground 1C: Lan renders claim 2 obvious

Lan's gates 904 and 906 comprise "cap layers 912, 918." (Lan, 4:56-58; *see id.*, 2:51-62, 3:8-11, 3:32-34, 3:49-53.) When etching recesses in the substrate for the epitaxial source/drain layers, Lan's cap layers "serve as etching masks." (*Id.*, 2:49-61; *id.*, 3:49-53.) A POSITA would have understood this means the cap layers are made of a material, such as an oxide or nitride insulator, that provides etch selectivity over the silicon substrate. (Ex-1003 ¶¶163-164; *see* Ex-1011, 68, Tbl. 10-3; Lan, 5:54-56; Liaw, 4:6-20, 5:37-39; Wang407, 3:38-40; Wang753, 3:56-59; Chen, 4:43-48.)

Lan's Fig. 12 below confirms that Lan's cap layers 912 and 918 are positioned on conductive layers 910 and 916. (*See* Lan, 4:56-58.) Accordingly, Lan's gates (e.g., gates 904 and 906) comprise a cap layer (e.g., cap layers 912 and 918) positioned on the conductive layer (e.g., Lan's metal gate layers 910 and 916). (Ex-1003 ¶¶163-165.)



Lan, Fig. 12 (excerpted)

After forming the structure in FIG. 12, Lan states that “a self-aligned silicide process^[6] is performed to silicide ... the gates 904, 906, and the source/drain 1206, 1208.” (Lan, 5:35-37.) Performing this process on the gate only makes sense if Lan’s conductive layers 910 and 916 are made of polysilicon, and a POSITA would have understood it requires removing cap layers 912 and 918. (Ex-1003 ¶167.) As explained for [2b], however, Lan’s conductive layers 910 and 916 alternatively “can be made by ... any conductive material, such as metal.” (Lan, 5:58-60; *see supra* §VI.B.3.) When Lan’s conductive layers 910 and 916 are metal, a POSITA would have found it obvious to retain cap layers 912 and 918 because performing a silicide process on metal gate conductors is unworkable and unnecessary. (Ex-1003 ¶168.)

⁶ Self-aligned silicide is called “salicide” (**self-aligned silicide**) (Ex-1003 ¶166.)

In a salicide process, illustrated below, metal is deposited over a structure with exposed silicon regions and heated to a temperature sufficient to cause the metal atoms to react with the exposed silicon, creating a metallic silicide compound. (Ex-1024, 39-40, Fig. 12.13; Ex-1003 ¶169.) After the silicide forms, the unreacted metal is selectively stripped away using a chemical etchant, leaving behind the silicide in the reacted areas. (Ex-1024, 40, Fig. 12.13; Ex-1003 ¶169.)

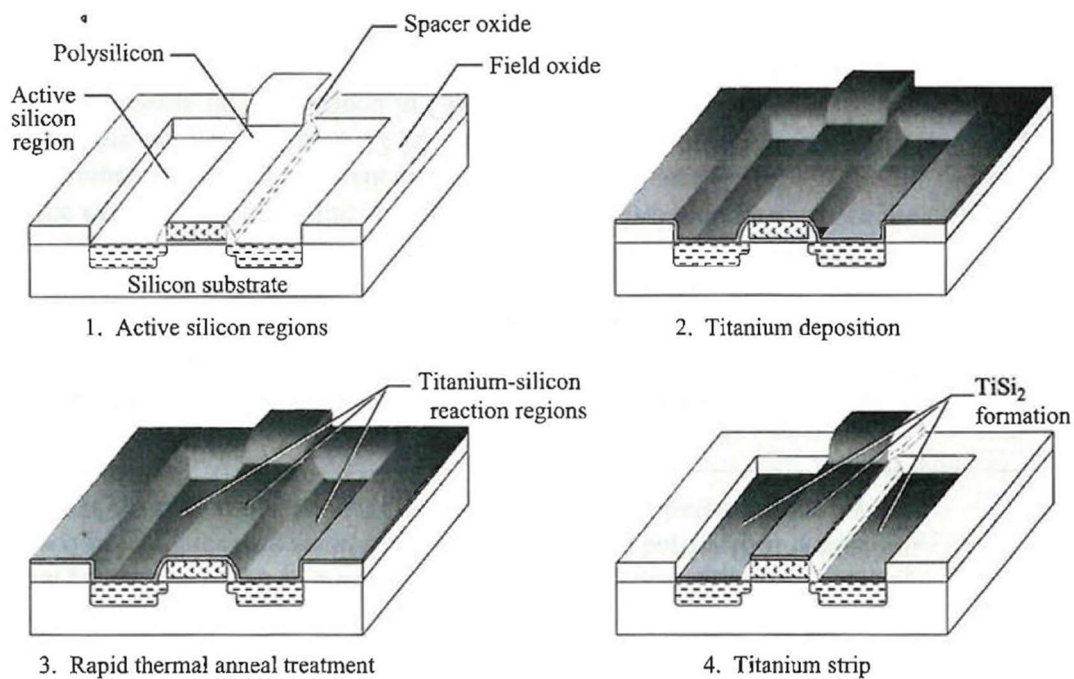


FIGURE 12.13 Formation of Self-Aligned Metal Silicide (Salicide)

Ex-1024, Fig. 12.13

Applying this textbook knowledge to Lan, a POSITA would have understood it is necessary to remove cap layers 912 and 918 to subsequently perform a salicide process on polysilicon layers 910 and 916. (See Lan, 4:56-58, 5:35-37; Ex-1003 ¶170.) Otherwise, cap layers 912 and 918 would block gate silicidation.

(*See* Ex-1024, 40, Fig. 12.13; Ex-1028, 9:28-38 (describing cap layer “to shield the gate stack” from silicidation); Ex-1003 ¶170.)

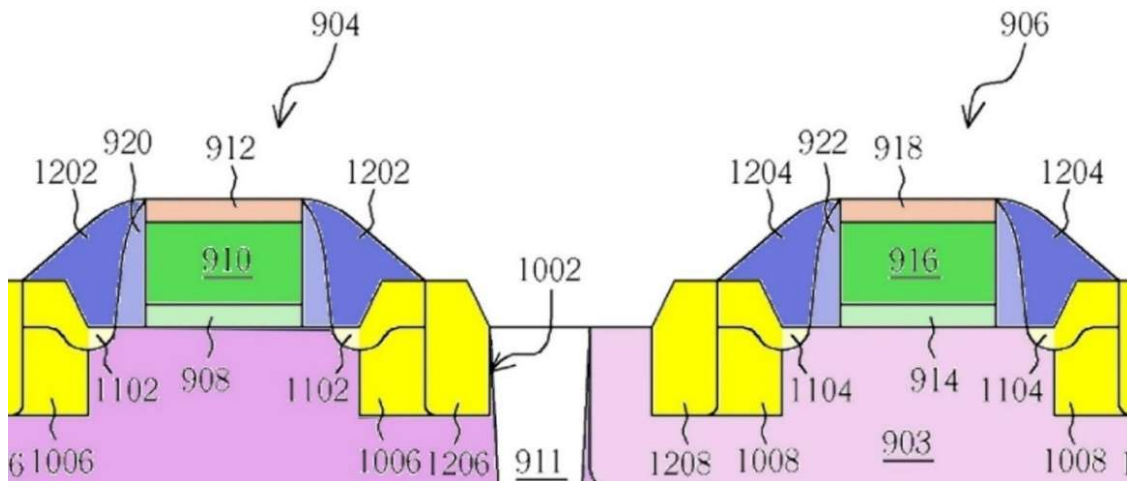
Applying this same textbook knowledge to Lan’s metal-gate embodiment (Lan, 5:58-60), a POSITA would have understood it is unworkable and unnecessary to perform a salicide process on the gates. (Ex-1003 ¶¶171-176.)

First, a salicide process would not work on a metal gate. (Ex-1003 ¶173.) Layers 910 and 916 are made of metal, so there would be no silicon in the gate with which the salicide metal layer could react. (*See* Ex-1024, 40, Fig. 12.13; Ex-1003 ¶172.)

Second, there would be no need. (Ex-1003 ¶173.) With polysilicon gates, silicidation reduces contact resistivity from about $500\ \mu\Omega\cdot\text{cm}$ to about $10\ \mu\Omega\cdot\text{cm}$. (*Compare* Ex-1024, 30, Tbl. 12.1, *with id.*, 39, Fig. 12.11; Ex-1003 ¶172.) Metals already provide low resistivity. (*See* Liaw, 4:66-5:2 (“[S]ince the gate conductor ... is made of metal, no salicide layer is needed”); Ex-1024, 30, Tbl. 12.1.)

Third, if cap layers 912 and 918 were removed when forming silicide on source/drain regions 1206 and 1208 (Lan, 5:35-37), metal gate layers 910 and 916 would be exposed to the etchant used to strip the unreacted silicidation metal, which could remove, corrode, or otherwise damage metal layers 910 and 916. (*See* Ex-1024, 40, Fig. 12.13; Ex-1003 ¶174.) In fact, a POSITA would have understood that retaining the cap layers beneficially protects the metal gate layers

when forming silicide on the source/drain regions. (See Liaw, 4:63-5:23, 5:14-23, FIG. 3B; Ex-1029, 5:56-59, 5:66-6:2, 6:31-32, FIG. 7; Ex-1030, 2:26-28, 3:13-18, Fig. 5; Ex-1003 ¶¶174-175.)



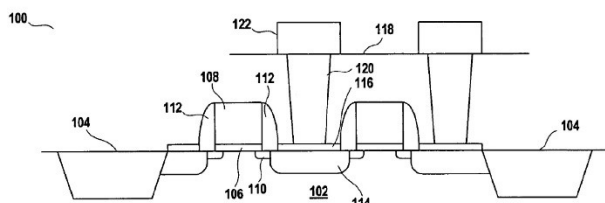
Lan, Fig. 12 (excerpted)

A POSITA thus would have found it obvious to retain cap layers 912 and 918 when layers 910 and 916 are made of metal. (Ex-1003 ¶¶163-176.) Doing so, a POSITA would have understood that Lan's gates (e.g., gates 904 and 906) include a cap layer (e.g., cap layers 912 and 918) positioned on the conductive layer (e.g., metal layers 910 and 916), as Fig. 12 shows above. (Ex-1003 ¶177.)

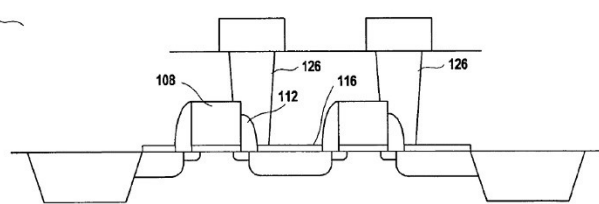
b. Ground 1D: The combination of Lan and Liaw renders claim 2 obvious

By further applying Liaw's teachings, a POSITA also would have found it obvious to retain Lan's cap layers 912 and 918 in conjunction with metal gate layers 910 and 916. (Ex-1003 ¶¶178-192; see Lan, 5:58-60.)

“[T]o avoid an undesired electrical connection between the gate conductor and the source/drain regions,” Liaw explains that “a cap layer is usually formed atop the gate conductor as a protection layer.” (Liaw, 1:45-48.) Without a cap layer, slight misalignment of a source/drain contact can cause “the circuit [to] be shorted, thereby causing failure,” as Liaw’s FIG. 1B illustrates. (*Id.*, 2:50-59.)

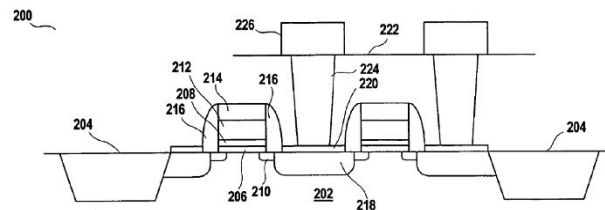


Liaw, FIG. 1A (aligned)

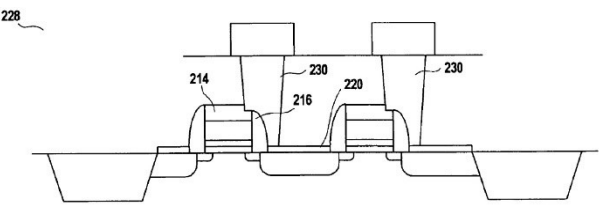


Liaw, FIG. 1B (misaligned)

An insulating gate cap layer—like cap layer 214 in Liaw’s FIG. 2B below—prevents this problem, a solution Liaw calls “self-aligned” source/drain contact plugs. (Liaw, 3:19-29, FIGS. 2A-2B; *see id.*, 4:48-51; Ex-1003 ¶¶179-180.)



Liaw, FIG. 2A (aligned)



Liaw, FIG. 2B (misaligned)

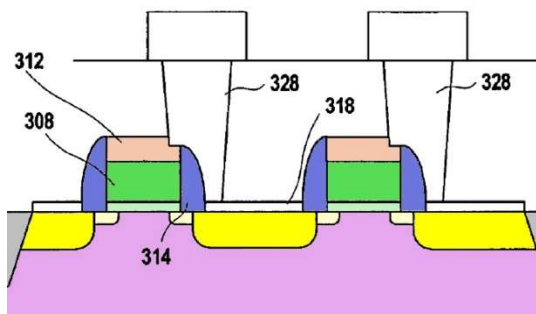
Forming such a gate cap layer on a polysilicon gate conductor can be challenging because the required gate silicidation process “significantly increases the fabrication overhead.” (Liaw, 3:30-49.) This causes what Liaw calls “the dilemma of choosing between a salicide layer on the poly-silicon gate conductor and

a self-aligned contact on the source/drain regions.” (Liaw, 4:63-66.) To avoid this dilemma, Liaw teaches a “MOS device with a gate structure of a non-poly-silicon material”—namely, a metal. (Liaw, 1:51-54; *see also id.*, Title.)

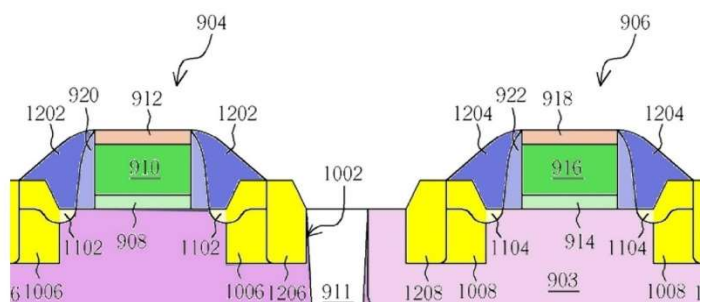
When using polysilicon gate conductor layers 910 and 916, Lan teaches to perform a salicide process “on the gates 904, 906, and the source/drain 1206, 1208.” (Lan, 4:56-58, 5:35-37.) This would involve **removing** Lan’s cap layers 912 and 918. (*Supra* §VI.B.4.a; Ex-1003 ¶¶169-170, ¶182.) Lan thus faces Liaw’s dilemma. (Liaw, 4:63-66; *see* Ex-1003 ¶182.) To achieve self-aligned source/drain contacts in Lan’s polysilicon-gate embodiment, Liaw teaches that multiple salicide processes are required. (*See* Liaw, 3:30-49; Ex-1003 ¶182.) This “significantly increases the fabrication overhead,” “complicates the fabrication process and increases costs.” (Liaw, 3:44-49.) But Lan’s “gate is not limited [to] poly-silicon, and it also can be made by ... any conductive material, such as metal.” (Lan, 5:58-60.)

Consistent with Lan’s alternative embodiment, Liaw teaches to use a metal gate conductor to avoid the dilemma above. (*Compare* Lan, 5:58-60 (“The gate ... can be made by ... any conductive material, such as metal.”), *with* Liaw, 1:58-67 (“[T]he gate structure includes ... a metal gate conductor disposed on the gate dielectric layer, [and] a cap layer disposed on the metal gate conductor”).) In fact, Liaw’s transistors have the same gate configuration as Lan’s alternative metal-gate embodiment. (*Compare* Liaw, 4:6-20, *with* Lan, 4:56-58, 5:58-60; Ex-1003

¶184.) Like Lan, Liaw's gate conductors are formed with a metal. (*Compare* Lan, 5:58-60 *with* Liaw, 3:58-65.) And Liaw's cap layer may be "an oxide layer or a layer of oxide covered by a layer of silicon nitride" (Liaw, 4:15-20), which satisfies Lan's objective for the cap layer to provide etch selectivity over the semiconductor substrate (Lan, 4:65-67). (*See* Ex-1003 ¶185; Ex-1011, 68, Tbl. 10-3.) Thus, when Lan states that "[t]he gate is not limited by the above poly-silicon, and it also can be made by ... any conductive material, such as metal" (Lan, 5:58-60), a POSITA would have understood Lan is describing a configuration like Liaw's (Ex-1003 ¶¶184-185). The figures below highlight their similarities.



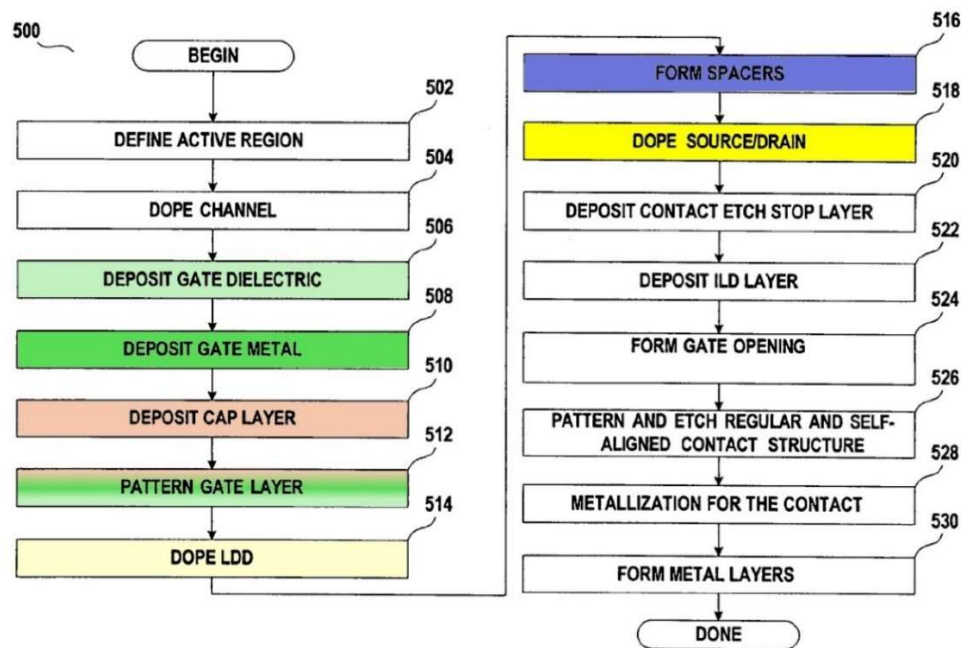
Liaw, FIG. 3B (excerpted)



Lan, Fig. 12 (excerpted)

As Liaw's chart below illustrates, the Lan and Liaw process flows are also similar. Both deposit and pattern gate dielectric, gate conductor, and cap layers to form a gate structure. Both also form LDD regions, gate sidewall spacers, and deep source/drain regions, in that order. (*Compare* Liaw, 3:50-4:36, 6:20-33, FIG. 5, *with* Lan, 4:49-5:35, Figs. 9-12; Ex-1003 ¶186.) And both disclose a salicide process

performed on the source/drain regions. (*Compare* Liaw, 4:36-38, *with* Lan, 5:35-37; Ex-1003 ¶186.) Thus, merely by retaining cap layers 912 and 918, Lan's metal-gate embodiment would implement Liaw's solution. (*See* Liaw, 4:63-5:8; Ex-1003 ¶187.)



Liaw, FIG. 5

A POSITA would have been motivated to implement Lan's metal-gate embodiment—and to retain cap layers 912 and 918 when doing so—because it avoids the increased overhead, added complexity, and increased costs associated with implementing self-aligned source/drain contacts in Lan's polysilicon-gate embodiment. (Liaw, 3:44-49; *see also id.*, 2:50-59, 3:44-49, 4:63-5:23, FIGS. 1B, 2B, 3B; Ex-1003 ¶188.) Liaw explains:

[S]ince the gate conductor 308 is made of metal, *no salicide layer is needed* for improving its interface quality with a metal interconnection structure. This naturally solves the dilemma by

choosing to form the self-aligned contact 318 atop the source/drain regions 316, without sacrificing the contact quality of the metal gate conductor 308. In addition, ***by keeping the cap layer 312 atop the metal gate conductor 308***, the MOS device 300 is able to tolerate a slight misalignment of the conductive plug 322.

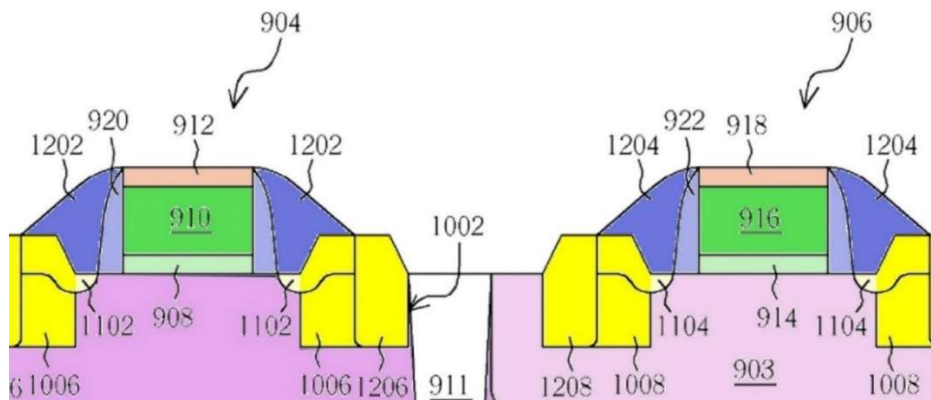
(*Id.*, 4:66-5:8, emphases added.) By retaining the cap layer, Liaw teaches that “[e]lectrical contact is, as intended, only made to the salicide source/drain contact 318, since the insulating cap layer 312 insulates the metal gate conductor 308 from being exposed.” (*Id.*, 5:18-21.) Thus, simply by retaining cap layers 912 and 918, Lan’s metal-gate embodiment achieves improved misalignment tolerance for the source/drain contacts. (*Id.*, 5:22-23; Ex-1003 ¶188.)

Moreover, retaining the cap layers avoids the various problems noted in the preceding subsection. (*Supra* §VI.B.4.a; Ex-1003 ¶189.)

A POSITA would have reasonably expected success because, as Liaw demonstrates, this approach requires no structural or process changes other than simply retaining Lan’s cap layer. (*See* Liaw, 4:63-5:23, 6:16-42, FIGS. 3B, 5; Ex-1003 ¶190.) Indeed, Liaw’s gate structure is exactly what a POSITA would have envisioned when Lan states the gate conductor may be a “metal,” because Liaw also includes dielectric capping materials that satisfy Lan’s etch selectivity requirements for source/drain recess etching. (Lan, 3:48-54, 5:58-60; Ex-1003 ¶190.)

A POSITA would have found such a combination of Lan and Liaw to be an example of (1) simply adopting one disclosed element (metal gate conductor) instead of another (polysilicon gate conductor) to obtain predictable results; (2) using a known technique (using a cap layer to protect a metal gate conductor) to improve similar devices in the same way; (3) applying a known technique (using a cap layer to protect a metal gate conductor) to a known device ready for improvement to yield predictable results; and (4) a teaching, suggestion, or motivation in the prior art (e.g., Liaw's teachings to use a metal gate conductor in a device like Lan's) that would have led one of ordinary skill to modify Lan to arrive at the claimed invention. (*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-21 (2007); Ex-1003 ¶191.)

In this configuration, Lan's cap layers 912 and 918 are positioned on the Lan's metal layers 910 and 916, as Fig. 12 shows below. Accordingly, the combination of Lan and Liaw discloses a cap layer (e.g., Lan's cap layers 912 and 918) positioned on the conductive layer (e.g., Lan's metal layers 910 and 916). (Ex-1003 ¶192.)



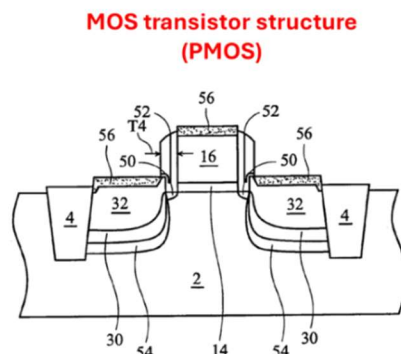
Lan, Fig. 12 (excerpted)

C. Grounds 2A and 2B: Wang407 Anticipates (Ground 2A) and Renders Obvious (Ground 2B) Claims 1 and 3-11

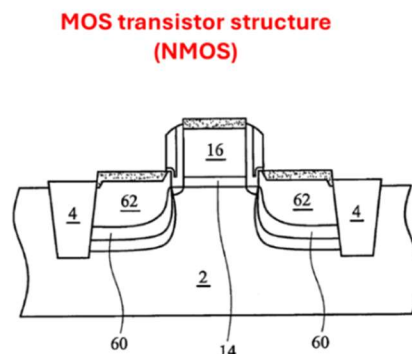
1. Independent Claim 1

a. [1pre]

Wang407 discloses “[a] novel method for forming stressors in metal-oxide-semiconductor (MOS) devices,” such as the PMOS and NMOS devices in Figs. 9 and 11 below. (Wang407, 3:15-16; *see id.*, 1:7-9, 2:59-3:2, 3:15-22, 5:58-62, Figs. 1-11.) Each has a MOS transistor structure. (Ex-1003 ¶¶196-197.)

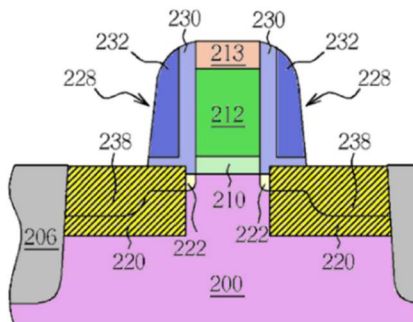


Wang407, Fig. 9

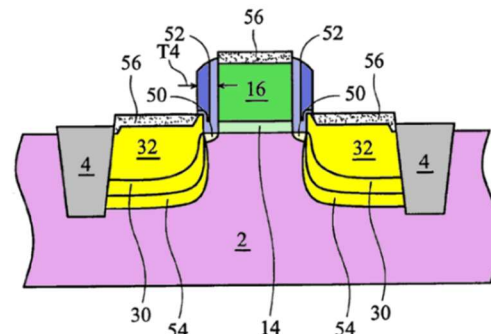


Wang407, Fig. 11

As the comparison below demonstrates, Wang407’s transistors have the same basic arrangement as the transistors the ’847 Patent describes. (Ex-1003 ¶198.)



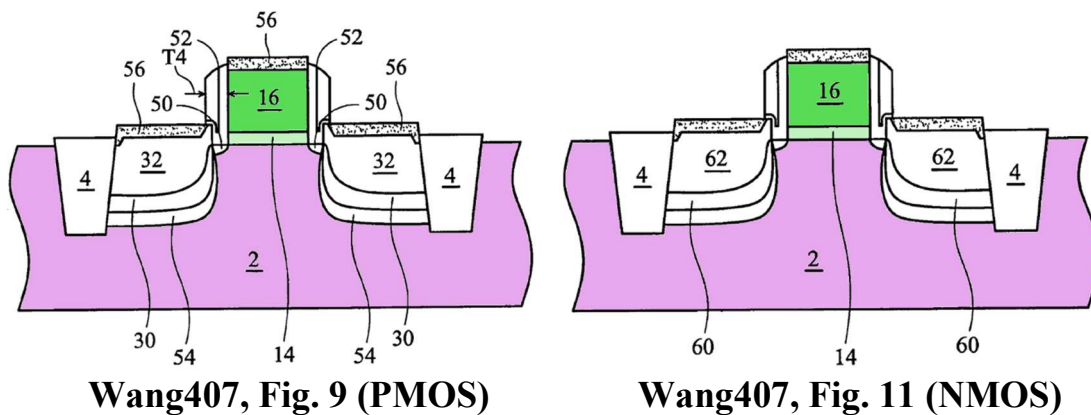
’847 Patent, Fig. 5 (excerpted)



Wang407, Fig. 9

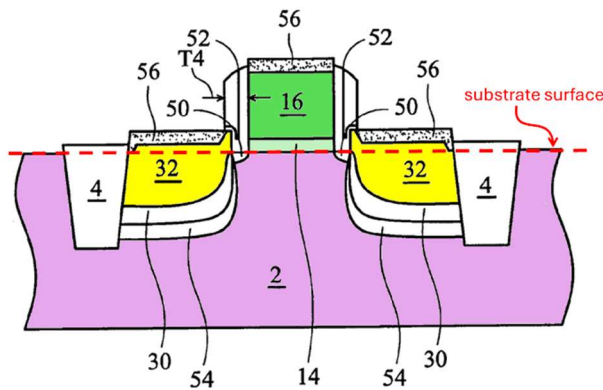
b. [1a]

Wang407 discloses “[a] gate stack 12 comprising a gate dielectric 14 [and] a gate electrode 16 ... formed on substrate 2.” (Wang407, 3:31-33). Substrate 2 may be “bulk silicon”—a semiconductor substrate. (*Id.*, 3:23-25; Ex-1003 ¶200.) Accordingly, Wang407 discloses a gate (gate stack 12) formed on a semiconductor substrate (substrate 2), as Figs. 9 and 11 show. (Ex-1003 ¶¶199-201.)

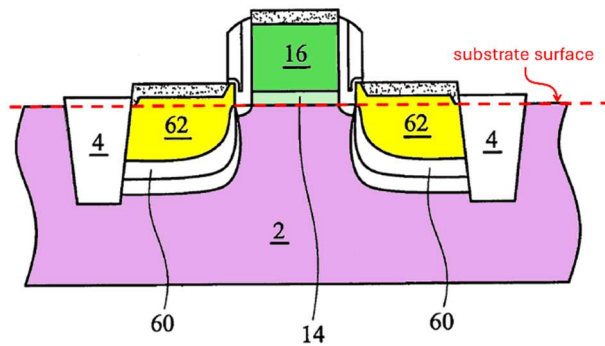


c. [1b]

Wang407 discloses “SiGe regions 32” (PMOS) and “SiC regions 62” (NMOS). (Wang407, 4:34-38, 5:60-65.) These regions comprise epitaxial layers, i.e., layers formed by crystal growth. (*Id.*, 4:34-38 (describing “process conditions for epitaxial growth ... to form [PMOS] SiGe regions 32”), 5:58-67 (explaining the same concept “may also be used with the formation of NMOS” by using SiC; describing the SiC “lattice constant”); Ex-1003 ¶203.) The epitaxial layers grow in recesses etched into the substrate adjacent to the sides of the gates. (Wang407, 3:63-4:6, 4:33-38, 5:47-60, Figs. 5-7; Ex-1003 ¶204.)



Wang407, Fig. 9



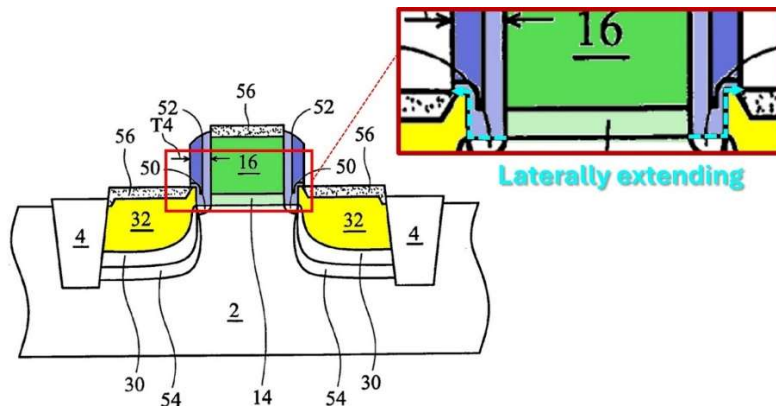
Wang407, Fig. 11

As Figs. 9 and 11 illustrate, a POSITA would have understood (Ground 2A), and at least found obvious (Ground 2B), that regions 32 and 62 each have the structure recited in [1b]. (Ex-1003 ¶205; *see Univ. of Cal.*, 2024 WL 4972639, at *3.) Each of regions 32 and 62 comprises two raised epitaxial layers⁷ positioned (a) in the substrate (substrate 2); (b) next to the relative sides of the gate stack (gate stack 12); and (c) above the surface of the substrate (substrate 2). (Wang407, Figs. 9, 11; *supra* §II.B (describing raised source/drain epitaxy); Ex-1003 ¶¶205-206 (discussing Ex-1012, 2, Fig. 6; Ex-1013, 1-3, Figs. 2-5; Ex-1016, 4, Fig. 1; Ex-1019, 4-5, Fig. 4; Ex-1017 ¶¶[0030]-[0032], FIG. 9; Ex-1015, FIGS. 4-7; Ex-1018, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13).)

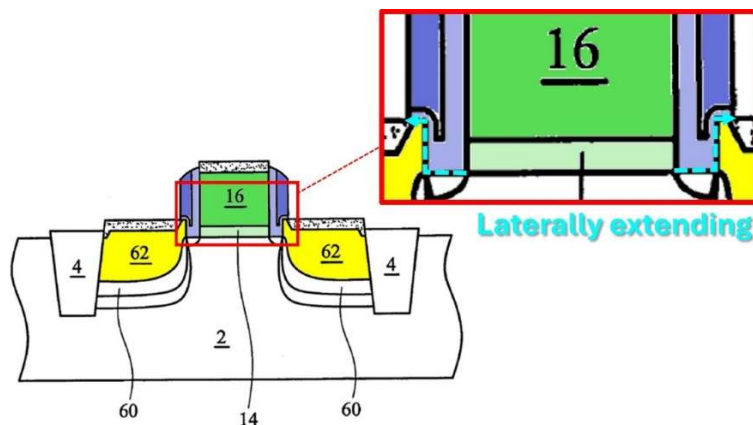
⁷ The “two raised epitaxial layers” may further include SiGe regions 30 or SiC regions 60. (Wang407, 4:4-38, 5:58-6:4; Ex-1003 ¶205.)

d. [1c]

Wang407 discloses “a liner oxide layer and a nitride layer [that] are blanket formed” and “then patterned to form spacers 52,” shown below in light and dark purple, respectively. (Wang407, 4:61-64, Fig. 9.) As Figs. 9 and 11 show, a POSITA would have understood spacers 52 are (a) formed on the sidewall of the gate (gate stack 12) and (b) extend laterally upon a portion of the raised epitaxial layer (SiGe region 32 and SiC region 62). (Ex-1003 ¶¶208-210; *see Univ. of Cal.*, 2024 WL 4972639, at *3.)



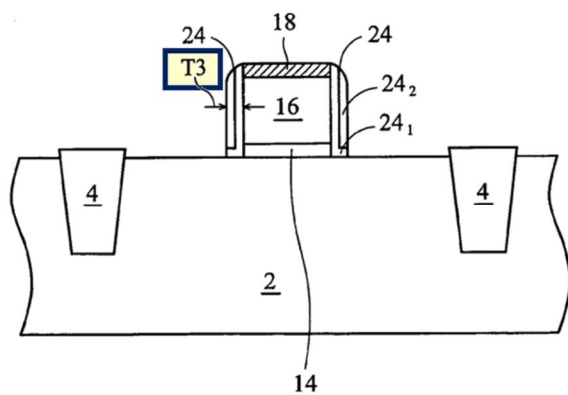
Wang407, Fig. 9 (magnified)



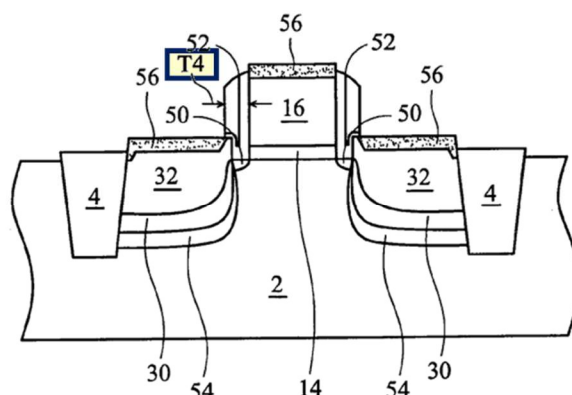
Wang407, Fig. 11 (magnified)

Recesses 26, where epitaxial growth of Wang407's SiGe regions 32 and SiC regions 62 takes place, "are formed along the edges of dummy spacers 24." (Wang407, 3:63-65; *see id.*, 4:33-40, Figs. 5-7.) Dummy spacers 24 have a thickness T3, as Fig. 4 shows. (*Id.*, 4:64-67.) Thus, SiGe regions 32 and SiC regions 62 are spaced a distance T3 away from gate stack 12. (Ex-1003 ¶210.)

Wang407's "spacers 52 have a thickness T4 greater than a thickness T3 of dummy spacers 24." (Wang407, 4:64-67, Fig. 4 (showing T3), Fig. 9 (showing T4).) Because T4 is **greater** than T3, spacers 52 necessarily extend laterally onto a portion of SiGe regions 32 and SiC regions 62. (*See id.*, 4:64-67, Figs. 4, 9; Ex-1003 ¶210.)



Wang407, Fig. 4

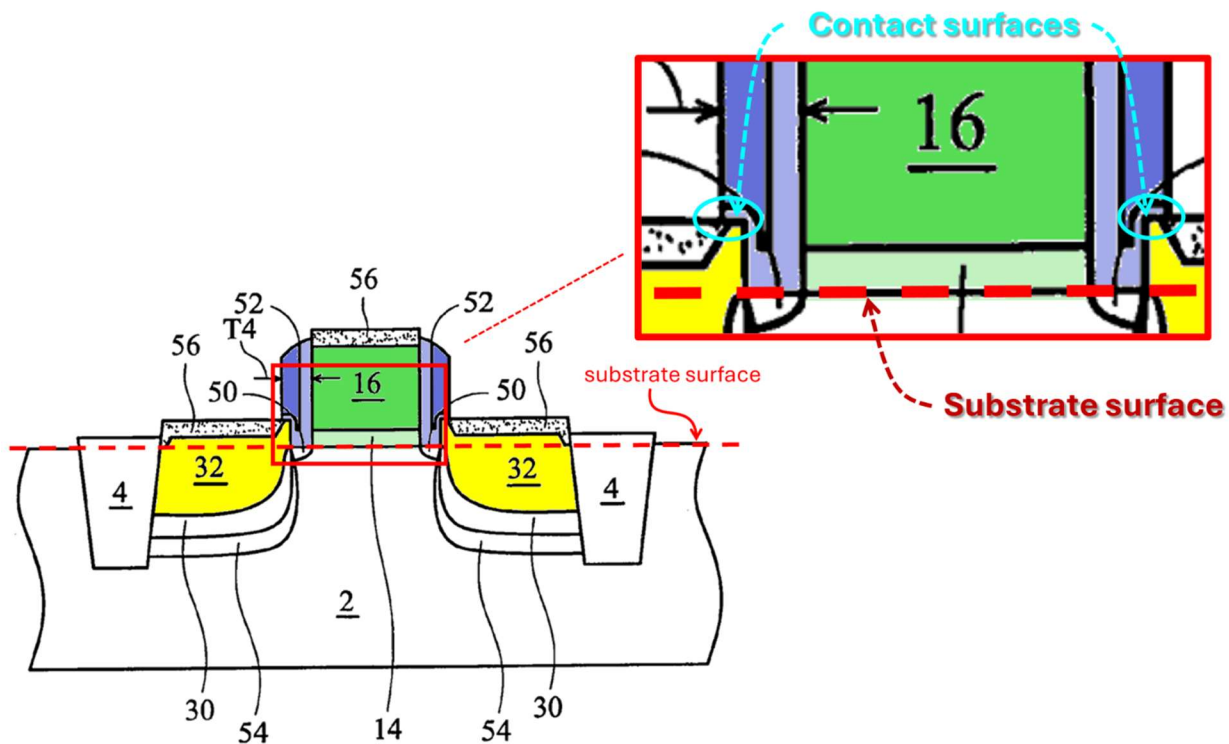


Wang407, Fig. 9

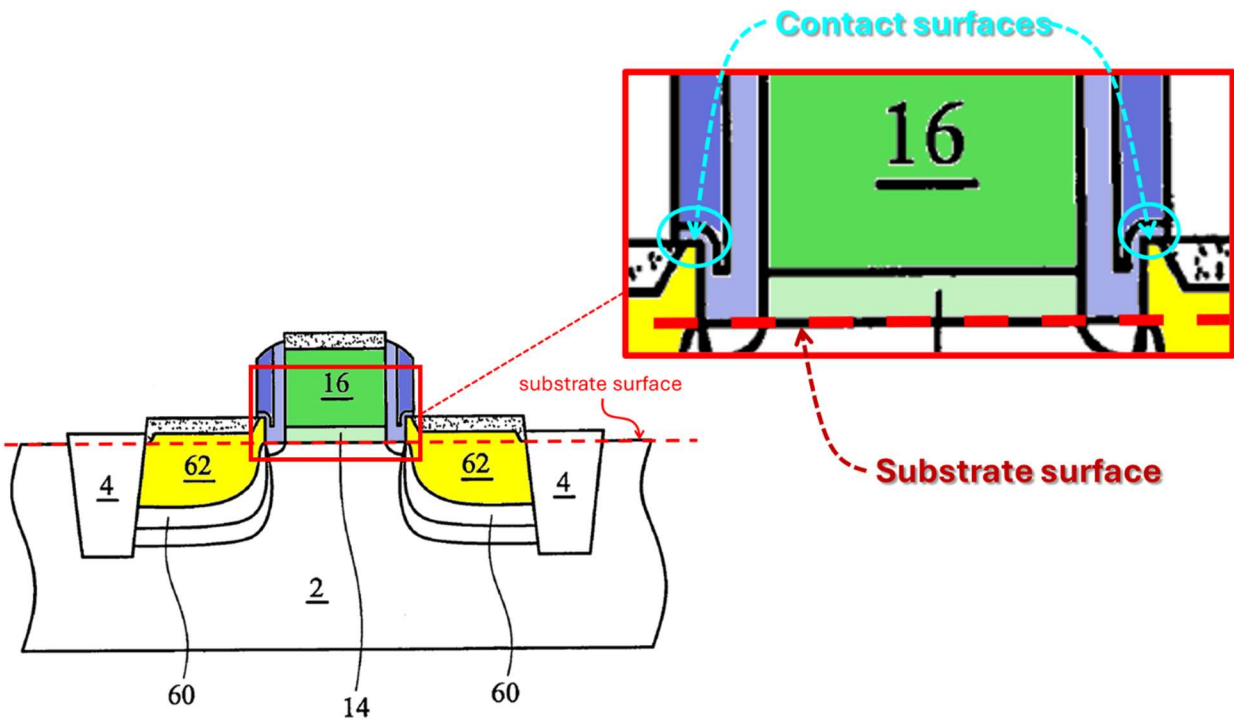
e. [1d]

As explained for [1c], Wang407's spacers 52 extend onto a portion of SiGe regions 32 and SiC regions 62. The portions of SiGe regions 32 and SiC regions 62 onto which spacers 52 extend define contact surfaces, each having a width $T4 - T3$.

(Wang407, 4:64-67, Figs. 4-7, 9, 11; *supra* §VI.C.1.d; Ex-1003 ¶212.) Moreover, as explained for [1b], a POSITA would have understood (Ground 2A), and at least found obvious (Ground 2B), that SiGe regions 32 and SiC regions 62 extend above the substrate surface. (*Supra* §VI.C.1.c; Ex-1003 ¶212].) Thus, as Figs. 9 and 11 confirm, a POSITA would have understood (Ground 2A), and at least found obvious (Ground 2B), that contact surfaces between the raised epitaxial layers (e.g., SiGe regions 32 or SiC regions 62) and a bottom of the spacer (e.g., spacers 52) lie above the surface of the semiconductor substrate (substrate 2). (Ex-1003 ¶212; Ex-1001, Figs. 5, 14.)



Wang407, Fig. 9 (annotated & magnified)



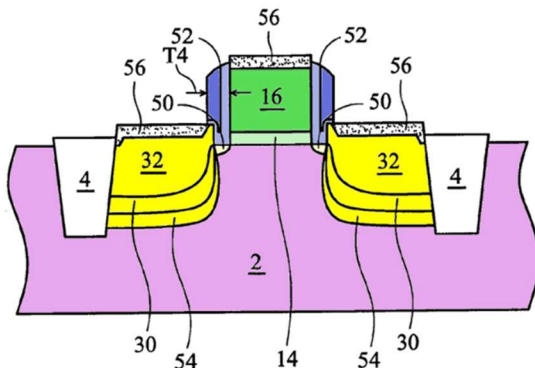
Wang407, Fig. 11 (annotated & magnified)

Although “silicide regions 56” are formed on SiGe regions 32 and SiC regions 62, they form on “exposed surfaces,” not on the contact surfaces where spacers 52 overlap with the epitaxial layers (see above). (Wang407, 5:3-7, Figs. 9, 11; Ex-1024, 40, Fig. 12.13; Ex-1003 ¶213.)

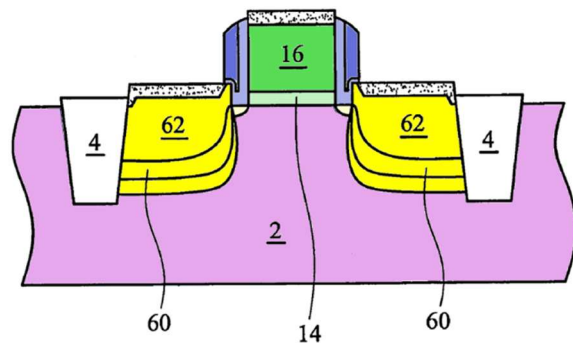
f. [1e]

On both sides of PMOS gate stack, Wang407 discloses source/drain regions comprising SiGe epitaxy regions 30 and 32, lightly doped source/drain (LDD) regions 50, and deep source/drain regions 54. (Wang407, 4:4-6, 4:34-58, 5:1-3, Figs. 8-9; Ex-1003 ¶215.) Wang407’s LDD regions 50 and deep source/drain regions 54 are formed by implanting p-type impurities, and they extend beyond SiGe

epitaxial regions 30 and 32 into substrate 2, as Fig. 9 shows. (Wang407, 4:55-58, 5:1-3, Fig. 8 (showing LDD regions 50 in substrate 2); Ex-1003 ¶216.) Although not specifically labeled, Wang407 illustrates these same regions in Fig. 11 and explains that the same concepts “may also be used with the formation of NMOS devices.” (Wang407, 5:58-62; *see id.*, claims 6, 13.)

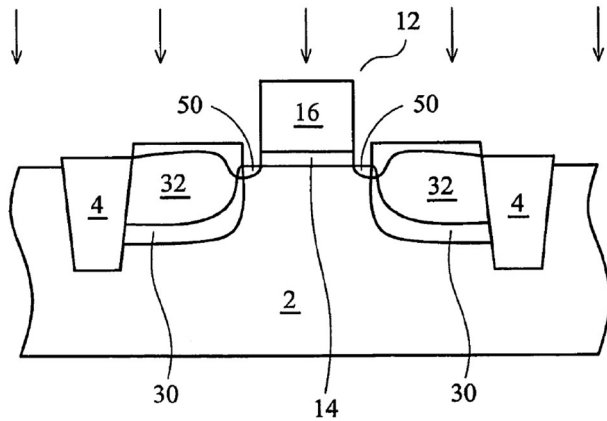


Wang407, Fig. 9

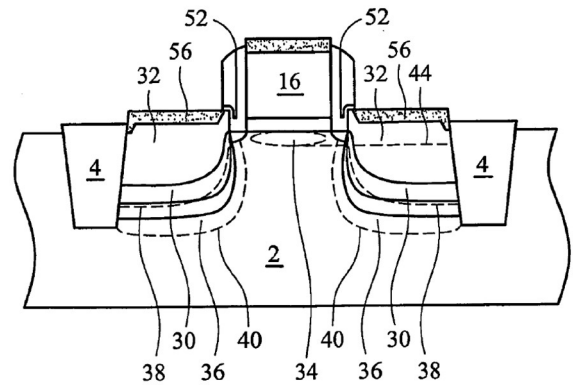


Wang407, Fig. 11

LDD regions 50 are formed with dummy spacers 24 removed, as in Fig. 8 below. (*Id.*, 4:49-58.) Only “[g]ate stack 12 acts as a mask” to the LDD p-type dopant ions, such that LDD regions 50 form in both SiGe epitaxial regions 32 and substrate 2. (*Id.*, 4:56-58; Ex-1003 ¶217.) Then, after forming spacers 52, deep source/drain regions 54 are formed by implanting p-type impurities into SiGe epitaxial regions 30 and 32 and portions of substrate 2 underneath, as Fig. 9 illustrates. (Wang407, 5:1-3; Ex-1003 ¶217.)



Wang407, Fig. 8



Wang407, Fig. 10

Wang's Fig. 10 describes an effect of this source/drain configuration. (Wang407, 5:1-46, Fig. 10; Ex-1003 ¶218.) A POSITA would have understood depletion regions 36 that lie between dotted lines 38 and 40 are characteristic of MOSFET source/drain regions, forming around the boundary between the source/drain regions and the rest of the substrate. (Wang407, 5:14-37; *see* Ex-1010, 14-15, Fig. 6; Ex-1021, 28-29, Fig. 5-17; Ex-1023, 23-25, Figs. 5-21, 5-22; Ex-1003 ¶218.)

As explained above, therefore, Wang407 discloses “two doped regions” (LDD regions 50 and/or deep source/drain regions 54) formed respectively in the semiconductor substrate (substrate 2) next to the relative sides of the gate (gate stack 12). (Ex-1003 ¶¶214-219.)

Additionally, if a doped epitaxial region qualifies as a “doped region formed ... in the semiconductor substrate,” then the claimed “two doped regions” may be mapped to any combination of Wang407's LDD regions 50, source/drain regions

(30, 32, 60, and 62), and/or deep source/drain regions 54. (Ex-1003 ¶220.) Like Wang407's LDD regions 50 and deep source/drain regions 54, epitaxial SiGe regions 32 and SiC regions 62 are formed next to the relative sides of the gate, as Figs. 9 and 11 confirm. (Wang407, 3:63-65, 4:33-40, Figs. 5-9, 11; Ex-1003 ¶220.)

2. Dependent Claims

a. Claim 3

Wang407 discloses and renders obvious the structure of claim 1. (*Supra* §VI.C.1.) Wang407 further discloses that the embodiment in Fig. 9 is a PMOS transistor. (Wang407, 2:63-64 (explaining FIG. 9 shows “the manufacture of a PMOS embodiment”), claim 8 (“[T]he semiconductor device comprises a PMOS device.”), claim 18 (same); Ex-1003 ¶¶221-223.)

b. Claim 4

Wang407 discloses and renders obvious the structure of claim 3. (*Supra* §VI.C.2.a.) Wang407 further discloses that the PMOS epitaxial layer in Fig. 9 (SiGe regions 32) comprises SiGe. (Wang407, 4:4-6, 4:34-38; Ex-1003 ¶¶224-226.)

c. Claim 5

Wang407 discloses and renders obvious the structure of claim 1. (*Supra* §V.C.1.) Wang407 further discloses that the embodiment in Fig. 11 is an NMOS transistor. (Wang407, 5:60-62 (explaining “FIG. 11 illustrates an NMOS device”);

claim 9 (“[T]he semiconductor device comprises an NMOS device.”), claim 19 (same); Ex-1003 ¶¶227-229.)

d. Claim 6

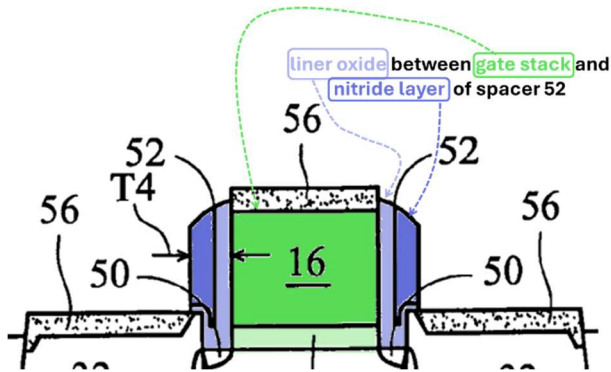
Wang407 discloses and renders obvious the structure of claim 5. (*Supra* §VI.C.2.c.) Wang407 further discloses that the NMOS epitaxial layer in Fig. 11 (SiC regions 62) comprises SiC. (Wang407, 5:60-67; Ex-1003 ¶¶230-232.)

e. Claim 7

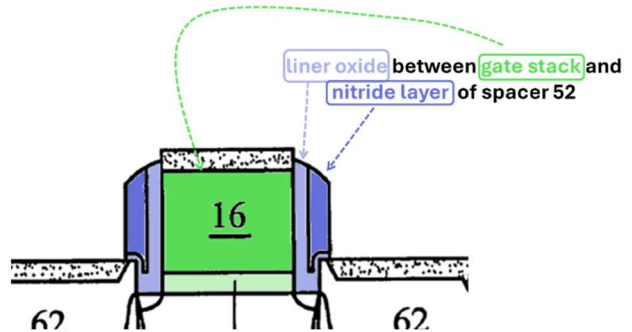
Wang407 discloses and renders obvious the structure of claim 1. (*Supra* §VI.C.1.)

Co-Petitioners expect Patent Owner to argue claim 7 may be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the gate. (*See supra* §III.C.) Wang407 discloses such an embodiment.

Wang407’s spacer (spacer 52) comprises “a liner oxide layer and a nitride layer.” (Wang407, 4:61-64.) Thus, Wang407 discloses an offset spacer (inner liner oxide of spacer 52) positioned between the gate (gate stack 12) and a portion of the “spacer” (the outer nitride layer of spacer 52), as Figs. 9 and 11 show below. (Wang407, 4:61-64; Ex-1003 ¶¶233-235.)



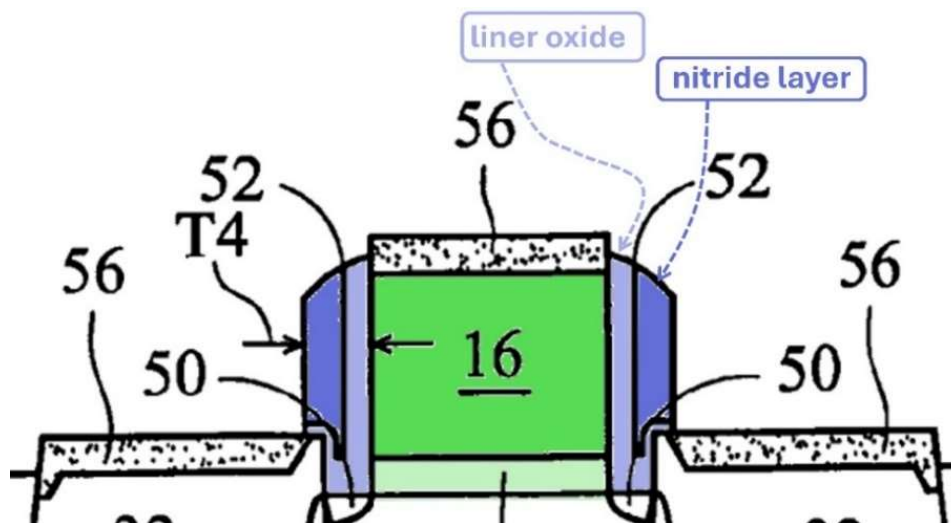
Wang407, Fig. 9 (excerpted)



Wang407, Fig. 11 (excerpted)

f. Claim 8

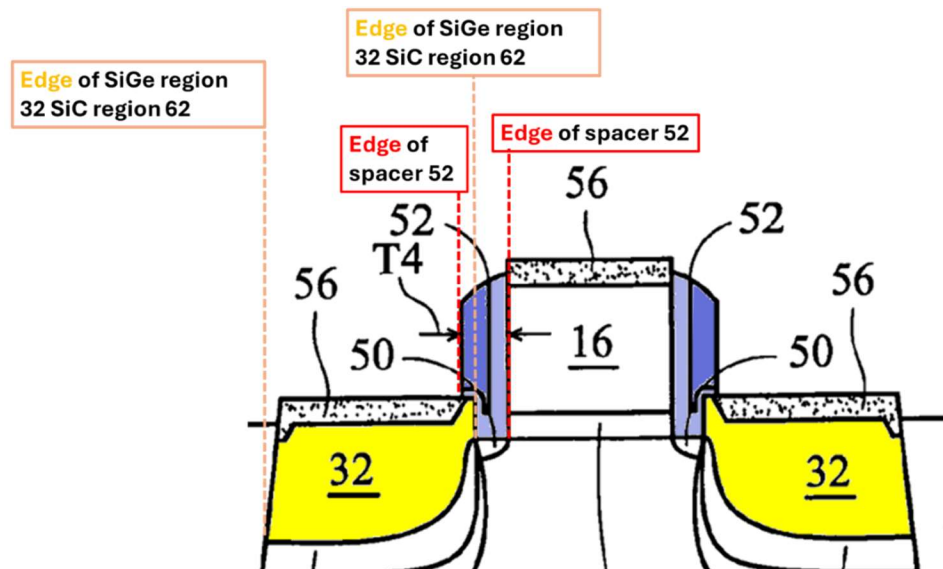
Wang407 discloses and renders obvious the structure of claim 1. (*Supra* §VI.C.1.) As the preceding subsection explains, Wang407's spacer 52 comprises "a liner oxide layer and a nitride layer." (Wang407, 4:61-64.) Accordingly, Wang407's spacer (spacer 52) comprises an oxide liner (liner oxide layer) and a nitride spacer (nitride layer). (Ex-1003 ¶¶236-238.)



Wang407, Fig. 9 (excerpted)

g. Claim 9

Wang407 discloses and renders obvious the structure of claim 1. (*Supra* §VI.C.1.) Additionally, the edge of Wang407's raised epitaxial layers (SiGe regions 32 or SiC regions 62) is not aligned with the edge of Wang407's spacers (spacers 52), as Wang407's figures confirm (*see* Fig. 9 below). (Wang407, Figs. 9, 11; Ex-1003 ¶241.)



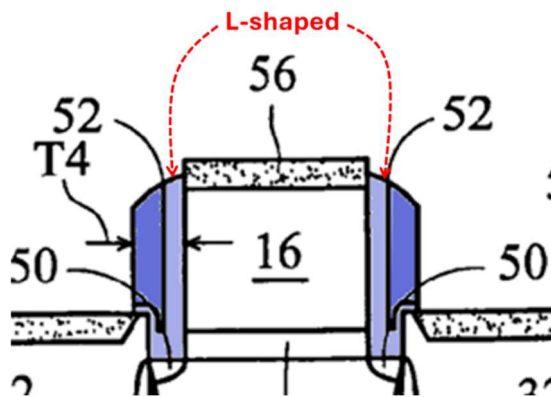
Wang407, Fig. 9 (annotated, excerpted)

As explained for [1c], Wang407's spacers 52 are thicker than dummy spacers 24, such that spacers 52 overlap SiGe regions 32 and SiC regions 62 by an amount $T4 - T3$. (*See* §VI.C.1.d; Wang407, 4:64-67.) With this configuration, shown above, the edges of the spacers and epitaxial regions cannot align because the distance from Wang407's gate stack 12 to the edge of the spacers 52 is necessarily larger than the distance to epitaxial regions 32 or 62. (Ex-1003 ¶242.) Wang407's fabrication thus

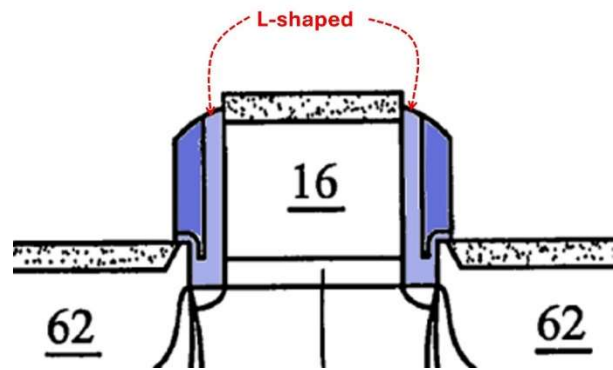
yields a device structure in which the edges of SiGe regions 32 / SiC regions 62 and spacers 52 are not aligned. (Ex-1003 ¶¶239-242.)

h. Claim 10: “The structure of claim 1, wherein the spacer further comprises a [sic] L-shaped spacer.”

Wang407 discloses and renders obvious the structure of claim 1. (*Supra* §VI.C.1.) Further, as Figs. 9 and 11 show, Wang407’s spacers 52 comprise an L-shaped spacer (liner oxide layer) with vertical portion along the gate sidewall and a substantially horizontal portion along the substrate. (See Wang407, Figs. 9, 11; Ex-1003 ¶¶243-245.)



Wang407, Fig. 9 (excerpted)



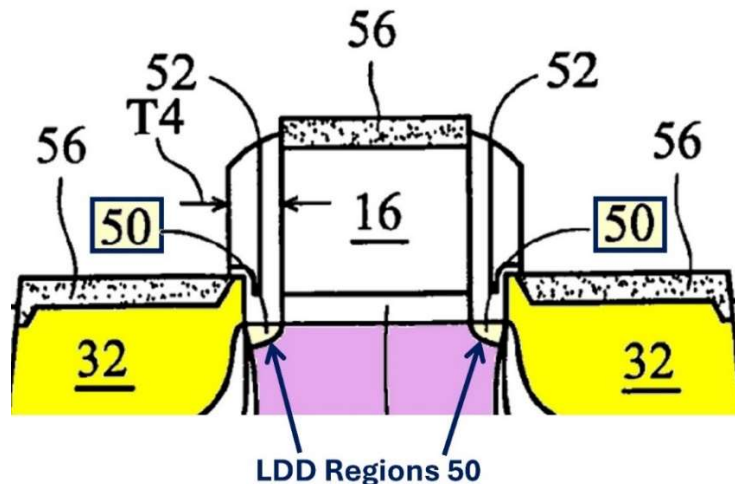
Wang407, Fig. 11 (excerpted)

i. Claim 11

Wang407 discloses and renders obvious the structure of claim 1. (*Supra* §VI.C.1.) Wang407 further discloses “[l]ightly doped source/drain (LDD) regions 50” formed “by implanting a p-type impurity.” (Wang407, 4:55-56.) This process takes place after dummy spacers have been removed, such that only

Wang407’s “gate stack 12 acts as a mask” and “LDD regions 50 are substantially aligned with the respective edge of gate stack 12.” (*Id.*, 4:56-58; *see id.*, 4:49-54, Fig. 8.) This process—making and removing a spacer to form LDD regions outside epitaxial regions—is the same process the ’847 Patent describes for forming its “lightly doped region 222.” (Ex-1001, 3:29-54, Figs. 3-4; *see* Ex-1003 ¶248.)

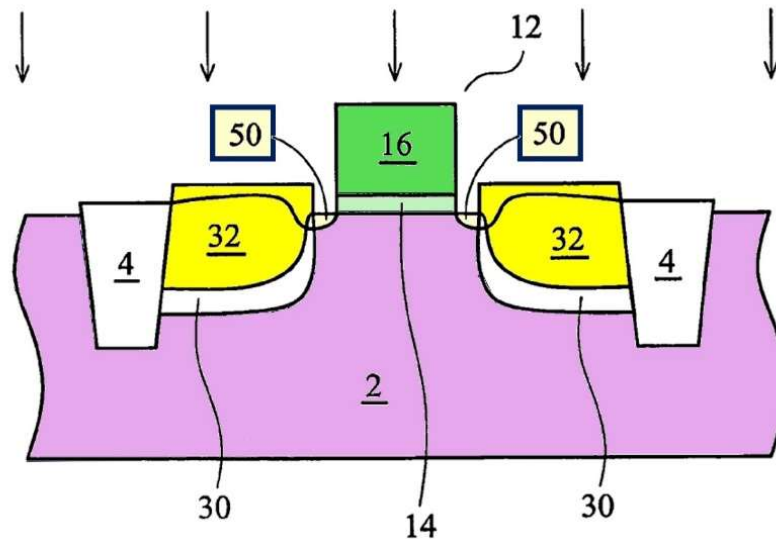
Thus, as Figs. 9 and 11 confirm, Wang407 discloses a lightly doped drain (LDD regions 50) disposed in the semiconductor substrate (substrate 2) outside the raised epitaxial layers (SiGe regions 32 or SiC regions 62). (Ex-1003 ¶¶246-249.)



Wang407, Fig. 9 (excerpted)

Epitaxial regions 32 and 62 grow selectively in recesses 26 delimited by dummy spacers 24. (Wang407 at 3:63-65, 4:34-48, Figs. 5-7.) Removing dummy spacers 24, as Fig. 8 shows below, creates a gap between the epitaxial regions and gate stack 12. (*See* Wang407 4:49-54, Fig. 8.) This exposes a portion of substrate 2 to the p-type ion implantation process used to form LDD regions 50. (Wang407,

4:55-58, Fig. 8; Ex-1003 ¶249.) Thus, LDD regions 50 form in a region that is both in substrate 2 and outside the epitaxial regions. (Ex-1003 ¶249.)



Wang407, Fig. 8

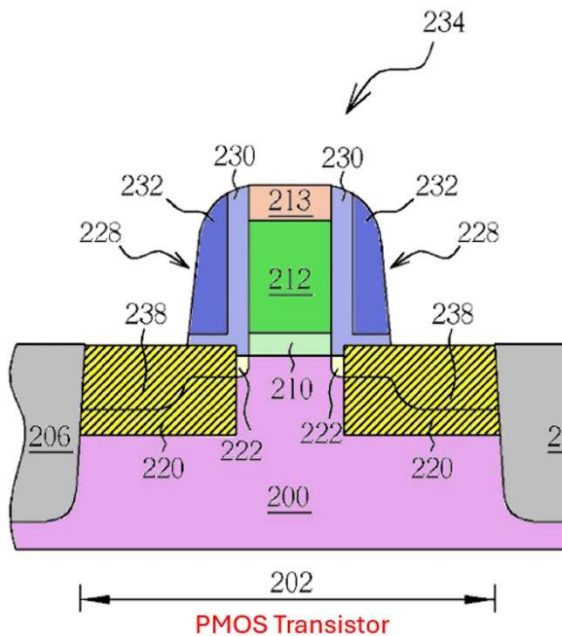
D. Grounds 3A and 3B: Wang753 Anticipates (Ground 3A) and Renders Obvious (Ground 3B) Claims 1 and 10

1. Independent Claim 1

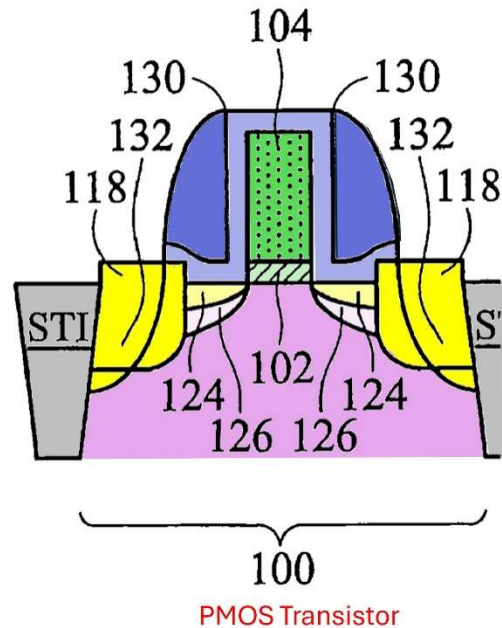
a. [1pre]

Wang753 discloses a semiconductor structure that “combines the formation of PMOS and NMOS devices for core circuits and SRAM cells.” (Wang753, 3:33-36; *see id.*, 3:43-49, FIG. 13.) Wang753’s PMOS devices (e.g., the PMOS device in core region 100) have MOS transistor structures. (Ex-1003 ¶¶253-255.)

As the comparison below demonstrates, Wang753’s transistors have the same basic arrangement as the transistors the ’847 Patent describes. (Ex-1003 ¶255.)



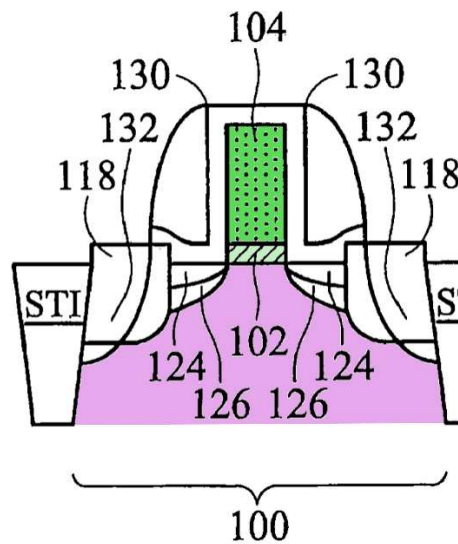
'847 Patent, Fig. 5
(PMOS excerpted)



Wang753, FIG. 13
(PMOS, excerpted)

b. [1a]

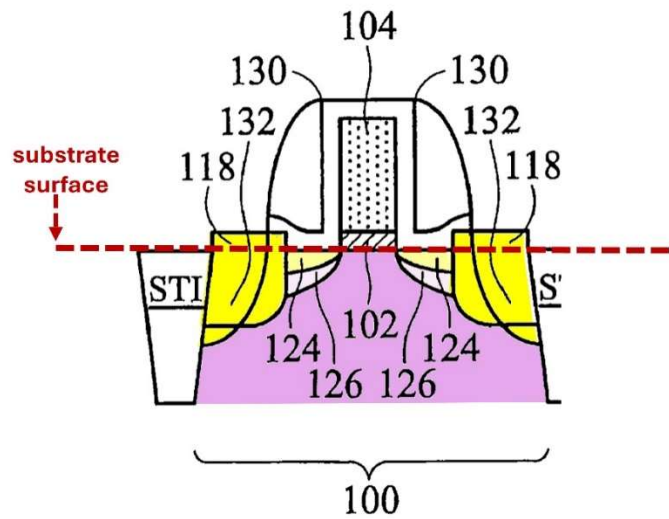
Wang753's PMOS device includes "a gate stack formed on the substrate 2" (fuchsia below). (Wang753, 3:49-52.) As FIG. 13 confirms below, the PMOS device comprises "a gate dielectric 102 on substrate 2 and a gate electrode 104 on gate dielectric 102." (*Id.*) "Substrate 2 preferably comprises bulk silicon," a well-known semiconductor substrate. (*Id.*, 3:41-43; Ex-1003 ¶257.) Accordingly, Wang753 discloses a gate (e.g., Wang753's "gate stack" comprising gate dielectric 102 and gate electrode 104) formed on a semiconductor substrate (silicon substrate 2). (Ex-1003 ¶¶256-258.)



Wang753, FIG. 13 (excerpted)

c. [1b]

Wang753's PMOS devices includes "SiGe stressors 118" in source/drain regions located next to the gate stack. (Wang753, 4:14-18; Ex-1003 ¶260.) Forming SiGe stressors 118 involves making "disposable spacers" (gate spacers 114, shown in Wang753's FIG. 4) that define "recesses 116" etched in the substrate. (Wang753, 4:10-13, 4:23-27, FIGS. 4-6.) "[T]he SiGe stressors [are] epitaxially grown in the recesses 116." (*Id.*, 4:14-17.) As Wang753's FIG. 13 illustrates below, a POSITA would have understood (Ground 3A), and at least found obvious (Ground 3B), that SiGe stressors 118 extend above the substrate surface. (*Id.*, 4:14-22; Ex-1003 ¶¶260; *Univ. of Cal.*, 2024 WL 4972639, at *3.)



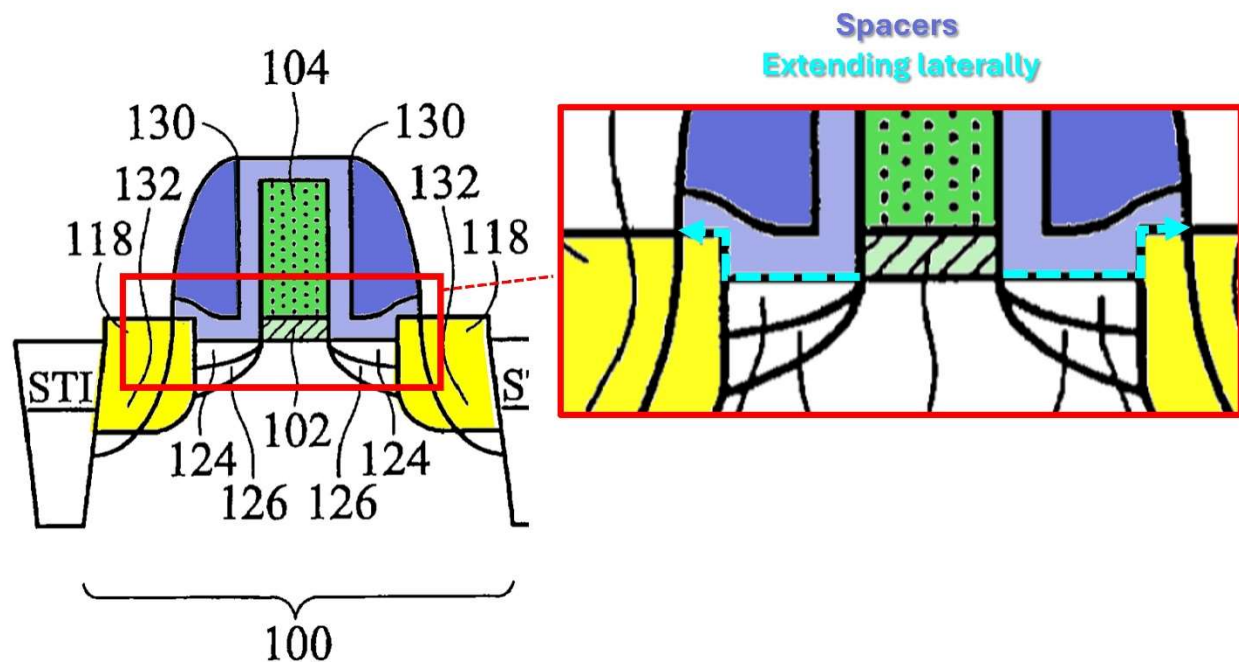
Wang753, FIG. 13 (excerpted, annotated)

Thus, Wang753 discloses (Ground 3A), and at least renders obvious (Ground 3B), two raised epitaxial layers (e.g., SiGe stressors 118) positioned respectively in the semiconductor substrate (substrate 2) next to the relative sides of the gate (e.g., Wang753’s gate stack comprising gate dielectric 102 and gate electrode 104) and above the surface of the semiconductor substrate—a typical and expected prior-art feature. (*Id.*, 4:14-22, FIG. 13; *supra* §II.B; Ex-1003 ¶¶259-262 (discussing Ex-1012, 2, Fig. 6; Ex-1013, 1-3, Figs. 2-5; Ex-1016, 4, Fig. 1; Ex-1019, 4-5, Fig. 4; Ex-1017 ¶¶[0030]-[0032], FIG. 9; Ex-1015, FIGS. 4-7; Ex-1018, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13).)

d. [1c]

Wang753 discloses “a liner oxide layer 25 and a nitride layer 27 [that] are blanket formed” on the PMOS device. (Wang753, 5:19-21; *see id.*, FIG. 10.) “The two layers are then patterned to form spacers 130 . . . as shown in FIG. 11.”

(*Id.*, 5:21-22; *see id.*, FIG. 11.). According to Wang753, spacers 130 are thicker than disposable spacers 114 used to define the distance between the gate and SiGe stressors 118. (*Id.*, 5:22-25). “As a result, spacers 130 ... have portions on SiGe stressors 118.” (*Id.* 5:25-27.) Wang753’s spacers 130 are thus formed after, and on portions of, SiGe stressors 118. (Wang753, 5:19-27, FIGS. 6-13.) As Wang753’s FIG. 13 confirms, the spacers extend laterally on top of a portion of the SiGe stressors 118. (Ex-1003 ¶264.)

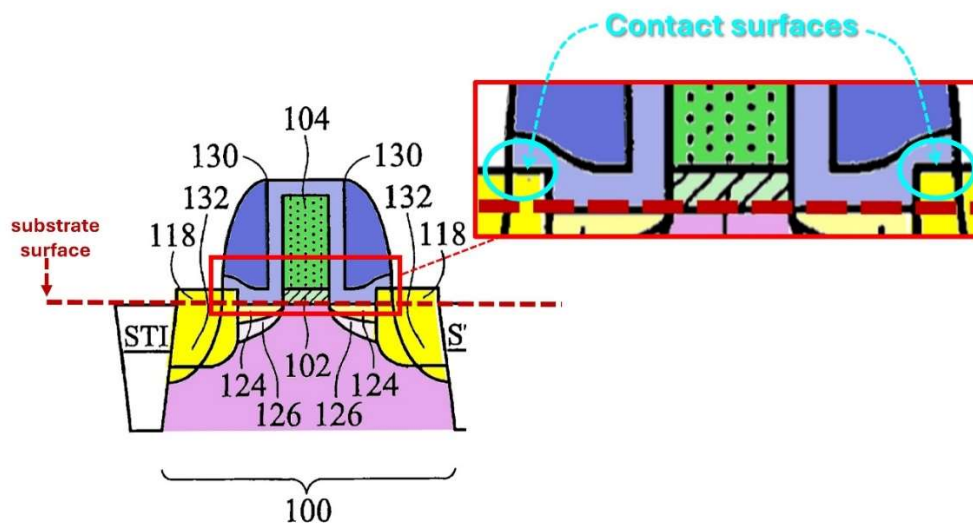


Wang753, Fig. 13 (magnified, annotated)

Accordingly, Wang753 discloses a spacer (spacers 130) formed on the sidewall of the gate (Wang753’s gate stack comprising gate dielectric 102 and gate electrode 104) and extending laterally upon a portion of the raised epitaxial layer (SiGe stressors 118 adjacent to the gate stack). (Ex-1003 ¶¶263-265.)

e. [1d]

As explained for [1c], Wang753's spacers (spacers 130) extend laterally onto a portion of SiGe stressors 118 adjacent to the gate stack. (*See* Wang753, FIG. 13; *supra* §VI.D.1.d.) The portions of SiGe stressors 118 onto which Wang753's spacers 130 extend define contact surfaces. (*See* Wang753, FIG. 13; Ex-1003 ¶267.) Moreover, as explained for [1b], a POSITA would have understood (Ground 3A), and at least found obvious (Ground 3B), that the upper surfaces of SiGe stressors 118 are located above the substrate surface. (*See supra* §VI.D.1.c.) Thus, as FIG. 13 confirms, Wang753 discloses (Ground 3A), and at least renders obvious (Ground 3B), that a contact surface of the raised epitaxial layers (SiGe stressors 118 adjacent to the gate stack) and a bottom of the spacer (bottom of spacers 130) is above the surface of the semiconductor substrate (substrate 2, in fuchsia). (Ex-1003 ¶¶266-267.)

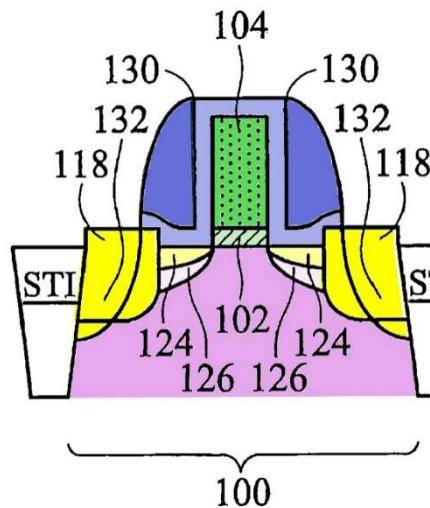


Wang753, FIG. 13 (excerpted, annotated, magnified)

f. [1e]

On both sides of the gate stack, Wang753 discloses source/drain regions comprising SiGe stressors 118, LDD regions 124, and deep source/drain regions 132. (Wang753, 4:14-18, 4:46-51, 5:36-42, FIG. 13.)

SiGe stressors 118 are preferably doped with “P-type impurities such as boron ... during epitaxial growth.” (*Id.*, 4:14-18.) “LDD regions 124 are formed by introducing p-type impurities” into the substrate.” (*Id.*, 4:49-51; *see id.*, 4:29-37, 4:46-51, FIG. 8; Ex-1003 ¶269.) And “deep source/drain regions 132,” which are “substantially aligned with edges of the spacers 130,” are also formed by “implanting p-type impurities.” (*Id.*, 5:36-42.)



Wang753, FIG. 13 (excerpted)

As FIG. 13 confirms, the LDD regions 124 lie next to the gate stack (green). According to Wang753, those LDD regions are “substantially aligned with the edges of the gate electrodes.” (*Id.*, 4:34-36.) Accordingly, Wang753 discloses two doped

regions (e.g., LDD regions 124) formed respectively in the semiconductor substrate (substrate 2) next to the relative sides of the gate (Wang753's gate stack comprising gate dielectric 102 and gate electrode 104). (Ex-1003 ¶¶268-270.)

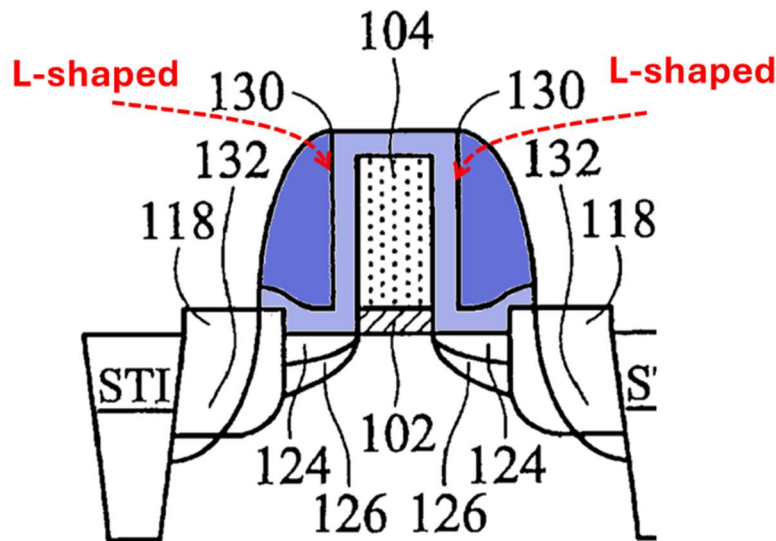
Additionally, if a doped epitaxial region qualifies as a “doped region formed ... in the semiconductor substrate,” then the claimed “two doped regions” may be mapped to any combination of Wang753's SiGe stressors 118, LDD regions 124, or deep source/drain regions 132. (Ex-1003 ¶271.) All these regions are doped, and, as FIG. 13 confirms, formed next to the relative sides of Wang753's gate stack. (Ex-1003 ¶271.)

2. Dependent Claim 10

Wang753 discloses and renders obvious the structure of claim 1. (*Supra* §VI.D.1.) Further, as FIG. 13 shows below, spacers 130 comprise an L-shaped “liner oxide layer 25” (light purple) with a vertical portion along the sidewall of the gate stack and a substantially horizontal portion along the substrate.⁸ (*See* Wang753,

⁸ Although immaterial, a POSITA would have understood liner oxide layer 25 (light purple) does not extend over the gate stack. Liner oxide layer 25 is “patterned to form spacers 130 ... as shown in FIG. 11.” (Wang753, 5:19-22.) Consistent with the process described in Wang753, liner oxide layer 25 would appear as in FIGS. 11

FIG. 13.) Accordingly, a POSITA would have understood (Ground 3A), and at least found obvious (Ground 3B), that Wang753's spacer (spacers 130) comprises an L-shaped spacer (liner oxide layer 25). (Ex-1003 ¶¶272-280.)



Wang753, Fig. 13 (excerpted)

E. Grounds 4A and 4B: Chen Anticipates (Ground 4A) and Renders Obvious (Ground 4B) Claims 1-2 and 7-8

1. Independent Claim 1

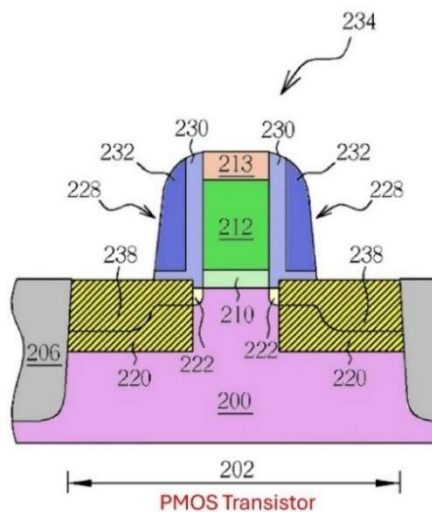
a. [1pre]

Chen “provides a method and structures for manufacturing MOS devices using strained silicon structures.” (Chen, 1:17-20.) This includes fabrication of a “CMOS device” with “NMOS gate structure (not shown)” and “PMOS gate structure (not shown).” (Chen, 1:21-22.)

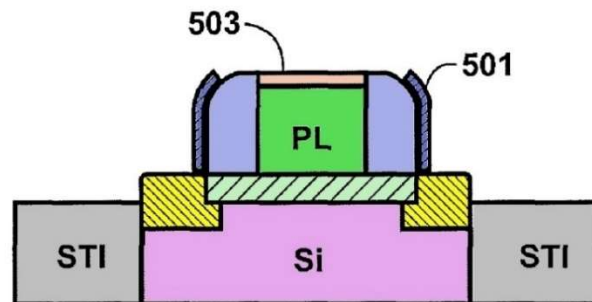
and 12, not as in FIG. 13. A POSITA would have identified this as a drawing error. (See Wang753, 5:19-42, FIGS. 11-13; Ex-1003 ¶¶275-279.)

structure 109.” (Chen, 4:15-56.) Chen’s PMOS structure in FIG. 5 is a MOS transistor structure. (Ex-1003 ¶¶284-286.)

As the comparison below demonstrates, Chen’s transistors have the same basic arrangement as the transistors the ’847 Patent describes. (Ex-1003 ¶286.)



'847 Patent, Fig. 5 (PMOS excerpted)



Chen, FIG. 5 (PMOS)

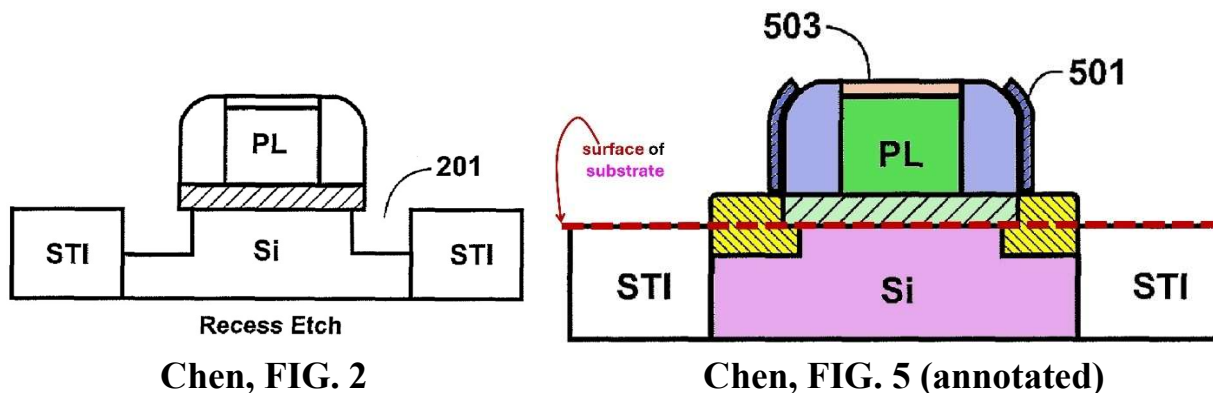
b. [1a]

Chen discloses “a semiconductor substrate 101” (fuchsia in FIG. 5 above) and “a gate dielectric layer 107 [light green in FIG. 5 above] overlying the surface of the substrate.” (Chen, 4:19-23, 4:30-35). Chen also discloses “a gate layer [dark green in FIG. 5 above] overlying the semiconductor substrate.” (*Id.*, 4:35-38.) In one embodiment, Chen’s PMOS transistor further includes a “hard mask” (peach in FIG. 5 above) overlying the gate layer. (*Id.*, 4:43-57, 6:11-15.) The gate dielectric layer, gate layer, and hard mask layer form “a PMOS gate structure 109.” (Chen, 4:44-57; *see id.*, 5:9-30, FIGS. 1-2.)

Accordingly, Chen discloses a gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask) formed on a semiconductor substrate (semiconductor substrate 101). (Ex-1003 ¶¶287-289.)

c. [1b]

Chen discloses a step of etching “recessed regions” 201 located “adjacent to the PMOS gate structure,” as in FIG. 2 below. (Chen, 5:9-30, 6:35-40.) Then, “silicon germanium material 405” layers are grown those recessed regions to compress the channel. (*Id.*, 5:31-41.) The “silicon germanium is epitaxially deposited using in-situ doping techniques.” (*Id.*, 5:36-38; *see id.*, 3:52-57 (describing steps 6 (etch) and 7 (deposit)).)



As FIG. 5 illustrates, a POSITA would have understood (Ground 4A), and at least found obvious (Ground 4B), that Chen’s silicon germanium material 405 (yellow) is positioned in the substrate (fuchsia) next to the relative sides of the gate stack and rises above the substrate surface—a typical and expected prior-art feature. (*See id.*, FIG. 5; *supra* §II.B; Ex-1003 ¶¶291-292 (discussing Ex-1012, 2, Fig. 6;

Ex-1013, 1-3, Figs. 2-5; Ex-1016, 4, Fig. 1; Ex-1019, 4-5, Fig. 4; Ex-1017 ¶¶[0030]-[0032], FIG. 9; Ex-1015, FIGS. 4-7; Ex-1018, Abstract, ¶[0025], ¶[0043], FIGS. 5, 13).)

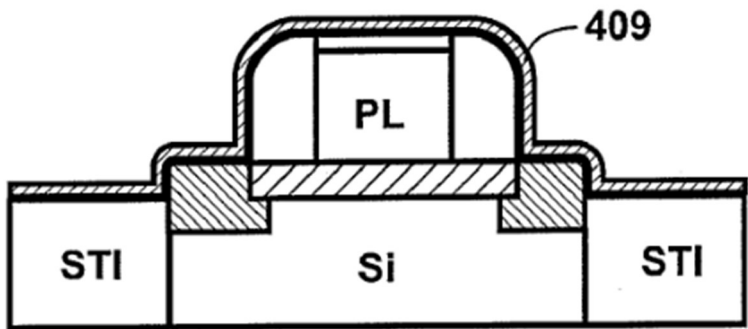
Accordingly, Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), two raised epitaxial layers (silicon germanium material 405) positioned respectively in the semiconductor substrate (semiconductor substrate 101) next to the relative sides of the gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask) and above the surface of the semiconductor substrate. (Ex-1003 ¶¶290-292)

d. [1c]

Chen discloses “sidewall spacers on edges of the patterned gate layer.” (Chen, 4:49-51; *see id.*, 3:65-66, 4:57-59, 6:11-13.) Chen’s sidewalls may be “made of a dielectric material, such as silicon dioxide, silicon nitride, or any combination of these, and the like.” (*Id.*, 4:49-53.) “Preferably, the final spacer structure comprises an ONO structure, as shown in FIG. 4A.” (*Id.*, 6:3-10.)

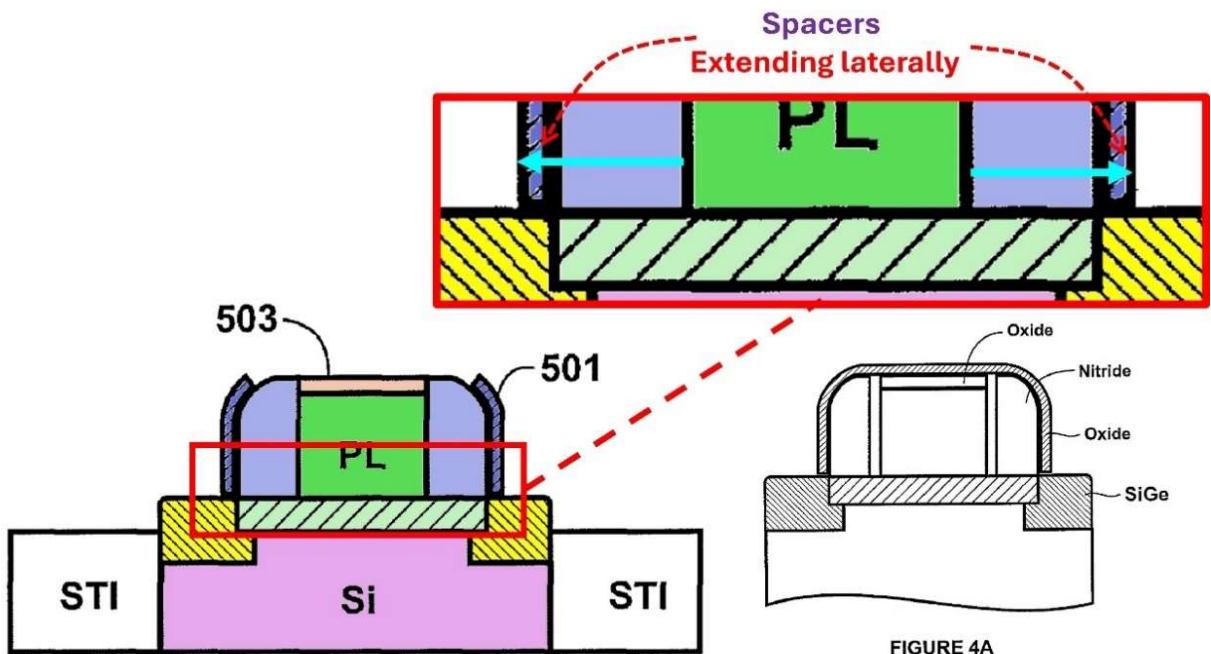
Chen’s “sidewall spacers 113” (the spacers directly contacting the gate structure) are formed “on edges of [the] patterned gate layer.” (*Id.*, 4:49-53; *see id.*, FIG. 1.) After etching recesses 201 and growing silicon germanium material 405, Chen further discloses “depositing a protective layer 409 overlying the entirety of

the patterned structure,” including silicon germanium material 405, as FIG. 4 confirms below. (*Id.*, 5:60-64.)



Chen, Fig. 4

“To finish the device according to an embodiment of [Chen’s] present invention, the method forms sidewall spacers 501” by etching protective layer 409 to “expose[] an upper portion 503 of the hard mask, while sealing regions on the edges of the gate layer” (*see* FIG. 5 below). (*Id.*, 6:11-15.)



Chen, FIG. 5 (annotated, magnified)

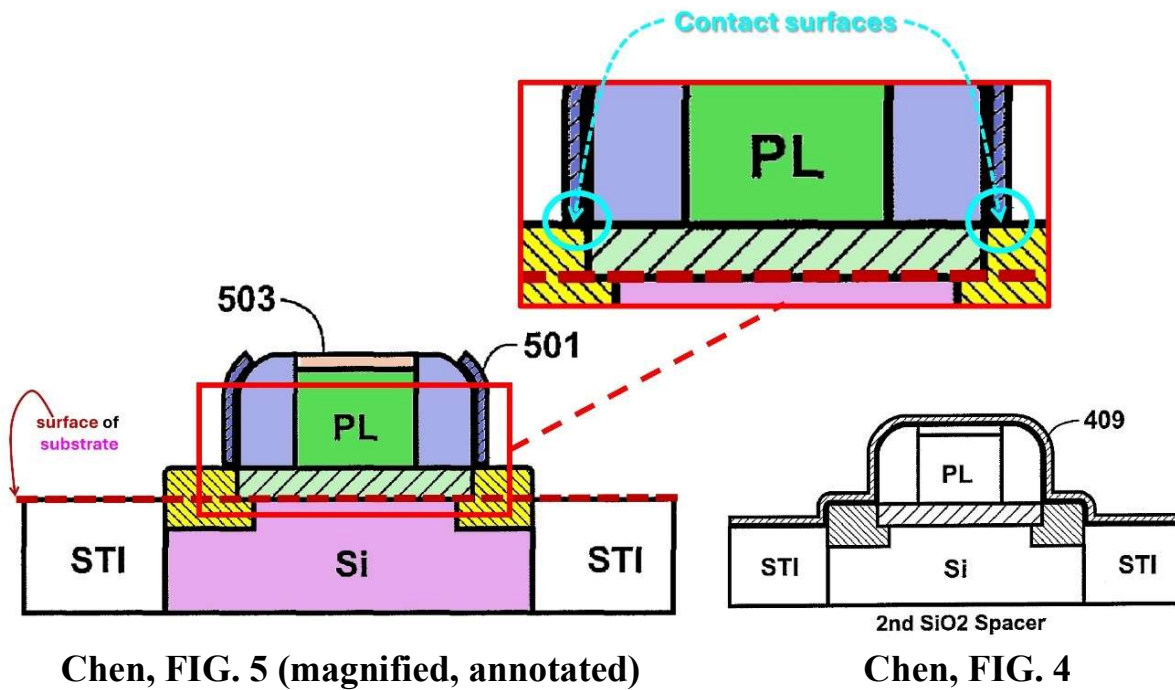
FIGURE 4A

Chen, Fig. 4A

Accordingly, as FIG. 5 illustrates, Chen discloses a spacer (Chen's sidewall spacers 501 together with Chen's sidewall spacers 113) formed on the sidewall of the gate (gate stack comprising the gate dielectric layer, gate layer, and the hard mask) and extending laterally upon a portion of the raised epitaxial layer (silicon germanium material 405). (Ex-1003 ¶¶293-297; *see Univ. of Cal.*, 2024 WL 4972639, at *3.)

e. [1d]

As explained for [1c], Chen's sidewall spacer structures extend laterally onto a portion of silicon germanium material 405. (*See* Chen, FIG. 5; *supra* §VI.E.1.d.) The portions of silicon germanium material 405 onto which Chen's sidewall spacer structures extend define contact surfaces. (*See id.*, FIGS. 4-5; Ex-1003 ¶299.) Moreover, as explained for [1b], a POSITA would have understood (Ground 4A), and at least found obvious (Ground 4B), that the upper surfaces of silicon germanium material 405 extend above the substrate surface. (*Supra* §VI.E.1.c; Ex-1003 ¶299.) Thus, as FIG. 5 confirms below, a POSITA would have understood (Ground 4A), and at least found obvious (Ground 4B), that the contact surface between Chen's silicon germanium material 405 and a bottom of Chen's sidewall spacer structures (e.g., bottom of sidewall spacer layer 501) lie above the surface of substrate 101. (Ex-1003 ¶299; Ex-1001, Figs. 5, 14; *see Univ. of Cal.*, 2024 WL 4972639, at *3.)

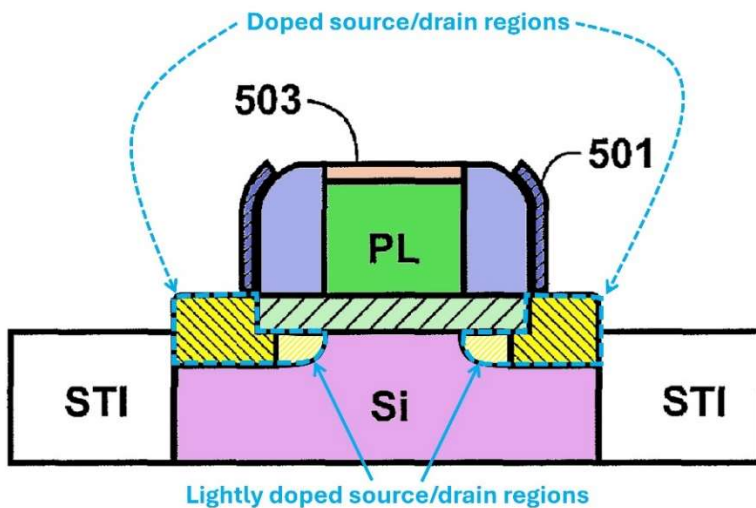


Chen’s spacers 501 are formed by depositing, then etching, “protective layer 409.” (Chen, 5:60-64, 6:11-15.) Protective layer 409 is deposited after, and on, silicon germanium material 405. (*Id.*, 5:60-62; *see id.*, FIG. 4.) After etching protective layer 409, the bottom of spacers 501 remains in direct contact with the upper surface of silicon germanium material 405. (*See id.*; Ex-1003 ¶300.)

As FIG. 5 confirms, Chen thus discloses (Ground 4A), and at least renders obvious (Ground 4B), a contact surface of the raised epitaxial layers (silicon germanium material 405) and a bottom of the spacer (e.g., bottom of constituent spacer layer 501) is above the surface of the semiconductor substrate (semiconductor substrate 101). (Ex-1003 ¶¶298-301.)

f. [1e]

Chen's silicon germanium material 405 is doped "using in-situ doping techniques" by introducing "impurities such as boron ... while the silicon germanium material grows." (Chen, 5:31-44.) Additionally, Chen discloses "form[ing] lightly doped drain regions ... on edges of patterned gate layer." (*Id.*, 4:57-5:8.) For the PMOS device, "the lightly doped drain region uses Boron or BF_2 " introduced by "[ion] implantation." (*Id.*, 4:59-63.) A POSITA thus would have understood (Ground 4A), and at least found obvious (Ground 4B), that Chen's lightly doped drain regions (not shown in Chen's images but added below) are formed in substrate 101. (*Supra* §II.C; Ex-1003 ¶¶304-305 (discussing Ex-1018 ¶¶[0021]-[0024], FIGS. 1, 4).)



Chen, FIG. 5 (annotated, LDD added)

Although part of Chen's lightly doped regions would be removed by the etch used to define silicon germanium epitaxy regions 201 (*see* Chen, 5:9-30, FIG. 2), a

POSITA would have understood (Ground 4A), and at least found obvious (Ground 4B), that the part of Chen's lightly doped layers nearest the channel must remain in substrate 101 adjacent to the channel region, else the lightly doped regions would be completely removed and serve no purpose. (Ex-1003 ¶306 (discussing Ex-1031, 5:52-64, 6:59-7:15, FIGS. 1A-1F; Ex-1032¶[0032], ¶[0039], ¶[0042], Figs. 1-5B; Ex-1033, 3:33-47, 4:31-5:3, 5:15-18, FIGS. 1-5; Ex-1034 ¶[0014], ¶¶[0017]-[0018], FIGS. 3-7; Ex-1018, ¶[0021], ¶¶[0023]-[0025], FIGS. 1-5; Ex-1035, ¶¶[0034]-[0038], ¶[0052], FIGS. 4-8); *see supra* §II.C.) Accordingly, Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), two doped regions (Chen's lightly doped regions) formed respectively in the semiconductor substrate (semiconductor substrate 101) next to the relative sides of the gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask). (Ex-1003 ¶¶302-307.)

Additionally, if a doped epitaxial region qualifies as a "doped region formed ... in the semiconductor substrate," then the claimed "two doped regions" may be mapped to any combination of Chen's lightly doped regions and/or silicon germanium material 405. (Ex-1003 ¶308.) Like Chen's lightly doped regions, Chen's silicon germanium material regions 405 are formed next to the relative sides of the gate, as FIG. 5 confirms. (Chen, 5:9-13, 5:32-36, FIG. 5; Ex-1003 ¶308.)

2. Dependent Claims

a. Claim 2

(1) [2pre]

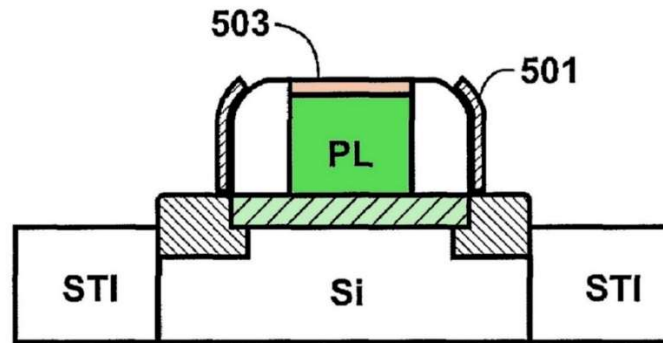
Chen discloses and renders obvious the structure of claim 1. (*Supra* §VI.E.1.)

(2) [2a]

Chen's gate stack includes "gate dielectric layer 107." (Chen, 4:30-35; *see id.* 3:45-46 ("Form a gate layer (e.g., polysilicon, metal) overlying the dielectric layer").) Chen describes dielectric layer 107 as "oxide or silicon oxynitride depending upon the embodiment." (*Id.*, 4:30-35.) Accordingly, the gate (Chen's gate stack, comprising at least gate dielectric layer 107 and gate layer PL) further comprises a dielectric layer (dielectric layer 107). (Ex-1003 ¶¶310-311.)

(3) [2b]

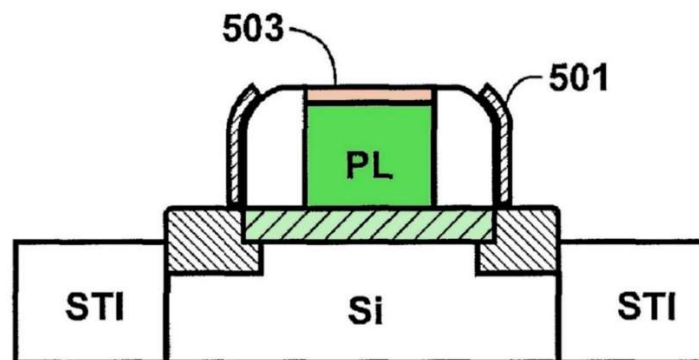
Chen discloses "[f]orm[ing] a gate layer [PL] ... overlying the dielectric layer." (Chen, 3:45-46; *see id.*, 2:10-11, 4:35-38, FIG. 5.) Chen's gate layer PL (dark green) thus overlies dielectric layer 107 (light green), as FIG. 5 confirms below. Moreover, Chen's gate layer PL is made of metal or doped polysilicon, both of which are conductive. (*Id.*, 3:45-46; *see* Ex-1024, 30 & Tbl. 12.1.) Accordingly, Chen's gate structure includes a conductive layer (gate layer PL), positioned on the dielectric layer (dielectric layer 107). (Ex-1003 ¶¶312-313.)



Chen, FIG. 5

(4) [2c]

Optionally, Chen’s gate stack further includes a “hard mask” (peach below) overlying the gate layer (PL, dark green) “to protect the underlying gate structure during etching and deposition steps.” (Chen, 4:43-59; *see id.*, 6:11-15; Ex-1003 ¶315.) This “hard mask layer can be made of any suitable material such as a dielectric material.” (*Id.*, 4:44-46; *see id.*, 3:49-51.)



Chen, FIG. 5

Despite the difference in nomenclature, Chen’s hard mask is a “cap layer” just like the ’847 Patent describes. (*See Adasa Inc. v. Avery Dennison Corp.*, 55 F.4th 900, 913 (Fed. Cir. 2022) (“[A] prior art inventor need not ‘conceive of its invention

using the same words as the patentee would later use to claim it.”); *compare* Ex-1001, 3:3-11, *with* Chen, 3:49-51, 4:43-53; *see* Ex-1003 ¶316.)

Chen discloses an embodiment that retains the cap layer:

To finish the device according to an embodiment of the present invention, the method forms sidewall spacers 501 from the second protective layer, *as illustrated by FIG. 5*. The sidewall spacers exposes an upper portion 503 of the hard mask, while sealing regions on the edges of the gate layer. *In a preferred embodiment*, the method removes the hard mask to expose 601 the top surface of the gate structures, *as shown in FIG. 6*.

(Chen, 6:11-18 (emphases added).) Chen thus makes clear that FIG. 5 represents a “finish[ed] ... device,” wherein the hard mask remains part of the gate structure. (*Id.*; *see* Ex-1003 ¶317.) Chen’s FIG. 6 is a different embodiment.

Accordingly, as Chen’s FIG. 5 “finish[ed] ... device” confirms, Chen expressly discloses (Ground 4A) that the gate (Chen’s gate stack, comprising at least gate dielectric layer 107 and gate layer PL) comprises a cap layer (Chen’s hard mask) positioned on the conductive layer (Chen’s gate layer PL). (Chen, 6:11-18; Ex-1003 ¶¶312-318.)

In addition to Chen expressly disclosing [2c] (Ground 4A, as described above), a POSITA also would have found it obvious, based on prior training

(Ground 4B), to retain Chen's cap layer (hard mask) in the final device structure. (Ex-1003 ¶¶319-326.)

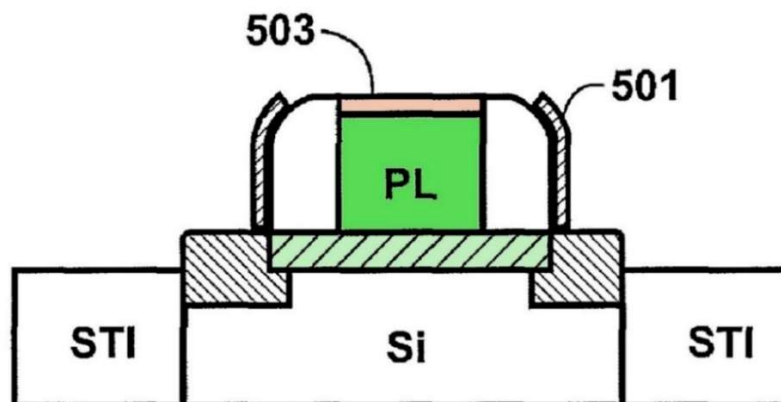
In one embodiment, Chen teaches to form silicide on the gate layer (PL) by "remov[ing] the hard mask to expose 601 the top surface of the gate structures." (Chen, 6:15-27 (discussing FIG. 6); *see supra* §VI.B.4.a.) But, as the passage quoted above makes clear, a POSITA would have understood this is only a preferred embodiment, not a requirement. (Chen, 6:11-18; Ex-1003 ¶320.)

Chen "is directed to integrated circuits." (Chen, 1:15-21.) A POSITA would have known that integrated circuits typically include "different types of transistors ... having different operating parameters and requirements." (*See, e.g.*, Ex-1036 ¶[0027]; Wang753, 1:51-56, 2:24-29; Ex-1003¶322.) A POSITA would have understood, for example, that it was desirable to avoid silicide formation in certain regions of an integrated circuit (e.g., where a higher impedance is desired). (*See* Ex-1036 ¶[0028]; Ex-1003 ¶¶322-323.) In device regions where silicide is unwanted on a polysilicon gate, for example, a POSITA would have found it obvious to retain Chen's hard mask because there is no need to remove it for silicidation. (*See* Chen, 6:11-27; Ex-1003 ¶¶323-324.)

Moreover, like Lan, Chen discloses embodiments in which its conductive gate layer (PL) is made of metal. (Chen, 3:45-46 ("Form a gate layer (e.g., polysilicon, metal) overlying the dielectric layer"); Ex-1003 ¶325.) For the same reasons a

POSITA would have found it obvious to retain Lan's cap layer, a POSITA also would have found it obvious to retain Chen's cap layer (hard mask). (*See supra* §VI.B.4.a; Ex-1003 ¶325.) As Section VI.B.4.a explains, a POSITA would have found it obvious that siliciding a metal conductive layer is unworkable and unnecessary because (1) a salicide process would not work on a metal gate; (2) there would be no need; and (3) if the cap layer were removed when forming silicide on source/drain regions, the metal gate layer may be removed, corroded, or otherwise damaged. (*Supra* §VI.B.4.a; Ex-1003 ¶325.) Thus, a POSITA would have understood that retaining the cap layer beneficially protects a metal gate layer when forming silicide on the source/drain regions. (*Supra* §VI.B.4.a; Ex-1003 ¶325.)

Viewing Chen, a POSITA therefore would have found it obvious that the gate (Chen's gate stack, comprising at least gate dielectric layer 107 and gate layer PL) further comprises a cap layer (Chen's hard mask) positioned on the conductive layer (Chen's gate layer PL), as FIG. 5 shows. (Ex-1003 ¶326.)



Chen, FIG. 5

b. Claim 7

Chen discloses and renders obvious the structure of claim 1. (*Supra* §VI.E.1.)

Co-Petitioners expect Patent Owner to argue claim 7 may be satisfied if one layer (an “offset spacer”) of the claimed “spacer” lies between another layer of the claimed “spacer” and the gate. (*See supra* §III.C.) Chen discloses such an embodiment.

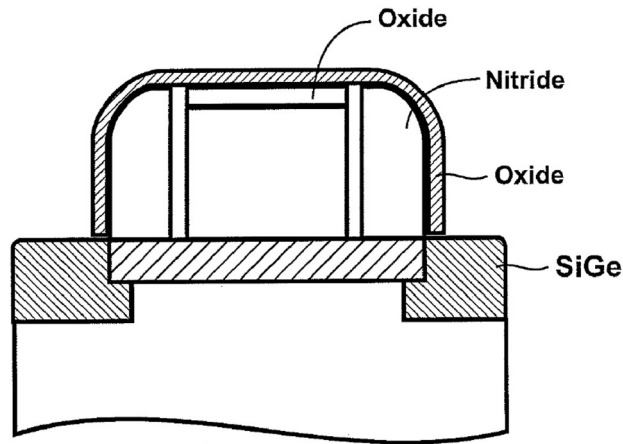
In Chen’s preferred embodiment, “the final spacer structure comprises an ONO structure, as shown in FIG. 4A.” (Chen, 6:3-10.) For example, “[t]he first oxide is about 200 Å, nitride 500 to 800 Å, second oxide 900 Å in the ONO, which is oxide on nitride on oxide structure.” (*Id.*, 6:4-6.)

Thus, Chen discloses an offset spacer (the “first oxide” in the ONO spacer) positioned between Chen’s gate stack and a portion of the spacer (e.g., the “nitride” and the “second oxide” of the ONO spacer). (Chen, 6:3-10; Ex-1003 ¶¶327-331.)

c. Claim 8

Chen discloses and renders obvious the structure of claim 1. (*Supra* §VI.E.1.) As the preceding subsection explains, Chen discloses that in a preferred embodiment “the final spacer structure comprises an ONO structure, as shown in FIG. 4A.” (Chen, 6:3-6.) In that embodiment, the “first oxide” layer of Chen’s ONO spacer is an oxide liner. (*See id.*, 6:3-6, FIGS. 4A, 5; Ex-1003 ¶333.) Additionally, Chen’s ONO spacer includes a “nitride” layer. (Chen, 6:3-6; Ex-1003 ¶333.) As FIG. 4A

confirms below, the “first oxide” of Chen’s ONO spacer lines the gate structure, and the “nitride” layer is sandwiched between the “first oxide” and the “second oxide.” (Chen, FIG. 4A; Ex-1003 ¶¶333.)



Chen, FIG. 4A

Accordingly, the spacer (Chen’s ONO spacer) comprises an oxide liner (the “first oxide” of the ONO spacer) and a nitride spacer (the “nitride” of the ONO spacer). (Ex-1003 ¶¶332-334.)

VII. TRIAL SHOULD BE INSTITUTED

The Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” sets out a temporary procedure under which Co-Petitioners will have an opportunity to respond to any discretionary denial arguments Patent Owner may raise through a bifurcated briefing process. Co-Petitioners believe discretionary denial is unwarranted and, at the appropriate time, plan to rebut any claims Patent Owner may advance to the contrary.

Meanwhile, Co-Petitioners identify below several non-limiting considerations that weigh against discretionary denial:

- The ITC instituted investigation on March 21, 2025, just 27 days before this Petition was filed. The ITC has not even set a schedule, let alone issued any substantive orders. (*See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 11 (Mar. 20, 2020) (expeditious filing weighs against denial); *SharkNinja v. iRobot Corp.*, IPR2021-00545, Paper 11, at 8 (Sept. 8, 2021) (petitioner's diligence and remaining work at the ITC weighs against denial).)
- This Petition challenges all claims of the '847 Patent, including claim 6, which has not been asserted in any parallel proceeding.
- No other forum has adjudicated these claims.
- Petitioner TSMC has a 94% institution rate on the merits and a 100% success rate in FWDs. Consistent with that track record, the merits here are strong, presenting grounds that map onto every claim limitation of the '847 Patent.
- Expert testimony is corroborated by documentary evidence.

- Each of Co-Petitioners (not to mention the other real parties-in-interest) is responsible for substantial and sustained investments and economic activity in the U.S.⁹
- The ITC lacks authority to invalidate the claims, but the companion district court cases, which will be stayed, triggered one-year bar dates for Co-Petitioners and the other real parties-in-interest, thereby limiting their options to invalidate the Challenged Claims. (*See 3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12, at 33-34 (May 26, 2020) (instituting despite parallel ITC case to preserve the “efficiency and integrity of the system”); *Emerson Electric Co., v. Sipco, LLC*, IPR2019-00547, Paper 15, at 9 (Aug. 30, 2019) (IPR proceedings not

⁹ “TSMC Intends to Expand Its Investment in the United States to US **\$165 Billion** to Power the Future of AI,” <https://pr.tsmc.com/english/news/3210> (Mar. 4, 2025); “Apple Will Spend More Than **\$500 billion** in the U.S. Over the Next Four Years,” <https://www.apple.com/newsroom/2025/02/apple-will-spend-more-than-500-billion-usd-in-the-us-over-the-next-four-years/> (Feb. 24, 2025); “Trump and TSMC Announce **\$100 Billion** Plan to Build Five New US Factories,” <https://www.reuters.com/technology/tsmc-ceo-meet-with-trump-tout-investment-plans-2025-03-03/> (Mar. 4, 2025).

duplicative of parallel ITC case).) The ITC may not even reach the issue of invalidity. (*See, e.g., Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).)

VIII. MANDATORY NOTICES

A. Real Parties-in-Interest

Co-Petitioners Taiwan Semiconductor Manufacturing Company Limited and Apple Inc., as well as Broadcom Inc. and Qualcomm Inc., are the real parties-in-interest.

B. Related Matters

First, the '847 Patent has been asserted in *Longitude Licensing Ltd. v. Lenovo Grp. Ltd. et al.*, Case No. 2:25-cv-00171-JRG (E.D. Tex.). In that proceeding, Patent Owner has alleged infringement by the following entities:

- Taiwan Semiconductor Manufacturing Company Ltd.
- Lenovo Group Ltd.
- Motorola Mobile Communication Technology Ltd.
- Motorola (Wuhan) Mobility Technologies Communication Co. Ltd.
- OnePlus Technology (Shenzhen) Co. Ltd.

Second, the '847 Patent has been asserted in *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 1:25-cv-00215-ADA (W.D. Tex.). In that proceeding, Patent Owner has alleged infringement by the following entities:

- Apple Inc.
- Broadcom Inc.
- Qualcomm Inc.

Third, the '847 Patent has been asserted in *Certain Foreign-Fabricated Semiconductor Devices, Products Containing the Same, and Components Thereof*, Inv. No. 337-TA-1443 (U.S.I.T.C.). In that proceeding, Patent Owner has alleged infringement by the following entities:

- Taiwan Semiconductor Manufacturing Company Ltd.
- Apple Inc.
- Broadcom Inc.
- Qualcomm Inc.
- Lenovo Group Ltd.
- Motorola Mobile Communication Technology Ltd.
- Motorola (Wuhan) Mobility Technologies Communication Co. Ltd.
- OnePlus Technology (Shenzhen) Co. Ltd.

Co-Petitioners are not aware of any other proceedings involving the '847 Patent.

C. Lead and Back-Up Counsel

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D. Service Information

Co-Petitioner TSMC consents to service by e-mail at the following addresses:

- jp.long@finnegan.com;
- aidan.skoyles@finnegan.com;
- carlos.duarte-guevara@finnegan.com;
- TSMC-MSL-IPR@finnegan.com.

Co-Petitioner Apple consents to electronic service by email at IPR50095-0267IP1@fr.com (referencing No. 50095-0267IP1 and cc'ing PTABInbound@fr.com, axf-ptab@fr.com, tar@fr.com, and ahn@fr.com).

IX. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 06-0916.

X. GROUNDS FOR STANDING

Co-Petitioners certify the '847 Patent is available for *inter partes* review and Co-Petitioners are not barred or estopped from requesting review on the grounds presented here.

XI. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft 365, this Petition contains 13,773 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, List of Challenged Claims, Mandatory Notices, and Certificate of Service.

XII. CONCLUSION

Trial should be instituted and the challenged claims cancelled.

Dated: April 17, 2025

Respectfully submitted,

/ J. Preston Long /

J. Preston Long, Ph.D., Reg.# 65,125
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Lead Counsel for Co-Petitioners

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Co-Petitioners' Powers of Attorney, and the associated Exhibits 1001-1036** were served via FedEx International delivery on April 17, 2025, on the correspondence address of record below indicated in the U.S. Patent Office's Patent Center for U.S. Patent No. 7,745,847.

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New Taipei City, - 234645
Taiwan

Courtesy copies have been concurrently served by FedEx Priority Overnight delivery on Patent Owner's litigation counsel at:

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Boston, MA 02111

Dated: April 17, 2025

By: / William Esper /
William Esper
Legal Assistant and PTAB Coordinator
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