

Combining Embedded and Overlayer Compressive Stressors in Advanced SOI CMOS Technologies

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Abstract

PMOS with embedded-SiGe and a compressive overlayer is demonstrated for the first time on partially-depleted SOI. SiGe is embedded into the SOI using a novel integration scheme highly compatible with SOI manufacturing. PMOS drive current improvement of 42% IDSAT and 100% IDLIN have been achieved. Product speed improvement of up to 29% has been demonstrated.

1. Introduction

Compressive overlayers [1] and embedded-SiGe [2,3] are being used in manufacturing to improve PMOS drive current. Both techniques improve hole mobility in the PMOS channel region through compressive stress. This is in the form of mechanical stress transfer from the compressive overlayer and a lattice-level stress transfer from the embedded-SiGe, due to the lattice mismatch between Si and SiGe. The latter is not well understood and has not been well predicted by continuum mechanical modeling. Thus, the interaction of the two stressors in generating the same compressive stress in the channel is of great interest. In this work, we describe an embedded-SiGe technology on partially-depleted SOI with greatly enhanced transistor properties and show the effect of combining this with a well-optimized overlayer stressor technology.

2. Compressive Stressor Process Integration on SOI

The main challenge of integrating embedded-SiGe into SOI is the limited silicon film thickness, which limits the depth of the embedded-SiGe. As an integration similar to [2,3] is not possible on thin-film SOI, we developed a novel integration scheme which embeds SiGe very close to the channel via a disposable spacer process. Our embedded-SiGe process sequence is shown in Fig. 1. Directly after gate and disposable spacer formation, a highly selective Si etch is used to form cavities in the PMOS active regions, leaving a seed-layer for selective SiGe-epitaxy. A hardmask protects the NMOS from both the cavity etch and SiGe-epitaxy.

Standard microprocessor fabrication follows, after hardmask and disposable spacer removal. A compressively-stressed overlayer is then added after silicide formation, and serves the dual purpose as a compressive stressor, and as a contact etch stop. A XTEM of a PMOS with embedded-SiGe (eSiGe) and compressive overlayer (COL) is shown in Fig. 2.

3. Improvement from Stress Combination

Drive current improvement from the combination of the two stressors is shown in Fig. 3. For the same compressive overlayer, both saturated and linear drive currents improve more when there is also embedded-SiGe. Equivalently in Fig. 3, drive current improvement from embedded-SiGe is higher if a compressive overlayer is used. This demonstrates that the two stressors enhance each other when combined, as evidenced by the drive current improvements being more than additive with each other.

However, measurement of short channel mobility based on [4] shows that mobility improvements from the two stressors are just additive. Without eSiGe, mobility increases by 60% when a compressive overlayer is added. With eSiGe, mobility increases by the same 60% when the compressive overlayer is added. Similarly, without COL, mobility increases by 70% when eSiGe is added. With COL, mobility increases by the same 70%. We conclude that the more-than-additive drive current improvements are due to the mobility improvements in combination with the well-known reduced sheet- and silicide-active contact resistance in SiGe.

From this basic understanding, we have optimized our source/drain implants in our multiple spacer scheme to take full advantage of eSiGe and COL. At 40nA IOFF, Fig. 4 (a) and (b) show 23% IDSAT and 56% IDLIN improvement with eSiGe, and 42% IDSAT and 100% IDLIN improvement with eSiGe and COL.

4. Impact on SOI Technology

The eSiGe has also been engineered to reduce SOI floating-body effects. Our integration allows the eSiGe to be placed in a position to increase forward diode current as shown in Fig. 5, due to the decreased bandgap of SiGe. This is beneficial for reducing floating-body effects in SOI. Fig. 6 (a) shows that DIBL due to the floating-body is reduced with eSiGe. The reduced floating-body voltages also improves transistor rolloff as shown in Fig. 6 (b).

For manufacturability, it is of great necessity to optimize the SiGe epitaxy process, SiGe position, and subsequent implants because the eSiGe is in compressive strain. Otherwise, defects in the SiGe can induce random leakage paths which are detrimental to the product. Properly optimized, product yield with SiGe is on the level of control, as shown in Fig. 7. Fig. 8 shows product speed improvement relative to a control without compressive stressors. The improvement is up to 17% with eSiGe, and up to 29% when eSiGe and COL are combined.

5. Conclusion

A novel embedded-SiGe process highly compatible with SOI manufacturing has been demonstrated. Combined with a compressive overlayer, up to 29% product speed improvement has been achieved. This combination has been integrated with our dual-stress overlayer technology [1] for further 90nm product family speed improvement. A second generation of this integration with over twice the SiGe improvement shown here is the basis of our 65nm technology.

References

- [1] H. Yang, et al., IEDM 2004, p. 1075
- [2] T. Ghani, et al., IEDM 2003, p. 978.
- [3] P. Bai, et al., IEDM 2004, p. 657
- [4] K. Rim et al., IEDM 2002, p. 43

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- Gate Formation
- Disposable Spacer
- Hardmask
- Cavity Etch
- SiGe-Epitaxy
- Dispose Hardmask
- Dispose Spacer
- Standard Processing

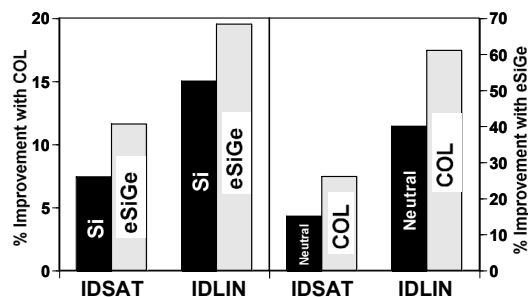
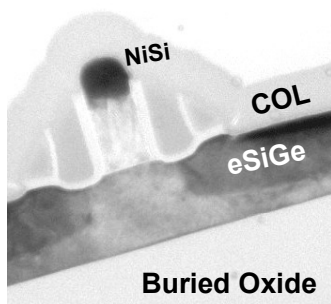


Fig. 1. Process sequence to insert SiGe into our 90nm and 65nm flows.

Fig. 2. XTEM of 90nm technology PMOS with eSiGe and COL on SOI.

Fig. 3. Relative drive current improvement when combining COL with eSiGe.

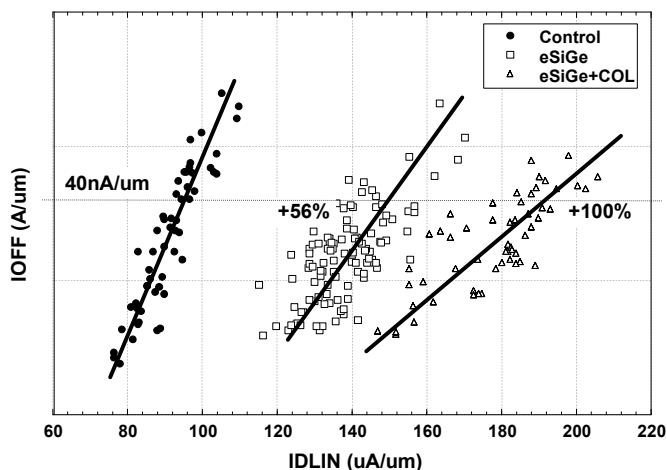
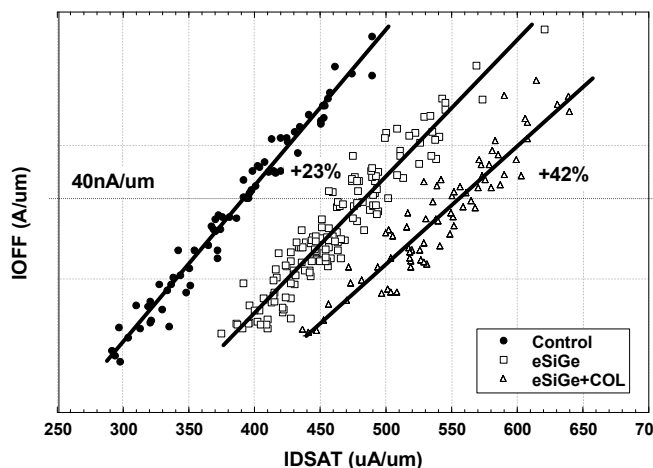


Fig. 4. (a) IOFF vs IDSAT at VDD=1.0V. (b) IOFF vs IDLIN (VGS=-1.0V VDS=-0.1V).

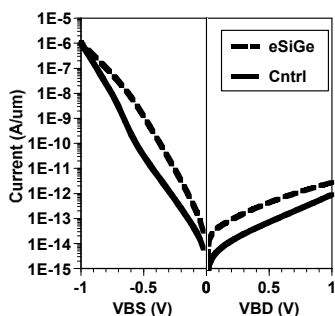


Fig. 5. Body-source/drain diode characteristics.

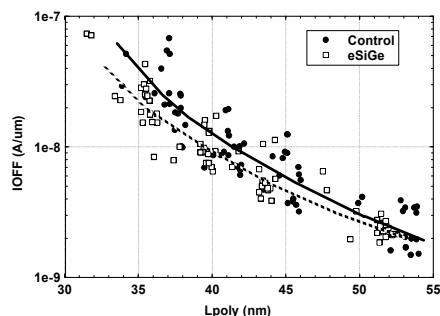
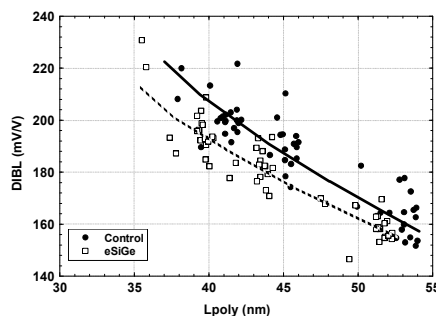


Fig. 6. (a) IOFF vs Lpoly rolloff and (b) DIBL vs Lpoly rolloff at Vdd=1.0V.

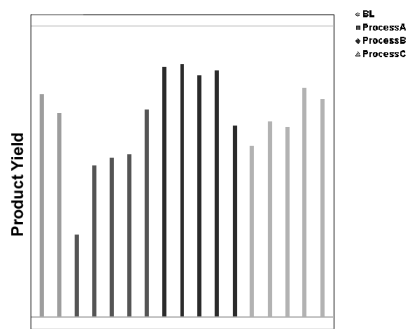


Fig. 7. Normalized microprocessor yield for 3 eSiGe processes versus control BL. Equivalent yield can be achieved.

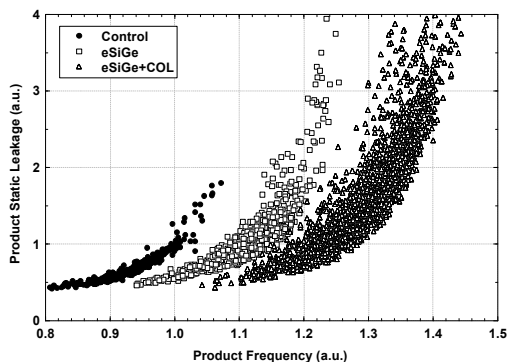


Fig. 8. Normalized microprocessor speed showing the improvement with eSiGe and eSiGe with compressive overlayer.