

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
and APPLE INC.
Petitioners,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-00847
U.S. Patent No. 7,745,847 B2

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Dr. Joseph McAlexander
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)

I. Introduction

The Petition should be denied because none of the grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teach or make obvious the “**raised** epitaxial layers” limitation found in every challenged claim. Indeed, because none of the asserted references mentions or describes a “raised epitaxial layer,” the Petition asks the Board to rely solely on not-to-scale patent drawings to find this missing limitation, an approach that the Federal Circuit has repeatedly held is wrong as a matter of law and is reversible error.

There are thus at least three independent reasons why each Petition ground fails to show the required “raised epitaxial layers”:

(1) The Petition alternatively relies on *Lan* (Grounds 1A, 1B, 1C, and 1D), *Wang407* (Grounds 2A and 2B), *Wang753* (Grounds 3A and 3B), and *Chen* (Grounds 4A and 4B) for the “raised epitaxial layer” limitation. But none of these references concern, discuss, describe, or even mention a “raised epitaxial layer.” Instead, the references merely describe conventional epitaxial layers and are completely silent regarding **raised** layers. Fatally, the Petition does not assert otherwise or even attempt to identify a single mention or description of “raised epitaxial layers” in any of these references.

(2) In light of this complete failure of the asserted references, Petitioners ignore the text and subject matter of the references and instead attempt to rely **solely** on their interpretations of select drawings from these references. According to Petitioners, they can discern “raised epitaxial layers” in these drawings, and this is sufficient to invalidate the challenged “raised epitaxial layer” claims, despite the references’ text and their accounts of those very same drawings never mentioning or describing any raised epitaxial layers. Petitioners are incorrect—their attempts to rely solely on interpretation of not-to-scale drawings without any textual support is contrary to the case law, including the single decision that they cite in attempt to support this disallowed approach. Indeed, the only decision Petitioners cite as supporting the Petition expressly **rejects** their argument:

[I]t is well established, however, that patent drawings do not define the precise proportions of elements and may not be relied on to show particular sizes if the specification is completely silent on the issue. In other words, figures in a patent are not drawn to scale unless otherwise indicated. **Arguments based on drawings not explicitly made to scale in issued patents are thus unavailing.**

Regents of Univ. of Cal. v. Satco Prods., Inc., 2024 WL 4972639, at *3 (Fed. Cir. Dec. 4, 2024) (reversing final written decision of obviousness due in part to “[t]he Board’s improper reliance on the figures).¹

The patent drawings asserted here are not explicitly made to scale and Petitioners’ arguments based on those drawings are “thus unavailing” as a matter of law. For this reason alone, the Petition fails.

(3) Petitioners’ interpretations of the drawings are not only insufficient as a matter of law, those interpretations are inconsistent with and not supported by the accompanying text and the drawings themselves, as explained below.

For any and all of these reasons, Patent Owner respectfully requests that the Board deny institution.

II. Semiconductor Transistor Technology Primer

The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (e.g., fin) transistors; and (3) common process steps for creating transistors. (EX2001, ¶5).

¹ Unless otherwise indicated, all emphasis in quotations is added.

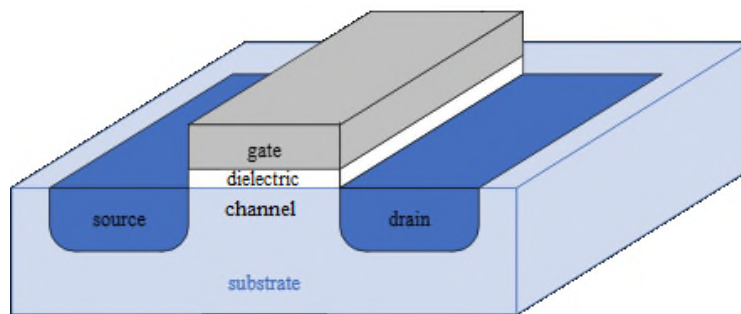
A. Basic Transistor Components

Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (i.e., turning electrical current on and off) and amplification (i.e., increasing the amplitude of a signal while retaining its electrical characteristics). (EX2002 at 1-2). Where earlier tube devices used a vacuum to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. (EX2002 at 3; EX2001, ¶6).

One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. The '847 patent describes different types of transistors and FETs, including a Metal Oxide Semiconductor ("MOS") FET. (*E.g.*, EX1001 at 1:12-24; EX2001, ¶7).

Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. (EX2002 at 29-34). In a conductor (e.g., a metal), electric current can flow freely. (EX2002 at 29). A dielectric (e.g., silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. (EX2002 at 30). Semiconductors (e.g., silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. (EX2002 at 31-34; EX2001, ¶7).

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. (See, *e.g.*, EX2002 at 510-511). The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.

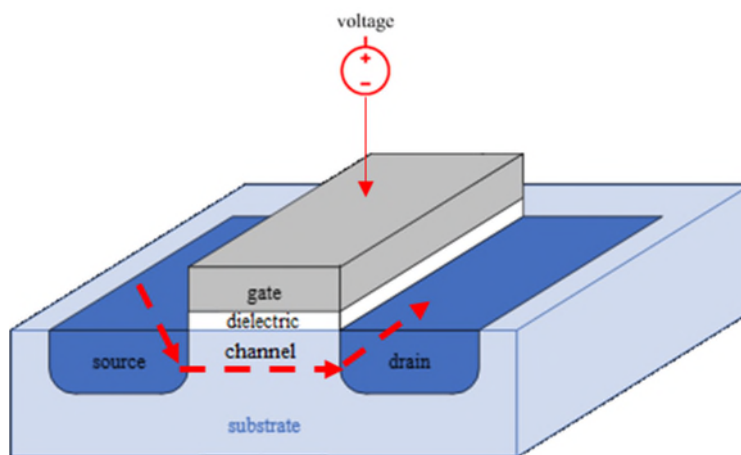


(See, *e.g.*, EX2002 at 510-511; EX2001, ¶8).

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). (EX2002 at 26-28, 427-28.) The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). (EX2002 at 510-511; EX2001, ¶9).

The gate is a conductor located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. (EX2002 at 510-511). When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation of a “field effect” in the channel. (EX2002 at 510-511). This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). (EX2002 at 510-511; EX2001, ¶10).

As illustrated below, this field effect allows electrical current to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping the flow of electrical current. (EX2001, ¶11).



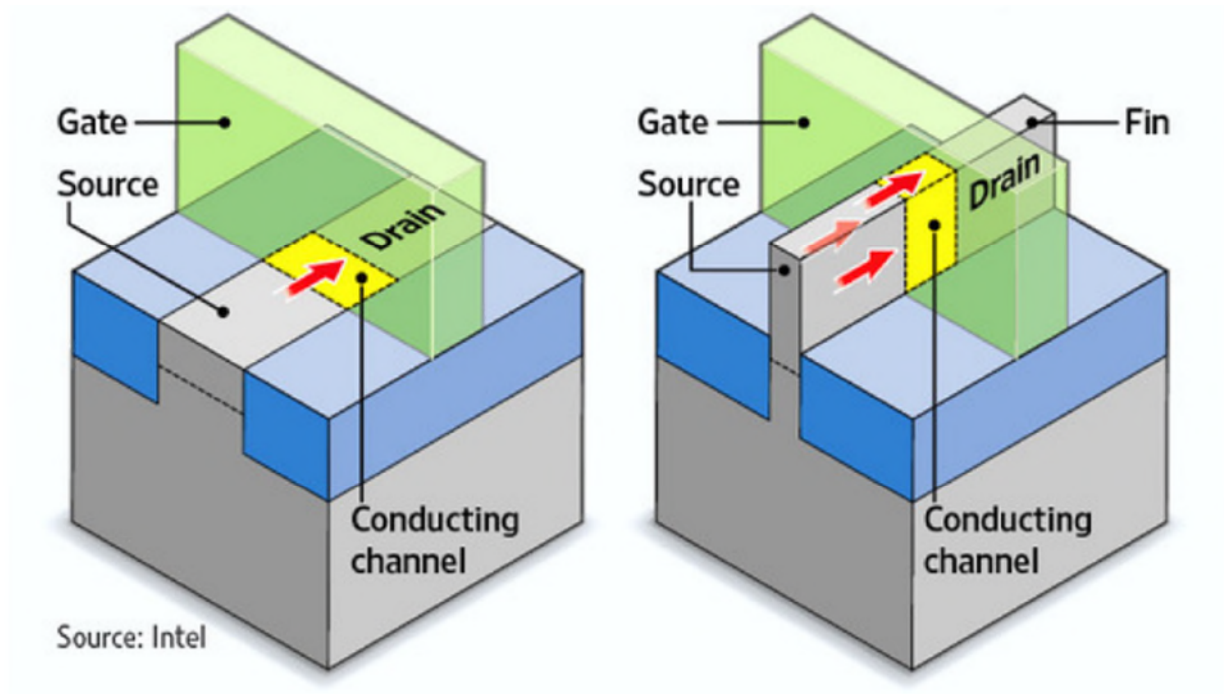
B. Planar vs. Three-Dimensional Transistors

Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947

were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more on a chip has been constant and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.” (EX2001, ¶12).

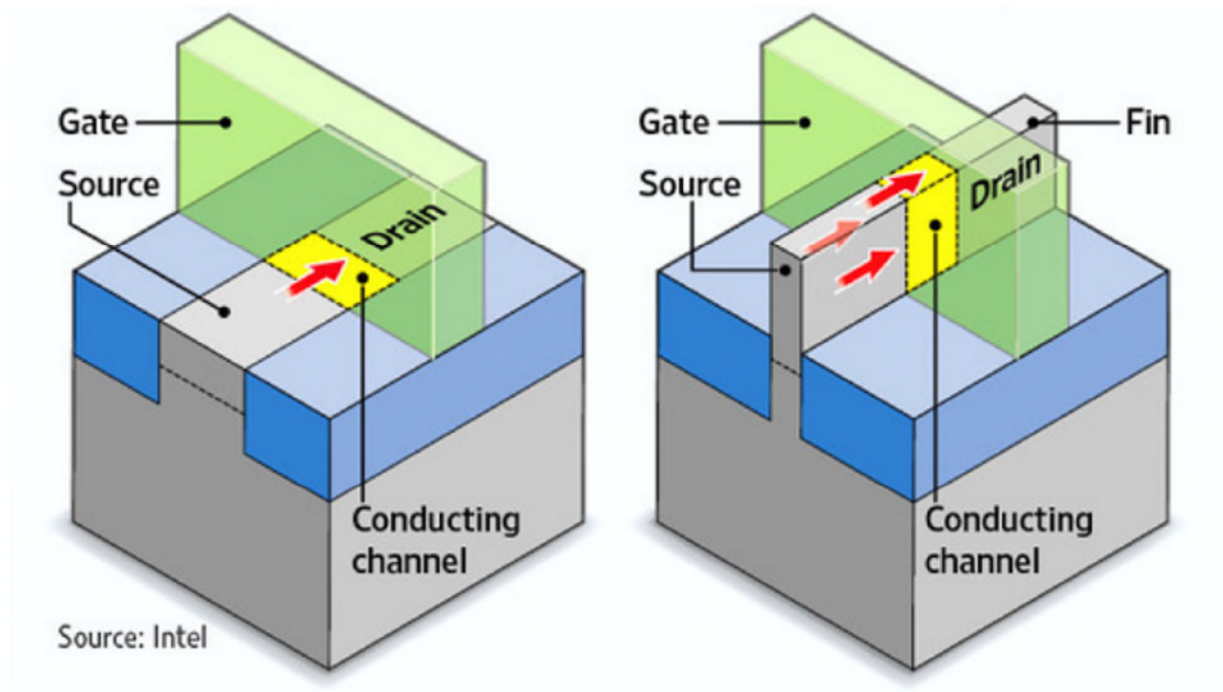
The simplified illustrative FET transistors illustrated in the previous section all feature a gate built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors. (EX2001, ¶13).

In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



(EX2001, ¶14).

In contrast, as illustrated below in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.



(EX2001, ¶15).

Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip. (EX2001, ¶16).

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. (EX2001, ¶17).

In the first stage, the semiconductor material itself is created. (EX2002 at 13). For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. (EX2002 at 13; EX2001, ¶18).

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” (EX2002 at 13-14). A wafer acts as a semiconductor substrate on and in which transistors may be formed. (EX2001, ¶19).

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. (EX2002 at 14). Thousands of integrated circuits can be formed on the substrate of a single wafer. (EX2002 at 14; EX2001, ¶20).

In the packaging stage, the wafer is separated into individual chips. (EX2002 at 14-15; EX2001, ¶21).

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in the wafer's substrate. (EX2002 at 14). These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). (See EX2002 at 29-31, 71). For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. (EX2001, ¶22).

Layering is the operation used to add thin layers to the semiconductor substrate. (EX2002 at 72). The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. (EX2002 at 72; EX2001, ¶23).

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's

semiconductor substrate, some deposited, some grown. (EX2002 at 72; EX2001, ¶24).

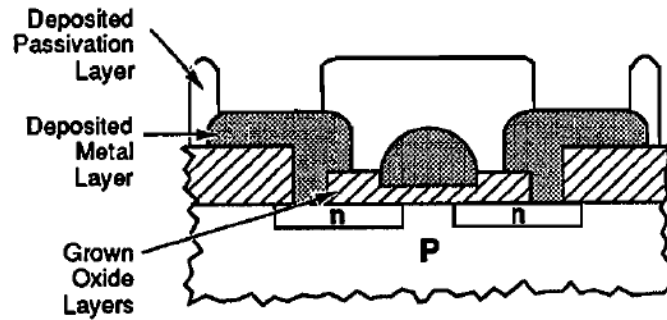


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. (EX2002 at 72-73). This creates a pattern on the wafer surface. (EX2002 at 72-73; EX2001, ¶25).

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. (EX2002 at 72-73; EX2001, ¶26). For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

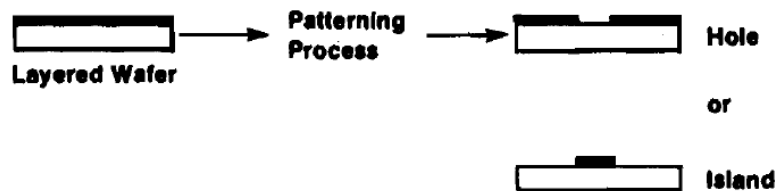


Figure 4.7 Patterning.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

(EX2002 at 73; EX2001, ¶27).

III. The Challenged '847 Patent

The '847 Patent describes and claims improved FET designs intended to improve the transistor's performance. The patent discloses a number of ways of improving performance, including combining “raised epitaxial layers” with various other transistor features. (EX2001, ¶37).

An “epitaxial layer” is a high-purity layer of semiconducting material. (EX2002 at 18, 380). As the patent describes, these layers may be formed within recesses in the semiconductor substrate and, in addition, “may be grown higher than the surface of the semiconductor substrate 200,” thereby making them “**raised** epitaxial layers.” (*E.g.*, EX1001 at 3:29-44; EX2001, ¶38).

A. The Inventive Transistor Structure Includes Raised Epitaxial Layers

The '847 Patent describes one illustrative inventive transistor structure as including:

“a gate formed on a semiconductor substrate;

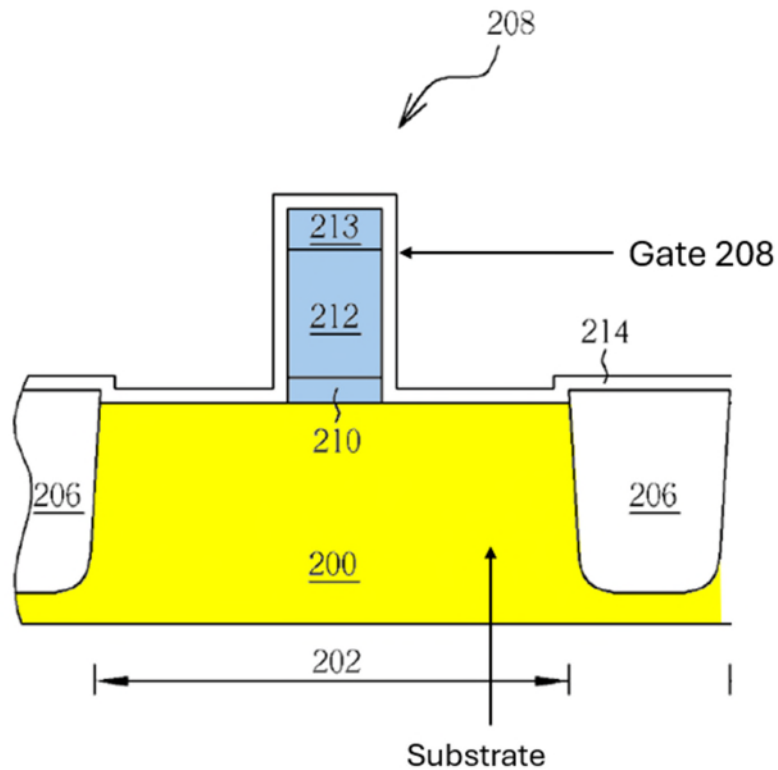
two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate;

a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer; and

two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.”

(EX1001 at 2:21-29; EX2001, ¶39).

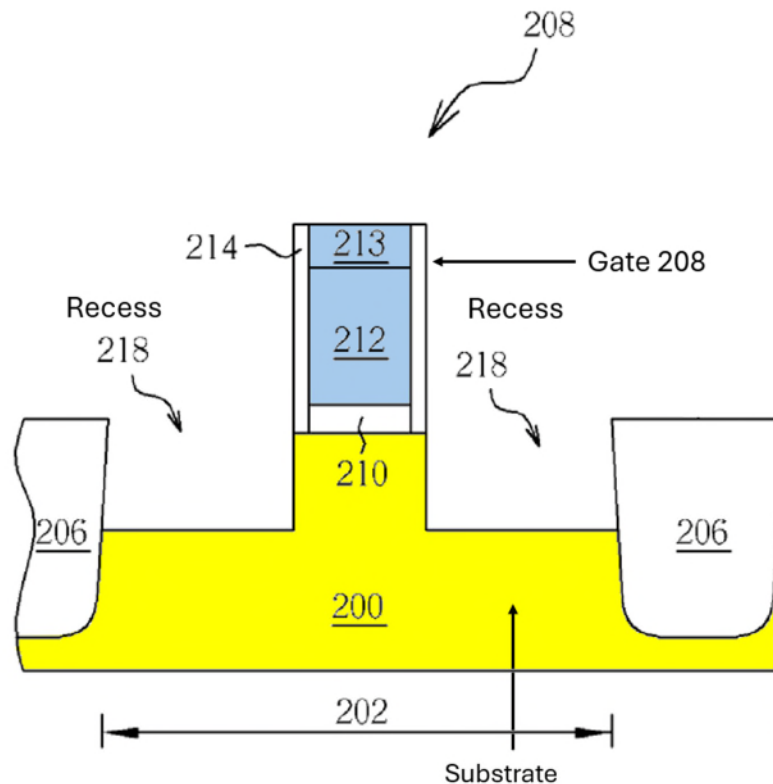
The '847 Patent further describes an exemplary method of fabricating such a transistor structure. For example, as illustrated below in an annotated portion of Figure 1, the method may start with a gate 208 (annotated in blue and comprising dielectric layer 210, conductive layer 212, and cap layer 213) positioned on substrate 200 (annotated in yellow):



(EX1001 at Fig. 1, 2:56-3:6²; EX2001, ¶40).

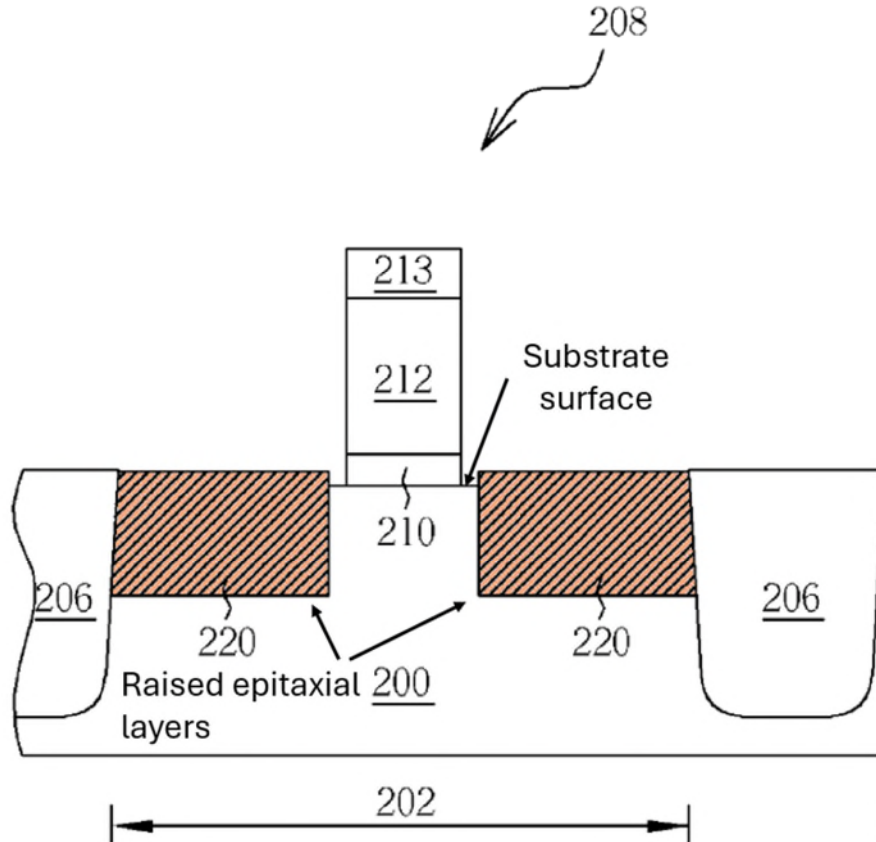
The substrate is then patterned to form recesses therein. For example, as shown below in an annotated portion of Figure 2, portions of the substrate may be selectively etched away to form recesses 218:

² Unless otherwise indicated, all colors and annotations to the challenged patent's figures are added.



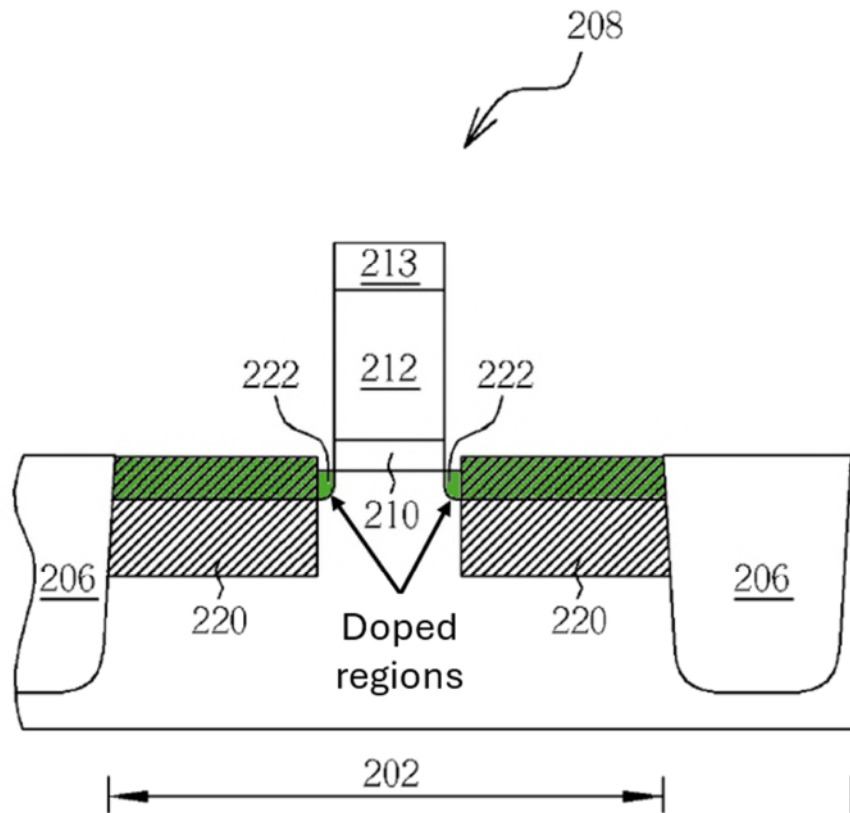
(EX1001 at Fig. 2, 3:23-28; EX2001, ¶41).

“Raised epitaxial layers” are then formed in these substrate recesses and next to sides of the gate. For example, “an epitaxial growth process is carried out to form epitaxial layers 220 in the recesses 218.” (EX1001 at 3:33-34). As the patent describes, these layers may be formed to a height higher than the surface of that substrate, thereby making them “raised epitaxial layers”: “epitaxial layer 220 is grown in the recess 218 and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.” (EX1001 at 3:35-38). The illustrative raised epitaxial layers are shown in orange in the following annotated excerpt from Figure 3:



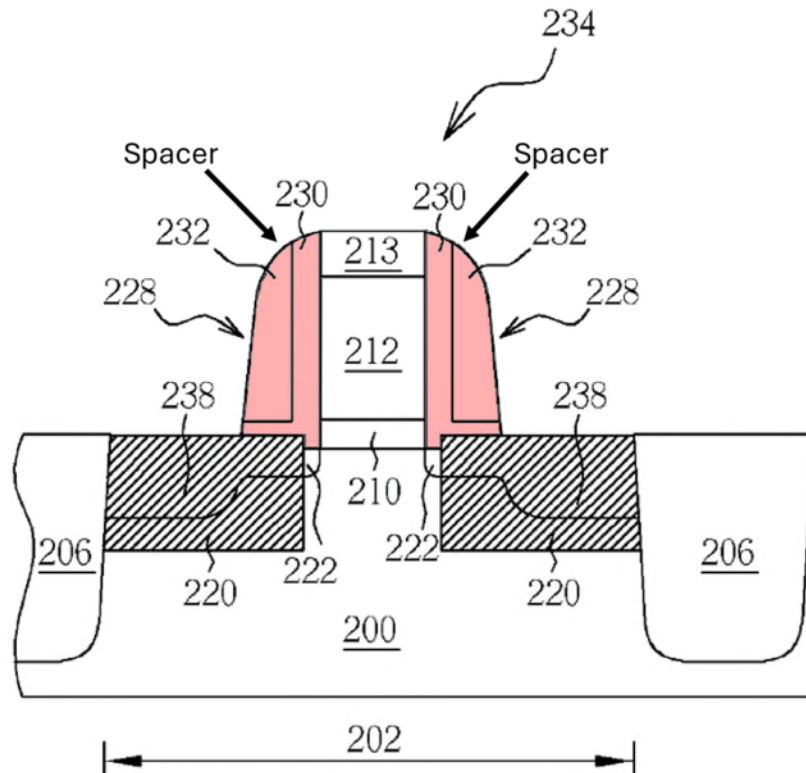
(EX1001 at Fig. 3, 3:35-38; EX2001, ¶42).

Selective doping is then performed to form doped regions 222 (annotated n green) in the substrate:



(EX1001 at Fig. 4, 3:45-48; EX2001, ¶43).

Spacer 228 (shown below in pink and comprising layers 230 and 232) is subsequently formed on the sidewalls of the gate:



(EX1001 at Fig. 5; EX2001, ¶44).

B. The Challenged '847 Patent Claims

The foregoing illustrative method results in an inventive transistor structure that includes “raised epitaxial layers” in combination with a gate on a substrate, a spacer, and two doped regions, which is reflected in each of the challenged claims. (EX2001, ¶45).

The Petition challenges all of the '847 Patent claims, namely independent claim 1 and dependent claims 2-11. Each of these claims includes the foregoing inventive concepts and combinations, including “raised epitaxial layers.” For example, exemplary claim 1 recites:

1. A MOS transistor structure, comprising:

a gate formed on a semiconductor substrate;

two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;

a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and

two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

(EX1001 at claim 1; EX2001, ¶46).

IV. PTAB Should Deny The Petition Because It Fails To Establish The Required Likelihood Of Success

The Petition asserts ten different grounds against various selections of claims:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A/1B	1, 3-9, 11	102/103	Lan
1C	2	103	Lan
1D	2	103	Lan, Liaw
2A/2B	1, 3-11	102/103	Wang407
3A/3B	1, 10	102/103	Wang753
4A/4B	1-2, 7-8	102/103	Chen

(EX2001, ¶47).

The Petition should be denied because, among other reasons, none of these grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teaches or makes obvious each limitation in any challenged claim. (EX2001, ¶48).

For example, for at least the following independent reasons (discussed in more detail in the following sections), each ground fails to identify a reference that teaches or makes obvious the “raised epitaxial layers” limitation found in every challenged claim:

(1) The Petition alternatively relies on *Lan* (Grounds 1A, 1B, 1C, and 1D), *Wang407* (Grounds 2A and 2B), *Wang753* (Grounds 3A and 3B), and *Chen* (Grounds 4A and 4B) for the “raised epitaxial layer” limitation. But none of these references concern, discuss, describe, or even mention a “raised epitaxial layer.” Instead, the references are completely silent regarding such raised layers, and the Petition does not assert otherwise or even attempt to identify a single mention of “raised epitaxial layers” in any of these references.

(2) In light of this complete failure of the asserted references, Petitioners ignore the text and subject matter of the references and instead attempt to rely solely on select drawings from these references. According to Petitioners, they can

discern “raised epitaxial layers” in these drawings, and this is sufficient to invalidate the challenged “raised epitaxial layer” claims, despite the references’ text and their account of those very same drawings never mentioning or describing any raised epitaxial layers. Petitioners are incorrect—their attempts to rely solely on interpretation of not-to-scale drawings without any textual support is contrary to the case law, including the single decision that they cite in attempt to support this disallowed approach.

Petitioners’ interpretations of the drawings are not only insufficient as a matter of law, those interpretations are inconsistent with and not supported by the accompanying text and the drawings themselves. (EX2001, ¶49).

A. The Asserted References Do Not Mention, Describe, Or Concern “Raised Epitaxial Layers”

The Petition alternatively relies on *Lan* (Grounds 1A, 1B, 1C, and 1D), *Wang407* (Grounds 2A and 2B), *Wang753* (Grounds 3A and 3B), and *Chen* (Grounds 4A and 4B) for the “raised epitaxial layer” limitation. But these references are completely silent regarding raised epitaxial layers, and the Petition does not assert otherwise or even attempt to identify a single mention or description of “raised epitaxial layers” in any of these references. (EX2001, ¶50).

1. *Lan* (Grounds 1A, 1B, 1C, and 1D)

For example, *Lan* does not concern, mention, advocate or describe “**raised** epitaxial layers.” Instead, *Lan* concerns a different topic, the order of certain process steps, teaching that source/drain extension areas regions should be formed “before forming epitaxial layers” so that “the high temperature of the [growing the epitaxial layer] doesn’t damage the source-drain extension areas.” (*E.g.*, EX1005 at 1:12-15, 1:41-46, 2:23-26; EX2001, ¶51).

But other than the order of formation, *Lan* does not describe or allege that its epitaxial layers have any particular features. For example, *Lan* does not describe its epitaxial layers as raised, nor does *Lan* describe them as grown so that they extend up and out of the substrate recesses and above the substrate surface. Instead, as opposed to the claimed “raised epitaxial layers,” *Lan* simply describes typical epitaxial layers that are grown **in** the recesses rather than grown out of and above those recesses:

An etching process is performed...so as to form recesses 202 in the substrate 102... . And then, a selective epitaxial growth (SEG) process is performed to form epitaxial layers **in** the recesses 202.

(*E.g.*, EX1005 at 2:59-64; EX2001, ¶52).

Lan’s description is in direct contrast to the challenged ’847 Patent, which describes that its epitaxial layers are “raised” because they are not merely grown

“in” the recesses, they are further grown “higher than the surface of the semiconductor substrate”: “epitaxial layer 220 is grown in the recess 218 **and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.**” (EX1001 at 3:35-38; EX2001, ¶53).

Indeed, the Petition does not dispute that *Lan* fails to describe the claimed “raised epitaxial layers.” Instead, the Petition merely asserts that “*Lan* discloses that “a SEG [selective epitaxial growth] process is performed to form epitaxial layers 1006, 1008 in the recesses 1002, 1004.”” (Petition at 20). The Petition does not assert—and could not reasonably assert—that this passage somehow describes “raised” epitaxial layers or otherwise describes that the *Lan* epitaxial layers were further grown out from and above the recesses. To the contrary, the Petition admits that this process merely “filled” the recesses. (Petition at 20; EX2001, ¶54).

2. ***Wang407* (Grounds 2A and 2B)**

Wang407 likewise does not concern, mention, advocate or describe “raised epitaxial layers.” Consistent with its title—“Composite Stressors With Variable Element Atomic Concentrations In MOS Devices”—*Wang407* instead describes that conventional SiGe stressors suffer leakage problems and proposes solving this problem by providing a composite SiGe stressor comprising two different portions: a lower portion having an atomic concentration, and a higher portion having a

different, larger atomic concentration. (*E.g.*, EX1007 at 1:52-59, 4:4-48; EX2001, ¶55).

At no point does *Wang407* additionally mention, describe, or advocate for raised epitaxial layers, nor does it describe this composite stressor as “raised” or otherwise formed so that it extends up and out of the substrate recesses and above the substrate surface. Instead, like *Lan*, *Wang407* simply describes that these stressors (SiGe regions 30 and 32) are grown “in recesses 26,” rather than grown out of and above those recesses, with regions 30 occupying “the bottom portions of the recesses 26” and regions 32 formed in situ on regions 30. (*E.g.*, EX1007 at 4:4-7, 4:34-40; EX2001, ¶56).

The Petition admits that *Wang407* describes that these regions “grow in recesses etched in the substrate,” and identifies no description of either region being further grown out of the recesses and above the substrate. (Petition at 48-49). Indeed, the Petition does not even attempt to identify any such description. (EX2001, ¶57).

3. ***Wang753* (Grounds 3A and 3B)**

Wang753 and *Wang407* share an inventor and the same relevant defects—like *Wang407* (and the other asserted references), *Wang753* does not concern, mention, advocate, or describe “raised epitaxial layers.” Instead, as its title suggests—“Write Margin Improvement For SRAM Cells With SiGe Stressors”—

Wang407 instead addresses how to incorporate conventional SiGe stressors into SRAM cells without those stressors degrading write operations. (*E.g.*, EX1008 at 1:62-2:14). *Wang407*'s proposed solution was to provide a "current-tuning region" along with the conventional SiGe stressors, locating at least part of the current-tuning region under a typical SiGe stressor conventionally formed in a substrate recess. (*E.g.*, EX1008 at 4:10-11, 4:14-22, 4:56-67; EX2001, ¶58).

At no point does *Wang753* additionally mention, describe, or advocate for raised epitaxial layers, nor does it describe its SiGe stressors as "raised" or otherwise formed so that it extends up and out of the substrate recesses and above the substrate surface. Instead, like *Lan* and *Wang407*, *Wang753* simply describes that its stressors 118 are "grown in [substrate] recesses 116," rather than grown out of and above those recesses. (*E.g.*, EX1008 at 4:10-11, 4:14-17; EX2001, ¶59) The Petition admits that *Wang753* describes that "[t]he SiGe stressors [are] epitaxially grown in the recesses 116," and identifies no description of the stressors being further grown out of the recesses and above the substrate. (Petition at 63-64). Indeed, as with each Ground's asserted references, the Petition does not even attempt to identify any such description. (EX2001, ¶60)

4. *Chen* (Grounds 4A and 4B)

Finally, like each of the foregoing references, *Chen* also does not concern, mention, advocate, or describe "raised epitaxial layers." Consistent with its title—

“Method And Structure For Second Spacer Formation For Strained Silicon MOS Transistors”—*Chen* instead seeks to improve transistor fabrication by forming a second spacer after the formation of conventional SiGe deposits in the substrate. (*E.g.*, EX1009 at 5:9-10, 5:31-38, 5:60-6:13, 7:14-18; EX2001, ¶61).

Once again, at no point does *Chen* additionally mention, describe, or advocate for raised epitaxial layers, nor does it describe its SiGe deposits as “raised” or otherwise formed so that they extend up and out of the substrate recesses and above the substrate surface. To the contrary, like the other asserted references, *Chen* simply describes that recesses (which *Chen* calls source and drain regions) are etched into the substrate and that SiGe material is then deposited into those regions “to fill” them:

[Step] 6. Etch a source region and a drain region adjacent to the gate structure using the dielectric layer as a protective layer;

[Step] 7. Deposit silicon germanium material **into** the source region and the drain region to fill the etched source region and the etched drain region.

(*E.g.*, EX1009 at 3:52-58, 5:9-10, 5:31-38). *Chen* does not describe that the silicon germanium material is then somehow further grown out of the recesses and above the substrate, and the Petition does not assert otherwise. (EX2001, ¶62).

B. Petitioners Cannot Rely On Patent Drawings Not Made To Scale To Cure The Asserted References' Failure To Disclose "Raised Epitaxial Layers"

In light of the asserted references' complete failure to describe or identify any raised epitaxial layers, the Petition resorts to interpreting select figures from the *Lan*, *Wang407*, *Wang753*, and *Chen* patents in an effort to find this missing limitation. (*E.g.*, Petition at 21, 48, 62-63, 71-72). But Petitioners' attempt to rely on non-scale drawings to save their Petition should be rejected as (1) wrong as a matter of law; and (2) inconsistent with and not supported by the accompanying text and the drawings themselves. (EX2001, ¶64).

1. Petitioners' Attempt To Rely On Non-Scale Drawings Is Wrong As A Matter Of Law

Petitioners' attempts to use patent drawings to provide claim limitations that are not described in the references are wrong as a matter of law, directly contrary to the Federal Circuit's repeated admonishment that it is reversible legal error to assess prior art and "not properly apply[] . . . our prior precedents that arguments [such as Petitioners'] based on drawings not explicitly made to scale are unavailing." *Nystrom v. Trex Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005).

None of the *Lan*, *Wang407*, *Wang753*, and *Chen* patents state that its drawings or any elements depicted therein are to scale, and the Petition does not assert otherwise. Nor would anyone expect these simplistic drawings to be to

scale, because a transistor in 2007 was roughly 45 nanometers (where a human hair diameter is 50,000-100,000 nanometers), with a single chip containing hundreds of millions of transistors. (EX2001, ¶65). For example, *Chen* refers to its drawings as “**simplified** cross-sectional view diagram of a method of fabricating.”

(EX1009, 4:15-16). No POSITA would understand “simplified” drawings to be drawn to scale or to represent the actual shapes and proportions of their elements.

And because the drawings and their elements are not explicitly to scale, Petitioners cannot, as they attempt to do here, properly rely on those drawings to establish and prove the “proportions,” “sizes,” or “quantitative relationship” of any elements in those drawings. *E.g., Hockerson-Halberstadt, Inc. v. Avia Group Intern.*, 222 F.3d 951, 956 (Fed. Cir. 2000). For example, in *Hockerson*, the Federal Circuit rejected as a matter of law an attempt to rely on patent drawings to establish the “quantitative relationship” between different elements in the drawings. *Id.* In doing so, the Federal Circuit stated, “it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Id.* But what the Federal Circuit forbids is exactly what Petitioners are attempting to do here.

And as the Federal Circuit has repeatedly made clear, this prohibition on relying on drawings in the manner Petitioners attempt here is well established. For example:

- “[A]rguments based on drawings not explicitly made to scale in issued patents are unavailing.” *Nystrom*, 424 F.3d at 1149.
- A POSITA “would be aware that figures in a patent are not drawn to scale unless otherwise indicated.” *Hockerson*, 222 F.3d at 956.
- “Absent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value.” *In re Wright*, 569 F.2d 1124 (C.C.P.A. 1977).
- Absent a written description, patent drawings may not be used to evidence the shape or proportions of an element “[b]ecause the figures in a drawing are not evidence of actual proportions when the drawings are not to scale.” *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1351 (Fed. Cir. 2013) (holding that the patent’s figures cannot be used to establish that an element of the figures has an elongated shape).

Petitioners provide no basis for their attempt to contravene this “well established” precedent. They cite—without any explanation or discussion—only a single non-precedential decision as supposedly supporting their attempt to rely on

patent drawings that are not scale. (Petition at 21, citing *Regents of Univ. of Cal. v. Satco Prods., Inc.*, 2024 WL 4972639 (Fed. Cir. Dec. 4, 2024)). Petitioners' failure to discuss or explain how this *Regents* decision supposedly supports this Petition is telling because in *Regents* the Federal Circuit (again) expressly **rejects** Petitioners' approach.

In *Regents*, the Federal Circuit found the Board committed legal error by relying on patent drawings to establish the relative size of elements because “nothing in the [reference] indicates that its figures are drawn to scale.” *Regents*, 2024 WL 4972639, at *8-12. The Federal Circuit again warned that, contrary to the Petitioners' grounds here, “it is well established, however, that patent drawings do not define the precise proportions of elements and may not be relied on to show particular sizes if the specification is completely silent on the issue. In other words, figures in a patent are not drawn to scale unless otherwise indicated.

Arguments based on drawings not explicitly made to scale in issued patents are thus unavailing.” *Regents*, 2024 WL 4972639, at *3.

The patent drawings relied on in the Petition are not explicitly made to scale and Petitioners' arguments based on those drawing are “thus unavailing.” For this reason alone, the Petition fails.

2. **Petitioners' Interpretations of the Drawings Are Unsupported**

Even if relying on non-scale drawings were not reversible legal error, the Petition would still fail because Petitioners' interpretations of the drawings are inconsistent with, and not supported by, the references and the drawings themselves, and thus cannot provide the required reasonable likelihood of success.

For example, although Petitioners argue that the non-scale drawings from *Lan*, *Wang407*, *Wang753*, and *Chen* establish that they included raised epitaxial layers, that interpretation is belied by each reference's explicit description of those alleged epitaxial layers. In each reference—and contrary to Petitioners' argument—the alleged epitaxial layer is explicitly described merely as being formed in the corresponding substrate recess, rather than grown out of and above that recess. For example:

- ***Lan***: “An etching process is performed...so as to form recesses 202 in the substrate 102... . And then, a selective epitaxial growth (SEG) process is performed to form epitaxial layers in the recesses 202.” (*E.g.*, EX1005 at 2:59-64).
- ***Wang407***: “[R]ecesses 26 are formed ...preferably by isotropically or anisotropically etching substrate 2 [and] SiGe stressors or regions

[are grown] **in** recesses 26.” (*E.g.*, EX1007 at 3:63-65, 4:4-7, 4:34-40).

- **Wang753**: “Recesses 116 and 316 are formed along the outside edges of the spacers [and] the SiGe stressors [are] epitaxially grown **in** [substrate] recesses 116.” (*E.g.*, EX1008 at 4:10-11, 4:14-17).
- **Chen**: “Deposit silicon germanium material **into** the source region and the drain region [recesses] **to fill** the etched source region and the etched drain region [recesses].” (*E.g.*, EX1009 at 3:52-58, 5:9-10, 5:31-38).

(EX2001, ¶65).

Thus, because Petitioners’ interpretations of the drawings find no support in, and are in fact inconsistent with, the references themselves, those interpretations could not provide the required reasonable likelihood of success, even absent the Federal Circuit’s clear directive that reliance on such non-scale drawings is wrong as a matter of law.

V. Conclusion

For at least the foregoing reasons, the Board should deny institution of the Petition.

Dated: August 15, 2025

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 5,463. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

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CERTIFICATE OF SERVICE

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