

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner.

Case No. IPR2025-00847
U.S. Patent No. 7,745,847 B2

PATENT OWNER'S RESPONSE

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2001	Declaration of Joseph McAlexander III
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	Second Declaration of Joseph McAlexander III
2004	Transcript of January 6, 2026, Deposition of Eugene Fitzgerald, Ph.D.
2005	Igor Polishchuk, <i>Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion</i> , IEEE ELECTRON DEVICE LETTERS, Vol. 22, No. 9, September 2001.
2006-2100	<i>Reserved</i>
2101	Procedural Schedule (Order No. 10) (May 7, 2025) from 337-TA-1443
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I. INTRODUCTION

None of Petitioner's presented grounds anticipates or renders obvious claims 1-11 of U.S. Patent No. 7,745,847 ("the '847 Patent). As explained below, and in more detail throughout this Patent Owner Response ("Response") and in the accompanying declaration of Joseph McAlexander (Ex. 2003), Petitioner's presented grounds fail for multiple reasons. First, as explained in Patent Owner's Preliminary Response (Paper 9) and below, none of the asserted references mention, describe, or concern "raised epitaxial layers," as required by all challenged claims. Instead, the Petition relies on interpretations of drawings in those references that are legally insufficient and inconsistent with and not supported by the accompanying text. Thus, all grounds fail to disclose or render obvious raised epitaxial layers.

Moreover, if the Board instead finds that the drawings are clear enough to be relied upon, those same drawings and the descriptions of them in the specification illustrate that other challenged claim limitations are not met by the references. For example, the Petition relies on the Chen reference (Ex. 1008) in Grounds 4A and 4B. However, Chen's drawings and text show that its epitaxial layers are not "positioned... next to the relative sides of the gate."

Finally, none of the asserted grounds disclose or render obvious dependent claim 2, wherein the gate includes additional layers including a cap layer. The only grounds that challenge claim 2 are Grounds 1C (Lan), 1D (Lan and Liaw) and 4A/4B

(Chen). As to Ground 1C, Petitioner concedes that the cap layer is removed in Lan and does not rely on it, in the only described embodiment that addresses the cap layer, but asserts that a POSITA would know in another embodiment, where the gate uses a metal conductive layer, he or she would not remove the cap layer. But Lan does not say that, and there are several reasons a POSITA *would* remove the cap layer in that embodiment, and so the Lan's silence on the issue, combined with its explicitly disclosure of affirmatively removing the cap, is insufficient to disclose the cap layer of claim 2. As to Ground 1D, there is no motivation to combine Lan and Liaw. Petitioner alleges Liaw has a cap layer whose sole use is to protect against misalignment of a source/drain plug contact. But Lan already contains a different measure to protect against misalignment of such a plug, and so does not benefit from Liaw, and a POSITA would not combine them. As to Ground 4A/4B, Chen explicitly says to remove the cap layer.

II. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER

The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors. Ex. 2003, ¶*.

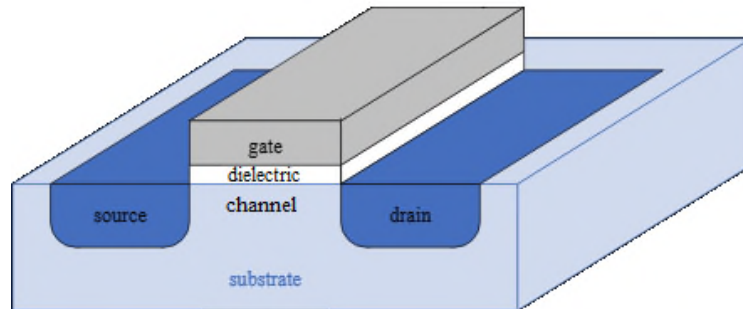
A. Basic Transistor Components

Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). Ex. 2002 at 1-2; Ex. 2003, ¶18. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. Ex. 2002 at 3; Ex. 2003, ¶18.

One type of transistor typically used in an integrated circuit (or “chip”) is a “field effect transistor,” or FET. Ex. 2003, ¶19. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. Ex. 2002 at 29-34; Ex. 2003, ¶19. In a conductor (*e.g.*, a metal), electric current can flow freely. Ex. 2002 at 29; Ex. 2003, ¶19. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. Ex. 2002 at 30; Ex. 2003, ¶19. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. Ex. 2002 at 31-34; Ex. 2003, ¶19.

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. Ex. 2003, ¶20. As shown, the transistor is

built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.*, Ex. 2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



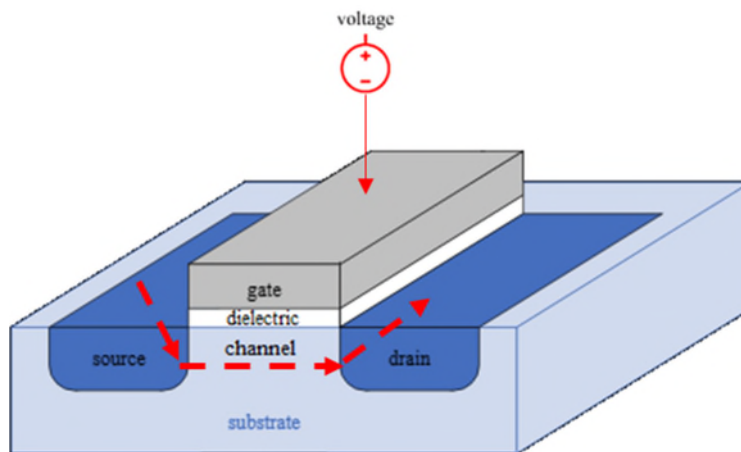
See, e.g., Ex. 2002 at 510-511; Ex. 2003, ¶20.

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). Ex. 2002 at 26-28, 427-28; Ex. 2003, ¶21. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). Ex. 2002 at 510-511; Ex. 2003, ¶21.

The gate is a conductor (or semiconductor) located above the channel. Ex. 2003, ¶22. In this simplified version of a FET, there is a dielectric between the channel and the gate. Ex. 2002 at 510-511; Ex. 2003, ¶22. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate

and the channel, but the applied voltage results in the creation of a “field effect” in the channel. Ex. 2002 at 510-511; Ex. 2003, ¶22. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). Ex. 2002 at 510-511; Ex. 2003, ¶22.

As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Ex. 2003, ¶23. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current. Ex. 2003, ¶23.



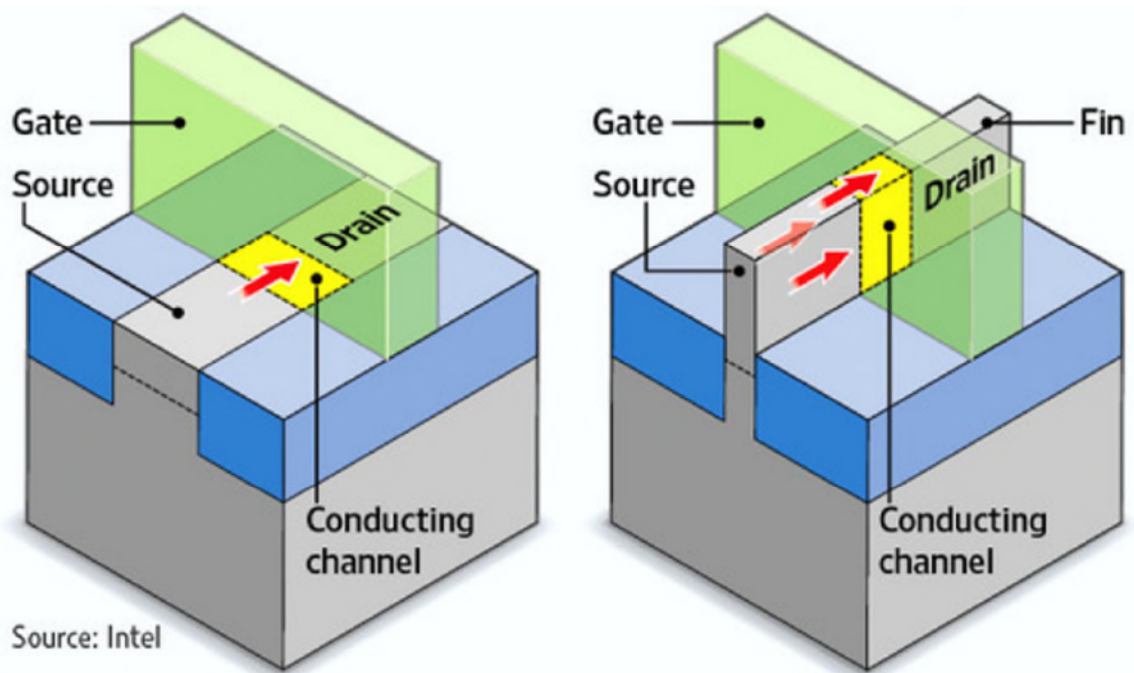
B. Planar vs. Three-Dimensional Transistors

Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. Ex. 2003, ¶24. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. *Id.* Given those numbers, and the correlation between an increased number of transistors and

increased computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. *Id.* This desire led to the development of a new type of transistor, a “FinFET.” Ex. 2003, ¶24.

The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a “planar” FET. Ex. 2003, ¶25. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors. Ex. 2003, ¶25.

In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. Ex. 2003, ¶26. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



Ex. 2003, ¶26.

In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. Ex. 2003, ¶27. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides. *Id.*

Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. Ex. 2003, ¶28. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. *Id.* In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. *Id.* This, too, increases the number of FinFET transistors that may fit onto a single chip. *Id.*

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct

stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. Ex. 2003, ¶29.

In the first stage, the semiconductor material itself is created. Ex. 2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. Ex. 2002 at 13; Ex. 2003, ¶30.

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” Ex. 2002 at 13-14; Ex. 2003, ¶31. A wafer acts as a semiconductor substrate on and in which transistors may be formed. Ex. 2003, ¶31.

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. Ex. 2002 at 14; Ex. 2003, ¶32. Thousands of integrated circuits can be formed on the substrate of a single wafer. Ex. 2002 at 14; Ex. 2003, ¶32.

In the packaging stage, the wafer is separated into individual chips. Ex. 2002 at 14-15; Ex. 2003, ¶33.

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer’s substrate. Ex. 2002 at 14; Ex. 2003, ¶34. These steps are generally performed using three categories of materials (conductors,

semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* Ex. 2002 at 29-31, 71; Ex. 2003, ¶34. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. Ex. 2003, ¶34.

Layering is the operation used to add thin layers to the semiconductor substrate. Ex. 2002 at 72; Ex. 2003, ¶35. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. Ex. 2002 at 72; Ex. 2003, ¶35.

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Ex. 2003, ¶36. Another way of adding a layer of material is to grow the material on the semiconductor substrate. *Id.* After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. *Id.* To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. Ex. 2002 at 72; Ex. 2003, ¶36.

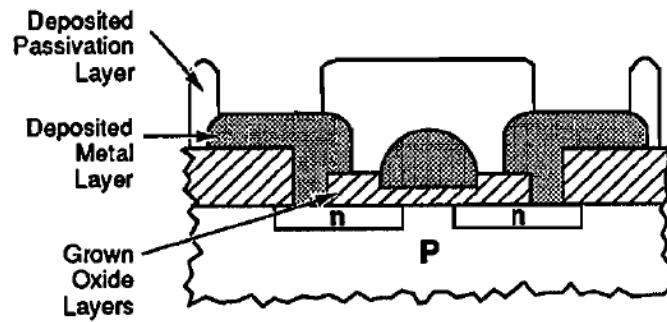


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. Ex. 2002 at 72-73; Ex. 2003, ¶37. This creates a pattern on the wafer surface. Ex. 2002 at 72-73; Ex. 2003, ¶37.

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. Ex. 2002 at 72-73; Ex. 2003, ¶38. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

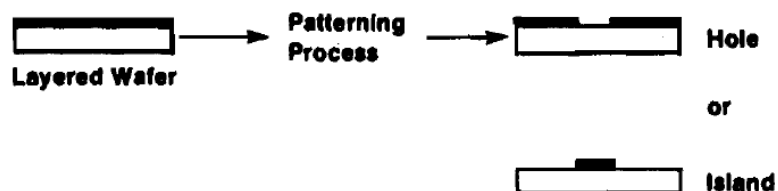


Figure 4.7 Patterning.

Ex. 2003, ¶38.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

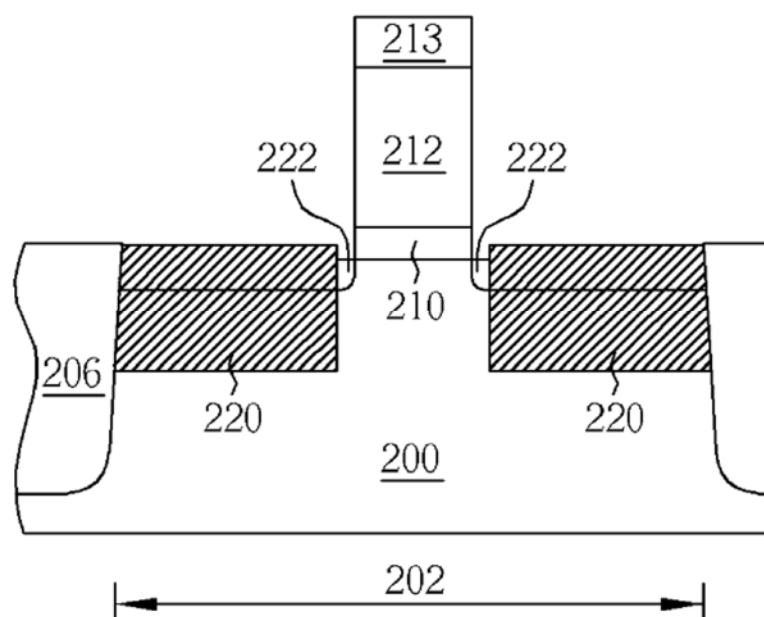
Ex. 2002 at 73; Ex. 2003, ¶39.

III. THE INVENTION OF THE '847 PATENT

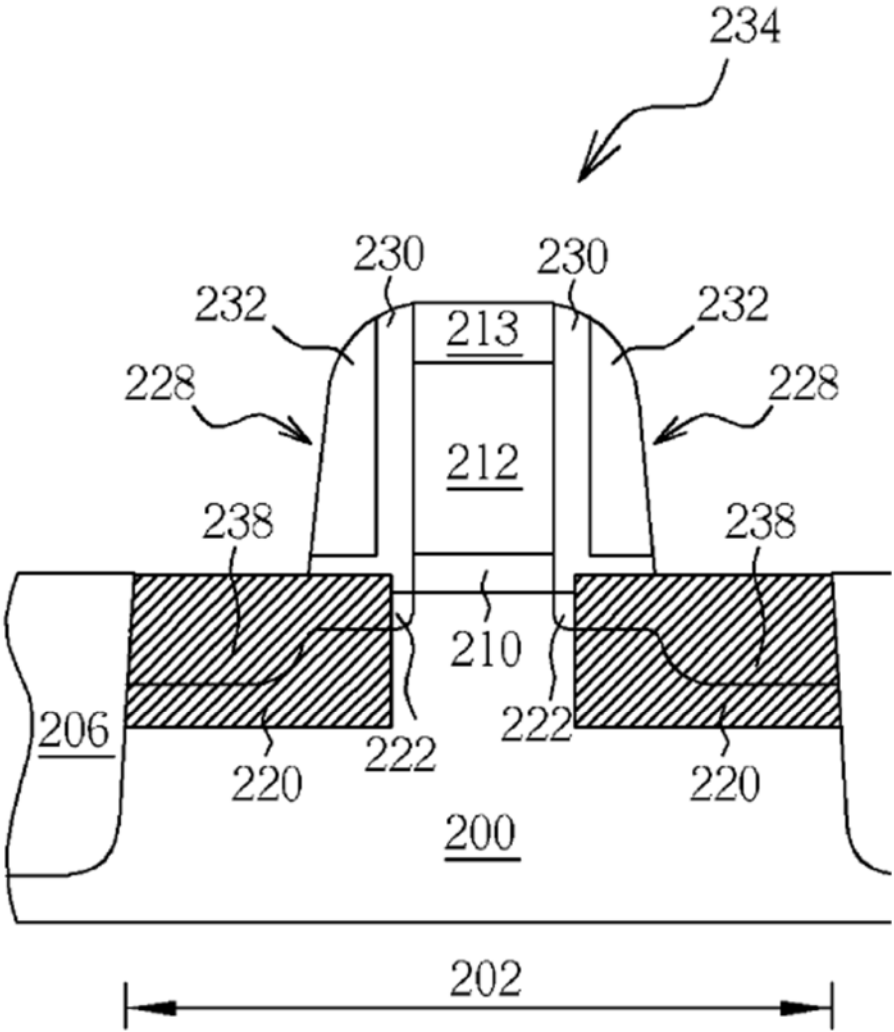
The '847 Patent describes and claims improved FET designs intended to improve the transistor's performance. For example, the patent discloses "a method of fabricating strained silicon channel MOPS transistors to improve the shortages from the prior art, and then increase the carrier mobility of MOS transistors." Ex. 1001, 1:49-52. One characteristic of the improved fabrication process "is to form the epitaxial layer before forming the spacer." *Id.*, 6:64-65. "[T]hus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer." *Id.*, 6:65-67. Moreover, "the process of etching the recess is carried out before forming the spacer. At this moment, the pattern density on the semiconductor substrate is lower than the time when the spacer is formed, thus the micro-loading

effect caused by the pattern density can be reduced, and then the uniformity in etching the recess is increased.” *Id.*, 6:67-7:6.

The claims of the '847 patent are directed to a MOS transistor structure fabricated using the described novel fabrication method. Because the recess and epitaxial layer are formed before the spacer is formed, the method results in a novel MOS transistor structure, which includes “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate” and “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.” This is illustrated in Figures 4 and 5 of the '847 patent. In Figure 4, the raised epitaxial layers 220, as well as the doped regions 222, are formed next to the sides of the gate structure before any spacers are formed:



Ex. 1001, Fig. 4 (partial). Subsequently, as shown in Figure 5, the spacers are formed on top of the raised epitaxial layers:



Ex. 1001, Fig. 5 (partial).

IV. THE PETITION GROUNDS FAIL TO DISCLOSE OR RENDER OBVIOUS LIMITATIONS OF INDEPENDENT CLAIM 1

A. All Petition Grounds Fail To Disclose Or Render Obvious “Two Raised Epitaxial Layers Positioned . . . Above The Surface Of The Semiconductor Substrate”

1. The Asserted References Do Not Mention, Describe, Or Concern “Raised Epitaxial Layers”

The Petition alternatively relies on Lan (Grounds 1A, 1B, 1C, and 1D), Wang407 (Grounds 2A and 2B), Wang753 (Grounds 3A and 3B), and Chen (Grounds 4A and 4B) for the “raised epitaxial layer” limitation. But these references are completely silent regarding raised epitaxial layers, and the Petition does not assert otherwise or even attempt to identify a single mention or description of “raised epitaxial layers” in any of these references. Ex. 2001, ¶50.

a. Lan (Grounds 1A, 1B, 1C, and 1D)

For example, Lan does not concern, mention, advocate or describe “**raised** epitaxial layers.” Instead, Lan concerns a different topic, the order of certain process steps, teaching that source/drain extension areas are made after the SEG (epitaxial) process so that “the high temperature of the SEG doesn’t damage the source-drain extension areas.” *E.g.*, Ex. 1005 at 1:12-15, 1:41-46, 2:23-26; Ex. 2001, ¶51.

But other than the order of formation relative to the source/drain extensions, Lan does not describe or allege that its epitaxial layers have any particular features. For example, Lan does not describe its epitaxial layers as raised, nor does Lan

describe them as grown so that they extend up and out of the substrate recesses and above the substrate surface. Instead, as opposed to the claimed “raised epitaxial layers,” Lan simply describes typical epitaxial layers that are grown in the recesses rather than grown out of and above those recesses:

An etching process is performed...so as to form recesses 202 in the substrate 102... . And then, a selective epitaxial growth (SEG) process is performed to form epitaxial layers in the recesses 202.

E.g., Ex. 1005 at 2:59-64; Ex. 2001, ¶52.

Lan’s description is in direct contrast to the challenged ’847 Patent, which describes that its epitaxial layers are “raised” because they are not merely grown “in” the recesses, they are further grown “higher than the surface of the semiconductor substrate”: “epitaxial layer 220 is grown in the recess 218 and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.” Ex. 1001 at 3:35-38; Ex. 2001, ¶53.

Indeed, the Petition does not dispute that Lan fails to describe the claimed “raised epitaxial layers.” Instead, the Petition merely asserts that “Lan discloses that “a SEG [selective epitaxial growth] process is performed to form epitaxial layers 1006, 1008 in the recesses 1002, 1004.”” Pet., 20. The Petition does not assert—and could not reasonably assert—that this passage somehow describes “raised” epitaxial layers or otherwise describes that that the Lan epitaxial layers were further

grown out from and above the recesses. To the contrary, the Petition admits that this process merely “filled” the recesses. Pet., 20; Ex. 2001, ¶54.

b. Wang407 (Grounds 2A and 2B)

Wang407 likewise does not concern, mention, advocate or describe “raised epitaxial layers.” Consistent with its title—“Composite Stressors With Variable Element Atomic Concentrations In MOS Devices”—Wang407 instead describes that conventional SiGe stressors suffer leakage problems and proposes solving this problem by providing a composite SiGe stressor comprising two different portions: a lower portion having an atomic concentration, and a higher portion having a different, larger atomic concentration. *E.g.*, Ex. 1007 at 1:52-59, 4:4-48; Ex. 2001, ¶55.

At no point does Wang407 additionally mention, describe, or advocate for raised epitaxial layers, nor does it describe this composite stressor as “raised” or otherwise formed so that it extends up and out of the substrate recesses and above the substrate surface. Instead, like Lan, Wang407 simply describes that these stressors (SiGe regions 30 and 32) are grown “in recesses 26,” rather than grown out of and above those recesses, with regions 30 occupying “the bottom portions of the recesses 26” and regions 32 formed in situ on regions 30. *E.g.*, Ex. 1007 at 4:4-7, 4:34-40; Ex. 2001, ¶56.

The Petition admits that Wang407 describes that these regions “grow in recesses etched in the substrate,” and identifies no description of either region being further grown out of the recesses and above the substrate. Pet., 48-49. Indeed, the Petition does not even attempt to identify any such description. Ex. 2001, ¶57.

c. Wang753 (Grounds 3A and 3B)

Wang753 and Wang407 share an inventor and the same relevant defects—like Wang407 (and the other asserted references), Wang753 does not concern, mention, advocate, or describe “raised epitaxial layers.” Instead, as its title suggests—“Write Margin Improvement For SRAM Cells With SiGe Stressors”—Wang407 instead addresses how to incorporate conventional SiGe stressors into SRAM cells without those stressors degrading write operations. *E.g.*, Ex. 1008 at 1:62-2:14. Wang407’s proposed solution was to provide a “current-tuning region” along with the conventional SiGe stressors, locating at least part of the current-tuning region under a typical SiGe stressor conventionally formed in a substrate recess. *E.g.*, Ex. 1008 at 4:10-11, 4:14-22, 4:56-67; Ex. 2001, ¶58.

At no point does Wang753 additionally mention, describe, or advocate for raised epitaxial layers, nor does it describe its SiGe stressors as “raised” or otherwise formed so that it extends up and out of the substrate recesses and above the substrate surface. Instead, like Lan and Wang407, Wang753 simply describes that its stressors

118 are “grown in [substrate] recesses 116,” rather than grown out of and above those recesses. *E.g.*, Ex. 1008 at 4:10-11, 4:14-17; Ex. 2001, ¶59.

The Petition admits that Wang⁷⁵³ describes that “[t]he SiGe stressors [are] epitaxially grown in the recesses 116,” and identifies no description of the stressors being further grown out of the recesses and above the substrate. (Petition at 63-64). Indeed, as with each Ground’s asserted references, the Petition does not even attempt to identify any such description. Ex. 2001, ¶60.

d. Chen (Grounds 4A and 4B)

Finally, like each of the foregoing references, Chen also does not concern, mention, advocate, or describe “raised epitaxial layers.” Consistent with its title—“Method And Structure For Second Spacer Formation For Strained Silicon MOS Transistors”—Chen instead seeks to improve transistor fabrication by forming a second spacer after the formation of conventional SiGe deposits in the substrate. *E.g.*, Ex. 1009 at 5:9-10, 5:31-38, 5:60-6:13, 7:14-18; Ex. 2001, ¶61.

Once again, at no point does Chen additionally mention, describe, or advocate for raised epitaxial layers, nor does it describe its SiGe deposits as “raised” or otherwise formed so that they extend up and out of the substrate recesses and above the substrate surface. To the contrary, like the other asserted references, Chen simply describes that recesses (which Chen calls source and drain regions) are etched

into the substrate and that SiGe material is then deposited into those regions “to fill” them:

[Step] 6. Etch a source region and a drain region adjacent to the gate structure using the dielectric layer as a protective layer;

[Step] 7. Deposit silicon germanium material **into** the source region and the drain region to fill the etched source region and the etched drain region.

E.g., Ex. 1009 at 3:52-58, 5:9-10, 5:31-38. *Chen* does not describe that the silicon germanium material is then somehow further grown out of the recesses and above the substrate, and the Petition does not assert otherwise. Ex. 2001, ¶62.

2. Petitioners Cannot Rely On Patent Drawings Not Made To Scale To Cure The Asserted References’ Failure To Disclose “Raised Epitaxial Layers”

In light of the asserted references’ complete failure to describe or identify any raised epitaxial layers, the Petition resorts to interpreting select figures from the Lan, Wang407, Wang753, and Chen patents in an effort to find this missing limitation. *E.g.*, Petition at 21, 48, 62-63, 71-72. But Petitioners’ attempt to rely on non-scale drawings to save their Petition should be rejected as (1) wrong as a matter of law; and (2) inconsistent with and not supported by the accompanying text and the drawings themselves. Ex. 2001, ¶64.

a. *Petitioners’ Attempt To Rely On Non-Scale Drawings Is Wrong As A Matter Of Law*

Petitioners’ attempts to use patent drawings to provide claim limitations that are not described in the references are wrong as a matter of law, directly contrary to the Federal Circuit’s repeated admonishment that it is reversible legal error to assess prior art and “not properly apply[] . . . our prior precedents that arguments [such as Petitioners’] based on drawings not explicitly made to scale are unavailing.” *Nystrom v. Trex Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005).

None of the Lan, Wang407, Wang753, and Chen references state that its drawings or any elements depicted therein are to scale, and the Petition does not assert otherwise. Nor would anyone expect these simplistic drawings to be to scale, because a transistor in 2007 was roughly 45 nanometers (where a human hair diameter is 50,000-100,000 nanometers), with a single chip containing hundreds of millions of transistors. Ex. 2001, ¶65. For example, *Chen* refers to its drawings as “simplified cross-sectional view diagram of a method of fabricating.” Ex. 1009, 4:15-16. No POSITA would understand “simplified” drawings to be drawn to scale or to represent the actual shapes and proportions of their elements.

And because the drawings and their elements are not explicitly to scale, Petitioners cannot, as they attempt to do here, properly rely on those drawings to establish and prove the “proportions,” “sizes,” or “quantitative relationship” of any

elements in those drawings. *E.g., Hockerson-Halberstadt, Inc. v. Avia Group Intern.*, 222 F.3d 951, 956 (Fed. Cir. 2000). For example, in *Hockerson*, the Federal Circuit rejected as a matter of law an attempt to rely on patent drawings to establish the “quantitative relationship” between different elements in the drawings. *Id.* In doing so, the Federal Circuit stated, “it is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue.” *Id.* But what the Federal Circuit forbids is exactly what Petitioners are attempting to do here.

And as the Federal Circuit has repeatedly made clear, this prohibition on relying on drawings in the manner Petitioners attempt here is well established. For example:

- “[A]rguments based on drawings not explicitly made to scale in issued patents are unavailing.” *Nystrom*, 424 F.3d at 1149.
- A POSITA “would be aware that figures in a patent are not drawn to scale unless otherwise indicated.” *Hockerson*, 222 F.3d at 956.
- “Absent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value.” *In re Wright*, 569 F.2d 1124 (C.C.P.A. 1977).
- Absent a written description, patent drawings may not be used to evidence the shape or proportions of an element “[b]ecause the figures

in a drawing are not evidence of actual proportions when the drawings are not to scale.” *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1351 (Fed. Cir. 2013) (holding that the patent’s figures cannot be used to establish that an element of the figures has an elongated shape).

Petitioners provide no basis for their attempt to contravene this “well established” precedent. They cite—without any explanation or discussion—only a single non-precedential decision as supposedly supporting their attempt to rely on patent drawings that are not scale. Pet., 21, citing *Regents of Univ. of Cal. v. Satco Prods., Inc.*, 2024 WL 4972639 (Fed. Cir. Dec. 4, 2024). Petitioners’ failure to discuss or explain how this *Regents* decision supposedly supports this Petition is telling because in *Regents* the Federal Circuit (again) expressly rejects Petitioners’ approach.

In *Regents*, the Federal Circuit found the Board committed legal error by relying on patent drawings to establish the relative size of elements because “nothing in the [reference] indicates that its figures are drawn to scale.” *Regents*, 2024 WL 4972639, at *8-12. The Federal Circuit again warned that, contrary to the Petitioners’ grounds here, “it is well established, however, that patent drawings do not define the precise proportions of elements and may not be relied on to show particular sizes if the specification is completely silent on the issue. In other words, figures in a patent are not drawn to scale unless otherwise indicated. Arguments

based on drawings not explicitly made to scale in issued patents are thus unavailing.”

Regents, 2024 WL 4972639, at *3.

The patent drawings relied on in the Petition are not explicitly made to scale and Petitioners’ arguments based on those drawing are “thus unavailing.” For this reason alone, the Petition fails.

b. Petitioners’ Interpretations Of The Drawings Are Unsupported

Even if relying on non-scale drawings were not reversible legal error, the Petition would still fail because Petitioners’ interpretations of the drawings are inconsistent with, and not supported by, the references and the drawings themselves.

For example, although Petitioners argue that the non-scale drawings from Lan, Wang407, Wang753, and Chen establish that they included raised epitaxial layers, that interpretation is belied by each reference’s explicit description of those alleged epitaxial layers. In each reference—and contrary to Petitioners’ argument—the alleged epitaxial layer is explicitly described merely as being formed in the corresponding substrate recess, rather than grown out of and above that recess. For example:

- ***Lan***: “An etching process is performed...so as to form recesses 202 in the substrate 102... . And then, a selective epitaxial growth (SEG)

process is performed to form epitaxial layers in the recesses 202.”

(*E.g.*, Ex. 1005 at 2:59-64).

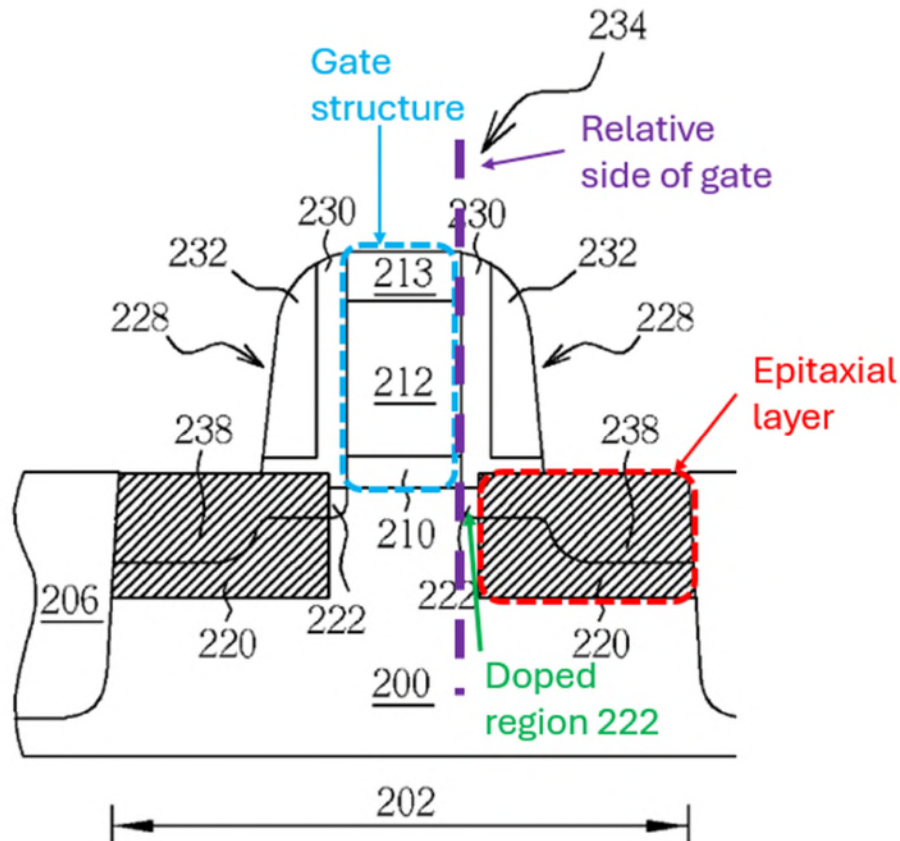
- **Wang407**: “[R]ecesses 26 are formed ...preferably by isotropically or anisotropically etching substrate 2 [and] SiGe stressors or regions [are grown] in recesses 26.” (*E.g.*, Ex. 1007 at 3:63-65, 4:4-7, 4:34-40).
- **Wang753**: “Recesses 116 and 316 are formed along the outside edges of the spacers [and] the SiGe stressors [are] epitaxially grown in [substrate] recesses 116.” (*E.g.*, Ex. 1008 at 4:10-11, 4:14-17).
- **Chen**: “Deposit silicon germanium material into the source region and the drain region [recesses] to fill the etched source region and the etched drain region [recesses].” (*E.g.*, Ex. 1009 at 3:52-58, 5:9-10, 5:31-38).

Ex. 2001, ¶65.

Thus, because Petitioners’ interpretations of the drawings find no support in, and are in fact inconsistent with, the references themselves, the Petition fails, even absent the Federal Circuit’s clear directive that reliance on such non-scale drawings is wrong as a matter of law.

**B. Petition Grounds 4A And 4B Fail To Disclose Or Render Obvious
“Two Raised Epitaxial Layers Positioned Respectively In The
Semiconductor Substrate Next To The Relative Sides Of The Gate”
And “Two Doped Region [sic] Formed Respectively In The
Semiconductor Substrate Next To The Relative Sides Of The Gate”**

Limitation [1.b] recites “two raised epitaxial layers positioned respective in the semiconductor substrate next to the relative sides of the gate.” Similarly, limitation [1.e] recites “two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.” As explained above in §III, the claimed MOS transistor structure is fabricated in a manner such that the raised epitaxial layer and doped regions are formed before a sidewall spacer. As a result, the raised epitaxial layer and doped region are positioned next to the relative side of the gate because their positions are not limited by the width of the spacer. Ex. 1001, 6:64-67; Ex. 2003, ¶43. This is illustrated in Figure 5 of the '847 patent, which shows that raised epitaxial layer 220 and doped region 222 are next to the relative side of the gate:



Ex. 1001, Fig. 5 (partial and annotated). “Each gate 208 comprises a dielectric layer 210, a conductive layer 212 positioned on the dielectric layer 210 and a cap layer 213 positioned on the conductive layer 212.” Ex. 1001, 3:3-6. As can be observed in the above Figure 5, the doped region 222 and raised epitaxial layer 220 are next to—as opposed to under—each of the layers that make up the gate stack, with some horizontal space in between the gate stack and the raised epitaxial layer. Ex. 2003, ¶44.

In contrast, Chen’s fabrication method forms a “gate dielectric layer 107” and “sidewall spacers 113” before etching recesses and forming epitaxial layers:

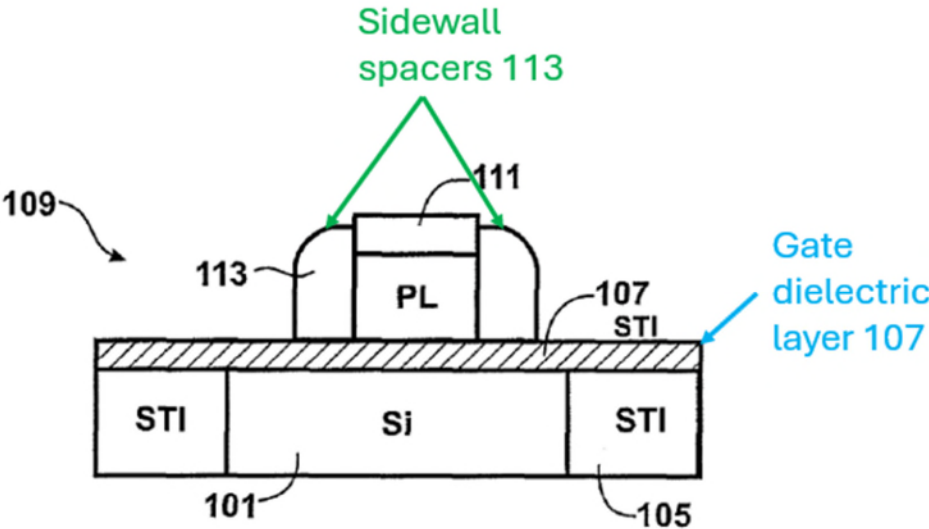


FIGURE 1

Ex. 1009, Fig. 1 (annotated), 4:30-59; Ex. 2003, ¶45. Then, as shown in Figure 2, the recesses are etched:

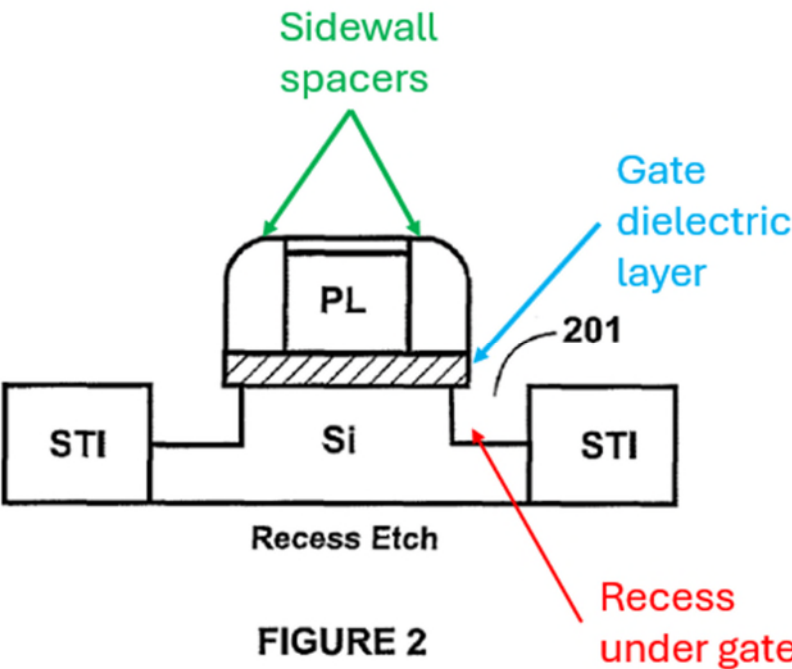


FIGURE 2

Ex. 1009, Fig. 2 (annotated); Ex. 2003, ¶46. As shown, because the gate dielectric layer extends to the edges of the sidewall spacers, the recesses are etched under the gate rather than next to the relative side of the gate. Ex. 2003, ¶47.

Finally, the epitaxial layer is formed in the etched recess:

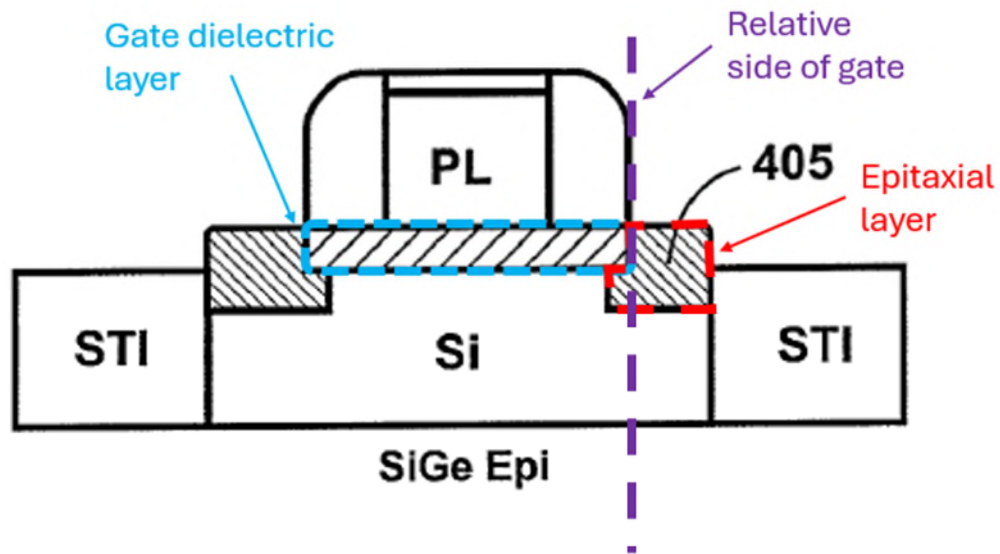
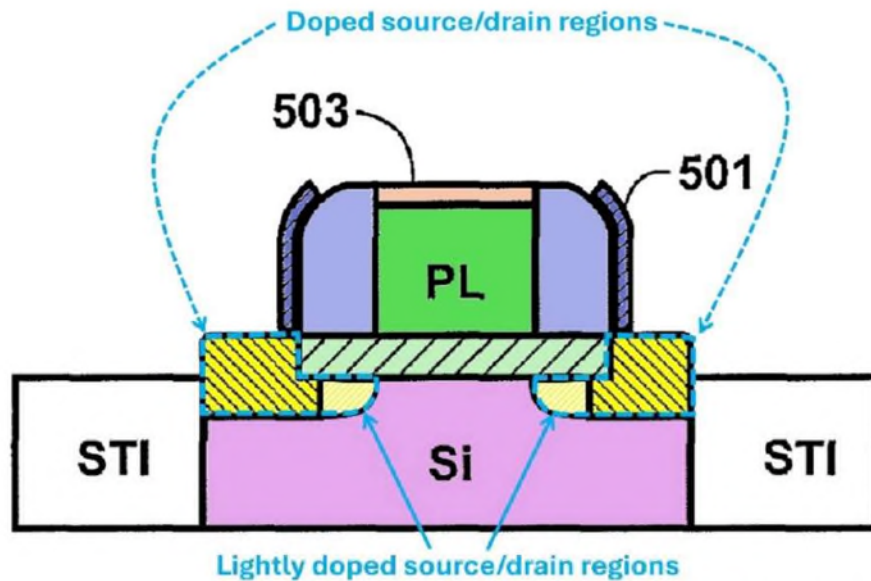


FIGURE 3

Ex. 1009, Fig. 3 (annotated); Ex. 2003, ¶48. As shown, the epitaxial layer is under the gate dielectric layer, rather than “next to the relative sides of the gate,” as required by limitation [1.b]. Ex. 2003, ¶49. Similarly, the Petition acknowledges that the doped regions would also be positioned under the gate dielectric layer:



Chen, FIG. 5 (annotated, LDD added)

Pet., 76 (annotated Ex. 1009, Fig. 5). This is significant because positioning the doped region and epitaxial layer under the gate (as disclosed in Chen) increases the risk of an electrical or physical short between the gate and the source/drain region. Ex. 2003, ¶51. The '847 patent's design avoids this potential problem by positioning the doped region and epitaxial layer "next to the relative sides of the gate," as recited in claim 1. Ex. 2003, ¶51.

The Petition acknowledges that Chen's gate dielectric layer extends to the edges of the sidewall spacers. Pet., 70 (annotating Ex. 1008, Fig. 5 to show gate dielectric layer 107 in light green). The Petition further acknowledges that the gate dielectric layer is part of the gate structure. Pet., 70 ("The gate dielectric layer, gate layer, and hard mask layer form 'a PMOS gate structure 109.'"). Nevertheless, the

Petition alleges, without explanation, that the epitaxial layers and doped regions are “next to the relative sides of the gate.” Pet., 72, 76-77. This unsupported allegation is incorrect, as the epitaxial layer is clearly shown to be under the gate in Figure 3. Ex. 2003, ¶52.

Thus, Lan does not disclose or render obvious limitations [1.b] and [1.e] and Grounds 4A and 4B fail.

V. THE PETITION GROUNDS FAIL TO DISCLOSE OR RENDER OBVIOUS LIMITATIONS OF CLAIM 2

The Petition alleges that Grounds 1C/1D and 4A/4B anticipate or render obvious dependent claim 2. First, these grounds fail for the same reasons as stated above with respect to independent claim 1. *Supra* §IV. Grounds 1C and 1D rely on Lan to disclose or render obvious “the structure of claim 1,” as required by claim 2. Pet., 33. Grounds 4A and 4B rely on Chen to disclose or render obvious “the structure of claim 1.” Pet., 78. But as explained above, neither Lan nor Chen discloses or renders obvious claim 1.

Moreover, Grounds 1C/1D and 4A/4B fail to disclose or render obvious that “the gate further comprises... a cap layer,” as required by limitation [2.c].

A. Ground 1C: Lan Does Not Disclose Or Render Obvious A Gate Cap Layer

The Petition alleges that “Lan’s gates 904 and 906 comprise ‘cap layers 912, 918.’” Pet., 35. However, as the Petition acknowledges, Lan’s cap layers must be

removed. Pet., 36 (citing Ex. 1005, 5:35-37). Thus, Lan does not disclose a gate cap layer. Ex. 2003, ¶56. Indeed, the Petition does not allege that Lan discloses a gate cap layer, as Ground 1C is an obviousness-only ground.

At the outset, the Petition appears to concede that the claims require a finished transistor structure, as opposed to an intermediate processing step in the creation of the structure. For example, the claims recite “A MOS transistor structure.” The Petition does not argue that Lan’s temporary intermediate structure discloses a gate cap layer. Pet., 36. Further, in Grounds 4A/4B, the Petition argues that Chen’s Fig. 5 discloses the gate cap layer in part because it is a “finish[ed]... device,” which is factually incorrect as explained below, but demonstrates Petitioner’s acknowledgement that the claims require a finished structure. Pet., 79-80.

Lan’s cap layer “serve[s] as [an] etching mask[], so as to form recesses 202 in the substrate 102 of the two side of the gate 104.” Ex. 1005, 2:59-62. Once the recesses are formed, the cap layer would serve no additional purpose and would be removed. Ex. 2003, ¶57. Indeed, the Petition admits that a POSITA would have understood that Lan’s cap layer would be removed. Pet., 36.

Despite admitting that Lan’s described fabrication process would require removing the gate cap layer, the Petition nevertheless alleges that a POSITA would have found it obvious to retain the cap layer if the conductive layer of the gate were made of metal. Pet., 39. The Petition argues that the cap layer would only be

removed in order to perform a salicide process, which is only beneficial if the gate conductive layer is polysilicon rather than metal. Pet., 37-38. Petitioner points to no disclosure of retaining the cap layer, but thus argues that because there is no reason to remove the cap layer when the gate is metal, a POSITA would know it would be retained. *Id.*

But Petitioner is incorrect that there is no reason to remove the cap layer when the gate is metal. First, the gate cap layer would need to be removed because the cap layer would block access to the gate conductive layer. Ex. 2003, ¶59. A voltage must be applied to the gate in order to allow charge to flow between the source and drain, *i.e.*, for the transistor to operate, and that in order to apply that voltage, the gate conductive layer must be contacted. Ex. 2003, ¶59; *supra* §II.A; Ex. 2004, 31:16-19. Thus, the Petition’s proposed modification of Lan—retaining the gate cap layer—is unworkable because it would create a further problem of blocking access to the gate conductive layer. Ex. 2003, ¶59. The Petition offers no solution for how this problem would be resolved.

Second, there are multiple reasons to remove the gate cap layer and to diffuse additional metal onto the gate even when the gate is metal, and these reasons are not limited to when the gate is made from polysilicon (a “silicide” or “salicide” process on the gate). Ex. 2003, ¶60. Diffusing an additional metal when the gate is metal (as when the gate is polysilicon) is beneficial for several reasons—and such a

diffusion, like a salicide, requires removal of the cap layer. *Id.* For example, in general, metal comprising the contact can be, and often is, a different metal from the gate metal, as Petitioner's expert agreed. Ex. 2003, ¶60; Ex. 2004, 31:20-22. A POSITA would have understood that a gate and contact would often be formed from different metals due to unique functional requirements for the respective components. Ex. 2003, ¶60. Moreover, the gate metal is typically deposited at a higher temperature than the contact metal, which further limits the selection of a specific metal material for the gate, as a metal with too low a melting temperature will melt and not be suitable, whereas the contact is deposited at a lower temperature, leading to a great set of options to choose from. Ex. 2003, ¶60.

However, interconnecting dissimilar metals leads to poor adhesion between the gate metal and the contact metal, as well as higher-than-desired contact resistance between the two. Ex. 2003, ¶61. For example, tungsten is often used as a contact metal because of its gap-fill characteristics, while titanium may be more suitable for a gate due to its work function, and could be used in Lan, as Lan does not restrict what metal is used for the gate. *Id.*; Ex. 2004, 29:4-21, 42:19-43:13. A POSITA would have known that it would be beneficial to diffuse an additional metal, such as nickel (which is a common diffusion metal in a salicide process) into a gate (for example, a titanium gate) before connecting the metal contact, for example a tungsten contact. Ex. 2003, ¶61; Ex. 2004, 25:21-26:16; *see* Ex. 2005,

446 (explaining benefits of interdiffusing titanium and nickel to fine-tune work function of a metal gate). This would benefit, for example, the tunability of the work function, which as Petitioner's expert agreed, impacts threshold voltage of a transistor, which is a key factor in transistor design, and thus a POSITA would know it is beneficial to be able to fine-tune the work function as desired for the given design. Ex. 2003, ¶61; Ex. 2004, 42:3-43:13. In addition, Petitioner's expert testified that in certain settings, the interface between the metal contact and the gate might not be as clean as one would like, and when asked if a POSITA would diffuse a metal into a gate in that scenario, he agreed "people might do things like that" in order to reduce contact resistance, which is a concern in transistor design. Ex. 2004, 34:24-35:24. Metal diffusion in to a metal gate would also improve adhesion, for example, if the same metal as the contact were diffused into the gate before the contact-gate junction is formed. Ex. 2003, ¶61. There is therefore agreement that there are reasons to remove the cap layer in the gate, rather than to keep the cap layer when the gate is metal. Further, Petitioner's expert admitted that a titanium nitride "liner" would "help with the connectivity" between a tungsten contact and another metal as the gate. Ex. 2004, 33:11-34:23.

The Petition argues that a POSITA would know that the cap layer on the gate is beneficial to retain (despite not being discussed as being retained in Lan) because "if cap layers 912 and 918 were removed when forming silicide on source/drain

regions 1206 and 1208, the metal gate layers 910 and 916 would be exposed to the etchant used to strip the unreacted silicidation metal, which could remove, corrode, or otherwise damage metal layers 910 and 916.” Pet., 37 (internal citations omitted). However, this argument makes no sense, because a POSITA would have understood that in selectively removing any unreacted silicidation metal, an etchant would be selected that would not attack the metal gate. Ex. 2003, ¶62. Thus, contrary to the Petition’s allegations, retaining the cap layer is not necessary to protect the metal layers of the gate during a salicide process performed on the source/drain. *Id.* Moreover, a POSITA would have understood that even if a small portion of the metal layer was removed by the etchant, this would not be an issue due to the large relative thickness of the gate as compared to the unreacted silicidation metal, which Petitioner’s expert agreed is how these types of devices are structured. *Id.*; *see also* Ex. 2004, 49:12-23 (Petitioner’s expert testifying that the gate is “much thicker” than the unreacted metal layer). Thus, the amount of etching necessary to remove the unreacted silicidation metal is very low relative to the large thickness of the gate metal, which would be functionally unaffected. Ex. 2003, ¶62. Thus, the Petition’s explanation does not provide a reasonable justification for retaining the cap layer. *Id.*

In short, the Petition admits that Lan’s fabrication method requires removing the gate cap layer and does not offer sufficient rationale for its proposed modification

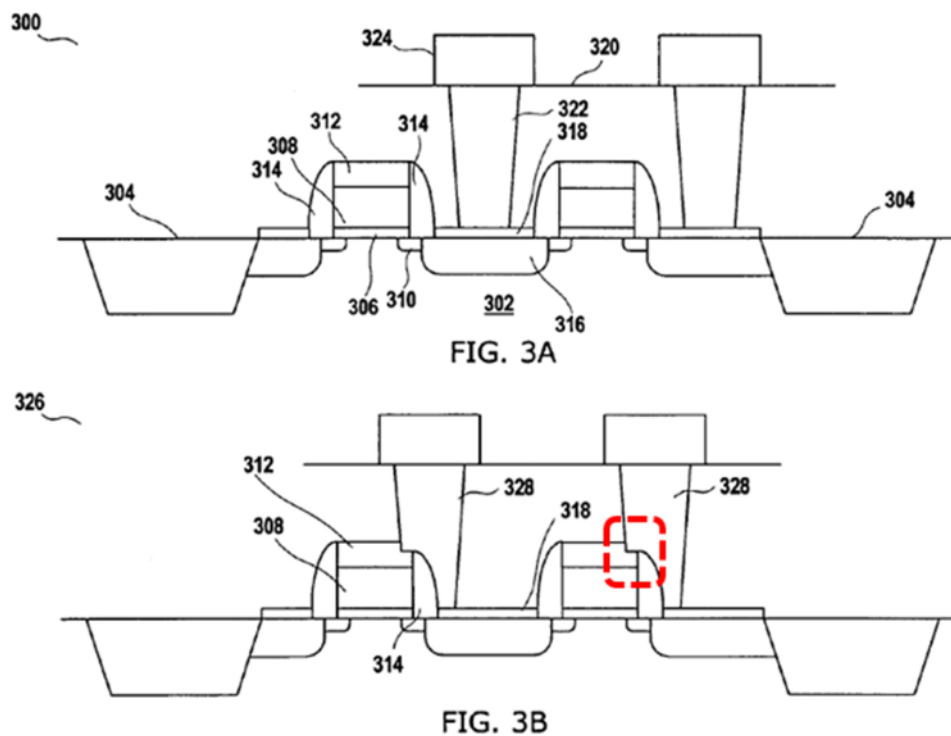
of instead retaining the cap layer. Ex. 2003, ¶63. As such, Ground 1C fails to render obvious claim 2.

B. Ground 1D: The Combination Of Lan and Liaw Does Not Render Obvious A Gate Cap Layer

Next, in Ground 1D, the Petition argues that “[b]y further applying Liaw’s teachings, a POSITA also would have found it obvious to retain Lan’s cap layers 912 and 918 in conjunction with metal gate layers 910 and 916.” Pet., 39. Not so. First, as with Lan’s cap layer, Liaw’s cap layer is subsequently removed after it serves its purpose for assisting in the etching process. Ex. 2003, ¶64. Liaw discloses that, after initially retaining the cap layer as cited by Petitioner, “[i]n step 524, the inter-level dielectric layer 320 and the cap layer 312 are etched through, down to the metal gate conductor 308, forming a gate contact opening (not shown).” Ex. 1006, 6:35-38 (emphasis added). A POSITA would have recognized that this is necessary in order to allow electrical contact with the gate conductor. Ex. 2003, ¶* 64. Thus, because neither Lan nor Liaw’s cap layer is retained, the combination of Lan and Liaw does not render obvious retaining the cap layer. Ex. 2003, ¶64.

Moreover, a POSITA would not have been motivated to combine Lan and Liaw in the manner proposed by the Petition because Liaw’s retained cap layer would not offer any benefit to Lan’s design but would instead only complicate the fabrication process and increase costs. Ex. 1005, 3:46-49; Ex. 2003, ¶65. Liaw’s

cap layer (along with a sidewall spacer) is designed to avoid an undesired electrical connection between the gate conductor and the source/drain regions through a self-aligned contact. Ex. 1006, 1:44-47, 1:67-2:2. For example, Liaw's Figures 3A and 3B illustrate how the cap layer can protect against this problem by separating a misaligned contact and the gate conductive layer:



Ex. 1005, Figs. 3A and 3B (annotated). In Figure 3A above, a well-aligned conductive plug 322 contacts the source/drain region 316 but not the gate. Ex. 2003, ¶67. In this case, the gate cap layer is not necessary because the conductive plug is not in danger of contacting the gate conductive layer. *Id.* However, in Figure 3B above, the conductive plugs 328 are misaligned. Ex. 1006, 5:11. In this case, the

cap layer 312 and sidewall spacer 314 serve to separate the misaligned plug and the gate conductor 308. Ex. 2003, ¶67. Sidewall spacer 314 is quite narrow relative to the size of source/drain region 316, and as a result the exposed part of the source/drain region 316 reaches quite close horizontally to the gate. *Id.* The risk of short occurring due to the plug 328 contacting the gate 308 and the source/drain 316 simultaneously is thus much higher due to the closer distance, in turn due to the narrow sidewall spacer. *Id.*

On the other hand, Lan's design includes not only a sidewall spacer like Liaw's, numbered 112 below, but also an additional, very wide main spacer 302 covering fully half of the source/drain region, and thus already avoids such an undesired electrical connection by separating the exposed portion of the source/drain region 402 from the gate much farther apart than in Liaw, which needs the gate cap. Ex. 2003, ¶68. As shown below, Lan's design differs from Liaw's in that in addition to sidewall spacers 112, Lan's design also includes a "main spacer 302" that covers half of the epitaxial layer that comprises the source/drain (402):

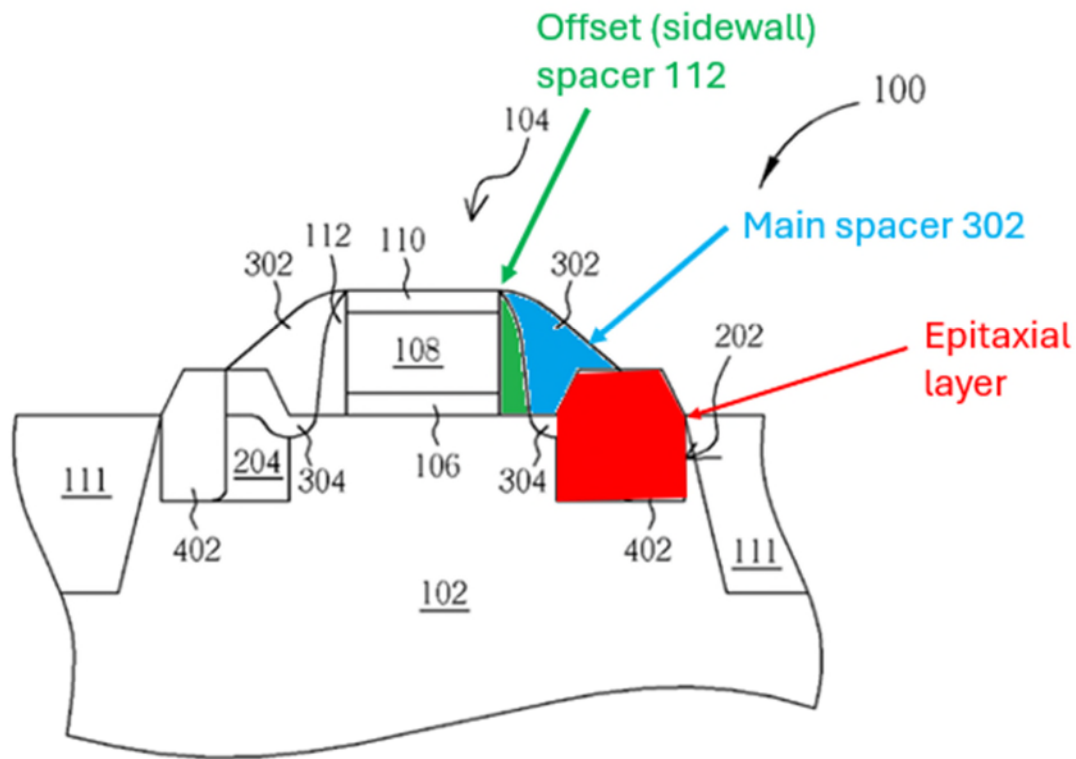


Fig. 4

Ex. 1005, Fig. 4 (annotated). As can be appreciated, this additional spacer separates source/drain 402 significantly from the gate structure. Ex. 2003, ¶69. This creates much better resilience against source/drain contact misalignment than Liaw's narrow sidewalls spacer, because it is far more unlikely that a contact would be able to connect the exposed gate with the farther removed exposed source/drain. Thus, even if a conductive plug contacting the source/drain region were slightly misaligned, the plug would still not contact the gate structure and the source/drain.

Ex. 2003, ¶69. And so Lan’s main spacers obviate the need for Liaw’s cap layer: they serve the same purpose. Ex. 2003, ¶69.

Additionally, as Liaw states, the gate cap layer presents downsides as well. For example, Liaw admits that “[w]hile the cap layer 214 avoids the misalignment problem, it complicates the fabrication process and increases costs.” Ex. 1006, 3:47-49. In light of these downsides, and because Lan’s design obviates the need for Liaw’s cap layer to avoid the misalignment problem, a POSITA would not have been motivated to implement Liaw’s retained cap layer in Lan’s design. Ex. 2003, ¶70.

Accordingly, Ground 1D fails to render obvious claim 2.

C. Grounds 4A and 4B: Chen Does Not Disclose Or Render Obvious A Gate Cap Layer

The Petition alleges that Chen’s “hard mask 503” is the claimed “cap layer.” Pet., 79. This argument fails because even assuming for the sake of argument that Chen’s hard mask constitutes a cap layer like that of the ’847 patent, Chen explicitly states that the hard mask is removed and never says it is retained in any embodiment or that another alleged cap layer is ever added. Ex. 1009, 4:1-3, 6:15-30.

Chen explains that the purpose of its hard mask layer is “to protect the underlying gate structure during etching and deposition steps.” Ex. 1009, 4:46-49. For example, Chen explains that while etching the source and drain regions, “[p]referably, the hard mask remains on the gate structure and does not expose any

of the gate structure during the etching process.” Ex. 1009, 5:28-30. Subsequently, when depositing the epitaxial layers into the etched regions, “the hard mask 401 still remains in tact [sic] to selectively grow the silicon germanium material into the etched regions without depositing on the top of the gate structure.” Ex. 1009, 5:41-44, Fig. 3. Subsequently, Chen explains that “the method **removes the hard mask** to expose 601 the top surface of the gate structures, as shown in FIG. 6.” Ex. 1009, 6:15-18. This is done to silicide the gate and create electrical contact with the gate. Ex. 1009, 6:21-30.

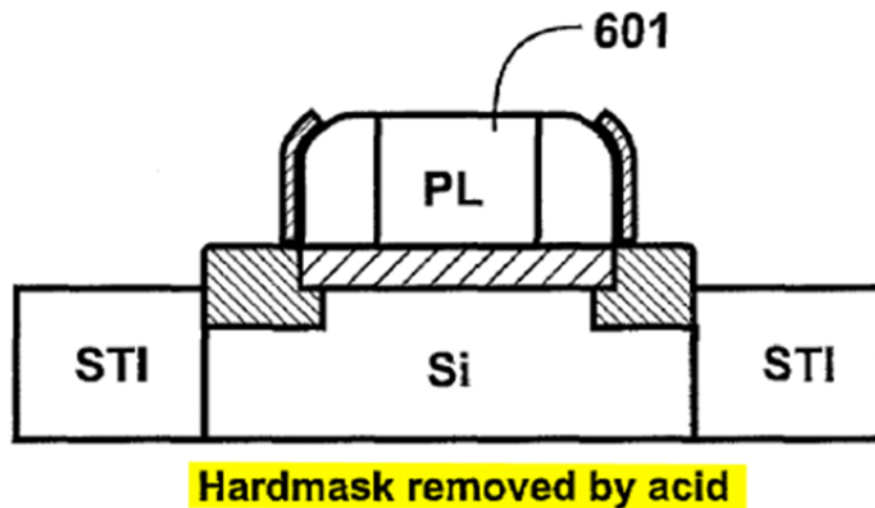


FIGURE 6

Ex. 1009, Fig. 6 (emphasis added). The method is also described such that in step 11 of 12, the method “[s]electively **remove[s] the hard mask on patterned gate layer**

while maintaining the sidewall spacers overlying the patterned gate layer.” *Id.* 4:1-3.

The Petition argues that “Chen discloses an embodiment that retains the cap layer,” arguing that Chen’s Figure 5 (which includes the hard mask) is a “finish[ed]... device,” which is an apparent reference to the claim requiring a “MOS transistor structure.” Pet., 80. But Figure 5 is not a “MOS transistor structure,” because it is not a transistor. Ex. 2003, ¶74. As Petitioner’s expert conceded, the device in Figure 5 would not function as a transistor. Ex. 2004, 83:14-24. The Petition’s basis for its argument is that Chen states: “To finish the device according to an embodiment of the present invention, the method forms sidewall spacers 501 from the second protective layer, as illustrated by FIG. 5.” Pet., 80 (citing Ex. 1009, 6:11-18). However, this language does not indicate that Fig. 5 represents a “finished device,” as the Petition suggests. Ex. 2003, ¶74. This first sentence of the paragraph introduces a number of steps in the paragraph as a whole that are required to finish the device. *Id.* The specification indicates that Fig. 5 illustrates forming sidewall spacers 501, which is merely one step of “finish[ing] the device,” not that Fig. 5 illustrates a finished device. *Id.* Subsequent steps for finishing the device are described in the remaining portion of the paragraph. *Id.*; Ex. 1009, 6:11-31. At a minimum, the inclusion of those steps is explicitly indicated because Figure 6 is a later step in the process, and in Figure 6, the hard mask has been removed. Ex. 1009,

Fig. 6. Indeed, the remainder of the paragraph states that further steps are necessarily performed after Figure 5, including: (1) “remov[ing] the hard mask to expose 601 the top surface of the gate structures, as shown in FIG. 6”; (2) “form[ing] a silicide layer overlying gate layer and source/drain regions”; (3) “form[ing] an interlayer dielectric layer overlying NMOS and PMOS transistor devices”; and (4) “perform[ing] electrical contacts.” Ex. 1009, 6:21-31. These are steps required by Chen and are not described as optional. *Id.* And a POSITA would know they are required to create a transistor as claimed. Ex. 2003, ¶74. Thus, the Petition is incorrect that Chen discloses a transistor, as claimed, with a hard mask.

The Petition also argues that a POSITA would have found it obvious to retain Chen’s hard mask in the final device structure. Pet., 81. Specifically, the Petition alleges that the hard mask would not be removed for two reasons: (1) “[i]n device regions where silicide is unwanted on a polysilicon gate”; or (2) if Chen’s conductive gate layer were made of metal, for the same reasons as alleged with respect to Ground 1C. Pet., 81.

As to the first rationale, it is purely speculative. Chen explicitly states that “[t]he method forms a silicide layer overlying gate layer” and that in order to accomplish that, it removes the hard mask. Ex. 1009, 6:15-25. There is no discussion of not siliciding the gate (whether metal or polysilicon) and no discussion of not removing the hard mask. As to the second rationale, wherein the Petition

alleges a POSITA would have found it obvious to retain Chen's hard mask for the same reasons that a POSITA would have found it obvious to retain Lan's cap layer in Ground 1C (Pet., 81-82), it fails for the same reasons as explained above with respect to Lan: (1) the proposed modification is unworkable because it would create a further problem of the hard mask blocking access to the gate conductive layer, and the Petition offers no solution for how this problem would be resolved, and (2) there are numerous reasons to remove the cap layer, as explained above regarding Lan. *Supra* §V.A; Ex. 2003, ¶76.

Accordingly, Chen does not disclose or render obvious limitation [2.c] and Grounds 4A and 4B fail.

VI. CONCLUSION

For at least the reasons discussed above, the challenged claims of the '847 patent should be found patentable.

Dated: January 9, 2026

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the portions of the above-captioned PATENT OWNER'S RESPONSE specified in 37 C.F.R. § 42.24 have 8,660 words, in compliance with the 14,000 word limit set forth in 37 C.F.R. § 42.24(b)(1). This word count was prepared by the word-processing program used to prepare this paper (Microsoft Word).

Dated: January 9, 2026

/s/ William A. Meunier

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CERTIFICATE OF SERVICE

I certify that a copy of this PATENT OWNER'S RESPONSE is being served
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