

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,  
Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,  
Patent Owner.

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Case No. IPR2025-00847  
U.S. Patent No. 7,745,847 B2

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**DECLARATION OF JOSEPH C. MCALEXANDER III REGARDING  
PATENT OWNER'S RESPONSE**

## TABLE OF CONTENTS

|        |                                                                                                                                                                                                                                                                                                                                     |    |
|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| I.     | Qualifications .....                                                                                                                                                                                                                                                                                                                | 1  |
| II.    | OVERVIEW.....                                                                                                                                                                                                                                                                                                                       | 2  |
| III.   | MATERIALS CONSIDERED.....                                                                                                                                                                                                                                                                                                           | 4  |
| IV.    | UNDERSTANDING OF THE LAW.....                                                                                                                                                                                                                                                                                                       | 4  |
|        | A. Claim Construction.....                                                                                                                                                                                                                                                                                                          | 4  |
|        | B. Invalidity .....                                                                                                                                                                                                                                                                                                                 | 5  |
| V.     | SEMICONDUCTOR TRANSISTOR TECHNOLOGY                                                                                                                                                                                                                                                                                                 |    |
| PRIMER | 7                                                                                                                                                                                                                                                                                                                                   |    |
|        | A. Basic Transistor Components.....                                                                                                                                                                                                                                                                                                 | 7  |
|        | B. Planar vs. Three-Dimensional Transistors .....                                                                                                                                                                                                                                                                                   | 10 |
|        | C. Processes For Manufacturing Integrated Circuits And<br>Transistors .....                                                                                                                                                                                                                                                         | 12 |
|        | 1. The Four Stages Of Fabricating Integrated Circuits.....                                                                                                                                                                                                                                                                          | 12 |
|        | 2. The Wafer Fabrication Stage .....                                                                                                                                                                                                                                                                                                | 13 |
| VI.    | THE INVENTION OF THE '847 PATENT .....                                                                                                                                                                                                                                                                                              | 15 |
| VII.   | THE PETITION GROUNDS FAIL TO DISCLOSE OR<br>RENDER OBVIOUS LIMITATIONS OF INDEPENDENT CLAIM 1 .....                                                                                                                                                                                                                                 | 18 |
|        | A. Petition Grounds 4A And 4B Fail To Disclose Or Render<br>Obvious “Two Raised Epitaxial Layers Positioned Respectively<br>In The Semiconductor Substrate Next To The Relative Sides Of<br>The Gate” And “Two Doped Regions Formed Respectively In<br>The Semiconductor Substrate Next To The Relative Sides Of<br>The Gate” ..... | 18 |
| VIII.  | THE PETITION GROUNDS FAIL TO DISCLOSE OR<br>RENDER OBVIOUS LIMITATIONS OF CLAIM 2.....                                                                                                                                                                                                                                              | 24 |
|        | A. Ground 1C: Lan Does Not Disclose Or Render Obvious A Gate<br>Cap Layer .....                                                                                                                                                                                                                                                     | 24 |
|        | B. Ground 1D: The Combination Of Lan and Liaw Does Not<br>Render Obvious A Gate Cap Layer.....                                                                                                                                                                                                                                      | 29 |

C. Grounds 4A and 4B: Chen Does Note Disclose Or Render  
Obvious A Gate Cap Layer .....34

IX. CONCLUSION .....38

## **I. Qualifications**

1. I am a Registered Professional Engineer (#79454) and the President of M<sup>c</sup>Alexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involved use of mechanical calibration and

measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae, which is attached to my first declaration in this matter (Ex. 2001).

## **II. OVERVIEW**

4. Claims 1-11 of U.S. Patent No. 7,745,847 (“the ’847 Patent”) should be found patentable because none of Petitioner’s presented grounds anticipates or renders obvious those claims. Petitioner’s presented grounds fail for multiple reasons. First, as explained in my first declaration (Ex. 2001), none of the asserted

references mention, describe, or concern “raised epitaxial layers,” as required by all challenged claims. Instead, the Petition relies on interpretations of drawings in those references that are inconsistent with and not supported by the accompanying text. Thus, all grounds fail to disclose or render obvious raised epitaxial layers.

5. Moreover, if the Board instead finds that the drawings are clear enough to be relied upon, those same drawings and the descriptions of them in the specification illustrate that other challenged claim limitations are not met by the references. For example, the Petition relies on the Chen reference (Ex. 1008) in Grounds 4A and 4B. However, Chen’s drawings and text show that its epitaxial layers are not “positioned... next to the relative sides of the gate.” Grounds 3 and 4 fail to disclose or render obvious at least claim element [1.c].

6. Finally, none of the asserted grounds disclose or render obvious dependent claim 2, wherein the gate includes additional layers including a cap layer. The only grounds that challenge claim 2 are Grounds 1C (Lan), 1D (Lan and Liaw) and 4A/4B (Chen). As to Ground 1C, Petitioner concedes that the cap layer is removed in Lan and does not rely on it in the only described embodiment that addresses the cap layer. Instead, the Petition asserts that a POSITA would know in another embodiment in which the gate uses a metal conductive layer, that he or she would not remove the cap layer. But Lan does not say that. There are several reasons a POSITA *would* also remove the cap layer in that embodiment, consistent with

Lan's only teaching that the cap layer is removed. Lan's silence on the issue with the use of a metal gate conductive layer, combined with its explicit disclosure of affirmatively removing the cap, is insufficient to disclose the cap layer of claim 2. As to Ground 1D, there is no motivation to combine Lan and Liaw. Petitioner alleges Liaw has a cap layer whose sole use is to protect against misalignment of a source/drain plug contact. But Lan already contains a different measure to protect against misalignment of such a plug, and so does not benefit from Liaw—a POSITA would not combine them. As to Ground 4A/4B, Chen explicitly says to remove the cap layer.

### **III. MATERIALS CONSIDERED**

7. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the materials that they cite, including the asserted prior art.

### **IV. UNDERSTANDING OF THE LAW**

8. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

#### **A. Claim Construction**

9. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a physical machine, etc.

10. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

11. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

## **B. Invalidity**

12. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

13. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

14. I have been informed that, in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

15. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one is to consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that, for such objective evidence to be relevant to the non-obviousness of claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

16. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that

the prior art must create a reasonable expectation of success in producing the claimed subject matter.

## **V. SEMICONDUCTOR TRANSISTOR TECHNOLOGY PRIMER**

17. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors.

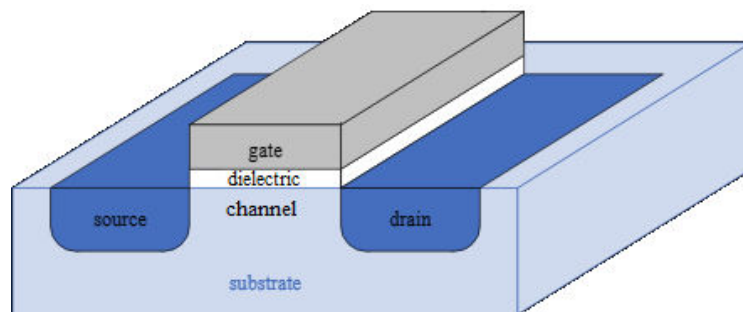
### **A. Basic Transistor Components**

18. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (*i.e.*, turning access to electrical current on and off) and amplification (*i.e.*, increasing the amplitude of a signal while retaining its electrical characteristics). Ex. 2002 at 1-2. Where earlier tube devices used a vacuum tube to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. Ex. 2002 at 3.

19. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. Ex. 2002 at 29-34. In a conductor (*e.g.*,

a metal), electric current can flow freely. Ex. 2002 at 29. A dielectric (*e.g.*, silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. Ex. 2002 at 30. Semiconductors (*e.g.*, silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. Ex. 2002 at 31-34.

20. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. *See, e.g.*, Ex. 2002 at 510-511. The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



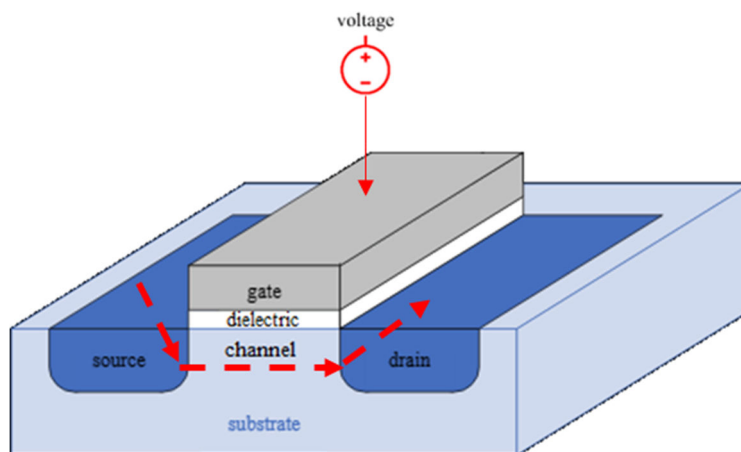
*See, e.g.*, Ex. 2002 at 510-511.

21. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). Ex. 2002 at 26-28, 427-28. The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source

and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). Ex. 2002 at 510-511.

22. The gate is a conductor (or semiconductor) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. Ex. 2002 at 510-511. When a voltage is applied to the gate, the dielectric prevents the “flow of charge” (current) between the gate and the channel, but the applied voltage results in the creation of a “field effect” in the channel. Ex. 2002 at 510-511. This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). Ex. 2002 at 510-511.

23. As illustrated below, this field effect allows charge to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping drain-to-source or source-to-drain current.

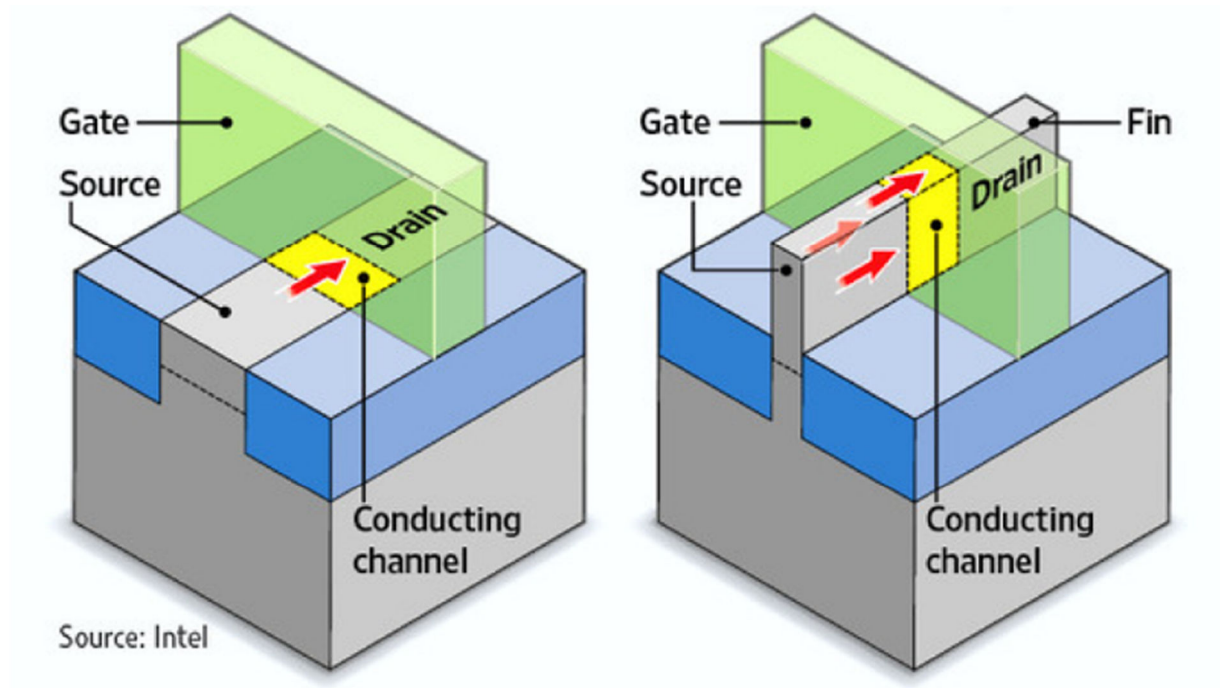


**B. Planar vs. Three-Dimensional Transistors**

24. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.”

25. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

26. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



27. In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.

28. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than

planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

### **C. Processes For Manufacturing Integrated Circuits And Transistors**

#### **1. The Four Stages Of Fabricating Integrated Circuits**

29. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

30. In the first stage, the semiconductor material itself is created. Ex. 2002 at 13. For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. Ex. 2002 at 13.

31. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” Ex. 2002 at 13-14. A wafer acts as a semiconductor substrate on and in which transistors may be formed.

32. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. Ex. 2002 at 14. Thousands of integrated circuits can be formed on the substrate of a single wafer. Ex. 2002 at 14.

33. In the packaging stage, the wafer is separated into individual chips. Ex. 2002 at 14-15.

## 2. The Wafer Fabrication Stage

34. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in and on the wafer's substrate. Ex. 2002 at 14. These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). *See* Ex. 2002 at 29-31, 71. For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

35. **Layering** is the operation used to add thin layers to the semiconductor substrate. Ex. 2002 at 72. The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. Ex. 2002 at 72.

36. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate, additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor

structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. Ex. 2002 at 72.

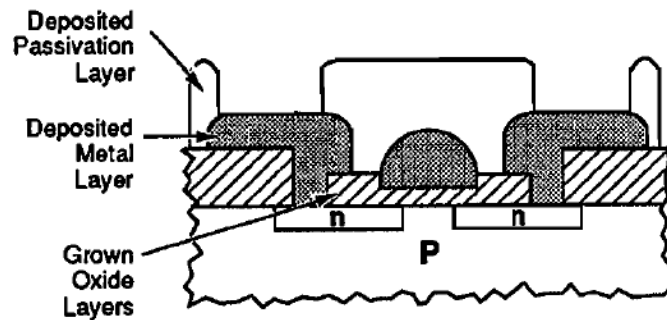


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

37. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. Ex. 2002 at 72-73. This creates a pattern on the wafer surface. Ex. 2002 at 72-73.

38. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. Ex. 2002 at 72-73. For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

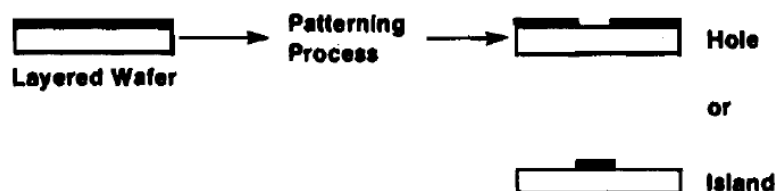


Figure 4.7 Patterning.

39. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

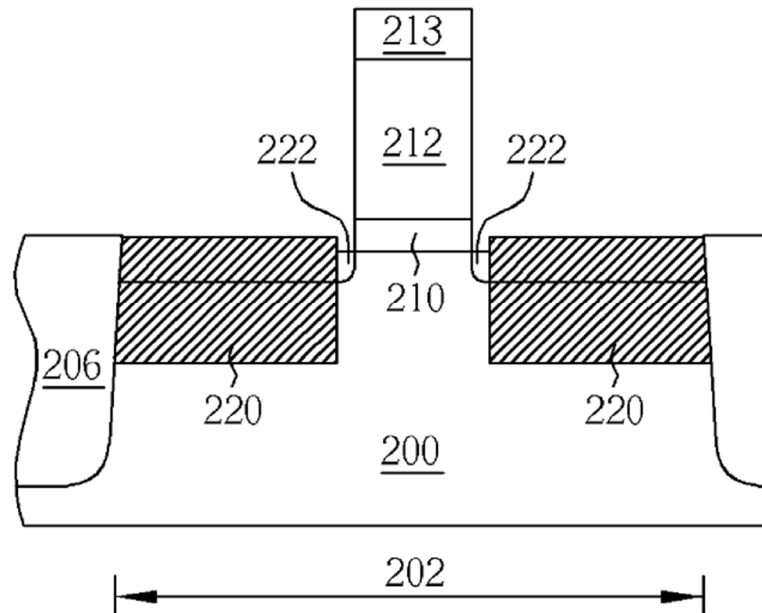
Ex. 2002 at 73.

## **VI. THE INVENTION OF THE '847 PATENT**

40. The '847 Patent describes and claims improved FET designs intended to improve the transistor's performance. For example, the patent discloses "a method of fabricating strained silicon channel MOPS transistors to improve the shortages from the prior art, and then increase the carrier mobility of MOS transistors." Ex. 1001, 1:49-52. One characteristic of the improved fabrication process "is to form the epitaxial layer before forming the spacer." *Id.*, 6:64-65. "[T]hus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer." *Id.*, 6:65-67. Moreover, "the process of etching the recess is carried out before forming the spacer. At this moment, the pattern density on the semiconductor substrate is lower than the time when the spacer is formed, thus the

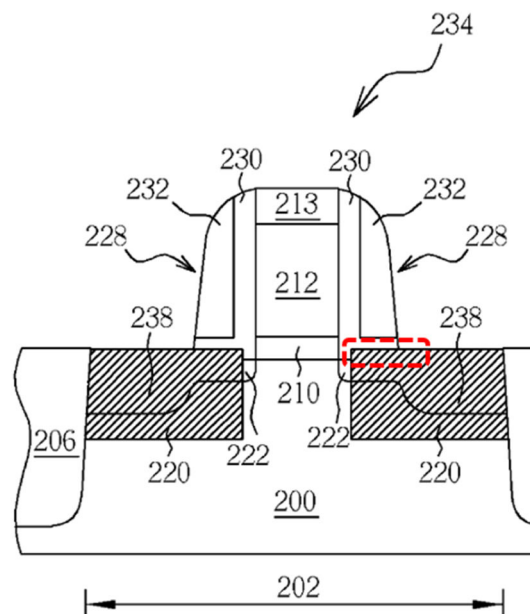
micro-loading effect caused by the pattern density can be reduced, and then the uniformity in etching the recess is increased.” *Id.*, 6:67-7:6.

41. The claims of the '847 patent are directed to a MOS transistor structure fabricated using the described novel fabrication method. Because the recess and epitaxial layer are formed before the spacer is formed, the method results in a novel MOS transistor structure, which includes “two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate” and “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.” This is illustrated in Figures 4 and 5 of the '847 patent. In Figure 4, the raised epitaxial layers 220, as well as the doped regions 222, are formed next to the sides of the gate structure before any spacers are formed:



Ex. 1001, Fig. 4 (partial).

42. Subsequently, as shown in Figure 5, the spacers are formed on top of the raised epitaxial layers:

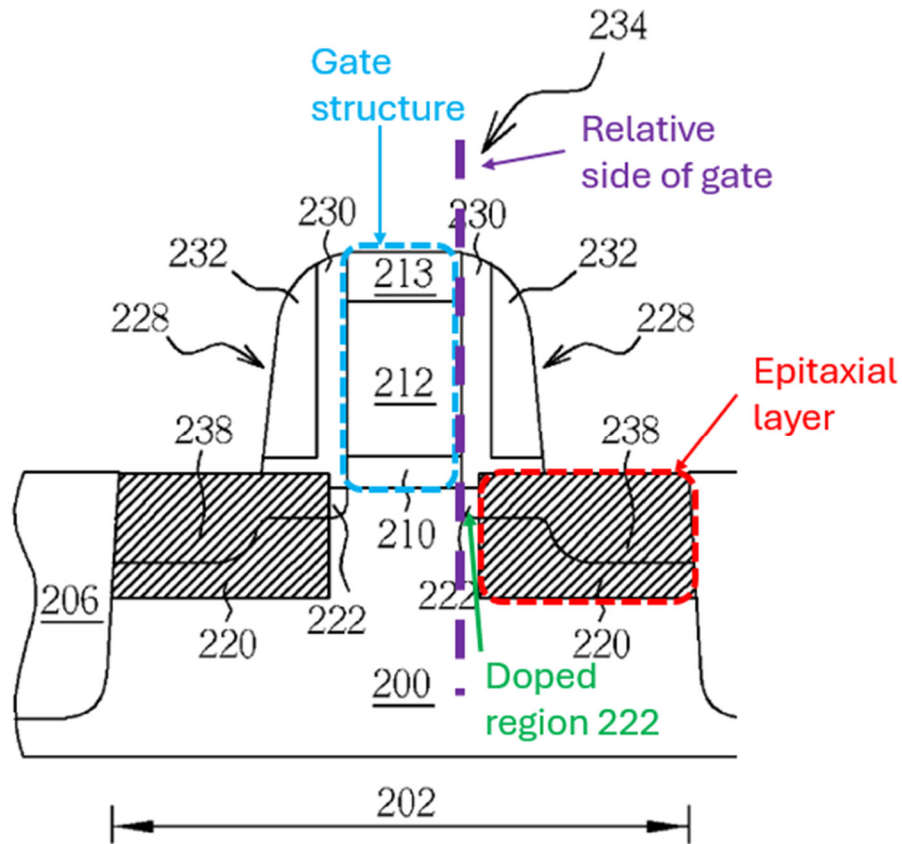


Ex. 1001, Fig. 5 (partial and annotated).

**VII. THE PETITION GROUNDS FAIL TO DISCLOSE OR RENDER OBVIOUS LIMITATIONS OF INDEPENDENT CLAIM 1**

**A. Petition Grounds 4A And 4B Fail To Disclose Or Render Obvious “Two Raised Epitaxial Layers Positioned Respectively In The Semiconductor Substrate Next To The Relative Sides Of The Gate” And “Two Doped Regions Formed Respectively In The Semiconductor Substrate Next To The Relative Sides Of The Gate”**

43. Limitation [1.b] recites “two raised epitaxial layers positioned respective in the semiconductor substrate next to the relative sides of the gate.” Similarly, limitation [1.e] recites “two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.” As explained above in §VI, the claimed MOS transistor structure is fabricated in a manner such that the raised epitaxial layer and doped regions are formed before a sidewall spacer. As a result, the raised epitaxial layer and doped region are positioned next to the relative side of the gate because their positions are not limited by the width of the spacer. Ex. 1001, 6:64-67. This is illustrated in Figure 5 of the ’847 patent, which shows that raised epitaxial layer 220 and doped region 222 are next to the relative side of the gate:



Ex. 1001, Fig. 5 (partial and annotated).

44. “Each gate 208 comprises a dielectric layer 210, a conductive layer 212 positioned on the dielectric layer 210 and a cap layer 213 positioned on the conductive layer 212.” Ex. 1001, 3:3-6. As can be observed in the above Figure 5, the doped region 222 and raised epitaxial layer 220 are next to—as opposed to under—each of the layers that make up the gate stack, with some horizontal space in between the gate stack and the raised epitaxial layer.

45. In contrast, Chen's fabrication method forms a "gate dielectric layer 107" and "sidewall spacers 113" before etching recesses and forming epitaxial layers:

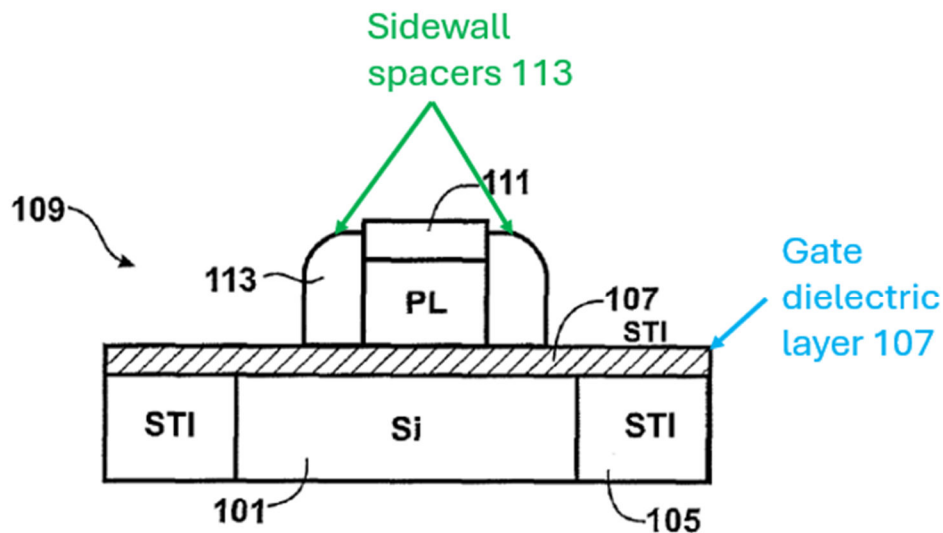
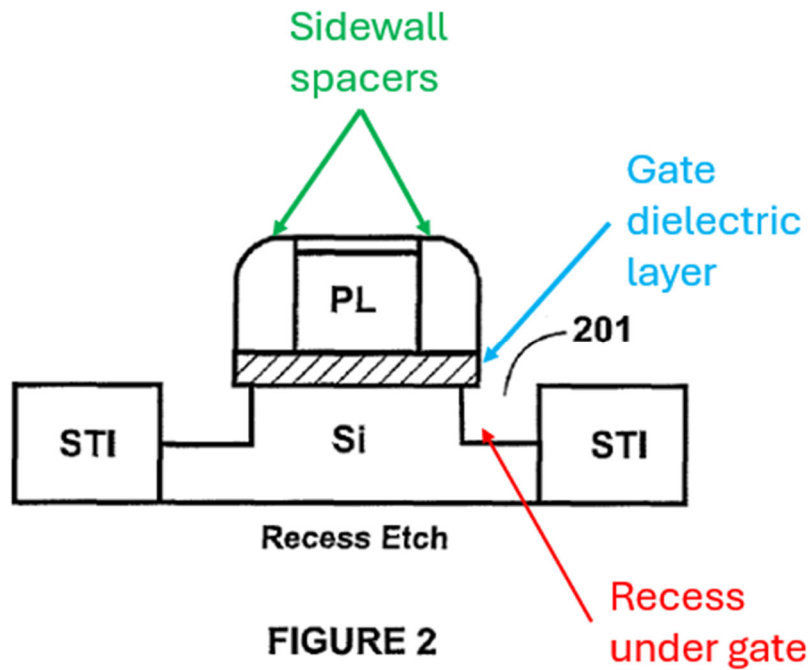


FIGURE 1

Ex. 1009, Fig. 1 (annotated), 4:30-59.

46. Then, as shown in Figure 2, the recesses are etched:



Ex. 1009, Fig. 2 (annotated).

47. As shown, because the gate dielectric layer extends to the edges of the sidewall spacers, the recesses are etched under the gate rather than next to the relative side of the gate.

48. Finally, the epitaxial layer is formed in the etched recess:

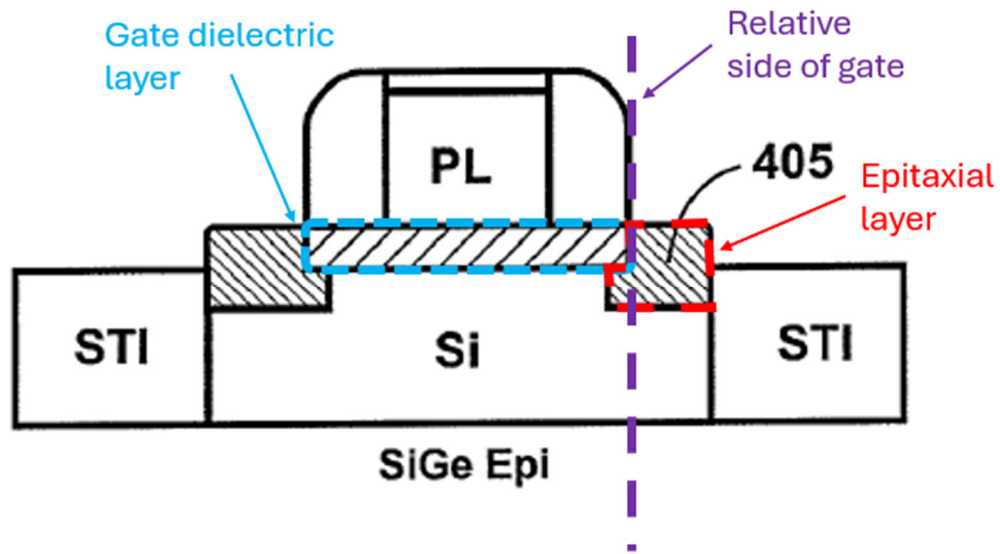
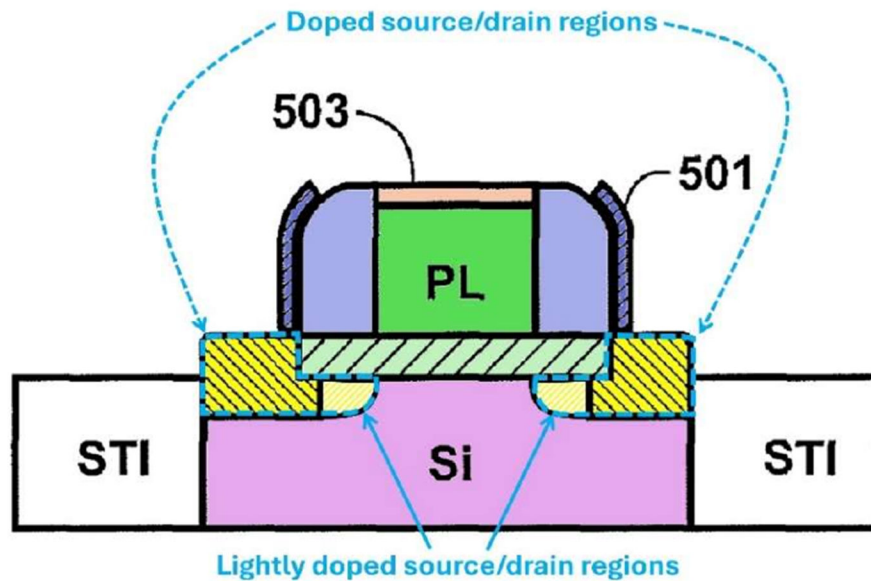


**FIGURE 3**

Ex. 1009, Fig. 3 (annotated).

49. As shown, the epitaxial layer is under the gate dielectric layer, rather than “next to the relative sides of the gate,” as required by limitation [1.b].

50. Similarly, the Petition acknowledges that the doped regions would also be positioned under the gate dielectric layer:



**Chen, FIG. 5 (annotated, LDD added)**

Pet., 76 (annotated Ex. 1009, Fig. 5).

51. This distinction is significant because positioning the doped region and epitaxial layer under the gate (as disclosed in Chen) increases the risk of an electrical or physical short between the gate and the source/drain region. The '847 patent's design avoids this potential problem by positioning the doped region and epitaxial layer "next to the relative sides of the gate," as recited in claim 1.

52. The Petition acknowledges that Chen's gate dielectric layer extends to the edges of the sidewall spacers. Pet., 70 (annotating Ex. 1008, Fig. 5 to show gate dielectric layer 107 in light green). The Petition further acknowledges that the gate dielectric layer is part of the gate structure. Pet., 70 ("The gate dielectric layer, gate layer, and hard mask layer form 'a PMOS gate structure 109.'"). Nevertheless, the

Petition alleges, without explanation, that the epitaxial layers and doped regions are “next to the relative sides of the gate.” Pet., 72, 76-77. This unsupported allegation is incorrect, as the epitaxial layer is clearly shown to be under the gate in Figure 3.

53. Thus, Lan does not disclose or render obvious limitations [1.b] and [1.e] and Grounds 4A and 4B fail.

### **VIII. THE PETITION GROUNDS FAIL TO DISCLOSE OR RENDER OBVIOUS LIMITATIONS OF CLAIM 2**

54. The Petition alleges that Grounds 1C/1D and 4A/4B anticipate or render obvious dependent claim 2. First, these grounds fail for the same reasons as stated above with respect to independent claim 1. *Supra* §VI. Grounds 1C and 1D rely on Lan to disclose or render obvious “the structure of claim 1,” as required by claim 2. Pet., 33. Grounds 4A and 4B rely on Chen to disclose or render obvious “the structure of claim 1.” Pet., 78. But as explained above, neither Lan nor Chen discloses or renders obvious claim 1.

55. Moreover, Grounds 1C/1D and 4A/4B fail to disclose or render obvious that “the gate further comprises... a cap layer,” as required by limitation [2.c].

#### **A. Ground 1C: Lan Does Not Disclose Or Render Obvious A Gate Cap Layer**

56. The Petition alleges that “Lan’s gates 904 and 906 comprise ‘cap layers 912, 918.’” Pet., 35. However, as the Petition acknowledges, Lan’s cap layers must

be removed. Pet., 36 (citing Ex. 1005, 5:35-37). Thus, Lan does not disclose a gate cap layer.

57. Lan's cap layer "serve[s] as [an] etching mask[], so as to form recesses 202 in the substrate 102 of the two side of the gate 104." Ex. 1005, 2:59-62. Once the recesses are formed, the cap layer would serve no additional purpose and would be removed. Indeed, the Petition admits that a POSITA would have understood that Lan's cap layer would be removed. Pet., 36.

58. Despite admitting that Lan's described fabrication process would require removing the gate cap layer, the Petition nevertheless alleges that a POSITA would have found it obvious to retain the cap layer if the conductive layer of the gate were made of metal. Pet., 39. The Petition argues that the cap layer would only be removed in order to perform a salicide process, which is only beneficial, according to the Petition, if the gate conductive layer is polysilicon rather than metal. Pet., 37-38. Petitioner points to no disclosure of retaining the cap layer, but thus argues that because there is no reason to remove the cap layer when the gate is metal, a POSITA would know it would be retained.

59. But Petitioner is simply incorrect that there is no reason to remove the cap layer when the gate is metal. First, the gate cap layer would need to be removed because the cap layer would block access to the gate conductive layer. A voltage must be applied to the gate in order to allow charge to flow between the source and

drain, *i.e.*, for the transistor to operate, and that in order to apply that voltage, the gate conductive layer must be contacted. *See supra* §**Error! Reference source not found.**; Ex. 2004, 31:16-19. Thus, the Petition’s proposed modification of Lan—retaining the gate cap layer—is unworkable because it would create a further problem of blocking access to the gate conductive layer. The Petition offers no solution for how this problem would be resolved.

60. Second, there are multiple reasons to remove the gate cap layer and to deposit followed by diffusion additional metal onto the gate even when the gate is metal, not only when it is polysilicon (a “silicide” or “salicide” process). Depositing followed by diffusion of an additional metal when the gate is metal (as when the gate is polysilicon) is beneficial for several reasons—and such a deposition followed by diffusion, like a salicide, requires removal of the cap layer. For example, in general, a metal contact can be, and often is, a different metal from the gate metal, as Petitioner’s expert agreed. Ex. 2004, 31:20-22. A POSITA would have understood that a gate and contact would often be formed from different metals due to unique functional requirements for the respective components. Moreover, the gate metal is typically deposited at a higher temperature than the contact metal, which further limits the selection of a specific metal material for the gate, as a metal with too low a melting temperature will melt and not be suitable, whereas the contact is deposited at a lower temperature, leading to a great set of options to choose from..

61. However, interconnecting dissimilar metals leads to poor adhesion between the gate metal and the contact metal, as well as higher-than-desired contact resistance between the two. For example, tungsten is often used as a contact metal because of its gap-fill characteristics, while titanium may be more suitable for a gate due to its work function, and could be used in Lan, as Lan does not restrict what metal is used for the gate.. *Id.*; Ex. 2004, 29:4-21, 42:19-43:13. A POSITA would have known that it would be beneficial to diffuse an additional metal, such as nickel (which is a common diffusion metal used in a salicide process) into a gate (which may be titanium) before connecting the metal contact, for example, which may be tungsten. Ex. 2004, 25:21-26:16; *see* Ex. 2005, 446 (explaining benefits of interdiffusing titanium and nickel to fine-tune work function of a metal gate). This would benefit, for example, the tunability of the work function, which impacts threshold voltage of a transistor, which is a key factor in transistor design. Thus, a POSITA would have known it was beneficial to be able to fine-tune the work function as desired for the given design. In addition, Petitioner's expert testified that in certain settings, the interface between the metal contact and the gate might not be as clean as one would like, and when asked if a POSITA would diffuse a metal into a gate in that scenario, he agreed "people might do things like that." Ex. 2002, 34:24-35:24. Such a diffusion would also improve adhesion, for example, if the same metal as the contact were diffused into the gate before the contact-gate junction is formed.

Thus, there are reasons to remove the cap layer in the gate, rather than to keep the cap layer when the gate is metal. Further, Petitioner's expert admitted that a titanium nitride "liner" would "help with the connectivity" between a tungsten contact and another metal as the gate. Ex. 2004, 33:11-34:23.

62. Moreover, even if the gate conductive layer is metal, a salicide process would still need to be performed on the source and drain regions. The Petition argues that a POSITA would know that the cap layer on the gate is beneficial to retain (despite not being discussed as being retained in Lan) because "if cap layers 912 and 918 were removed when forming silicide on source/drain regions 1206 and 1208, the metal gate layers 910 and 916 would be exposed to the etchant used to strip the unreacted silicidation metal, which could remove, corrode, or otherwise damage metal layers 910 and 916." Pet., 37 (internal citations omitted). However, this argument makes no sense, because a POSITA would have understood that, in selectively removing any unreacted silicidation metal, an etchant would be selected that would not attack the metal gate. Thus, retaining the cap layer is not necessary to protect the metal layers of the gate during a salicide process performed on the source/drain. Moreover, a POSITA would have understood that even if a small portion of the metal layer was removed by the etchant, this would not be an issue due to the large relative thickness of the gate as compared to the unreacted silicidation metal. The amount of etching necessary to remove the unreacted

silicidation metal is very low relative to the large thickness of the gate metal, which would be functionally unaffected. Thus, the Petition's explanation does not provide a reasonable justification for retaining the cap layer.

63. In short, the Petition admits that Lan's fabrication method requires removing the gate cap layer and does not offer sufficient rationale for its proposed modification of instead retaining the cap layer. As such, Ground 1C fails to render obvious claim 2.

**B. Ground 1D: The Combination Of Lan and Liaw Does Not Render Obvious A Gate Cap Layer**

64. Next, in Ground 1D, the Petition argues that "[b]y further applying Liaw's teachings, a POSITA also would have found it obvious to retain Lan's cap layers 912 and 918 in conjunction with metal gate layers 910 and 916." Pet., 39. Not so. First, as with Lan's cap layer, Liaw's cap layer is subsequently removed after it serves its purpose for assisting in the etching process. Liaw discloses that, after initially retaining the cap layer as cited by Petitioner, "[i]n step 524, the inter-level dielectric layer 320 *and the cap layer 312 are etched through, down to the metal gate conductor 308*, forming a gate contact opening (not shown)." Ex. 1006, 6:35-38 (emphasis added). A POSITA would have recognized that this is necessary in order to form a gate contact opening to allow electrical contact with the gate conductor. Thus, because neither Lan nor Liaw's cap layer is retained, the

combination of Lan and Liaw does not render obvious retaining the cap layer, in fact, just the opposite.

65. Moreover, a POSITA would not have been motivated to combine Lan and Liaw in the manner proposed by the Petition because Liaw would not offer any benefit to Lan's design but would instead only complicate the fabrication process and increase costs. Ex. 1005, 3:46-49.

66. Liaw's cap layer (along with a sidewall spacer) is designed to avoid an undesired electrical connection between the gate conductor and the source/drain regions through a self-aligned contact. Ex. 1006, 1:44-47, 1:67-2:2. For example, Liaw's Figures 3A and 3B illustrate how the cap layer can protect against this problem by separating a misaligned contact and the gate conductive layer:

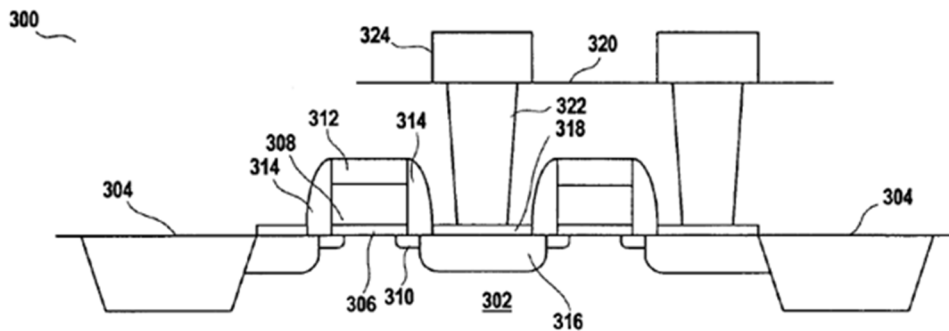


FIG. 3A

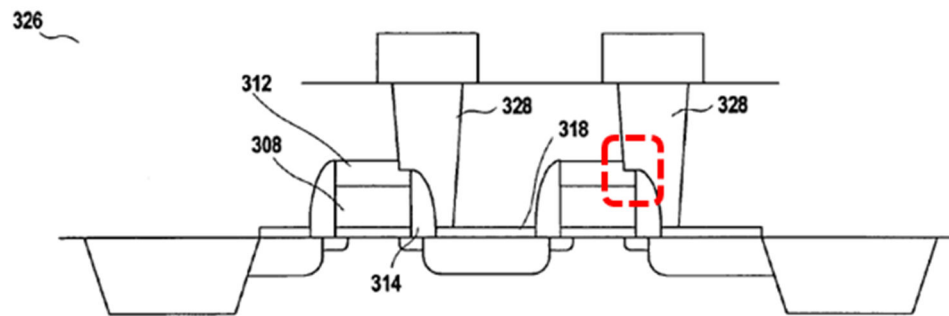


FIG. 3B

Ex. 1005, Figs. 3A and 3B (annotated).

67. In Figure 3A above, a well-aligned conductive plug 322 contacts the source/drain region 316 but not the gate. In this case, the gate cap layer is not necessary because the conductive plug is not in danger of contacting the gate conductive layer. *Id.* However, in Figure 3B above, the conductive plugs 328 are misaligned. Ex. 1006, 5:11. In this case, the cap layer 312 and sidewall spacer 314 serve to separate the misaligned plug and the gate conductor 308. Sidewall spacer 314 is quite narrow relative to the size of source/drain region 316, and as a result, the exposed part of the source/drain region 316 reaches quite close horizontally to the gate. The risk of short occurring due to the plug 328 contacting the gate 308 and

the source/drain 316 simultaneously is thus much higher due to the closer distance, in turn due to the narrow sidewall spacer.

68. On the other hand, Lan's design not only includes a sidewall spacer like Liaw's, numbered 112 below, but also includes an additional, very wide main spacer 302 covering fully half of the source/drain region, thus already avoiding such an undesired electrical connection by separating the exposed portion of the source/drain region 402 from the gate much farther apart than in Liaw, which needs the gate cap. As shown below, Lan's design differs from Liaw's in that, in addition to sidewall spacers 112, Lan's design also includes a "main spacer 302" that covers half of the epitaxial layer that comprises the source/drain:

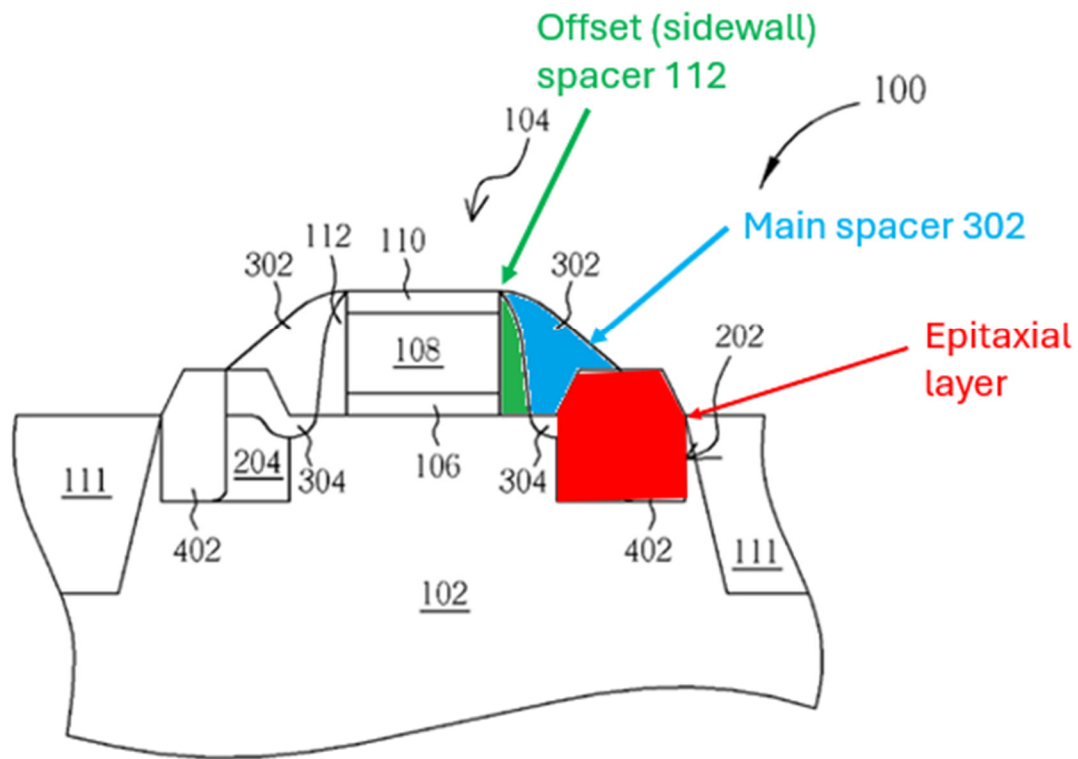


Fig. 4

Ex. 1005, Fig. 4 (annotated).

69. As can be appreciated, this additional spacer separates source/drain 402 significantly from the gate structure. This creates much better resilience against source/drain contact misalignment than Liaw's narrow sidewall spacer, because it is far more unlikely that a contact would be able to connect the exposed gate with the farther removed exposed source/drain. Thus, even if a conductive plug contacting the source/drain region were slightly misaligned, the plug would still not contact the

gate structure and the source/drain. As such, Lan's main spacers obviate the need for Liaw's cap layer; they serve the same purpose.

70. Additionally, as Liaw states, the gate cap layer presents downsides as well. For example, Liaw admits that "[w]hile the cap layer 214 avoids the misalignment problem, it complicates the fabrication process and increases costs." Ex. 1006, 3:47-49. In light of these downsides, and because Lan's design obviates the need for Liaw's cap layer to avoid the misalignment problem, a POSITA would not have been motivated to implement Liaw's retained cap layer in Lan's design.

71. Accordingly, Ground 1D fails to render obvious claim 2.

**C. Grounds 4A and 4B: Chen Does Not Disclose Or Render Obvious A Gate Cap Layer**

72. The Petition alleges that Chen's "hard mask 504" is the claimed "cap layer." Pet., 79. This argument fails because, even assuming for the sake of argument that Chen's hard mask constitutes a cap layer like that in the '847 patent, Chen explicitly states that the hard mask is removed and never says it is retained in any embodiment or that another alleged cap layer is ever added. Ex. 1009, Fig. 6, 6:16-18. Chen explains that the purpose of its hard mask layer is "to protect the underlying gate structure during etching and deposition steps." Ex. 1009, 4:46-49. For example, Chen explains that while etching the source and drain regions, "[p]referably, the hard mask remains on the gate structure and does not expose any

of the gate structure during the etching process.” Ex. 1009, 5:28-30. This prevents accidental damage to the gate during the etching process. Subsequently, when depositing the epitaxial layers into the etched regions, “the hard mask 401 still remains in tact [sic] to selectively grow the silicon germanium material into the etched regions without depositing on the top of the gate structure.” Ex. 1009, 5:41-44, Fig. 3. A POSITA would have understood that the reason Chen emphasizes that the hard mask remains intact during these steps is that the mask is later removed. Indeed, subsequently, Chen explains that “the method removes the hard mask to expose 601 the top surface of the gate structures, as shown in FIG. 6.” Ex. 1009, 6:16-18.

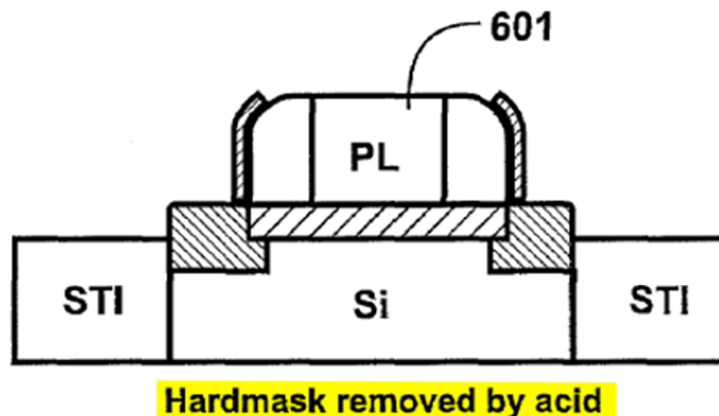


**FIGURE 6**

Ex. 1009, Fig. 6 (emphasis added).

73. The method is also described such that in step 11 of 12, the method “[s]electively *remove[s] the hard mask on patterned gate layer* while maintaining the sidewall spacers overlying the patterned gate layer.” *Id.* 4:1-3.

74. The Petition argues that “Chen discloses an embodiment that retains the cap layer,” arguing that Chen’s Figure 5 (which includes the hard mask) is a “finish[ed]... device,” which is an apparent reference to the claim requiring a “MOS transistor structure.” Pet., 80. But Figure 5 is not a “MOS transistor structure,” because it is not a transistor. As Petitioner’s expert conceded, the device in Figure 5 would not function as a transistor. Ex. 2004, 84:10-24. The Petition’s basis for its argument is that Chen states: “To finish the device according to an embodiment of the present invention, the method forms sidewall spacers 501 from the second protective layer, as illustrated by FIG. 5.” Pet., 80 (citing Ex. 1009, 6:11-18). However, this language does not indicate that Fig. 5 represents a “finished device,” as the Petition suggests. This first sentence of the paragraph introduces a number of steps in the paragraph as a whole that are required to finish the device. The specification indicates that Fig. 5 illustrates forming sidewall spacers 501, which is merely one step of “finish[ing] the device,” not that Fig. 5 illustrates a finished device. Subsequent steps for finishing the device are described in the remaining portion of the paragraph. Ex. 1009, 6:11-31. At a minimum, the inclusion of those steps is explicitly indicated because Figure 6 is a later step in the process, and in

Figure 6, the hard mask has been removed. Ex. 1009, Fig. 6. Indeed, the remainder of the paragraph states that further steps are necessarily performed after Figure 5, including: (1) “remov[ing] the hard mask to expose 601 the top surface of the gate structures, as shown in FIG. 6”; (2) “form[ing] a silicide layer overlying gate layer and source/drain regions”; (3) “form[ing] an interlayer dielectric layer overlying NMOS and PMOS transistor devices”; and (4) “perform[ing] electrical contacts.” Ex. 1009, 6:21-31. These are steps required by Chen and are not described as optional. *Id.* And a POSITA would know they are required to create a transistor as claimed. Thus, the Petition is incorrect that Chen discloses a transistor, as claimed, with a hard mask.

75. The Petition also alleges that a POSITA would have found it obvious to retain Chen’s hard mask in the final device structure. Pet., 81. Specifically, the Petition alleges that the hard mask would not be removed for two reasons: (1) “[i]n device regions where silicide is unwanted on a polysilicon gate”; or (2) if Chen’s conductive gate layer were made of metal, for the same reasons as alleged with respect to Ground 1C. Pet., 81.

76. As to the first rationale, it is purely speculative. Chen explicitly states that “[t]he method forms a silicide layer overlying gate layer” and that in order to accomplish that, it removes the hard mask. Ex. 1009, 6:15-25. There is no discussion of not siliciding the gate (whether metal or polysilicon) and no discussion

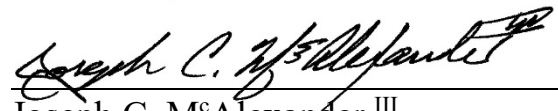
of not removing the hard mask. As to the second rationale, wherein the Petition alleges a POSITA would have found it obvious to retain Chen's hard mask for the same reasons that a POSITA would have found it obvious to retain Lan's cap layer in Ground 1C (Pet., 81-82), this fails for the same reasons as explained above with respect to Lan: (1) the proposed modification is unworkable because it would create a further problem of the hard mask blocking access to the gate conductive layer, and the Petition offers no solution for how this problem would be resolved; and (2) there are numerous reasons to remove the cap layer, as explained above regarding Lan. *Supra* §VIII.A.

77. Accordingly, Chen does not disclose or render obvious limitation [2.c] and Grounds 4A and 4B fail.

## **IX. CONCLUSION**

78. For at least the reasons discussed above, the challenged claims of the '847 patent should be found patentable.

Dated: January 9, 2026

  
Joseph C. McAlexander III