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Transcript of Eugene Fitzgerald, Ph.D.

Date: January 6, 2026

Case: Taiwan Semiconductor Manufacturing Co, et al -v- Marlin Semiconductor
Ltd (PTAB)

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR	)	
MANUFACTURING COMPANY LTD.,	)	
and APPLE INC.,	)	
	)	
Petitioners,	)	
	)	
VS.	)	Case No. IPR2025-00847
	)	Patent No. 7,745,847 B2
MARLIN SEMICONDUCTOR LTD.,	)	
	)	
Patent Owner.	)	
_____	)	

REMOTE VIDEOTAPED DEPOSITION OF
EUGENE FITZGERALD, PH.D.
TUESDAY, JANUARY 6, 2026

STENOGRAPHIC REPORTER: CHRISTA YAN, CSR NO. 14316, RPR

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21 MARCELLOUS GRANT, The Videographer

22 --oOo--

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EXHIBIT FOR IDENTIFICATION

PAGE

No Exhibits Marked.

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1 BE IT REMEMBERED that on TUESDAY, the 6TH DAY OF
2 JANUARY, 2026, at the hour of 7:32 a.m., Pacific Standard
3 Time, of said day, before me remotely, CHRISTA YAN, a
4 Certified Shorthand Reporter, State of California,
5 remotely appeared EUGENE FITZGERALD, PH.D., who was
6 examined as a witness in said cause; that said transcript
7 format was prepared in accordance with California Code of
8 Regulations Section 2473.

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1	THE TECHNICIAN: Thank you to everyone for attending	07:31:34
2	this proceeding remotely, which we anticipate will run	07:31:35
3	smoothly. Please remember to speak slowly and do your	07:31:37
4	best not to talk over one another. Please be aware that	07:31:39
5	we are recording this proceeding for backup purposes. Any	07:31:42
6	off the record discussions should be had away from the	07:31:44
7	computer.	07:31:46
8	Please remember to mute your mic for those	07:31:46
9	conversations. Please have your video enabled to help the	07:31:49
10	reporter identify who is speaking. If you're unable to	07:31:51
11	connect with video and are connecting via phone, please	07:31:53
12	identify yourself each time before speaking. And we	07:31:56
13	apologize in advance for any technical-related	07:31:58
14	interruptions. Thank you.	07:32:00
15	THE VIDEOGRAPHER: Please stand by.	07:32:01
16	Here begins Media Number 1 in the videotaped	07:32:04
17	deposition of Dr. Eugene Fitzgerald in the matter of	07:32:14
18	Taiwan Semiconductor Manufacturing Company, et al., versus	07:32:19
19	Marlin Semiconductor Limited in the United States Patent	07:32:24
20	and Trademark Office, Case Number IPR2025-00847.	07:32:30
21	Today's date is January 6, 2026. The time on the	07:32:40
22	video monitor is 7:32 a.m. The remote videographer today	07:32:45
23	is Marcellous Grant representing Planet Depos. All	07:32:53
24	parties of this video deposition are attending remotely.	07:32:56
25	Would counsel please voice identify themselves	07:32:59

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1	and state whom they represent.	07:33:00
2	MR. DOKHANCHY: Reza Dokhanchy, Mintz Levin, on behalf	07:33:03
3	of the patent owner, Marlin Semiconductor Limited.	07:33:07
4	MR. LONG: Justin Long -- (audio technical	07:33:11
5	difficulty).	07:33:18
6	THE VIDEOGRAPHER: I'm sorry. We can't hear you, sir.	07:33:18
7	THE WITNESS: It should be on. Is it? We'll see.	07:33:24
8	Could you hear that tapping?	07:33:26
9	MR. LONG: Is it...	07:33:28
10	THE WITNESS: It's solid.	07:33:30
11	MR. LONG: Can you hear me now?	07:33:32
12	THE VIDEOGRAPHER: I can hear you now, sir.	07:33:34
13	MR. LONG: Okay. My name is J. Preston Long on behalf	07:33:35
14	of petitioner Taiwan Semiconductor Company, the law firm	07:33:39
15	of Finnegan. I'm joined today by my colleague Carlos	07:33:41
16	Duarte-Guevara.	07:33:47
17	THE STENOGRAPHIC REPORTER: And, Mr. Long, I just want	07:33:50
18	to let you know I can barely hear you. You may want to	07:33:56
19	scoot closer to the mic.	07:34:01
20	THE VIDEOGRAPHER: The court reporter today is Christa	07:34:04
21	Yan representing Planet Depos. The witness will now be	07:34:06
22	sworn.	07:34:08
23	THE STENOGRAPHIC REPORTER: Okay. Mr. Fitzgerald,	
24	please raise your right hand. Do you solemnly swear or	
25	affirm to tell the truth, the whole truth, and nothing but	

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1 the truth?

2 THE WITNESS: Yes.

3 THE STENOGRAPHIC REPORTER: Thank you. Please
4 proceed.

5 EUGENE FITZGERALD, PH.D.,
6 the Witness, called on behalf of Patent Owner, being duly
7 sworn to state the truth, the whole truth, and nothing but
8 the truth, testified on oath as follows:

9 EXAMINATION 07:34:18

10 BY MR. DOKHANCHY: 07:34:18

11 Q Good morning, Dr. Fitzgerald. And do you prefer 07:34:22
12 Dr. Fitzgerald or Professor Fitzgerald? 07:34:25

13 A Either is fine. 07:34:28

14 Q Okay. Great. 07:34:30

15 We'll go with doctor since it's slightly shorter. 07:34:31

16 Have you been deposed before, Dr. Fitzgerald? 07:34:35

17 A Yes. 07:34:36

18 Q Have you done a remote deposition before? 07:34:37

19 A Once during COVID. 07:34:40

20 Q Okay. And approximately how many times have you 07:34:43
21 been deposed? 07:34:47

22 A Oh, like, six times, something like that. 07:34:48

23 Q Okay. So you're pretty familiar with the 07:34:55

24 process. I'll just lay down a couple of ground rules as 07:34:57

25 reminders. You know, I'll be asking questions. You'll be 07:35:02

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1 providing answers. Your counsel may object from time to 07:35:05
2 time. You should still answer the question regardless of 07:35:08
3 the objection unless it's a privilege objection, in which 07:35:10
4 case counsel may instruct you not to answer. But 07:35:13
5 otherwise, you should answer. 07:35:15

6 And for the court reporter's benefit, let's try 07:35:16
7 to speak slowly and not speak over each other and allow 07:35:19
8 the court reporter to hear what we're saying and take 07:35:23
9 everything down. Does that all make sense? 07:35:25

10 A Yes. 07:35:27

11 Q Is there any reason you cannot testify truthfully 07:35:28
12 and accurately today? 07:35:31

13 A No. 07:35:32

14 Q Okay. Can you tell me about your experience in 07:35:33
15 transistor fabrication? 07:35:41

16 A Wow. Okay. Sure. Let's see. In the earliest 07:35:42
17 phase, I fabricated transistors in graduate school. Then 07:35:51
18 after that, I went to AT&T Bell Laboratories. While I was 07:35:56
19 there, we fabricated many different kinds of semiconductor 07:36:02
20 devices including transistors. Those were the days of 07:36:06
21 trying new materials for various applications including an 07:36:10
22 important thing, which is -- this is -- which is they 07:36:16
23 discovered higher mobility in strained silicon. 07:36:17

24 THE STENOGRAPHIC REPORTER: I'm sorry. It's a bit 07:36:19
25 hard to hear you, Doctor. Could you scoot closer to your 07:36:22

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1	mic? You may want to try speaking up as well.	07:36:23
2	THE WITNESS: Testing, 1, 2, 3. Testing, 1, 2, 3.	07:36:36
3	Can you hear me?	07:36:40
4	THE STENOGRAPHIC REPORTER: I can hear you better now.	07:36:41
5	Thank you.	07:36:43
6	THE WITNESS: Okay. So talking like this is working,	07:36:43
7	what you hear right now?	07:36:51
8	THE STENOGRAPHIC REPORTER: Yes, thank you.	07:36:52
9	THE WITNESS: Okay.	07:36:53
10	So just to repeat part of that, at AT&T, our job	07:36:54
11	was to, you know, create new kinds of electronic	07:37:01
12	materials, see if we could make devices and if they could	07:37:03
13	be practical in different applications. So one of the	07:37:06
14	core things I was doing there was trying to use	07:37:11
15	lattice-mismatched semiconductors to create strain in	07:37:16
16	silicon and silicon-germanium. And we discovered high	07:37:20
17	electron mobility in strained silicon in those days.	07:37:27
18	And then separately, after that, I moved to MIT	07:37:32
19	where I founded a company to commercialize strained	07:37:36
20	silicon technology. And so there, we worked with many	07:37:40
21	foundries around the world, tried to implement strained	07:37:45
22	silicon, including AMD, TSMC, UMC, which are -- TSMC and	07:37:49
23	UMC are foundries. And then since then, continued with	07:37:57
24	different devices. Probably my more recent focus has been	07:38:01
25	on integrating different materials into CMOS flows so that	07:38:07

1 you could design new kinds of silicon chips with other 07:38:13
2 devices inside them. 07:38:15

3 And so with that, you know, we had many partners 07:38:18
4 around the world, and I founded a new company called New 07:38:22
5 Silicon Corporation, which is to make integrated circuits 07:38:28
6 from those kind of process and materials advantages. 07:38:29

7 THE STENOGRAPHIC REPORTER: And I'm sorry, Doctor. 07:38:38
8 You said CMOS flows? 07:38:39

9 THE WITNESS: CMOS flows. So CMOS is C-M-O-S 07:38:40
10 capitalized, flows, f-l-o-w-s. 07:38:46

11 THE STENOGRAPHIC REPORTER: Thank you. 07:38:48

12 BY MR. DOKHANCHY: 07:38:49

13 Q What sort of different materials has New Silicon 07:38:54
14 Corporation been involved in integrating into CMOS flows? 07:39:01

15 A So the goal of New Silicon is to integrate 07:39:04
16 compound semiconductor devices into silicon CMOS. So 07:39:12
17 silicon CMOS is a standard platform. The way NSC looks at 07:39:18
18 it is that it has PMOS and NMOS devices, which -- you 07:39:23
19 know, for computation, but then there are new options that 07:39:28
20 are needed for chips in the future that require different 07:39:34
21 materials. 07:39:35

22 And compound semiconductors offer -- just to give 07:39:36
23 you an example, compound semiconductors are typically 07:39:42
24 things like gallium arsenide, gallium nitride, those types 07:39:42
25 of materials. And the company has focused in the newest 07:39:48

1 products on gallium nitride devices being incorporated 07:39:52
2 into CMOS flows. You could design circuits that have NMOS 07:39:58
3 devices, PMOS devices, and then something like a GaN LED 07:40:04
4 or a GaN HEMT, which is a transistor. 07:40:13

5 Q What was the name of the first company you 07:40:20
6 mentioned? You said that after you joined MIT, you 07:40:21
7 founded a company? 07:40:23

8 A Yes. 07:40:24

9 Q I think that was -- 07:40:25

10 A AmberWave Systems. 07:40:26

11 Q Okay. So what was the product or purpose for the 07:40:30
12 creation of AmberWave Systems? 07:40:37

13 A So, yeah, it was very exciting times. The work 07:40:40
14 that we had done at Bell Labs and continued at MIT in 07:40:44
15 lattice mismatch, lattice-mismatched materials, things 07:40:49
16 that, you know, have different lattice -- semiconductors 07:40:56
17 that have a different lattice constant than silicon were 07:40:57
18 never thought to be practical, right, so the ability to 07:41:01
19 kind of now have useful devices come from them are very 07:41:05
20 exciting. 07:41:11

21 And when AmberWave started, we were looking at 07:41:11
22 both incorporating strain into CMOS devices with our 07:41:16
23 partners there -- our closest partner, like I said, in the 07:41:22
24 end, ended up being AMD and UMC. And then also, though we 07:41:24
25 did have, on our roadmap, incorporating compound 07:41:30

1 semiconductor devices. 07:41:32

2 But, of course, over time, as a start-up, you 07:41:34

3 start to focus on, and the impact of strained silicon on 07:41:36

4 the digital world, meaning compute chips, essentially CPUs 07:41:44

5 at the time, ended up being super important, and that's 07:41:47

6 when the company really zeroed in and focused on strained 07:41:51

7 silicon commercialization. 07:41:59

8 And so, initially, the products were engineered 07:42:00

9 wafers that allow foundries and fabrication facilities to 07:42:05

10 build strained silicon devices, and the model was always 07:42:14

11 to supply materials, but then also license technology. 07:42:14

12 Q And did AmberWave Systems reach a point of 07:42:25

13 actually producing commercial products? 07:42:29

14 A Yes, we were selling engineered wafers, like I 07:42:31

15 said, to our partners. And we ended up -- over time, 07:42:40

16 intellectual property became important. And then Intel 07:42:48

17 took a license, and then after that, the -- some 07:42:54

18 intellectual properties purchased by TSMC. 07:43:02

19 Q And I saw in your CV and I think also discussed 07:43:05

20 in your declaration a few other companies, Contour 07:43:23

21 Semiconductor, 4Power LLC, Paradigm Research? 07:43:28

22 A Yes. 07:43:33

23 Q That's correct? 07:43:33

24 Can you go through each of those and explain to 07:43:36

25 me what those companies produced and why they were 07:43:39

1	founded?	07:43:43
2	A Sure. Contour Semiconductor was introduced to me	07:43:43
3	by some investors and the founder of that company, and so	07:43:48
4	I joined to help them, you know, more or less, to make the	07:43:54
5	founder's ideas practical. Being from the CMOS side and	07:44:01
6	with the strained silicon activity, I immediately could	07:44:06
7	see that the founder's idea could be done in silicon with	07:44:12
8	silicon process technologies, and the goal was low cost	07:44:17
9	memory.	07:44:18
10	And the design for low cost memory involved only	07:44:19
11	diodes. It's an old idea that's been out there for a	07:44:28
12	while, but the founder had some ideas about how to build	07:44:32
13	that in the fewest numbers of mask levels. And so that is	07:44:35
14	what we were doing in that company.	07:44:42
15	THE STENOGRAPHIC REPORTER: I'm sorry. You said mask	07:44:44
16	levels?	07:44:47
17	THE WITNESS: Yeah, mask levels, which is proportional	07:44:47
18	to cost. So basically building memory with very few mask	07:44:51
19	levels and changing the way that the industry does low	07:44:53
20	cost memory. When I say low cost, I don't mean	07:44:59
21	leading-edge memory. I meant low cost in the sense of	07:45:03
22	very, very cheap memory that is not on the leading-edge.	07:45:06
23	So that's what that company was about.	07:45:09
24	4Power was a company that -- or still is a	07:45:13
25	company, actually, but I founded with Steve Ringel from	07:45:16

1 Ohio State University, and we -- Steve had a long history 07:45:21
2 of working in solar. And so we ended up founding that 07:45:25
3 company, and the goal there is high efficiency solar cells 07:45:32
4 built on a silicon/III-V platform, so again the compound 07:45:41
5 semiconductor on silicon. 07:45:47

6 So we were both to build a -- we were able to 07:45:49
7 build a dual junction, high efficiency cell that was of 07:45:52
8 interest. Now, we never went down the path of commercial 07:46:00
9 solar because commercial solar is extremely low cost. If 07:46:04
10 you look at where compound semiconductor devices had 07:46:08
11 markets, they're in space. And at this time, they were -- 07:46:14
12 there was a lot of interest in high-altitude aircraft 07:46:20
13 being powered by this kind of solar. And so 4Power, we 07:46:24
14 had many government contracts to work on on the solar 07:46:32
15 cells, so that's -- that's what we did in that company. 07:46:35

16 Paradigm Research is -- you could think of it as 07:46:39
17 sort of my catch-all company. At the beginning. I used 07:46:44
18 it to create a program with Raytheon to help them head 07:46:49
19 down this path of integrating compound semiconductors into 07:46:57
20 silicon, and that was largely funded by DARPA. And then 07:47:00
21 after that, I used it for different projects, basically. 07:47:07
22 So you could think of it as my own personal consulting 07:47:12
23 umbrella company. 07:47:16

24 BY MR. DOKHANCHY: 07:47:18

25 Q What types of projects are you referring to after 07:47:20

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1 the Raytheon engagement? 07:47:24

2 A Many different kinds. I mean, it became an 07:47:31
3 umbrella for my innovation work, so, obviously, with all 07:47:34
4 these things going on, we had a good model for 07:47:37
5 understanding innovation, which is sort of research to 07:47:40
6 market, so the -- I started capturing that in different 07:47:42
7 ways and helping companies, so I earned some consulting 07:47:50
8 money for helping them with innovation. 07:47:54

9 And then also, I worked with the Kauffman 07:47:57
10 Foundation, which is the entrepreneurship foundation, with 07:48:03
11 the United States. I did expert witness work, which I do 07:48:07
12 out of Paradigm. And I had licensed technology from MIT 07:48:12
13 in Paradigm in order to keep that invested. And then 07:48:22
14 eventually, that, you know, intellectual property, I 07:48:28
15 licensed into New Silicon Corporation at the very 07:48:32
16 beginning of that company. 07:48:36

17 Q In your work with or through Paradigm Research 07:48:37
18 today, are you involved in any active research or 07:48:49
19 consulting work other than your expert witness work? 07:48:53

20 A No. It's pretty much, right now, just 07:48:59
21 consulting. 07:49:05

22 Q And more broadly, are you involved with any of 07:49:08
23 the companies that you mentioned, any ongoing research or 07:49:12
24 consulting capacity beyond expert witness work? 07:49:17

25 A Define that a little more -- more resolved. 07:49:19

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1 Q Sure. So you went through a number of companies. 07:49:28
2 I'm just not sure if they're operational anymore. That's 07:49:31
3 kind of my question. 07:49:34
4 A Okay. Let's see. Well 4Power and Paradigm are 07:49:35
5 still in existence. Let's see. AmberWave, like I said, 07:49:41
6 was mostly sold, TSMC and Micron. Let's see. Contour was 07:49:47
7 eventually, after -- I had left working with them, and so 07:49:57
8 I'm not as clear what happened. But eventually, I think 07:50:02
9 they were bought by a company, a foreign company. 07:50:05
10 And then let's see. Anything else I forgot. 07:50:09
11 Let's see. I think that's it. Right? Oh, no, 4Power -- 07:50:15
12 no, I said 4Power is still there. Yes. But, yeah, most 07:50:17
13 of my research now was in MIT, and then we spun that out 07:50:21
14 into NSC. So most of my activity outside of MIT is 07:50:29
15 working with NSC. I'm chairman of NSC. 07:50:36
16 Q So you're still involved with NSC, and that's 07:50:46
17 still an ongoing engineering tech company; is that 07:50:49
18 correct? 07:50:51
19 A Correct. Correct. 07:50:51
20 Q Okay. And you mentioned that with Contour 07:50:52
21 Semiconductor, one of the goals was to minimize the number 07:51:00
22 of mask layers. Did I have that right? 07:51:04
23 A That is correct. 07:51:07
24 Q Why was that a goal or why is that desirable in 07:51:08
25 general? 07:51:13

1 A So the key to CMOS processing economically is 07:51:13
2 that you could build complex devices with a number of mask 07:51:16
3 levels, and you can build in great complexity. So in 07:51:23
4 general, you have a silicon substrate, which is a cost, 07:51:29
5 and then you have -- you have the processing cost, which 07:51:32
6 when you print patterns on a wafer, each one of those 07:51:35
7 patterns you have to make with a mask. 07:51:39

8 And so what happens to silicon is by the time you 07:51:42
9 do all these mask levels, the processing cost dominates 07:51:46
10 the cost of the final chip because, of course, you could 07:51:53
11 build these fantastic different kinds of integrated 07:51:55
12 circuits in the same platform. Turns out that because of 07:51:58
13 the number of mask levels, the cost of the chip, in the 07:52:00
14 end, is proportional to the number of mask levels. The 07:52:03
15 silicon substrate, comparatively speaking, is quite low 07:52:06
16 compared to that. 07:52:10

17 So if you're -- if, like the founder of that 07:52:12
18 company was saying, well, I have this idea about diode 07:52:22
19 memory, diodes are simpler, and I imagine a process where 07:52:25
20 I can only have four mask levels instead of 30 to make 07:52:27
21 memory, and so now, the -- because it's proportional to 07:52:33
22 the number of mask levels, you know, the -- obviously, 07:52:39
23 four is less than 30. 07:52:40

24 And so that was the purpose -- was to build 07:52:42
25 memory in the silicon-based process in the end. That was 07:52:47

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1 my contribution, that would only use four, maybe five mask 07:52:53
2 levels. 07:52:57
3 Q Okay. And can we distribute or -- no. Let's 07:52:58
4 see. Can you access that link in the chat, 07:53:11
5 Dr. Fitzgerald, that says Exhibit 010626? 07:53:13
6 A Okay. In the chat. Okay. 07:53:25
7 THE TECHNICIAN: And, Counsel, this is the tech. In 07:53:26
8 that exhibit link, it's just going to be a test link 07:53:27
9 currently, so just let me know what document you'd like me 07:53:32
10 to drag into that. I can -- 07:53:33
11 MR. DOKHANCHY: Yeah. Can you put Exhibit 1001, which 07:53:34
12 is the '847 patent in that link? 07:53:37
13 THE TECHNICIAN: Please stand by. 07:53:42
14 BY MR. DOKHANCHY: 07:53:47
15 Q And let me ask, Dr. Fitzgerald, do you have any 07:53:47
16 paper documents in front of you? 07:53:49
17 A Yes. 07:53:50
18 Q What do you have? 07:53:50
19 A On my right side, I have my declaration in paper 07:53:51
20 form. And then on my left side, I have all the exhibits 07:54:00
21 that are referenced there. 07:54:04
22 Q Okay. Are there any annotations or markings on 07:54:07
23 any of those documents? 07:54:12
24 A No. 07:54:13
25 Q Maybe we can just do this with the documents you 07:54:13

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1	have rather than dealing with virtual exhibits. That	07:54:19
2	should simplify things.	07:54:22
3	A Okay.	07:54:23
4	Q Do you have Exhibit 1001, the '847 patent?	07:54:23
5	A Yes.	07:54:27
6	THE STENOGRAPHIC REPORTER: And I'm sorry, Counsel.	07:54:29
7	Are you marking this as Exhibit 1?	07:54:29
8	MR. DOKHANCHY: It's already marked.	07:54:29
9	THE STENOGRAPHIC REPORTER: Okay. So it'll be shown	07:54:29
10	in the transcript as Exhibit 1001?	07:54:29
11	MR. DOKHANCHY: Correct.	07:54:29
12	THE STENOGRAPHIC REPORTER: Okay. Same as the file	07:54:42
13	name, correct?	07:54:42
14	MR. DOKHANCHY: I think that is in the file name. The	07:54:43
15	file name is lengthier than the digital copies that you	07:54:47
16	have, but, yes, it includes 1001. This IPR proceeding has	07:54:50
17	a number of premarked exhibits.	07:54:55
18	THE STENOGRAPHIC REPORTER: Thank you. Okay. So this	07:54:56
19	is premarked. I'm sorry. I just needed clarification on	07:55:05
20	that.	07:55:10
21	MR. DOKHANCHY: Yes. And it looks like Kylan has put	07:55:10
22	that in the chat as well.	07:55:17
23	BY MR. DOKHANCHY:	07:55:20
24	Q Okay. Dr. Fitzgerald, if you could turn to the	07:55:27
25	claims of the '847 patent, which are on page 19 of 19 in	07:55:31

1	Exhibit 1001. Let me know when you're there.	07:55:37
2	A I am there.	07:55:41
3	Q Okay. And you see there's Claim 1, which, in	07:55:44
4	your declaration, you allege is invalidated by a number of	07:55:53
5	prior art references and combinations of prior art	07:55:58
6	references in your declaration; is that right?	07:56:02
7	A Say that again.	07:56:04
8	Q You see a Claim 1?	07:56:08
9	A Yes, I see Claim 1. Yes.	07:56:10
10	Q And you allege that Claim 1 is invalidated by a	07:56:12
11	number of prior art references and combinations thereof in	07:56:18
12	your declaration, right?	07:56:21
13	A Yes, that's correct.	07:56:22
14	Q And then you see a Claim 2 that says -- I'll just	07:56:22
15	read it in for the record. The structure of Claim 1,	07:56:29
16	wherein the gate further comprises: a dielectric layer; a	07:56:32
17	conductive layer, positioned in the dielectric -- excuse	07:56:39
18	me -- on the dielectric layer; and a cap layer, positioned	07:56:41
19	on the conductive layer.	07:56:46
20	Do you see that?	07:56:48
21	A Yes.	07:56:48
22	Q And you argue in your declaration that that claim	07:56:48
23	is invalidated by a number of obviousness grounds. Do you	07:56:57
24	recall that?	07:57:04
25	A Yes.	07:57:04

Transcript of Eugene Fitzgerald, Ph.D.
Conducted on January 6, 2026

21

1 MR. LONG: Objection; mischaracterizes. 07:57:06
2 BY MR. DOKHANCHY: 07:57:08
3 Q And do you recall that the grounds you assert 07:57:10
4 against Claim 2 are Grounds 1C, 1D, and 4B; is that 07:57:13
5 correct? 07:57:29
6 THE STENOGRAPHIC REPORTER: You said 4B as in boy, 07:57:29
7 correct, Counsel? 07:57:34
8 MR. DOKHANCHY: Yes. 07:57:34
9 BY MR. DOKHANCHY: 07:57:48
10 Q I can point you to page 39 of your declaration if 07:57:48
11 that's helpful. 07:57:51
12 A Yes, there's a table there that talks about the 07:58:18
13 claims that's -- that are challenged and the reference 07:58:28
14 doing so on the ground labels that are on the far left. 07:58:33
15 Q Great. And your contention is that Claim 2 is 07:58:35
16 invalidated by Grounds 1C, 1D, and Ground 4, correct? 07:58:41
17 A Yeah, so 1C, 1D is Claim 2 challenge, right, and 07:58:47
18 then 4A and 4B. Yes. 07:59:12
19 Q Okay. If you could turn back to the patent and 07:59:13
20 look at the claim language, you'll see, as I read, that 07:59:24
21 the claim requires a cap layer positioned on the 07:59:26
22 conductive layer. Do you see that? 07:59:34
23 A Yes. 07:59:36
24 Q When you were providing your opinions in this 07:59:38
25 case about invalidity, what meaning or understanding of 07:59:42

1 cap layer were you applying? 07:59:47

2 A In the meaning of '847, the way that they 07:59:49

3 describe cap layer in the -- in the specification -- 07:59:57

4 Q Which is what? 07:59:59

5 A -- in the figures. So as an example, I mean, 08:00:01

6 just if you look at Figure 14, 313 is the cap layer and -- 08:00:13

7 in the '847. 08:00:23

8 Q Right. What I'm trying to understand is what 08:00:24

9 meaning were you using? What definition of cap layer did 08:00:32

10 you apply? 08:00:38

11 A Well, the one that's defined in the patent. 08:00:38

12 Q And can you put in words what that definition is? 08:00:43

13 A Well, I mean, if I use this as an example, in 08:00:48

14 '847, 313 is a cap layer on the conductive gate 312, so 08:00:52

15 it's part of the gate stack that is being made in the 08:00:59

16 '847. 08:01:04

17 Q Okay. So your definition of cap layer is 08:01:04

18 anything part of the gate stack? 08:01:11

19 A No, it's what I said. '847 defines the gate 08:01:14

20 stack as having these three components, and 313 is the top 08:01:18

21 one of the gate stack. 08:01:22

22 Q I understand. But looking at the claim language, 08:01:23

23 it uses the word cap layer. So what's the definition of 08:01:27

24 cap layer? 08:01:30

25 A It's as I said. It's described -- I mean, if you 08:01:31

1 read in the specification -- let's see. If I go back 08:01:37
2 earlier... 08:01:44
3 So reading in Column 3 of the '847 at the top, it 08:02:09
4 describes the cap layer 213 positioned on a conductive 08:02:13
5 layer 212. 08:02:19
6 Q Right. That says where the cap layer is. What 08:02:25
7 I'm asking you is what is a cap layer? 08:02:28
8 A The cap layer 213 comprises dielectric materials 08:02:30
9 such as silicon nitride. 08:02:47
10 Q Okay. One of the concepts you describe in your 08:02:52
11 declaration is the concept of a self-aligned silicide, 08:02:57
12 sometimes called a salicide; is that right? 08:03:05
13 A Correct. 08:03:09
14 Q What is a silicide? 08:03:10
15 A The silicide is a compound that's created between 08:03:14
16 a metal reaction in the silicon. 08:03:17
17 Q And the way you describe it in your declaration 08:03:21
18 is that a metal layer is deposited on top of silicon and 08:03:23
19 diffused by a heat process into the silicon; is that 08:03:29
20 right? 08:03:34
21 A Well, you deposit metal on silicon, and then you 08:03:34
22 have to have compound formation. One way to do compound 08:03:38
23 formation is to use thermal, so you heat it. And then you 08:03:45
24 have diffusion reaction of metal into the -- yeah, the way 08:03:50
25 metal atoms go into the silicon is through diffusion, and 08:03:57

1 And so the thermal part is what I've already 08:05:56
2 mentioned for forming silicide, which is atoms move and 08:05:59
3 react. 08:06:06
4 Q Okay. Are there any other methods for diffusing 08:06:06
5 metal into the silicon besides heat and lasers for a 08:06:09
6 silicide process that you're aware of? 08:06:13
7 A I haven't really looked into that for this. I've 08:06:15
8 been mostly studying, you know, the '847 and the exhibits 08:06:22
9 here for this particular case, so I really can't say. 08:06:26
10 Q Okay. What types of metal are used in the 08:06:30
11 silicide process commonly? 08:06:38
12 A It depends on the -- on the time period in which 08:06:40
13 CMOS fabrication's occurring. In terms of research, 08:06:48
14 people have used all sorts of metals and silicides to look 08:06:51
15 at. 08:06:56
16 Q Okay. At the time of the '847 patent, which -- 08:06:56
17 let's establish that date. 08:07:10
18 So are you familiar with the state of the art in 08:07:11
19 this area around August 2007? 08:07:19
20 A Yes. 08:07:22
21 Q So around that time, what metals were used in 08:07:27
22 silicide processes for gates? 08:07:36
23 A In high volume silicon manufacturing? 08:07:41
24 Q Let's say broadly, but we can start with that. 08:07:43
25 A So the time sequence of silicides in 08:07:47

1 manufacturing are sort of titanium, cobalt, and then 08:07:52
2 nickel silicide. So the earlier technologies used 08:08:01
3 titanium. Then as scaling went ahead and, you know, 08:08:06
4 Moore's Law increasing transistor density with time, the 08:08:10
5 cobalt was used. So cobalt silicide. And then after a 08:08:14
6 few generations then nickel silicide became attractive. 08:08:22
7 And then in things like the '847, nickel's 08:08:28
8 especially attractive because it makes a better silicide 08:08:33
9 at low temperature with silicon-germanium. 08:08:37
10 Q Okay. So titanium, cobalt, nickel. What others, 08:08:48
11 if any? 08:08:52
12 A In manufacturing, I mean, there's been, I mean, 08:08:53
13 many different things. I mean, I... I guess I'd have to 08:08:57
14 understand what area you're talking about. People have 08:09:03
15 done moly, people have done ruthenium. There's all sorts 08:09:06
16 of things people have done. 08:09:14
17 Q Have you ever seen tungsten used? 08:09:15
18 A Yeah, tungsten for sure. 08:09:21
19 Q And in your declaration, you discuss the reason 08:09:23
20 to perform this metal diffusion on the gate is to improve 08:09:35
21 the electrical properties of the gate; is that correct? 08:09:39
22 A You know, specifically, the reason people 08:09:41
23 silicide a gate is when the underlying silicon poly is not 08:09:51
24 conductive enough for the application -- 08:09:54
25 THE STENOGRAPHIC REPORTER: Sorry. Sorry. 08:09:54

Transcript of Eugene Fitzgerald, Ph.D.
Conducted on January 6, 2026

27

1	Dr. Fitzgerald, you're speaking quite fast.	08:09:54
2	THE WITNESS: Okay.	08:09:54
3	THE STENOGRAPHIC REPORTER: If you could slow down.	08:10:00
4	I'm just not familiar with these terms. Thank you.	08:10:03
5	THE WITNESS: Okay.	08:10:03
6	So siliciding is used typically in the gate when	08:10:03
7	the application requires very low resistance and the	08:10:10
8	polysilicon is not conductive enough on its own. And so	08:10:21
9	therefore, by making a silicide, as it's a metal, the	08:10:28
10	resistance in the gate is lower.	08:10:37
11	BY MR. DOKHANCHY:	08:10:41
12	Q Are there any other properties besides	08:10:44
13	resistivity that are improved when siliciding a gate?	08:10:48
14	A I mean, in the context that we're doing here, I	08:10:56
15	think that it's -- it's -- CMOS is mostly for	08:11:01
16	connectivity. That's why people employed it.	08:11:07
17	Q What about when you eventually need to create a	08:11:11
18	contact with the gate, you would have to do that, right?	08:11:13
19	A Sure. Yes. So another benefit of course is that	08:11:16
20	if I were to make contact, I have to think about barriers	08:11:22
21	between whatever I'm making contact to. And thinking	08:11:28
22	about as electrons or holes flow from there, through the	08:11:33
23	device, I have to look at every interface and see if	08:11:38
24	there's any barriers to the electron or hole flow. And --	08:11:41
25	and one of the barriers can be that if the silicon,	08:11:52

1 polysilicon is not doped high enough, then you could have 08:11:57
2 a barrier there which you create some resistance. 08:12:04
3 Of course, if you dope silicon high enough, you 08:12:04
4 can make -- 08:12:07
5 THE STENOGRAPHIC REPORTER: I'm sorry. If you what 08:12:07
6 silicon high enough? 08:12:10
7 THE WITNESS: Oh, sorry. Dope, d-o-p-e. 08:12:10
8 If you dope polysilicon with a high enough 08:12:14
9 density of dopant, you can not have a barrier there. But 08:12:17
10 if I keep the poly lower doped, then when I create metal, 08:12:22
11 it improves connectivity of the gate, but it also 08:12:30
12 decreases the barrier between another metal and the poly. 08:12:37
13 So it lowers contact resistance. 08:12:45
14 BY MR. DOKHANCHY: 08:12:47
15 Q And contact resistance is also something that can 08:12:53
16 exist at the junction between two metals; is that right? 08:12:57
17 A There is a work function in metals, and you can 08:13:00
18 have a variety of things at the interface that can affect 08:13:08
19 that. So usually, those barriers are pretty, pretty low. 08:13:14
20 Q When -- when the gate is metal, what sorts of 08:13:22
21 metals were used in the 2007 time frame? 08:13:32
22 A Say this again -- which metal are you talking 08:13:36
23 about? I got silicide. And you're asking what metals go 08:13:43
24 on top of that? 08:13:45
25 Q No. So moving to a different concept. So not 08:13:46

1 when the gate is polysilicon, but rather when the gate is 08:13:49
2 metal. 08:13:52
3 A Oh, okay. 08:13:52
4 Q What sorts of metals are used for the gate? 08:13:54
5 A So early on for a while in this time period when 08:13:57
6 you went to metal gate, there's a variety of things that 08:14:03
7 people used. So the dominate ones are things like 08:14:06
8 titanium nitride. 08:14:11
9 Q Okay. What others? 08:14:13
10 A I think on the P, there's titanium aluminum 08:14:14
11 nitride. So a better work function, to your point before. 08:14:23
12 You know, you could have a better access -- a lower access 08:14:30
13 resistance. But -- but I -- I'd have to review. I mean, 08:14:32
14 obviously in these patents for this case, metal gates were 08:14:36
15 coming in. And the patents allow option for metal gate. 08:14:42
16 But, you know, that field at this time is still evolving 08:14:50
17 rapidly, so there's many things people are trying. 08:14:56
18 But as I said, you know, when you look at the 08:14:58
19 early days, titanium nitride was one that, at least in 08:14:59
20 high volume manufacturing, was used quite a bit in the 08:15:06
21 early days of implementation. 08:15:08
22 Q You have an opinion that the Lan reference can 08:15:10
23 use a metal gate, or a gate for the conductive layer, in 08:15:23
24 the Lan reference. 08:15:28
25 A Lan has that option, yes. 08:15:30

1 Q What types of metals are used in the gate in the 08:15:32
2 Lan reference? 08:15:37

3 A I'd have to look up where -- whether it gives 08:15:42
4 examples or not in -- do you want me to do that? 08:15:45

5 Q Yes, please. 08:15:48

6 A So on Lan, column 5, at line 60, it -- you know, 08:16:10
7 and a little before -- it says, The gate is not limited by 08:16:32
8 the above polysilicon, and it can -- it also can be made 08:16:35
9 by dummy gate or any conductive material, such as metal. 08:16:39

10 And it doesn't give any examples of -- of a 08:16:47
11 metal. 08:16:50

12 Q Given what you know about the industry at this 08:16:53
13 time frame, what metals do you think would have been used 08:17:00
14 in the Lan reference? 08:17:04

15 A Like I said there was a lot of experiments at the 08:17:09
16 time. And -- and I think the reason they probably don't 08:17:11
17 specify is that they know that there's many possibilities. 08:17:14
18 I mean, from a work function point of view, titanium 08:17:24
19 nitride was definitely a lead, right? 08:17:27

20 Q You've mentioned a few compounds -- or I don't 08:17:30
21 know if compounds is the right word -- but titanium 08:17:55
22 nitride, titanium aluminum nitride; is that right? 08:17:57

23 A Correct. 08:18:00

24 Q Are there any instances where a -- a single metal 08:18:01
25 would have been used, such as just titanium or just 08:18:09

1 aluminum, for the gate metal? 08:18:13

2 A Aluminum was dropped a while back because of 08:18:15

3 temperature constraints and reliability. Refractory 08:18:23

4 metals were experimented with quite a bit. So... 08:18:29

5 certainly things like tungsten, titanium, tantalum, these 08:18:32

6 were all things that people were employing to see if they 08:18:39

7 would be possible gate -- gate metals. 08:18:42

8 Q Okay. So it might be the case that the gate 08:18:50

9 metal was just a given elementary metal, right? 08:18:53

10 A I mean, the -- it -- the Lan reference just 08:18:59

11 leaves it as a metal, which means it could be any metal. 08:19:05

12 Q Is the -- withdrawn. 08:19:07

13 In general, was the contact metal the same as the 08:19:15

14 gate metal? 08:19:22

15 A What... which contact are you talking about? 08:19:24

16 Q So ultimately, for the transistor to be 08:19:31

17 operational, you need to contact the gate to apply a 08:19:34

18 voltage to it, right? 08:19:37

19 A Correct. 08:19:38

20 Q The metal used for that contact, was it typically 08:19:39

21 the same metal as the gate metal or a different metal? 08:19:42

22 A It doesn't have to be the same. 08:19:45

23 Q Would there be any reasons to use the same metal 08:19:50

24 and any reasons to use a different metal? 08:19:56

25 A Could be. I -- I haven't really ventured outside 08:19:58

1 the possibilities described in these patents. And these, 08:20:04
2 you know, the structures in '847 and Lan and Chen are 08:20:12
3 MOSFET structures. 08:20:35

4 THE STENOGRAPHIC REPORTER: I'm sorry. Are -- you 08:20:35
5 said are what structures? 08:20:40

6 THE WITNESS: MOS -- well, I said MOSFET, or MOS, 08:20:40
7 structures. It's M-O-S or M-O-S-F-E-T, capitalized, 08:20:40
8 structures. 08:20:40

9 So they're not working integrated circuits. So 08:20:41
10 as you -- as you point out, other things happen after the 08:20:48
11 embodiments, you know. And, you know, as I've argued, the 08:20:53
12 '847, Lan, and Chen are the same embodiments, right? You 08:20:58
13 know, and that they have things happen afterwards in order 08:21:03
14 to build circuits, like you're describing, where you have 08:21:07
15 to have contacts come down and metallization and 08:21:12
16 interconnects in order to make real circuits. 08:21:17

17 But they don't -- in these three patents, they 08:21:19
18 don't describe a lot or anything about the interconnect 08:21:27
19 structure. 08:21:30

20 BY MR. DOKHANCHY: 08:21:30

21 Q Okay. And those are steps that you would have to 08:21:30
22 take to finalize the transistor; is that right? 08:21:35

23 A Those are steps you would have to do to finalize 08:21:38
24 the working transistor in a circuit. 08:21:42

25 Q Would there be any benefit to adding a diffusion 08:21:44

1 step if the gate were metal; for example, laying down an 08:21:55
2 additional type of metal and diffusing it into the gate 08:21:59
3 metal? 08:22:02

4 A I haven't really looked into that. None of these 08:22:03
5 patents describe that. I mean, in general, diffusion, as 08:22:08
6 you go ahead and process technology, you want to limit 08:22:13
7 that, because you're trying to create an electrostatic 08:22:17
8 design inside the transistor. So, you know, I can't say 08:22:25
9 much more than that, because I'd have to look at the 08:22:27
10 specific details you're talking about. 08:22:30

11 Q If you were to add a metal diffusion onto a metal 08:22:39
12 gate, could that improve properties such as contact 08:22:43
13 resistance between the metal contact and the gate? 08:22:46

14 MR. LONG: Objection; incomplete hypothetical. 08:22:56

15 THE STENOGRAPHIC REPORTER: And I'm sorry. I'm sorry. 08:22:59
16 Was that objection by Mr. Long? 08:23:00

17 MR. LONG: Yeah, sorry. 08:23:03

18 Objection; incomplete hypothetical. 08:23:04

19 THE STENOGRAPHIC REPORTER: Thank you. 08:23:05

20 THE WITNESS: I mean, I -- again, you know, it's like 08:23:07
21 infinite number of things because, you know, you have to 08:23:14
22 talk about exactly... but, you know, if you look at the 08:23:17
23 way things are typically done, layers are -- are also put 08:23:20
24 in there. Like if you make an interconnect, you have 08:23:25
25 liners inside, and they -- they go inside. 08:23:28

1 And so those are all designed to help the 08:23:31
2 connectivity between the interconnects and contacts on top 08:23:34
3 of the device. 08:23:39

4 THE STENOGRAPHIC REPORTER: You're saying 08:23:43
5 connectivity, correct? 08:23:49

6 THE WITNESS: Interconnects and interconnectivity. 08:23:50
7 BY MR. DOKHANCHY: 08:23:52

8 Q Sorry, what sorts of liners are you talking 08:23:56
9 about? 08:23:59

10 A So in a -- when you're trying to interconnect 08:23:59
11 transistors and you bring down metal, usually there's not 08:24:06
12 just the metal itself. You have a liner that is around 08:24:09
13 those contacts. And that liner also helps with the 08:24:16
14 connectivity between the interconnects and the -- whatever 08:24:20
15 the interconnect metals are and the -- and the underlying 08:24:24
16 contact. 08:24:28

17 Q What is that liner made out of? 08:24:28

18 A Changes with time, with different technologies. 08:24:33

19 Q What sorts of materials have you seen the liner 08:24:36
20 being made out of? 08:24:43

21 A Can't recall. But I think if I recall, there 08:24:43
22 might be... in the -- in the tungsten case, I think it was 08:24:50
23 titanium nitride. 08:24:57

24 Q So going back to my question, if you were to 08:25:02
25 diffuse a metal onto a metal gate before connecting the 08:25:08

1 contact, could that improve the contact resistance that 08:25:13
2 would otherwise exist between the contact and the metal 08:25:17
3 gate? 08:25:21

4 MR. LONG: Objection; incomplete hypothetical. 08:25:22

5 THE WITNESS: So I -- I -- I -- you know, it depends. 08:25:23
6 I mean, if you have a clean interface, you -- you don't 08:25:34
7 want any, you know, because it would add thermal budget, 08:25:37
8 right? If you have a -- 08:25:41

9 THE STENOGRAPHIC REPORTER: Because it -- I'm sorry. 08:25:41
10 I can't hear you. Because it would what budget? I can't 08:25:44
11 hear you. 08:25:45

12 THE WITNESS: If you have a clean interface and you 08:25:45
13 have metal-metal, you would want to not have any thermal 08:25:50
14 processing because it would add to the thermal budget of 08:25:55
15 the entire process. So in general, people are trying to 08:25:59
16 avoid that. 08:26:03

17 In the early days, like, you know, if you were in 08:26:05
18 a research lab, there's all sorts of contamination and 08:26:09
19 things like that, and it's very different from 08:26:11
20 manufacturing. Manufacturing tries to remove all that 08:26:13
21 over time to reduce mask levels and to keep thermal budget 08:26:15
22 low. 08:26:20

23 But of course, if you have a problem there, then 08:26:20
24 people might do things like that. 08:26:23
25

1 BY MR. DOKHANCHY: 08:26:24

2 Q So if the interface between the contact and the 08:26:27

3 metal gate were not as clean as you'd like, the metal gate 08:26:30

4 could benefit from a metal diffusion to improve contact 08:26:35

5 resistance between the metal contact and the gate; is that 08:26:38

6 fair? 08:26:42

7 A I would say that I would have to look at the 08:26:42

8 exact situation. Because again, I try to -- I try to not 08:26:47

9 have to do that. And oftentimes, if it's a dielectric 08:26:51

10 material problem there, then annealing won't help. 08:27:07

11 Because, you know, oftentimes -- again, it all depends on 08:27:10

12 the material -- it might not help. 08:27:15

13 Q So it might help or it might not help; is that 08:27:16

14 right? 08:27:18

15 A Correct. Correct. 08:27:18

16 Q What about the concept of adhesion or mission, is 08:27:19

17 that a term you're familiar with? 08:27:29

18 A Adhesion, yes. 08:27:30

19 Q And maybe I'm getting the technical terminology 08:27:31

20 wrong. Is the concept of miscibility related to that 08:27:36

21 concept of adhesion? 08:27:42

22 A Okay. So this is, like, way, way off set, but 08:27:43

23 yes. In material science, miscibility deals with -- with 08:27:48

24 phase diagrams, which are thermodynamics between two 08:27:54

25 different materials. I can -- I can give you a whole 08:27:59

1 lecture on that. But I think, you know, what we're doing 08:28:02
2 here, I'm not sure how that is relevant to anything we're 08:28:06
3 discussing here today. 08:28:17

4 Q If you have a metal gate and a metal contact, 08:28:17
5 would it improve the adhesion or the miscibility of those 08:28:26
6 two components if you were to diffuse a metal onto the 08:28:31
7 gate before that contact is made? 08:28:37

8 A Again, these things are all really dependent on 08:28:39
9 many factors. And I'd have to see a very specific thing 08:28:46
10 and, you know, I... I just... I have context of the '847 08:28:49
11 and all these other things. But... I don't want to 08:28:57
12 speculate. I'm under oath, and I'm just trying to be as 08:29:00
13 accurate as possible. 08:29:04

14 Q Okay. So you can't say one way or another. It 08:29:05
15 might improve the adhesion in some cases, or it might not 08:29:11
16 other cases; is that right? 08:29:16

17 A I would need to look at details. 08:29:17

18 Q Okay. Can you imagine or think of a type of 08:29:20
19 metal contact and a type of metal gate that would 08:29:37
20 experience improved adhesion if the metal gate were to 08:29:42
21 have a diffusion of a metal performed on it before the 08:29:48
22 connection is made? 08:29:52

23 MR. LONG: Objection; incomplete hypothetical. 08:29:55

24 THE WITNESS: Could you point to me somewhere in these 08:29:56
25 cases how -- this metal-metal interface that you're 08:30:03

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1	describing?	08:30:08
2	BY MR. DOKHANCHY:	08:30:09
3	Q I'm just asking you the question as a professor	08:30:09
4	in this field and an expert in this case.	08:30:11
5	A Yeah, I'm -- I'm here to discuss my declaration	08:30:14
6	and what's in these materials here. That's what I'm	08:30:19
7	prepared for. I'm not prepared for any hypotheticals.	08:30:21
8	Q So you're unable to answer the question as a	08:30:24
9	person with decades of experience in this field; is that	08:30:28
10	correct, Mr. Fitzgerald?	08:30:32
11	A I need lots of information and time to look at --	08:30:34
12	at what we're talking about.	08:30:37
13	Q Okay. So sitting here today, you can't answer if	08:30:38
14	there is a type of metal contact and a type of metal gate	08:30:43
15	that would experience improved adhesion if the metal gate	08:30:49
16	were to have a metal layer diffused on it prior to	08:30:53
17	contact; is that correct?	08:30:57
18	A I could speculate on many things.	08:30:57
19	Q Okay. Please answer that question then.	08:31:02
20	A I mean, there -- there are cases where, of	08:31:05
21	course, I engineer things for that, and there's other	08:31:09
22	cases where I don't.	08:31:13
23	Q Okay. Are you able to answer my question?	08:31:14
24	A Again, I go back to the same thing. I'd like to	08:31:18
25	see -- have time and lots of information about what we're	08:31:25

1 talking about. 08:31:28

2 Q What more information do you need? 08:31:29

3 A Lots of data about what the metals are, what's 08:31:34

4 thermal budget, what -- are we doing a CMOS process? Is 08:31:42

5 this compound semiconductor? Are we -- you know, what are 08:31:45

6 we doing, right? 08:31:47

7 Q Sure. So in a CMOS process, can you think of a 08:31:48

8 type of metal contact and a type of metal gate that would 08:31:56

9 have been used in the time frame of the '847 patent 08:32:00

10 wherein the adhesion between those two things would be 08:32:06

11 improved if there were metal diffusion done beforehand on 08:32:10

12 the metal gate? 08:32:15

13 A I don't know. 08:32:17

14 Q And why don't you know? 08:32:20

15 A It's an open-ended hypothetical. 08:32:34

16 Q So as a professor in this field, and someone with 08:32:39

17 a lot of experience in material science, you can't think 08:32:56

18 of two metals that would experience an improvement in 08:33:00

19 adhesion if a metal diffusion were done on one of them 08:33:05

20 beforehand; is that your testimony? 08:33:09

21 A My testimony is that I'm here today to talk about 08:33:10

22 this declaration and anything related to it. And I would 08:33:14

23 love to meet you at MIT and we could go through many, many 08:33:20

24 different kinds of things. We could discuss the details, 08:33:24

25 what you have there, and I hopefully can help you. But 08:33:27

1 right now, it's hard for me to say. 08:33:32

2 Q Would a titanium nitride gate experience better 08:33:33

3 adhesion with a contact made of any material -- excuse 08:34:02

4 me -- any metal, if it were to be diffused beforehand with 08:34:22

5 that same metal? 08:34:30

6 A I -- I didn't understand what you just said. 08:34:35

7 Q So let's say you have a titanium nitride gate, 08:34:38

8 right? Okay. And you're going to use a contact that's 08:34:42

9 made of metal, right? Could you give a verbal yes? 08:34:47

10 A Yes. 08:34:54

11 Q What are some metal contacts -- withdrawn. 08:34:55

12 What are some metals that would be used as 08:35:02

13 contacts in this time frame? 08:35:05

14 A I... I actually have not gone back to see what -- 08:35:06

15 what would be implemented after the -- either Lan or '847 08:35:15

16 in this time period, above this MOSFET structure. 08:35:21

17 THE STENOGRAPHIC REPORTER: I'm sorry. Above this

18 what structure?

19 THE WITNESS: MOSFET structure. Same thing I said

20 before.

21 THE STENOGRAPHIC REPORTER: Thank you.

22 BY MR. DOKHANCHY:

23 Q Okay. So you don't know, right? 08:35:39

24 A Yeah, I -- I wouldn't know. 08:35:40

25 Q Let's say it was going to be a titanium -- 08:35:41

1 withdrawn. 08:35:58

2 Let's say it's going to be a tungsten contact. 08:35:58

3 Okay? 08:36:02

4 A Yes. 08:36:05

5 Q Would the adhesion between the tungsten contact 08:36:05

6 and the titanium nitride gate improve if there were a 08:36:11

7 metal diffusion into the titanium nitride gate before that 08:36:16

8 contact were made? 08:36:20

9 A I do not know. 08:36:22

10 Q Okay. Would the contact resistance lower if a 08:36:23

11 metal diffusion were performed on the titanium nitride 08:36:29

12 gate before that contact were made? 08:36:32

13 A Repeat that, please? 08:36:35

14 Q Would the contact resistance improve if a metal 08:36:38

15 diffusion were performed on the titanium nitride gate 08:36:41

16 before the contact with the tungsten contact were made? 08:36:45

17 A I do not know. 08:36:48

18 Q I have a few more questions on this topic. We 08:36:49

19 can take a break now or we can continue. Which would you 08:37:05

20 prefer, Dr. Fitzgerald? 08:37:08

21 A I -- we can continue, if you'd like. 08:37:09

22 Q Okay. You mentioned a work function earlier. Do 08:37:14

23 you recall that? 08:37:23

24 A Yes. 08:37:23

25 Q And that's a property of the gate material; is 08:37:26

1 that correct? 08:37:29

2 A It's a property of any material. 08:37:29

3 Q In the context that we're talking about with Lan 08:37:34

4 and other references in a transistor architecture, there 08:37:40

5 is the concept of a work function of the gate material; is 08:37:45

6 that right? 08:37:50

7 A Yes. 08:37:50

8 Q And what is the -- what is a work function? 08:37:53

9 A It's the -- the work function is the energy from 08:38:01

10 the Fermi level to the vacuum. 08:38:08

11 THE STENOGRAPHIC REPORTER: I'm sorry, you said 08:38:14

12 formula wall to the vacuum? 08:38:15

13 THE WITNESS: Sorry. The energy -- the work function 08:38:16

14 energy is between the Fermi level and vacuum. 08:38:20

15 THE STENOGRAPHIC REPORTER: Fermi level? 08:38:25

16 THE WITNESS: Fermi level. F-e-r-m-i. 08:38:27

17 THE STENOGRAPHIC REPORTER: Thank you. 08:38:29

18 BY MR. DOKHANCHY: 08:38:30

19 Q And the -- the work function of the gate impacts 08:38:38

20 certain properties of the transistor such as the threshold 08:38:45

21 voltage; is that correct? 08:38:51

22 A Yes. 08:38:53

23 Q And when designing the transistor, you might want 08:38:53

24 it to have a particular threshold voltage; is that right? 08:38:57

25 A Yes. 08:39:01

1 Q You may therefore want to design a particular 08:39:01
2 work function for the gate; is that right? 08:39:07
3 A Yes. 08:39:09
4 Q And one way you could do that to adjust the work 08:39:10
5 function would be to diffuse one metal into another in the 08:39:16
6 gate; is that right? 08:39:23
7 A I am not familiar with that in this time period. 08:39:24
8 That's why I mentioned the titanium aluminum nitride. 08:39:31
9 They put aluminum inside titanium nitride in order to 08:39:34
10 shift the work function, I believe for the -- for the 08:39:39
11 PMOS, but I'm not sure about that. But yeah, to change 08:39:44
12 the work function of one, either NMOS or the PMOS, for -- 08:39:47
13 just what you said. 08:39:54
14 Q In the Lan reference, you point to the cap layers 08:39:56
15 912 and 918, which serve as etching masks for forming 08:40:01
16 recesses in the substrate. Do you recall that? 08:40:06
17 A The cap layer -- let's see. It's etch mask for 08:40:08
18 sure. I'd have to look at the process. But yeah, it's an 08:40:20
19 etch mask. 08:40:23
20 Q So we can go to your declaration, if that's 08:40:25
21 helpful. 08:40:27
22 A Yeah. 08:40:27
23 Q So paragraph 163, on page 64. 08:40:28
24 Let me know when you get there. 08:40:46
25 A Yes, I'm there. And it's, you know, what I just 08:40:48

1 said, which is an -- it's an etch mask. 08:41:07

2 Q So as you state here, Lan's cap layers serve as 08:41:12

3 etch masks, correct? 08:41:16

4 A Yes. 08:41:17

5 Q Lan's cap layers are not for protecting the gate 08:41:18

6 during silicide of the source or drain, correct? 08:41:23

7 THE STENOGRAPHIC REPORTER: You said source or drain? 08:41:33

8 MR. DOKHANCHY: Correct. 08:41:34

9 THE STENOGRAPHIC REPORTER: Thank you. 08:41:35

10 THE WITNESS: Oh, can you repeat that question again? 08:41:35

11 BY MR. DOKHANCHY: 08:41:49

12 Q As you state in paragraph 163, Lan's cap layers 08:41:51

13 serve as etch masks. Lan's cap layers are not for 08:41:54

14 protecting the gate during silicide of the source or 08:41:59

15 drain, correct? 08:42:02

16 A I don't say that here. 08:42:02

17 Q I see that you don't say that. I'm asking you, 08:42:05

18 you've said here that Lan's cap layers serve as etch 08:42:12

19 masks. Lan does not say that its cap layers are for 08:42:15

20 protecting the gate during silicide of the source or 08:42:19

21 drain, correct? 08:42:21

22 A Lan -- the purpose of the cap layer is to protect 08:42:22

23 it in a variety of times, right? And then in Lan, it's 08:42:32

24 there as an etch mask. Now, getting to the silicidation, 08:42:37

25 remember there's two versions of gates in Lan, right, a 08:42:44

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1 polysilicon one or a -- or, you know -- or a metal one. 08:42:50

2 And so in a metal one, the cap is protecting the metal. 08:42:58

3 In a polysilicon one, you would have to remove the cap 08:43:05

4 layer to silicide it. 08:43:10

5 Q Nowhere in Lan does it say that when the metal -- 08:43:11

6 withdrawn. 08:43:16

7 Nowhere in Lan does it say that when the gate is 08:43:16

8 metal, the cap protects the metal during silicidation of 08:43:19

9 the source and drain, correct? 08:43:31

10 A Yeah, I mean, what I just said is because a 08:43:32

11 POSITA would know, of course, that the cap layer, as I 08:43:34

12 wrote in my declaration, has to be removed if the gate's 08:43:39

13 polysilicon. And so you have to do that to create a 08:43:43

14 silicide. If not, you know, you have the advantage of 08:43:47

15 having the dielectric on top of the metal gate, which 08:43:52

16 is -- which is great. And a POSITA would know that for 08:43:59

17 sure. 08:44:03

18 Q Okay. That doesn't answer my question. What I 08:44:03

19 asked is, nowhere in Lan does it say that when the gate is 08:44:09

20 metal, the cap should be retained to protect the gate, 08:44:12

21 correct? 08:44:17

22 A Correct, yeah. I was just saying that that -- 08:44:17

23 that is an option. To have the cap in an embodiment with 08:44:21

24 a metal gate is in Lan. Because it says that -- when 08:44:25

25 referring, let's say, to Figure 12, right, it's saying 08:44:31

1 that the gate could be metal. There's a cap layer there. 08:44:34

2 And a POSITA would know that that's a good thing, because 08:44:36

3 it's protecting the metal gate. 08:44:41

4 The last part is me saying that as an expert, a 08:44:46

5 POSITA reading this would know that's the case. 08:44:48

6 Q Later on, as we discussed, after those steps, you 08:44:51

7 need to remove the cap to contact the gate, right? 08:45:00

8 A What do you mean contact... you would need to 08:45:04

9 have penetrations through the cap or move the cap, but 08:45:12

10 that's not shown. You know, it basically depends on 08:45:16

11 what's coming afterwards from an interconnect point of 08:45:21

12 view. 08:45:23

13 Q Just a bit more on this. 08:45:23

14 The benefit or one benefit, you say, of retaining 08:45:33

15 the cap in the Lan reference would be to protect the gate 08:45:43

16 during silicide of the source/drain, right? 08:45:47

17 A Yeah, all sorts of processes, I mention, also, 08:45:51

18 you know, yeah, various chemicals, whatever. And a second 08:45:55

19 one is that, of course, the -- whatever interconnect you 08:46:00

20 do on top of that after this process, the advantage is you 08:46:06

21 need to have not shorting. Right? So for a bunch of 08:46:09

22 reasons, it's great to have the cap there. 08:46:14

23 Q And one of the concerns you list is that if 08:46:16

24 there's no cap and the gate is metal, the etching that 08:46:24

25 removes the unreacted metal after siliciding the 08:46:30

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1 source/drain might also strip some of the gate, correct? 08:46:35

2 A Yes, it's an example of as you go forward with 08:46:38

3 CMOS process after that point, that you may be able to -- 08:46:44

4 you know, you might -- you don't want chemical exposure of 08:46:48

5 your metal gate is basically what I'm saying. 08:46:51

6 Q Okay. And could someone choose to simply not 08:46:53

7 remove the unreacted metal? 08:46:58

8 A You mean if you're making silicide in the 08:47:00

9 source/drain? 08:47:09

10 Q Yes. 08:47:09

11 A These references don't discuss that, but I don't 08:47:10

12 have -- I don't know if there's any processes because, of 08:47:14

13 course, the silicide process works where -- typically, you 08:47:17

14 do an aligned one, so, you know, the reason you're doing 08:47:21

15 that is you react it, and then you etch away metals from 08:47:25

16 everywhere else, and if you were to leave those metals in 08:47:34

17 the CMOS process, you short out a bunch of stuff. 08:47:36

18 THE STENOGRAPHIC REPORTER: I'm sorry. You're 08:47:36

19 speaking really fast. 08:47:36

20 THE WITNESS: Sorry, sorry. 08:47:36

21 THE STENOGRAPHIC REPORTER: You said if you were to 08:47:41

22 leave what? 08:47:41

23 THE WITNESS: In regular CMOS process, you deposit 08:47:42

24 metal everywhere and then react, and the areas are exposed 08:47:52

25 to silicon to form silicide. And then you etch the metal 08:48:01

1 away, and it doesn't etch the silicide, and that way, you 08:48:04
2 have a selective process. If you left the metal in place, 08:48:09
3 you'd have metal everywhere over your surface in a typical 08:48:15
4 CMOS process, and that, of course, you can't have. 08:48:19

5 BY MR. DOKHANCHY: 08:48:21

6 Q When you lay down the metal, you don't lay it 08:48:27
7 down everywhere, right, because then it would diffuse 08:48:29
8 everywhere in the silicide process? 08:48:32

9 A No. I mean, that's the whole point, right? In a 08:48:34
10 silicide process, you expose the areas -- so if you go 08:48:37
11 back in time, the silicide process where -- if using a 08:48:40
12 poly gate and you have two silicon source and drain, there 08:48:45
13 were periods of time where technology -- the beauty of 08:48:51
14 that is you minimize mask levels by depositing metal 08:48:53
15 everywhere. You heat it up. It reacts in those areas. 08:48:56
16 And then you etch -- you take an etchant to remove only 08:49:00
17 where there's metal, not silicide. 08:49:06

18 And then -- so then in one mask level, you 08:49:08
19 basically all these self-aligned contacts and the gate, 08:49:10
20 and that's the beauty of the silicide process. 08:49:13

21 Q How thick, ordinarily, is that unreacted metal, 08:49:21
22 ballpark? 08:49:32

23 A Depends on the technology. As technology goes 08:49:32
24 further and the transistors get smaller, the metal layer's 08:49:36
25 thinner and thinner, so -- and I -- I mean, off the top of 08:49:40

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1 my head, since, you know, again, it's not covered in any 08:49:43
2 of these sources, I don't recall -- you know, in the time 08:49:47
3 period of the '847, I don't recall the exact thickness. 08:49:53
4 But, I mean, we're not talking -- I mean, 08:49:58
5 obviously, it's not microns, and it's not 10 angstroms, 08:50:01
6 right, you know. 08:50:03
7 THE STENOGRAPHIC REPORTER: And it's not what? 08:50:03
8 THE WITNESS: It's not a micron and it's not 10 08:50:05
9 angstroms. Angstrom is a-n-g-s-t-r-o-m. 08:50:12
10 THE STENOGRAPHIC REPORTER: Thank you. 08:50:18
11 BY MR. DOKHANCHY: 08:50:19
12 Q And what about the relative thickness of the 08:50:20
13 unreacted metal versus the thickness of the gate? Is one 08:50:23
14 thicker than the other? Are they the same thickness? 08:50:26
15 A You mean when you do the silicide process I was 08:50:30
16 just talking about? 08:50:33
17 Q Yes. 08:50:34
18 A Typically, the gate thickness is greater than the 08:50:34
19 metal you put down. 08:50:41
20 Q Would you say it's a little bit thicker or much 08:50:42
21 thicker? Can you... 08:50:47
22 A I mean, you know, from a topological point of 08:50:49
23 view, usually it's much thicker. 08:50:55
24 MR. DOKHANCHY: All right. Why don't we take a 08:51:03
25 ten-minute break? 08:51:04

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1 THE WITNESS: Okay. 08:51:05

2 THE VIDEOGRAPHER: We are going off the record. The 08:51:07

3 time on the video monitor is 8:51. 08:51:12

4 (Recess taken.) 09:03:21

5 THE VIDEOGRAPHER: We're going back on the record. 09:03:37

6 The time on the video monitor is 9:04. 09:04:00

7 BY MR. DOKHANCHY: 09:04:04

8 Q Welcome back, Dr. Fitzgerald. 09:04:07

9 During the break, did you speak to your counsel 09:04:09

10 about anything related to this deposition or the prior art 09:04:13

11 references? 09:04:18

12 A No. 09:04:18

13 Q Okay. Do you have the Liaw reference? 09:04:19

14 A Yes, let me turn to it. Okay. 09:04:26

15 Q Okay. If you turn to Figures 3A and 3B. 09:04:46

16 A Okay. 09:05:03

17 Q There is a structure there called plug 322 in 09:05:04

18 Figure 3A, 328 in Figure 3B. Do you see that? 09:05:11

19 A Yes. 09:05:16

20 Q And that plug is created for the purpose of 09:05:17

21 accessing the source/drain and applying a voltage to it, 09:05:21

22 right? 09:05:26

23 A Yeah. That plug is meant to connect to the 09:05:26

24 MOSFET context, which -- you know, yeah. 09:05:32

25 Q And you talk about, in your declaration, that 09:05:34

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1 Liaw says to keep the cap layer 312 in an embodiment, 09:05:40
2 right? 09:05:46
3 A The 312 is -- I mean, basically, it was about -- 09:05:46
4 about that cap saying that if it's there, then, of course, 09:05:52
5 if you're misaligned, it doesn't short out. So that's 09:05:55
6 what they're saying. 09:05:58
7 Q Right. So Liaw's motivation for keeping the cap 09:05:59
8 layer 312 is for avoiding or accommodating a misalignment 09:06:04
9 of the plug 328 to avoid a short between the source/drain 09:06:11
10 and the gate, right? 09:06:17
11 A Yeah, this is the additional benefit of the cap 09:06:18
12 layer where, remember, before, we were talking about 09:06:22
13 the -- protecting the metal gate. Liaw shows that, you 09:06:26
14 know, of course, like what we've been talking about, what 09:06:30
15 comes later -- there's an additional benefit, of course, 09:06:32
16 which is that, well, if you have the cap layer there, then 09:06:35
17 there's certain benefits to it when you're making 09:06:38
18 interconnects and not shorting things out. 09:06:40
19 Q Right. The only benefit that Liaw points to 09:06:44
20 specifically is the resilience against misalignment of the 09:06:49
21 plug in terms of the rationale for keeping the cap over 09:06:56
22 the gate, correct? 09:07:00
23 A You know, Liaw's main concern, I would say, is 09:07:01
24 that the -- on the source self-aligned, that they don't 09:07:06
25 have to be as accurate with photolithography and that the 09:07:10

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1 plug comes down. Because the cap's there to prevent 09:07:14
2 shorting, it can kind of still contact the source/drain. 09:07:18
3 But if, you know, the plug goes over on top of 09:07:22
4 where the gate is, that the cap layer protects it, right? 09:07:25
5 So that's what I was saying before. The cap layer 09:07:30
6 protects, continuing forward, from, you know, the gate 09:07:33
7 being shorted out, and Liaw is an example of that. 09:07:37
8 THE STENOGRAPHIC REPORTER: And I'm sorry. Are you 09:07:41
9 saying Neaw or Liaw? 09:07:42
10 THE WITNESS: Yeah, I don't know how to pronounce it. 09:07:43
11 It's L-i-a-w. I think it's Liaw, I think, but I don't 09:07:45
12 know. 09:07:57
13 BY MR. DOKHANCHY: 09:07:57
14 Q Right. So that is the one benefit described in 09:07:57
15 Liaw. When I say that, it is -- withdrawn. That was a 09:08:00
16 terribly formed question. 09:08:06
17 Here's the question: The sole benefit described 09:08:07
18 in Liaw of retaining the cap over the gate layer -- or 09:08:11
19 over the gate is to protect against inadvertent contact 09:08:17
20 between the plug and the gate, thereby preventing a short 09:08:24
21 between the gate and the source/drain; is that right? 09:08:28
22 A I mean, yeah, like, generalized, just saying 09:08:31
23 that, yeah, when you're making interconnects after those 09:08:35
24 MOS structures, the cap aids in preventing shorts, right? 09:08:38
25 That's their -- that's their goal. 09:08:43

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1 Q Right. Specifically, the benefit described in 09:08:44
2 Liaw of retaining that cap during any subsequent step is 09:08:48
3 to prevent a short specifically from the plug 328 to the 09:08:52
4 gate, correct? 09:08:57

5 A Well, that's the embodiment they show. But, of 09:08:59
6 course, a POSITA would know, yeah, sure. I mean, as you 09:09:04
7 know, when you look, like, out of the plane of this, 09:09:07
8 there's all sorts of patterns and stuff, right, so you 09:09:09
9 would know, like, okay, they're talking about the plug and 09:09:13
10 interconnect on the MOSFET, but it's true, of course, for 09:09:14
11 all the other plugs coming down too, right, that, you 09:09:17
12 know, you don't want an open gate so that then there's a 09:09:20
13 long line that could short on anything, right? 09:09:22

14 So, yeah, I mean, it's a -- it's an embodiment of 09:09:25
15 the idea that the cap helps insulate the gate from shorts 09:09:28
16 from plugs, right? 09:09:33

17 Q So if you go to Column 5 of Liaw and go to 09:09:34
18 line 5. 09:09:42

19 A Column 5, line 5? 09:09:45

20 Q Yes. 09:09:46

21 A Okay. 09:09:47

22 Q Liaw says, In addition, by keeping the cap layer 09:09:49
23 312 atop the metal gate conductor 308, the MOS device 300 09:09:54
24 is able to tolerate a slight misalignment of the 09:10:00
25 conductive plug 322. Do you see that? 09:10:04

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1 a POSITA would understand, yes, preventing the shorting 09:11:29
2 from these interconnects to the gate is a good thing. 09:11:33
3 Q Okay. Now, the Lan reference does not create 09:11:35
4 such a plug to the source/drain, right? 09:11:44
5 A The Lan and Chen and -- yeah, I mean, all those 09:11:47
6 cases do not show what comes after the MOS structure. 09:11:54
7 Q So to be clear, the Lan reference does not create 09:11:58
8 a plug to the source/drain as in Liaw, right? 09:12:05
9 A Yeah, it doesn't show the processes that come 09:12:08
10 afterwards -- in Lan, it does not show the processes that 09:12:10
11 come afterwards to make an integrated circuit so that the 09:12:17
12 device can function. 09:12:20
13 Q And it's not just about showing the process, but 09:12:27
14 the Lan reference does not describe or reference in any 09:12:31
15 way creating a plug analogous to the Liaw reference plug, 09:12:36
16 right? 09:12:40
17 A I don't believe so. 09:12:40
18 Q The Liaw reference, if you go back to the figure 09:12:42
19 we were looking at, 3A and/or 3B. 09:12:51
20 A Yes. 09:12:56
21 Q You see there's a sidewall spacer 314? 09:12:56
22 A Yes. 09:13:01
23 Q What is the purpose of sidewall spacer 314? 09:13:02
24 A So spacers in general -- well, 314 spacer, the 09:13:10
25 purpose is to offset a process, which -- looks like 316, 09:13:16

1 which is the source/drain, to offset that from the gate. 09:13:24
2 In CMOS, you use spacers because vertical films can be 09:13:31
3 done with great precision from a thickness perspective. 09:13:38
4 And so what happens is if you deposit a uniform layer 09:13:43
5 across the gate in the source/drain area, then with an 09:13:48
6 anisotropic etch, what happens is you're left with a very 09:13:53
7 thin layer on the sidewall that's very reproducible 09:13:59
8 because of both CMOS processing and the accuracy of that 09:14:02
9 thickness, and what that means is you can have very small 09:14:06
10 distances at the bottom of that gate, so you can offset 09:14:12
11 processes and you know exactly how far they are from the 09:14:16
12 gate, and to do that with lithography, you would have 09:14:19
13 lower yield. 09:14:23
14 So that's the purpose of a spacer, and in 3A, it 09:14:25
15 looks like the spacer was used to make things like 316 09:14:28
16 because that needs to be offset from where the channel 09:14:35
17 under the gate is. 09:14:39
18 Q Okay. So one of the purposes of sidewall spacer 09:14:45
19 314 is to space the gate away from the source/drain; is 09:14:48
20 that right? 09:14:52
21 A That's one use of spacers, yes. 09:14:52
22 Q So why is it that one would need a cap on the 09:14:54
23 gate if the source/drain were spaced apart from the gate 09:15:01
24 via the sidewall spacer, which should prevent shorting 09:15:06
25 between the gate and the source/drain? 09:15:12

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1 a mask level. 09:16:59

2 Right? So there's an economic but also a 09:17:00

3 technical one, which is that I could precisely control 09:17:02

4 really tiny distances, so then I can play this trade-off 09:17:04

5 where for electrostatic optimization of my MOSFET design, 09:17:06

6 I can move that source/drain pretty close, but not so 09:17:13

7 close that I get all these undesirable overlaps with the 09:17:18

8 inversion channel. 09:17:22

9 So, you know, all over MOSFET, what you just said 09:17:23

10 is true. I would like to space everything out as far as I 09:17:28

11 could, and my yield would go up. The reason people had to 09:17:32

12 move away from that was that as Moore's law continued and, 09:17:36

13 you know, the economics of increasing density, you know, 09:17:39

14 you got to squish things closer and closer together, and 09:17:42

15 then I have lithography problems because, you know, 09:17:49

16 there's overlap, and then I get lower yield, and so the 09:17:52

17 spacer came in and had this huge benefit that I can do 09:17:54

18 tiny distances reproducibly, I get fantastic MOSFET 09:17:58

19 performance. But I don't -- I don't have to worry about 09:18:01

20 the yield problem because the spacers are reproducible 09:18:06

21 because of the accuracy of depositing that layer. 09:18:11

22 But, no, I understand what you're saying, which 09:18:14

23 is that, you know, principle, oh, I'll just put them where 09:18:18

24 I won't have to worry about it. And that's why Liaw 09:18:21

25 says -- you know, they're saying, oh, man, when this comes 09:18:25

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1 in closer, you know -- that problem the spacer's solving, 09:18:26
2 they're saying, like, look, well, if I'm off a little bit, 09:18:33
3 if I have a -- if I have a cap layer on top, then it 09:18:35
4 doesn't short out, right? That's what they're saying. 09:18:38

5 Q Okay. So in your view, that sidewall spacer 314, 09:18:41
6 Liaw is saying that's not effective to protect against a 09:18:48
7 short caused by misalignment of the plug? 09:18:51

8 A I mean, Liaw's definitely saying that, right? 09:18:54
9 They're saying if you shift the plug and you're not 09:18:57
10 hitting it exactly, then, you know, this helps, right? 09:19:01

11 Q And the Lan reference, by contrast, does not say 09:19:05
12 that it is particularly concerned with plug misalignment 09:19:12
13 issues, right? 09:19:17

14 A As I said before, the Lan reference, like '847, 09:19:21
15 is a MOS structure, so they're not going to the point of 09:19:25
16 making those interconnects. Of course, you have to 09:19:30
17 follow, you know, CMOS process because you know that's 09:19:39
18 coming, so you don't want to have things happen or design 09:19:42
19 things that, of course, don't think about the 09:19:44
20 interconnect, right? 09:19:48

21 So, you know, that's why this sort of cap can be 09:19:48
22 useful further down the line, right? It's because you 09:19:54
23 have knowledge of what's coming. But Lan doesn't talk 09:20:00
24 about the interconnect that comes after at all. 09:20:02

25 Q Go back to the Lan reference and jump down to 09:20:06

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1 Figure 12. Let me know when you're there. 09:20:20

2 A Yeah. 09:20:27

3 Q So the Lan reference has... 09:20:31

4 A Here. 09:20:40

5 Q Are you there? 09:20:40

6 A Yeah, I'm here. Yeah. 09:20:42

7 Q So the Lan reference in Figure 12 has sidewall 09:20:45

8 spacers 920. Do you see that? 09:20:49

9 A Yes. 09:20:52

10 Q And those are analogous to the Liaw sidewall 09:20:54

11 spacers 314; is that right? 09:21:01

12 A They're both spacers. 09:21:02

13 Q And additionally, Lan has what it calls a main 09:21:04

14 spacer 920 -- excuse me. Withdrawn. 09:21:11

15 Additionally, Lan has what it calls a main spacer 09:21:14

16 1202 and 1204. Do you see that? 09:21:20

17 A Yes. 09:21:22

18 Q And what is the purpose of main spacer 1202? 09:21:24

19 A The purpose of 1202 after, you know, processing 09:21:34

20 is to create a spacer that goes up over and covers 09:21:41

21 everything, essentially, up the raised source/drain. 09:21:46

22 Q Okay. And the main spacer 1202 has the effect of 09:21:56

23 further separating the source/drain 1206 from the gate 910 09:22:05

24 beyond what sidewall spacer 920 provide, correct? 09:22:12

25 A I think you're saying 920 is a thinner spacer, 09:22:18

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1 and 1202, for example, is a larger spacer, and so the 09:22:25
2 contact for the -- partial contact of the 09:22:32
3 silicon-germanium on top is, of course, further out from 09:22:39
4 where, you know, the 920 spacer is. 09:22:44
5 Q Yes. 09:22:47
6 Is that right? 09:22:48
7 A Yes. 09:22:50
8 Q And so the impact of the 1202 spacer being added 09:22:50
9 -- (audio technical difficulty) -- 09:23:06
10 THE STENOGRAPHIC REPORTER: Sorry. I can't hear you. 09:23:06
11 MR. DOKHANCHY: Sorry. 09:23:08
12 BY MR. DOKHANCHY: 09:23:10
13 Q The impact of the main spacer 1202 being added in 09:23:10
14 addition to sidewall spacer 920 is to further distance the 09:23:19
15 source/drain from the gate beyond what that distance would 09:23:24
16 be if 1202 were not there, right? 09:23:29
17 A So, of course, the silicon-germanium source/drain 09:23:34
18 goes in, right, further and closer to the gate as you can 09:23:45
19 see, right, because the -- so from a channel resistance 09:23:49
20 perspective, right, the source/drain still goes in quite 09:23:56
21 far. It's just that it's covering up part of -- a part of 09:24:02
22 this raised source/drain, and that way, the contact for 09:24:08
23 the raised source/drain is not going down into the area 09:24:14
24 that would be exposed there beyond 920, right? That's 09:24:21
25 the -- that's what you've got to make sure of, right? 09:24:24

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1 Q And why would that -- 09:24:26

2 THE STENOGRAPHIC REPORTER: Sorry. You're now saying 09:24:27

3 resource drain? 09:24:30

4 THE WITNESS: I think I might have said raised 09:24:30

5 source/drain, r-a-i-s-e-d. 09:24:36

6 THE STENOGRAPHIC REPORTER: Raised. Thank you. 09:24:47

7 THE WITNESS: Yeah. 09:24:47

8 THE STENOGRAPHIC REPORTER: And then there was one -- 09:24:47

9 another thing you said you said. Going down the ear that 09:24:50

10 would be exposed there beyond 920? You said ear? 09:24:53

11 MR. DOKHANCHY: Area. 09:24:53

12 THE STENOGRAPHIC REPORTER: Area. Thank you, thank 09:24:54

13 you. 09:24:54

14 BY MR. DOKHANCHY: 09:24:59

15 Q Why would it be beneficial to cover up part of 09:24:59

16 the raised source/drain with main spacer 1202? 09:25:04

17 A Because there, you know, could be leakage and 09:25:09

18 things like that, and also, your contact might go into the 09:25:14

19 silicon instead of the silicon-germanium and all that kind 09:25:17

20 of thing. 09:25:19

21 Q Another benefit would be that the contact would 09:25:20

22 be less likely to short the gate versus the source/drain, 09:25:25

23 correct? 09:25:30

24 A Well, I mean, these things are, of course, you 09:25:30

25 know -- these spacings are still small, right, because 09:25:34

1 they're going to -- as I said before, the demand to shrink 09:25:38
2 is still there, right, so they're not -- you couldn't 09:25:43
3 employ raised silicon source/drains -- sorry, for the 09:25:46
4 court reporter -- raised silicon-germanium source/drains 09:25:49
5 if you expanded the size of the transistor. 09:25:54

6 So meaning that, from a Moore's law point of 09:26:02
7 view, this whole thing still has to fit into a tight area, 09:26:05
8 right? So, I mean, they're drawing this stretched out so 09:26:10
9 you can see what's there, but these are all really still 09:26:16
10 tiny distances, and the raised source/drain can't be way, 09:26:18
11 way, way far out compared to where it would have been if 09:26:23
12 you didn't do strained silicon. 09:26:26

13 Q I understand that. I think we're sort of talking 09:26:29
14 past each other. My question is: One of the benefits of 09:26:32
15 using that main spacer 1202 is to push out the contact 09:26:35
16 with the source/drain farther from the gate, which reduces 09:26:42
17 the risk of short, correct? 09:26:47

18 A I mean, reduce the risk of short down -- down the 09:26:49
19 edge of it, I mean, so -- but like I said, these distances 09:26:55
20 are still small, so, I mean, I think Liaw and all that 09:26:57
21 stuff is still important. 09:27:01

22 Q So I guess I don't understand your answer. Is it 09:27:02
23 yes or no? Does the main spacer 1202 reduce the risk of 09:27:12
24 short between the contact shorting the source and the 09:27:16
25 drain? 09:27:20

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1 A Shorting the -- not the source and the drain, you 09:27:20
2 mean. 09:27:26
3 Q Sorry. Yeah, let me ask that again. The 09:27:27
4 question is simply yes or no, does the main spacer reduce 09:27:28
5 the risk that the contact will short the source/drain and 09:27:31
6 the gate? 09:27:34
7 A No. What I was saying before was that if 1202 09:27:34
8 were not there, then when you deposit the contact, it 09:27:39
9 could go down that inner part and touch, like, 1102, for 09:27:44
10 example, and that would be bad. 09:27:52
11 Q Right. That's one method. I'm asking about an 09:27:53
12 additional method. If 1202 were not there and you had a 09:27:58
13 misalignment in the source/drain contact, it would be more 09:28:04
14 likely to short the gate than if 1202 were there, correct? 09:28:08
15 A I mean, it's just like -- to the same thing we 09:28:14
16 talked about in the other case, right? Which is that 09:28:18
17 you're going to minimize these distances. So, you know, 09:28:22
18 this is going to be as close as possible, and, you know, 09:28:25
19 if 1202 is protecting that whole area on the side that's 09:28:32
20 way more important, the danger of the contact when you 09:28:40
21 come down is on -- on the source/drain, the way Liaw is 09:28:44
22 talking about, and the gate is still there if you misalign 09:28:47
23 it, right. 09:28:51
24 Q Yeah. I'm sorry. That's -- you're saying a lot 09:28:55
25 of things that are not an answer to my question, so I'm 09:28:59

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1 just going to ask it one more time, and if you can't 09:29:01
2 answer it yes or no, just tell me that. 09:29:03
3 Yes or no, the addition of the 1202 spacer has 09:29:04
4 the effect of increasing the resilience against 09:29:12
5 misalignment of the source/drain contact when it comes to 09:29:19
6 shorting the gate and the source/drain? 09:29:22
7 A I wouldn't say that. 09:29:24
8 Q Why is that, given that the contact is farther 09:29:25
9 from where it originally would be without 1202? 09:29:34
10 A Well, that's all the stuff that I just talked 09:29:37
11 about that you didn't want to hear me say. 09:29:41
12 Q Well, you're saying that it's still important to 09:29:43
13 further protect against misalignment. That doesn't answer 09:29:45
14 the question of whether 1202 improves the resilience 09:29:48
15 against misalignment. Two different questions. 09:29:52
16 MR. LONG: Objection; argumentative. 09:29:54
17 THE WITNESS: So, okay. So here's from a device 09:30:00
18 engineer's perspective. I can't not have 1202. If I did, 09:30:03
19 my metals would go down that slope off the source/drain 09:30:09
20 and create all sorts of problems. Like, the device 09:30:14
21 wouldn't work, right? I'd get shorts. I would have metal 09:30:17
22 too close to the -- to the gate, all sorts of 09:30:21
23 consequences. So I have to have 1202 to cover that space 09:30:27
24 there, which is very tiny, right? 09:30:30
25 In that space, it's like -- the 1102 is an LDD, 09:30:34

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1 right? So it's a very tiny space. So the purpose of 09:30:40
2 1202, those are all the priorities. And I still have the 09:30:45
3 problem that Liaw talks about because if I'm sloppy on my 09:30:48
4 source/drain alignment, right, then I -- then I would -- I 09:30:55
5 could still hit the gate if I don't have the cap layer, 09:31:03
6 right? That's all I'm saying. 09:31:08
7 BY MR. DOKHANCHY: 09:31:09
8 Q If the -- if the spacer did not extend as far as 09:31:25
9 it does in Figure 12 of Lan, and instead were thinner, you 09:31:30
10 agree there would be less resilience to misalignment of 09:31:37
11 the plug to the source/drain, fair? 09:31:41
12 A You know, both problems become worse. The 09:31:43
13 problem I was talking about, which is the principal reason 09:31:48
14 you've got to have 1202. But then also your chances, and 09:31:51
15 statistically based on alignment, would be higher as well. 09:31:57
16 But it doesn't mean it's zero, by covering up that space. 09:32:01
17 Q Right. That's the disconnect I was talking 09:32:04
18 about. And I don't mean to... explain. But, for example, 09:32:10
19 the spacer 1202 in Lan extends further and covers more of 09:32:19
20 the source/drain than the spacer in Liaw, right? 09:32:30
21 MR. LONG: Objection; foundation. 09:32:37
22 THE WITNESS: I don't -- I mean, I don't know how to 09:32:39
23 compare the two. 09:32:50
24 BY MR. DOKHANCHY: 09:32:54
25 Q We can put them up side by side. You'll see that 09:32:55

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1 the spacer in Lan reaches all the way to the midpoint of 09:32:57
2 the raised epitaxial layer. 09:33:09
3 THE STENOGRAPHIC REPORTER: I'm sorry. It's a bit 09:33:02
4 hard to hear you, Reza. You said all the way to the 09:33:06
5 midpoint what? 09:33:07
6 BY MR. DOKHANCHY: 09:33:08
7 Q The midpoint of the raised epitaxial layers. 09:33:08
8 And the sidewall spacer in Liaw reaches just 09:33:15
9 barely into the source/drain area, correct? 09:33:21
10 A But I don't think Liaw -- sorry. 09:33:26
11 MR. LONG: Objection; foundation. 09:33:30
12 THE WITNESS: Liaw doesn't have the silicon-germanium 09:33:31
13 source/drain, so they're different devices. 09:33:34
14 BY MR. DOKHANCHY: 09:33:36
15 Q Why does it matter that it doesn't have a 09:33:40
16 silicon-germanium source/drain versus some other type of 09:33:44
17 source/drain? 09:33:47
18 A Well, just meaning that if I'm looking at things 09:33:47
19 relatively between the diagrams, the Figure 12 over here 09:33:51
20 is for different kind of source/drain. The Liaw is for a 09:33:55
21 regular MOSFET source/drain. So, you know, here we're 09:34:00
22 showing a 920 and 1202, and the other one is just a, you 09:34:04
23 know, regular conventional spacer. 09:34:09
24 Q Does that impact, in your view, the concerns 09:34:11
25 regarding misalignment problems of the plug? 09:34:18

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1	A	No.	09:34:22
2	Q	Okay. So it's correct, isn't it, that the	09:34:28
3		spacers in Lan cover, and therefore protect from a short,	09:34:34
4		a greater proportion of the source/drain than in Liaw,	09:34:42
5		right?	09:34:47
6	MR. LONG:	Objection; foundation.	09:34:47
7	THE WITNESS:	No. Because, you know, the -- for	09:34:48
8		example, 920 can be much thinner than the other in -- that	09:34:53
9		other figure in Liaw. And then 1202, you know, it could	09:34:59
10		be a double spacer that's the same thickness as the one in	09:35:02
11		Liaw, right?	09:35:08
12	BY MR. DOKHANCHY:		09:35:11
13	Q	Well, the spacer in Lan reaches the midpoint of	09:35:11
14		the source/drain, right?	09:35:17
15	A	It --	09:35:18
16	MR. LONG:	Objection; foundation.	09:35:19
17	THE WITNESS:	It is covering in that picture what	09:35:19
18		looks to be about half of the raised source/drain. But	09:35:25
19		that doesn't say anything about its total distance from	09:35:30
20		the gate in comparison to Liaw.	09:35:33
21	BY MR. DOKHANCHY:		09:35:43
22	Q	And in Liaw, the sidewall spacer covers much less	09:35:43
23		than half of the source/drain.	09:35:51
24	MR. LONG:	Objection; foundation.	09:35:54
25			

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1 BY MR. DOKHANCHY: 09:35:55

2 Q Correct? 09:35:56

3 A As I said, it doesn't have a silicon-germanium 09:35:56

4 source/drain, and the distances are -- are -- are 09:36:02

5 obviously different scales or not to scale. 09:36:06

6 Q So let me touch on that first point first. I 09:36:11

7 thought you said it doesn't matter, for the purposes of 09:36:15

8 the misalignment concern, that one source/drain is 09:36:18

9 silicon-germanium and the other one is not. Do you still 09:36:23

10 believe that? 09:36:27

11 A What -- because of the statement I just made, 09:36:27

12 which is that if you imagine you're keeping -- you know 09:36:30

13 electrostatic's the same and the density is the same, 09:36:33

14 right, and I try to make sure the spacers aren't pushing 09:36:38

15 the silicon-germanium out any further out because of 09:36:41

16 density, then the distances are the same. So then I have 09:36:43

17 the same misalignment problem. 09:36:45

18 Q So the only thing that matters, in your view, is 09:36:47

19 the absolute distances between the gate and the 09:36:53

20 source/drain, not the relative sizes and distances of 09:36:57

21 those items; is that right? 09:37:02

22 MR. LONG: Objection; vague. 09:37:05

23 THE WITNESS: What I'm saying is that I have to have 09:37:07

24 these transistors in the same footprint. That means that 09:37:09

25 I'm going to design these things so that the gate and the 09:37:14

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1 source/drains are occupying the same area. So therefore, 09:37:17
2 if I have spacers and whatever else I have in there, when 09:37:21
3 I -- when I make my source/drain mask, right, the error is 09:37:29
4 going to be the same if I have the density being the same. 09:37:38
5 So let's say there's a delta L on my window from 09:37:40
6 my source/drain that I'm worried about, and it could 09:37:43
7 shift, you know, this much this way or that way, it will 09:37:47
8 be the same, unless I've expanded my area footprint for 09:37:50
9 the silicon-germanium device, right? 09:37:55
10 But I -- but I can't, because of Moore's law. So 09:37:58
11 all these devices have to be squeezed in and -- squeezed 09:38:01
12 into the same -- to the same space, right? So if I take a 09:38:06
13 silicon MOSFET and a silicon-germanium MOSFET, trust me 09:38:09
14 that when they jump to the silicon-germanium source/drain, 09:38:12
15 there's no way you can go backwards on Moore's law to 09:38:15
16 incorporate that technology. 09:38:19
17 So what I'm saying is Liaw would be -- you have a 09:38:20
18 gate opening and a source/drain opening and there's not 09:38:23
19 going to be much difference in terms of the error. There 09:38:30
20 can't be, because they have to squeeze into the same area. 09:38:36
21 BY MR. DOKHANCHY: 09:38:36
22 Q Well, there could be a difference in the error 09:38:37
23 resilience if more of the -- 09:38:41
24 THE STENOGRAPHIC REPORTER: I'm sorry, you're saying 09:38:45
25 error resilience or area resilience? 09:38:46

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1 MR. DOKHANCHY: Error. 09:38:49

2 THE STENOGRAPHIC REPORTER: Error resistance. Okay. 09:38:49

3 MR. DOKHANCHY: E-r-r-o-r. 09:38:51

4 THE STENOGRAPHIC REPORTER: Thank you. 09:38:53

5 BY MR. DOKHANCHY: 09:38:55

6 Q If the footprint, as you said, is the same 09:38:57

7 between the two references, but the spacer covers more of 09:39:02

8 the source/drain in one of them, that architecture would 09:39:11

9 be more resilient to source/drain contact misalignment, 09:39:15

10 right? 09:39:20

11 A You can't do that because your source/drain area 09:39:20

12 goes down, which means your channel resistance would go -- 09:39:29

13 I mean, your whole circuit of source/drain through 09:39:34

14 channel -- you know, if you abstract yourself, you could 09:39:36

15 call it channel resistance, right? The -- the resistance 09:39:39

16 would go up, because you can't cut down the area. 09:39:41

17 Q That's exactly what's done in Lan. Half of the 09:39:45

18 source/drain is covered by the -- by the spacer. And in 09:39:48

19 Liaw, 10 percent of it is. 09:39:51

20 A But it can't be. So -- 09:39:54

21 MR. LONG: Objection; argumentative. Foundation. 09:39:56

22 THE WITNESS: So what I'm saying is that you want to 09:39:57

23 cover up part of the raised source/drain for the purposes 09:40:03

24 of not having metal go down into that tiny gap between the 09:40:09

25 gate and the raised source/drain. I have to fit the 09:40:13

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1 transistor in the same footprint, and I don't want to 09:40:18
2 decrease my source/drain area, because my resistance goes 09:40:22
3 up. 09:40:25

4 So if you were to actually put these all 09:40:26
5 together, these -- these are things we know even though 09:40:28
6 the -- the diagrams aren't to scale. So -- so that would 09:40:30
7 mean that -- that the alignment problem is still basically 09:40:34
8 the same. Because I'm not going to give up as a design of 09:40:40
9 a -- if I'm designing that device, there's no way I'm 09:40:45
10 going to shrink the source/drain contact. 09:40:48

11 BY MR. DOKHANCHY: 09:40:53

12 Q So then how do you explain Figure 12 of Lan that 09:40:53
13 shows half of the source/drain being covered? 09:40:57

14 A I'm saying that that schematic -- first of all, 09:40:59
15 nowhere in Lan is it saying that. But what I'm saying is 09:41:06
16 that if I were to cover it halfway, the way the diagram 09:41:08
17 shows, then that means that I'd have to have more width 09:41:11
18 than shown here. 09:41:19

19 Q So you're saying the diagram is drawn incorrectly 09:41:19
20 in Lan? 09:41:27

21 A No. I'm just saying it's just saying that I need 09:41:27
22 a spacer there -- if you read the whole thing together, I 09:41:29
23 have a spacer there that is to prevent the contact from 09:41:33
24 going down, you know, into that hole. 09:41:37

25 Q But the spacer covers much more than the amount 09:41:41

1 that you would need to protect contact going down into 09:41:45
2 that hole as depicted in Figure 12. Unless the figure's 09:41:48
3 inaccurate, it covers half the source/drain, correct? 09:41:54
4 A Yeah, but Figure 12 isn't saying anything about 09:41:57
5 Moore's law, total device design, anything like that. So 09:42:00
6 it's just saying, Look, I have to have 1202 go up on top 09:42:04
7 of that raised source/drain. And -- and you could use my 09:42:07
8 invention, and there's a thousand things I want to do when 09:42:13
9 I incorporate this and other inventions in designing a 09:42:15
10 real MOSFET. 09:42:19
11 Q Okay. So do you disagree that the structure in 09:42:20
12 Lan includes a sidewall spacer and a main spacer 1202, 09:42:28
13 wherein the main spacer in the actual design of the Lan 09:42:32
14 device covers and protects half of the source/drain? Do 09:42:38
15 you agree with that? 09:42:43
16 A I have no -- I have no problem saying that 09:42:43
17 Figure 12 shows 1202 covering half of the 09:42:45
18 silicon-germanium raised source/drain in that picture. 09:42:50
19 Q Okay. All right. Let's go to the Chen 09:42:52
20 reference. Do you have that? 09:43:08
21 A Yes. Yes, I am here. 09:43:09
22 Q Okay. All right. So your analysis focuses on 09:43:38
23 Figure 5 of the Chen reference. 09:43:42
24 A My analysis involves the whole specification. 09:43:48
25 But Figure 5 is the embodiment that is the same as the 09:43:50

1 '847 and the Lan embodiment. 09:43:59

2 Q Yeah. 09:44:01

3 And you point to a hard mask 503 as the cap 09:44:03

4 layer, right? 09:44:13

5 A I believe so. 09:44:13

6 Q Now, after Figure 5 of Chen, there are further 09:44:15

7 steps required to finalize the transistor, right? 09:44:24

8 A The Figure 5 is one embodiment that's finalized, 09:44:27

9 and Figure 6 is a different one. 09:44:34

10 Q Okay. So you could use Figure 5 as a transistor; 09:44:39

11 is that your testimony? 09:44:42

12 A Well, recall what I have already testified, which 09:44:42

13 is that all of these devices have further processes coming 09:44:45

14 to put them into a working CMOS integrated circuit. So 09:44:50

15 the elements in '847 are all in Figure 5. And so that 09:44:56

16 means it's been disclosed. I can go further and take 09:45:00

17 Figure 5 and head towards interconnects like in Liaw, 09:45:05

18 right? But then I would do additional steps. 09:45:09

19 And what Chen's showing is that, of course, one 09:45:12

20 step I could do is remove the cap layer at some point. 09:45:18

21 Q And one of the steps that Chen refers to is 09:45:23

22 siliciding the gate, right? 09:45:31

23 A Yes. 09:45:33

24 Q And it does not describe that step as optional, 09:45:36

25 correct? 09:45:40

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1 A No. I believe that... oh, well, it depends what 09:45:40
2 you mean by that question. Can you say that again? 09:45:52
3 Q Yeah. So if you go to Column 6, lines 21 to 22. 09:45:53
4 It says, The method forms a silicide layer overlying gate 09:46:04
5 layer and source/drain regions. Right? 09:46:10
6 A Yes. 09:46:13
7 Q It doesn't say you could perform those silicides 09:46:18
8 or you could not. It says that the method of the 09:46:23
9 invention performs silicide on gate and source/drain, 09:46:27
10 correct? 09:46:32
11 A Hold on a sec. 09:46:32
12 So if you're saying that you have to do a 09:46:36
13 silicide gate in Chen, that is incorrect. 09:46:44
14 Q Do you have to do a silicide source/drain? 09:46:46
15 A In Chen? Let's see. 09:46:50
16 I mean, I'm reading Claim 1. Let's see. Might 09:47:01
17 be missing it, but I don't think it's in Claim 1. I don't 09:48:01
18 think in Claim 1, but I didn't read the whole thing. So 09:48:39
19 do you want me to read the whole thing? 09:48:43
20 Q No, that's okay. One thing that is required in 09:48:45
21 Claim 1 is exposing a top surface of the gate structure, 09:48:47
22 right? It's the last element. 09:49:09
23 A Oh, it says exposing a top source of the gate 09:49:11
24 structure -- I have to go back to what a gate structure 09:49:24
25 is. 09:49:26

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1 Q Well, if you look in Column 6, lines -- 09:49:38

2 A I think it says the gate structure is forming a 09:49:41

3 dielectric layer overlying the gate structure -- 09:49:49

4 THE STENOGRAPHIC REPORTER: I'm sorry. I'm sorry. 09:49:49

5 Could you repeat that? 09:49:49

6 THE WITNESS: Oh, sorry. 09:49:49

7 THE STENOGRAPHIC REPORTER: I couldn't hear that. 09:49:52

8 THE WITNESS: I mean, in Independent Claim 1, it says, 09:49:53

9 Forming a dielectric layer overlying the gate structure to 09:49:57

10 protect the gate structure. 09:50:02

11 BY MR. DOKHANCHY: 09:50:06

12 Q Yeah, so I think if you go to line -- Column 6, 09:50:07

13 line 15, you'll see that the way the invention exposes the 09:50:10

14 top surface of the gate structure is to remove the hard 09:50:17

15 mask, right? 09:50:20

16 A Yes. And as I pointed out, in that option, the 09:50:21

17 reason you have to do that is if you're going to make a 09:50:27

18 silicide gate, you have to have the reaction between the 09:50:30

19 metal and the poly, right? But you -- you wouldn't do 09:50:34

20 that if you had a metal gate, right? 09:50:39

21 And the metal gate option in Chen, so Column 3, 09:50:42

22 somewhere when it talks about the gate, it says the gate 09:50:49

23 can be metal. Number 3 -- oh, sorry. It's Column 3, 45. 09:50:52

24 Right. If you look there, it says that the gate can be 09:50:59

25 metal. In which case, I don't mean the silicide. 09:51:02

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1 Q Yeah. In Claim 1, the inventors on Chen are 09:51:05
2 saying, Part of my invention is to expose the top surface 09:51:10
3 of the gate structure. Which in Column 6, is done by 09:51:13
4 removing the hard mask, right? 09:51:17
5 A Did you guys hear that? 09:51:19
6 MR. LONG: Sorry. Objection; argumentative. 09:51:28
7 THE WITNESS: So just to revert, yes, so it describes 09:51:44
8 the silicide process there. But it also says that it has 09:51:44
9 to have a -- 09:51:50
10 THE STENOGRAPHIC REPORTER: Sorry. I'm not hearing 09:51:50
11 you, Mr. Fitzgerald. Your audio is cutting out. Could 09:51:50
12 you repeat that? 09:51:50
13 THE WITNESS: I said that, yes, in Chen, in the 09:51:51
14 specification, it describes the silicide process. And it 09:51:56
15 also says that there's a metal option. Of course, the 09:52:01
16 metal gate option would not have silicide, so that would 09:52:07
17 be a different thing, right? 09:52:10
18 BY MR. DOKHANCHY: 09:52:12
19 Q Right. But when it comes to defining their 09:52:14
20 invention in Claim 1, the inventors on Chen said strip off 09:52:16
21 the cap layer 503, right? 09:52:23
22 A I'm not sure it says that. It says expose the 09:52:26
23 top surface of the gate structure. The top surface of the 09:52:31
24 gate structure may be dielectric. But my point here is 09:52:34
25 that, you know, the elements of '847 are in this document 09:52:40

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1 and included in Figure 5, right? 09:52:48

2 So, you know, it's already been disclosed. So if 09:52:51

3 you do things afterwards, I think -- I think that -- 09:52:53

4 that -- as we said, as you move towards interconnects, I'm 09:53:00

5 going to do other things. If I'm going to access that 09:53:03

6 gate to silicide, yes, I'm going to remove that top -- 09:53:06

7 that top structure. 09:53:09

8 But, you know, it does say that Figure 5 is -- 09:53:10

9 can be a final embodiment, and that's consistent with the 09:53:14

10 fact that we -- 09:53:14

11 THE STENOGRAPHIC REPORTER: I'm sorry. Can be what? 09:53:14

12 THE WITNESS: A final embodiment. And that's 09:53:14

13 consistent with the option that it says at Column 3 for a 09:53:22

14 metal gate. 09:53:25

15 BY MR. DOKHANCHY: 09:53:26

16 Q In order to finalize the device, even if the gate 09:53:26

17 is metal, Chen describes siliciding the source/drain, 09:53:36

18 which is something you'd have to do to finalize the 09:53:46

19 device, right? 09:53:48

20 A I was -- I was looking at that. I mean, it 09:53:49

21 wouldn't surprise me if -- I didn't see silicide the 09:53:56

22 source/drain in here, but, you know, I was just looking 09:54:00

23 very fast. But... what's the question? 09:54:02

24 Q So I'll point you to where it says that. 09:54:05

25 A Okay. Thanks. 09:54:07

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1 Q So in Column 6, line 21. 09:54:08
2 A Yes. 09:54:16
3 Q It describes siliciding the source/drain. Now, 09:54:16
4 you wouldn't consider such a structure finalized until the 09:54:21
5 source/drain were silicided, right? 09:54:26
6 A I consider a -- well, first of all, in terms of 09:54:29
7 what's finalized, we can only go by what, I guess, the 09:54:38
8 specification says and what a POSITA knows how this 09:54:42
9 processor used to interconnect things, right? So in... 09:54:48
10 let's see. I've got to find that part. Yeah, so Column 6 09:54:53
11 is where they talk about finishing device in a couple of 09:55:02
12 ways. 09:55:05
13 So Figure 5 is an embodiment with -- with all the 09:55:05
14 elements in -- in '847. And then it says that in a 09:55:18
15 preferred embodiment, I can remove the top and continue. 09:55:23
16 And that's Figure 6. So that's the way I was reading it. 09:55:30
17 Q That's talking about the gate structure. But 09:55:33
18 then separately, it talks about the source/drain silicide. 09:55:36
19 And just asking you, you wouldn't consider a transistor 09:55:39
20 structure final until the source/drain were silicided, 09:55:44
21 right? 09:55:49
22 A I mean, the terminology of final here is -- is, 09:55:49
23 like we said -- I mean, final is when it's in the circuit. 09:55:53
24 It could be, you know, a practical version of that. And 09:55:58
25 here, the specification, they're using the terms of what's 09:56:01

1 finalized and then what is, you know, from -- from their 09:56:06
2 perspective. 09:56:10

3 But, you know, from the point of view of me using 09:56:11
4 Chen for the '847, I'm just trying to show that there's an 09:56:13
5 embodiment that discloses all the elements that are in 09:56:18
6 Figure 1 -- sorry -- Claim 1, for example, in the '847, 09:56:23
7 right? 09:56:33

8 So, you know, the term finalized means a 09:56:33
9 practical thing. What I'm doing here is just to show that 09:56:36
10 the '847 was disclosed. Right? 09:56:39

11 Q Right. I -- I just want to get your 09:56:42
12 understanding of when a transistor is finalized. And I 09:56:49
13 understand that you could -- after finalization, you can 09:56:53
14 connect it up to other things. But what I'm talking about 09:56:57
15 is when the transistor structure itself is finalized. 09:56:59

16 You wouldn't consider that transistor structure 09:57:02
17 finalized until the source/drain were silicided, right? 09:57:05

18 A So, I mean, here, the term finalized, what's that 09:57:09
19 mean? 09:57:14

20 Q Whatever it means to you. 09:57:14

21 A Well, I think what matters here is what it means 09:57:16
22 in the prior art and the '847, right? 09:57:24

23 Q That's fine. As a person of skill in the art, 09:57:29
24 would you consider the transistor structure finalized 09:57:34
25 before the silicide of the source/drain, yes or no? 09:57:36

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1 A I have -- what -- the term finalized is referring 09:57:38
2 to what kind of finalization? If I look at what we're 09:57:43
3 doing here, and I see an embodiment that discloses 09:57:47
4 everything in the '847, that's all that matters. 09:57:50
5 And I know there's other stuff coming from a 09:57:53
6 practical finalization point of view, right? But I 09:57:55
7 don't -- the practical finalization point of view doesn't 09:57:59
8 have anything to do with the mission that I had today, 09:58:02
9 right? 09:58:05
10 Q So when you say practical finalization, what are 09:58:09
11 you talking about? 09:58:12
12 A A working integrated circuit. 09:58:12
13 Q Okay. Can the transistor be finalized, in your 09:58:16
14 understanding of what finalized is, before it is part of a 09:58:21
15 working integrated circuit? 09:58:26
16 A So -- okay. So if we just go to look at how MOS 09:58:27
17 devices are used, there's devices where the transistor 09:58:34
18 itself, like a power MOSFET, can be put into practical 09:58:40
19 things. And they have nothing to do with the designs in 09:58:45
20 any of these, '847 or anything else. These are CMOS 09:58:48
21 MOSFETs, you know, that have to be in a deeply scaled 09:58:54
22 technology to create digital integrated circuits, right? 09:58:58
23 So that's why even the practical end, an abstract 09:59:02
24 sense of finalization doesn't make sense. Because if I 09:59:06
25 have a power MOSFET -- which are not any of these devices, 09:59:10

1 and these devices wouldn't be used as a power MOSFET -- 09:59:13
2 then that finalization is different than if I'm looking at 09:59:17
3 these devices, which have to be incorporated into an 09:59:21
4 integrated circuit, and they are being used at highly 09:59:25
5 scaled, high density, with interconnects to make a circuit 09:59:29
6 in some sort of, you know, application or a whole entire 09:59:33
7 integrated circuit at the end. 09:59:40

8 Q Is the structure device -- withdrawn. 09:59:41

9 Is the structure described in Chen ready to be 09:59:48
10 connected to other components before the source/drain have 09:59:52
11 been silicided? 09:59:59

12 A Let me unpack that. Is the... you're -- you're 10:00:01
13 asking, does Chen talk about how to finalize its use into 10:00:09
14 circuits? It doesn't discuss that. 10:00:14

15 Q I'm just saying if you look at -- if you look at 10:00:16
16 Figure 5, there's been no silicide of the source/drain, 10:00:21
17 right? 10:00:28

18 A I would have to go back and look at the process 10:00:29
19 flow... I mean, obviously, it's got a raised source/drain 10:00:33
20 and -- and everything. I need to look at the sequence. 10:00:36
21 But I... I can trust you. 10:00:45

22 Q Okay. Well, let's just say that it doesn't. In 10:00:49
23 your view, is the device in Figure 5, without the silicide 10:00:57
24 on the source/drain, ready to be connected up to other 10:01:04
25 components in an integrated circuit? 10:01:08

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1 A So I would say that the '847, Chen, and Lan, none 10:01:11
2 of them are ready to be connected with, you know, final 10:01:20
3 back-end materials or something. 10:01:26
4 Q Okay. And you said earlier that in your view, 10:01:27
5 when the gate in Chen is metal, one would not silicide the 10:01:36
6 gate, right? 10:01:42
7 A Correct. 10:01:43
8 Q Chen never says, When the gate is metal, don't 10:01:43
9 perform the silicide process. Right? 10:01:51
10 A Correct. But of course, you know, a POSITA would 10:01:53
11 know, if I have a metal gate, I'm not going to get 10:01:59
12 silicide -- I mean, it's not physical, right? I... I'm 10:02:02
13 not going to get silicide if I have a metal gate. 10:02:07
14 Q And Chen never says to retain the cap layer. The 10:02:10
15 only embodiment in Chen described is to remove the cap 10:02:17
16 layer, right? 10:02:22
17 A No. It says... from the perspective of the prior 10:02:22
18 art, you know, Chen, it says, To finish a device according 10:02:36
19 to an embodiment of the invention, the method forms 10:02:43
20 sidewall spacers from the second protective layer, as in 10:02:48
21 Figure 5. The sidewall spacers exposes an upper portion 10:02:52
22 of the hard mask, while sealing regions on the edges of 10:02:57
23 the gate layer. 10:03:03
24 So according to Chen, that's a final version from 10:03:06
25 the -- from this perspective. But -- but it has to go 10:03:09

1 through other steps, as I've said before, if it's going to 10:03:14
2 be in an integrated circuit, right? 10:03:18
3 Q And one of those steps in Figure 6 is to remove 10:03:20
4 the hard mask, right? 10:03:25
5 A One -- that's another preferred embodiment. And 10:03:26
6 of course, like I said, because of the physics involved, 6 10:03:34
7 would be used if you had to silicide the gate. Because 10:03:39
8 you have to have exposure to a polysilicon in order to 10:03:43
9 have a silicide form with a -- with a metal. 10:03:48
10 Q Chen never says anything about when continuing on 10:03:51
11 in the processing, as you've described, to make it 10:03:59
12 functional, affirmatively retaining the cap layer, the 10:04:01
13 hard mask 503, right? 10:04:08
14 A I mean, it -- it doesn't have to. It just says a 10:04:13
15 final embodiment is Figure 5, from its perspective, right? 10:04:16
16 Q Right. But as we discussed, that's not final in 10:04:22
17 the sense of being able to use it, right? 10:04:25
18 A It's not final in terms of all these devices go 10:04:26
19 through subsequent processing to -- to make working 10:04:29
20 integrated circuits. So these intermittent embodiments 10:04:36
21 are what they're talking about. And so from my 10:04:42
22 perspective as an expert, I'm just saying, Look, these 10:04:44
23 intermediate embodiments show all the features in Chen, 10:04:48
24 Ian, the same as the '847, right. 10:04:55
25 Q And in going from Figure 5 to a functional 10:05:04

1 transistor, whereas one method involves stripping the hard 10:05:08
2 mask, there is no explicit disclosure in Chen of any 10:05:13
3 subsequent processing after Figure 5 that retains the hard 10:05:17
4 mask; is that correct? 10:05:23

5 A I mean, Chen, as I said, there's two final 10:05:23
6 embodiments, the 5 and the 6. One has the cap layer, one 10:05:32
7 doesn't have the cap layer. Downstream, there are many 10:05:35
8 things that can happen, as you were actually asking me 10:05:39
9 before, the numerous interfaces and dielectrics and other 10:05:45
10 metals that would be used. And so either 5 or 6 could 10:05:50
11 have a -- a future of many different things as you go 10:05:53
12 towards the integrated circuit fabrication. 10:05:57

13 Q Right. One of those pathways is to continue on 10:05:59
14 to Figure 6 and strip the hard mask, right? 10:06:05

15 A I would say you could use the Figure 6 embodiment 10:06:07
16 if you wanted to, and -- and in effect, if you were -- had 10:06:09
17 a poly gate, wouldn't use embody -- you would do number 6 10:06:18
18 in order to make silicide, if you're making silicide. You 10:06:23
19 don't have to make silicide if you have doped moly, right? 10:06:27

20 So -- and then you go on to -- and yet do all the 10:06:32
21 other things we talked about, right? Like there's some 10:06:36
22 other processes to make interconnects and all that. 10:06:38

23 Q Do you view the siliciding of the source/drain 10:06:42
24 described in Chen as part of Figure 5 or Figure 6 or 10:06:47
25 neither? 10:06:53

1 A I mean, I look at Figure 5 as having all the 10:06:53
2 elements for '847. So I don't think the '847 has silicide 10:07:07
3 either mentioned in the... in the -- the beginning either, 10:07:15
4 I think. 10:07:19

5 But, yeah, I mean, if it doesn't -- let me put it 10:07:21
6 this way, instead of searching around. If it doesn't have 10:07:27
7 the silicide on the source or drain, it is a total 10:07:32
8 possibility you could make this, silicide on the source 10:07:36
9 and drain afterwards in order to build a circuit that has 10:07:43
10 lower access resistance. 10:07:45

11 Q And in that Column 6 disclosure that we talked 10:07:47
12 about, one method of continuing to process the design is 10:07:55
13 to silicide the gate and the source/drain. But there's 10:08:06
14 never any embodiment discussed where you just silicide the 10:08:10
15 source/drain, not the gate, right? 10:08:16

16 A I -- I think in that -- in that area, yes. But 10:08:17
17 of course if you have a metal gate like in 3, right, then 10:08:24
18 of course, you're not forming a silicide, right? 10:08:28

19 Q Chen doesn't say that, right? You're saying 10:08:31
20 that? 10:08:35

21 A Well, a POSITA says, well, if I have to make a 10:08:35
22 metal gate, right, I'm not going to do the silicide 10:08:38
23 process. And that's, like, both physics and experience 10:08:41
24 from a POSITA would know that, right? 10:08:44

25 Q I'm just saying Chen doesn't say that, right? 10:08:46

1 A Oh, yeah, I mean, there's lots of physical laws 10:08:49
2 and things that are done everyday that Chen doesn't talk 10:08:53
3 about. 10:08:56
4 Q And to be clear, Chen doesn't describe an 10:08:56
5 embodiment in which the gate is retained explicitly, 10:09:01
6 right? 10:09:06
7 A In what -- what are you saying? A gate? The 10:09:06
8 gate's there. 10:09:12
9 Q Right. Chen doesn't describe an embodiment in 10:09:13
10 which the gate cap is explicitly retained, correct? 10:09:16
11 A In Figure 5. 10:09:19
12 Q I mean, okay, Chen doesn't describe an embodiment 10:09:24
13 that could actually be used and connected up to other 10:09:27
14 components which the gate cap is retained, right? 10:09:31
15 A So again, I mean, I think all these, '847, Chen, 10:09:33
16 Lan, they all have intermediate embodiments, MOSFET 10:09:43
17 structures. That's what we're talking about. All of them 10:09:52
18 have to move forward and have other processes done to them 10:09:53
19 to make them useful and what we know are practical scaled 10:09:56
20 CMOS circuits. 10:10:01
21 And so what we are doing here is looking at all 10:10:03
22 these intermediate embodiments, including '847, and 10:10:08
23 saying, okay, '847 has this patent on it, which is the 10:10:14
24 intermediate embodiment with all these claims. Are they 10:10:18
25 similar to other intermediate embodiments like Lan and 10:10:21

1 Chen? And the answer is, of course, yes. And so all of 10:10:25
2 them would have to have different things done, which is 10:10:31
3 why the cap layer is really a ridiculous thing, actually, 10:10:33
4 because, you know, you're going to put the cap layer in 10:10:36
5 there even if -- even if it's removed, you're going to put 10:10:39
6 it back in because you don't want to get shorts, right? 10:10:41
7 So there's so many things that could happen 10:10:45
8 downstream that I think -- I think a POSITA easily, like, 10:10:48
9 no problem, looking at Chen and Lan -- '847 is the 10:10:52
10 intermediate embodiment -- would say they're the same 10:10:56
11 thing. 10:11:01
12 Q Now, when the gate is polysilicon in Chen, Chen 10:11:01
13 never says that there should be some polysilicon gate 10:11:17
14 transistors that should be silicided and some polysilicon 10:11:23
15 gate transistors that should not be silicided, right? 10:11:28
16 A You mean, like, in words in the specification, or 10:11:32
17 you mean in the fact that he talks about a metal gate, 10:11:38
18 talks about a silicide gate, or, you know, so -- and they 10:11:41
19 require different processes. He talks about the silicide 10:11:50
20 one, as you pointed out, when using the metal gate 10:11:53
21 obviously, relying in a POSITA knowing that if you have a 10:11:58
22 metal gate, you're not going to do silicide on it. 10:12:04
23 So I don't think he -- he talks about those 10:12:06
24 embodiments in the specification, but he doesn't -- but he 10:12:09
25 doesn't talk about one versus the other or anything. He's 10:12:13

1 just saying that, you know, you could have a metal gate. 10:12:19
2 He talks a lot about the silicide version. 10:12:22
3 Q Right. Set aside the metal gate. I just want to 10:12:25
4 talk about polysilicon gate. 10:12:30
5 So when the gate is polysilicon, Chen says you 10:12:31
6 perform silicide on that gate by removing the cap and then 10:12:37
7 siliciding the polysilicon gate, correct? 10:12:42
8 A Yeah, that's the section we talked about. Yeah. 10:12:44
9 Q And it never says or suggests if the gate is 10:12:47
10 polysilicon, you should not perform that process of 10:12:52
11 silicide? 10:12:57
12 A I mean, this goes back to the same thing that, 10:12:57
13 you know, in number 3, a doped polysilicon gate can have 10:13:08
14 the same resistivity as a metal. So therefore, in that 10:13:16
15 case, whether you silicide or not, you know, is kind of 10:13:24
16 questionable, right? But if you have undoped polysilicon, 10:13:25
17 then that embodiment that you're talking about has to 10:13:29
18 happen. You have to have the silicide. 10:13:33
19 Q Does Chen say whether its polysilicon is doped or 10:13:37
20 not sufficiently -- 10:13:41
21 A It says it's polysilicon, and, yeah, a POSITA 10:13:42
22 would know that, well, if I can get polysilicon to be high 10:13:45
23 enough doped depending on the application, then I may not 10:13:51
24 need silicide. 10:13:56
25 Q Okay. But Chen says when the gate is 10:13:57

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1 polysilicon, you do silicide the gate? 10:14:00

2 A Yeah. And I think a POSITA would know that if -- 10:14:02

3 that would be the case if polysilicon is too low doped, 10:14:05

4 right, which is often the case. 10:14:09

5 MR. DOKHANCHY: Okay. That's all the questions I 10:14:22

6 have. If there's any redirect, we can continue now or 10:14:23

7 take a break. I'll just reserve my right to recross, but 10:14:27

8 that's it for my affirmative questions. 10:14:31

9 MR. LONG: Sure. Why don't we take a break. We've 10:14:39

10 been going a bit anyway. And let me see if I have 10:14:41

11 anything, and also a bio break. 10:14:44

12 MR. DOKHANCHY: Okay. Do you want to come back in ten 10:14:46

13 minutes, five, whatever you want? 10:14:50

14 MR. LONG: Yeah, let's go off the record first. 10:14:51

15 THE VIDEOGRAPHER: We are going off the record. The 10:14:54

16 time on the video monitor is 10:14. 10:14:56

17 (Recess taken.) 10:36:13

18 THE VIDEOGRAPHER: We are going back on the record. 10:36:13

19 The time on the video monitor is 10:37. 10:37:13

20 EXAMINATION 10:37:13

21 BY MR. LONG: 10:37:13

22 Q Thank you, Professor Fitzgerald. I'm just going 10:37:19

23 to ask you a few questions. Hopefully it won't take too 10:37:19

24 long. 10:37:19

25 A Okay. 10:37:19

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1 Q Do you recall being asked some questions earlier 10:37:25
2 about polysilicon and metal gate electrodes? 10:37:32
3 A Yes. 10:37:36
4 Q What types of materials does the '847 patent 10:37:37
5 disclose for use as its gate electrodes? 10:37:38
6 A It has, I think, both polysilicon and silicide. 10:37:41
7 Q Okay. So if we look at Column 3, line 6 of 10:37:51
8 the -- 10:37:51
9 A '847. 10:37:51
10 Q -- '847 patent. 10:37:59
11 A All right. Sorry. Say that again. 10:38:06
12 Q Sure. Column 3, the sentence begins on 6. 10:38:13
13 A Okay. 10:38:20
14 Q So what materials does it disclose there? 10:38:20
15 A It says that the dielectric layer 210 is 10:38:24
16 comprised of things like silicon oxide or nitride, and 10:38:31
17 then the conductive layer is polysilicon or metal silicide 10:38:40
18 and cap layers 213. 10:38:41
19 Q Okay. And which one of those is the gate 10:38:45
20 electrode material? 10:38:50
21 THE STENOGRAPHIC REPORTER: I'm sorry. I didn't hear 10:38:50
22 that, Mr. Long. It's hard to hear you. Please repeat. 10:38:50
23 MR. LONG: Sorry. Yes. 10:38:51
24 BY MR. LONG: 10:38:51
25 Q So which materials describe the gate electrode in 10:38:53

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1 the '847 patent? 10:39:01

2 A And it's the conductive material such as 10:39:01

3 polysilicon or metal silicide. 10:39:06

4 Q Is metal silicide a metal? 10:39:08

5 A Yes. 10:39:13

6 Q Okay. And in your view, how do the materials 10:39:13

7 disclosed for the gate electrode in the '847 patent 10:39:13

8 compare to the materials disclosed -- (audio technical 10:39:13

9 difficulty) -- the gate electrode in the Lan reference? 10:39:24

10 THE STENOGRAPHIC REPORTER: Sorry. Mr. Long, I can't 10:39:24

11 hear you. I don't know what you're saying. I'm sorry. 10:39:25

12 BY MR. LONG: 10:39:28

13 Q How do the materials disclosed for use as the 10:39:29

14 gate electrode in the '847 patent compare to the materials 10:39:32

15 disclosed for use as the gate electrode in Lan? 10:39:35

16 MR. DOKHANCHY: Objection; leading. 10:39:41

17 THE WITNESS: The materials are the same, metal and 10:39:42

18 poly. 10:39:47

19 BY MR. LONG: 10:39:47

20 Q Okay. Same question for the Chen reference. How 10:39:48

21 do the materials disclosed for use as the gate electrode 10:39:51

22 in the '847 patent compare to the materials disclosed for 10:39:55

23 use as the gate electrode in Chen? 10:39:58

24 A Yes, same thing, which is that the Chen 10:40:03

25 reference, as I said before, is polysilicon and metal 10:40:07

1 gate. 10:40:11

2 Q Okay. Now, do you recall earlier being asked 10:40:12

3 some questions about whether certain structures are final? 10:40:20

4 A Correct, yes. 10:40:23

5 Q Okay. I'll try to avoid that terminology and be 10:40:24

6 a little more specific. But could you turn to Figure 5 in 10:40:29

7 the '847 patent? 10:40:32

8 A Figure 5 of the '847. Yes. 10:40:32

9 Q Okay. Looking at the embodiment shown in 10:40:41

10 Figure 5 of the '847 patent, is it possible at that stage 10:40:45

11 of fabrication to operate the gate? 10:40:49

12 A Is it in this stage -- 10:40:53

13 Q Is it possible at this stage of fabrication to 10:40:55

14 operate the gate? 10:40:58

15 A No. 10:40:59

16 Q Looking at Figure 5, is it possible at this stage 10:41:00

17 of fabrication to operate the source and drain? 10:41:05

18 A No. 10:41:08

19 Q Okay. Could you turn to Figure 14 of the '847 10:41:08

20 patent, please? 10:41:12

21 A Figure 14 of the '847. Yes. 10:41:13

22 Q Looking at the embodiment shown in Figure 14 of 10:41:22

23 the '847 patent, is it possible at that stage of 10:41:26

24 fabrication to operate the gate? 10:41:33

25 A No. 10:41:34

1 Q Is it possible -- looking at the embodiment shown 10:41:35
2 in Figure 14 of the '847 patent, is it possible at that 10:41:37
3 stage of fabrication to operate the source and drain? 10:41:41
4 A No. 10:41:44
5 Q Okay. Does the '847 patent describe any 10:41:45
6 subsequent processing steps performed after the stage of 10:41:50
7 fabrication we see in Figures 5 and 14? 10:41:53
8 A No. 10:41:56
9 Q Does the '847 patent say not to remove the cap 10:41:57
10 after the stage of fabrication shown in Figures 5 and 14? 10:42:01
11 A No. 10:42:06
12 Q Does Lan disclose a MOS transistor structure at 10:42:06
13 the same stage of fabrication as the embodiments of the 10:42:12
14 '847 patent that satisfies Claim 2? 10:42:16
15 A Yes. 10:42:18
16 MR. DOKHANCHY: Objection; leading. 10:42:19
17 BY MR. LONG: 10:42:20
18 Q Does Chen disclose a MOS transistor structure at 10:42:21
19 the same stage of fabrication as the embodiments of the 10:42:25
20 '847 patent that satisfies Claim 2? 10:42:29
21 A (Inaudible). 10:42:31
22 MR. DOKHANCHY: Same objection. 10:42:31
23 THE WITNESS: Sorry. I'll pause more. 10:42:31
24 MR. LONG: So no further questions. We reserve any 10:42:36
25 right for any recross should there be any... 10:42:40

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1 THE STENOGRAPHIC REPORTER: I didn't hear your answer, 10:42:45
2 Professor Fitzgerald, at all to that. 10:42:47
3 THE WITNESS: That was a yes and yes. 10:42:48
4 THE STENOGRAPHIC REPORTER: Thank you. 10:42:50
5 MR. DOKHANCHY: No questions for me. 10:42:52
6 THE STENOGRAPHIC REPORTER: Okay. Thank you. Before 10:43:01
7 we go off, I just want to confirm your order, Mr. Long, 10:43:02
8 for the rough draft and the regular turnaround for your 10:43:07
9 copy. 10:43:10
10 MR. LONG: We'll take whatever, I guess, the patent 10:43:10
11 owner is doing. 10:43:12
12 THE STENOGRAPHIC REPORTER: Okay. All right. 10:43:14
13 And, Reza, we have your transcript order as well. 10:43:20
14 So we can go off the record now. Thank you. 10:43:22
15 MR. DOKHANCHY: Okay. 10:43:24
16 THE VIDEOGRAPHER: Okay. We're going off the video 10:43:24
17 record. The time on the video monitor is 10:43. 10:43:27
18 (WHEREUPON THE DEPOSITION WAS
19 CONCLUDED AT 10:43 A.M.)
20
21
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3 98, inclusive.

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EUGENE FITZGERALD, PH.D.

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2

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7 Case Title: TAIWAN V. MARLIN
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CERTIFICATE OF SHORTHAND REPORTER/STENOGRAPHER

I, Christa Yan, Certified Shorthand/Stenographic Reporter
within and for the State of California do hereby certify:

That Eugene Fitzgerald, the Witness whose deposition is
hereinbefore set forth, was duly sworn by me before the
commencement of such deposition and that such deposition
was taken before me and is a true record of the testimony
given by such witness.

I further certify that both parties were represented by
counsel at the remote deposition.

I further certify that the deposition of Eugene Fitzgerald
occurred remotely on January 6, 2026, commencing at
7:32 a.m. to 10:43 a.m., Pacific Standard Time.

I further certify that I am not related to any of the
parties to this action by blood or marriage, I am not
employed by or an attorney to any of the parties to this
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otherwise, in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 8th
day of January 2026.



CERTIFIED SHORTHAND/STENOGRAPHIC REPORTER
IN AND FOR THE STATE OF CALIFORNIA

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