

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd. and Apple Inc.,

Petitioners

v.

Marlin Semiconductor Ltd.

Patent Owner

Patent No. 7,745,847 B2
Filing Date: August 9, 2007
Issue Date: June 29, 2010

Title: METAL OXIDE SEMICONDUCTOR TRANSISTOR

Inter Partes Review No. IPR2025-00847

PETITIONERS' REPLY

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Exhibit	Description
Ex-1001	U.S. Patent No. 7,745,847 B2 to Tseng et al. (“’847 Patent”).
Ex-1003	Declaration of Dr. Eugene Fitzgerald, Ph.D.
Ex-1004	Curriculum Vitae of Dr. Eugene Fitzgerald, Ph.D.
Ex-1005	U.S. Patent No. 7,935,590 B2 to Lan et al. (“Lan”).
Ex-1006	U.S. Patent No. 7,026,689 B2 to Liaw (“Liaw”).
Ex-1007	U.S. Patent No. 7,605,407 B2 to Wang (“Wang407”).
Ex-1008	U.S. Patent No. 7,449,753 B2 to Wang et al. (“Wang753”)
Ex-1009	U.S. Patent No. 7,591,659 B2 to Chen et al. (“Chen”).
Ex-1011	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted).
Ex-1024	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> , Ch. 12: Metallization (2001) (excerpted).
Ex-1201	Mr. McAlexander Docket Navigator Report: Cases by Year
Ex-1202	Mr. McAlexander Docket Navigator Report: List of Declarations
Ex-1203	Mr. McAlexander Docket Navigator Report: Declarations by Year
Ex-1204	Mr. McAlexander Deposition Transcript

Exhibit	Description
Ex-1205	Complaint, <i>Longitude Licensing Ltd. & Marlin Semiconductor Ltd. v. Lenovo Grp. Ltd.</i> , No. 2:25-cv-171 (E.D. Tex. Feb. 13, 2025).
Ex-1206	Complaint, <i>Longitude Licensing Ltd. & Marlin Semiconductor Ltd. v. Apple Inc.</i> , No. 1:25-cv-215 (W.D. Tex. Feb. 13, 2025).
Ex-1207	The American Heritage College Dictionary (4th ed. 2004, excerpted).
Ex-1208	U.S. Patent Appl. Pub. No. 2005/0112858 A1 to Yuan et al.
Ex-1209	U.S. Patent Appl. Pub. No. 2005/0164460 A1 to Mathew et al.
Ex-1210	U.S. Patent Appl. Pub. No. 2004/0113171 A1 to Chiu et al.
Ex-1215	Chen's FIG. 3, as annotated by J. McAlexander during deposition.

***NOTE: All citations herein to stand-alone page numbers identify stamped page numbers of the cited exhibit, not page numbers of the original reference.**

I. INTRODUCTION

Marlin found little to dispute. Across all challenged claims, the Patent Owner’s Response (“POR”) addressed just three claim elements—[1b], [1e], and [2c]. And Marlin’s positions regarding those elements lack merit.

First, Marlin’s general challenge to element [1b] misapplies settled case law. Offering no new authorities, evidence, or reasoning, the POR merely reiterates the same legal argument already rejected in the Board’s Institution Decision (“ID”).

Second, Marlin’s challenge to Chen’s disclosure of elements [1b] and [1e] hinges on tacit and unsupported positions. Marlin assumes that (1) “next to” means *entirely* next to and (2) “the relative sides of the gate” excludes the relative sides of the gate conductive layer. Nothing supports either position.

Third, Marlin does not dispute that Lan, the Lan-Liaw combination, or Chen discloses a structure comprising all elements of claim 2, including the “cap layer” of element [2c]. Marlin instead argues the cap layer must be removed, a position that is both factually incorrect and insufficient to distinguish the prior art. None of those references requires cap layer removal; to the contrary, they expressly disclose and/or suggest retaining the cap layer. Regardless, nothing precludes an intermediate (i.e., transitional) structure from disclosing claim 2, even if the cap layer may optionally be removed thereafter.

Thus, as further explained below, Marlin’s positions are not persuasive.

II. MARLIN SIMPLY REPEATS ITS LEGALLY AND FACTUALLY FLAWED POR CHALLENGES TO ELEMENT [1B], WHICH THE BOARD ALREADY REJECTED

The Petition relies on drawings to show a spatial relationship—that various epitaxial layers extend above a substrate surface. Marlin argues it is “wrong as a matter of law” to rely on drawings to show this. (Paper 15 (“POR”) at 21.) For reasons the Board correctly noted (Paper 12 (“ID”) at 14-20), Marlin is incorrect. And Marlin’s POR offers no reason to reverse course.

Marlin’s authorities are inapposite. They stand for the proposition that “precise” or “actual” dimensions may not be extracted from drawings not to scale. *See Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1351 (Fed. Cir. 2013); *Nystrom v. TREX Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005); *Hockerson-Halberstadt, Inc. v. Avia Grp. Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000); *In re Wright*, 569 F.2d 1124, 1127 (CCPA 1977). But that is not how the Petition uses the prior-art drawings. (See Petition at 20-21, 47-48, 63-64, 71-72.) Marlin’s authorities thus do not control.

Marlin criticizes Petitioners for citing “only a single non-precedential decision as supposedly supporting their attempt to rely on patent drawings that are not [to] scale.” (POR at 23.) But Petitioners did not cite that case for its precedential value; they cited it because a Federal Circuit panel succinctly summarized a known distinction between permissible and impermissible uses of drawings: “*As we have*

previously explained, patent drawings may be useful in shedding light about the general shapes and relative sizes of elements of the claimed invention, as well as their *spatial relations* to one another.” *Regents of Univ. of Cal. v. Satco Prods., Inc.*, No. 2023-1356, 2024 WL 4972639, at *3 (Fed. Cir. Dec. 4, 2024) (nonprecedential) (emphases added). The Petition’s use of drawings to show the spatial relations between epitaxial source/drain regions and the substrate surface is thus permissible.

The distinction stated in *Regents* is not subject to reasonable debate. It finds support in precedential cases stretching back to the 1940s, at least. *See, e.g., Saffran v. Johnson & Johnson*, 712 F.3d 549, 559 (Fed. Cir. 2013) (figures showing “a spray nozzle depositing a continuous, unbroken sheet that spans open gaps between individual bone fragments”); *Krippelz v. Ford Motor Co.*, 667 F.3d 1261, 1268 (Fed. Cir. 2012) (figures showing “light extending from various lamps to the surface of the ground”); *Koito Mfg. Co. v. Turn-Key-Tech, LLC*, 381 F.3d 1142, 1154-55 (Fed. Cir. 2004) (figure showing “that flow channel 6 is ‘significantly thicker and wider’ than the adjacent mold cavity 2”); *In re Schreiber*, 128 F.3d 1473, 1478 (Fed. Cir. 1997) (“[A]n embodiment according to Harz (Fig. 5) and the embodiment depicted in figure 1 of Schreiber’s application have the same general shape.”); *In re Mraz*, 455 F.2d 1069, 1072 (CCPA 1972) (explaining “the teachings of patent drawings, even as to features unexplained by the specification, [may be] dispositive”); *In re Pentz*, 162 F.2d 226, 229 (CCPA 1947) (“There is nothing in either appellant’s

drawing or specification which distinguishes the shape or form of the fluid container from the form shown in the drawings of the England patent and of the Barrett patent.”); *In re Jennings*, 134 F.2d 492, 494 (CCPA 1943) (figures showing “the porous member extending from the water to the root soil and thence to the atmosphere”).

The distinction in *Regents* is a corollary to the settled rule that inventions may be disclosed through “words, structures, **figures, diagrams**, formulas, etc.” *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) (emphasis added). Drawings alone suffice so long as “they describe what is claimed.” *Cooper Cameron Corp. v. Kvaerner Oilfield Prods., Inc.*, 291 F.3d 1317, 1322 (Fed. Cir. 2002); *see also Wang Lab’ys, Inc. v. Toshiba Corp.*, 933 F.2d 858, 866 (Fed. Cir. 1993) (“drawings alone” may suffice). Here, the drawings describe what is claimed. As Dr. Fitzgerald explains, such drawings had been “a staple in the field for many decades.” (Ex-1003 ¶110.) “[I]f such a figure shows one structural feature being higher than another, especially extending above the substrate, a [POSITA] would have understood that positional relationship to be a relevant detail.” (*Id.*)

This also accords with the state of the art at the time. The Petition explains: “Ensuring adequate strain transfer commonly involved growing epitaxial source/drain regions that extended above the substrate.” (Petition at 4; *see also* Ex-1003 ¶54.) Even “the two most recent generations of high-volume commercial

devices” included that feature. (Petition at 4; *see also* Ex-1003 ¶111 (“[E]pitaxial source/drain stressors extending above the substrate surface (as [the prior art] shows) was a typical and expected feature of prior-art strained channel technology.”), ¶206 (same), ¶262 (same), ¶292 (same).)

Moreover, Lan’s Fig. 8 and Wang753’s FIG. 13 show the epitaxial source/drain regions of the PMOS devices are raised, whereas the non-epitaxial source/drain regions of the NMOS devices are not. That distinction was no accident. And it confirms a POSITA would have understood more generally that raised epitaxial source/drain regions in such drawings was deliberate and meaningful.

Marlin offers no contrary evidence, just a conclusory assertion by its expert that raised epitaxial layers were somehow “atypical.” (Ex-2001 ¶52.)

Marlin’s insistence that “Petitioners’ interpretations of the drawings are inconsistent with, and not supported by, the references” is also baseless. (POR at 24.) As the ID correctly notes, growing epitaxy “in” a recess does not mean it cannot extend above the substrate surface. (*See* ID at 20.) That is what the ’847 Patent’s figures show. (*See* Ex-1001 at FIGS. 5, 14.) And it is how Marlin alleged infringement. (*See* Ex-1205 at 36-40; Ex-1206 at 27-35.) Marlin cannot maintain the opposite for prior art.

At bottom, Marlin does not dispute that the drawings in Lan, Wang407, Wang753, or Chen depict what element [1b] recites: “two raised epitaxial layers

positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate.” Because those drawings suffice to disclose element [1b], Marlin’s challenge fails.

III. THE CHEN GROUNDS SATISFY ELEMENTS [1B] AND [1E]

Relying on the annotations below, Marlin argues that Chen’s epitaxial layers and doped regions are “under the gate dielectric layer” and not “next to the relative sides of the gate.” (POR at 29-30.) Marlin’s position fails. As explained below, Marlin tacitly applies the claims in two unduly limiting ways, neither of which comports with the claim language.

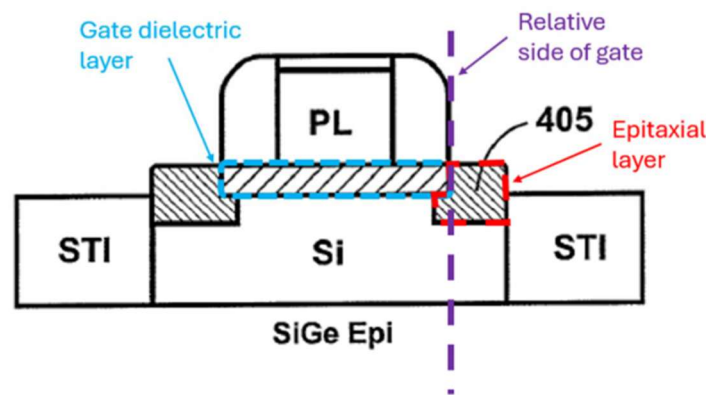


FIGURE 3

A. The Phrase “Next To” Does Not Mean Entirely Next To

At the outset, Marlin’s own annotations (see above) contradict its position. They show Chen’s epitaxial layer (red) located “next to” what Marlin labels the “Relative side of gate” (purple). (See POR at 29.) Even Marlin’s own expert concedes that the epitaxial layer is substantially located “to the right of that gate

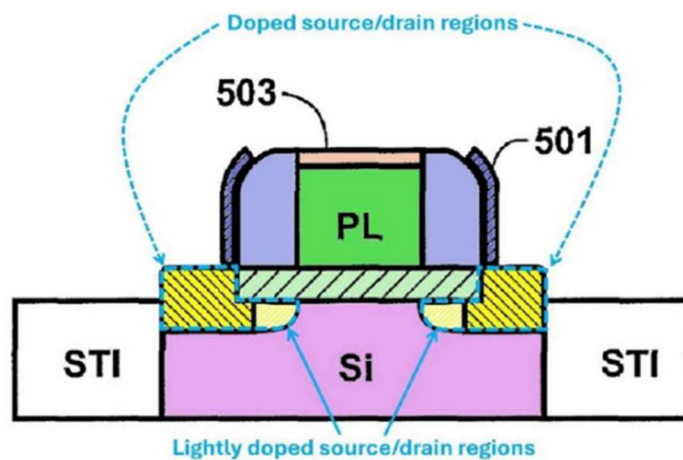
oxide.” (Ex-1204 at 60:17-61:8.) And he testified that “next to” means “beside.” (*Id.* at 61:17-20, 71:2-4.) It should be beyond dispute that the “Epitaxial layer” above includes portions located ***beside*** what Marlin labeled the “Relative side of gate.”

Further weakening Marlin’s position, its expert acknowledges that the phrase “next to” encompasses the phrase “adjacent to.” (*Id.* at 71:5-19; *see also* Ex-1207 at 5-6 (defining “adjacent” as “Next to” and defining “next to” as “Adjacent to”).) And Chen expressly states that its epitaxial layers are “deposited in recessed regions ***adjacent to*** the channel region” under the gate. (Chen at 2:56-60 (emphasis added); *accord id.* at Abstract, 2:17-21, 2:42-47, 3:52-55, 5:9-59, 6:65-67, 8:25-26.) The inquiry should end there in Petitioners’ favor. (*See* Petition at 71-72.)

This is not a question of claim construction. Neither party has suggested that anything other than the plain meaning applies. Yet Marlin tacitly applies the phrase “next to the relative sides of the gate” in a way that requires the epitaxial layers to be ***entirely*** next to the relative sides of the gate. For example, Marlin’s expert testified that he applied element [1b] to require ***the entirety*** of the claimed “epitaxial layers” to be located beside the claimed gate “dielectric layer.” (*See* Ex-1204 at 62:3-17, 68:12-22.) That was inappropriate, as his own contradictory testimony demonstrates. The same phrase—“next to the relative sides of the gate”—also describes the location of the “two doped regions” in element [1e]. Despite his position regarding element [1b], Marlin’s expert admitted that this very same phrase

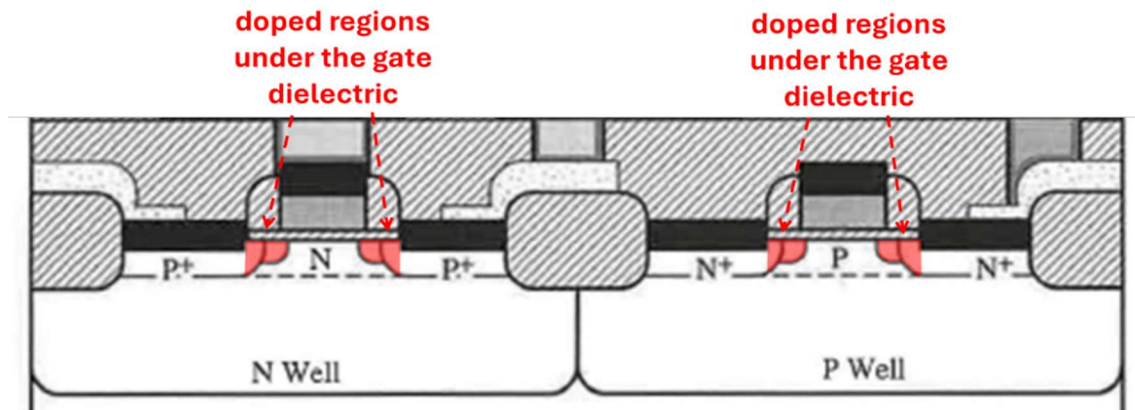
in element [1e] **does not** require the entirety of the “two doped regions” to be located beside the gate “dielectric layer.” (*See id.* at 69:4-71:1.) That blatant contradiction undermines the credibility of Marlin’s position regarding element [1b], not to mention its expert’s credibility.

Absent disavowal or lexicography, issues neither party has raised, the phrase “next to the relative sides of the gate” carries its ordinary meaning. Applying that ordinary meaning, Chen discloses “two raised epitaxial layers” and “two doped regions” located “next to” (i.e., adjacent to) what Marlin identified as the relative sides of the gate, as shown below. (*See* Petition at 71-72, 76-77.)



Seeking to justify its baseless position, Marlin contends that “positioning the doped region and epitaxial layer under the gate (as disclosed in Chen) increases the risk of an electrical or physical short.” (POR at 30.) Not only is Marlin’s position divorced from the claim language, but it would mean textbook MOSFET designs are somehow faulty. Yet, just like Chen, textbooks like the one below frequently show

the gate dielectric extending underneath the sidewall spacers and over part of the doped source/drain regions. (See Ex-1011 at Figs. 2-2 & 2-44; Ex-1024 at Fig. 9.27.)



Ex-1011, Fig. 2-44 (excerpted, annotated)

Thus, contrary to Marlin’s position, Chen’s structure is not some unusual design that “increases the risk of an electrical or physical short.” (POR at 30.) This aspect of Chen’s design was textbook. And, regardless, “teaching away is not relevant” since Chen itself discloses the claimed feature. *Krippelz*, 667 F.3d at 1269.

Nor does the ’847 Patent support Marlin’s position on this issue. According to the ’847 Patent, everything highlighted yellow in the left-hand figure below may be silicon oxide. (See Ex-1001 at 3:6-11, 3:56-58, 4:59-64, 6:28-30.) Similarly, Chen’s spacers are made of the same or similar material as the gate dielectric. (See Ex-1204 at 56:21-57:8.) As in the ’847 Patent, both can be made of silicon oxide. (See Chen at 2:8-10, 4:30-32, 4:51-53, 6:3-6.) Thus, in both Chen and the ’847 Patent, silicon oxide layers physically touching the gate electrode extend over part of the source/drain regions.

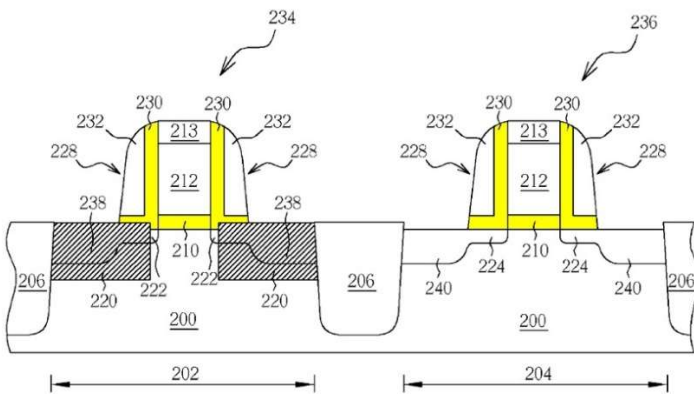


Fig. 5

'847 Patent, FIG. 5 (annotated)

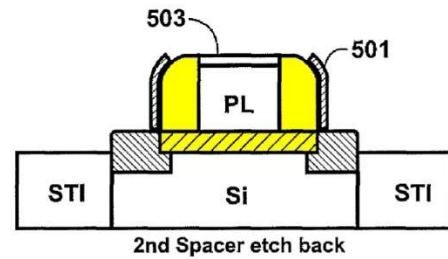


FIGURE 5

Chen, FIG. 5 (annotated)

The same insulating silicon oxide material is present above part of the source/drain regions, regardless of whether the spacers extend down to the substrate surface or whether the gate dielectric layer extends underneath them. Again, this is a textbook feature, not some questionable approach that risks short-circuiting.

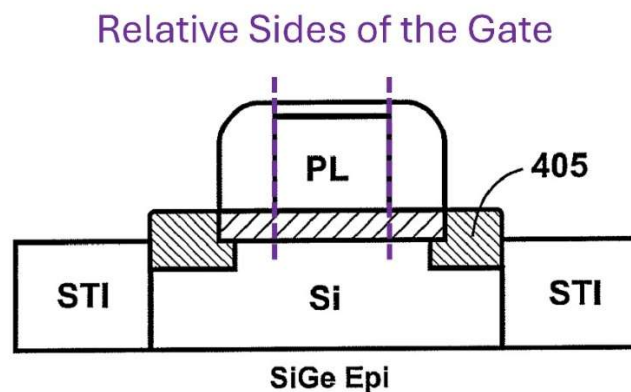
In sum, there is no basis for Marlin's tacit position that "next to" means *entirely* next to. Chen satisfies both elements [1b] and [1e], even under Marlin's narrow view of what constitutes "the relative sides of the gate." (See Petition at 71-72, 76-77.)

B. The Phrase "Relative Sides of the Gate" Encompasses the Relative Sides of the Gate Conductive Layer

Marlin's narrow view of what constitutes "the relative sides of the gate" is also flawed. The claims require only that "two raised epitaxial layers" and "two doped regions" lie next to "the relative sides of the gate." (See Ex-1001 at cl. 1.) Because the "gate" includes a gate "conductive layer" (*id.* at cl. 2), the plain meaning

of “the relative sides of the gate” encompasses the relative sides of the gate conductive layer.

As Marlin’s expert admits, Chen’s gate includes a gate conductive layer “PL.” (See Ex-1215; Ex-1204 at 55:3-18). Nothing precludes the edges of that gate conductor from being “the relative sides of the gate.”¹ For example, Chen teaches to “[f]orm a gate layer (e.g., polysilicon, metal) overlying the dielectric layer” and to “[p]attern the gate layer to form a *gate structure including edges (e.g., a plurality of sides or edges)*.” (Chen at 3:45-48 (emphasis added).) Chen further discloses “form[ing] sidewall spacers on *edges of the patterned gate layer*, as shown” below. (Chen at 4:49-51 (emphasis added); see also Petition at 72.) There is no principled reason why the phrase “the relative sides of the gate” should exclude these sides/edges in Chen (annotated below), and Marlin has not offered one.



¹ The phrase “the relative sides” has no antecedent basis in claim 1 and is not defined as any particular sides of the gate.

Chen's descriptions above also accord with textbooks. Plummer, for example, describes "Gate Formation." (Ex-1011 at 39-44.) As shown below, a gate dielectric is formed (*id.* at Fig. 2-24), followed by depositing a conductive layer (*id.* at Fig. 2-25).

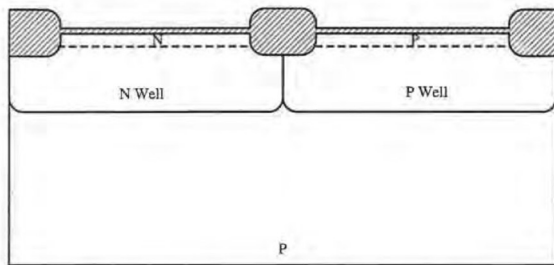


Figure 2-24 After etching back the thin oxide to bare silicon, the gate oxide is grown for the MOS transistors.

Ex-1011, Fig. 2-24

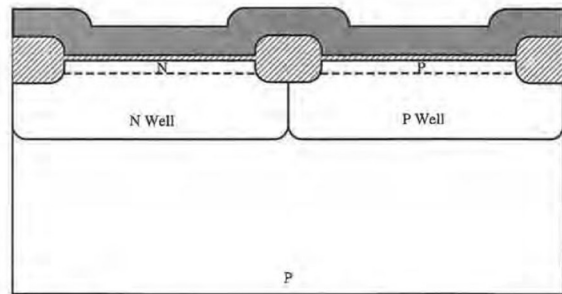


Figure 2-25 A layer of polysilicon is deposited. Ion implantation of phosphorus follows the deposition to heavily dope the poly.

Ex-1011, Fig. 2-25

The conductive layer is then etched "*to define the regions where MOS gates are located.*" (*Id.* at 43, Fig. 2-26 (caption).) As shown below, the edges of the gate conductors thus define relative sides of the gates, even though the gate dielectric layer has yet to be patterned. (*Id.* at Fig. 2-26; *see also id.* at Fig. 2-44.)

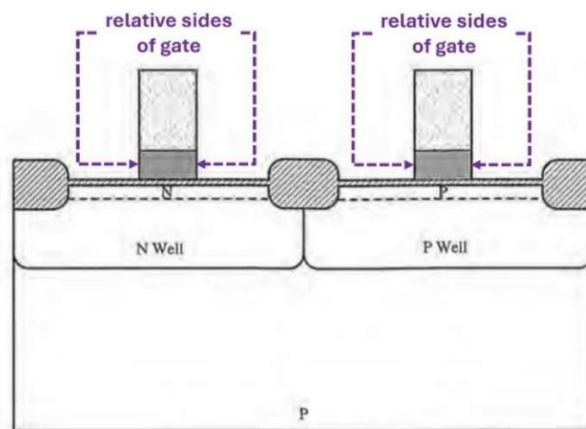


Figure 2-26 Photoresist is applied and mask 6 is used to define the regions where MOS gates are located. The polysilicon layer is then etched using plasma etching.

Ex-1011, Fig. 2-26 (annotated)

Understanding that “the relative sides of the gate” may include the sides of the gate conductive layer, there can again be no dispute that Chen satisfies [1b] and [1e]. (*See* Petition at 71-72, 76-77.)

In sum, Marlin’s challenge to Chen fails unless two things are true: (1) “next to” means *entirely* next to and (2) “the relative sides of the gate” excludes the sides of the gate conductive layer. Marlin is wrong on both points.

IV. THE LAN AND CHEN GROUNDS SATISFY ELEMENT [2C]

Element [2c] requires “a cap layer, positioned on the conductive layer.” Marlin does not dispute that Lan, Liaw, and Chen each disclose a cap layer. Marlin instead argues those cap layers must be removed. (*See* POR at 31-32, 44.) Marlin is wrong. As Section IV.A explains, Lan, Liaw, and Chen expressly disclose and/or suggest retaining their respective cap layers. And regardless, Marlin’s position does not even distinguish the prior art, as Section IV.B explains.

A. Marlin’s Allegations Regarding Cap Layer Removal Are Factually Incorrect

Lan, Liaw, and Chen each disclose the cap layer of element [2c]. None of them require cap layer removal. To the contrary, they expressly disclose and/or suggest retaining the cap layer. (*See* Petition at 37-39 (discussing Lan), 39-45 (discussing the Lan-Liaw combination), 80-82 (discussing Chen); Ex-2004 at 76:12-

78:14, 85:13-22, 89:19-24.) With no credible response, Marlin resorts to fighting the disclosures themselves.

1. Ground 1C: Lan discloses the claimed cap layer, and it would have been obvious to retain it

Lan discloses a “cap layer” as recited in [2c]. (*See* Petition at 34-39; Lan at 2:51-52, 3:32-34, 4:56-58, Figs. 4, 8, 12.) Marlin does not dispute that. Rather, Marlin argues the cap layer must be removed after further processing. (*See* POR at 31-36.) Marlin is wrong.

Marlin argues, for instance, that “[o]nce the recesses are formed, the cap layer would serve no additional purpose and would be removed.” (POR at 32.) Lan teaches the opposite. The cap layer remains intact after recess formation, specifically serving as an ion-implantation mask. (*See* Lan at 3:4-11, Figs. 4, 8, 12.)

Marlin then contends the cap “would need to be removed” because it would “block access” to the gate electrode, allegedly making the device “unworkable.” (POR at 33.) If that were true, then the ’847 Patent would lack utility for describing and claiming the same “unworkable” device. Marlin’s argument is thus baseless.

A POSITA would have understood that forming contacts to a metal gate electrode involves etching a contact hole through only part of the cap layer (which is a long stripe), not removing it entirely. (*See* Ex-1208 at [0022], Figs. 3, 4f (describing how to contact a metal gate 18 through a gate cap layer 19); Liaw at

6:35-38, FIG. 3A; Ex-2004 at 46:6-12 (describing “penetrations through the cap”), 53:1-13 (explaining “you don’t want an open gate so that then there’s a long line that could short on anything”).) Nothing about Lan’s structure is “unworkable.”

Marlin next resorts to irrelevant speculation, suggesting a POSITA might have removed the cap layer in Lan’s metal-gate embodiments to “diffuse additional metal.” (POR at 33; *see also id.* at 33-36.) But Petitioners did not argue it would have been *impossible* to remove the cap layer in a metal-gate embodiment or that cap layer retention would have been *necessary*. (See Petition at 35-45; Ex-2004 at 45:18-47:5.) Whether a POSITA might have removed the cap layer in some other hypothetical scenario is irrelevant. Obviousness does not require inherency.

Regardless, Marlin’s hypothetical is baseless. The only supposed evidence Marlin cites is Ex-2005, which does not even mention a cap layer, let alone describe removing a cap layer to diffuse additional metals.

Next, Marlin speculates that a POSITA would not have been deterred from subjecting the surface of a metal gate to silicidation. (See POR at 35-36; Ex-2003 ¶62.) That position is not just conclusory; it contradicts contemporaneous evidence. One prior-art reference explains, for example: “Selective removal of unreacted metal via wet etch procedures can ... result in unwanted removal or attack of an exposed metal gate structure, resulting in decreased word line resistance.” (Ex-1209 at [0005]; *accord* Ex-1210 at [0005], [0019].) As Marlin’s expert admits, this can cause

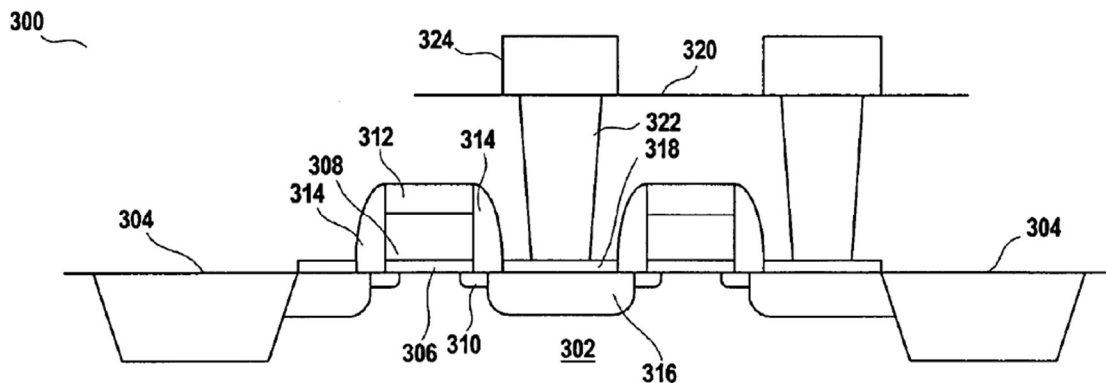
non-uniform switching and power distribution in an integrated circuit. (Ex-1204 at 83:21-84:15; *see also id.* at 82:17-20, 83:6-20, 84:16-85:21.) Additionally, he acknowledges that interface quality “plays a major role” in contact resistance (*id.* at 85:22-86:4), which could exacerbate such problems when exposing a metal gate to a metal etchant, regardless of gate thickness (*see* Ex-1003 ¶174, ¶325; Ex-1209 at [0005]; Ex-1210 at [0005], [0019]).

At bottom, Lan discloses the MOSFET structure of claim 2, and it provides the same level of disclosure as the '847 Patent. (*See, e.g.*, Ex-2004 at 59:11-24, 87:9-88:11, 94:5-15; Lan at Fig. 12.) Moreover, a POSITA would have found it obvious to retain Lan’s cap layer. (*See* Petition at 34-39.) Lan thus renders claim 2 obvious.

2. Ground 1D: Liaw expressly teaches to retain a cap layer like Lan’s, showing it would have been obvious

The Lan-Liaw combination includes a “cap layer” as recited in [2c], and it expressly teaches to retain that layer. (*See* Petition at 39-45; Liaw at Abstract, 1:6-9, 4:6-34, FIGS. 3A-3B; Lan at 2:51-52, 3:32-34, 4:56-58, Figs. 4, 8, 12.) Marlin incorrectly contends that (1) the cap layer must later be removed and (2) a POSITA would have lacked motivation to combine Lan with Liaw. (*See* POR at 37-41.) Marlin, however, misreads Liaw’s teachings and improperly compares dimensions between references based solely on drawings that are not to scale.

First, Marlin misreads Liaw’s disclosures. Liaw does not teach **removing** the cap layer for a gate contact. (*See* POR at 37.) Rather, Liaw teaches to “etch[] through” (i.e., form a hole in) the cap layer. (Liaw at 6:35-38; *see also* Ex-1208 at [0022]; Ex-2004 at 46:6-12.) Liaw uses the same phrase—“etch[] through”—to describe forming holes in inter-level dielectric layer 320 for conductive plugs 322, as shown below. (Liaw at 4:40-43.) And, as shown below, inter-level dielectric layer 320 is not completely removed when “etched through.” The same applies when cap layer 312 is “etched through.” (Liaw at 6:35-38.)



Liaw, FIG. 3A

When Marlin suggests that Liaw’s step 524 requires complete cap layer removal, it contradicts Liaw’s figures another way, too. As Liaw’s FIG. 3A shows above, cap layer 312 remains intact even after step 530, when “interconnect 324 is formed.” (Liaw at 6:40-42; *see also id.* at 6:16-42 (describing Liaw’s process steps “[w]ith reference to both FIGS. 3A and 5”).) This is well after step 524, indicating that cap layer 312 remains after being “etched through.” (*Id.* at 6:35-38; *see also id.*

at FIG. 5.) The “etched through” portion of cap layer 312 is simply not depicted in Liaw’s figures; it resides in a different cross-section. As Dr. Fitzgerald explains, a POSITA would have understood Liaw’s figures show only a single cross-section without the gate contact hole. (See Ex-2004 at 46:6-12 (describing “penetrations through the cap ... not shown”), 53:1-16 (explaining that “out of the plane of this, there’s all sorts of patterns and stuff”).

Marlin also misreads Liaw’s following statement: “While the cap layer 214 avoids the misalignment problem, it complicates the fabrication process and increases costs.” (Liaw at 3:47-49; *see also* POR at 41.) This statement criticizes “conventional MOS devices, as shown in FIGS. 2A and 2B,” which perform *silicidation* of *polysilicon gates*. (Liaw at 3:44-49; *see also id.* at 3:5-8.) Liaw proposes to *eliminate gate silicidation* by using *metal gates*—precisely why a POSITA would have applied Liaw’s teaching to Lan’s metal-gate structures. (See Petition at 43-44.) Put differently, Liaw teaches that retaining a cap layer on a metal-gate structure *avoids* the issues noted above. (See Liaw at 2:50-59, 3:44-49, 4:63-5:23, FIGS. 1B, 2B, 3B; Ex-1003 ¶¶188-189.) Liaw’s statement above thus fully supports the Lan-Liaw combination. Marlin’s misguided suggestion that it undermines the combination misses the point entirely.

Second, Marlin incorrectly contends that Lan’s spacers appear “very wide” compared to Liaw’s, such that Lan would not benefit from Liaw. (POR at 39.) But

as Marlin’s expert admits, neither Lan nor Liaw discloses any spacer dimensions that would permit such a comparison. (*See* Ex-1204 at 86:22-87:5, 87:11-18.) Marlin thus attempts to use non-scale drawings for an impermissible purpose: extracting “precise proportions” and “particular sizes.” *Hockerson-Halberstadt*, 222 F.3d at 956; *see also supra* Section II (discussing permissible and impermissible uses of drawings). Even worse, Marlin compares sizes between *different references*.

Marlin’s argument regarding spacer thickness also fails factually. As Dr. Fitzgerald explains, Moore’s Law of device scaling means that Lan and Liaw are trying to fit their respective transistors within a comparable physical space, such that their total sidewall thicknesses would be similar. (*See* Ex-2004 at 69:18-72:10.) In other words, Lan faces “the same misalignment problem” as Liaw. (*Id.* at 69:6-17.) Marlin is thus incorrect to suggest Lan is somehow immune to misalignment. No credible evidence supports that position.

Marlin’s criticisms of the Lan-Liaw combination thus fail, and the Lan-Liaw combination thus renders claim 2 obvious.

3. Grounds 4A and 4B: Chen discloses retaining the claimed cap layer, which also would have been obvious

Marlin does not dispute that Chen’s hard mask is a “cap layer” as element [2c] requires. (*See* Petition at 79-82; Chen at 4:43-44, FIG. 5.) Rather, Marlin argues the

hard mask must later be removed. (*See* POR at 41.) As with Lan, Marlin’s position lacks merit. (*See supra* Section IV.A.1.)

Contrary to Marlin’s position, hard mask removal in Chen is not “necessarily performed” or “required.” (POR at 44.) Rather, Chen expressly distinguishes the embodiments in FIG. 5 (with hard mask) and FIG. 6 (without hard mask):

To finish the device *according to an embodiment* of the present invention, the method forms sidewall spacers 501 from the second protective layer, as illustrated by **FIG. 5**. The sidewall spacers exposes an upper portion 503 of the hard mask, while sealing regions on the edges of the gate layer.

(Chen at 6:11-15 (emphases added).) Additionally, “[i]n *a preferred embodiment*, the method removes the hard mask to expose 601 the top surface of the gate structures, as shown in **FIG. 6**.” (*Id.* at 6:15-18 (emphases added); *see also id.* at 6:40-44 (explaining that steps may be added or removed “without departing from the scope” of Chen).) Chen never suggests the step of FIG. 6 is necessary.

As Marlin acknowledges, Chen’s FIG. 6 removes the hard mask to facilitate gate silicidation. (POR at 42.) And the experts agree silicidation is applicable only to polysilicon gates, not metal gates. (*See* Ex-1204 at 81:10-22; Ex-2004 at 76:12-77:17.) Direct silicidation of a metal gate would not work. (*See* Ex-2004 at 83:4-13; Ex-1003 ¶¶167-176, ¶¶324-325.) In fact, removing Chen’s hard mask would be

detrimental for metal-gate structures. (*See* Petition at 81-82.) A POSITA thus would have understood to retain Chen’s hard mask, at least for metal-gate embodiments. (*See* Chen at 3:45-46.)

At bottom, Chen discloses the MOSFET structure of claim 2, and it provides the same level of disclosure as the ’847 Patent. (*See, e.g.,* Ex-2004 at 87:9-88:11, 94:5-95:3; Chen at FIG. 5.) And Chen expressly discloses retaining its cap layer, rendering it obvious as well. (*See* Petition at 79-82.) Chen thus anticipates and renders obvious claim 2.

B. Marlin’s Allegations Regarding Cap Layer Removal Fail to Distinguish the Prior Art

Marlin’s arguments about cap layer removal are not just factually incorrect; they are also legally insufficient. Lan and Chen both disclose MOS transistor structures that satisfy all elements of claim 2, including the claimed “cap layer.” (*See* Petition at 35, 79-80; Lan at 2:51-52, 3:32-34, 4:56-58, Figs. 4, 8, 12; Chen at 4:43-49, 4:56-57, 5:28-30, 5:41-44, 5:62-64, 6:11-15, FIG. 5.) Marlin’s argument that those disclosed cap layers must be subsequently removed is not even legally sufficient to distinguish Lan or Chen:

The question of whether or not a reference can be regarded as prior art that describes a composition or structure as being an intermediate has been resolved in this court

It matters not one whit that it was intended to be and

appreciated as being an intermediate structure rather than an end use item.

In re Mullin, 481 F.2d 1333, 1335-36 (CCPA 1973) (emphases added); *accord Ex Parte Kick*, Appeal 2020-005161, 2021 WL 4050616, at *4-6 (P.T.A.B. Sept. 2, 2021); *Ex Parte Dai*, Appeal 2016-001506, 2017 WL 4418883, at *3 & n.4 (P.T.A.B. Sept. 26, 2017); *Ex Parte Taffinder*, Appeal 2008-4667, 2008 WL 4823242, at *5 (P.T.A.B. Nov. 5, 2008). Because “[i]t matters not one whit” whether the cap layers are later removed, *Mullin*, 481 F.2d at 1335-36, there can be no genuine dispute that Lan and Chen alone demonstrate the unpatentability of claim 2. Both disclose the claimed structure.

Attempting to circumvent Lan and Chen, Marlin argues the claim language somehow *excludes* intermediate (i.e., transitional) MOS transistor structures: “[T]he Petition appears to concede that the claims require a finished transistor structure, as opposed to an intermediate processing step in the creation of the structure.”² (POR at 32; *see also id.* at 43.) The ’847 Patent itself disproves Marlin’s position.

Marlin identifies nothing in the claims, specification, or prosecution history that excludes intermediate (i.e., transitional) structures. Marlin’s own expert even admits that the ’847 Patent encompasses intermediate structures. To function as

² The Petition makes no such concession.

transistors, Marlin’s expert testified that “[e]ventually you would” “need [to make] contacts to the structures” described in the ’847 Patent. (Ex-1204 at 76:13-77:2.) Yet he acknowledged that the specification does not “describe how to form electrical contacts to the source drain or gate.” (Ex-1204 at 77:12-21; *see also id.* at 75:15-76:3.) He admitted: “[T]hat is beyond the particular scope of what this specification is talking about.” (Ex-1204 at 79:15-80:4.) Petitioners’ expert agrees. (*See, e.g.*, Ex-2004 at 93:2-94:8.)

The claims of the ’847 Patent also do not recite electrical contacts. (*See, e.g.*, Ex-1204 at 73:11-74:6 (Marlin’s expert agreeing).) Although Marlin’s expert testified the transistor structures in the ’847 Patent are not “finished” because they lack contacts, he agreed that they satisfy the claims. (*See* Ex-1204 at 76:4-77:2; *see also* Ex-2004 at 74:6-20.) To suggest that the claims **exclude** such transitional structures is baseless. (*See* POR at 33, 43.)

As Dr. Fitzgerald explains, Chen and Lan both disclose MOS transistor structures at the same stage of processing that the ’847 Patent describes and claims. (*See* Ex-2004 at 94:12-95:3; *see also id.* at 82:22-83:3, 83:16-24, 87:12-88:11.) Thus, in addition to being wrong, Marlin’s allegations that the cap layers in Lan’s Fig. 12 or Chen’s FIG. 5 must be removed do not even distinguish Lan or Chen from claim 2. Their respective structures comprise all elements of claim 2, and that suffices. *See Mullin*, 481 F.2d at 1335-36.

Because the MOS transistor structures in Lan’s Fig. 12 and Chen’s FIG. 5 include all elements of claim 2, Lan and Chen alone render claim 2 unpatentable, regardless of any subsequent processing or optional cap layer removal.

V. MR. MCALEXANDER’S OPINIONS ARE ENTITLED TO LITTLE WEIGHT

The Board should afford Mr. McAlexander’s testimony little weight. His opinions do not reflect independent technical analysis; they track the POR essentially verbatim. Moreover, Mr. McAlexander is a serial declarant who lacks specialized experience with the technologies at issue.

A. Mr. McAlexander’s Declaration Parrots the POR

As the Board has repeatedly held, expert testimony that echoes a party’s arguments, lacking independent technical analysis or supporting evidence, has little probative value. *See Giesecke+Devrient GmbH v. Lumenco, LLC*, No. IPR2024-00838, Paper 31, at 21 (P.T.A.B. Nov. 19, 2025); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, at 15-17 (P.T.A.B. Aug. 24, 2022) (precedential).

That is exactly what occurred here. Mr. McAlexander’s declaration tracks Marlin’s POR nearly verbatim and provides no additional technical reasoning or evidentiary support. This includes, for example, reproducing the same typographical error as the POR. (*Compare* Ex-2003 ¶40 (misquoting the ’847 Patent as reciting “MOPS transistors,” when the patent correctly writes “MOS transistors”), *with* POR

at 11 (same).) It also includes verbatim repetition of Marlin’s arguments that “Grounds 4A and 4B Fail To Disclose Or Render Obvious” certain claim elements. (*Compare* Ex-2003 ¶¶43-52, *with* POR at 26-30.) And these are not isolated instances. Mr. McAlexander’s declaration generally tracks the POR nearly word-for-word. (*Compare generally* Ex-2003 §§VII-VIII, *with* POR §§IV.B-V.C.) It should therefore be given little weight.

B. Mr. McAlexander Lacks Relevant Expertise

Mr. McAlexander’s testimony also should be given little weight because he lacks meaningful expertise in the relevant technologies.

Mr. McAlexander has not done any semiconductor processing since the mid-1990s and has not obtained any patents for MOSFETs since the 1980s. (*See* Ex-1204 at 37:7-20, 42:8-11.) He has no experience with epitaxially strained MOSFETs. (*See id.* at 39:15-40:5, 41:7-9.) He has never been involved in silicidation involving metal-gate structures. (*See id.* at 38:9-15.) And he has no experience with contemporaneous metal gates, having last dealt with them in the 1970s. (*See id.* at 39:11-14.)

Instead, Mr. McAlexander has served as a serial expert witness. He has been retained as an expert in “350 or more” patent litigations. (*Id.* at 7:18-22.) He has been deposed “[m]ore than 200” times. (*Id.* at 8:21-9:1.) In addition to patent expert work, he performs product liability and insurance claims investigations. (*Id.* at

18:16-19.) And he provides acoustic system design installation services. (*Id.* at 18:2-11.)

In the PTAB alone, Mr. McAlexander has submitted over 100 expert declarations. (*See generally* Ex-1201; Ex-1202; Ex-1203; Ex-1204 at 11:14-12:3, 14:4-12.) Those declarations purport to provide expert testimony on fields as far-flung as sobriety monitoring (Ex-1204 at 15:15-18), electromechanical systems (*id.* at 15:19-22), blower motors for HVAC systems (*id.* at 16:1-4), electronic cigarettes (*id.* at 16:5-8), automotive inventions (*id.* at 16:9-16), circuits for LED dimmers (*id.* at 16:17-20), RFID systems (*id.* at 16:21-17:2), location tracking (*id.* at 17:3-6), wireless earphones (*id.* at 17:7-10), and acoustic systems (*id.* at 17:11-15). And in 2021, he submitted 33 declarations—an average of nearly three declarations per month. (*See generally* Ex-1203; Ex-1204 at 14:13-15:14.)

In contrast, Dr. Fitzgerald, a professor at MIT, is one of the pioneers of strained-channel MOSFET devices—precisely the kinds of devices at issue in these IPR proceedings. While a researcher at prestigious Bell Laboratories, Dr. Fitzgerald discovered that strained Si has higher mobility, and he has spent his career extensively researching and publishing peer-reviewed papers about the very technologies at issue here. (Ex-2004 at 8:14-10:6; Ex-1004.) And, unlike Mr. McAlexander, Dr. Fitzgerald has been deposed only 6 or 7 times. (*Id.* at 7:20-22.)

Because Mr. McAlexander lacks relevant experience to meaningfully opine on the disputed technical issues in this proceeding, the Board should give his opinions little weight. That should be especially true here, where Mr. McAlexander's declaration echoes Marlin's POR and cites almost no corroborating evidence.³

VI. CONCLUSION

The Board should issue an order cancelling challenged claims 1-11 of the '847 Patent because they are unpatentable.

Dated: April 1, 2026

Respectfully submitted,

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³ It cites just one independent document one time as supporting evidence. (*See* Ex-2003 ¶61 (citing Ex-2005 at 3).) And that document has little relevance.

CERTIFICATION UNDER 37 CFR § 42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft 365, this Reply contains 5,552 words, excluding this Certification and the following: Table of Contents, Table of Authorities, Table of Exhibits Cited, and Certificate of Service.

Dated: April 1, 2026

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing **Petitioners' Reply** was served electronically via email on April 1, 2026, to counsel of record below. These parties have consented to electronic service via email.

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