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Transcript of Joseph C. McAlexander, III

Date: March 17, 2026

Case: Taiwan Semiconductor Manufacturing Co, et al -v- Marlin Semiconductor
Ltd (PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 -----
3 BEFORE THE PATENT TRIAL AND APPEAL BOARD
4 -----

5 TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

6 Petitioner,

7 v.

8 MARLIN SEMICONDUCTOR LIMITED,

9 Patent Owner,
10 -----

11 Case IPR2025-00847

12 U.S. Patent No. 7,745,847 B2
13 -----

14
15 DEPOSITION OF JOSEPH C. McALEXANDER, III

16 Richardson, Texas

17 March 17, 2026
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21 Reported by: Susan S. Klinger, RMR-CRR, CSR

22 Job No. 624426

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March 17, 2026

9:05 a.m.

Deposition of JOSEPH C. McALEXANDER, III, held
at the offices of McAlexander Sound, 101 W. Renner
Road, Richardson, Texas, before Susan S. Klinger,
a Registered Merit Reporter and Certified Realtime
Reporter of the State of Texas.

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2

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I N D E X

WITNESS	PAGE
JOSEPH C. McALEXANDER, III	
EXAMINATION BY MR. LONG	5
EXAMINATION BY MR. LU	88

E X H I B I T S

No.	Description	Page
Exhibit 1201	Graph of PTAB cases	11
Exhibit 1202	Graph of PTAB declarations	12
Exhibit 1203	Graph of Exhibit 1202	14
Exhibit 1215	Chen's Figure 3 with markings	55

Previously Marked Exhibits

(Not attached.)

Exhibit 1001	45
Exhibit 1005	86
Exhibit 1006	87
Exhibit 1008	53
Exhibit 1009	54
Exhibit 2001	9
Exhibit 2003	42

1 P R O C E E D I N G S

2 JOSEPH McALEXANDER, III,

3 having been first duly sworn testified as follows:

4 MR. LONG: My name is J. Preston Long
5 counsel for the petitioners in this case with the
6 firm of Finnegan, Henderson, Farabow, Garrett &
7 Dunner. I'm joined today by my colleague Carlos
8 Duarte also with Finnegan.

9 MR. LU: I am Raymond Lu with Mintz Levin
10 for patent owner Marlin Semiconductor Limited.

11 MR. DOKHANCHY: Reza Dokhanchy with Mintz
12 also on behalf of patent owner.

13 EXAMINATION

14 BY MR. LONG:

15 Q Thank you, Mr. McAlexander. You have been
16 deposed before, correct?

17 A Yes, I have.

18 Q I assume you are familiar with the rules,
19 but just so we're clear today I will go over, you
20 know, what I expect and make sure we're on the
21 same page; is that okay?

22 A Certainly.

1 Q Okay. First, you understand please answer
2 verbally. Don't talk over me so that the court
3 reporter can accurately transcribe our
4 conversation; is that okay?

5 A Yes.

6 Q And I will also ask that if you require
7 clarification of one of my questions, please ask
8 just so that I make sure you are answering the
9 question that I think you are answering; is that
10 okay?

11 A That is okay, I understand.

12 Q Okay. From time to time counsel may
13 object during my questioning. But unless
14 instructed not to answer for purposes of
15 privilege, I would ask that you please give me an
16 answer to my question; is that okay?

17 A Yes.

18 Q Is there anything that might impact your
19 ability to give testimony today, any illness,
20 medications, anything like that?

21 A No.

22 Q What is your understanding of why you are

1 here today?

2 A I understand that there is a IPR that has
3 been filed and I have provided several reports,
4 declarations on behalf of the patent owner with
5 regard to those particular -- that particular
6 petition. So my understanding is I'm here to
7 discuss those matters.

8 Q So we're here for your declaration
9 regarding the validity of US Patent Number
10 7,745,847. Is it okay if I refer to that today as
11 the '847 patent?

12 A Yes, that is fine.

13 Q Did you bring anything with you today?

14 A I did not.

15 Q Roughly how many engagements have you had
16 as an expert witness in patent cases?

17 A How many engagements. Could you clarify?

18 Q How many expert consulting agreements have
19 you signed to provide opinions on behalf of a
20 party to a patent litigation?

21 A That is an interesting question. Probably
22 300, 350 or more.

1 Q Okay. And over what time period?

2 A Since about 1990.

3 Q Okay. Would you say they've been fairly
4 evenly distributed since 1990 or have they been
5 more skewed towards recent times or older times
6 closer to 1990?

7 A I would say overall, the -- the -- if you
8 compare probably about 50/50 between plaintiff
9 versus defendant.

10 Q So let me -- let me ask again, so I'm
11 asking about the time distribution.

12 A Okay.

13 Q Would you say you have had more
14 engagements recently, say, within the past 10
15 years or more engagements, say, within your first
16 10 years since 1990, just distribution over time?

17 A I would say that the engagements initially
18 during the first probably eight years was lower,
19 but it has been a fairly consistent engagement
20 since that time.

21 Q Roughly how many times have you been
22 deposed as an expert witness?

1 A More than 200.

2 Q Okay. So let me go ahead and hand you
3 exhibit -- this is an exhibit already marked.
4 This is Marlin Semiconductor Limited, Exhibit
5 Number 2001. And it is titled, Declaration of
6 Joseph C. McAlexander, III regarding patent
7 owner's preliminary response for inter partes
8 review of U.S. Patent number 7,745,847.

9 Are you familiar with this document?

10 (Exhibit 2001 discussed.)

11 A Yes, I am.

12 Q Okay. What is it?

13 A It is my preliminary declaration
14 supporting the patent owner's preliminary
15 response. It was dated August 15th of 2025.

16 Q Okay. And Exhibit 2001 contains some of
17 your opinions regarding the validity of the '847
18 patent; is that right?

19 A Correct.

20 Q Okay. And if I for brevity refer to this
21 as your first declaration today, will you
22 understand what I'm talking about?

1 A Yes.

2 Q Is everything in your first declaration
3 accurate to the best of your knowledge sitting
4 here today?

5 A Yes.

6 Q Okay. If you could turn to paragraph 1,
7 which is on page 1 of your first declaration.

8 A I'm there.

9 Q Okay. And it says that you hold a
10 bachelor of science degree in electrical
11 engineering from North Carolina State University;
12 is that right?

13 A That is correct.

14 Q Do you have an advanced degree beyond
15 that, a masters or Ph.D.?

16 A No, I do not.

17 Q Let's turn to page 34 of your first
18 declaration -- well, strike that.

19 Can you turn to your CV which begins the
20 first page following page 30 of your declaration?

21 A Okay, I'm there.

22 Q Was this CV up-to-date as of the time you

1 filed your first declaration?

2 A I would say since the footer shows first
3 quarter, this is probably the declaration that was
4 provided to counsel when I first started the IPR
5 process. And it was probably provided at that
6 time, so there are probably a few entries
7 additional to that.

8 Q Okay. So this would have been accurate as
9 of the first quarter of 2025?

10 A Yes, sir, that's correct.

11 Q I am going to introduce what is going to
12 be marked as Exhibit 1201.

13 (Exhibit 1201 marked.)

14 Q And I will represent to you that this is a
15 graph showing the number of PTAB cases you have
16 been involved in each year from 2013 to 2025.
17 This was pulled from a service called Docket
18 Navigator.

19 Does this data look correct to you?

20 A Interesting, so this is just PTAB?

21 Q This is just PTAB cases?

22 A As I sit here, I have no information to

1 dispute it one way or the other. If you pulled
2 this out of the PTAB type records, then I would
3 say it is probably clearly correct.

4 Q Okay. I will hand you what is being
5 marked Exhibit 1202.

6 (Exhibit 1202 marked.)

7 Q I will represent that this is a list of
8 PTAB declarations again obtained from Docket
9 Navigator as of the date in the upper left corner,
10 March 13th, 2026?

11 A Okay.

12 Q Does this look about right to you?

13 A I do recognize these, so yes, I would say
14 it -- it was correctly reflected.

15 Q Okay. And according to this, you filed
16 looks like a -- in the upper right corner you can
17 see on the first page 109 results. Does that
18 sound right, that you filed about 109 declarations
19 in the PTAB?

20 A Well, I think it is -- if I'm looking at
21 this chart on Exhibit 1201, I would say that the
22 chart and this list, Exhibit 1201 versus 1202, do

1 not connect, do not correlate.

2 Q One is cases, one is declarations, so I
3 wouldn't expect them to be the exact same number.

4 A Okay. All right. So my -- my apologies,
5 because I thought that -- that Exhibit 1201 --
6 Exhibit 1201 is PTAB, correct?

7 Q Exhibit 1201 is PTAB cases. So in other
8 words, has a certain case caption. Is it possible
9 you filed more than one declaration in one case?

10 A Yes.

11 Q Okay. So that would explain --

12 A Okay. That is the disconnect, because I
13 see a number that -- that are for a particular
14 case. So what you are saying is this -- this
15 total list here on Exhibit 1202 is then kind of
16 reduced to a combination within cases.

17 Q What I'm saying is that Exhibit 1201 is
18 the number of cases. So in other words, case
19 captions with the PTAB you have been involved in,
20 Exhibit 1202 is a list of declarations that you
21 filed?

22 A That would be associated with those case

1 captions.

2 Q Correct.

3 A All right. Then fine, yes.

4 Q So just for the record -- let me reask
5 again. So according to the upper right corner of
6 Exhibit 1202, you filed approximately 109
7 declarations in the PTAB. Does that sound right
8 to you?

9 A And again the case caption you are
10 pointing to is on 1202 or --

11 Q Correct.

12 A Okay, yes, correct.

13 Q Okay. And let me hand you what is being
14 marked as Exhibit 1203.

15 (Exhibit 1203 marked.)

16 Q I will represent to you this is a graph
17 where I went through that list in Exhibit 1202 and
18 I pulled out the number of declarations per year
19 and graphed it. And I guess I will note that this
20 one only has 108 entries, because it does not
21 capture the most recent one listed in Exhibit
22 1202. So I believe the last entry for 2026 should

1 have four instead of three.

2 MR. LU: Just to be clear, this is a graph
3 that you created?

4 MR. LONG: I prepared this based on the
5 data in 1202 minus the most recent entry.

6 Q Does this look about right to you in terms
7 of the distribution on your declarations?

8 A I certainly have not seen this before.
9 I'm not here to judge the accuracy of how you
10 compile your list, but if you represent it as such
11 then I can accept it perhaps represents a timeline
12 review of different PTAB declarations filed.

13 Q Okay.

14 A No reason to dispute it.

15 Q Okay. Have you submitted to the PTAB an
16 expert declaration opining on a sobriety
17 monitoring system?

18 A With AMS, yes.

19 Q Have you submitted to the PTAB an expert
20 declaration opining on electromechanical systems?

21 A A number of PTAB results in
22 electromechanical systems as a general topic.

1 Q Okay. Have you submitted to the PTAB an
2 expert declaration regarding a blower motor for an
3 HVAC system?

4 A I believe I recall that, yes.

5 Q Have you submitted to the PTAB an expert
6 declaration opining on an electronic cigarette
7 device?

8 A Multiple ones.

9 Q Have you submitted to the PTAB an expert
10 declaration opining from the perspective of
11 someone in the automotive industry?

12 A I have, yes.

13 Q Have you submitted to the PTAB an expert
14 declaration regarding automotive electrical
15 systems?

16 A Yes.

17 Q Have you submitted to the PTAB a
18 declaration as an expert in the field of design
19 and testing of LED drivers and dimmers?

20 A Yes.

21 Q Have you submitted to the PTAB a
22 declaration as an expert in the field of RFID

1 systems?

2 A I have.

3 Q Have you submitted to the PTAB a
4 declaration as an expert opining on GPS-related
5 location tracking techniques?

6 A Yes.

7 Q Have you submitted to the PTAB a
8 declaration as an expert opining on wireless
9 earphones?

10 A Yes.

11 Q Have you submitted to the PTAB a
12 declaration as an expert in the field of acoustic
13 implementation and/or the design of acoustic
14 systems?

15 A I have, yes.

16 Q Go back to your CV in Exhibit 2001 and ask
17 a few questions about your work experience. And
18 I'm looking specifically at page 3 of your CV in
19 page 0021.

20 A Okay, I'm there.

21 Q Okay. And this is where it begins with
22 your experience profile, correct?

1 A Correct.

2 Q What is the name of the company that you
3 use for providing your expert witness services?

4 A McAlexander Sound.

5 Q Okay. And is it McAlexander Sound, Inc.,
6 McAlexander Sound PT -- Ltd., or --

7 A Inc.

8 Q Okay. Now, you perform acoustic system
9 design installation services as part of your work
10 at McAlexander Sound, Inc., right?

11 A Correct.

12 Q And you provide patent portfolio
13 development and valuation services as part of your
14 work with McAlexander Sound, right?

15 A Correct.

16 Q You perform product liability and
17 insurance claim investigation services as part of
18 your work with McAlexander Sound, right?

19 A Correct.

20 Q Okay. So the next - and are the dates
21 listed here on your CV for McAlexander Sound
22 correct?

1 A Yes.

2 Q The next entry is something called
3 MDFHoldings, Inc. Las Vegas, Nevada, 2002 to
4 present. Do you see that?

5 A Yes, I do.

6 Q And you're the CEO of MDFHoldings; is that
7 correct?

8 A Correct.

9 Q MDF is an IP holding and licensing
10 company, right?

11 A Correct.

12 Q And MDFHoldings owns IP related to an
13 object locating system; is that right?

14 A Correct.

15 Q And do you see the last bullet entry under
16 MDFHoldings it says, has not been and is not
17 engaged in any IP related litigation or licensing
18 activities?

19 A Yes.

20 Q Could you help clarify for me what it
21 means that MDFHoldings has not been and is not
22 engaged in any IP related litigation or licensing

1 activities if MDFHoldings is an IP holding and
2 licensing company?

3 A Because MDFHoldings holds patents
4 currently and none of them are under litigation or
5 licensing, so therefore, MDFHoldings is not
6 involved in IP litigation or license.

7 Q I see. So would it be more accurate to
8 say MDFHoldings is a IP holding and licensing
9 company?

10 A No, it is not correct.

11 Q So why is MDFHoldings a licensing company?

12 A Because it holds patents that it can
13 license. Currently it is not engaged in licensing
14 the patents.

15 Q I see. Has it?

16 A It has done so in the past.

17 Q It has done so in the past?

18 A Yes.

19 Q So is it accurate when it says has not
20 been engaged in any IP related licensing
21 activities?

22 A The truth is, yes, it is correct, because

1 the patents that were to be licensed were sold,
2 and so the licensing took place under a different
3 entity. So we have not -- I have not been, as
4 MDF, actually involved directly in licensing even
5 though we hold patents that can be licensed.

6 Q Okay. Did you participate in licensing or
7 sales activities on behalf of another company for
8 those patents?

9 A No. In that particular case, the patents
10 were actually sold to another company.

11 Q Okay. And were you involved in that
12 company?

13 A No.

14 Q No, okay.

15 Does MDFHoldings receive revenues from any
16 litigation or licensing activities involving those
17 patents?

18 A No.

19 Q The next entry is QM Partners, LP. Do you
20 see that?

21 A Yes, I do.

22 Q And the dates are 2006 to 2020; is that

1 correct?

2 A That is correct.

3 Q Okay. And you were the manager of QM
4 Partners from 2006 to 2020; is that right?

5 A Correct.

6 Q And QM Partners was involved in the
7 management and development, licensing, prosecution
8 and exploitation of assigned intellectual
9 property; is that right?

10 A Correct.

11 Q And is that work that you did when you
12 were at QM Partners?

13 A It is.

14 Q Okay. What kind of management of
15 prosecution did you do at QM Partners?

16 A The -- if I can answer the question on QM
17 Partners in relationship to the next entry which
18 is Guardian Technologies, the -- the aspect of QM
19 Partners was to manage and develop intellectual
20 property and we did that by identifying specific
21 patents that we would like to represent, including
22 the inventors of those patents, and we formed

1 companies. And one of the companies that QM
2 Partners formed was Guardian Technologies.

3 And so to answer your question if you look
4 within the Guardian Technologies umbrella, you
5 will see a number of patents that are listed
6 there. The original aspect of this was we --
7 there was a filing of a lawsuit against Tandy
8 Corporation, and that resulted in a settlement.

9 And then the rest of this is the
10 development of patentable ideas, for instance, the
11 -- I mentioned the litigated U.S. Patent '076,
12 that was specifically Tandy. And then the
13 additional patent here, the 8,334,775, is the one
14 that is co-invented from myself as well as a
15 couple of other inventors. And so that is what I
16 mean by participating in the prosecution of
17 patents that we own.

18 Q Okay. And does the same thing go for the
19 rest of the description in QM Partners in terms of
20 management and development, licensing and
21 exploitation of the assigned intellectual
22 property?

1 A That's correct. The primary focus that we
2 developed during that period of time was the
3 development and part ownership of the created
4 company Guardian Technologies.

5 Q Okay. And so the last bullet under QM
6 Partners is not assigned any patents and is not
7 engaged in any IP related licensing or litigation
8 activities. That only refers to current times,
9 not -- not --

10 A Yes.

11 Q It is not backwards looking; is that
12 right?

13 A Yes, that's correct.

14 Q Okay. So it was -- so QM Partners was
15 assigned -- was engaged in IP related licensing or
16 litigation activities, right?

17 A In the past, yes.

18 Q Okay. And if I look at Guardian
19 Technologies on the next page this is page 4 of
20 your CV in Exhibit 2001, it says, not engaged in
21 any IP related licensing or litigation activities.
22 Again, that -- that refers to the present tense,

1 not the past tense, correct?

2 A That is correct, yes.

3 Q So Guardian Technologies was involved in
4 IP related licensing or litigation activities in
5 the past, yes?

6 A Both in the past, yes.

7 Q If I turn to page 5 of your CV in Exhibit
8 2001, looks like you were at Texas Instruments
9 from 1972 to 1986; is that right?

10 A That's correct.

11 Q Since 1986, have you worked at any company
12 that designs its own MOSFET structures or
13 fabricates its own MOSFETs?

14 A I'm not sure what you mean. I was not
15 employed by, but I've worked in that particular
16 field on behalf of clients since that time, yes.

17 Q Okay. Specifically designing transistor
18 structures?

19 A Yes.

20 Q Designing the -- well, explain what kind
21 of work you are referring to, please?

22 A Well, I was -- I consulted under contract

1 with TI working on their DLP strategy. That is --
2 that is the -- that is the strategy where the
3 transistors are used to actually these large TV
4 screens and large cinema screens, that digital
5 light projection capability, that was DLP. So I
6 worked with them to develop the transistors as
7 well as the inculcation of that into cameras and
8 processors and TV as well as cinema as well as
9 printers.

10 Q Okay.

11 A So that is one.

12 Q What specific aspects of transistor design
13 did you do in that regard?

14 A That is development of the actual
15 transistor core itself.

16 Q Okay. And specifically what did you do,
17 what deliverables did you give to --

18 A Well, again, I was a consultant. I was
19 not given a product -- I was not given a hard copy
20 product, okay, but I worked with those that were
21 in that to help them in the aid of that design,
22 the evaluation of the design and the -- and the --

1 I would say the -- the improvement in the design
2 based upon the performance, so that is what I did.

3 Q Okay. What kind of file formats did you
4 look at?

5 A I do know what you mean, that would be
6 proprietary to TI.

7 Q But you can't tell me if you were looking
8 at GDS files or if you were looking at hardware
9 code, if you were looking at, you know, process
10 flows, you can't tell me that?

11 A Generally I was looking at the CAD design
12 drawings and the schematic design drawings. Now,
13 you can output those into GDS, that is a file
14 format for output. But when you are looking at it
15 on the computer on the screen, that is basically
16 under the CAD program that is proprietary to TI.

17 Q So when you were looking at the CAD
18 layout, you were looking at circuit layouts,
19 correct?

20 A Yes.

21 Q And that circuit layout included
22 transistors and other electronic components,

1 right?

2 A Yes.

3 Q Okay. Did it describe the physical layout
4 of any particular transistor, in other words, how
5 it would look in silicon?

6 A Absolutely.

7 Q It did. And how so?

8 A Any time you do a schematic type program,
9 it -- it is only memorialized if you can create a
10 -- a three-dimensional aspect for -- for
11 generation of the reticles for the wafers. So you
12 can look at the schematics and the schematic would
13 then translate into a layout, so both -- both were
14 available.

15 Q Okay. So when you talk about layout, now
16 we're talking about GDS files, right, GDS layout?

17 A Again, GDS is an output, okay. I'm
18 looking at it on the computer.

19 Q Right.

20 A There is various formats, GDS is one of
21 those formats.

22 Q So you're looking at mask layouts, not

1 TEMs or SEMs of transistors, correct?

2 A Well, you are mixing things, so let me try
3 to clarify.

4 What we're talking about here is the
5 actual schematic and the schematic will translate
6 because it is dimensioned in terms of the process
7 parameters as well as the physical parameters.
8 That is translated into a layout on the computer
9 so you can see three-dimensionally what this would
10 look like when it was instantiated into an actual
11 device. That would be the ones that use the
12 tapeout to generate the reticles for fabrication.
13 That is what I'm speaking of.

14 Now, I also did evaluations of the
15 product. As I mentioned, I looked at it from the
16 performance standpoint, and so I looked at these
17 particular products both optically as well as
18 scanning -- with scanning microscopy.

19 Q And you looked at specifically transistor
20 structures?

21 A That's correct.

22 Q Okay. Now, these -- what years was that

1 that you worked on DLP?

2 A I would say principally it is in the
3 1990s.

4 Q Okay. So after the 1990s, did you work
5 for any company or did you do any work related to
6 the specific design fabrication of MOSFET
7 structures?

8 A Yes, I did.

9 Q Okay. What was that work?

10 A Well, I continued work with TI
11 specifically working on their magnetic RAM,
12 ferrous RAM memory device. I and one of my
13 colleagues were contracted by TI to actually do
14 the design and development of the ferrous
15 technology.

16 Q And is an MRAM a transistor design?

17 A Yes.

18 Q Okay. And what materials were used in
19 MRAM?

20 A What materials?

21 Q Uh-huh.

22 A I'm not exactly sure what you mean by

1 materials.

2 Q Well, it is magnetic, so what makes it
3 magnetic?

4 A Well, you use ferrous related materials.
5 Basically it is a -- it is a combination material.
6 It still uses some of the technology that you have
7 standard for MOS.

8 Q But is it an MOS device?

9 A It is an MOS type device, yes.

10 Q What makes it magnetic?

11 A I'm not sure what I can -- I really don't
12 think I can really give you that information,
13 because that is proprietary in terms of the way
14 they did their design.

15 Q What about MRAM in general, what makes it
16 a magnetic device?

17 A It is -- one of the ways in which it is
18 done is by utilizing different types of ferrous
19 material that is inculcated or involved in the
20 particular material itself.

21 Q In the substrate, in the gate, in the
22 where?

1 A Primarily in the -- in the gate channel
2 area.

3 Q And what year or years was that?

4 A That would have been in the last half of
5 the 1990s.

6 Q Okay. So again, after the 1990s, have you
7 done any work that specifically relates to design
8 of MOSFET structures or the fabrication of
9 MOSFETs?

10 A Yes.

11 Q Okay. And what work is that?

12 A That was work with STMicroelectronics.

13 Q What work did you do for STMicro?

14 A That was involved in MOS technology
15 specifically in the design and development of
16 their microprocessor systems. Also as a part of
17 that, did quite a bit of work with them consulting
18 in the, in the flash memory using EEPROM
19 technology.

20 Q Okay. And what years did you do your work
21 for STMicro?

22 A I did work with STMicro from the early

1 1990s through about 2016.

2 Q Was that continuous work?

3 A Yes, I would say.

4 Q You were continuously developing for
5 STMicro between the early 1990s to 2016; is that
6 right?

7 A I was continuously consulting with
8 STMicro, some of that was involved with those
9 designs, but I did other work with them as well.

10 Q Okay. I'm only interested in the work you
11 did relating to the design of MOSFET structures
12 for STMicro, what years would you say that was?

13 A I would say through -- probably up through
14 2010, 2011.

15 Q So early 1990s through 2010 or 2011?

16 A Yes.

17 Q You were designing MOSFET structures for
18 STMicro; is that right?

19 A Again, consulting with STMicro on the
20 design of structures.

21 Q Consulting with STMicro, okay.

22 A And the reason I say 2010, 2011 is because

1 several of my patents that are assigned to
2 STMicroelectronics are directed to the release
3 beam sensor technology, which is at the transistor
4 level, semiconductor beams used in airbag
5 deployment, GEO orientation and that was up
6 through 2011.

7 Q Okay. And you worked specifically -- now,
8 let me be clear. When I talk about consulting on
9 the design of MOSFET structures, I'm not just
10 talking about specifying a gate length or a
11 resistance and so forth. I'm talking about
12 actually designing how the MOSFET is going to look
13 in a -- in a fabrication process. Are we talking
14 about the same thing?

15 A Yes.

16 Q We are, okay. Does STMicro fabricate its
17 own transistors?

18 A Yes.

19 Q Has its own fabs?

20 A Yes.

21 Q Okay. What -- what sizes are they capable
22 of making?

1 A State of the art.

2 Q Okay. What do you mean by state of the
3 art? How many -- what is the -- what is the gate
4 length?

5 A I haven't worked with them directly for
6 about 10 to 11 years, so I really can't tell you
7 what their current is.

8 Q Okay.

9 A But they were maintaining -- I mean, they
10 were one of the key industries in flash memory.
11 They -- they -- they maintained competitive rates
12 there. It is certainly in the sub hundred
13 nanometer.

14 Q Okay.

15 A I believe their technology is at least
16 down to in the 20 to 8. 20 nanometers some of
17 their products are representatives now. But I
18 would say it was in that 20 to 100 nanometer
19 during the time I was working with them.

20 Q 20 to 100 nanometer. You worked on 20
21 nanometer devices with STMicro, is that right?

22 A No, I said their technology was in the 20

1 to 100 nanometer during that period of time. The
2 particular ones I was looking at it really depends
3 upon the instantiation as to how that transistor
4 would be worked into a particular device, but it
5 was standard MOS type technology using standard
6 CMOS technology.

7 Q So in other words, your circuit designs
8 would be instantiated differently depending on the
9 process that was used; is that fair?

10 A Correct.

11 Q Do you know which processes were used to
12 instantiate the designs you worked on at STMicro?

13 A I can't give you the specific names
14 because that is proprietary. I'm not exactly sure
15 what you are looking for.

16 Q Can you tell me the company?

17 A What do you mean the company,
18 STMicroelectronics.

19 Q So STMicro fabbed the products that you
20 consulted on; is that right?

21 A That's correct.

22 Q Okay. And you don't know what sizes those

1 circuit were instantiated on or what process nodes
2 those circuits were instantiated on; is that
3 right?

4 A I don't recall.

5 Q Okay.

6 A Not specifically.

7 Q When was the last time you were personally
8 involved in processing a semiconductor wafer to
9 fabricate a MOSFET?

10 A Could you clarify processing? You mean
11 actually involved in the following with the wafer
12 -- through the process in the wafer fabrication,
13 is that what you are referring to?

14 Q Correct.

15 A I would say probably the mid '90s in terms
16 of actually in process for a particular design. I
17 consulted with processing of quite a few designs,
18 but your -- your clarification was actually
19 involved in the actual following of a design in a
20 process, so that would be the mid 1990s.

21 Q Have you ever personally performed
22 silicidation of a wafer?

1 A I have not personally performed that. I
2 have set the recipes up and -- and been a part of
3 that process, but no, I haven't actually done it
4 myself, no.

5 Q Okay. And when was that that you were
6 involved in setting up the process for
7 silicidation?

8 A Mid '90s again.

9 Q Have you ever personally performed
10 silicidation on a MOSFET with a metal gate?

11 A No.

12 Q Have you ever designed a process for
13 performing silicidation on a MOSFET with a metal
14 gate?

15 A Personally, no.

16 Q Have you ever been involved with metal
17 gate MOSFETs as opposed to poly gate MOSFETs?

18 A Yes.

19 Q Yes. Can you show me where on your CV
20 that experience is?

21 A I do not list it specifically in the CV,
22 but I will point you to the fact that in the '72

1 to '79 timeframe -- '72 to '79 timeframe where I
2 designed RAMs. Part of that evaluation was the
3 looking -- was the evaluation of current products.
4 And the current products as of 1972 were metal
5 gate. Metal gate is old technology. That was the
6 original -- before they developed polished silicon
7 in the '70s, metal gate was the way it was done.

8 Q I see.

9 A So that is evaluating products and
10 converting it to poly gate.

11 Q Got you. So have you been personally
12 involved in metal gate technology since the '72 to
13 '79 timeframe?

14 A No, not -- not directly with metal gate.

15 Q Have you ever been involved in strained
16 channel MOSFET design?

17 A Not personally, no.

18 And I want to clarify that when we talk
19 about strained channel design using something like
20 silicon uranium or silicon carbide. I have not
21 done that personally, but even in the design of
22 our memory devices even as of 1976, we actually

1 did with the way we grew the field oxide, we
2 created a strain on the channel even in 1976 in
3 order to change the -- the capacitance ratio as
4 far as the transfer of charge or voltage from the
5 gate to the drain or to the source.

6 Q And is that -- was that work published
7 or --

8 A It was the way it was designed.

9 Q Okay.

10 A I don't know that it was necessarily
11 published, per se. I think if you go back and you
12 look at a number of papers and articles in terms
13 of the way in which you create the -- the source
14 and drain technology, any time you do source and
15 drain there is always going to be some interface
16 to the channel. And so the way you construct that
17 there is a lot of papers and articles on that, but
18 in terms of silicon-uranium and silicon carbide, I
19 have not worked directly with that.

20 Q When you talk about the field oxide, we
21 are talking about the isolation oxide that defines
22 the active regions?

1 A The isolation oxide, that is one. The
2 other is the way in which you can -- you can grow
3 the -- the additional oxides that are above or
4 beside the gate oxide. In that growth process you
5 can also alter the -- the presentation of the gate
6 oxide as it appears to the substrate.

7 Q Do any of your own patents involve
8 strained channel MOSFETs of any sort?

9 A They -- they are not directed to that, no.

10 Q Okay. Can you identify any of your own
11 patents since 1990 that provide a specific MOSFET
12 design?

13 A The only -- in terms of just MOS design,
14 the patents that are related to the weighted
15 release beam sensor are MOS technology and they're
16 dated in 2008.

17 Q Are you referring to U.S. Patent Number
18 7,353,706?

19 A That's correct and also Patent Number
20 7,989,906 in 2011. There are two EP patents
21 listed on page 10 of the CV dated in 2010.

22 Q Those are --

1 A I may have missed one, but they are
2 directed to MOS technologies specifically in
3 developing sensors.

4 Q Okay. And those patents would include a
5 specific MOSFET design; is that right?

6 A Well, it is an MOS design. It is not a
7 field-effect transistor. It is an MOS design.

8 Q Okay, okay. So can you identify any of
9 your own patents after the year 1990 that provide
10 a specific MOSFET design?

11 A No.

12 Q I will hand you now what is being marked
13 -- well, it is already marked actually Marlin
14 Semiconductor Limited Exhibit 2003. And this
15 document is titled Declaration of Joseph C.
16 McAlexander, III regarding patent owner's
17 response. Do you see that?

18 (Exhibit 2003 discussed.)

19 A I do.

20 Q Okay. Are you familiar with this
21 document?

22 A Yes, this was the second declaration dated

1 January the 9th, 2026.

2 Q Okay. And if I refer to Exhibit 2003 as
3 your second declaration, will you understand what
4 I am referring to?

5 A Yes.

6 Q And your second declaration contains
7 additional opinions you provided regarding the
8 validity of the '847 patent; is that right?

9 A Correct.

10 Q Is everything in your second declaration
11 accurate to the best of your knowledge sitting
12 here today?

13 A To the best of my knowledge.

14 Q Okay. Can you go to paragraph 24? I
15 believe it is on page 10 and this is a section
16 titled Planar versus Three-Dimensional
17 Transistors. Do you see that?

18 A Did you say page or paragraph?

19 Q I said paragraph 24.

20 A Thank you.

21 Q It is on page 10.

22 A Yes. Okay, I'm there, yes.

1 Q Okay. All right. So beginning at
2 paragraph 24 there is a section of your second
3 declaration titled, Planar versus
4 Three-Dimensional Transistors. Do you see that?

5 A Yes, I do.

6 Q And so in paragraphs 24 through 28 of your
7 second declaration it describes a differences
8 between planar and FinFET devices; is that right?

9 A Yes, that's correct.

10 Q Okay. Why did you provide that discussion
11 in your second declaration?

12 A The most representative qualification of
13 that is because it is copied out of my first
14 declaration.

15 Q Okay.

16 A It is one-to-one corresponding to my first
17 declaration.

18 Q Okay. Well, let's look at paragraph 12 of
19 your first declaration beginning at -- on page 6.

20 A Okay.

21 Q And beginning at paragraph 12 of your
22 first declaration is a section titled Planar

1 versus Three-Dimensional Transistors, correct?

2 A Yes, sir, that's correct.

3 Q And paragraphs 12 through 16 of your first
4 declaration describe the differences between
5 planar and three-dimensional transistors, right?

6 A It discusses that, yes.

7 Q Why did you provide that discussion in
8 your first declaration?

9 A Just setting the environment that there is
10 -- in the development of MOS type technology for
11 FETs there are two different primary methods and
12 one is the planar, which is the older method. And
13 there is an advent of the three-dimensional
14 transistor specifically with the FinFET for newer
15 technologies.

16 Q Uh-huh. Does the '847 patent mention the
17 work FinFET?

18 A Do you have a copy of the patent?

19 Q Sure. I will hand you TSMC Exhibit 1001.
20 (Exhibit 1001 discussed.)

21 A Thank you.

22 Q -- which is the '847 patent?

1 A Yeah. I don't recall it directly
2 addressing FinFET, per se. It is a -- it is a MOS
3 which was generally applicable to both the older
4 technology and the newer technology.

5 Q Okay. Do any illustrations in the '847
6 patent depict a FinFET?

7 A No, not that I recall.

8 Q Does any of the prior art in this
9 proceeding describe FinFETs?

10 A I don't recall the prior art that is at
11 issue for this particular IPR specifically
12 addressing FinFET.

13 Q Okay. Did you decide to include a
14 discussion of FinFET in your first declaration?

15 A I did.

16 Q And in your view, is the difference
17 between planar and FinFET geometries relevant to
18 this IPR?

19 A If I understand your question correctly, I
20 don't think the geometries, per se, are relevant.
21 In terms of whether or not it is applicable only
22 to planar versus three-dimensional, the answer is

1 no. There are -- the technologies that are
2 available today are both the planar and the -- and
3 the FinFET. Those are both current technologies,
4 so this was basically just describing those and
5 how you develop the three-dimensional FinFET, so
6 it is just a general background.

7 But in terms of the patent itself, one
8 looks at the claims and determines how the claims
9 can be read on a particular product. And so I
10 don't think it is -- it is only directed to
11 planar.

12 Q Okay. But does any of the prior art we're
13 concerned with describe FinFETs?

14 A I don't believe so.

15 Q Okay. Then how is FinFET related to the
16 IPR proceeding we're here discussing today?

17 A I think I just said that. That the
18 technologies that are existing today are both
19 planar and three-dimensional. So I'm giving a
20 general background as to state of the art.

21 Q Okay. And what is relevant to the
22 invalidity of this patent, the state of the art or

1 the technology as it was as of the priority date
2 of the '847 patent?

3 A Well, in terms of the relevance to the
4 invalidity of the '847 patent or the validity of
5 the '847 patent, that -- that ties back to the
6 filing date of 2007, so what is the relevant
7 technology as of that time. Again, I don't want
8 to mix the two up. In my declaration, I do
9 address the particular art that has been provided
10 by the petitioner and specifically addressing that
11 as it applies to the '847 patent.

12 In this section on both the initial first
13 declaration and the second declaration, I'm just
14 by way of example giving the basics of how -- what
15 this transistance with MOSFETs looks like.

16 Q I see.

17 A It is just a basic technology overview.

18 Q Okay. And you came up with the language
19 for the technology overview in paragraphs 12
20 through 16 of your first declaration; is that
21 right?

22 A I'm not sure what you mean by came up

1 with. I worked jointly with counsel, but the
2 words -- I would say the majority of what is here
3 is what I created, yes.

4 Q Okay. Do you recall when you would have
5 created that language? I guess, the date of this
6 document is --

7 A This is August.

8 Q August 15th, 2025. Okay. And so would
9 you have come up with this language around that
10 time?

11 A No.

12 Q No.

13 A I've used this in previous IPRs as well.

14 Q You have used this language --

15 A But as I sit here, I can't tell you
16 exactly when.

17 Q I see, okay.

18 Do you remember any particular IPR where
19 this language appeared specifically?

20 A Not as I sit here.

21 Q But you understand that this language was
22 in previous IPRs?

1 A I have used -- I have used the substance
2 of this language. There may have been a few word
3 changes, but I've used the substance to give a
4 background of the technology in a number of
5 different IPRs.

6 Q I see, okay.

7 And in paragraph 14 of Exhibit 2001, does
8 the figure on the left illustrate a 2D planar
9 transistor built on the flat silicon substrate, do
10 you see that?

11 A Yes, sir, I do.

12 Q Is that how you would characterize a 2D
13 planar transistor is one being built on a flat
14 silicon substrate?

15 A Well, from a general standpoint, the
16 answer is yes. It is built on the substrate. The
17 -- the gate sits above the substrate and the
18 channel is through the surface area of the
19 substrate itself.

20 Q I see. And paragraph 15 of Exhibit 2001
21 the first sentence says, an exemplary 3D fin
22 transistor design features a vertical

1 semiconductor fin structure above the substrate
2 that acts as a channel between the source and
3 drain regions.

4 Do you see that?

5 A Yes, I do.

6 Q Is that how you would characterize a 3D
7 fin transistor?

8 A It is a general overview of one, yes.

9 Q FinFET, right?

10 A Correct.

11 Q We've been going about an hour. I will
12 leave it to you if you want to take a break or
13 keep going.

14 A It is up to you. I'm ready to keep going.

15 COURT REPORTER: I'm fine.

16 Q All right. We will keep going.

17 A Unless you just want to break and finish.

18 Q Trust me. I'm trying to get there as
19 quickly as you are.

20 Could you turn to claim 1 of the '847
21 patent, that is Exhibit 1001?

22 A Sure.

1 Q So claim 1, I'm looking at the first
2 limitation after the preamble. It says, a gate
3 formed on the semiconductor substrate.

4 Do you see that?

5 A I do.

6 Q And then the third element recites in
7 part, a spacer formed on the sidewall of the gate.

8 Do you see that?

9 A Yes, I do.

10 Q Okay. In your view, is the claimed
11 sidewall -- excuse me, strike that.

12 In your view, is the claimed spacer part
13 of the claimed gate?

14 MR. LU: Objection, calls for a legal
15 conclusion.

16 A If I read the specifics here, the
17 structure is a gate formed on the substrate. And
18 the third element is a spacer formed on the
19 sidewall of the gate. So that seems to me to be
20 something that is added and formed on the sidewall
21 of the gate, so therefore, it is not part of the
22 gate --

1 Q Okay.

2 A -- as claimed.

3 Q Right. So your understanding is that the
4 spacer is not part of the gate, correct?

5 A The spacer that is claimed here is not
6 part of the gate.

7 Q Okay.

8 A It is a part of the MOS transistor
9 structure.

10 Q Sure. Now, let's go back to your second
11 declaration, Exhibit 2003.

12 Paragraph 5, which begins on page 3.

13 A You're going the wrong direction.
14 Paragraph 5, okay.

15 Q And do you see midway through this
16 paragraph it refers to the Chen reference 1008?

17 A Yes, I do.

18 Q Okay. So I'm going to introduce two
19 exhibits. The first exhibit is TSMC Exhibit 1008,
20 which is U.S. Patent Number 7,449,753 to Wang,
21 W-a-n-g, et al.

22 (Exhibit 1008 discussed.)

1 And the second one is TSMC Exhibit 1009,
2 which is U.S. Patent Number 7,591,659 to Chen,
3 C-h-e-n, et al.

4 (Exhibit 1009 discussed.)

5 Q Do you have those exhibits?

6 A When you give it to me, yes.

7 Q Do you have both of those exhibits now?

8 A Clearly exhibit number is not right.

9 Q Okay. You are getting ahead of me. I
10 just want to clarify it for the record.

11 A Yes.

12 Q So in paragraph 5 when you refer to the
13 Chen reference, you are referring to Exhibit 1009,
14 correct?

15 A That's correct.

16 Q Okay. So if I refer to -- you can put
17 aside the Exhibit 1008.

18 A Okay.

19 Q If I refer to Chen today, you will
20 understand I'm talking about Exhibit 1009?

21 A That would be correct, yes.

22 Q Okay. And I'm going to hand you what I

1 would like to be marked Exhibit 1215.

2 (Exhibit 1215 marked.)

3 Q You can check me if you would like, I will
4 just represent to you that Exhibit 1215 is a clean
5 copy of Chen's Figure 3. Let me know if you agree
6 with that characterization?

7 A It appears to be.

8 Q All right. Could you please use this red
9 marker to circle what you understand in Chen's
10 Figure 3 to be the gate or, I guess, I should --
11 circle is probably the wrong word. I guess
12 outline what you consider to be the gate, please?

13 A Thank you. It would be difficult to draw
14 a circle.

15 Q Yes.

16 A (Witness complies.)

17 Q Are you done?

18 A I'm done.

19 Q May I look at that, please? Thank you.

20 Could you please turn to column 4 of Chen?

21 A I'm at column 4.

22 Q And the sentence that begins on line 31

1 going over to line 32 that says, Preferably the
2 gate dielectric layer is oxide or silicon
3 oxynitride depending on the environment.

4 Do you see that?

5 A The line numbers again?

6 Q 31 to 32?

7 A Yes, that's what it says.

8 Q Okay. So you understand that Chen's gate
9 dielectric layer may be silicon oxide or silicon
10 oxynitride, right?

11 A Preferably, yes.

12 Q Let's go to the sentence that begins on
13 line 51 going to line 53. Are you with me?

14 A All right.

15 Q It says, the sidewall spacers are often
16 made of a dielectric material, such as silicon
17 dioxide, silicon nitride or any combination of
18 these, and the like.

19 Do you see that?

20 A Yes, I do.

21 Q Do you agree that Chen's gate dielectric
22 layer and sidewall spacers are made of the same or

1 similar insulating materials?

2 A It can be.

3 Q So for example, both could be silicon
4 dioxide, right?

5 A Both can be silicon dioxide. The
6 deposition methods are probably different, but in
7 terms of composition, yes, they can both be
8 silicon dioxide or silicon nitride.

9 Q Okay. All right. Turn to page 22 of
10 Exhibit 2003, please.

11 A Page 20?

12 Q Page 22, correct.

13 A Okay, got it.

14 Q There is an annotated version of Chen's
15 Figure 3 here, correct?

16 A Yes.

17 Q And are those your annotations?

18 A Yes.

19 Q And so specifically there are purple, blue
20 and red annotations here, correct?

21 A Correct.

22 Q And the purple annotation reads, relative

1 side of gate. Do you see that?

2 A Yes.

3 Q Okay. Keep that open and let's also look
4 at the claim 1 again of the '847 patent.

5 So the second limitation in claim 1
6 recites two raised epitaxial layers positioned
7 respectively in the semiconductor substrate next
8 to the relative sides of the gate.

9 Do you see that?

10 A Yes.

11 Q And so when you refer to relative side of
12 gate in purple on page 22 of Exhibit 2003, are you
13 referring to the -- one of the relative sides of
14 the gate recited in the second element of claim 1?

15 A Yes. And the relative side of the gate as
16 is shown in 22 when I annotated Figure 3, I'm
17 talking about the gate oxide which is part of the
18 gate. I'm not talking about the side -- I'm not
19 talking about the sidewall, just the gate oxide.

20 Q Okay. Thank you for that clarification.

21 Again, let me -- let me ask. So when you
22 say relative side of gate in purple, you are

1 referring to the claimed -- one of the claimed
2 relative sides of the gate in the second element
3 of claim 1; is that fair?

4 A That's what I'm referring to, right.

5 Q Okay.

6 A So it is the right edge of the gate oxide.

7 Q Okay. If we look at the last element of
8 claim 1 at the top of column 8 it says, two doped
9 region formed respectively in the semiconductor
10 substrate next to the relative sides of the gate.

11 Do you see that?

12 A Yes.

13 Q Okay. And so again, this purple
14 annotation, "relative side of gate," in Exhibit
15 2003 page 22, you are referring to one of the
16 relative sides of the gate recited in the last
17 limitation of claim 1 as well, right?

18 A Yes. Again, the rightmost edge of the
19 gate oxide as I depict on Figure 3 on page 22 of
20 my -- of Exhibit 2003.

21 Q Okay. And looking at the annotated image
22 on page 22, your second declaration, is it your

1 position that the epitaxial layer outlined in red
2 is not positioned next to the side of the gate
3 that you indicated in purple?

4 A Yes. I think I made statements in my
5 declaration to the fact that the epitaxial layer
6 actually goes underneath the gate.

7 Q Okay. And so in your view if it goes
8 under the gate at all, it is not next to the side
9 of the gate; is that right?

10 A Well, I'm looking at specifically the way
11 in which Chen, Exhibit 1009, is being represented
12 as art relevant to the '847 patent. And I'm
13 saying specifically that in that particular
14 reference that the epitaxial layer that has been
15 defined here goes underneath the gate and is not
16 next to the relative side of the gate.

17 Q Okay. So looking at the figure on page 22
18 of your second declaration, do you agree that
19 there is a large portion of the epitaxial layer
20 identified in red that is to the right of the
21 purple line that you drew?

22 A Well, the representation in the -- in the

1 drawing would give some indication that it was to
2 the right of that gate oxide, but also goes down
3 underneath the oxide. And there is nothing in the
4 specification that supports the fact that it would
5 go above the substrate. So again, it is a matter
6 of the context of the drawing as -- as supported
7 by the specification, but it does go under the
8 gate.

9 Q So in paragraph 49 you say that the
10 epitaxial layer is under the gate dielectric layer
11 rather than, quote, next to the relative sides of
12 the gate, closed quote, as required by limitation
13 1B; is that right?

14 A That's correct.

15 Q And that is your opinion?

16 A Correct.

17 Q Okay. What is the plain meaning of the
18 phrase "next to" in your opinion?

19 MR. LU: Object to form.

20 A Beside.

21 Q Okay. And so is it your position that
22 limitation 1B precludes any portion of the

1 epitaxial layer from extending underneath the
2 epitaxial layer or -- excuse me, strike that.

3 Is it your position that limitation 1B, as
4 you call it here in paragraph 49, precludes any
5 portion of the epitaxial layer from extending
6 underneath part of the gate dielectric layer?

7 A I believe the claim requires it to be next
8 to. And the specification of the '847 in terms of
9 utilizing the -- I'm answering yes by the way, but
10 the specification deposition of the epi is
11 specifically the epi to -- that is -- that is
12 grown in the -- in and above the recess.

13 And the recess is created using the gate
14 as the mask, and so therefore, the edge of the
15 recess does not go underneath the gate, and
16 therefore, the epi that is built in that recess
17 would not go underneath the gate.

18 Q I see. Does it say in the '847 patent
19 that that edge has to be perfectly anisotropic and
20 cannot undercut the gate?

21 A I don't think it says that, but let me
22 clarify. If you have this particular structure

1 where you are not displacing and you are actually
2 creating it according to this claim where you are
3 using the gate to create the side at which you are
4 going to cut the recess, you are actually getting
5 the -- the recess and the epitaxial growth is
6 going to be at that edge, it is going to be next
7 to.

8 And because of that if you begin to
9 undercut, you are actually getting into the
10 channel and that is going to create a -- a anomaly
11 within the channel. So I think the patent is very
12 specific on creating it next to --

13 Q Okay. So --

14 A -- and not getting underneath the channel
15 as Chen has done or underneath the oxide and
16 moving into the channel.

17 Q I see. So in your view the channel is
18 formed underneath the entire gate sidewall; is
19 that right?

20 MR. LU: Object to form.

21 A The channel here is going to be that which
22 exists between the drain and the source. And if

1 the epi and the epilayer is providing that, then
2 obviously the -- when you activate the gate you
3 provide a voltage to the gate itself that sits
4 above the gate oxide. That is going to arbitrate
5 what happens in the channel underneath that gate
6 oxide.

7 Q The entire gate oxide?

8 A Yes.

9 Q Okay. So no matter how wide the gate
10 oxide is, when you apply voltage to the channel is
11 going to create -- excuse me, to the gate
12 electrode, it is going to create a channel
13 underneath the entire width of the gate
14 dielectric; is that right?

15 A Unfortunately, yes. It is -- when you
16 start to look at a gate oxide, it is literally
17 aligned with the edges of the gate itself. And
18 you look at the channel aligned with that gate,
19 you have got control on a homogenous basis of the
20 transport of the electrons or holes in that
21 channel.

22 When you begin to take the gate oxide out

1 beyond that, you are going to -- it is not going
2 to have a homogenous effect. It is going to have
3 a degrading effect, but it is still going to
4 create a contribution to the channel, but it is
5 going to be graded.

6 Q Okay. And do you have any idea how far
7 such fringing effects would reach anything you can
8 cite to or point me to to suggest that it would go
9 the entire width of the gate dielectric?

10 MR. LU: Object to form.

11 A Well, that depends upon the instantiation,
12 but in typical MOS technology you obviously have
13 some constraints. If you run a 20 nanometer
14 technology, you are certainly not going to go very
15 far. You've basically damaged and taken away from
16 the fact you are running 20 nanometer technology.

17 Q Okay.

18 A So in terms of the actual extent it
19 depends upon the particular instantiation, the
20 voltage levels used, the material content that is
21 used.

22 Q Okay. So in your view, if the gate

1 dielectric overlaps the source drain region, the
2 channel would be formed within the source drain
3 region itself?

4 A Say that again.

5 Q If the gate dielectric overlaps the source
6 drain regions, would the channel be formed in the
7 source drain region itself?

8 A No.

9 Q Okay.

10 A There is based upon this design with the
11 overlap, there is an effect on that particular
12 overlapped region of the source drain, but the
13 channel would be what is the area under the gate
14 oxide between the source and the drain.

15 Q Okay.

16 A By doing a design like this basically --
17 you are basically shortening the channel under
18 that gate, but you do it in such a way that the
19 gate itself when it is activated is going to have
20 an effect on that particular part of the source
21 and drain that undercuts the gate oxide.

22 Q Okay. The gate oxide by definition is

1 highly insulating, right?

2 A The gate oxide is an insulator.

3 Q Okay. And it is by definition highly
4 insulating, right?

5 A I'm not sure what you mean by highly.

6 Q I mean, you do not want current to leak
7 between the gate electrode and anything below it,
8 right?

9 A You would like to not have a charged
10 transfer between the gate above and the channel
11 below --

12 Q Right.

13 A -- unless it is a flash.

14 Q Right. And so let's get back to the --
15 the '847 patent.

16 I think the question I asked is, so in
17 your view, does limitation 1B as you refer to it
18 in paragraph 49 of your second declaration, does
19 that preclude any portion of the epitaxial layer
20 from extending underneath part of the gate
21 dielectric layer, yes or no?

22 MR. LU: Objection, asked and answered.

1 A First to answer that question, I would
2 have -- if I was going to look at a particular
3 other patent or product in terms of whether or not
4 it practices or doesn't practice, I would look at
5 the merits of what that particular patent teaches
6 or what that product does.

7 This is not a product analysis, so I
8 haven't done any analysis on that type of thing.
9 But in looking at the way the claim is written,
10 what is required as compared to what Chen produces
11 there is a mismatch.

12 Q Okay. And let me -- let me just ask
13 again. So yes, no or I can't answer yes or no, is
14 it your position that the language of claim
15 limitation 1B as you've referred to in paragraph
16 49 of your second declaration precludes any
17 portion of the epitaxial layer from extending
18 underneath part of the gate dielectric layer?

19 MR. LU: Same objection.

20 A If -- if -- if the representation you are
21 making is consistent with what Chen is showing,
22 then that precludes it.

1 Q Okay. Same question for the last
2 limitation.

3 A Okay.

4 Q The 2 doped region at the top of column 8
5 of the '847 patent. Is it your position that that
6 limitation precludes any portion of the doped
7 regions from extending underneath any part of the
8 gate dielectric layer?

9 A No.

10 Q Okay. So part of the doped region can
11 extend underneath part of the gate dielectric
12 layer in the last limitation of Claim 8, right?

13 A The -- the reason I say that is because
14 the -- the formation of the recess provides a
15 physical boundary. And the growth of the epi is
16 within that physical boundary.

17 Here when you are talking about 2 doped
18 regions, once the dope is implanted and then
19 diffused it could extend. That depends upon the
20 way in which the process dopes the material or
21 diffuses the material.

22 Q Okay. So just to be clear, it is your

1 position that the epilayer itself cannot extend
2 under the relative side of the -- relative
3 sides -- excuse me.

4 It is your position that no part of the
5 epitaxial layer can extend beneath part of the
6 gate dielectric layer, however, part of the two
7 doped regions may extend underneath part of the
8 gate dielectric layer; is that right?

9 A The answer is yes, because the two doped
10 regions are formed respective to the relative
11 sides of the gate, right. It says 2 doped formed
12 respectively in the semiconductor substrate next
13 to the relative sides of the gate.

14 And as I said, when you are doping, when
15 you are implanting, the gate itself is going to
16 provide that boundary. And so the boundary is the
17 implants actually will be bounded by that gate
18 next to the gate.

19 Now, once you go through the diffusion,
20 the high temperature diffusion process, it could
21 migrate below the gate, but in terms of the
22 instantiation it would be implanted next to the

1 gate.

2 Q You told me the plain meaning of "next to"
3 is beside, right?

4 A Correct.

5 Q Do you have an understanding what the
6 plain meaning of "adjacent to" is?

7 A Plain meaning of what?

8 Q "Adjacent to"?

9 A Yes, a little bit more restrictive.

10 Q More restrictive?

11 A Yes.

12 Q How so?

13 A Well, adjacent would indicate some -- I
14 just think it is closer.

15 Q Okay. Would you consider something that
16 is adjacent to the gate dielectric layer to be
17 next to the gate dielectric layer?

18 A I think it would fall within the
19 guidelines of next.

20 Q If you want to break, now is a good time
21 for it.

22 A I will keep going.

1 Q If you are good to keep going.

2 MR. LONG: Are you good?

3 COURT REPORTER: I'm fine.

4 A I will defer to you.

5 Q Could you turn to paragraph 74 of your
6 second declaration? And we're still talking about
7 the Chen reference in paragraph 74, correct?

8 A Yes, that's correct.

9 Q And the fourth line in to that paragraph
10 the sentence reads, but Figure 5 is not a, quote,
11 MOS transistor structure, closed quote, because it
12 is not a transistor.

13 Do you see that?

14 A Yes, I see that.

15 Q Okay. And so you agree that Figure 5 of
16 Chen would not function as a transistor; is that
17 right?

18 A Well, if you look at the next sentence I
19 have basically positioned that also in terms of
20 the petitioner's expert.

21 Q Okay. And do you agree with that
22 position?

1 A Yes.

2 Q Okay. And --

3 A Not complete.

4 Q Right. And it can't be operated as a
5 transistor, because it doesn't have any electrical
6 contacts to the source drain or gate; is that
7 right?

8 A That is correct.

9 Q Okay.

10 A It does not have.

11 Q Do any of the claims of the '847 patent
12 require contacts to the source drain and/or gate?

13 A It requires a MOS transistor.

14 Q Okay. And does it require electrical
15 contacts to the source drain or gate?

16 MR. LU: Objection, calls for a legal
17 conclusion.

18 A I don't see any limitations that add
19 electrical contacts into the words, but if it is
20 not a MOS transistor structure that can be
21 electrically connected to, then it is not a
22 completed structure.

1 Q Okay. But do any claims in the '847
2 patent require electrical contacts to the source
3 drain or gate?

4 MR. LU: Asked and answered.

5 A I believe I answered that, that that is
6 not part of the claim limitation.

7 Q Okay. When you say it is not part of the
8 claim limitation, do you mean that it is not
9 required in order to practice the claims of the
10 '847 patent?

11 MR. LU: Same objection.

12 A The patented claim -- claims are directed
13 to a MOS transistor structure, not the electrical
14 connections part of it.

15 Q Okay. But in your view, does a structure
16 have to have contacts to the source drain and gate
17 to satisfy claim 1?

18 MR. LU: Same objection.

19 A Again, having contacts is what you would
20 do with that MOS transistor to put it into an
21 actual operative product, but it has to be a MOS
22 transistor that can do that. So in Figure 5, you

1 do not have such a structure, because at that
2 point you have no way to access the poly. You
3 have no access -- no access to the gate.

4 Q Okay.

5 A So it is not a MOS transistor at that
6 stage and the petitioner expert agreed with that
7 as well.

8 Q And that is because there is no access to
9 make a contact to the gate in Figure 5 of Chen,
10 correct?

11 A Yes.

12 Q Okay. Could you turn to Figure 14 of the
13 '847 patent?

14 A Go ahead.

15 Q Okay. Does Figure 14 of the '847 patent
16 illustrate any electrical contacts to the source
17 drain or gate?

18 A Not in Figure 14, no.

19 Q Does the specification describe how to
20 form electrical contacts to the source drain or
21 gate of the structure in Figure 14?

22 A I don't believe as I sit here looking

1 through the specification that it goes into any
2 detail about the electrical connections after you
3 complete the structure.

4 Q And when you say complete the structure,
5 you are referring to the structure on Figure -- in
6 Figure 14, right?

7 A Right, and this completed structure
8 includes all of what was required by the claim.

9 Q Okay. Figure 14 also doesn't illustrate
10 any interconnections between MOS transistor
11 structures, correct?

12 A No, it does not.

13 Q You would need that for a functioning
14 circuit, right?

15 A Well, for a functioning circuit, when
16 you -- when you take the particular transistor
17 that is invented and you put that into a circuit
18 then obviously there would be additional
19 connections in order to create the circuit.

20 Q And in order to make those
21 interconnections you would need contacts to the
22 structures we see on the left and right side of

1 Figure 14, right?

2 A Eventually you would, yes.

3 Q Let's turn to Figure 5 of the '847 patent.

4 MR. LU: Is now a good stopping point,
5 counsel? We have been going for an hour and a
6 half.

7 MR. LONG: Let me finish this line of
8 questioning and if you need a break we will take
9 one.

10 MR. LU: Okay.

11 A Okay.

12 Q Now, Figure 5 also does not illustrate
13 electrical contacts to the source drain or gate,
14 correct?

15 A That is correct, it is the MOS structure.

16 Q And does the specification describe how to
17 form electrical contacts to the source drain or
18 gate of the structure in Figure 5 of the '847
19 patent?

20 A No, that would be done after the formation
21 of the transistor.

22 Q Okay. Let's go off the record.

1 (Recess, 10:42 to 11:03 a.m.)

2 Q Welcome back, Mr. McAlexander.

3 A Nice to be back.

4 Q You know you are supposed to tell the
5 truth, right. Sorry, I shouldn't make jokes.

6 A I love my job.

7 Q All right. If you could turn to paragraph
8 59 of your second declaration kind of spills on to
9 page 26, so I guess I should say page 26, please.

10 A Okay, paragraph 59, okay.

11 Q The second to last sentence it says, thus,
12 the petitions proposed modification of Lan
13 retaining the gate cap layer is unworkable,
14 because it would create a further problem of
15 blocking access to the gate conductive layer.

16 Do you see that sentence?

17 So we're in Exhibit 2003, page 26?

18 A Amazing what you see when you print it
19 rather than on a computer. This error that is in
20 paragraph 59.

21 Q There is an error. I'm asking about the
22 sentence after that.

1 A Okay.

2 Q So let me ask again. So do you see the
3 sentence that says, thus, the petition's proposed
4 modification in Lan retaining the gate cap layer
5 is unworkable because it would create a further
6 problem of blocking access to the gate conductive
7 layer?

8 A Yes, I do.

9 Q When you refer to the problem of blocking
10 access to the gate connective layer, you are
11 referring to the problem of making electrical
12 contact to the gate, correct?

13 A That's correct, as -- as instantiated by
14 Lan what he was creating, that's correct.

15 Q Does retaining the gate cap layer in the
16 '847 patent block access to the gate conductive
17 layer?

18 A It will not eventually once contact is
19 made typically using a mask or something like that
20 to make contact in the specific points.

21 Q Okay. Does the '847 patent describe how
22 to make electrical contact to the gate?

1 A I believe that was asked before. That
2 was -- that is beyond the particular scope of what
3 this specification is talking about, the '847
4 patent.

5 Q Okay. And does -- okay.

6 Shift gears a little bit and talk about
7 silicidation. Do you agree that silicidation is a
8 process by which metal is deposited on silicon and
9 centered to form a layer resistance electrical
10 contact region?

11 A That is a good general description of it,
12 yes.

13 Q Okay. Do you agree that performing a
14 silicidation process directly to a metal gate
15 would not create a silicide on the metal gate?

16 A Say that again, please.

17 Q Do you agree that performing a
18 silicidation process directly on a metal gate
19 would not create a silicide on the metal gate?
20 Let me strike that and ask it again to be more
21 specific.

22 Referring to the definition of

1 silicidation that we just discussed.

2 A And state that again for me.

3 Q Yes. So you generally agree that
4 silicidation is a process by which a metal is
5 deposited on silicon and centered to form a layer
6 resistance electrical contact region, correct?

7 A That is generally correct. It could be a
8 silicon single crystal, it could be poly, it could
9 be doped.

10 Q Right. And do you agree that performing
11 such a silicidation process directly to a metal
12 gate would not create a silicide on the metal
13 gate?

14 A If one were to use a metal gate, it would
15 not fall under direct definition that we just
16 agreed to as far as silicidation. You would be
17 forming a -- depositing -- depositing or sputtering
18 a metal on top of another metal and you create an
19 interface between the two. When you do center it
20 or they call it anneal, there could then be a
21 superposition and a homogenous collection between
22 the two metals.

1 Q Okay. So you could form a metal alloy,
2 for example?

3 A Yeah, you could. Basically it is at that
4 interface.

5 Q Okay.

6 A It depends upon the particular metals as
7 to how far that annealing diffuses the atoms.

8 Q Uh-huh. And that would not be a silicide
9 though, right?

10 A Not by the definition that we talked about
11 earlier.

12 Q Would it be a silicide by any definition?

13 A That -- that does not fall within the
14 scope. That is basically metal to metal --

15 Q Okay.

16 A -- and alloy.

17 Q Do you agree that gate resistance is a
18 function of gate electrode thickness?

19 A Gate thickness is a contribution to
20 resistance.

21 Q Okay. And do you agree that a nonuniform
22 gate resistance can result if the thickness of the

1 gate is nonuniform?

2 MR. LU: Object to form.

3 A I will let you state that a different way.
4 It doesn't make sense.

5 Q I'm sorry, maybe I misspoke.

6 Do you agree that a nonuniform thickness
7 of the gate electrode can lead to a nonuniform
8 gate resistance?

9 A I'm questioning what you mean by
10 nonuniform gate thickness.

11 Q Across a wafer?

12 A Okay.

13 Q Not within a single device --

14 A Okay.

15 Q -- across a wafer.

16 A Thank you, thank you. Now it make sense.

17 If you have a nonuniformity across a
18 wafer, then you could have differences in terms of
19 resistance on any particular given common element
20 from one circuit to another.

21 Q Do you agree that nonuniform gate
22 resistance can result in nonuniform switching and

1 nonuniform power distribution across a wafer?

2 A There is a chance for that. It depends
3 upon how the circuit has been designed. Most
4 circuits are designed to accommodate such
5 variations because they take into context where
6 that circuit is on the wafer.

7 In other words, since I see you
8 questioning that, when you take a particular
9 transistor and you put that into a circuit, that
10 circuit is going to be then stepped across the
11 wafer. So the question is, based upon the way you
12 have nonuniformity, have you accounted for that in
13 your design so that you can make sure that your
14 distribution is such that you still have a
15 workable product.

16 Q Is nonuniformity in semiconductor
17 processing uniform from wafer to wafer in your
18 experience?

19 MR. LU: Object to form.

20 A Well, there is two aspects to this. If
21 you are talking about within a wafer, it goes to
22 the planarity and the way you process it as to how

1 far out you get. Now, obviously the circuits that
2 are out at the periphery are going to have some
3 outlier characteristics that are different from
4 towards the center, but that is -- again that is
5 processing.

6 You will have a differentiation from wafer
7 to wafer, you could. That depends again upon
8 the -- the in situ aspect. If you are looking at
9 it on a diffusion tube basis, when you have a lot
10 of multiple wafers in a carousel or a boat that is
11 in a diffusion tube, its location in that
12 diffusion tube is going to have some
13 differentiation.

14 When you look at it as sputtering, again,
15 you might have some differentiation. If you
16 take -- if you takeaway the vacuum and then
17 reevacuate it. So there will be some variations
18 within the process, that is typical.

19 Q And with etching too, right?

20 A I would say all processes have potential
21 variations, certainly.

22 Q Do you agree that contact resistance is a

1 function of interface quality between the
2 electrode and the contact?

3 A The interface plays a major role in that
4 resistance.

5 Q Can you turn back to Chen, please? It is
6 Exhibit 1009.

7 A Okay.

8 Q Are the figures in Chen drawn to scale?

9 A There is no scale identified, so they're
10 not drawn to scale.

11 Q Does Chen's specification disclose any
12 dimensions for the widths of the sidewall spacers?

13 A I don't recall it giving any dimensions
14 whatsoever, but basically it does not state that
15 you can depend on the drawings in terms of any
16 scale. I don't see elaboration in the
17 specification for that.

18 Q Okay. Let me hand you exhibit TSMC
19 Exhibit 1005, which is the Lan reference, U.S.
20 Patent Number 7,935,590.

21 (Exhibit 1005 discussed.)

22 Q Are the figures in Lan drawn to scale?

1 A Not as I recall, no.

2 Q Does the specification in Lan disclose any
3 dimensions for the widths of the sidewall spacers?

4 A I don't recall it showing any dimensions
5 as it applies to the sidewall spacers.

6 Q I'm going to hand you a copy of TSMC
7 Exhibit 1006, the Liaw, L-i-a-w, US Patent Number
8 7,026,689.

9 (Exhibit 1006 discussed.)

10 A Thank you.

11 Q Are the figures in the Liaw reference
12 drawn to scale?

13 A No.

14 Q Does the specification in Liaw disclose
15 any dimensions for the widths of the sidewall
16 spacers?

17 A I don't see anything in here that draws
18 anything to a dimension on the sidewall spacers.

19 Q Okay. Let's go off the record.

20 (Recess, 11:16 to 11:29 a.m.)

21 Q So Mr. McAlexander, did you at any point
22 during either the breaks today speak with counsel

1 about the substance of your testimony?

2 A No, I did not.

3 Q Did counsel speak about the substance of
4 your testimony within your earshot?

5 A No.

6 Q Did counsel write anything down about the
7 substance of your testimony that you can see?

8 A No.

9 MR. LONG: I pass the witness.

10 EXAMINATION

11 BY MR. LU:

12 Q I just have a few questions.

13 First of all, Mr. McAlexander, in total,
14 how many years of work experience do you have in
15 the design and manufacturing of transistors
16 including MOSFETs?

17 A Well, if the design and manufacturing
18 includes consulting with -- with companies that
19 design and manufacture, I've got 54 years of
20 experience total.

21 Q And can you just walk me through your
22 education and experience in the design and

1 manufacturing of transistors including MOSFETs?

2 A Well, when it goes back to academic, my --
3 my discipline was electrical engineering was
4 specifically focused on solid state, which is the
5 basic physics that go into MOS development.

6 Tenure wise I was involved with Texas
7 Instruments designing static random access
8 memories, circuits that go into microcontrollers,
9 flash memory, EPROM, EEPROM, and those were the
10 principal ones. But then as a manager of the
11 entire cost center for Texas Instruments for
12 several years, I actually ran the operation for
13 everything from design to fab to assembly,
14 reliability analysis, and marketing. So I was
15 very fortunate to be involved in all phases of
16 that.

17 Subsequent to that, I joined a company
18 with my former design manager. He formed a
19 company in Richardson, Texas and for five years I
20 operated as the vice president of technology. And
21 there I built my now third scanning microscopy
22 laboratory to do reverse engineering of failure

1 analysis of components. And -- and did -- and
2 therefore, had contracting arrangements with a
3 number of semiconductor companies on analysis of
4 their products to determine what to do to modify
5 the design of those products in order to improve
6 performance and reliability.

7 I then spent 12 years with another
8 company, that its -- its main products were
9 underwater dive computers, so I was working with
10 them on the -- on the integration of components,
11 not the actual design of the MOS transistor but
12 the integration of the components in systems that
13 would operate wirelessly underwater and provide
14 all the sensing mechanisms for keeping divers
15 safe.

16 In addition to that, as a part of that
17 company, I also was contracted by TI to work on
18 the FeRAM product, and was also working jointly
19 with TI on their DLP products.

20 And I will just finish off by saying that
21 during the time from the early 1990s to about
22 2016, I was a consultant with STMicroelectronics.

1 I worked not only directly with their designers on
2 some of their products at the transistor level, I
3 also have several patents that -- that came out of
4 some of that analysis.

5 And I also provided consultation with that
6 company on their entire patent portfolio every
7 year for about 15 years. And that was now
8 reviewing the inventions across the MOS transistor
9 products both -- both the design and wafer
10 processing. And so I became intimately familiar
11 with the particular integration of designs at that
12 time at the node levels where it is state of the
13 art.

14 So that is kind of my experience in MOS
15 transistor technology. It is -- I've been blessed
16 to have quite a few years working in that
17 technology.

18 Q Okay, thank you. And the last thing real
19 quick, can you turn to page 26 of Exhibit 2003,
20 which is your second declaration?

21 A Which page again?

22 Q Page 26.

1 A Yes, sir.

2 Q Do you see at the top the second line
3 there is an error, reference source not found?

4 A Yes, I do.

5 Q What section of your declaration is that
6 referring to?

7 A That actually refers back to the
8 semiconductor transistor technology Section 5.
9 That does not appear on my computer. When I
10 looked at the printout, the system generated an
11 error. There was a link that did not transfer to
12 the PDF, but Section 5 is what it should be, Super
13 Section 5.

14 MR. LU: Okay. Thank you I have nothing
15 further at this time.

16 MR. LONG: Nothing further for me.

17 (Deposition adjourned at 11:35 a.m.)

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19

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22

CERTIFICATE OF SHORTHAND REPORTER

I, Susan S. Klinger, Certified Reporter
before whom the foregoing deposition was taken, do
hereby certify:

That JOSEPH C. McALEXANDER, III, the
witness whose deposition is hereinbefore set
forth, was duly sworn by me before the
commencement of such deposition, and that such
deposition was taken before me and is a true
record of the testimony given by such witness,
that said testimony was taken by me
stenographically and thereafter reduced to
typewriting under my direction.

I further certify that the adverse party,
Marlin Semiconductor was represented by counsel at
the deposition.

I further certify that the deposition of
JOSEPH C. McALEXANDER, III, occurred on
the 17th of March, 2026, commencing at 9:05 to
11:35.

I further certify that reading and signing

1 was not discussed.

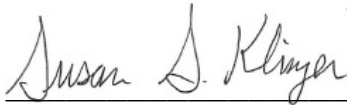
2 I further certify that I am not related to
3 any of the parties to this action by blood or
4 marriage, I am not employed by or an attorney to
5 any of the parties to this action, and that I am
6 in no way interested, financially or otherwise, in
7 the outcome of this matter.

8 IN WITNESS WHEREOF, I have herunto set my
9 hand on the 18th of March, 2026.

10

11

12

A handwritten signature in cursive script, reading "Susan S. Klinger", is written over a horizontal line.

13

Susan S. Klinger, RMR-CRR, CSR

14

Texas CSR 6531, Exp: 10/31/27

15

California CSR 14487, Exp: 11/30/26

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Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

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A			
ability	accurate	addition	80:13, 80:17,
6:19	10:3, 11:8,	90:16	81:3, 81:10,
about	20:7, 20:19,	additional	82:17, 82:21,
8:2, 8:8, 8:11,	43:11	11:7, 23:13,	83:6, 83:21,
9:22, 12:12,	accurately	41:3, 43:7,	85:22
12:18, 15:6,	6:3	76:18	agreed
17:17, 28:15,	acoustic	address	75:6, 81:16
28:16, 29:4,	17:12, 17:13,	48:9	agreements
31:15, 33:1,	18:8	addressing	7:18
34:8, 34:10,	across	46:2, 46:12,	ahead
34:11, 34:14,	83:11, 83:15,	48:10	9:2, 54:9,
35:6, 39:19,	83:17, 84:1,	adjacent	75:14
40:20, 40:21,	84:10, 91:8	71:6, 71:8,	aid
51:11, 54:20,	action	71:13, 71:16	26:21
58:17, 58:18,	94:3, 94:5	adjourned	airbag
58:19, 69:17,	activate	92:17	34:4
72:6, 76:2,	64:2	advanced	al
78:21, 80:3,	activated	10:14	53:21, 54:3
80:6, 82:10,	66:19	advent	aligned
84:21, 88:1,	active	45:13	64:17, 64:18
88:3, 88:6,	40:22	adverse	all
90:21, 91:7	activities	93:15	13:4, 14:3,
above	19:18, 20:1,	after	44:1, 51:16,
41:3, 50:17,	20:21, 21:7,	30:4, 32:6,	55:8, 56:14,
51:1, 61:5,	21:16, 24:8,	42:9, 52:2,	57:9, 60:8,
62:12, 64:4,	24:16, 24:21,	76:2, 77:20,	76:8, 78:7,
67:10	25:4	78:22	85:20, 88:13,
absolutely	acts	again	89:15, 90:14
28:6	51:2	8:10, 12:8,	alloy
academic	actual	14:5, 14:9,	82:1, 82:16
89:2	26:14, 29:5,	24:22, 26:18,	already
accept	29:10, 37:19,	28:17, 32:6,	9:3, 42:13
15:11	65:18, 74:21,	33:19, 38:8,	also
access	90:11	48:7, 56:5,	5:8, 5:12, 6:6,
75:2, 75:3,	actually	58:4, 58:21,	29:14, 32:16,
75:8, 78:15,	21:4, 21:10,	59:13, 59:18,	41:5, 41:19,
79:6, 79:10,	26:3, 30:13,	61:5, 66:4,	58:3, 61:2,
79:16, 89:7	34:12, 37:11,	68:13, 74:19,	72:19, 76:9,
accommodate	37:16, 37:18,	79:2, 80:16,	77:12, 90:17,
84:4	38:3, 39:22,	80:20, 81:2,	90:18, 91:3,
according	42:13, 60:6,	85:4, 85:7,	91:5
12:15, 14:5,	63:1, 63:4,	85:14, 91:21	alter
63:2	63:9, 70:17,	against	41:5
accounted	89:12, 92:7	23:7	always
84:12	add	agree	40:15
accuracy	73:18	55:5, 56:21,	amazing
15:9	added	60:18, 72:15,	78:18
	52:20	72:21, 80:7,	ams
			15:18

analysis 68:7, 68:8, 89:14, 90:1, 90:3, 91:4 anisotropic 62:19 anneal 81:20 annealing 82:7 annotated 57:14, 58:16, 59:21 annotation 57:22, 59:14 annotations 57:17, 57:20 anomaly 63:10 another 21:7, 21:10, 81:18, 83:20, 90:7 answer 6:1, 6:14, 6:16, 22:16, 23:3, 46:22, 50:16, 68:1, 68:13, 70:9 answered 67:22, 74:4, 74:5 answering 6:8, 6:9, 62:9 any 6:19, 19:17, 19:22, 20:20, 21:15, 24:6, 24:7, 24:21, 25:11, 28:4, 28:8, 30:5, 32:7, 40:14, 41:7, 41:8, 41:10, 42:8, 46:5, 46:8, 47:12, 49:18, 56:17, 61:22, 62:4, 65:6,	67:19, 68:8, 68:16, 69:6, 69:7, 73:5, 73:11, 73:18, 74:1, 75:16, 76:1, 76:10, 82:12, 83:19, 86:11, 86:13, 86:15, 87:2, 87:4, 87:15, 87:21, 94:3, 94:5 anything 6:18, 6:20, 7:13, 65:7, 67:7, 87:17, 87:18, 88:6 apologies 13:4 appeal 1:3 appear 92:9 appeared 49:19 appears 41:6, 55:7 applicable 46:3, 46:21 applies 48:11, 87:5 apply 64:10 approximately 14:6 arbitrate 64:4 area 32:2, 50:18, 66:13 around 49:9 arrangements 90:2 art 35:1, 35:3, 46:8, 46:10, 47:12, 47:20,	47:22, 48:9, 60:12, 91:13 articles 40:12, 40:17 aside 54:17 asked 67:16, 67:22, 74:4, 80:1 asking 8:11, 78:21 aspect 22:18, 23:6, 28:10, 85:8 aspects 26:12, 84:20 assembly 89:13 assigned 22:8, 23:21, 24:6, 24:15, 34:1 associated 13:22 assume 5:18 atoms 82:7 attached 4:15 attorney 94:4 attorneys 3:3, 3:11 august 9:15, 49:7, 49:8 automotive 16:11, 16:14 available 28:14, 47:2 avenue 3:7 away 65:15 B b2 1:12	bachelor 10:10 back 17:16, 40:11, 48:5, 53:10, 67:14, 78:2, 78:3, 86:5, 89:2, 92:7 background 47:6, 47:20, 50:4 backwards 24:11 based 15:4, 27:2, 66:10, 84:11 basic 48:17, 89:5 basically 27:15, 31:5, 47:4, 65:15, 66:16, 66:17, 72:19, 82:3, 82:14, 86:14 basics 48:14 basis 64:19, 85:9 beam 34:3, 41:15 beams 34:4 became 91:10 because 13:5, 13:12, 14:20, 20:3, 20:12, 20:22, 29:6, 31:13, 33:22, 36:14, 44:13, 63:8, 69:13, 70:9, 72:11, 73:5, 75:1, 75:8, 78:14, 79:5, 84:5 been 5:3, 5:15, 7:3,
--	---	---	--

8:3, 8:4, 8:19, 8:21, 11:8, 11:16, 13:19, 19:16, 19:21, 20:20, 21:3, 32:4, 38:2, 38:16, 39:11, 39:15, 48:9, 50:2, 51:11, 60:14, 77:5, 84:3, 91:15 before 1:3, 2:10, 5:16, 15:8, 39:6, 80:1, 93:4, 93:8, 93:10 begin 63:8, 64:22 beginning 44:1, 44:19, 44:21 begins 10:19, 17:21, 53:12, 55:22, 56:12 behalf 5:12, 7:4, 7:19, 21:7, 25:16 being 12:4, 14:13, 42:12, 50:13, 60:11 believe 14:22, 16:4, 35:15, 43:15, 47:14, 62:7, 74:5, 75:22, 80:1 below 67:7, 67:11, 70:21 beneath 70:5 beside 41:4, 61:20, 71:3	best 10:3, 43:11, 43:13 between 8:8, 33:5, 44:8, 45:4, 46:17, 51:2, 63:22, 66:14, 67:7, 67:10, 76:10, 81:19, 81:21, 86:1 beyond 10:14, 65:1, 80:2 bit 32:17, 71:9, 80:6 blessed 91:15 block 79:16 blocking 78:15, 79:6, 79:9 blood 94:3 blower 16:2 blue 57:19 board 1:3 boat 85:10 both 25:6, 28:13, 29:17, 46:3, 47:2, 47:3, 47:18, 48:12, 54:7, 57:3, 57:5, 57:7, 91:9 boundary 69:15, 69:16, 70:16 bounded 70:17 break 51:12, 51:17,	71:20, 77:8 breaks 87:22 brevity 9:20 bring 7:13 built 50:9, 50:13, 50:16, 62:16, 89:21 bullet 19:15, 24:5 C c-h-e-n 54:3 cad 27:11, 27:16, 27:17 california 3:15, 94:15 call 62:4, 81:20 called 11:17, 19:2 calls 52:14, 73:16 came 48:18, 48:22, 91:3 cameras 26:7 can't 27:7, 27:10, 35:6, 36:13, 49:15, 68:13, 73:4 cannot 62:20, 70:1 cap 78:13, 79:4, 79:15 capability 26:5 capable 34:21 capacitance 40:3	caption 13:8, 14:9 captions 13:19, 14:1 capture 14:21 carbide 39:20, 40:18 carlos 3:5, 5:7 carmel 3:14 carolina 10:11 carousel 85:10 case 1:11, 5:5, 13:8, 13:9, 13:14, 13:18, 13:22, 14:9, 21:9 cases 4:9, 7:16, 11:15, 11:21, 13:2, 13:7, 13:16, 13:18 center 81:19, 85:4, 89:11 centered 80:9, 81:5 ceo 19:6 certain 13:8 certainly 5:22, 15:8, 35:12, 65:14, 85:21 certificate 93:1 certified 2:11, 93:3 certify 93:5, 93:15, 93:18, 93:22, 94:2
--	---	--	---

chance 84:2 change 40:3 changes 50:3 channel 32:1, 39:16, 39:19, 40:2, 40:16, 41:8, 50:18, 51:2, 63:10, 63:11, 63:14, 63:16, 63:17, 63:21, 64:5, 64:10, 64:12, 64:18, 64:21, 65:4, 66:2, 66:6, 66:13, 66:17, 67:10 characteristics 85:3 characterization 55:6 characterize 50:12, 51:6 charge 40:4 charged 67:9 chart 12:21, 12:22 check 55:3 chen 53:16, 54:2, 54:13, 54:19, 55:20, 60:11, 63:15, 68:10, 68:21, 72:7, 72:16, 75:9, 86:5, 86:8 chen's 4:12, 55:5, 55:9, 56:8, 56:21, 57:14, 86:11 cigarette 16:6	cinema 26:4, 26:8 circle 55:9, 55:11, 55:14 circuit 27:18, 27:21, 36:7, 37:1, 76:14, 76:15, 76:17, 76:19, 83:20, 84:3, 84:6, 84:9, 84:10 circuits 37:2, 84:4, 85:1, 89:8 cite 65:8 claim 18:17, 51:20, 52:1, 58:4, 58:5, 58:14, 59:3, 59:8, 59:17, 62:7, 63:2, 68:9, 68:14, 69:12, 74:6, 74:8, 74:12, 74:17, 76:8 claimed 52:10, 52:12, 52:13, 53:2, 53:5, 59:1 claims 47:8, 73:11, 74:1, 74:9, 74:12 clarification 6:7, 37:18, 58:20 clarify 7:17, 19:20, 29:3, 37:10, 39:18, 54:10, 62:22 clean 55:4 clear 5:19, 15:2,	34:8, 69:22 clearly 12:3, 54:8 clients 25:16 closed 61:12, 72:11 closer 8:6, 71:14 cmos 36:6 co-invented 23:14 code 27:9 colleague 5:7 colleagues 30:13 collection 81:21 column 55:20, 55:21, 59:8, 69:4 combination 13:16, 31:5, 56:17 come 49:9 commencement 93:9 commencing 93:20 common 83:19 companies 23:1, 88:18, 90:3 company 1:5, 18:2, 19:10, 20:2, 20:9, 20:11, 21:7, 21:10, 21:12, 24:4, 25:11, 30:5, 36:16, 36:17, 89:17, 89:19, 90:8, 90:17,	91:6 compare 8:8 compared 68:10 competitive 35:11 compile 15:10 complete 73:3, 76:3, 76:4 completed 73:22, 76:7 complies 55:16 components 27:22, 90:1, 90:10, 90:12 composition 57:7 computer 27:15, 28:18, 29:8, 78:19, 92:9 computers 90:9 concerned 47:13 conclusion 52:15, 73:17 conductive 78:15, 79:6, 79:16 connect 13:1 connected 73:21 connections 74:14, 76:2, 76:19 connective 79:10 consider 55:12, 71:15 consistent 8:19, 68:21 constraints 65:13
--	--	---	---

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

99

construct 40:16 consultant 26:18, 90:22 consultation 91:5 consulted 25:22, 36:20, 37:17 consulting 7:18, 32:17, 33:7, 33:19, 33:21, 34:8, 88:18 contact 75:9, 79:12, 79:18, 79:20, 79:22, 80:10, 81:6, 85:22, 86:2 contacts 73:6, 73:12, 73:15, 73:19, 74:2, 74:16, 74:19, 75:16, 75:20, 76:21, 77:13, 77:17 contains 9:16, 43:6 content 65:20 context 61:6, 84:5 continued 30:10 continuous 33:2 continuously 33:4, 33:7 contract 25:22 contracted 30:13, 90:17 contracting 90:2 contribution 65:4, 82:19 control 64:19	conversation 6:4 converting 39:10 copied 44:13 copy 26:19, 45:18, 55:5, 87:6 core 26:15 corner 12:9, 12:16, 14:5 corporation 23:8 correct 5:16, 9:19, 10:13, 11:10, 11:19, 12:3, 13:6, 14:2, 14:11, 14:12, 17:22, 18:1, 18:11, 18:15, 18:19, 18:22, 19:7, 19:8, 19:11, 19:14, 20:10, 20:22, 22:1, 22:2, 22:5, 22:10, 24:1, 24:13, 25:1, 25:2, 25:10, 27:19, 29:1, 29:21, 36:10, 36:21, 37:14, 41:19, 43:9, 44:9, 45:1, 45:2, 51:10, 53:4, 54:14, 54:15, 54:21, 57:12, 57:15, 57:20, 57:21, 61:14, 61:16, 71:4, 72:7, 72:8, 73:8, 75:10, 76:11, 77:14, 77:15, 79:12,	79:13, 79:14, 81:6, 81:7 correctly 12:14, 46:19 correlate 13:1 corresponding 44:16 cost 89:11 could 7:17, 10:6, 19:20, 37:10, 51:20, 55:8, 55:20, 57:3, 69:19, 70:20, 72:5, 75:12, 78:7, 81:7, 81:8, 81:20, 82:1, 82:3, 83:18, 85:7 counsel 5:5, 6:12, 11:4, 49:1, 77:5, 87:22, 88:3, 88:6, 93:16 couple 23:15 court 6:2, 51:15, 72:3 create 28:9, 40:13, 63:3, 63:10, 64:11, 64:12, 65:4, 76:19, 78:14, 79:5, 80:15, 80:19, 81:12, 81:18 created 15:3, 24:3, 40:2, 49:3, 49:5, 62:13 creating 63:2, 63:12, 79:14 crystal 81:8	csr 1:21, 94:13, 94:14, 94:15 current 24:8, 35:7, 39:3, 39:4, 47:3, 67:6 currently 20:4, 20:13 cut 63:4 cv 10:19, 10:22, 17:16, 17:18, 18:21, 24:20, 25:7, 38:19, 38:21, 41:21 D damaged 65:15 data 11:19, 15:5 date 12:9, 48:1, 48:6, 49:5 dated 9:15, 41:16, 41:21, 42:22 dates 18:20, 21:22 dc 3:8 decide 46:13 declaration 7:8, 9:5, 9:13, 9:21, 10:2, 10:7, 10:18, 10:20, 11:1, 11:3, 13:9, 15:16, 15:20, 16:2, 16:6, 16:10, 16:14, 16:18, 16:22, 17:4, 17:8, 17:12, 42:15, 42:22, 43:3,
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Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

100

43:6, 43:10, 44:3, 44:7, 44:11, 44:14, 44:17, 44:19, 44:22, 45:4, 45:8, 46:14, 48:8, 48:13, 48:20, 53:11, 59:22, 60:5, 60:18, 67:18, 68:16, 72:6, 78:8, 91:20, 92:5 declarations 4:10, 7:4, 12:8, 12:18, 13:2, 13:20, 14:7, 14:18, 15:7, 15:12 defendant 8:9 defer 72:4 defined 60:15 defines 40:21 definition 66:22, 67:3, 80:22, 81:15, 82:10, 82:12 degrading 65:3 degree 10:10, 10:14 deliverables 26:17 depend 86:15 depending 36:8, 56:3 depends 36:2, 65:11, 65:19, 69:19, 82:6, 84:2, 85:7 depict 46:6, 59:19 deployment 34:5	deposed 5:16, 8:22 deposing 81:17 deposited 80:8, 81:5 depositing 81:17 deposition 1:15, 2:8, 57:6, 62:10, 92:17, 93:4, 93:7, 93:9, 93:10, 93:17, 93:18 describe 28:3, 45:4, 46:9, 47:13, 75:19, 77:16, 79:21 describes 44:7 describing 47:4 description 4:8, 23:19, 80:11 design 16:18, 17:13, 18:9, 26:12, 26:21, 26:22, 27:1, 27:11, 27:12, 30:6, 30:14, 30:16, 31:14, 32:7, 32:15, 33:11, 33:20, 34:9, 37:16, 37:19, 39:16, 39:19, 39:21, 41:12, 41:13, 42:5, 42:6, 42:7, 42:10, 50:22, 66:10, 66:16, 84:13, 88:15, 88:17, 88:19, 88:22, 89:13, 89:18, 90:5,	90:11, 91:9 designed 38:12, 39:2, 40:8, 84:3, 84:4 designers 91:1 designing 25:17, 25:20, 33:17, 34:12, 89:7 designs 25:12, 33:9, 36:7, 36:12, 37:17, 91:11 detail 76:2 determine 90:4 determines 47:8 develop 22:19, 26:6, 47:5 developed 24:2, 39:6 developing 33:4, 42:3 development 18:13, 22:7, 23:10, 23:20, 24:3, 26:14, 30:14, 32:15, 45:10, 89:5 device 16:7, 29:11, 30:12, 31:8, 31:9, 31:16, 36:4, 83:13 devices 35:21, 39:22, 44:8 diego 3:15 dielectric 56:2, 56:9, 56:16, 56:21, 61:10, 62:6, 64:14, 65:9,	66:1, 66:5, 67:21, 68:18, 69:8, 69:11, 70:6, 70:8, 71:16, 71:17 difference 46:16 differences 44:7, 45:4, 83:18 different 15:12, 21:2, 31:18, 45:11, 50:5, 57:6, 83:3, 85:3 differentiation 85:6, 85:13, 85:15 differently 36:8 difficult 55:13 diffused 69:19 diffuses 69:21, 82:7 diffusion 70:19, 70:20, 85:9, 85:11, 85:12 digital 26:4 dimension 87:18 dimensioned 29:6 dimensions 86:12, 86:13, 87:3, 87:4, 87:15 dimmers 16:19 dioxide 56:17, 57:4, 57:5, 57:8 direct 81:15 directed 34:2, 41:9,
---	---	--	---

42:2, 47:10, 74:12 direction 53:13, 93:14 directly 21:4, 35:5, 39:14, 40:19, 46:1, 80:14, 80:18, 81:11, 91:1 discipline 89:3 disclose 86:11, 87:2, 87:14 disconnect 13:12 discuss 7:7 discussed 9:10, 42:18, 45:20, 53:22, 54:4, 81:1, 86:21, 87:9, 94:1 discusses 45:6 discussing 47:16 discussion 44:10, 45:7, 46:14 displacing 63:1 dispute 12:1, 15:14 distributed 8:4 distribution 8:11, 8:16, 15:7, 84:1, 84:14 dive 90:9 divers 90:14 dlp 26:1, 26:5,	30:1, 90:19 docket 11:17, 12:8 document 9:9, 42:15, 42:21, 49:6 doing 66:16 dokhanchy 3:13, 5:11 done 20:16, 20:17, 31:18, 32:7, 38:3, 39:7, 39:21, 55:17, 55:18, 63:15, 68:8, 77:20 dope 69:18 doped 59:8, 69:4, 69:6, 69:10, 69:17, 70:7, 70:9, 70:11, 81:9 dopes 69:20 doping 70:14 down 35:16, 61:2, 88:6 drain 40:5, 40:14, 40:15, 51:3, 63:22, 66:1, 66:2, 66:6, 66:7, 66:12, 66:14, 66:21, 73:6, 73:12, 73:15, 74:3, 74:16, 75:17, 75:20, 77:13, 77:17 draw 55:13 drawing 61:1, 61:6	drawings 27:12, 86:15 drawn 86:8, 86:10, 86:22, 87:12 draws 87:17 drew 60:21 drivers 16:19 duarte 5:8 duarte-guevara 3:5 duly 5:3, 93:8 dunner 3:6, 5:7 during 6:13, 8:18, 24:2, 35:19, 36:1, 87:22, 90:21 E each 11:16 earlier 82:11 early 32:22, 33:5, 33:15, 90:21 earphones 17:9 earshot 88:4 edge 59:6, 59:18, 62:14, 62:19, 63:6 edges 64:17 education 88:22 EEPROM 32:18, 89:9 effect 65:2, 65:3,	66:11, 66:20 effects 65:7 eight 8:18 either 87:22 elaboration 86:16 electrical 10:10, 16:14, 73:5, 73:14, 73:19, 74:2, 74:13, 75:16, 75:20, 76:2, 77:13, 77:17, 79:11, 79:22, 80:9, 81:6, 89:3 electrically 73:21 electrode 64:12, 67:7, 82:18, 83:7, 86:2 electromechanical 15:20, 15:22 electronic 16:6, 27:22 electrons 64:20 element 52:6, 52:18, 58:14, 59:2, 59:7, 83:19 employed 25:15, 94:4 engaged 19:17, 19:22, 20:13, 20:20, 24:7, 24:15, 24:20 engagement 8:19 engagements 7:15, 7:17, 8:14, 8:15, 8:17 engineering 10:11, 89:3,
--	---	--	---

89:22 entire 63:18, 64:7, 64:13, 65:9, 89:11, 91:6 entity 21:3 entries 11:6, 14:20 entry 14:22, 15:5, 19:2, 19:15, 21:19, 22:17 environment 45:9, 56:3 ep 41:20 epi 62:10, 62:11, 62:16, 64:1, 69:15 epilayer 64:1, 70:1 epitaxial 58:6, 60:1, 60:5, 60:14, 60:19, 61:10, 62:1, 62:2, 62:5, 63:5, 67:19, 68:17, 70:5 eprom 89:9 error 78:19, 78:21, 92:3, 92:11 esquire 3:4, 3:5, 3:12, 3:13 et 53:21, 54:3 etching 85:19 evaluating 39:9 evaluation 26:22, 39:2, 39:3	evaluations 29:14 even 21:4, 39:21, 39:22, 40:2 evenly 8:4 eventually 77:2, 79:18 ever 37:21, 38:9, 38:12, 38:16, 39:15 every 91:6 everything 10:2, 43:10, 89:13 exact 13:3 exactly 30:22, 36:14, 49:16 examination 4:4, 4:5, 5:13, 88:10 example 48:14, 57:3, 82:2 excuse 52:11, 62:2, 64:11, 70:3 exemplary 50:21 exhibit 4:9, 4:10, 4:11, 4:12, 4:16, 4:17, 4:18, 4:19, 4:20, 4:21, 4:22, 9:3, 9:4, 9:10, 9:16, 11:12, 11:13, 12:5, 12:6, 12:21, 12:22, 13:5, 13:6, 13:7, 13:15, 13:17, 13:20,	14:6, 14:14, 14:15, 14:17, 14:21, 17:16, 24:20, 25:7, 42:14, 42:18, 43:2, 45:19, 45:20, 50:7, 50:20, 51:21, 53:11, 53:19, 53:22, 54:1, 54:4, 54:8, 54:13, 54:17, 54:20, 55:1, 55:2, 55:4, 57:10, 58:12, 59:14, 59:20, 60:11, 78:17, 86:6, 86:18, 86:19, 86:21, 87:7, 87:9, 91:19 exhibits 4:14, 53:19, 54:5, 54:7 existing 47:18 exists 63:22 exp 94:14, 94:15 expect 5:20, 13:3 experience 17:17, 17:22, 38:20, 84:18, 88:14, 88:20, 88:22, 91:14 expert 7:16, 7:18, 8:22, 15:16, 15:19, 16:2, 16:5, 16:9, 16:13, 16:18, 16:22, 17:4, 17:8, 17:12, 18:3, 72:20, 75:6 explain 13:11, 25:20	exploitation 22:8, 23:21 extend 69:11, 69:19, 70:1, 70:5, 70:7 extending 62:1, 62:5, 67:20, 68:17, 69:7 extent 65:18 F fab 89:13 fabbed 36:19 fabricate 34:16, 37:9 fabricates 25:13 fabrication 29:12, 30:6, 32:8, 34:13, 37:12 fabs 34:19 fact 38:22, 60:5, 61:4, 65:16 failure 89:22 fair 36:9, 59:3 fairly 8:3, 8:19 fall 71:18, 81:15, 82:13 familiar 5:18, 9:9, 42:20, 91:10 far 40:4, 65:6, 65:15, 81:16, 82:7, 85:1 farabow 3:6, 5:6
---	--	---	--

features 50:22 feram 90:18 ferrous 30:12, 30:14, 31:4, 31:18 fets 45:11 few 11:6, 17:17, 37:17, 50:2, 88:12, 91:16 field 16:18, 16:22, 17:12, 25:16, 40:1, 40:20 field-effect 42:7 figure 4:12, 50:8, 55:5, 55:10, 57:15, 58:16, 59:19, 60:17, 72:10, 72:15, 74:22, 75:9, 75:12, 75:15, 75:18, 75:21, 76:5, 76:6, 76:9, 77:1, 77:3, 77:12, 77:18 figures 86:8, 86:22, 87:11 file 27:3, 27:13 filed 7:3, 11:1, 12:15, 12:18, 13:9, 13:21, 14:6, 15:12 files 27:8, 28:16 filing 23:7, 48:6 fin 50:21, 51:1,	51:7 financially 94:6 fine 7:12, 14:3, 51:15, 72:3 finfet 44:8, 45:14, 45:17, 46:2, 46:6, 46:12, 46:14, 46:17, 47:3, 47:5, 47:15, 51:9 finfets 46:9, 47:13 finish 51:17, 77:7, 90:20 finnegan 3:6, 5:6, 5:8 firm 5:6 first 5:3, 6:1, 8:15, 8:18, 9:21, 10:2, 10:7, 10:17, 10:20, 11:1, 11:2, 11:4, 11:9, 12:17, 44:13, 44:16, 44:19, 44:22, 45:3, 45:8, 46:14, 48:12, 48:20, 50:21, 52:1, 53:19, 68:1, 88:13 five 89:19 flash 32:18, 35:10, 67:13, 89:9 flat 50:9, 50:13 flows 27:10 focus 24:1	focused 89:4 following 10:20, 37:11, 37:19 follows 5:3 footer 11:2 foregoing 93:4 form 61:19, 63:20, 65:10, 75:20, 77:17, 80:9, 81:5, 82:1, 83:2, 84:19 format 27:14 formation 69:14, 77:20 formats 27:3, 28:20, 28:21 formed 22:22, 23:2, 52:3, 52:7, 52:17, 52:18, 52:20, 59:9, 63:18, 66:2, 66:6, 70:10, 70:11, 89:18 former 89:18 forming 81:17 forth 34:11, 93:8 fortunate 89:15 found 92:3 four 15:1 fourth 72:9 fringing 65:7	function 72:16, 82:18, 86:1 functioning 76:13, 76:15 further 78:14, 79:5, 92:15, 92:16, 93:15, 93:18, 93:22, 94:2 G garrett 3:6, 5:6 gds 27:8, 27:13, 28:16, 28:17, 28:20 gears 80:6 general 15:22, 31:15, 47:6, 47:20, 50:15, 51:8, 80:11 generally 27:11, 46:3, 81:3, 81:7 generate 29:12 generated 92:10 generation 28:11 geo 34:5 geometries 46:17, 46:20 getting 54:9, 63:4, 63:9, 63:14 give 6:15, 6:19, 26:17, 31:12, 36:13, 50:3, 54:6, 61:1 given 26:19, 83:19,
--	---	---	---

93:11 giving 47:19, 48:14, 86:13 go 5:19, 9:2, 17:16, 23:18, 40:11, 43:14, 53:10, 56:12, 61:5, 61:7, 62:15, 62:17, 65:8, 65:14, 70:19, 75:14, 77:22, 87:19, 89:5, 89:8 goes 60:6, 60:7, 60:15, 61:2, 76:1, 84:21, 89:2 going 11:11, 34:12, 40:15, 51:11, 51:13, 51:14, 51:16, 53:13, 53:18, 54:22, 56:1, 56:13, 63:4, 63:6, 63:10, 63:21, 64:4, 64:11, 64:12, 65:1, 65:2, 65:3, 65:5, 65:14, 66:19, 68:2, 70:15, 71:22, 72:1, 77:5, 84:10, 85:2, 85:12, 87:6 good 71:20, 72:1, 72:2, 77:4, 80:11 gps-related 17:4 graded 65:5 graph 4:9, 4:10,	4:11, 11:15, 14:16, 15:2 graphed 14:19 grew 40:1 grow 41:2 grown 62:12 growth 41:4, 63:5, 69:15 guardian 22:18, 23:2, 23:4, 24:4, 24:18, 25:3 guess 14:19, 49:5, 55:10, 55:11, 78:9 guidelines 71:19 H half 32:4, 77:6 hand 9:2, 12:4, 14:13, 42:12, 45:19, 54:22, 86:18, 87:6, 94:9 happens 64:5 hard 26:19 hardware 27:8 held 2:8 help 19:20, 26:21 henderson 3:6, 5:6 here 7:1, 7:6, 7:8, 10:4, 11:22,	13:15, 15:9, 18:21, 23:13, 29:4, 43:12, 47:16, 49:2, 49:15, 49:20, 52:16, 53:5, 57:15, 57:20, 60:15, 62:4, 63:21, 69:17, 75:22, 87:17 hereby 93:5 hereinbefore 93:7 herunto 94:8 high 70:20 highly 67:1, 67:3, 67:5 hold 10:9, 21:5 holding 19:9, 20:1, 20:8 holds 20:3, 20:12 holes 64:20 homogenous 64:19, 65:2, 81:21 hour 51:11, 77:5 however 70:6 hundred 35:12 hvac 16:3 I idea 65:6 ideas 23:10 identified 60:20, 86:9	identify 41:10, 42:8 identifying 22:20 iii 1:15, 2:8, 4:3, 5:2, 9:6, 42:16, 93:6, 93:19 illness 6:19 illustrate 50:8, 75:16, 76:9, 77:12 illustrations 46:5 image 59:21 impact 6:18 implanted 69:18, 70:22 implanting 70:15 implants 70:17 implementation 17:13 improve 90:5 improvement 27:1 inc 18:5, 18:7, 18:10, 19:3 include 42:4, 46:13 included 27:21 includes 76:8, 88:18 including 22:21, 88:16, 89:1 inculcated 31:19 inculcation 26:7 indicate 71:13
---	--	---	---

indicated 60:3 indication 61:1 industries 35:10 industry 16:11 information 11:22, 31:12 initial 48:12 initially 8:17 installation 18:9 instance 23:10 instantiate 36:12 instantiated 29:10, 36:8, 37:1, 37:2, 79:13 instantiation 36:3, 65:11, 65:19, 70:22 instead 15:1 instructed 6:14 instruments 25:8, 89:7, 89:11 insulating 57:1, 67:1, 67:4 insulator 67:2 insurance 18:17 integration 90:10, 90:12, 91:11 intellectual 22:8, 22:19, 23:21 inter 9:7	interconnections 76:10, 76:21 interested 33:10, 94:6 interesting 7:21, 11:20 interface 40:15, 81:19, 82:4, 86:1, 86:3 intimately 91:10 introduce 11:11, 53:18 invalidity 47:22, 48:4 invented 76:17 inventions 91:8 inventors 22:22, 23:15 investigation 18:17 involve 41:7 involved 11:16, 13:19, 20:6, 21:4, 21:11, 22:6, 25:3, 31:19, 32:14, 33:8, 37:8, 37:11, 37:19, 38:6, 38:16, 39:12, 39:15, 89:6, 89:15 involving 21:16 ip 19:9, 19:12, 19:17, 19:22, 20:1, 20:6, 20:8, 20:20, 24:7, 24:15, 24:21, 25:4 ipr 1:11, 7:2, 11:4, 46:11,	46:18, 47:16, 49:18 iprs 49:13, 49:22, 50:5 isolation 40:21, 41:1 issue 46:11 itself 26:15, 31:20, 47:7, 50:19, 64:3, 64:17, 66:3, 66:7, 66:19, 70:1, 70:15 J january 43:1 job 1:22, 78:6 joined 5:7, 89:17 jointly 49:1, 90:18 jokes 78:5 joseph 1:15, 2:8, 4:3, 5:2, 9:6, 42:15, 93:6, 93:19 judge 15:9 K keep 51:13, 51:14, 51:16, 58:3, 71:22, 72:1 keeping 90:14 key 35:10 kind 13:15, 22:14, 25:20, 27:3, 78:8, 91:14	klinger 1:21, 2:10, 93:3, 94:13 know 5:20, 27:5, 27:9, 36:11, 36:22, 40:10, 55:5, 78:4 knowledge 10:3, 43:11, 43:13 L l-i-a-w 87:7 laboratory 89:22 lan 78:12, 79:4, 79:14, 86:19, 86:22, 87:2 language 48:18, 49:5, 49:9, 49:14, 49:19, 49:21, 50:2, 68:14 large 26:3, 26:4, 60:19 las 19:3 last 14:22, 19:15, 24:5, 32:4, 37:7, 59:7, 59:16, 69:1, 69:12, 78:11, 91:18 lawsuit 23:7 layer 56:2, 56:9, 56:22, 60:1, 60:5, 60:14, 60:19, 61:10, 62:1, 62:2, 62:5, 62:6, 67:19, 67:21,
--	---	---	--

68:17, 68:18, 69:8, 69:12, 70:5, 70:6, 70:8, 71:16, 71:17, 78:13, 78:15, 79:4, 79:7, 79:10, 79:15, 79:17, 80:9, 81:5 layers 58:6 layout 27:18, 27:21, 28:3, 28:13, 28:15, 28:16, 29:8 layouts 27:18, 28:22 lead 83:7 leak 67:6 least 35:15 leave 51:12 led 16:19 left 12:9, 50:8, 76:22 legal 52:14, 73:16 length 34:10, 35:4 let's 10:17, 44:18, 53:10, 56:12, 58:3, 67:14, 77:3, 77:22, 87:19 level 34:4, 91:2 levels 65:20, 91:12 levin 5:9 liability 18:16	liaw 87:7, 87:11, 87:14 license 20:6, 20:13 licensed 21:1, 21:5 licensing 19:9, 19:17, 19:22, 20:2, 20:5, 20:8, 20:11, 20:13, 20:20, 21:2, 21:4, 21:6, 21:16, 22:7, 23:20, 24:7, 24:15, 24:21, 25:4 light 26:5 limitation 52:2, 58:5, 59:17, 61:12, 61:22, 62:3, 67:17, 68:15, 69:2, 69:6, 69:12, 74:6, 74:8 limitations 73:18 limited 1:8, 5:10, 9:4, 42:14 line 55:22, 56:1, 56:5, 56:13, 60:21, 72:9, 77:7, 92:2 link 92:11 list 12:7, 12:22, 13:15, 13:20, 14:17, 15:10, 38:21 listed 14:21, 18:21, 23:5, 41:21	literally 64:16 litigated 23:11 litigation 7:20, 19:17, 19:22, 20:4, 20:6, 21:16, 24:7, 24:16, 24:21, 25:4 little 71:9, 80:6 locating 19:13 location 17:5, 85:11 long 3:4, 4:4, 5:4, 5:14, 15:4, 72:2, 77:7, 88:9, 92:16 look 11:19, 12:12, 15:6, 23:3, 24:18, 27:4, 28:5, 28:12, 29:10, 34:12, 40:12, 44:18, 55:19, 58:3, 59:7, 64:16, 64:18, 68:2, 68:4, 72:18, 85:14 looked 29:15, 29:16, 29:19, 92:10 looking 12:20, 17:18, 24:11, 27:7, 27:8, 27:9, 27:11, 27:14, 27:17, 27:18, 28:18, 28:22, 36:2, 36:15, 39:3, 52:1, 59:21, 60:10, 60:17, 68:9, 75:22, 85:8	looks 12:16, 25:8, 47:8, 48:15 lot 40:17, 85:9 love 78:6 lower 8:18 lp 21:19 lu 3:12, 4:5, 5:9, 15:2, 52:14, 61:19, 63:20, 65:10, 67:22, 68:19, 73:16, 74:4, 74:11, 74:18, 77:4, 77:10, 83:2, 84:19, 88:11, 92:14 M made 56:16, 56:22, 60:4, 79:19 magnetic 30:11, 31:2, 31:3, 31:10, 31:16 main 90:8 maintained 35:11 maintaining 35:9 major 86:3 majority 49:2 make 5:20, 6:8, 75:9, 76:20, 78:5, 79:20, 79:22, 83:4, 83:16, 84:13 makes 31:2, 31:10,
--	--	---	---

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

107

31:15 making 34:22, 68:21, 79:11 manage 22:19 management 22:7, 22:14, 23:20 manager 22:3, 89:10, 89:18 manufacture 88:19 manufacturing 1:5, 88:15, 88:17, 89:1 many 7:15, 7:17, 7:18, 8:21, 35:3, 88:14 march 1:17, 2:3, 12:10, 93:20, 94:9 marked 4:14, 9:3, 11:12, 11:13, 12:5, 12:6, 14:14, 14:15, 42:12, 42:13, 55:1, 55:2 marker 55:9 marketing 89:14 markings 4:12 marlin 1:8, 5:10, 9:4, 42:13, 93:16 marriage 94:4 mask 28:22, 62:14, 79:19 masters 10:15	material 31:5, 31:19, 31:20, 56:16, 65:20, 69:20, 69:21 materials 30:18, 30:20, 31:1, 31:4, 57:1 matter 61:5, 64:9, 94:7 matters 7:7 maybe 83:5 mcalexander 1:15, 2:8, 2:9, 4:3, 5:2, 5:15, 9:6, 18:4, 18:5, 18:6, 18:10, 18:14, 18:18, 18:21, 42:16, 78:2, 87:21, 88:13, 93:6, 93:19 mdf 19:9, 21:4 mdfholdings 19:3, 19:6, 19:12, 19:16, 19:21, 20:1, 20:3, 20:5, 20:8, 20:11, 21:15 mean 23:16, 25:14, 27:5, 30:22, 35:2, 35:9, 36:17, 37:10, 48:22, 67:5, 67:6, 74:8, 83:9 meaning 61:17, 71:2, 71:6, 71:7 means 19:21 mechanisms 90:14	medications 6:20 memorialized 28:9 memories 89:8 memory 30:12, 32:18, 35:10, 39:22, 89:9 mention 45:16 mentioned 23:11, 29:15 merit 2:11 merits 68:5 metal 38:10, 38:13, 38:16, 39:4, 39:5, 39:7, 39:12, 39:14, 80:8, 80:14, 80:15, 80:18, 80:19, 81:4, 81:11, 81:12, 81:14, 81:18, 82:1, 82:14 metals 81:22, 82:6 method 45:12 methods 45:11, 57:6 microcontrollers 89:8 microprocessor 32:16 microscopy 29:18, 89:21 mid 37:15, 37:20, 38:8 midway 53:15 might 6:18, 85:15	migrate 70:21 mintz 5:9, 5:11 minus 15:5 mismatch 68:11 missed 42:1 misspoke 83:5 mix 48:8 mixing 29:2 modification 78:12, 79:4 modify 90:4 monitoring 15:17 more 7:22, 8:5, 8:13, 8:15, 9:1, 13:9, 20:7, 71:9, 71:10, 80:20 mos 31:7, 31:8, 31:9, 32:14, 36:5, 41:13, 41:15, 42:2, 42:6, 42:7, 45:10, 46:2, 53:8, 65:12, 72:11, 73:13, 73:20, 74:13, 74:20, 74:21, 75:5, 76:10, 77:15, 89:5, 90:11, 91:8, 91:14 mosfet 25:12, 30:6, 32:8, 33:11, 33:17, 34:9, 34:12, 37:9,
--	--	---	--

PLANET DEPOS
888.433.3767 | WWW.PLANETDEPOS.COM

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

108

38:10, 38:13, 39:16, 41:11, 42:5, 42:10 mosfets 25:13, 32:9, 38:17, 41:8, 48:15, 88:16, 89:1 most 14:21, 15:5, 44:12, 84:3 motor 16:2 mountain 3:14 moving 63:16 mrar 30:16, 30:19, 31:15 multiple 16:8, 85:10 myself 23:14, 38:4	newer 45:14, 46:4 next 18:20, 19:2, 21:19, 22:17, 24:19, 58:7, 59:10, 60:2, 60:8, 60:16, 61:11, 61:18, 62:7, 63:6, 63:12, 70:12, 70:18, 70:22, 71:2, 71:17, 71:19, 72:18 nice 78:3 nitride 56:17, 57:8 node 91:12 nodes 37:1 none 20:4 nonuniform 82:21, 83:1, 83:6, 83:7, 83:10, 83:21, 83:22, 84:1 nonuniformity 83:17, 84:12, 84:16 north 10:11 note 14:19 nothing 61:3, 92:14, 92:16 number 7:9, 9:5, 9:8, 11:15, 13:3, 13:13, 13:18, 14:18, 15:21, 23:5, 40:12, 41:17, 41:19, 50:4, 53:20, 54:2, 54:8,	86:20, 87:7, 90:3 numbers 56:5 nw 3:7 O object 6:13, 19:13, 61:19, 63:20, 65:10, 83:2, 84:19 objection 52:14, 67:22, 68:19, 73:16, 74:11, 74:18 obtained 12:8 obviously 64:2, 65:12, 76:18, 85:1 occurred 93:19 office 1:1 offices 2:9 often 56:15 old 39:5 older 8:5, 45:12, 46:3 once 69:18, 70:19, 79:18 one 6:7, 12:1, 13:2, 13:9, 14:20, 14:21, 23:1, 23:13, 26:11, 28:20, 30:12, 31:17, 35:10, 41:1, 42:1, 45:12, 47:7, 50:13,	51:8, 54:1, 58:13, 59:1, 59:15, 77:9, 81:14, 83:20 one-to-one 44:16 ones 16:8, 29:11, 36:2, 89:10 only 14:20, 24:8, 28:9, 33:10, 41:13, 46:21, 47:10, 91:1 open 58:3 operate 90:13 operated 73:4, 89:20 operation 89:12 operative 74:21 opining 15:16, 15:20, 16:6, 16:10, 17:4, 17:8 opinion 61:15, 61:18 opinions 7:19, 9:17, 43:7 opposed 38:17 optically 29:17 order 40:3, 74:9, 76:19, 76:20, 90:5 orientation 34:5 original 23:6, 39:6 other 12:1, 13:7, 13:18, 23:15,
N			
name 5:4, 18:2 names 36:13 nanometer 35:13, 35:18, 35:20, 35:21, 36:1, 65:13, 65:16 nanometers 35:16 navigator 11:18, 12:9 necessarily 40:10 need 76:13, 76:21, 77:8 nevada 19:3 new 3:7			

PLANET DEPOS
888.433.3767 | WWW.PLANETDEPOS.COM

27:22, 28:4, 33:9, 36:7, 41:2, 68:3, 84:7 otherwise 94:6 out 12:2, 14:18, 44:13, 64:22, 85:1, 85:2, 91:3 outcome 94:7 outlier 85:3 outline 55:12 outlined 60:1 output 27:13, 27:14, 28:17 over 5:19, 6:2, 8:1, 8:16, 56:1 overall 8:7 overlap 66:11 overlapped 66:12 overlaps 66:1, 66:5 overview 48:17, 48:19, 51:8 own 23:17, 25:12, 25:13, 34:17, 34:19, 41:7, 41:10, 42:9 owner 1:9, 3:11, 5:10, 5:12, 7:4 owner's 9:7, 9:14, 42:16 ownership 24:3 owns 19:12	oxide 40:1, 40:20, 40:21, 41:1, 41:4, 41:6, 56:2, 56:9, 58:17, 58:19, 59:6, 59:19, 61:2, 61:3, 63:15, 64:4, 64:6, 64:7, 64:10, 64:16, 64:22, 66:14, 66:21, 66:22, 67:2 oxides 41:3 oxynitride 56:3, 56:10 P page 4:2, 4:8, 5:21, 10:7, 10:17, 10:20, 12:17, 17:18, 17:19, 24:19, 25:7, 41:21, 43:15, 43:18, 43:21, 44:19, 53:12, 57:9, 57:11, 57:12, 58:12, 59:15, 59:19, 59:22, 60:17, 78:9, 78:17, 91:19, 91:21, 91:22 papers 40:12, 40:17 paragraph 10:6, 43:14, 43:18, 43:19, 44:2, 44:18, 44:21, 50:7, 50:20, 53:12, 53:14, 53:16, 54:12, 61:9, 62:4, 67:18, 68:15, 72:5,	72:7, 72:9, 78:7, 78:10, 78:20 paragraphs 44:6, 45:3, 48:19 parameters 29:7 part 18:9, 18:13, 18:17, 24:3, 32:16, 38:2, 39:2, 52:7, 52:12, 52:21, 53:4, 53:6, 53:8, 58:17, 62:6, 66:20, 67:20, 68:18, 69:7, 69:10, 69:11, 70:4, 70:5, 70:6, 70:7, 74:6, 74:7, 74:14, 90:16 partes 9:7 participate 21:6 participating 23:16 particular 7:5, 13:13, 21:9, 25:15, 28:4, 29:17, 31:20, 36:2, 36:4, 37:16, 46:11, 47:9, 48:9, 49:18, 60:13, 62:22, 65:19, 66:11, 66:20, 68:2, 68:5, 76:16, 80:2, 82:6, 83:19, 84:8, 91:11 parties 94:3, 94:5 partners 21:19, 22:4,	22:6, 22:12, 22:15, 22:17, 22:19, 23:2, 23:19, 24:6, 24:14 party 7:20, 93:15 pass 88:9 past 8:14, 20:16, 20:17, 24:17, 25:1, 25:5, 25:6 patent 1:1, 1:3, 1:9, 1:12, 3:11, 5:10, 5:12, 7:4, 7:9, 7:11, 7:16, 7:20, 9:6, 9:8, 9:14, 9:18, 18:12, 23:11, 23:13, 41:17, 41:19, 42:16, 43:8, 45:16, 45:18, 45:22, 46:6, 47:7, 47:22, 48:2, 48:4, 48:5, 48:11, 51:21, 53:20, 54:2, 58:4, 60:12, 62:18, 63:11, 67:15, 68:3, 68:5, 69:5, 73:11, 74:2, 74:10, 75:13, 75:15, 77:3, 77:19, 79:16, 79:21, 80:4, 86:20, 87:7, 91:6 patentable 23:10 patented 74:12 patents 20:3, 20:12, 20:14, 21:1,
---	---	--	---

21:5, 21:8, 21:9, 21:17, 22:21, 22:22, 23:5, 23:17, 24:6, 34:1, 41:7, 41:11, 41:14, 41:20, 42:4, 42:9, 91:3 pdf 92:12 perfectly 62:19 perform 18:8, 18:16 performance 27:2, 29:16, 90:6 performed 37:21, 38:1, 38:9 performing 38:13, 80:13, 80:17, 81:10 perhaps 15:11 period 8:1, 24:2, 36:1 periphery 85:2 personally 37:7, 37:21, 38:1, 38:9, 38:15, 39:11, 39:17, 39:21 perspective 16:10 petition 7:6 petition's 79:3 petitioner 1:6, 3:3, 48:10, 75:6 petitioner's 72:20 petitioners 5:5 petitions 78:12	ph 3:5, 10:15 phases 89:15 phrase 61:18 physical 28:3, 29:7, 69:15, 69:16 physics 89:5 place 21:2 plain 61:17, 71:2, 71:6, 71:7 plaintiff 8:8 planar 43:16, 44:3, 44:8, 44:22, 45:5, 45:12, 46:17, 46:22, 47:2, 47:11, 47:19, 50:8, 50:13 planarity 84:22 plays 86:3 please 6:1, 6:7, 6:15, 25:21, 55:8, 55:12, 55:19, 55:20, 57:10, 78:9, 80:16, 86:5 point 38:22, 65:8, 75:2, 77:4, 87:21 pointing 14:10 points 79:20 polished 39:6 poly 38:17, 39:10,	75:2, 81:8 portfolio 18:12, 91:6 portion 60:19, 61:22, 62:5, 67:19, 68:17, 69:6 position 60:1, 61:21, 62:3, 68:14, 69:5, 70:1, 70:4, 72:22 positioned 58:6, 60:2, 72:19 possible 13:8 potential 85:20 power 84:1 practice 68:4, 74:9 practices 68:4 preamble 52:2 preclude 67:19 precludes 61:22, 62:4, 68:16, 68:22, 69:6 preferably 56:1, 56:11 preliminary 9:7, 9:13, 9:14 prepared 15:4 present 19:4, 24:22 presentation 41:5 president 89:20 preston 3:4, 5:4 previous 49:13, 49:22	previously 4:14 primarily 32:1 primary 24:1, 45:11 principal 89:10 principally 30:2 print 78:18 printers 26:9 printout 92:10 prior 46:8, 46:10, 47:12 priority 48:1 privilege 6:15 probably 7:21, 8:8, 8:18, 11:3, 11:5, 11:6, 12:3, 33:13, 37:15, 55:11, 57:6 problem 78:14, 79:6, 79:9, 79:11 proceeding 46:9, 47:16 process 11:5, 27:9, 29:6, 34:13, 36:9, 37:1, 37:12, 37:16, 37:20, 38:3, 38:6, 38:12, 41:4, 69:20, 70:20, 80:8, 80:14, 80:18, 81:4, 81:11, 84:22, 85:18 processes 36:11, 85:20
--	---	--	--

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

111

processing 37:8, 37:10, 37:17, 84:17, 85:5, 91:10 processors 26:8 produces 68:10 product 18:16, 26:19, 26:20, 29:15, 47:9, 68:3, 68:6, 68:7, 74:21, 84:15, 90:18 products 29:17, 35:17, 36:19, 39:3, 39:4, 39:9, 90:4, 90:5, 90:8, 90:19, 91:2, 91:9 profile 17:22 program 27:16, 28:8 projection 26:5 property 22:9, 22:20, 23:22 proposed 78:12, 79:3 proprietary 27:6, 27:16, 31:13, 36:14 prosecution 22:7, 22:15, 23:16 provide 7:19, 18:12, 41:11, 42:9, 44:10, 45:7, 64:3, 70:16, 90:13 provided 7:3, 11:4, 11:5, 43:7,	48:9, 91:5 provides 69:14 providing 18:3, 64:1 pt 18:6 ptab 4:9, 4:10, 11:15, 11:20, 11:21, 12:2, 12:8, 12:19, 13:6, 13:7, 13:19, 14:7, 15:12, 15:15, 15:19, 15:21, 16:1, 16:5, 16:9, 16:13, 16:17, 16:21, 17:3, 17:7, 17:11 published 40:6, 40:11 pulled 11:17, 12:1, 14:18 purple 57:19, 57:22, 58:12, 58:22, 59:13, 60:3, 60:21 purposes 6:14 put 54:16, 74:20, 76:17, 84:9 Q qm 21:19, 22:3, 22:6, 22:12, 22:15, 22:16, 22:18, 23:1, 23:19, 24:5, 24:14 qualification 44:12 quality 86:1	quarter 11:3, 11:9 question 6:9, 6:16, 7:21, 22:16, 23:3, 46:19, 67:16, 68:1, 69:1, 84:11 questioning 6:13, 77:8, 83:9, 84:8 questions 6:7, 17:17, 88:12 quick 91:19 quickly 51:19 quite 32:17, 37:17, 91:16 quote 61:11, 61:12, 72:10, 72:11 R raised 58:6 ram 30:11, 30:12 rams 39:2 ran 89:12 random 89:7 rates 35:11 rather 61:11, 78:19 ratio 40:3 raymond 3:12, 5:9 reach 65:7 read 47:9, 52:16	reading 93:22 reads 57:22, 72:10 ready 51:14 real 91:18 really 31:11, 31:12, 35:6, 36:2 realtime 2:11 reask 14:4 reason 15:14, 33:22, 69:13 recall 16:4, 37:4, 46:1, 46:7, 46:10, 49:4, 86:13, 87:1, 87:4 receive 21:15 recent 8:5, 14:21, 15:5 recently 8:14 recess 62:12, 62:13, 62:15, 62:16, 63:4, 63:5, 69:14, 78:1, 87:20 recipes 38:2 recited 58:14, 59:16 recites 52:6, 58:6 recognize 12:13 record 14:4, 54:10, 77:22, 87:19,
---	--	--	---

93:11 records 12:2 red 55:8, 57:20, 60:1, 60:20 reduced 13:16, 93:13 reevacuate 85:17 refer 7:10, 9:20, 43:2, 54:12, 54:16, 54:19, 58:11, 67:17, 79:9 reference 53:16, 54:13, 60:14, 72:7, 86:19, 87:11, 92:3 referred 68:15 referring 25:21, 37:13, 41:17, 43:4, 54:13, 58:13, 59:1, 59:4, 59:15, 76:5, 79:11, 80:22, 92:6 refers 24:8, 24:22, 53:16, 92:7 reflected 12:14 regard 7:5, 26:13 regarding 7:9, 9:6, 9:17, 16:2, 16:14, 42:16, 43:7 region 59:9, 66:1, 66:3, 66:7, 66:12, 69:4, 69:10, 80:10, 81:6	regions 40:22, 51:3, 66:6, 69:7, 69:18, 70:7, 70:10 registered 2:11 related 19:12, 19:17, 19:22, 20:20, 24:7, 24:15, 24:21, 25:4, 30:5, 31:4, 41:14, 47:15, 94:2 relates 32:7 relating 33:11 relationship 22:17 relative 57:22, 58:8, 58:11, 58:13, 58:15, 58:22, 59:2, 59:10, 59:14, 59:16, 60:16, 61:11, 70:2, 70:10, 70:13 release 34:2, 41:15 relevance 48:3 relevant 46:17, 46:20, 47:21, 48:6, 60:12 reliability 89:14, 90:6 remember 49:18 renner 2:9 reported 1:21 reporter 2:11, 2:12,	6:3, 51:15, 72:3, 93:1, 93:3 reports 7:3 represent 11:14, 12:7, 14:16, 15:10, 22:21, 55:4 representation 60:22, 68:20 representative 44:12 representatives 35:17 represented 60:11, 93:16 represents 15:11 require 6:6, 73:12, 73:14, 74:2 required 61:12, 68:10, 74:9, 76:8 requires 62:7, 73:13 resistance 34:11, 80:9, 81:6, 82:17, 82:20, 82:22, 83:8, 83:19, 83:22, 85:22, 86:4 respective 70:10 respectively 58:7, 59:9, 70:12 response 9:7, 9:15, 42:17 rest 23:9, 23:19 restrictive 71:9, 71:10 result 82:22, 83:22 resulted 23:8	results 12:17, 15:21 retaining 78:13, 79:4, 79:15 reticles 28:11, 29:12 revenues 21:15 reverse 89:22 review 9:8, 15:12 reviewing 91:8 reza 3:13, 5:11 rfid 16:22 richardson 1:16, 2:10, 89:19 right 9:18, 10:12, 12:12, 12:16, 12:18, 13:4, 14:3, 14:5, 14:7, 15:6, 18:10, 18:14, 18:18, 19:10, 19:13, 22:4, 22:9, 24:12, 24:16, 25:9, 28:1, 28:16, 28:19, 33:6, 33:18, 35:21, 36:20, 37:3, 42:5, 43:8, 44:1, 44:8, 45:5, 48:21, 51:9, 51:16, 53:3, 54:8, 55:8, 56:10, 56:14, 57:4, 57:9, 59:4, 59:6, 59:17, 60:9, 60:20, 61:2, 61:13,
---	---	--	--

63:19, 64:14, 67:1, 67:4, 67:8, 67:12, 67:14, 69:12, 70:8, 70:11, 71:3, 72:17, 73:4, 73:7, 76:6, 76:7, 76:14, 76:22, 77:1, 78:5, 78:7, 81:10, 82:9, 85:19 rightmost 59:18 rnr-crr 1:21, 94:13 road 2:10, 3:14 role 86:3 roughly 7:15, 8:21 rules 5:18 run 65:13 running 65:16	satisfy 74:17 say 8:3, 8:7, 8:13, 8:14, 8:15, 8:17, 11:2, 12:3, 12:13, 12:21, 20:8, 27:1, 30:2, 33:3, 33:12, 33:13, 33:22, 35:18, 37:15, 43:18, 49:2, 58:22, 61:9, 62:18, 66:4, 69:13, 74:7, 76:4, 78:9, 80:16, 85:20 saying 13:14, 13:17, 60:13, 90:20 says 10:9, 19:16, 20:19, 24:20, 50:21, 52:2, 56:1, 56:7, 56:15, 59:8, 62:21, 70:11, 78:11, 79:3 scale 86:8, 86:9, 86:10, 86:16, 86:22, 87:12 scanning 29:18, 89:21 schematic 27:12, 28:8, 28:12, 29:5 schematics 28:12 science 10:10 scope 80:2, 82:14 screen 27:15 screens 26:4	se 40:11, 46:2, 46:20 second 42:22, 43:3, 43:6, 43:10, 44:2, 44:7, 44:11, 48:13, 53:10, 54:1, 58:5, 58:14, 59:2, 59:22, 60:18, 67:18, 68:16, 72:6, 78:8, 78:11, 91:20, 92:2 section 43:15, 44:2, 44:22, 48:12, 92:5, 92:8, 92:12, 92:13 see 12:17, 13:13, 19:4, 19:15, 20:7, 20:15, 21:20, 23:5, 29:9, 39:8, 42:17, 43:17, 44:4, 48:16, 49:17, 50:6, 50:10, 50:20, 51:4, 52:4, 52:8, 53:15, 56:4, 56:19, 58:1, 58:9, 59:11, 62:18, 63:17, 72:13, 72:14, 73:18, 76:22, 78:16, 78:18, 79:2, 84:7, 86:16, 87:17, 88:7, 92:2 seems 52:19 seen 15:8 semiconductor 1:5, 1:8, 5:10,	9:4, 34:4, 37:8, 42:14, 51:1, 52:3, 58:7, 59:9, 70:12, 84:16, 90:3, 92:8, 93:16 sems 29:1 sense 83:4, 83:16 sensing 90:14 sensor 34:3, 41:15 sensors 42:3 sentence 50:21, 55:22, 56:12, 72:10, 72:18, 78:11, 78:16, 78:22, 79:3 service 11:17 services 18:3, 18:9, 18:13, 18:17 set 38:2, 93:7, 94:8 setting 38:6, 45:9 settlement 23:8 several 7:3, 34:1, 89:12, 91:3 shift 80:6 shortening 66:17 shorthand 93:1 should 14:22, 55:10, 78:9, 92:12 shouldn't 78:5
S			
s 3:1, 37:15, 38:8, 39:7 safe 90:15 said 35:22, 43:19, 47:17, 70:14, 93:12 sales 21:7 same 5:21, 13:3, 23:18, 34:14, 56:22, 68:19, 69:1, 74:11, 74:18 san 3:15			

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

114

show 38:19 showing 11:15, 68:21, 87:4 shown 58:16 shows 11:2 side 58:1, 58:11, 58:15, 58:18, 58:22, 59:14, 60:2, 60:8, 60:16, 63:3, 70:2, 76:22 sides 58:8, 58:13, 59:2, 59:10, 59:16, 61:11, 70:3, 70:11, 70:13 sidewall 52:7, 52:11, 52:19, 52:20, 56:15, 56:22, 58:19, 63:18, 86:12, 87:3, 87:5, 87:15, 87:18 signature-plkal 94:11 signed 7:19 signing 93:22 silicidation 37:22, 38:7, 38:10, 38:13, 80:7, 80:14, 80:18, 81:1, 81:4, 81:11, 81:16 silicide 80:15, 80:19, 81:12, 82:8, 82:12 silicon 28:5, 39:6,	39:20, 40:18, 50:9, 50:14, 56:2, 56:9, 56:16, 56:17, 57:3, 57:5, 57:8, 80:8, 81:5, 81:8 silicon-uranium 40:18 similar 57:1 since 8:2, 8:4, 8:16, 8:20, 11:2, 25:11, 25:16, 39:12, 41:11, 84:7 single 81:8, 83:13 sir 11:10, 45:2, 50:11, 92:1 sit 11:22, 49:15, 49:20, 75:22 sits 50:17, 64:3 sitting 10:3, 43:11 situ 85:8 sizes 34:21, 36:22 skewed 8:5 sobriety 15:16 sold 21:1, 21:10 solid 89:4 some 9:16, 31:6, 33:8, 35:16, 40:15, 61:1, 65:13, 71:13, 85:2, 85:12, 85:15, 85:17,	91:2, 91:4 someone 16:11 something 19:2, 39:19, 52:20, 71:15, 79:19 sorry 78:5, 83:5 sort 41:8 sound 2:9, 12:18, 14:7, 18:4, 18:5, 18:6, 18:10, 18:14, 18:18, 18:21 source 40:5, 40:13, 40:14, 51:2, 63:22, 66:1, 66:2, 66:5, 66:7, 66:12, 66:14, 66:20, 73:6, 73:12, 73:15, 74:2, 74:16, 75:16, 75:20, 77:13, 77:17, 92:3 spacer 52:7, 52:12, 52:18, 53:4, 53:5 spacers 56:15, 56:22, 86:12, 87:3, 87:5, 87:16, 87:18 speak 87:22, 88:3 speaking 29:13 specific 22:20, 26:12, 30:6, 36:13, 41:11, 42:5, 42:10, 63:12, 79:20, 80:21	specifically 17:18, 23:12, 25:17, 26:16, 29:19, 30:11, 32:7, 32:15, 34:7, 37:6, 38:21, 42:2, 45:14, 46:11, 48:10, 49:19, 57:19, 60:10, 60:13, 62:11, 89:4 specification 61:4, 61:7, 62:8, 62:10, 75:19, 76:1, 77:16, 80:3, 86:11, 86:17, 87:2, 87:14 specifics 52:16 specifying 34:10 spent 90:7 spills 78:8 sputtering 81:17, 85:14 stage 75:6 standard 31:7, 36:5 standpoint 29:16, 50:15 start 64:16 started 11:4 state 2:12, 10:11, 35:1, 35:2, 47:20, 47:22, 81:2, 83:3, 86:14, 89:4, 91:12 statements 60:4
--	--	---	---

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

115

states 1:1 static 89:7 stenographically 93:13 stepped 84:10 still 31:6, 65:3, 72:6, 84:14 stmicro 32:13, 32:21, 32:22, 33:5, 33:8, 33:12, 33:18, 33:19, 33:21, 34:16, 35:21, 36:12, 36:19 stmicroelectroni- cs 32:12, 34:2, 36:18, 90:22 stopping 77:4 strain 40:2 strained 39:15, 39:19, 41:8 strategy 26:1, 26:2 strike 10:18, 52:11, 62:2, 80:20 structure 51:1, 52:17, 53:9, 62:22, 72:11, 73:20, 73:22, 74:13, 74:15, 75:1, 75:21, 76:3, 76:4, 76:5, 76:7, 77:15, 77:18 structures 25:12, 25:18, 29:20, 30:7,	32:8, 33:11, 33:17, 33:20, 34:9, 76:11, 76:22 sub 35:12 submitted 15:15, 15:19, 16:1, 16:5, 16:9, 16:13, 16:17, 16:21, 17:3, 17:7, 17:11 subsequent 89:17 substance 50:1, 50:3, 88:1, 88:3, 88:7 substrate 31:21, 41:6, 50:9, 50:14, 50:16, 50:17, 50:19, 51:1, 52:3, 52:17, 58:7, 59:10, 61:5, 70:12 suggest 65:8 suite 3:14 super 92:12 superposition 81:21 supported 61:6 supporting 9:14 supports 61:4 supposed 78:4 sure 5:20, 6:8, 25:14, 30:22, 31:11, 36:14, 45:19, 48:22, 51:22, 53:10,	67:5, 84:13 surface 50:18 susan 1:21, 2:10, 93:3, 94:13 switching 83:22 sworn 5:3, 93:8 system 15:17, 16:3, 18:8, 19:13, 92:10 systems 15:20, 15:22, 16:15, 17:1, 17:14, 32:16, 90:12 T taiwan 1:5 take 51:12, 64:22, 76:16, 77:8, 84:5, 84:8, 85:16 takeaway 85:16 taken 65:15, 93:4, 93:10, 93:12 talk 6:2, 28:15, 34:8, 39:18, 40:20, 80:6 talked 82:10 talking 9:22, 28:16, 29:4, 34:10, 34:11, 34:13, 40:21, 54:20, 58:17, 58:18, 58:19, 69:17, 72:6, 80:3, 84:21	tandy 23:7, 23:12 tapeout 29:12 teaches 68:5 techniques 17:5 technologies 22:18, 23:2, 23:4, 24:4, 24:19, 25:3, 42:2, 45:15, 47:1, 47:3, 47:18 technology 30:15, 31:6, 32:14, 32:19, 34:3, 35:15, 35:22, 36:5, 36:6, 39:5, 39:12, 40:14, 41:15, 45:10, 46:4, 48:1, 48:7, 48:17, 48:19, 50:4, 65:12, 65:14, 65:16, 89:20, 91:15, 91:17, 92:8 tell 27:7, 27:10, 35:6, 36:16, 49:15, 78:4 temperature 70:20 tems 29:1 tense 24:22, 25:1 tenure 89:6 terms 15:6, 23:19, 29:6, 31:13, 37:15, 40:12, 40:18, 41:13, 46:21, 47:7,
--	---	--	--

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

116

48:3, 57:7, 62:8, 65:18, 68:3, 70:21, 72:19, 83:18, 86:15 testified 5:3 testimony 6:19, 88:1, 88:4, 88:7, 93:11, 93:12 testing 16:19 texas 1:16, 2:10, 2:12, 25:8, 89:6, 89:11, 89:19, 94:14 th 9:15, 12:10, 49:8, 93:20, 94:9 thank 5:15, 43:20, 45:21, 55:13, 55:19, 58:20, 83:16, 87:10, 91:18, 92:14 thereafter 93:13 therefore 20:5, 52:21, 62:14, 62:16, 90:2 thickness 82:18, 82:19, 82:22, 83:6, 83:10 thing 23:18, 34:14, 68:8, 91:18 things 29:2 think 6:9, 12:20, 31:12, 40:11, 46:20, 47:10, 47:17, 60:4,	62:21, 63:11, 67:16, 71:14, 71:18 third 52:6, 52:18, 89:21 thought 13:5 three 15:1 three-dimensional 28:10, 43:16, 44:4, 45:1, 45:5, 45:13, 46:22, 47:5, 47:19 three-dimensiona- lly 29:9 through 14:17, 33:1, 33:13, 33:15, 34:6, 37:12, 44:6, 45:3, 48:20, 50:18, 53:15, 70:19, 76:1, 88:21 ti 26:1, 27:6, 27:16, 30:10, 30:13, 90:17, 90:19 ties 48:5 time 6:12, 8:1, 8:11, 8:16, 8:20, 10:22, 11:6, 24:2, 25:16, 28:8, 35:19, 36:1, 37:7, 40:14, 48:7, 49:10, 71:20, 90:21, 91:12, 92:15 timeframe 39:1, 39:13 timeline 15:11	times 8:5, 8:21, 24:8 titled 9:5, 42:15, 43:16, 44:3, 44:22 today 5:7, 5:19, 6:19, 7:1, 7:10, 7:13, 9:21, 10:4, 43:12, 47:2, 47:16, 47:18, 54:19, 87:22 told 71:2 took 21:2 top 59:8, 69:4, 81:18, 92:2 topic 15:22 total 13:15, 88:13, 88:20 towards 8:5, 85:4 tracking 17:5 trademark 1:1 transcribe 6:3 transfer 40:4, 67:10, 92:11 transistance 48:15 transistor 25:17, 26:12, 26:15, 28:4, 29:19, 30:16, 34:3, 36:3, 42:7, 45:14, 50:9, 50:13, 50:22, 51:7, 53:8, 72:11,	72:12, 72:16, 73:5, 73:13, 73:20, 74:13, 74:20, 74:22, 75:5, 76:10, 76:16, 77:21, 84:9, 90:11, 91:2, 91:8, 91:15, 92:8 transistors 26:3, 26:6, 27:22, 29:1, 34:17, 43:17, 44:4, 45:1, 45:5, 88:15, 89:1 translate 28:13, 29:5 translated 29:8 transport 64:20 trial 1:3 true 93:10 trust 51:18 truth 20:22, 78:5 try 29:2 trying 51:18 tsmc 45:19, 53:19, 54:1, 86:18, 87:6 tube 85:9, 85:11, 85:12 turn 10:6, 10:17, 10:19, 25:7, 51:20, 55:20, 57:9, 72:5, 75:12, 77:3, 78:7, 86:5,
--	---	---	---

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

117

91:19 tv 26:3, 26:8 two 41:20, 45:11, 48:8, 53:18, 58:6, 59:8, 70:6, 70:9, 81:19, 81:22, 84:20 type 12:2, 28:8, 31:9, 36:5, 45:10, 68:8 types 31:18 typewriting 93:14 typical 65:12, 85:18 typically 79:19	67:20, 68:18, 69:7, 69:11, 70:7 understand 6:1, 6:11, 7:2, 9:22, 43:3, 46:19, 49:21, 54:20, 55:9, 56:8 understanding 6:22, 7:6, 53:3, 71:5 underwater 90:9, 90:13 unfortunately 64:15 uniform 84:17 united 1:1 university 10:11 unless 6:13, 51:17, 67:13 unworkable 78:13, 79:5 up-to-date 10:22 upper 12:9, 12:16, 14:5 uranium 39:20 use 18:3, 29:11, 31:4, 55:8, 81:14 uses 31:6 using 32:18, 36:5, 39:19, 62:13, 63:3, 79:19 utilizing 31:18, 62:9	validity 7:9, 9:17, 43:8, 48:4 valuation 18:13 variations 84:5, 85:17, 85:21 various 28:20 vegas 19:3 verbally 6:2 version 57:14 versus 8:9, 12:22, 43:16, 44:3, 45:1, 46:22 vertical 50:22 vice 89:20 view 46:16, 52:10, 52:12, 60:7, 63:17, 65:22, 67:17, 74:15 voltage 40:4, 64:3, 64:10, 65:20	wang 53:20 want 39:18, 48:7, 51:12, 51:17, 54:10, 67:6, 71:20 washington 3:8 way 12:1, 31:13, 39:7, 40:1, 40:8, 40:13, 40:16, 41:2, 48:14, 60:10, 62:9, 66:18, 68:9, 69:20, 75:2, 83:3, 84:11, 84:22, 94:6 ways 31:17 we're 5:19, 5:20, 7:8, 28:16, 29:4, 47:12, 47:16, 72:6, 78:17 we've 51:11 weighted 41:14 welcome 78:2 went 14:17 whatsoever 86:14 whereof 94:8 whether 46:21, 68:3 wide 64:9 width 64:13, 65:9 widths 86:12, 87:3,
U		W	
uh-huh 30:21, 45:16, 82:8 umbrella 23:4 under 19:15, 20:4, 21:2, 24:5, 25:22, 27:16, 60:8, 61:7, 61:10, 66:13, 66:17, 70:2, 81:15, 93:14 undercut 62:20, 63:9 undercuts 66:21 underneath 60:6, 60:15, 61:3, 62:1, 62:6, 62:15, 62:17, 63:14, 63:15, 63:18, 64:5, 64:13,	vacuum 85:16	w-a-n-g 53:21 wafer 37:8, 37:11, 37:12, 37:22, 83:11, 83:15, 83:18, 84:1, 84:6, 84:11, 84:17, 84:21, 85:6, 85:7, 91:9 wafers 28:11, 85:10 walk 88:21	

Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

118

87:15 wireless 17:8 wirelessly 90:13 wise 89:6 within 8:14, 8:15, 13:16, 23:4, 63:11, 66:2, 69:16, 71:18, 82:13, 83:13, 84:21, 85:18, 88:4 witness 4:2, 7:16, 8:22, 18:3, 55:16, 88:9, 93:7, 93:11, 94:8 word 50:2, 55:11 words 13:8, 13:18, 28:4, 36:7, 49:2, 73:19, 84:7 work 17:17, 18:9, 18:14, 18:18, 22:11, 25:21, 30:4, 30:5, 30:9, 30:10, 32:7, 32:11, 32:12, 32:13, 32:17, 32:20, 32:22, 33:2, 33:9, 33:10, 40:6, 45:17, 88:14, 90:17 workable 84:15 worked 25:11, 25:15, 26:6, 26:20, 30:1, 34:7, 35:5, 35:20,	36:4, 36:12, 40:19, 49:1, 91:1 working 26:1, 30:11, 35:19, 90:9, 90:18, 91:16 wouldn't 13:3 write 88:6 written 68:9 wrong 53:13, 55:11 Y yeah 46:1, 82:3 year 11:16, 14:18, 32:3, 42:9, 91:7 years 8:15, 8:16, 8:18, 29:22, 32:3, 32:20, 33:12, 35:6, 88:14, 88:19, 89:12, 89:19, 90:7, 91:7, 91:16 york 3:7 . .1500 3:16 .4000 3:9 0 0021 17:19 00847 1:11 03 78:1 05 2:4, 93:20	076 23:11 1 1 59:3 10 8:14, 8:16, 35:6, 41:21, 43:15, 43:21, 78:1, 94:14 100 35:18, 35:20, 36:1 1001 4:16, 45:19, 45:20, 51:21 1005 4:17, 86:19, 86:21 1006 4:18, 87:7, 87:9 1008 4:19, 53:16, 53:19, 53:22, 54:17 1009 4:20, 54:1, 54:4, 54:13, 54:20, 60:11, 86:6 101 2:9 108 14:20 109 12:17, 12:18, 14:6 11 4:9, 35:6, 78:1, 87:20, 92:17, 93:21, 94:15 12 4:10, 44:18, 44:21, 45:3, 48:19, 90:7	1201 4:9, 11:12, 11:13, 12:21, 12:22, 13:5, 13:6, 13:7, 13:17 1202 4:10, 4:11, 12:5, 12:6, 12:22, 13:15, 13:20, 14:6, 14:10, 14:17, 14:22, 15:5 1203 4:11, 14:14, 14:15 1215 4:12, 55:1, 55:2, 55:4 13 12:10 14 4:11, 50:7, 75:12, 75:15, 75:18, 75:21, 76:6, 76:9, 77:1 14487 94:15 15 9:15, 49:8, 50:20, 91:7 16 45:3, 48:20, 87:20 17 1:17, 2:3, 93:20 18 94:9 1972 25:9, 39:4 1976 39:22, 40:2 1986 25:9, 25:11 1990 8:2, 8:4, 8:6, 8:16, 30:3,
---	--	---	---

PLANET DEPOS
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Transcript of Joseph C. McAlexander, III
Conducted on March 17, 2026

119

30:4, 32:5, 32:6, 33:1, 33:5, 33:15, 37:20, 41:11, 42:9, 90:21 1b 61:13, 61:22, 62:3, 67:17, 68:15 2	2013 11:16 2016 33:1, 33:5, 90:22 202.408 3:9 2020 21:22, 22:4 2025 1:11, 9:15, 11:9, 11:16, 49:8 2026 1:17, 2:3, 12:10, 14:22, 43:1, 93:20, 94:9 22 57:9, 57:12, 58:12, 58:16, 59:15, 59:19, 59:22, 60:17 24 43:14, 43:19, 44:2, 44:6 26 78:9, 78:17, 91:19, 91:22, 94:15 27 94:14 28 44:6 29 87:20 2d 50:8, 50:12 3	34 10:17 35 92:17, 93:21 350 7:22 3580 3:14 3d 50:21, 51:6 4	7,449,753 53:20 7,591,659 54:2 7,745,847 1:12, 7:10, 9:8 7,935,590 86:20 7,989,906 41:20 70 39:7 72 38:22, 39:1, 39:12 74 72:5, 72:7 79 39:1, 39:13 8
20 35:16, 35:18, 35:20, 35:22, 41:21, 57:11, 65:13, 65:16 200 9:1 20001 3:8 2001 4:21, 9:5, 9:10, 9:16, 17:16, 24:20, 25:8, 50:7, 50:20 2002 19:3 2003 4:22, 42:14, 42:18, 43:2, 53:11, 57:10, 58:12, 59:15, 59:20, 78:17, 91:19 2006 21:22, 22:4 2007 48:6 2008 41:16 2010 33:14, 33:15, 33:22, 41:21 2011 33:14, 33:15, 33:22, 34:6, 41:20	30 10:20, 94:15 300 3:14, 7:22 31 55:22, 56:6, 94:14 32 56:1, 56:6	50 8:8 51 56:13 53 4:19, 56:13 54 4:20, 88:19 55 4:12 59 78:8, 78:10, 78:20 6	8,334,775 23:13 847 7:11, 9:17, 43:8, 45:16, 45:22, 46:5, 48:2, 48:4, 48:5, 48:11, 51:20, 58:4, 60:12, 62:8, 62:18, 67:15, 69:5, 73:11, 74:1, 74:10, 75:13, 75:15, 77:3, 77:18, 79:16, 79:21, 80:3 858.314 3:16 86 4:17 87 4:18 88 4:5 9
		624426 1:22 6531 94:14 7	7,026,689 87:8 7,353,706 41:18

90
37:15, 38:8
901
3:7
92130
3:15
9th
43:1