

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner.

Case No. IPR2025-00847
U.S. Patent No. 7,745,847 B2

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. THE CHALLENGED CLAIMS ARE PATENTABLE	2
A. Petitioner’s Own Arguments Regarding Patent Drawings Illustrate Why The Asserted References’ Patent Drawings Are Unreliable	3
B. The Chen Grounds Do Not Disclose Or Render Obvious “Two Raised Epitaxial Layers Positioned... Next To The Relative Sides Of The Gate”	8
1. The Gate Dielectric Layer Is Part Of The Gate	8
2. Chen’s Epitaxial Layers Are Not “Next To” The Sides Of The Gate Under The Plain And Ordinary Meaning Of “Next To”	11
C. No Asserted Ground Discloses Or Renders Obvious Claim 2	12
1. Petitioner’s Attempt To Introduce A New Theory Of Invalidity On Reply Is Improper	13
2. A POSITA Would Not Have Been Motivated To Retain Lan’s Cap Layer (Grounds 1C And 1D)	14
3. Chen Does Not Disclose Or Render Obvious Claim 2 (Grounds 4A And 4B)	16
III. MR. MCALEXANDER’S TESTIMONY IS CREDIBLE	16
IV. CONCLUSION	19

TABLE OF AUTHORITIES

Page(s)

Federal Cases

<i>Giesecke+Devrient GmbH v. Lumenco, LLC</i> , No. IPR2024-00838, Paper 31 (P.T.A.B. Nov. 19, 2025).....	17
<i>Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.</i> , 222 F.3d 951 (Fed. Cir. 2000)	5
<i>Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.</i> , 821 F.3d 1359 (Fed. Cir. 2016)	13
<i>Xerox Corp. v. Bytemark, Inc.</i> , IPR2022-00624, Paper 9 (P.T.A.B. Aug. 24, 2022).....	17, 18

TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph McAlexander III
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	Second Declaration of Joseph McAlexander III
2004	Transcript of January 6, 2026, Deposition of Eugene Fitzgerald, Ph.D.
2005	Igor Polishchuk, <i>Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion</i> , IEEE ELECTRON DEVICE LETTERS, Vol. 22, No. 9, September 2001.
2006-2100	<i>Reserved</i>
2101	Procedural Schedule (Order No. 10) (May 7, 2025) from 337-TA-1443
2102	Defendants’ Unopposed Motion To Stay Action Pending ITC Determination (Dkt 28) (April 18, 2025) from Case No. 2:25-cv-00171-JRG (EDTX)
2103	Unopposed Motion To Stay Action Pursuant to 28 U.S.C. § 1659 Pending Parallel ITC Action (Dkt 24) (April 10, 2025) Case No. 1:25-cv-00215-ADA (WDTX)
2104	Order Granting Defendants’ Unopposed Motion To Stay (Dkt 29) (April 23, 2025) from Case No. 2:25-cv-00171-JRG (EDTX)
2105	Order Granting Unopposed Motion To Stay Action (Dkt 25) (April 21, 2025) Case No. 1:25-cv-00215-ADA (WDTX)
2106	ITC Motion to Stay Pending IPR Stats
2107	Guidance on USPTO’s Recission of ‘Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation’” (the “Guidance Memo”)
2108	Section 337 Statistics: Average Length of Investigations (April 11, 2025)
2109	Notice of Institution of Investigation (March 21, 2025) from 337-TA-1443
2110	Proposed Respondent Apple Inc.’s Action Request Not to Institute and Public Interest Statement Under Commission Rule 210.8(c) (March 4, 2025) from 337-TA-1443

2111	Proposed Respondent Taiwan Semiconductor Manufacturing Company Limited's Statement Regarding the Public Interest (March 4, 2025) from 337-TA-1443
------	---

I. INTRODUCTION

Petitioner attempts to re-write its Petition, presenting new arguments on reply that contradict the Petition. **First**, Petitioner's arguments regarding the Lan reference's spacers contradict the Petition's reliance on patent drawings to determine precise proportions and particular sizes. Petitioner argues that Patent Owner impermissibly relies on Lan's Figure 4 to show that Lan's main spacer 302 covers approximately half of the epitaxial layer, which belies the Petition's contentions that the same figure allegedly discloses: (1) raised epitaxial layers and (2) spacers extending laterally onto the epitaxial layers:

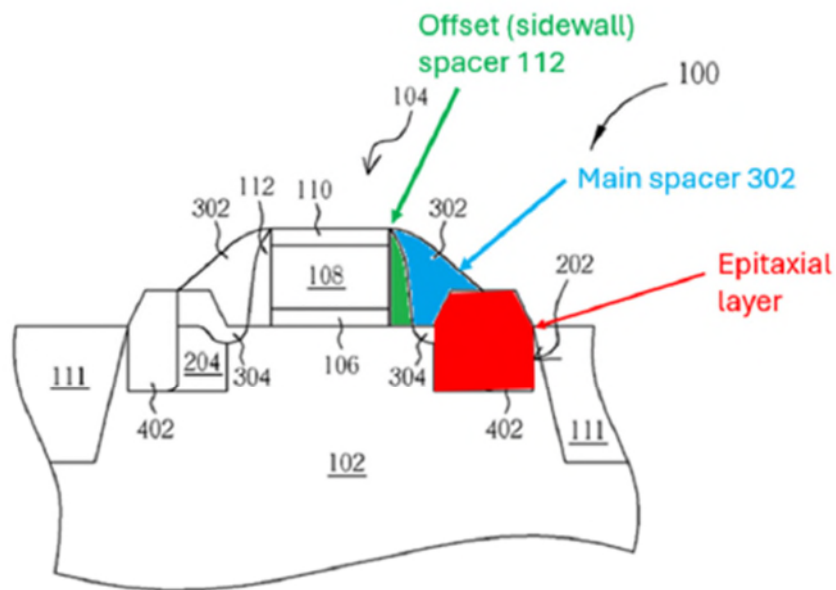


Fig. 4

Second, Petitioner now proposes new constructions on reply that: (1) the claim language “two raised epitaxial layers positioned respectively... next to the relative sides of the gate” may be satisfied if **any portion** of the epitaxial layers are positioned next to the relative sides of the gate; and (2) the “relative sides of the gate” are defined by only the gate conductor regardless of the position of the gate dielectric layer. These new constructions contradict the Petition’s contention that the “relative sides of the gate” refer to the entire gate stack comprising the gate dielectric layer. Moreover, the Petition did not raise any claim construction issue regarding these limitations.

Third, Petitioner now argues that the cap layers in Lan and Chen satisfy the “gate cap layer” limitation of claim 2 even if they are removed in the finished device. This is in clear contrast to the Petition, which consistently argued that these cap layers would satisfy claim 2 only because it would have been obvious to retain these cap layers.

In short, Petitioner’s reply improperly attempts to remedy shortcomings of the Petition by introducing new theories of invalidity that directly contradict the Petition. The Board should not entertain Petitioner’s attempts to re-write its Petition on reply.

II. THE CHALLENGED CLAIMS ARE PATENTABLE

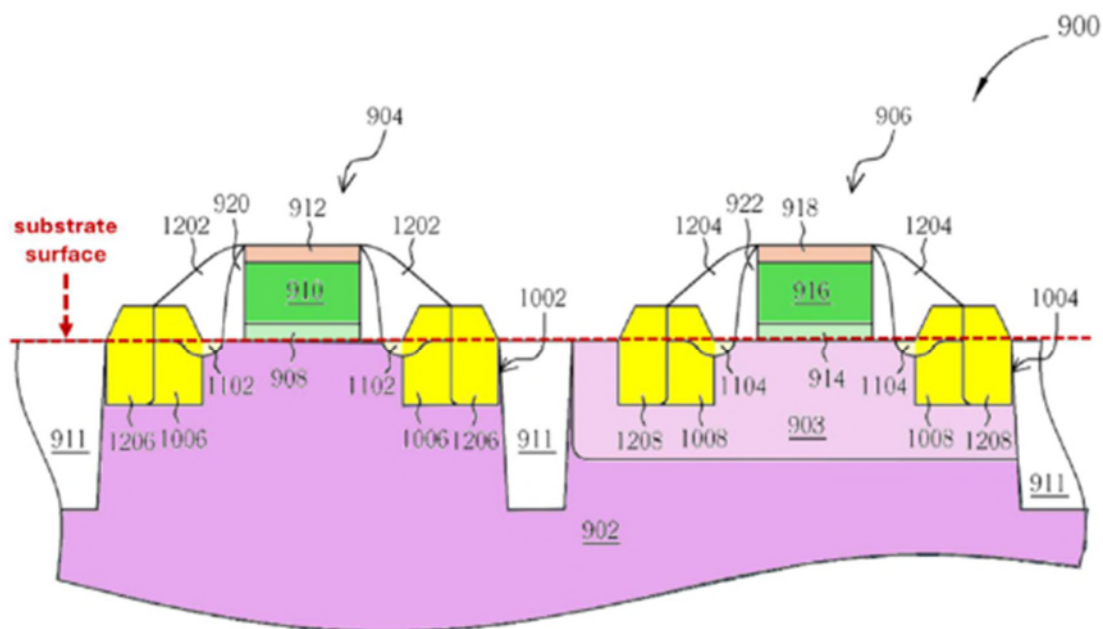
All challenged claims 1-11 should be upheld as patentable, because no prior art reference discloses or renders obvious “raised epitaxial layers.” At the very least,

claim 2 is patentable, because no asserted ground discloses or renders obvious a gate comprising a cap layer.

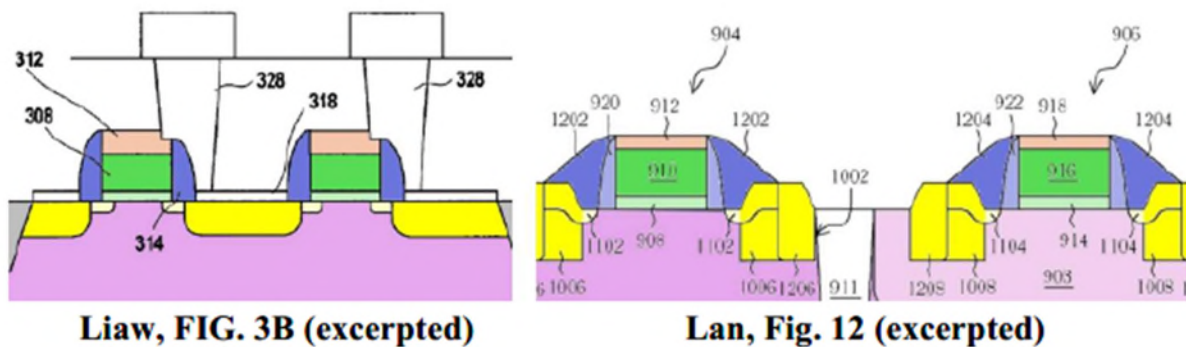
A. Petitioner's Own Arguments Regarding Patent Drawings Illustrate Why The Asserted References' Patent Drawings Are Unreliable

Petitioner agrees that precise or actual dimensions may not be extracted from drawings not to scale. Reply, 2. However, Petitioner characterizes the Petitioner's use of patent drawings as showing "general shapes and relative sizes of elements," rather than precise dimensions. Reply, 2-3. But Petitioner's distinction is undermined by its own arguments regarding the figures of the Lan reference.

For context, below is a brief summary of the briefing to date with respect to the issue at hand. In the Petition, Petitioner argued that Figure 12 of Lan discloses epitaxial layers that extend above the surface of the substrate:



Pet., 21 (showing annotated EX1005-Lan, Fig. 12). The Petition also argued that Figure 12 disclosed that Lan’s main spacers 1202 and 1204 “extend onto a portion of Lan’s epitaxial layers 1006 and 1008” and that “epitaxial layers 1006/1008 are spaced away from the gate edge.” Pet., 24, 31-32. Separately, regarding claim 2, the Petition argued that a POSITA would have been motivated to implement Liaw’s cap layer in Lan in order to mitigate potential issues with misaligned electrical contacts:



Pet., 39-45.

In its Response, Patent Owner pointed out that—as stated in the Petition—Lan’s figures depict Lan’s main spacers extending laterally onto part of the epitaxial layer:

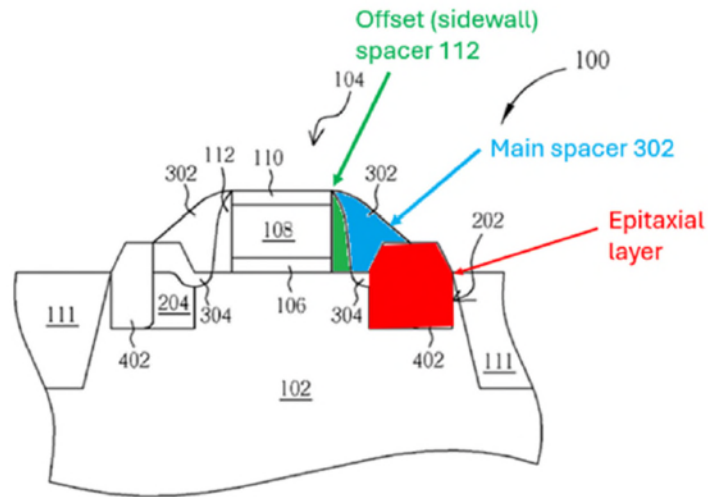


Fig. 4

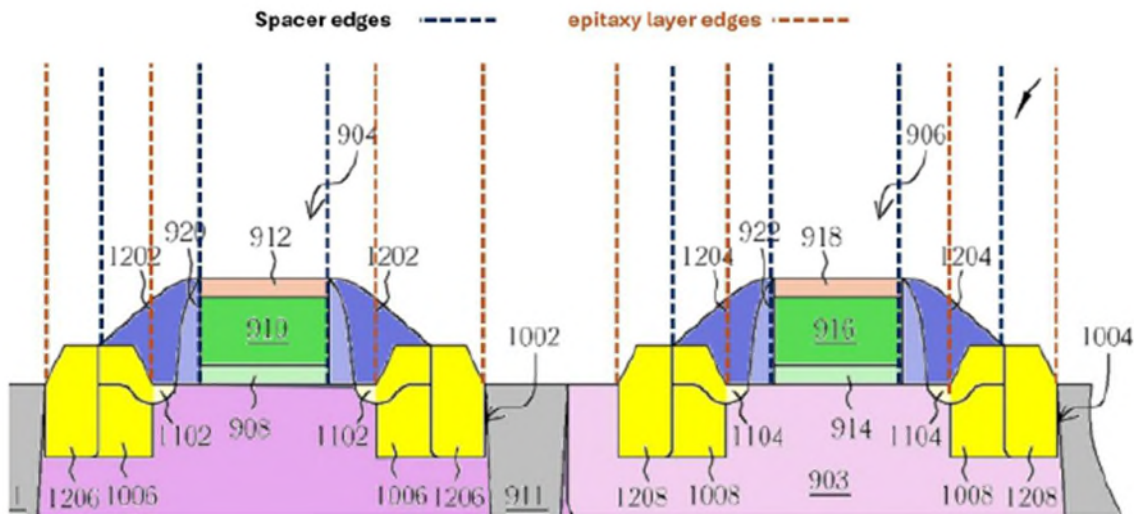
POR, 39-41 (showing annotated EX1005-Lan, Fig. 4).¹ Thus, Lan's wide main spacers obviate the need for Liaw's cap layer, because Lan's main spacers already provide resilience against contact misalignment by spacing out the epitaxial layer from the gate structure. *Id.*

In response, in its Reply, Petitioner argues that “Marlin [] attempts to use non-scale drawings for an impermissible purpose: extracting ‘precise proportions’ and ‘particular sizes.’” Reply, 18-19 (citing *Hockerson-Halberstadt, Inc. v. Avia Group Int’l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000)). But Petitioner cannot credibly argue that its sole reliance on Lan’s figures—to allegedly disclose

¹ For the purposes of depicting the spacers covering a portion of the epitaxial layer, Figures 4 and 12 are identical.

the claim element “raised epitaxial layers positioned... above the surface of the semiconductor substrate” to invalidate a patent claim—is *proper*, while simultaneously arguing that Patent Owner’s reliance on those same figures as showing that Lan’s spacers cover a substantial portion of Lan’s epitaxial layers is *improper*. This is especially so because unlike Petitioner, Patent Owner is not interpreting Lan’s figures inconsistently with Lan’s written description. As explained in the Patent Owner Response, the written description of Lan (as well as that of the three other primary asserted references) describe the epitaxial layers as being formed *in* a recess in the substrate. POR, 24-25. In contrast, the ’847 Patent describes that its epitaxial layers are “raised” because they are not merely grown “in” the recesses, they are further grown “higher than the surface of the semiconductor substrate”: “epitaxial layer 220 is grown in the recess 218 **and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.**” EX1001 at 3:35-38.

Moreover, as explained, the Petition uses Lan’s Figure 12 for substantially the same proposition as in the POR. Regarding claim 9, which requires that “the edge of the raised epitaxial layers is not aligned with the edge of the spacer,” the Petition relies upon Lan’s Figure 12 to show that “epitaxial layers 1006/1008 are spaced away from the gate edge:



Lan, Fig. 12 (excerpted, annotated)

Pet., 32 (showing annotated EX1005-Lan, Fig. 12). Petitioner offers no explanation for why it believes that Figure 12 may properly be relied upon to show that the spacers cover a portion of the epitaxial layers for the purposes of invalidating claim 9 but not to rebut Petitioner's proffered motivation to combine Lan and Liaw.

In short, Petitioner's contradictory arguments regarding patent drawings are illogical and unprincipled. If Lan's figures may not be relied upon to show that the main spacer covers a substantial portion of the epitaxial layer, then the figures similarly may not be relied upon to show that the epitaxial layers in the asserted references are raised above the semiconductor substrate.

B. The Chen Grounds Do Not Disclose Or Render Obvious “Two Raised Epitaxial Layers Positioned... Next To The Relative Sides Of The Gate”

Next, Petitioner argues that Chen’s epitaxial layers are positioned “next to the relative sides of the gate” because: (1) the “relative sides of the gate” are allegedly defined by the width of the gate conductive layer and does not include the gate dielectric layer; and (2) the claim language is allegedly met as long as any portion of the epitaxial layer is beside the sides of the gate. Reply, 6-13. Patent Owner addresses each of these issues below.

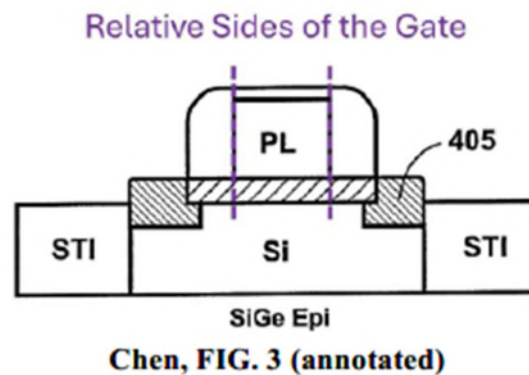
1. The Gate Dielectric Layer Is Part Of The Gate

The ’847 Patent explains that “[e]ach gate 208 comprises a dielectric layer 210, a conductive layer 212 positioned on the dielectric layer 210 and a cap layer 213 positioned on the conductive layer 212.” EX1001, 3:3-6. Thus, the gate dielectric layer is part of the gate, and as such, the “relative sides of the gate” is defined in part by the width of the gate dielectric layer. Indeed, the Petition conceded as much—in arguing that Chen discloses two raised epitaxial layers next to the relative sides of the gate, the Petition explicitly describes the “gate” as including the gate dielectric layer:

Accordingly, Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), two raised epitaxial layers (silicon germanium material 405) positioned respectively in the semiconductor substrate (semiconductor substrate

101) *next to the relative sides of the gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask)* and above the surface of the semiconductor substrate.”

Pet., 72 (emphasis added). But in contrast, on reply, Petitioner turns around and argues that the phrase “the relative sides of the gate” refers only to the sides of the gate conductive layer. Reply, 10-11. As shown below, Petitioner now argues that the “relative sides of the gate” should be defined exclusively by the width of the gate conductive layer, even though the gate dielectric layer extends beyond the gate conductive layer:



Reply, 11. This argument contradicts both the '847 Patent and the Petition itself. Because the gate includes the gate dielectric layer, the relative sides of the gate must also be defined in part by the gate dielectric layer. Thus, in Chen, where the gate dielectric layer extends past the gate conductive layer, the relative sides of the gate are defined by the width of the gate dielectric layer, as illustrated below:

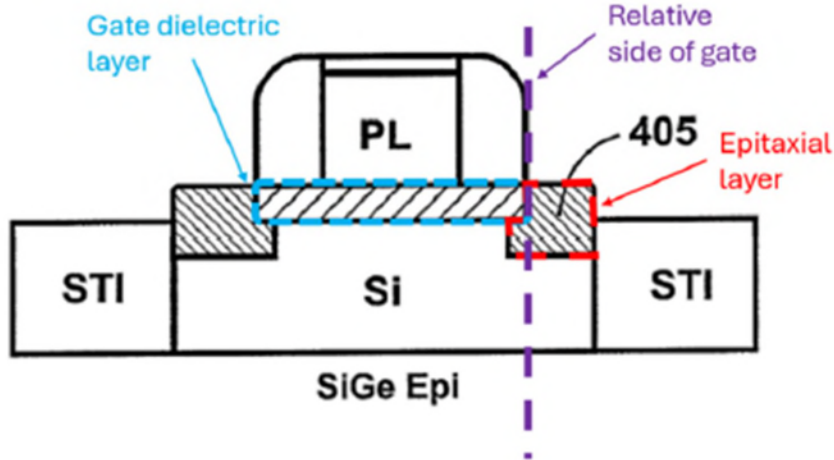


FIGURE 3

POR, 29 (annotated EX1009-Chen, Fig. 3).

Petitioner points to passages in Chen that refer to the edges of the patterned gate layer. Reply, 11 (citing EX1009-Chen, 3:45-48, 4:49-51). But these passages are irrelevant. The edges of the patterned gate layer (labelled “PL” in the Figure 3 above) do not define the “relative sides of the gate,” as used in the ‘847 patent, because the gate dielectric layer is part of the gate and in Chen, the gate dielectric layer extends past the patterned gate layer.² EX2003-McAlexander-Decl, ¶¶44-49.

² Petitioner appears to tacitly suggest that Chen’s “gate” or “gate structure” does not include the gate dielectric layer. See Reply, 11 (“Chen teaches to ‘[f]orm a gate layer (e.g., polysilicon, metal) overlying the dielectric layer’ and to ‘[p]attern the gate layer to form *a gate structure including edges (e.g., a plurality of sides or edges).*’”) (emphasis in original). This contradicts Petitioner’s contentions that Chen discloses

2. Chen’s Epitaxial Layers Are Not “Next To” The Sides Of The Gate Under The Plain And Ordinary Meaning Of “Next To”

Because the gate dielectric layer is part of the gate, Chen’s epitaxial layers are not positioned next to the relative sides of the gate. Petitioner argues that the claim language “next to the relative sides of the gate” is met as long as any portion of the epitaxial layer is beside the sides of the gate. Reply, 6-10. Asserting that “[t]his is not a question of claim construction,” Petitioner argues that the ordinary meaning of the “next to the relative sides of the gate” includes if any part of the epitaxial layer is beside the sides of the gate. Reply, 7-8. In essence, Petitioner is advocating for a belated construction that “next to” means “at least partially next to.” But this new argument is entirely conclusory—Petitioner advances no evidence or justification for this belated construction. Reply, 8. Thus, Petitioner has failed to set forth a *prima facie* allegation that the claim language “epitaxial layers positioned... next to the relative sides of the gate” is satisfied when only part of the epitaxial layers are beside the sides of the gate. Petitioner therefore fails to satisfy its burden as to element 1[b].

all elements of claim 2, which recites, in relevant part, that “the gate further comprises: a dielectric layer.”

C. No Asserted Ground Discloses Or Renders Obvious Claim 2

Petitioner’s arguments regarding claim 2 rely improperly and illogically on transistor designs that include a *sacrificial* cap layer—that is, a cap layer that is not present in the finished device. In its Petition, Petitioner consistently interpreted claim 2 as requiring the gate cap layer to be retained. That is, the Petition’s invalidity theory excluded any argument that a cap layer that is subsequently removed could satisfy element 2[c]. This is clear for multiple reasons.

At the outset, Petitioner’s asserted grounds confirm that the Petition did not contemplate that a subsequently-removed cap layer would satisfy element 2[c]. Only four grounds challenged claim 2: Grounds 1C, 1D, 4A, and 4B. Pet., 1. Significantly, the Petition did not allege that Lan anticipates claim 2, even though Lan discloses a cap layer that is subsequently removed. Instead, the Petition merely alleged that it would have been obvious to retain the cap layer in view of Lan, either alone (Ground 1C) or in combination with Liaw (Ground 1D). Pet., 35-45. At no point did the Petition allege that Lan’s cap layer—which is removed—discloses element 2[c]. Indeed, if the Petition had contemplated such a theory of invalidity, it would have challenged claim 2 in Ground 1A as anticipated by Lan.

Similarly, the Petition’s allegations that Chen anticipates claim 2 were rooted in its arguments that Chen explicitly disclosed an embodiment in which Chen’s “hard mask” (the alleged cap layer) is retained in a “finished device.” Pet., 80. At

no point did the Petition allege that Chen's hard mask discloses element 2[c] ***even if removed***. This is further confirmed by the Petition's Ground 4B, which alleged that "a POSITA also would have found it obvious, based on prior training (Ground 4B), to retain Chen's cap layer (hard mask) in the final device structure." Pet., 80-81.

1. Petitioner's Attempt To Introduce A New Theory Of Invalidity On Reply Is Improper

"It is of course well-established that new arguments cannot be raised in a reply brief." *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). "Allowing the petitioner to belatedly advance arguments on reply would circumvent the statutory requirement that a petitioner must identify 'with particularity' the evidence that supports the grounds for the challenge to each claim." *Id.* (citing 35 U.S.C. § 312(a)(3)).

Here, as explained above, the Petition did not set forth any argument that a cap layer that is subsequently removed satisfies claim element 2[c]. Nevertheless, in its Reply, Petitioner argued for the first time that Lan and Chen alone disclose element 2[c], regardless of whether the cap layers in those reference are removed. Reply, 21-24. Thus, Petitioner's new arguments are improper and should be disregarded. Regardless, Petitioner's new argument is unpersuasive, because the '847 Patent's claimed "gate cap layer" is not a sacrificial layer but rather is retained

in the finished device. EX1001, 56:59, Fig. 14 (showing final transistor structure with gate cap layers 313).

2. A POSITA Would Not Have Been Motivated To Retain Lan's Cap Layer (Grounds 1C And 1D)

The Petition admits that a POSITA would have understood that Lan's cap layer would be removed. Pet., 36. Nor does Petitioner identify any disclosure in Lan that would even suggest that the cap layer could be retained. Instead, the Petition alleged that a POSITA would have been motivated to retain Lan's cap layer if the gate conductive layer was metal instead of polysilicon, because there would allegedly be no reason to remove the cap layer in that scenario. Pet., 37-38.

The Patent Owner's Response rebutted this allegation, articulating multiple reasons why a POSITA would have understood that Lan's cap layer would be removed, including to perform additional processing on the gate conductive layer, regardless of whether the conductive layer is made from metal or polysilicon. POR, 33-37. Instead of meaningfully addressing these reasons, Petitioner attempts to write these reasons off as "irrelevant speculation." Reply, 15. But Patent Owner's arguments are at the very least no more speculative than the Petition's affirmative allegation that it would have been obvious to retain the cap layer. Patent Owner has thus offered unrebutted reasons why a POSITA would not have been motivated to retain Lan's cap layer as Petitioner alleges.

Petitioner similarly fails to meaningfully address Patent Owner's showing that a POSITA would not have been motivated to implement Liaw's cap layer in Lan. Lan's spacers separate the source/drain region from the gate and thus obviate the need for Liaw's cap layer. POR, 37-41. Again, Petitioner urges the Board to simply disregard these reasons, arguing that Lan's figures may not be used for this purpose. As explained above in Section II.A, these arguments contradict Petitioner's own positions. Petitioner also argues that Lan faces the same misalignment problem as Liaw because "Moore's Law of device scaling means that Lan and Liaw are trying to fit their respective transistors within a comparable physical space, such that their total sidewall thicknesses would be similar." Reply, 19. This argument strains reason. Even taking this argument at face value, common sense dictates that when devices are scaled to be smaller, the size of all components—including the electrical contacts—must also be smaller. But that does not mean that the relative proportions of the components within the device change. Thus, Lan's configuration would always include spacers covering a portion of the epitaxial layers, thereby separating the source/drain region from the gate, regardless of the total size of the device. Thus, Lan's spacers obviate the need for Liaw's cap layer.

3. Chen Does Not Disclose Or Render Obvious Claim 2 (Grounds 4A And 4B)

With respect to the Chen reference (Grounds 4A and 4B), the Reply simply re-states the Petition's argument that Chen discloses an embodiment in which the "hard mask" is retained. Reply, 20-21. Patent Owner already exposed these arguments as incorrect in the Patent Owner Response. POR, 41-45. Petitioner offers no rebuttal. Thus, Grounds 4A and 4B fail to disclose or render obvious claim element 2[c].

III. MR. MCALEXANDER'S TESTIMONY IS CREDIBLE

Conspicuously, Petitioner fails to meaningfully address many of Mr. McAlexander's technical opinions. For example, Petitioner does not substantively dispute at least the following of Mr. McAlexander's opinions:

- Lan's main spacers already protect against misalignment and thus serve the same purpose as Liaw's cap layer. EX2003-McAlexander-Decl, ¶¶67-69.
- Even with a metal gate, Lan's cap layer and Chen's hard mask would be removed to perform additional processing on the gate, such as to diffuse an additional metal layer onto the gate to improve work function and adhesion. *Id.*, ¶¶60-61.
- A gate metal would be functionally unaffected by an etchant after a salicide process performed on the source/drain regions due to the large

relative thickness of the gate metal in comparison to the silicidation metal. *Id.*, ¶62.

- Positioning the epitaxial layer under the gate (as disclosed in Chen) increases the risk of an electrical or physical short between the gate and the source/drain region. *Id.*, ¶51.

Unable to address Mr. McAlexander's testimony head-on, Petitioner instead resorts to attacking Mr. McAlexander's credibility. Petitioner argues that Mr. McAlexander's testimony should be afforded little weight because (1) Mr. McAlexander's declaration lacks technical analysis or supporting evidence; and (2) Mr. McAlexander lacks relevant expertise. Reply, 24-25. Both of Petitioner's arguments are unfounded and factually incorrect.

First, Petitioner is incorrect that expert testimony may be disregarded merely because it is similar to the party's arguments. Indeed, where a party's arguments are based on and supported by an expert's technical analysis, there will naturally be overlap between the analysis and arguments. Neither of Petitioner's cited cases stand for Petitioner's proposition. Rather, the expert testimony in the *Giesecke+Devrient* and *Xerox* cases was afforded little weight because it was conclusory and lacked technical analysis. *Giesecke+Devrient GmbH v. Lumenco, LLC*, No. IPR2024-00838, Paper 31, at 21 (P.T.A.B. Nov. 19, 2025); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, at 15-17 (P.T.A.B. Aug. 24, 2022). For

example, in *Xerox*, Petitioner’s expert’s testimony merely repeated the conclusory assertion that “[a] POSITA would understand that such a blocking would require recording the blocking in a data record associated with that user’s account.” *Xerox*, IPR2022-00624, Paper 9, at 15. That is not the case here. Mr. McAlexander’s declaration is replete with technical analysis supporting his opinions.

Tellingly, Petitioner omits the fact that its own expert’s declaration (Ex. 1003) also—to use Petitioner’s own language—“parrots” the language in the Petition. In myriad instances, the declaration merely recites the exact same language, or substantially similar language with minor word changes, as the Petition. *E.g.*, Pet., 1-2 (citing EX1003-Fitzgerald-Decl, ¶¶45-50); Pet., 5-6 (citing EX1003-Fitzgerald-Decl, ¶¶57, 58); Pet., 11-12 (citing EX1003-Fitzgerald-Decl, ¶38); Pet., 19-23 (citing EX1003-Fitzgerald-Decl, ¶¶103-117); Pet., 25 (citing EX1003-Fitzgerald-Decl, ¶¶121-123); Pet., 47 (citing EX1003-Fitzgerald-Decl, ¶¶199-201); Pet., 49 (citing EX1003-Fitzgerald-Decl, ¶208); Pet., 62-64 (citing EX1003-Fitzgerald-Decl, ¶¶256-262). This is yet another example of Petitioner attempting to hold Patent Owner to a different standard than itself.

Second, Petitioner incredibly argues that Mr. McAlexander lacks meaningful expertise in the relevant technologies, despite the fact that Mr. McAlexander has **54 years of experience** in the design and manufacturing of transistors, including MOSFETs—the very technology at issue. EX1204-McAlexander-Dep, 88:13-20.

His experience includes, among numerous other positions, consulting with STMicroelectronics regarding MOS transistor designs from the early 1990s to about 2016, which coincides with the time frame of the '847 Patent and Petitioner's asserted references. *Id.*, 88:21-91:17. In contrast, Petitioner's expert's industry experience at Bell Laboratories—which Petitioner touts in its Reply—lasted just six years in total and ended in 1994, over a decade before the relevant time frame. EX1004-Fitzgerald-CV, 1. Regardless, Mr. McAlexander's over half a century of relevant expertise is more than sufficient to opine on the issues in this case.

IV. CONCLUSION

For at least the reasons discussed above, the challenged claims of the '847 Patent should be upheld as patentable.

Dated: May 12, 2026

Respectfully submitted,

/s/ William A. Meunier

William A. Meunier (Reg. No. 41,193)
Adam S. Rizk (Reg. No. 66,867)
Michael T. Renaud (Reg. No. 44,299)
MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO, P.C.
One Financial Center
Boston, MA 02111
Telephone: (617) 348-1793
E-mail: WAMeunier@mintz.com
ARizk@mintz.com
MTRenaud@mintz.com
Mintz-Marlin-IPRs@mintz.com

Reza Dokhanchy (Reg. No. 62,795)
MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO, P.C.
3580 Carmel Mountain Road, Suite 300
San Diego, CA 92130
Telephone: (858) 314-1500
RDokhanchy@mintz.com

Tawfik Goma (Reg. No. 67,416)
MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO, P.C.
777 Brickell Avenue, Suite 500
Miami, FL 33131
Tel: (786) 949-6600
TAGoma@mintz.com

*Counsel to Patent Owner Marlin
Semiconductor Ltd.*

CERTIFICATE OF WORD COUNT

The undersigned certifies that the portions of the above-captioned PATENT OWNER'S SUR-REPLY specified in 37 C.F.R. § 42.24(a)(1) have 3,465 words, in compliance with the 5,600 word limit set forth in 37 C.F.R. § 42.24(c)(4). This word count was prepared by the word-processing program used to prepare this paper (Microsoft Word).

Dated: May 12, 2026

/s/ William A. Meunier

William A. Meunier (Reg. No. 41,193)

CERTIFICATE OF SERVICE

I certify that a copy of this PATENT OWNER'S SUR-REPLY is being served
by electronic mail on the following counsel of record:

Lead Counsel

J. Preston Long
(Reg. No. 65,125)
FINNEGAN, HENDERSON,
FARABOW, GARRETT & DUNNER,
LLP
901 New York Ave. N.W.
Washington, DC 20001
Telephone: (202) 408-4347
jp.long@finnegan.com
TSMC-MSL-IPR@finnegan.com

Backup Counsel

Aiden Skoyles
(Reg. No. 61,119)
FINNEGAN, HENDERSON,
FARABOW, GARRETT & DUNNER,
LLP
1875 Explorer St. Suite 800,
Reston, VA 20190
Telephone: (571) 203-2319
aidan.skoyles@finnegan.com

Carlos E. Duarte-Guevera
(Reg. No. 80,559)
FINNEGAN, HENDERSON,
FARABOW, GARRETT & DUNNER,
LLP
901 New York Ave. N.W.
Washington, DC 20001
Telephone: (202) 408-6013
carlos.duarte-guevara@finnegan.com

W. Karl Renner
(Reg. No. 41,265)
Thomas A. Rozylowicz
(Reg. No. 50,620)
FISH & RICHARDSON P.C.
60 South Sixth Street,
Suite 3200
Minneapolis, MN 55402
Telephone: (612) 335-5070
PTABInbound@fr.com

Minseung Ahn
(Reg. No. 76,611)
FISH & RICHARDSON P.C.
1000 Maine Ave., S.W., Suite 1000
Washington, DC 20024
Telephone: (202) 783-5070
PTABInbound@fr.com

Dated: May 12, 2026

/s/ William A. Meunier

William A. Meunier (Reg. No. 41,193)