

**Marlin
Semiconductor
Ltd.**

Marlin Semiconductor Limited Hearing Demonstratives

IPR2025-00847 – U.S. Patent No.7,745,847 B2

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Summary Of Arguments

1

Claim 1: “Raised Epitaxial Layers” (All Grounds)

- The asserted references form epitaxial layers “in” a recess and do not describe “raised epitaxial layers” above a surface
- The Petition improperly relies on non-scale patent drawings to cure this failure — wrong as a matter of law.

2

Claim 1: “Epitaxial Layers Positioned . . . Next To The Relative Sides Of The Gate”

Grounds 4A/4B: Chen’s epitaxial layers are under the gate, not next to the relative sides

3

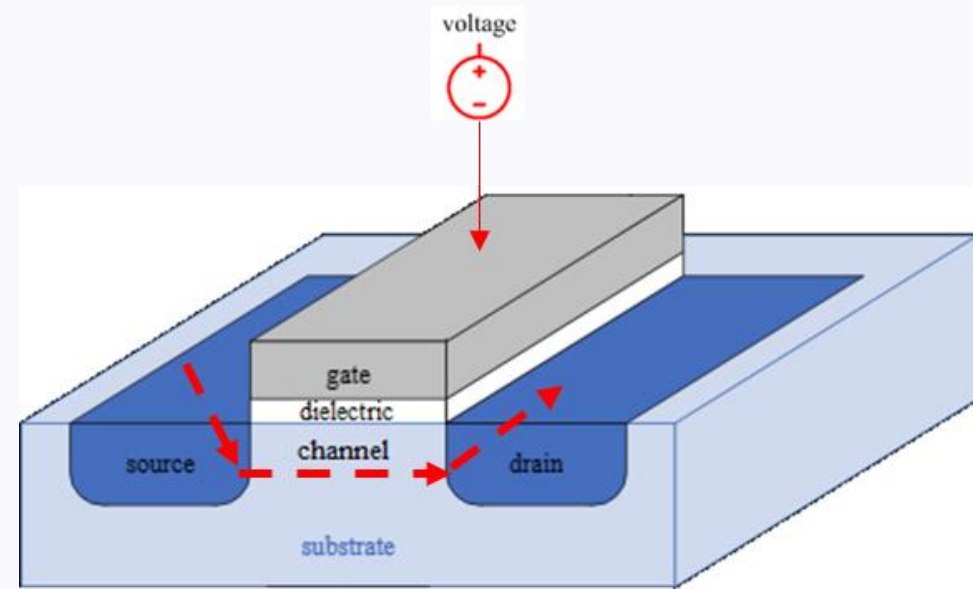
Claim 2: “Cap Layer”

None of the grounds discloses or renders obvious a gate “cap layer” because all references explicitly remove the cap layer.

Basic Transistor Components

Field Effect Transistors (FETs)

- Transistor built on semiconductor substrate and comprises a source, drain, gate, and channel. POR at 3-4 (citing EX2002 at 510-511).
- In this simplified version of a FET, there is a dielectric between the channel and gate. POR at 4 (citing EX2002 at 510-511; EX2003 ¶20).
- When a voltage is applied to the gate, the applied voltage results in the creation of a “field effect” in the channel. POR at 4-5 (citing EX2002 at 510-511; EX2003 ¶22).
- The field effect allows charge to flow from the source to the drain through the channel. POR at 5 (citing EX2003 ¶23).
- Selectively applying voltage to the gate switches the transistor on and off. POR at 4 (citing EX2002 at 510-511; EX2003 ¶20).



POR at 5 (citing EX2003, ¶23)

Manufacturing Stages: Wafer Fabrication

- Four stages of transistor manufacturing process: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. POR at 7-8 (citing EX2003, ¶129).
- Third stage, wafer fabrication, is the most relevant stage here. POR at 8 (citing EX2002 at 14; EX2003, ¶134).
- In wafer fabrication stage, steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). POR at 8-9 (citing EX2002 at 29-31, 71; EX2003, ¶134).
- Layering and patterning are two most important basic operations in wafer fabrication stage, and the most relevant here. POR at 9 (citing EX2003, ¶134).

Wafer Fabrication: Layering

Layering

- Operation used to add thin layers to the semiconductor substrate. POR at 9 (citing EX2002 at 72; EX2003, ¶135).
- One way of adding a layer is to directly deposit that material onto the substrate. POR at 9 (citing EX2003, ¶136).
- Another way is to grow the material on the substrate, such as through epitaxial growth. POR at 9 (citing EX2003, ¶136).
- Transistor structure to the right shows different layers that have been added through deposition or growth. POR at 9 (citing EX2002 at 72; EX2003, ¶136).

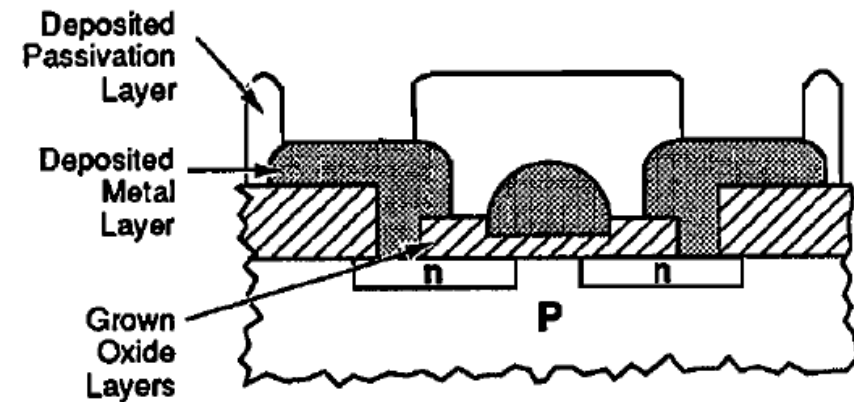


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

POR at 10 (citing EX2002 at 72; EX2003, ¶136)

Wafer Fabrication: Patterning

Patterning

- Steps to remove (etch away) selected portions of the semiconductor substrate or layers of materials. POR at 10 (citing EX2002 at 72-73; EX2003, ¶37).
- Patterning may result in holes in layered material or islands of material, as illustrated below. POR at 10 (citing EX2002 at 72-73; EX2003, ¶38).

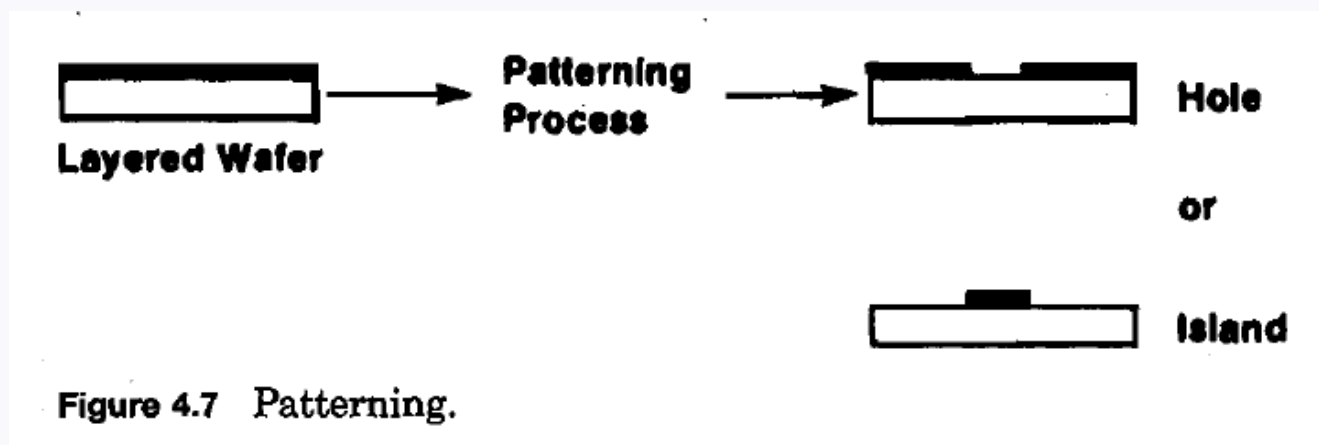


Figure 4.7 Patterning.

POR at 10 (citing EX2003, ¶38)

The '847 Patent's Innovations

Problem Solved

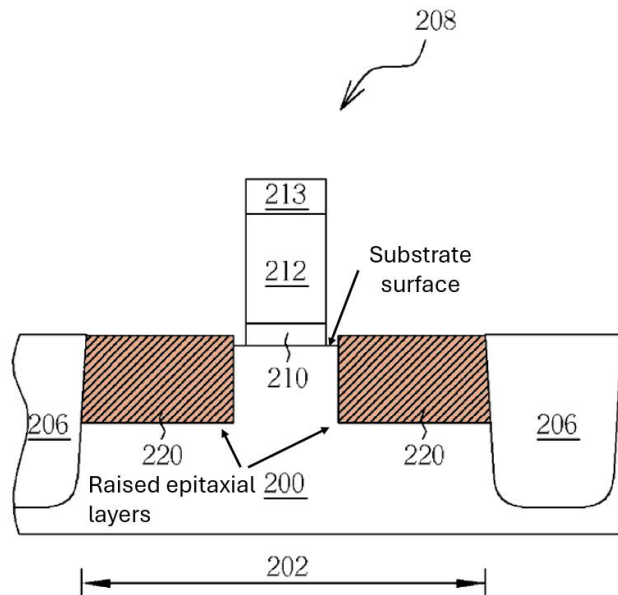
- In strained channel MOS transistors, “biaxial tensile strain occurs in the epitaxial silicon layer . . . And as a result, the band structure alters, and the carrier mobility increases,” which “enhances the speed performance” ’847 Patent, 1:36-40.
- Patent discloses “a method of fabricating strained silicon channel MOS transistors to improve the shortages from the prior art, and then increase the carrier mobility of MOS transistors.” ’847 Patent, 1:49-52.

Key Innovations

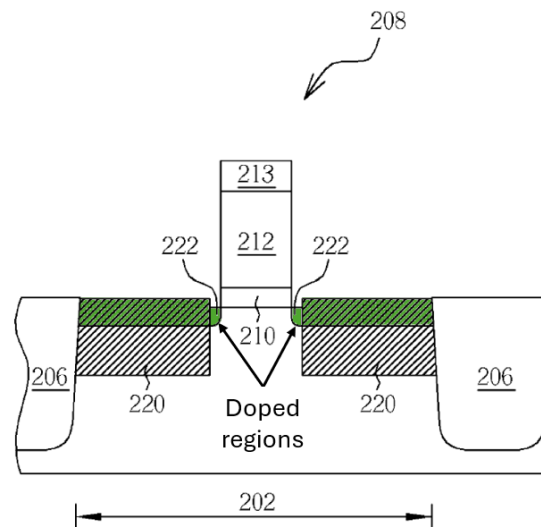
- Forming raised epitaxial layers before forming the spacers
 - “Since the characteristic of the present invention is to form the epitaxial layer before forming the spacer, thus the **distance between the gate and the epitaxial layer is not longer limited by the width of the spacer**. Besides, the process of etching the recess is carried out before forming the spacer. At this moment, the pattern density of the semiconductor substrate is lower than the time when the spacer is formed, **thus the microloading effect caused by the pattern density can be reduced, and then the uniformity in etching the recess is increased.**” ’847 Patent, 6:65-7:6
- Novel structural result: “a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and **a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate.**” ’847 patent, claim 1. POR at 12.

The '847 Patent's Innovations

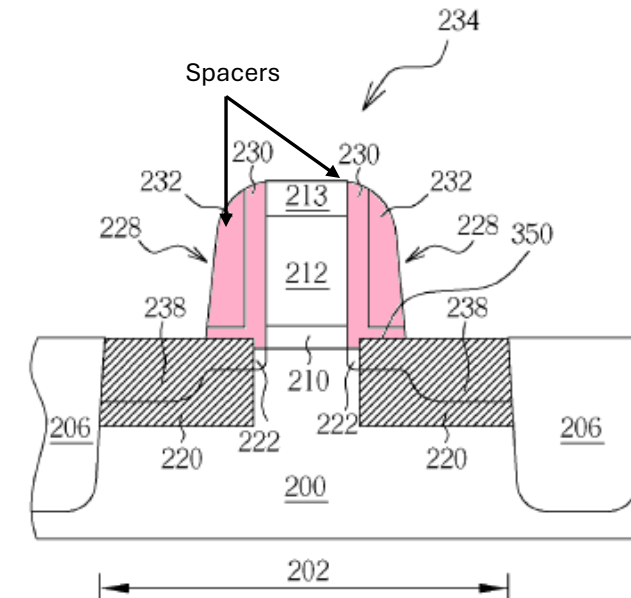
Raised epitaxial layers 220 formed before formation of spacers 230:



'847 Patent, Fig. 3 (partial and annotated)



'847 Patent, Fig. 4 (partial and annotated)



'847 Patent, Fig. 5 (partial and annotated)

Overview Of Petitioner's Grounds

Ground	Claims	Basis	Reference(s)
1A	1, 3–9, 11	§ 102	Lan
1B	1, 3–9, 11	§ 103	Lan
1C	2	§ 103	Lan
1D	2	§ 103	Lan + Liaw
2A	1, 3–11	§ 102	Wang407
2B	1, 3–11	§ 103	Wang407
3A	1, 10	§ 102	Wang753
3B	1, 10	§ 103	Wang753
4A	1, 2, 7, 8	§ 102	Chen
4B	1, 2, 7, 8	§ 103	Chen

Petition at 1

All Grounds: Claim 1, “raised epitaxial layers”

The References Are Silent On "Raised" Epitaxial Layers

No Reference Describes Raised Epitaxial Layers

- None of Lan, Wang407, Wang753, or Chen mentions, describes, or concerns raised epitaxial layers. POR at 15-20.
- Each reference describes epitaxial layers formed in recesses — not grown above the substrate surface
- The Petition does not identify a single textual description of raised epitaxial layers

What The References Actually Describe:

- **Lan:** “form epitaxial layers in the recesses” EX1005 at 2:59-64.
- **Wang407:** “SiGe stressors...grown in recesses 26” EX1007 at 3:63-65, 4:4-7, 4:34-40.
- **Wang753:** “SiGe stressors epitaxially grown in recesses 116” EX1008 at 4:10-11, 4:14-17.
- **Chen:** “Deposit silicon germanium material...to fill the etched source region” EX1009 at 3:52-58, 5:9-10, 5:31-38.
- **In contrast, the '847 Patent** describes that “epitaxial layer 220 is grown in the recess 218 and may be grown higher than the surface of the semiconductor substrate 200, so as to form a raised epitaxial layer 220.” EX1001 at 3:35-38.

Reliance On Non-Scale Drawings Is Impermissible

Federal Circuit Authority:

- “Arguments based on drawings not explicitly made to scale in issued patents are unavailing” *Nystrom v. Trex Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005).

The References’ Drawings:

- None of the references states its drawings are to scale. POR at 21.
- Chen expressly refers to its drawings as “**simplified** cross-sectional view diagram of a method of fabricating.” POR at 21 (quoting EX1009 at 4:15-16).

Supporting Precedent:

- *Hockerson-Halberstadt, Inc. v. Avia Group Intern.*, 222 F.3d 951, 956 (Fed. Cir. 2000): Improper to rely on drawings to establish “quantitative relationship” between elements
- *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1351 (Fed. Cir. 2013): Figures in a drawings are not evidence of actual proportions when drawings are not to scale
- *In re Wright*, 569 F.2d 1124 (C.C.P.A. 1977): Absent written description, arguments based on measurement of a drawing are of little value

Petitioner's Cited *Regents* Case

Petitioner's Own Citation Backfires:

- The Petition cites only a single non-precedential decision as supposedly supporting their attempt to rely on non-scale drawings. Pet. at 21 (citing *Regents of Univ. of Cal. v. Satco Prods., Inc.*, 2024 WL 4972639 (Fed. Cir. Dec. 4, 2024)).
- *Regents* rejects Board's use of drawings to establish relative size. POR at 23.
- Federal Circuit found the Board committed legal error by relying on patent drawings to establish the relative size of elements because "nothing in the [reference] indicates that its figures are drawn to scale." *Regents of Univ. of Cal. v. Satco Prods., Inc.*, 2024 WL 4972639, at *8-12 (Fed. Cir. Dec. 4, 2024).
- "[I]t is well established, however, that patent drawings do not define the precise proportions of elements and may not be relied on to show particular sizes if the specification is completely silent on the issue. In other words, figures in a patent are not drawn to scale unless otherwise indicated. **Arguments based on drawings not explicitly made to scale in issued patents are thus unavailing.**" *Regents*, 2024 WL 4972639, at *3.

Petitioner's Argument Relies On Precise Proportions Deduced From Drawings

Petitioner's Position (Reply at 2-3):

- Petitioner argues it uses figures only for “general shapes and relative sizes,” rather than “precise proportions”: “The Petition’s use of drawings to show the spatial relations between epitaxial source/drain regions and the substrate surface is thus permissible.” Reply at 3.

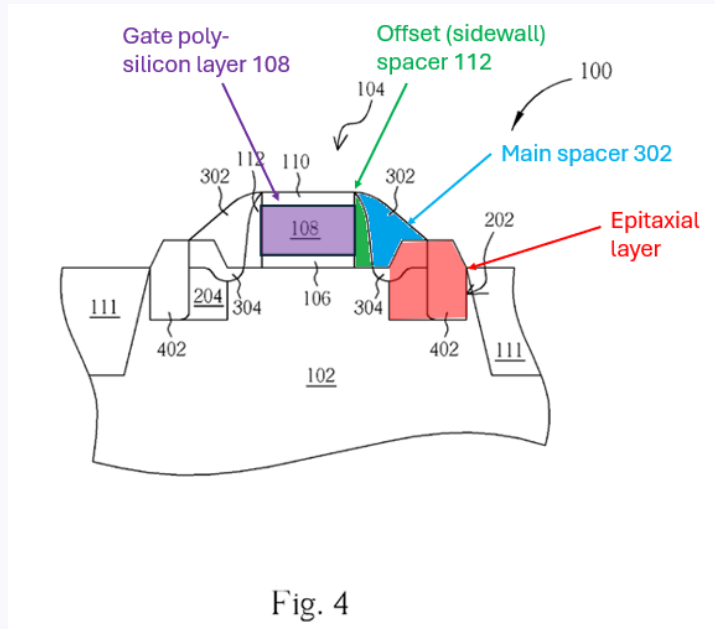
Petitioner Is Incorrect:

- Whether epitaxial layers are raised above the substrate surface is a precise proportion. Sur-reply at 3-7.
- Further, here, the text of the references contradicts the drawings — all describe epitaxial layer merely filling or grown in recesses. POR at 24-25.

Petitioner Argues A Similar Inference From Patent Owner Improperly Relies On Precise Proportions From A Drawing

POR at 39-40:

“As shown below, Lan’s design differs from Liaw’s in that in addition to sidewall spacers 112, Lan’s design also includes **a “main spacer 302” that covers half of the epitaxial layer that comprises the source/drain (402):**



EX-1005-Lan, Fig. 4 (annotated).

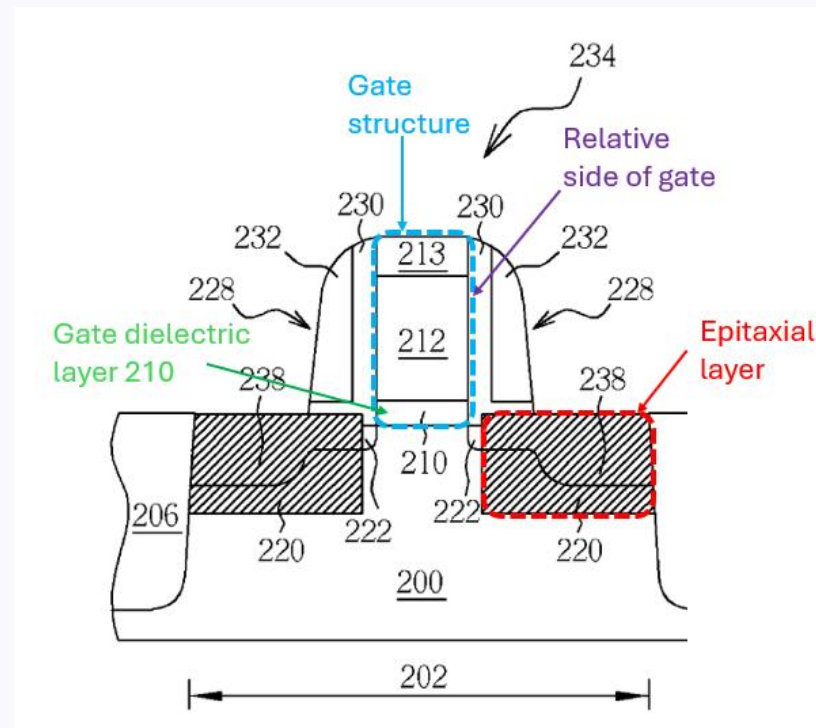
Petitioner’s Reply at 18-19:

“Second, Marlin incorrectly contends that Lan’s spacers appear ‘very wide’ compared to Liaw’s, such that Lan would not benefit from Liaw. (POR at 39.) But as Marlin’s expert admits, neither Lan nor Liaw discloses any spacer dimensions that would permit such a comparison. (See Ex-1204 at 86:22-87:5, 87:11-18). **Marlin thus attempts to use non-scale drawings for an impermissible purpose: extracting ‘precise proportions’ and ‘particular sizes.’** *Hockerson-Halberstadt*, 222 F.3d at 956; see also *supra* Section II (discussing permissible and impermissible uses of drawings).”

Ground 4 (Chen): Claim 1, “Epitaxial Layers Positioned . . . *Next To* The Relative Sides Of The Gate”

Limitation [1.b]

Claim language: “two raised epitaxial layers positioned respectively in the semiconductor substrate ***next to the relative sides of the gate***”

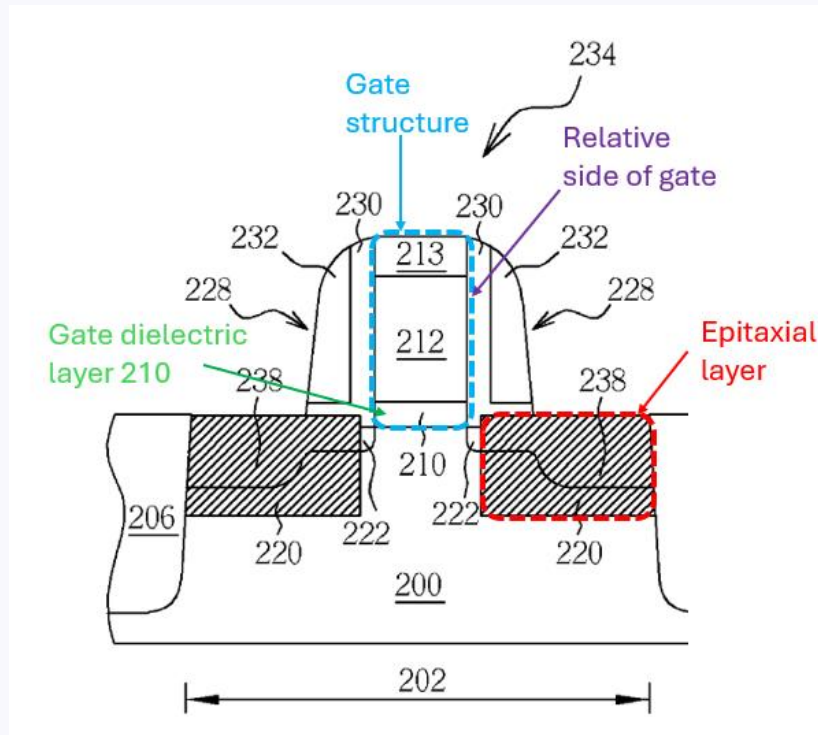


'847 Patent, Fig. 5 (partial and annotated)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

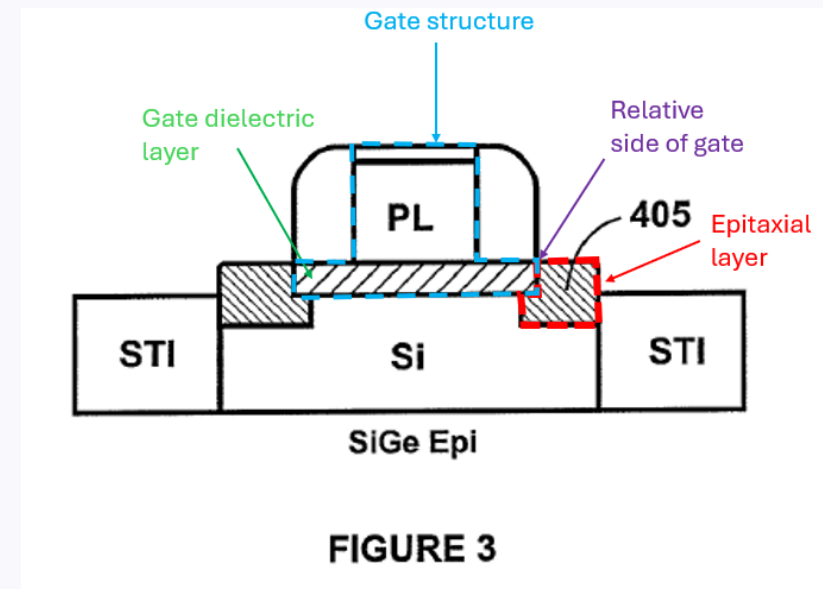
Ground 4: Chen’s Epitaxial Layers Not “Next To” Gate

'847 Patent: Epitaxial Layer “Next To” Relative Side of Gate:



'847 Patent, Fig. 5 (partial and annotated)

Chen: Epitaxial Layer Under Relative Side of Gate:



EX1009-Chen, Fig. 3 (annotated)

Ground 4: Chen's Epitaxial Layers Not "Next To" Gate

Chen's Process Sequence:

- Gate dielectric layer 107 and sidewall spacers 113 formed **before** etching recesses. POR at 27-28 (citing EX1009, Fig. 1, 4:30-59; EX2003, ¶45).
- Recesses are etched under the gate dielectric. POR at 28-29 (citing EX1009, Fig. 2; EX2003, ¶46).
- Gate dielectric layer (and thus the gate) extends to edges of spacers. POR at 29 (citing EX2003, ¶47).

Result:

- Epitaxial layer formed in recess is **under** the gate dielectric layer. POR at 29 (citing EX2003, ¶49).
- Not "next to the relative sides of the gate" as claimed. POR at 29 (citing EX2003, ¶49).

Design Consequence:

- Chen's design increases short-circuit risk. POR at 30 (citing EX2003, ¶51).
- The '847 Patent's process avoids this by forming epitaxial layers beside the gate. POR at 30 (citing EX2003, ¶51).

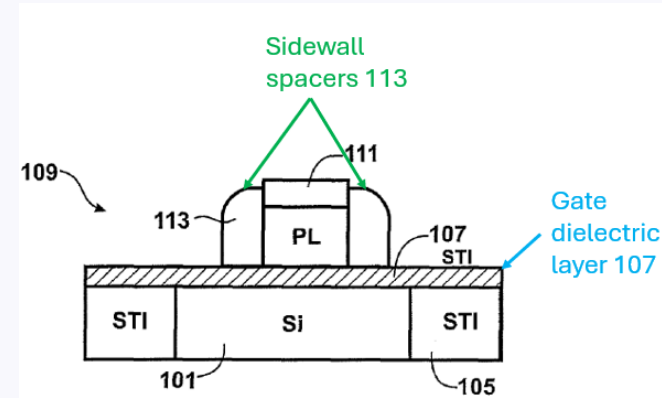


FIGURE 1

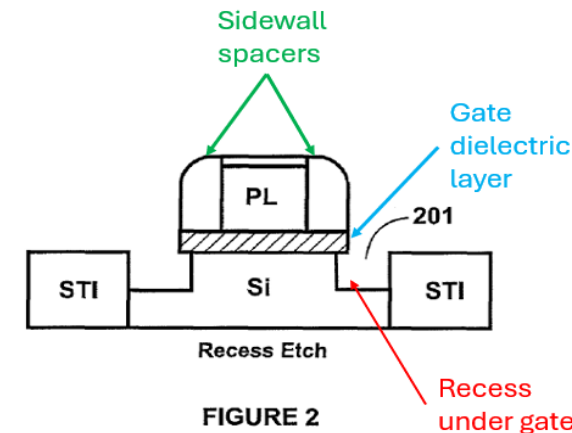


FIGURE 2

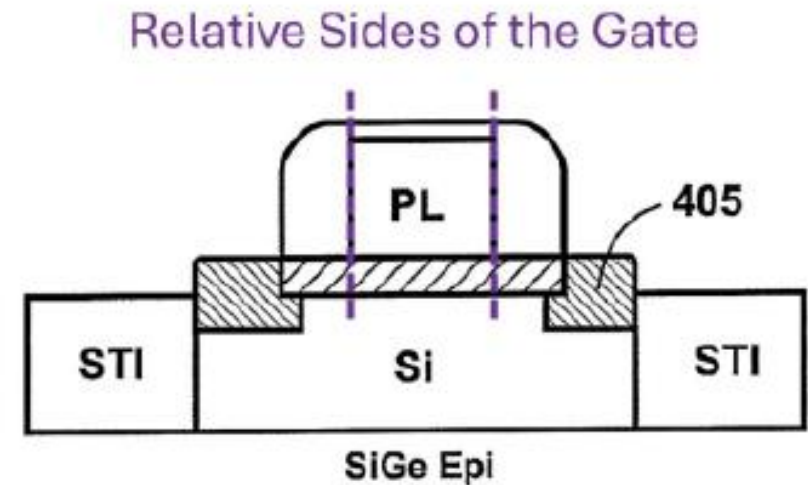
POR at 28
(EX1009-
Chen, Fig. 1
(annotated))

POR at 28
(EX1009-
Chen, Fig. 2
(annotated))

Petitioner's "Next To" Arguments

Petitioner's Two Arguments:

1. "Next to" means at least partially next to. Reply at 8 (arguing that the phrase "next to the relative sides of the gate" does not "require[] the epitaxial layers to be entirely next to the relative sides of the gate").
2. "Relative sides of the gate" means only the gate conductive layer's sides and does not include the gate dielectric on the sides. Reply at 10-11 ("[T]he plain meaning of 'the relative sides of the gate' encompasses the relative sides of the gate conductive layer.").



Chen, FIG. 3 (annotated)

Petitioner's Reply at 11.

Petitioner's "Next To" Arguments

Petitioner's argument that "relative sides of the gate" does not include the gate dielectric:

"Relative sides of the gate" means only the gate conductive layer's sides and does not include the gate dielectric on the sides. Reply at 10-11 ("[T]he plain meaning of 'the relative sides of the gate' encompasses the relative sides of the gate conductive layer.").

Response: The Gate Dielectric Is Part Of The Gate:

- The '847 Patent explains that "[e]ach gate 208 comprises a dielectric layer 210, a conductive layer 212 positioned on the dielectric layer 210 and a cap layer 213 positioned on the conductive layer 212." '847 Patent, 3:3-6.
- The gate dielectric layer **is** part of the gate — Petitioner concedes this. Pet. at 71 ("Accordingly, Chen discloses a gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask)...").
- Petitioner also concedes that "next to the relative sides of the gate" refers to the entire gate stack: "Accordingly, Chen discloses (Ground 4A), and at least renders obvious (Ground 4B), two raised epitaxial layers (silicon germanium material 405) positioned respectively in the semiconductor substrate (semiconductor substrate 101) **next to the relative sides of the gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask)** and above the surface of the semiconductor substrate." Pet., 72 (emphasis added)

Petitioner's "Next To" Arguments

Petitioner's Implicit Construction Argument:

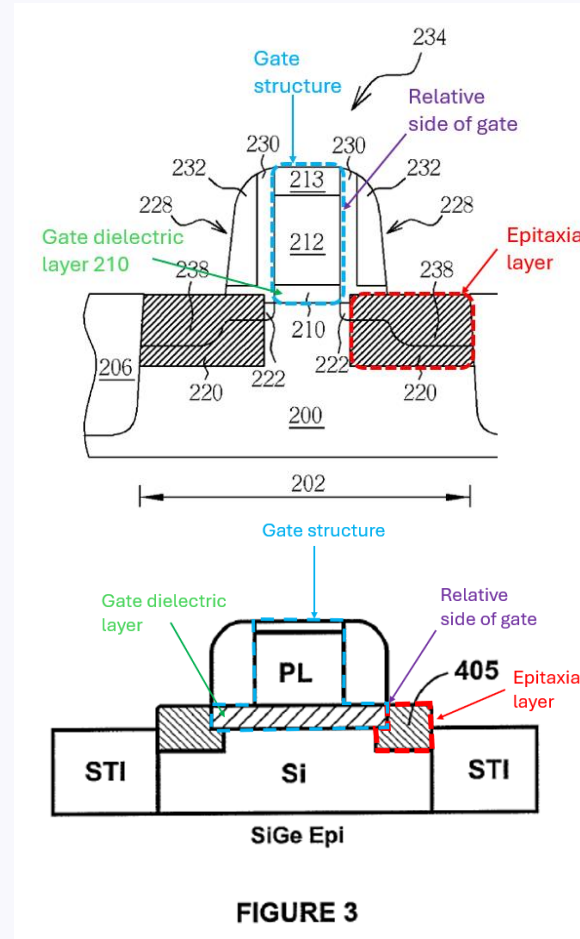
- Petitioner argues the plain meaning of "next to" means partially next to the gate. Reply at 8 (arguing that the phrase "next to the relative sides of the gate" does not "require[] the epitaxial layers to be entirely next to the relative sides of the gate").

This is an improper late construction that lacks support or analysis:

- In essence, Petitioner advocates for a belated construction that "next to" means "at least partially next to" on Reply. Sur-reply at 11
- This is entirely conclusory—Petitioner advances no evidence or justification for this belated construction. See Reply at 7-8.

In Chen, the "relative sides of the gate" are defined by the dielectric layer:

- In Chen, gate dielectric extends past gate conductive layer as shown by Chen's Figure 5. Sur-reply at 9-10.
- Petitioner concedes that "next to the relative sides of the gate" refers to the entire gate stack: "Accordingly, Chen discloses ... two raised epitaxial layers (silicon germanium material 405) positioned respectively in the semiconductor substrate (semiconductor substrate 101) **next to the relative sides of the gate (gate stack comprising the gate dielectric layer, gate layer, and, optionally, the hard mask)** and above the surface of the semiconductor substrate." Pet., 72 (emphasis added)
- Thus, in Chen, "relative sides of the gate" are defined by the width of the dielectric layer. Sur-reply at 9-10.



'847 Patent, Fig. 5
(partial and annotated)

EX1009-Chen,
Fig. 3
(annotated)

All Grounds: Claim 2, “A MOS transistor structure, comprising . . . a cap layer”

Claim 2: The Cap Layer Requirement

Claim 2 Language (depends from Claim 1):

- “A MOS transistor structure, comprising . . . a cap layer, positioned on the conductive layer”

Grounds Challenging Claim 2:

- Ground 1C: Lan (obviousness)
- Ground 1D: Lan + Liaw (obviousness)
- Ground 2: not challenged
- Ground 3: not challenged
- Grounds 4A/4B: Chen (anticipation / obviousness)

The Fatal Problem For Petitioner:

- All above references remove the cap layer during processing. POR at 31-32, 37, 42-44.
- The claims require a finished MOS transistor structure with the cap layer present. POR at 32, 43.
- No reference discloses or renders obvious retaining the cap layer. POR at 31-45.
- Even if Liaw discloses retaining the cap layer, there is no motivation to combine with Lan

Ground 1C: Lan Does Not Disclose A Cap Layer

Petitioner's Concession:

- Ground 1C (Lan alone) is an obviousness-only ground — Petitioner concedes Lan does not disclose the cap layer

Lan's Cap Layers 912/918:

- Acknowledged by Petitioner to be removed during processing. Pet. at 36.
- Purpose of Lan's cap layer: "serve[s] as [an] etching mask[], so as to form recesses 202 in the substrate 102 of the two sides of the gate 104." POR at 32 (citing EX1005-Lan, 2:59-62).
- Once recesses are formed, the cap layer serves no further purpose and is removed. POR at 32 (citing EX2003, ¶157).

Claims Require A Finished Structure:

- Claims recite "A MOS transistor structure" — a completed device, not an intermediate processing step. POR at 32.
- At the finished-device stage, Lan does not have a cap layer. POR at 32.

Ground 1C: Petitioner's Obviousness Argument Fails

Petitioner's Theory:

If gate is metal (not polysilicon), no reason to remove cap (no salicide needed).
Pet. at 36 (“When Lan’s conductive layers 910 and 916 are metal, a POSITA would have found it obvious to retain cap layers 912 and 918 because performing a salicide process on metal gate conductors is unworkable and unnecessary.”).

Response:

- Petitioner’s theory has no explicit disclosure in Lan
- Also incorrect: a POSITA would still remove the cap layer even if gate is metal

3 Reasons A POSITA Would Still Remove The Cap Layer Even With Metal Gate:

1. Cap blocks access: Voltage must be applied to gate conductor; cap layer blocks contact — device is unworkable. POR at 33.
2. Metal diffusion benefits: POSITA would diffuse additional metal into gate to fine-tune work function and improve adhesion — requires cap removal. POR at 33-35.
3. Etchant selectivity: POSITA would select etchant that doesn’t attack the metal gate, so cap is unnecessary for protection. POR at 35-36.

Ground 1C: Petitioner's Obviousness Argument Fails

Reason #1 To Remove Cap Layer: Cap Blocks Access To Gate:

- Gate cap layer must be removed because otherwise, cap layer would block access to the gate conductive layer. POR at 33 (citing EX2003, ¶59)
- A voltage must be applied to the gate in order to allow charge to flow between the source and drain. Thus, for the transistor to operate, the gate conductive layer must be contacted. POR at 33 (citing EX2003, ¶59)
- Thus, Petition's proposed modification of Lan—retaining the cap layer—is unworkable because it would create a further problem of blocking access to the gate conductive layer. POR at 33 (citing EX2003, ¶59)
- The Petition offers no solution for how this problem would be resolved.

Expert Admission:

- Petitioner's own expert (Fitzgerald) admitted cap blocks access to gate conductive layer (Ex. 2004, 31:16-19):

16	Q	So ultimately, for the transistor to be
17		operational, you need to contact the gate to apply a
18		voltage to it, right?
19	A	Correct.

Ground 1C: Petitioner's Obviousness Argument Fails

Reason #2 To Remove Cap Layer: To Diffuse Additional Metal Onto Gate:

- Multiple reasons to remove the gate cap layer and to diffuse additional metal onto the gate even when the gate is metal. POR at 33 (citing EX2003, ¶60)
- Like a salicide process, diffusing an additional metal requires removal of the cap layer. POR at 34 (citing EX2003, ¶60)
- For example, the metal of a contact plug is often a different metal from the gate metal. POR at 34 (citing EX2003, ¶60; EX2004, 31:20-22)
- Interconnecting dissimilar metals leads to poor adhesion between the gate metal and the contact metal, as well as high-than-desired contact resistance between the two metals. POR at 34 (citing EX2003, ¶61)
- For example: tungsten is often used as a contact metal, while titanium may be more suitable for a gate due to its work function. POR at 34 (citing EX2003, ¶61; EX2004, 29:4-21, 42:19-43:13)
- Thus, a POSITA would have known that it would be beneficial to diffuse an additional metal, such as nickel into a gate before connecting the metal contact. POR at 34 (citing EX2003, ¶61; EX2004, 29:4-21, 42:19-43:13)

Ground 1C: Petitioner's Obviousness Argument Fails

Reason #2 To Remove Cap Layer: To Diffuse Additional Metal Onto Gate:

- Thus, a POSITA would have known that it would be beneficial to diffuse an additional metal, such as nickel into a gate before connecting the metal contact. POR at 34-35 (citing EX2003, ¶61; EX2004, 25:21-26:16, EX2005, 446)
- This would benefit the tunability of the work function which impacts the threshold voltage of a transistor, which is a key factor in transistor design. POR at 35 (citing EX2003, ¶61; EX2004, 42:3-43:13)

Petitioner's Expert agreed that a POSITA could diffuse one metal into another in the gate to adjust the work function:

4 Q And one way you could do that to adjust the work
5 function would be to diffuse one metal into another in the
6 gate; is that right?
7 A I am not familiar with that in this time period.
8 That's why I mentioned the titanium aluminum nitride.
9 They put aluminum inside titanium nitride in order to
10 shift the work function, I believe for the -- for the
11 PMOS, but I'm not sure about that. But yeah, to change
12 the work function of one, either NMOS or the PMOS, for --
13 just what you said.

EX2004 (Fitzgerald Dep. Tr.) at 42:3-43:13

Ground 1C: Petitioner's Obviousness Argument Fails

Reason #2 To Remove Cap Layer: To Diffuse Additional Metal Onto Gate:

- Petitioner's expert admitted – TiN liner "would help with the connectivity" (EX2004 (Fitzgerald Dep. Tr.) at 33:11-34:23)

8	Q	Sorry, what sorts of liners are you talking
9		about?
10	A	So in a -- when you're trying to interconnect
11		transistors and you bring down metal, usually there's not
12		just the metal itself. You have a liner that is around
13		those contacts. And that liner also helps with the
14		connectivity between the interconnects and the -- whatever
15		the interconnect metals are and the -- and the underlying
16		contact.
17	Q	What is that liner made out of?
18	A	Changes with time, with different technologies.
19	Q	What sorts of materials have you seen the liner
20		being made out of?
21	A	Can't recall. But I think if I recall, there
22		might be... in the -- in the tungsten case, I think it was
23		titanium nitride.

Ground 1C: Petitioner's Obviousness Argument Fails

Reason #2 To Remove Cap Layer: To Diffuse Additional Metal Onto Gate:

- Petitioner's expert admitted – "people might do things like that" (diffuse metal onto metal gate to improve contact resistance) (EX2004 (Fitzgerald Dep. Tr.) at 34:24-35:24)

Q: [I]f you were going to diffuse a metal onto a metal gate before connecting the contact, could that improve the contact resistance that would otherwise exist between the contact and the metal gate?

A: If you have a clean interface and you have metal-metal, you would want to not have any thermal processing because it would add to the thermal budget of the entire process. So in general, people are trying to avoid that.

In the early days, like, you know, if you were in a research lab, there's all sorts of contamination and things like that, and it's very different from manufacturing. Manufacturing tries to remove all that over time to reduce mask levels and to keep thermal budget low.

But of course, if you have a problem there, then ***people might do things like that.***

Ground 1C: Petitioner's Obviousness Argument Fails

Reason #3 To Remove Cap Layer: Cap Is Unnecessary To Protect Against Etchant:

- The Petition argues that a POSITA would know that the cap layer on the gate is beneficial to retain because “if cap layers 912 and 918 were removed when forming silicide on source/drain regions 1206 and 1208, the metal gate layers 910 and 916 would be exposed to the etchant used to strip the unreacted silicidation metal, which could remove, corrode, or otherwise damage metal layers 910 and 916.” Pet. at 37 (internal citations omitted).
- This argument makes no sense, because a POSITA would have understood that an etchant would be selected that would not attack the metal gate. POR at 36 (citing EX2003, ¶62)
- Thus, retaining the cap layer is not necessary to protect the metal layers of the gate during a salicide process performed on the source/drain. POR at 36 (citing EX2003, ¶62)

Ground 1C: Petitioner's Obviousness Argument Fails

Reason #3 To Remove Cap Layer: Cap Is Unnecessary To Protect Against Etchant:

- Moreover, a POSITA would have understood that even if a small portion of the metal layer was removed by the etchant, this would not be an issue due to the large relative thickness of the gate as compared to the unreacted silicidation metal. POR at 36 (citing EX2003, ¶62; EX2004, 49:12-13)
- Petitioner's expert admitted – gate is "much thicker" than unreacted metal (EX2004, 49:12-23)

Petitioner's expert admitted that gate is "much thicker" than the unreacted metal:

12 Q And what about the relative thickness of the
13 unreacted metal versus the thickness of the gate? Is one
14 thicker than the other? Are they the same thickness?
15 A You mean when you do the silicide process I was
16 just talking about?
17 Q Yes.
18 A Typically, the gate thickness is greater than the
19 metal you put down.
20 Q Would you say it's a little bit thicker or much
21 thicker? Can you...
22 A I mean, you know, from a topological point of
23 view, usually it's much thicker.

EX2004 (Fitzgerald Dep. Tr.) at 49:12-23

Ground 1C: Petitioner's Obviousness Argument Fails

Conclusion:

- 3 Reasons A POSITA Would Still Remove The Cap Layer Even With Metal Gate:
 1. Cap blocks access: Voltage must be applied to gate conductor; cap layer blocks contact — device is unworkable. POR at 33.
 2. Metal diffusion benefits: POSITA would diffuse additional metal into gate to fine-tune work function and improve adhesion — requires cap removal. POR at 33-35.
 3. Etchant selectivity: POSITA would select etchant that doesn't attack the metal gate, so cap is unnecessary for protection. POR at 35-36.
- **Petition admits that Lan's fabrication method requires removing the gate cap layer and does not offer sufficient rationale for its proposed modification of instead retaining the cap layer. POR at 36-37 (citing EX2003. ¶63).**
- **Thus, Ground 1C fails to render obvious claim 2**

Ground 1D: Lan + Liaw Combination Fails

Liaw's Cap Layer Is Also Removed:

- “[T]he inter-level dielectric layer 320 and the cap layer 312 are etched through, down to the metal gate conductor 308, forming a gate contact opening (not shown).” EX1006-Liaw, 6:35-38.

No Motivation To Combine:

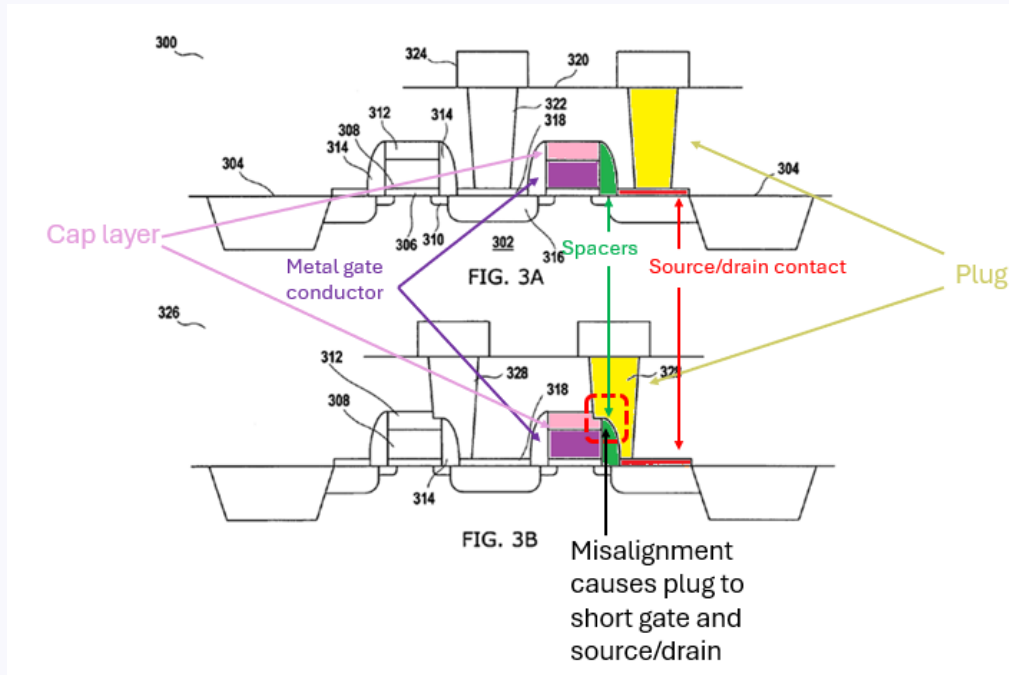
- Purpose of Liaw's cap layer is to mitigate issues with misaligned source/drain contact plugs. POR at 37-39; EX1006-Liaw at 5:61-62 (“[T]he cap layer 412 allows the MOS device 400 to tolerate a slight misalignment of the conductive plug 422.”).
- But Lan already has another superior form of misalignment mitigation, “main spacer 302,” which covers covering half the source/drain before contact formation. POR at 39-41.
- A POSITA would not add Liaw's cap layer to a structure that already solves the problem. POR at 41.

Liaw Itself Undermines The Combination:

- “While the cap layer 214 avoids the misalignment problem, it complicates the fabrication process and increases costs.” EX1006-Liaw, 3:47-49.
- No reason to complicate process and increase costs if the misalignment problem is already solved without cap layer, like in Lan. POR at 41.

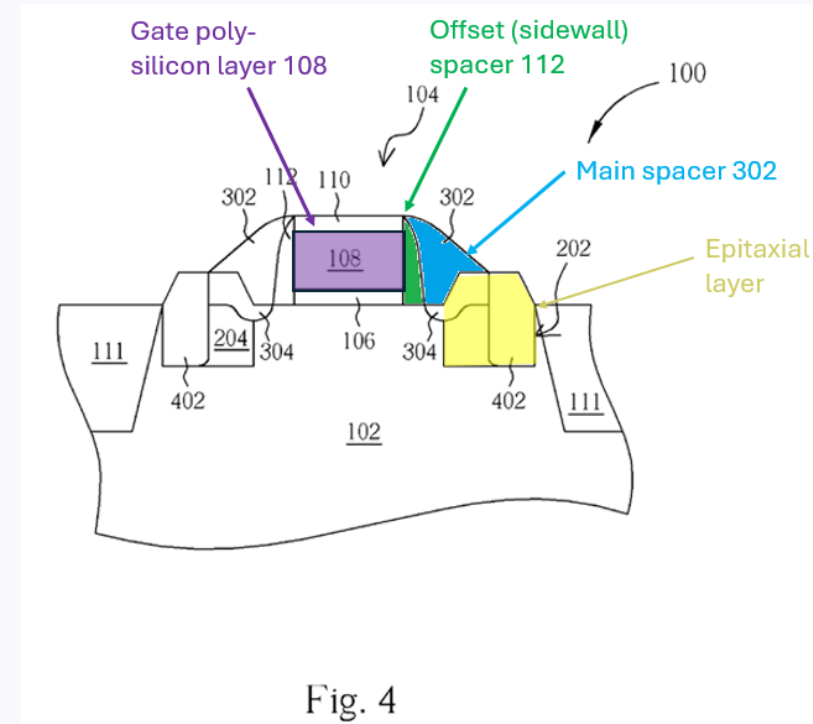
Ground 1D: Lan + Liaw Combination Fails

Liaw's cap layer is designed to solve misalignment problem:



EX1006-Liaw, Figs. 3A and 3B (annotated)

Lan's wide main spacer 302 already solves this problem:



EX1005-Lan, Fig. 4 (annotated)

Petitioner's Reply Arguments On Lan/Liaw

Petitioner argues Moore's Law means spacer widths would be comparable

- Reply at 19: “Moore's Law of device scaling means that Lan and Liaw are trying to fit their respective transistors within a comparable physical space, such that their total sidewall thicknesses would be similar.”
- This argument fails: When devices scale smaller, all components scale proportionally. Sur-reply at 15.
- Relative proportions remain constant regardless of absolute size. Sur-reply at 15.
- Lan's spacers will always cover a portion of epitaxial layers. Sur-reply at 15.

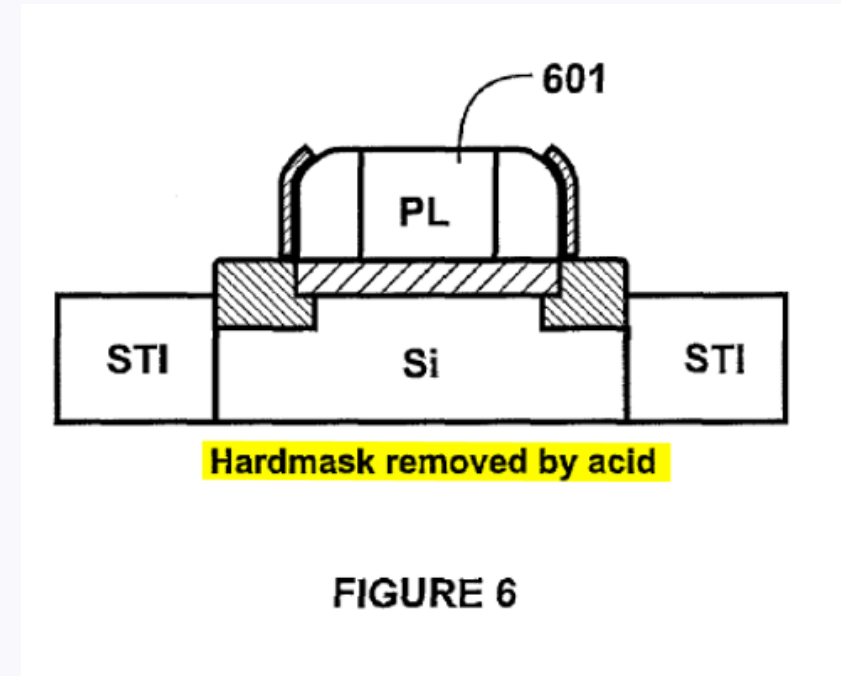
Bottom Line:

- Even under Petitioner's interpretation, the combination lacks motivation and teaches away from retaining the cap layer.

Grounds 4A/4B: Chen Explicitly Removes The Cap Layer

Chen's "Hard Mask 503" (Alleged Cap Layer) Is Removed

- Chen explicitly states: "the method removes the hard mask to expose 601 the top surface of the gate structures, as shown in FIG. 6." EX1009-Chen, 6:16-18.
- Step 11 of Chen's 12-step process: "[s]electively remove[s] the hard mask." EX1009-Chen, 3:40-4:4.
- Purpose: "The hard mask layer is deposited to a suitable thickness to protect the underlying gate structure during etching and deposition steps." EX1009-Chen, 4:46-48.



EX1009-Chen, Fig. 6 (annotated)

Grounds 4A/4B: Chen Explicitly Removes The Cap Layer

The Removal Is Not Optional:

- The paragraph (EX1009-Chen, 6:11-31) introducing Fig. 5 describes multiple subsequent required steps:
- Hard mask removal → Silicide formation → Interlayer dielectric → Electrical contacts
- None of these steps are described as optional

To finish the device according to an embodiment of the present invention, the method forms sidewall spacers 501 from the second protective layer, as illustrated by FIG. 5. The sidewall spacers exposes an upper portion 503 of the hard mask, while sealing regions on the edges of the gate layer. In a preferred embodiment, the method removes the hard mask to expose 601 the top surface of the gate structures, as shown in FIG. 6. Such gate structures are substantially free from any silicon germanium and/or silicon carbide bearing impurities. The gate structures are also substantially smooth and damage free. The method forms a silicide layer overlying gate layer and source/drain regions. Preferably, the silicide layer is a nickel bearing layer such as nickel silicide overlying the exposed source/drain regions and upper surface of the patterned gate layer. Other types of silicide layers can also be used. Such silicide layers include titanium silicide, tungsten silicide, nickel silicide, and the like. The method forms an interlayer dielectric layer overlying NMOS and PMOS transistor devices. The method then performs electrical contacts. Other steps include performing a back end processes and other steps, as desired.

Chen's Fig. 5 Is Not A "Finished Device"

Petitioner's Argument:

- Pet. at 80: "Chen thus makes clear that FIG. 5 represents a 'finish[ed] ... device,' wherein the hard mask remains part of the gate structure."

Petitioner's Expert Concession:

- Petitioner's own expert conceded: "the device in Figure 5 would not function as a transistor" (EX2004, 83:14-24)

Textual Evidence in Chen:

- The paragraph introducing Fig. 5 describes multiple **required** subsequent steps. EX1009-Chen, 6:16-18.
- List of steps in columns 1-2: Step 11: Remove hard mask; Step 12: Form silicide, ILD, and contacts. EX1009-Chen, 3:40-4:4.
- These are described as mandatory — not optional alternatives

Conclusion:

- Fig. 5 depicts an intermediate structure with a sacrificial hard mask, not a finished device with a cap layer. POR at 43-44.

Petitioner's Intermediate Structure Argument Fails

Petitioner Improperly Raises New Argument On Reply:

- Argues that Lan's and Chen's intermediate structure can anticipate. Reply at 21-22 ("Marlin's argument that those disclosed cap layers must be subsequently removed is not even legally sufficient to distinguish Lan or Chen.").
- But Petition did not even allege that Lan anticipates and specifically argued Chen's Fig. 5 showed a finished device. Pet. at 80 ("Chen thus makes clear that FIG. 5 represents a 'finish[ed] ... device,' wherein the hard mask remains part of the gate structure.").
- This is an improperly raised new argument on Reply. Sur-reply at 13-14.

Even If Considered, The Argument Fails:

- Claims recite "A MOS transistor structure" — structural product claim requiring all elements to coexist
- Thus, claim 2 requires a retained cap layer, rather than a sacrificial layer. Sur-reply at 13-14 (citing EX1001, 56:59, Fig. 14).

Critical Distinction:

- At the equivalent processing stage, the '847 Patent retains its cap layer
- Chen removes the cap layer as a required step
- The claimed MOS transistor structure never exists in Chen

Petitioner's Obviousness Arguments Regarding Chen Fail As Well

Petitioner's Argument (Pet., 81):

1. Hard mask would not be removed “[i]n device regions where silicide is unwanted on a polysilicon gate”
2. Hard mask would not be removed if Chen's conductive gate layer were made of metal, for the same reasons as alleged with respect to Ground 1C.

Petitioner's Arguments Are Incorrect:

1. As explained above, in Chen, the hard mask is removed, and the removal is not optional. Petitioner's rationale is baseless and purely hypothetical.
2. Incorrect for the same reasons as explained in connection with Ground 1C.

Mr. McAlexander's Testimony Is Credible

Petitioner's Attack:

Argues McAlexander "parrots the POR" and lacks relevant expertise. Reply at 24-27 ("The Board should afford Mr. McAlexander's testimony little weight. His opinions do not reflect independent technical analysis; they track the POR essentially verbatim. Moreover, Mr. McAlexander is a serial declarant who lacks specialized experience with the technologies at issue.").

Response:

- 54 years experience including MOSFETs — the very technology at issue (Ex. 1204 at 88:13-20; see *generally id.*)
- Consulted with STMicroelectronics on MOS designs from early 1990s to 2016 — directly coinciding with '847 Patent timeframe

Petitioner Fails To Dispute Key Technical Opinions (Sur-Reply at 16-17):

- Lan's main spacers already protect against misalignment (Ex. 2003 ¶¶67-69)
- Even with metal gate, cap/hard mask would be removed (Ex. 2003 ¶¶60-61)
- Gate metal unaffected by etchant due to relative thickness (Ex. 2003 ¶62)

Petitioner's Expert In Contrast:

- Fitzgerald's Bell Labs experience lasted only 6 years and ended in 1994: over a decade before the relevant time period. Sur-reply at 19 (citing EX1004 at 1).

Summary Of Key Points

1. All Grounds Fail On Raised Epitaxial Layers (All challenged claims)

- No reference describes raised epitaxial layers; reliance on non-scale drawings is legally impermissible and factually unsupported

2. Chen Grounds Additionally Fail On "Next To"(All challenged claims)

- Chen's epitaxial layers are under the gate, not next to the relative sides of the gate

3. All Grounds Fail On "Cap Layer" (Claim 2)

- All references explicitly remove the cap layer
- Petitioner's proposed modifications are unworkable and lack motivation
- Petitioner's own expert conceded Chen's Fig. 5 would not function as a transistor

Conclusion

The Board Should Find Claims 1–11 Patentable

- The challenged claims are not anticipated by any of the asserted references
- The challenged claims are not rendered obvious by any of the asserted grounds

Specific Findings Requested:

- No reference discloses raised epitaxial layers above the substrate surface and reliance on non-scale patent drawings cannot establish this element
- Chen's epitaxial layers are not next to the relative sides
- No ground discloses or renders obvious a retained cap layer in the finished structure
- The Lan + Liaw combination lacks motivation to combine