

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Chun-Hao Lin
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP3064USA

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8502316		2013-08-06	Fung et al.	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20140027820		2014-01-30	Aquilino et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	

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	1		
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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	First Named Inventor	Chun-Hao Lin
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP3064USA

CERTIFICATION STATEMENT			
Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):			
☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).			
OR			
☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).			
☐ See attached certification statement.			
☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.			
☒ None			
SIGNATURE			
A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.			
Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2017-07-26
Name/Print	Winston Hsu	Registration Number	41526

Doc Code: ECOMM.AUTH/ECOMM.WTDW

Doc Description: Internet Communications Authorized/Internet Communications Authorization Withdrawn

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS	Application No.	N/A
	Filing Date	N/A
	First Named Inventor	Chun-Hao Lin
	Art Unit	N/A
	Examiner Name	N/A
	Practitioner Docket No.	NAUP3064USA

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

☒ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☒ attorney or agent of record. Registration number 41526.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

Signature

Date

Typed or printed name

Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

As the below named inventor, I hereby declare that:
This declaration is directed to:

☒ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUL 21 2017 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP3064USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chun-Hao Lin**

Date: JUL 21 2017

Signature: Chun-Hao Lin

NPO#NAU-P3064-USA:0
CUST#UMCD-2017-0163

Page 2 of 6

F#NPO-P0002E-US1201
DSB0-106U012698

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
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☒ The attached application, or

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I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUL 21 2017 (Date of signing)

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Docket No NAUP3064USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Hsin-Yu Chen**

Date: JUL 21 2017

Signature: Hsin Yu Chen

NPO#NAU-P3064-USA:0
CUST#UMCD-2017-0163

Page 4 of 6

F#NPO-P0002E-US1201
DSB0-106U012698

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
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SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

As the below named inventor, I hereby declare that:
This declaration is directed to:

☒ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

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(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUL 21 2017 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP3064USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Shou-Wei Hsieh**

Date: JUL 21 2017

Signature: Shou-Wei Hsieh

NPO#NAU-P3064-USA:0
CUST#UMCD-2017-0163

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F#NPO-P0002E-US1201
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Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	N/A		
Filing Date	N/A		
First Named Inventor	Chun-Hao Lin		
Title	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
Art Unit	N/A		
Examiner Name	N/A		
Attorney Docket Number	NAUP3064USA		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/Winston Hsu/	Date (Optional)	07/26/2017
Name	Winston Hsu	Registration Number	41526
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
☐ *Total of _____ forms are submitted.			

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B (07-13)

Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

OR

27765

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone			Email		

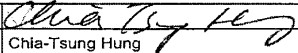
I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

UNITED MICROELECTRONICS CORP.

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	MAY 12 2015
Name	Chia-Tsung Hung		
Title	CHAIRMAN		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

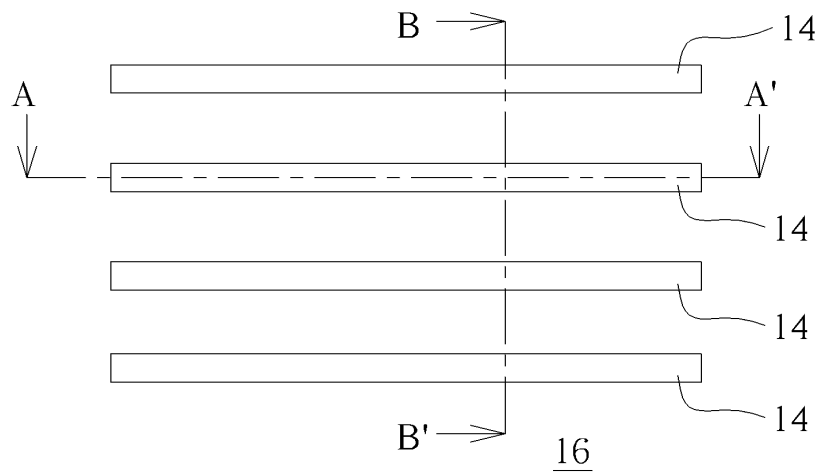


FIG. 1

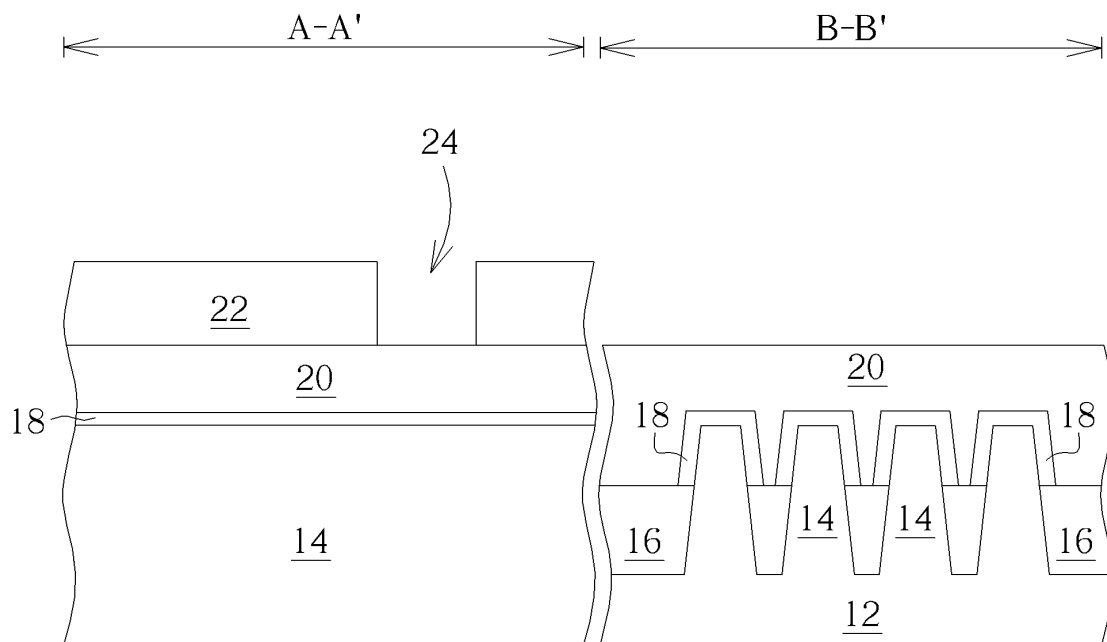


FIG. 2

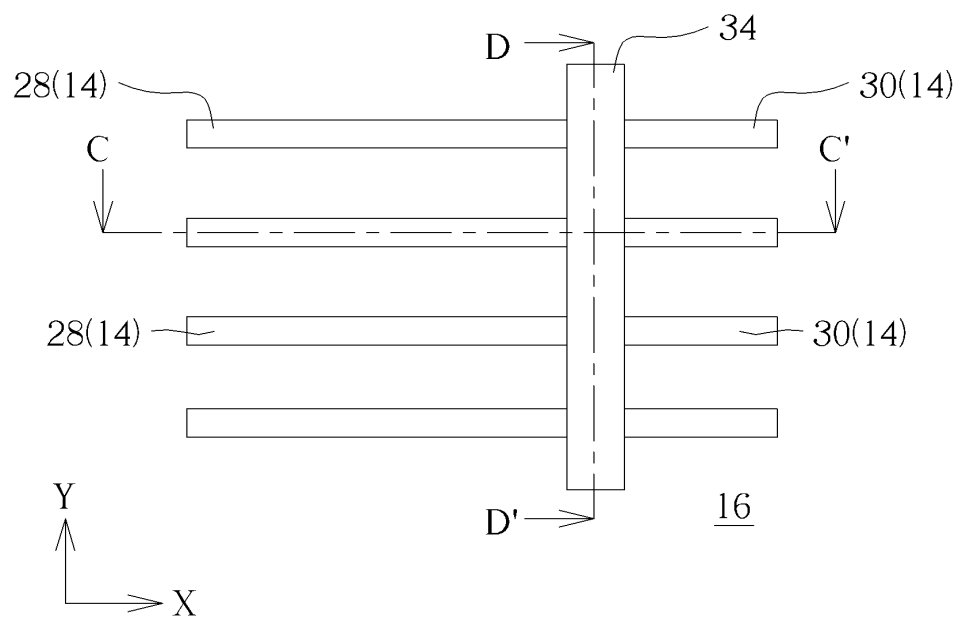


FIG. 5

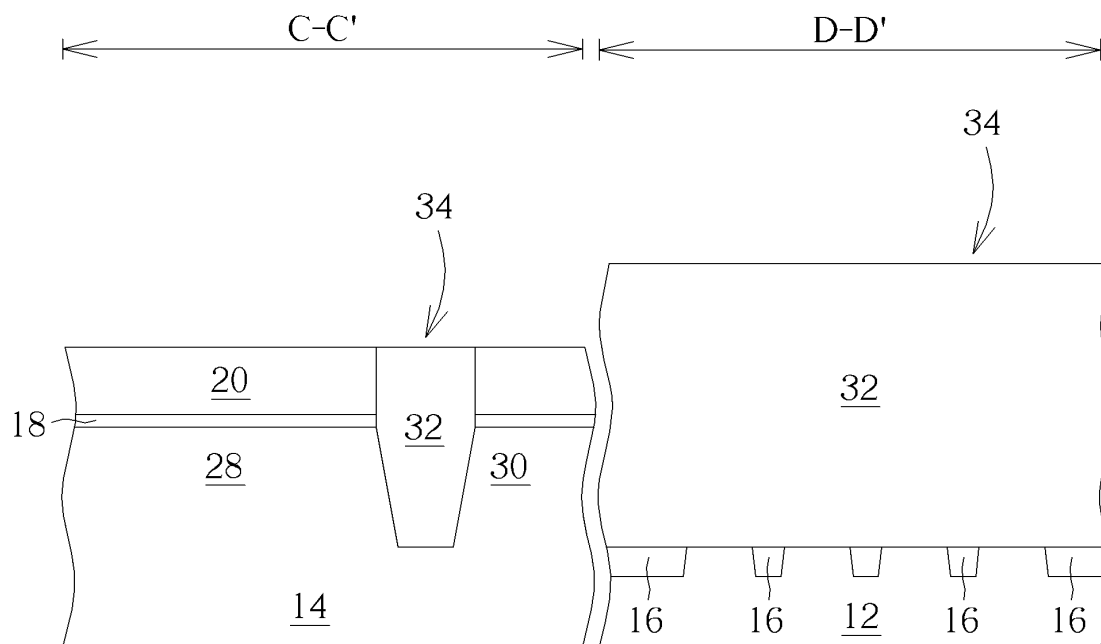


FIG. 6

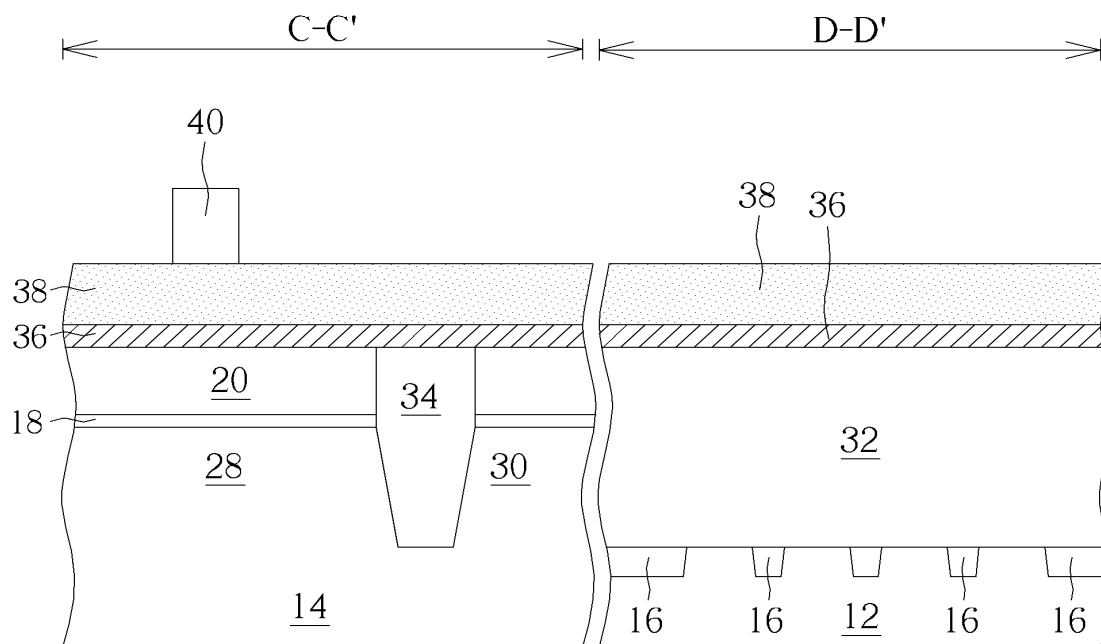


FIG. 7

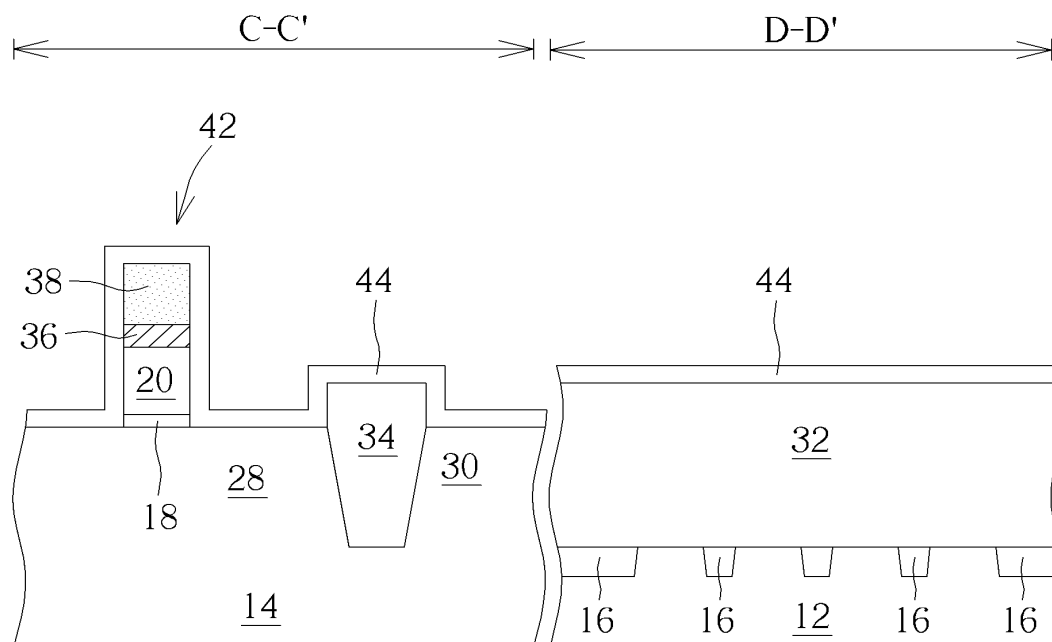


FIG. 8

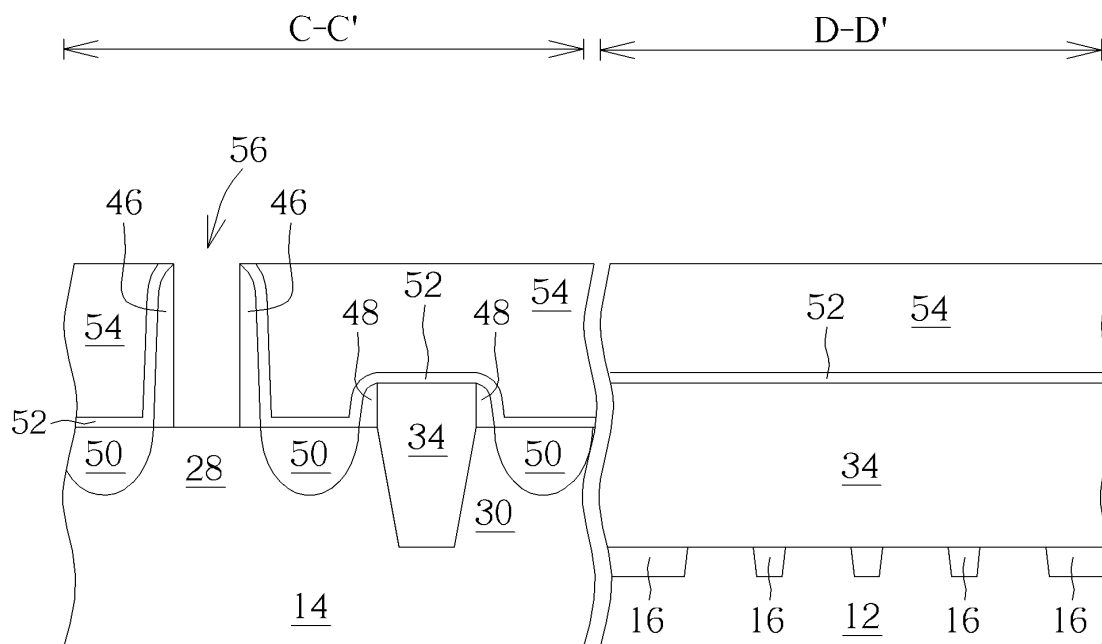


FIG. 9

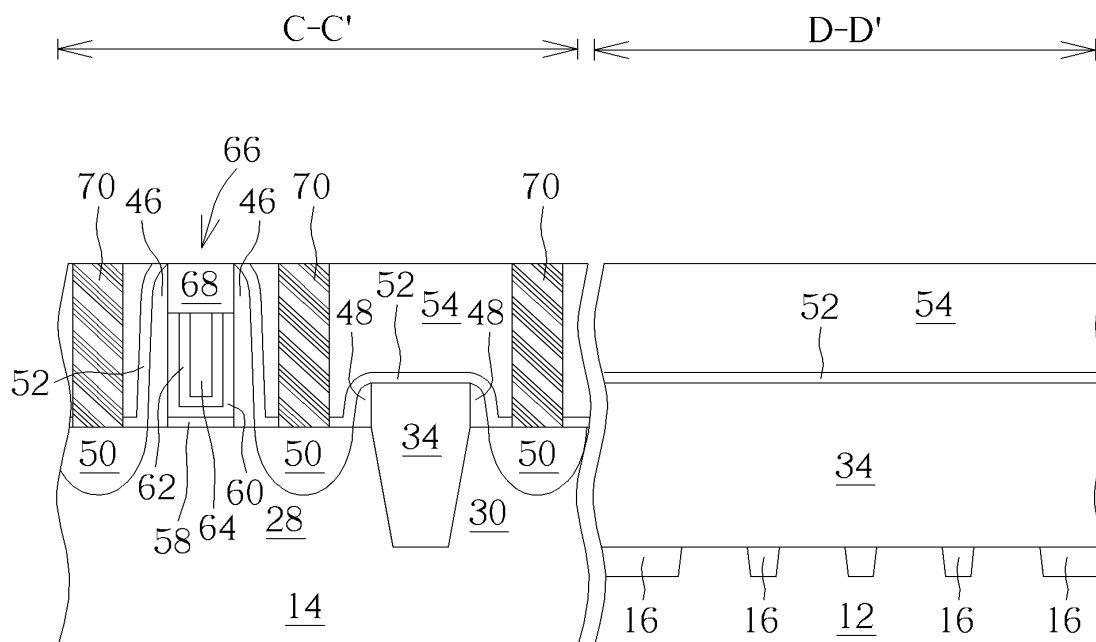


FIG. 10

Abstract of Disclosure

A method for fabricating semiconductor device includes the steps of: forming a fin-shaped structure on a substrate; forming a shallow trench isolation (STI) around the fin-shaped structure; forming a gate layer on the fin-shaped structure and the STI; removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench; and forming a dielectric layer into the trench to form a single diffusion break (SDB) structure.

Claims

What is claimed is:

1. A method for fabricating semiconductor device, comprising:
 - forming a fin-shaped structure on a substrate;
 - forming a shallow trench isolation (STI) around the fin-shaped structure;
 - forming a gate layer on the fin-shaped structure and the STI;
 - removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench; and
 - forming a dielectric layer into the trench to form a single diffusion break (SDB) structure.
2. The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.
3. The method of claim 2, further comprising:
 - forming a patterned mask on the gate layer; and
 - using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.
4. The method of claim 1, further comprising:
 - forming the dielectric layer into the trench and on the gate layer;
 - and
 - planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.
5. The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure.
6. The method of claim 5, further comprising:
 - forming a cap layer on the gate structure and the SDB structure;
 - and

removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer adjacent to the SDB structure.

7. The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.

8. The method of claim 7, wherein the first direction is orthogonal to the second direction.

9. The method of claim 1, wherein the gate layer comprises amorphous silicon.

10. The method of claim 1, wherein the gate layer comprises polysilicon.

11. The method of claim 1, wherein the dielectric layer comprises silicon nitride.

12. The method of claim 1, wherein the dielectric layer comprises silicon oxide.

13. A semiconductor device, comprising:

- a fin-shaped structure on a substrate;
- a single diffusion break (SDB) structure in the fin-shaped structure to divide the fin-shaped structure into a first portion and a second portion;
- a gate structure on the first portion; and
- a contact etch stop layer (CESL) adjacent to the gate structure and extending to cover the SDB structure.

14. The semiconductor device of claim 13, further comprising:

- a first spacer on sidewalls of the gate structure; and
- a second spacer on sidewalls of the SDB structure, wherein the

CESL is disposed on the first spacer and the second spacer.

15. The semiconductor device of claim 14, further comprising a source/drain region in the substrate adjacent to two sides of the first spacer.

16. The semiconductor device of claim 14, further comprising a source/drain region in the substrate adjacent to two sides of the second spacer.

17. The semiconductor device of claim 13, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.

18. The semiconductor device of claim 17, wherein the first direction is orthogonal to the second direction.

Title

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Background of the Invention

1. Field of the Invention

[0001] The invention relates to a method for fabricating semiconductor device, and more particularly to a method for dividing fin-shaped structure to form single diffusion break (SDB) structure.

2. Description of the Prior Art

[0002] With the trend in the industry being towards scaling down the size of the metal oxide semiconductor transistors (MOS), three-dimensional or non-planar transistor technology, such as fin field effect transistor technology (FinFET) has been developed to replace planar MOS transistors. Since the three-dimensional structure of a FinFET increases the overlapping area between the gate and the fin-shaped structure of the silicon substrate, the channel region can therefore be more effectively controlled. This way, the drain-induced barrier lowering (DIBL) effect and the short channel effect are reduced. The channel region is also longer for an equivalent gate length, thus the current between the source and the drain is increased. In addition, the threshold voltage of the fin FET can be controlled by adjusting the work function of the gate.

[0003] In current FinFET fabrication, after shallow trench isolation (STI) is formed around the fin-shaped structure part of the fin-shaped structure and part of the STI could be removed to form a trench, and insulating material is deposited into the trench to form single diffusion break (SDB) structure or isolation structure. However, the integration of the SDB structure and metal gate fabrication still remains numerous problems. Hence how to improve the current FinFET fabrication and structure has become an important task in this field.

Summary of the Invention

[0004] According to an embodiment of the present invention, a method for fabricating semiconductor device includes the steps of: forming a fin-shaped structure on a substrate; forming a shallow trench isolation (STI) around the fin-shaped structure; forming a gate layer on the fin-shaped structure and the STI; removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench; and forming a dielectric layer into the trench to form a single diffusion break (SDB) structure.

[0005] According to another aspect of the present invention, a semiconductor device includes: a fin-shaped structure on a substrate; a single diffusion break (SDB) structure in the fin-shaped structure to divide the fin-shaped structure into a first portion and a second portion; a gate structure on the first portion; and a contact etch stop layer (CESL) adjacent to the gate structure and extending to cover the SDB structure.

[0006] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0007] Figs. 1-10 illustrate a method for fabricating a semiconductor device according to an embodiment of the present invention.

Detailed Description

[0008] Referring to Figs. 1-2, in which Fig. 1 is a top view illustrating a method for fabricating a semiconductor device according to an embodiment of the present invention, the left portion

of Fig. 2 illustrates a cross-sectional view of Fig. 1 for fabricating the semiconductor device along the sectional line AA', and the right portion of Fig. 2 illustrates a cross-sectional view of Fig. 1 for fabricating the semiconductor device along the sectional line BB'. As shown in Figs. 1-2, a substrate 12, such as a silicon substrate or silicon-on-insulator (SOI) substrate is first provided, and a plurality of fin-shaped structures 14 are formed on the substrate 12. It should be noted that even though four fin-shaped structures 14 are disposed on the substrate 12 in this embodiment, it would also be desirable to adjust the number of fin-shaped structures 14 depending on the demand of the product, which is also within the scope of the present invention.

[0009] Preferably, the fin-shaped structures 14 of this embodiment could be obtained by a sidewall image transfer (SIT) process. For instance, a layout pattern is first input into a computer system and is modified through suitable calculation. The modified layout is then defined in a mask and further transferred to a layer of sacrificial layer on a substrate through a photolithographic and an etching process. In this way, several sacrificial layers distributed with a same spacing and of a same width are formed on a substrate. Each of the sacrificial layers may be stripe-shaped. Subsequently, a deposition process and an etching process are carried out such that spacers are formed on the sidewalls of the patterned sacrificial layers. In a next step, sacrificial layers can be removed completely by performing an etching process. Through the etching process, the pattern defined by the spacers can be transferred into the substrate underneath, and through additional fin cut processes, desirable pattern structures, such as stripe patterned fin-shaped structures could be obtained.

[0010] Alternatively, the fin-shaped structures 14 could also be obtained by first forming a patterned mask (not shown) on the substrate, 12, and through an etching process, the pattern of the patterned mask is transferred to the substrate 12 to form the fin-shaped structures

14. Moreover, the formation of the fin-shaped structures 14 could also be accomplished by first forming a patterned hard mask (not shown) on the substrate 12, and a semiconductor layer composed of silicon germanium is grown from the substrate 12 through exposed patterned hard mask via selective epitaxial growth process to form the corresponding fin-shaped structures 14. These approaches for forming fin-shaped structure are all within the scope of the present invention.

[0011] Next, a shallow trench isolation (STI) 16 is formed around the fin-shaped structures 14. In this embodiment, the formation of the STI 16 could be accomplished by conducting a flowable chemical vapor deposition (FCVD) process to form a silicon oxide layer on the substrate 12 and covering the fin-shaped structures 14 entirely. Next, a chemical mechanical polishing (CMP) process along with an etching process are conducted to remove part of the silicon oxide layer so that the top surface of the remaining silicon oxide is even with or slightly lower than the top surface of the fin-shaped structures 14 for forming the STI 16.

[0012] Next, a gate dielectric layer 18 and a gate layer 20 are formed to cover the fin-shaped structures 14 and the STI 16 entirely, and a patterned mask 22 is formed on the gate layer 20, in which the patterned mask 22 includes an opening 24 to expose part of the gate layer 20 surface. In this embodiment, the gate dielectric layer 18 preferably includes silicon oxide and the gate layer 20 is selected from the group consisting of amorphous silicon and polysilicon. The patterned mask 22 could additionally include an organic dielectric layer (ODL), a silicon-containing hard mask bottom anti-reflective coating (SHB), and a patterned resist and the step of forming the opening 24 in the patterned mask 22 could be accomplished by using the patterned resist as mask to remove part of the SHB and part of the ODL.

[0013] Next, as shown in Fig. 3, an etching process is conducted by

using the patterned mask 22 as mask to remove part of the gate layer 20, part of the gate dielectric layer 18, and part of the fin-shaped structures 14 to form a trench 26. The trench 26 preferably divides the fin-shaped structures 14 into two portions including a first portion 28 on the left side of the trench 26 and a second portion 30 on the right side of the trench 26.

[0014] Next, as shown in Fig. 4, a planar dielectric layer 32 is formed into the trench 26 and on the gate layer 20, in which the dielectric layer 32 preferably fills the trench 26 entirely so that the top surface of the dielectric layer 32 is slightly higher than the top surface of the gate layer 20. In this embodiment, the dielectric layer 32 and the STI 16 are preferably made of different material, in which the dielectric layer 32 filled into the trench 26 preferably includes silicon nitride while the STI 16 preferably includes silicon oxide, but not limited thereto. Nevertheless, according to an embodiment of the present invention, the dielectric layer 32 and the STI 16 could also include same material such as silicon oxide, which is also within the scope of the present invention.

[0015] Referring to Figs. 5-6, in which Fig. 5 is a top view illustrating the fabrication of the semiconductor device following Fig. 4, the left portion of Fig. 6 illustrates a cross-sectional view of Fig. 5 along the sectional line CC' and the right portion of Fig. 6 illustrates a cross-sectional view of Fig. 5 along the sectional line DD'. As shown in Figs. 5-6, a planarizing process such as CMP is conducted to remove part of the dielectric layer 32 so that the top surface of the remaining dielectric layer 32 is even with the top surface of the gate layer 20. This forms a single diffusion break (SDB) structure 34 protruding above the fin-shaped structures 14, in which the top surfaces of the SDB structure 32 and the gate layer 20 are coplanar. As shown in Fig. 5, the fin-shaped structures 14 are disposed extending along a first direction (such as X-direction) and the SDB structure 34 is disposed extending along a second direction (such as Y-direction), in which the SDB structure 34 preferably

separates each of the fin-shaped structures into two portions, including a first portion 28 on the left side of the SDB structure 34 and a second portion 30 on the right side of the SDB structure 34.

[0016] Next, as shown in Fig. 7, a pattern transfer process is conducted by first forming a first hard mask 36, a second hard mask 38, and a patterned mask 40 on the gate layer 20 while the patterned mask 40 not covering the SDB structure 34. In this embodiment, the first hard mask 36 and the second hard mask 38 are composed of different material, in which the first hard mask 36 preferably includes silicon nitride and the second hard mask 38 preferably includes silicon oxide, but not limited thereto. The patterned hard mask 40 could be a single patterned resist or could be made of same material as the patterned mask 22 from Fig. 2, and in such instance, the patterned mask 40 could include a tri-layered structure such as an organic dielectric layer (ODL), a silicon-containing hard mask bottom anti-reflective coating (SHB), and a patterned resist.

[0017] Next, as shown in Fig. 8, one or multiple etching processes are conducted by using the patterned mask 40 as mask to remove part of the second hard mask 38, part of the first hard mask 36, part of the gate layer 20, and part of the gate dielectric layer 18 to form a gate structure 42 adjacent to the SDB structure 34. It should be noted that no additional gate structure is formed directly on top of the SDB structure 34 during the formation of gate structure 42, however, dummy gate (not shown) could be disposed on an edge of the fin-shaped structures 14 to stand on top of both the fin-shaped structures 14 and the STI 16 at the same time, in which the top surface of the dummy gate is even with the top surface of the gate structure 42. Preferably, the top surface of the STI 16 is slightly lower than the top surface of the fin-shaped structure 14 while the top surface of the SDB structure 34 is higher than both the top surface of the fin-shaped structures 14 and the STI 16. Moreover, the height of the SDB 34 protruding above the fin-shaped structures 14 is reduced

slightly during the etching process so that the top surface of the SDB 34 would become slightly lower than the top surface of the gate layer 20. Next, a cap layer 44 is formed on the fin-shaped structures 14 to cover the gate structure 42 and the SDB structure 34 at the same time. In this embodiment, the cap layer 44 could include material such as SiN, SiO₂, SiON, SiCN, or combination thereof.

[0018] Next, as shown in Fig. 9, an etching process is conducted to remove part of the cap layer 44 for forming a first spacer 46 adjacent to the sidewalls of the gate structure 42 and at the same time forming a second spacer 48 on the sidewalls of the SDB structure 34. Next, source/drain regions 50 and/or epitaxial layers (not shown) are formed in the fin-shaped structures 14 adjacent to two sides of the first spacer 46 and second spacer 48, and silicides (not shown) could be selectively formed on the surface of the source/drain regions 50 and/or epitaxial layers afterwards. In this embodiment, each of the first spacer 46 and second spacer 48 could be a single spacer or a composite spacer, such as a spacer including but not limited to for example an offset spacer and a main spacer. Preferably, the offset spacer and the main spacer could include same material or different material while both the offset spacer and the main spacer could be made of material including but not limited to for example SiO₂, SiN, SiON, SiCN, or combination thereof. The source/drain regions 50 could include dopants and epitaxial material of different conductive type depending on the type of device being fabricated. For example, the source/drain regions 50 on an NMOS region could include SiC or SiP while the source/drain regions 50 on a PMOS region could include SiGe, but not limited thereto.

[0019] Next, a contact etch stop layer (CESL) 52 is formed on the surface of the fin-shaped structures 14 and covering the gate structure 42 and the SDB structure 34, and an interlayer dielectric (ILD) layer 54 is formed on the CESL 52. Next, a planarizing process such as CMP is conducted to remove part of the ILD layer 54 and part of the CESL 52 for exposing the gate layer 20 made of polysilicon,

in which the top surface of the gate layer 20 is even with the top surface of the ILD layer 52.

[0020] Next, a replacement metal gate (RMG) process is conducted to transform the gate structure 42 into a metal gate. For instance, the RMG process could be accomplished by first performing a selective dry etching or wet etching process using etchants including but not limited to for example ammonium hydroxide (NH_4OH) or tetramethylammonium hydroxide (TMAH) to remove the second hard mask 38, first hard mask 36, gate layer 20, and even gate dielectric layer 18 from gate structure 42 for forming a recess 56 in the ILD layer 54.

[0021] Next, as shown in Fig. 10, a selective interfacial layer 58 or gate dielectric layer (not shown), a high-k dielectric layer 60, a work function metal layer 62, and a low resistance metal layer 64 are formed in the recess 56, and a planarizing process such as CMP is conducted to remove part of low resistance metal layer 64, part of work function metal layer 62, and part of high-k dielectric layer 60 to form metal gate 66. Next, part of the low resistance metal layer 64, part of the work function metal layer 62, and part of the high-k dielectric layer 60 are removed to form another recess (not shown), and a hard mask 68 made of dielectric material including but not limited to for example silicon nitride is deposited into the recess so that the top surfaces of the hard mask 68 and ILD layer 54 are coplanar. In this embodiment, the gate structure or metal gate 66 fabricated through high-k last process of a gate last process preferably includes an interfacial layer 58 or gate dielectric layer (not shown), a U-shaped high-k dielectric layer 60, a U-shaped work function metal layer 62, and a low resistance metal layer 64.

[0022] In this embodiment, the high-k dielectric layer 60 is preferably selected from dielectric materials having dielectric constant (k value) larger than 4. For instance, the high-k dielectric layer 60 may be selected from hafnium oxide (HfO_2), hafnium silicon

oxide (HfSiO_4), hafnium silicon oxynitride (HfSiON), aluminum oxide (Al_2O_3), lanthanum oxide (La_2O_3), tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), strontium titanate oxide (SrTiO_3), zirconium silicon oxide (ZrSiO_4), hafnium zirconium oxide (HfZrO_4), strontium bismuth tantalate ($\text{SrBi}_2\text{Ta}_2\text{O}_9$, SBT), lead zirconate titanate ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$, PZT), barium strontium titanate ($\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$, BST) or a combination thereof.

[0023] In this embodiment, the work function metal layer 62 is formed for tuning the work function of the metal gate in accordance with the conductivity of the device. For an NMOS transistor, the work function metal layer 62 having a work function ranging between 3.9 eV and 4.3 eV may include titanium aluminide (TiAl), zirconium aluminide (ZrAl), tungsten aluminide (WAl), tantalum aluminide (TaAl), hafnium aluminide (HfAl), or titanium aluminum carbide (TiAlC), but it is not limited thereto. For a PMOS transistor, the work function metal layer 62 having a work function ranging between 4.8 eV and 5.2 eV may include titanium nitride (TiN), tantalum nitride (TaN), tantalum carbide (TaC), but it is not limited thereto. An optional barrier layer (not shown) could be formed between the work function metal layer 62 and the low resistance metal layer 64, in which the material of the barrier layer may include titanium (Ti), titanium nitride (TiN), tantalum (Ta) or tantalum nitride (TaN). Furthermore, the material of the low-resistance metal layer 64 may include copper (Cu), aluminum (Al), titanium aluminum (TiAl), cobalt tungsten phosphide (CoWP) or any combination thereof.

[0024] Next, a pattern transfer process is conducted by using a patterned mask (not shown) as mask to remove part of the ILD layer 54 adjacent to the metal gate 66 and SDB structure 34 for forming contact holes (not shown) exposing the source/drain regions 50 underneath. Next, metals including a barrier layer selected from the group consisting of Ti , TiN , Ta , and TaN and a low resistance metal layer selected from the group consisting of W , Cu , Al , TiAl , and CoWP are deposited into the contact holes, and a planarizing process such

as CMP is conducted to remove part of aforementioned barrier layer and low resistance metal layer for forming contact plugs 70 electrically connecting the source/drain regions 50. This completes the fabrication of a semiconductor device according to a preferred embodiment of the present invention.

[0025] Referring again to Fig. 10, which further illustrates a structural view of a semiconductor device according to an embodiment of the present invention. As shown in Fig. 10, the semiconductor device preferably includes a fin-shaped structure 14 disposed on the substrate 12, a SDB structure 34 disposed within the fin-shaped structure 14 while protruding above the fin-shaped structure 14 and dividing the fin-shaped structure 14 into a first portion 28 and a second portion 30, and a gate structure or metal gate 66 disposed on the first portion 28. Preferably, the top surface of the metal gate 66 is even with or slightly higher than the top surface of the SDB structure 34, the fin-shaped structure 14 is disposed extending along a first direction while the SDB structure 34 is disposed extending along a second direction, in which the first direction is orthogonal to the second direction as shown in Fig. 5.

[0026] The semiconductor device also includes a first spacer 46 on the sidewalls of the metal gate 66, a second spacer 48 on the sidewalls of the SDB structure 34, a CESL 52 disposed adjacent to the first spacer 46 and extending to cover the second spacer 48 and SDB structure 34 while contacting the SDB structure 34 directly, and source/drain regions 50 disposed in the fin-shaped structure 14 adjacent to two sides of the first spacer 46 and second spacer 48.

[0027] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Chun-Hao Lin		
Filer:		Winston Hsu/Wendy Chen		
Attorney Docket Number:		NAUP3064USA		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	29902798
Application Number:	15660991
International Application Number:	
Confirmation Number:	8497
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hao Lin
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Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP3064USA
Receipt Date:	27-JUL-2017
Filing Date:	
Time Stamp:	05:57:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	072717INTEFSW00009449503105
Deposit Account	503105
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2917418.PDF	1782319	no	9
			77687401a4a9614f5e4f47a63ae39a37a21e a694		
Warnings:					
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2	Information Disclosure Statement (IDS) Form (SB08)	2917417.PDF	28415	no	3
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			518b5a87826762280f8d20ca0765a5e04d4 4d327		
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6	Drawings-only black and white line drawings	2917907.PDF	84770	no	5
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7	Abstract	2917906.PDF	30581	no	1
			9c154d0ab24654d9bd7528c30d43b0b53a c3dd05		
Warnings:					
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8	Claims	2917905.PDF	35595	no	3
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Warnings:					
Information:					
9	Specification	2917904.PDF	69189	no	10
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Warnings:					
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10	Fee Worksheet (SB06)	fee-info.pdf	34882	no	2
			78cfd1a20d684675e692be99e4e12e25767 90fe		
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor	1				Remove
Legal Name					
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

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☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	27765		
Email Address	winstonhsu@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
Attorney Docket Number	NAUP3064USA	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

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Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)	
201710516576.7	CN	2017-06-29		
Additional Foreign Priority Data may be generated within this form by selecting the Add button.				Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1		Remove	
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
		Clear	
☒ Assignee	Legal Representative under 35 U.S.C. 117		Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	UNITED MICROELECTRONICS CORP.		
Mailing Address Information For Applicant:			
Address 1	No.3, Li-Hsin Road 2, Science-Based Industrial Park		
Address 2			
City	Hsin-Chu City	State/Province	
Country	TW	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

Assignee	1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
Remove				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add				

Signature:	Remove			
NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).				
This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a juristic entity (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.				
See 37 CFR 1.4(d) for the manner of making signatures and certifications.				
Signature	/Winston Hsu/		Date (YYYY-MM-DD)	2017-07-26
First Name	Winston	Last Name	Hsu	Registration Number
				41526
Additional Signature may be generated within this form by selecting the Add button. Add				

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP3064USA
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
15/660,991	07/27/2017	2812	1600	NAUP3064USA	18	2

CONFIRMATION NO. 8497

FILING RECEIPT

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN



0000000093200200

Date Mailed: 08/03/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Chun-Hao Lin, Kaohsiung City, TAIWAN;
Hsin-Yu Chen, Nantou County, TAIWAN;
Shou-Wei Hsieh, Hsinchu City, TAIWAN;

Applicant(s)

UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)
CHINA 201710516576.7 06/29/2017

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 08/02/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/660,991**

Projected Publication Date: 01/03/2019

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

**LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 15/660,991				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(i))	18	minus 20 = *				x 80 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE				TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE				TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



证 明

本证明之附件是向本局提交的下列专利申请文件副本。

申 请 号：201710516576.7

申 请 类 型：发明专利

发 明 创 造 名 称：半导体元件及其制作方法

申 请 日：2017 年 06 月 29 日

申 请 人：联华电子股份有限公司

发明人或设计人：林俊豪、陈信宇、谢守伟

局长

申长雨

2017 年 08 月 28 日



P17J27554

权 利 要 求 书

1. 一种制作半导体元件的方法, 包含:
 - 5 形成一鳍状结构于一基底上;
 - 形成一浅沟隔离于该鳍状结构周围;
 - 形成一栅极层于该鳍状结构及该浅沟隔离上;
 - 去除部分该栅极层、部分该鳍状结构以及部分该浅沟隔离以形成一开口; 以及
 - 10 形成一介电层于该开口内以形成一单扩散隔离结构。
2. 如权利要求 1 所述的方法, 另包含于形成该栅极层之前形成一栅极介电层于该鳍状结构上。
3. 如权利要求 1 所述的方法, 另包含:
 - 形成一图案化掩模于该栅极层上; 以及
 - 15 利用该图案化掩模为掩模去除部分该栅极层、部分该栅极介电层以及部分该鳍状结构以形成该开口。
4. 如权利要求 1 所述的方法, 另包含:
 - 形成该介电层于该开口内以及该栅极层上;
 - 平坦化该介电层并使该介电层上表面切齐该栅极层上表面。
5. 如权利要求 1 所述的方法, 另包含:
 - 20 在形成该单扩散隔离结构后去除部分该栅极层以于该单扩散隔离结构旁形成一栅极结构。
6. 如权利要求 1 所述的方法, 另包含:
 - 形成一遮盖层于该栅极结构及该单扩散隔离结构上; 以及
 - 25 去除部分该遮盖层以形成一第一间隙壁于该栅极结构旁以及一第二间隙壁于该单扩散隔离结构旁。
7. 如权利要求 1 所述的方法, 其中该鳍状结构沿着一第一方向延伸且该单扩散隔离结构沿着一第二方向延伸。
8. 如权利要求 7 所述的方法, 其中该第一方向垂直该第二方向。
9. 如权利要求 1 所述的方法, 其中该栅极层包含多晶硅。
- 30 10. 如权利要求 1 所述的方法, 其中该栅极层包含非晶硅。



11. 如权利要求 1 所述的方法，其中该介电层包含氮化硅。
12. 如权利要求 1 所述的方法，其中该介电层包含氧化硅。
13. 一种半导体元件，包含：
- 鳍状结构，设于一基底上；
- 5 单扩散隔离结构，设于该鳍状结构内并将该鳍状结构分隔为第一部分与第二部分；
- 栅极结构，设于该第一部分上；以及
- 接触洞蚀刻停止层，设于该栅极结构旁并延伸至该单扩散隔离结构上。
14. 如权利要求 13 所述的半导体元件，另包含：
- 10 第一间隙壁，设于该栅极结构侧壁；以及
- 第二间隙壁，设于该单扩散隔离结构侧壁，其中该接触洞蚀刻停止层设于该第一间隙壁以及该第二间隙壁上。
15. 如权利要求 14 所述的半导体元件，另包含一源极/漏极区域设于该第一间隙壁两侧的该基底内。
- 15 16. 如权利要求 14 所述的半导体元件，另包含一源极/漏极区域设于该第二间隙壁两侧的该基底内。
17. 如权利要求 13 所述的半导体元件，其中该鳍状结构沿着一第一方向延伸且该单扩散隔离结构沿着一第二方向延伸。
18. 如权利要求 17 所述的半导体元件，其中该第一方向垂直该第二方
- 20 向。



P17J27554

说明书

半导体元件及其制作方法

5

技术领域

本发明涉及一种制作半导体元件的方法，尤其是涉及一种分隔鳍状结构以形成单扩散隔离(single diffusion break, SDB)结构的方法。

10

背景技术

近年来，随着场效晶体管(field effect transistors, FETs)元件尺寸持续地缩小，现有平面式(planar)场效晶体管元件的发展已面临制作工艺上的极限。为了克服制作工艺限制，以非平面(non-planar)的场效晶体管元件，例如鳍状场效晶体管(fin field effect transistor, Fin FET)元件来取代平面晶体管元件已成为目前的主流发展趋势。由于鳍状场效晶体管元件的立体结构可增加栅极与鳍状结构的接触面积，因此，可进一步增加栅极对于载流子通道区域的控制，从而降低小尺寸元件面临的漏极引发能带降低(drain induced barrier lowering, DIBL)效应，并可以抑制短通道效应(short channel effect, SCE)。再者，由于鳍状场效晶体管元件在同样的栅极长度下会具有更宽的通道宽度，因而可获得加倍的漏极驱动电流。甚而，晶体管元件的临界电压(threshold voltage)也可通过调整栅极的功函数而加以调控。

20

在现行的鳍状场效晶体管元件制作工艺中，鳍状结构周围形成浅沟隔离后通常会以蚀刻方式去除部分鳍状结构与浅沟隔离形成凹槽，然后填入绝缘物以形成单扩散隔离结构并将鳍状结构分隔为两部分。然而现今单扩散隔离结构与金属栅极的制作工艺在搭配上仍存在许多问题，因此如何改良现有鳍状场效晶体管制作工艺与架构即为现今一重要课题。

25

发明内容

为解决上述问题，本发明一实施例公开一种制作半导体元件的方法。首先形成一鳍状结构于基底上，然后形成一浅沟隔离于鳍状结构周围，形成一栅极层于鳍状结构及浅沟隔离上，去除部分栅极层、部分鳍状结构以及部分

浅沟隔离以形成一开口，之后再形成一介电层于开口内以形成一单扩散隔离结构。

本发明另一实施例公开一种半导体元件，其主要包含一鳍状结构设于一基底上、一单扩散隔离结构设于鳍状结构内并将该鳍状结构分隔为第一部分与第二部分、一栅极结构设于该第一部分上以及一接触洞蚀刻停止层设于栅极结构旁并延伸至单扩散隔离结构上。

附图说明

图 1 至图 10 为本发明一实施例制作一半导体元件的方法示意图。

10 主要元件符号说明

12	基底	14	鳍状结构
16	浅沟隔离	18	栅极介电层
20	栅极层	22	图案化掩模
24	开口	26	开口
28	第一部分	30	第二部分
32	介电层	34	单扩散隔离结构
36	第一硬掩模	38	第二硬掩模
40	图案化掩模	42	栅极结构
44	遮盖层	46	第一间隙壁
48	第二间隙壁	50	源极/漏极区域
52	接触洞蚀刻停止层	54	层间介电层
56	凹槽	58	介质层
60	高介电常数介电层	62	功函数金属层
64	低阻抗金属层	66	金属栅极
68	硬掩模	70	接触插塞

具体实施方式

请参照图 1 至图 2，其中图 1 为本发明一实施例制作一半导体元件的上视图，图 2 左半部为图 1 中沿着切线 AA' 的剖面示意图，图 2 右半部则为图 1 中沿着切线 BB' 的剖面示意图。如图 1 至图 2 所示，首先提供一基底 12，例如一硅基底或硅覆绝缘(SOI)基板。然后形成多个鳍状结构 14 于基底 12

上。在本实施例中，设于基底 12 上的鳍状结构 14 虽以四根为例，但所设置的鳍状结构数量均可依据产品需求任意调整，并不局限于此。

依据本发明的优选实施例，鳍状结构 14 较佳通过侧壁图案转移(sidewall image transfer, SIT)等技术制得，其程序大致包括：提供一布局图案至电脑系统，并经过适当地运算以将相对应的图案定义于光掩模中。后续可通过光刻及蚀刻制作工艺，以形成多个等距且等宽的图案化牺牲层于基底上，使其个别外观呈现条状。之后依序施行沉积及蚀刻制作工艺，以于图案化牺牲层的各侧壁形成间隙壁。继以去除图案化牺牲层，并在间隙壁的覆盖下施行蚀刻制作工艺，使得间隙壁所构成的图案被转移至基底内，再伴随鳍状结构切割制作工艺(fin cut)而获得所需的图案化结构，例如条状图案化鳍状结构。

除此之外，鳍状结构 14 的形成方式又可包含先形成一图案化掩模(图未示)于基底 12 上，再经过一蚀刻制作工艺，将图案化掩模的图案转移至基底 12 中以形成鳍状结构 14。另外，鳍状结构 14 的形成方式也可以先形成一图案化硬掩模层(图未示)于基底 12 上，并利用外延制作工艺于暴露出图案化硬掩模层的基底 12 上成长出例如包含硅锗的半导体层，而此半导体层即可作为相对应的鳍状结构 14。这些形成鳍状结构 14 的实施例均属本发明所涵盖的范围。

然后形成一浅沟隔离(shallow trench isolation, STI)16 环绕鳍状结构 14。在本实施例中，形成浅沟隔离 16 的方式可先利用一可流动式化学气相沉积(flowable chemical vapor deposition, FCVD)制作工艺形成一氧化硅层于基底 12 上并完全覆盖鳍状结构 14。接着利用化学机械研磨(chemical mechanical polishing, CMP)制作工艺并搭配蚀刻制作工艺去除部分氧化硅层，使剩余的氧化硅层低于鳍状结构 14 表面以形成浅沟隔离 16。

接着依序形成一栅极介电层 18 以及一栅极层 20 并完全覆盖于鳍状结构 14 与浅沟隔离 16 上，然后形成一图案化掩模 22 于栅极层 20 上，其中图案化掩模 22 具有一开口 24 暴露出部分栅极层 20 表面。在本实施例中，栅极介电层 18 较佳包含氧化硅，栅极层 20 则可选自由非晶硅以及多晶硅所构成的群组。另外图案化掩模 22 可包含一有机介电层(organic dielectric layer, ODL)、一含硅硬掩模与抗反射(silicon-containing hard mask bottom anti-reflective coating, SHB)层以及一图案化光致抗蚀剂，且于图案化掩模 22 中形成开口 24 的步骤可利用图案化光致抗蚀剂为掩模去除部分含硅硬掩模

与抗反射层与部分有机介电层来达成。

如图 3 所示，然后利用图案化掩模 22 为掩模进行一蚀刻制作工艺，依序去除部分栅极层 20、部分栅极介电层 18 以及部分鳍状结构 14 以形成开口 26，并同时将鳍状结构 14 分隔为两部分，包括位于开口 26 左侧的第一部分 28 与位于开口 26 右侧的第二部分 30。

随后如图 4 所示，形成一平坦的介电层 32 于开口 26 内与栅极层 20 上，其中介电层 32 较佳填满开口 26 且介电层 32 上表面较佳高于栅极层 20 上表面。在本实施例中，介电层 32 与浅沟隔离 16 较佳包含不同材料，例如填入开口 26 内的介电层 32 较佳包含氮化硅而浅沟隔离 16 包含氧化硅，但不局限于此，依据本发明一实施例介电层 32 又可与浅沟隔离 16 选用相同材料，例如同样包含氧化硅，此实施例也属本发明所涵盖的范围。

请接着参照图 5 与图 6，图 5 为接续图 4 制作半导体元件的上视图，图 6 左半部为图 5 中沿着切线 CC' 的剖面示意图，图 6 右半部则为图 5 中沿着切线 DD' 的剖面示意图。如图 5 至图 6 所示，然后进行一平坦化制作工艺，例如利用化学机械研磨制作工艺去除部分介电层 32 并使剩余的介电层 32 上表面约略切齐栅极层 20 上表面，由此形成一单扩散隔离结构 34 突出于鳍状结构 14，并约略切齐栅极层 20 上表面。如图 5 的上视图所示，各鳍状结构 14 较佳沿着一第一方向(例如 X 方向)延伸而单扩散隔离结构 34 则较佳沿着一第二方向(例如 Y 方向)延伸横跨鳍状结构并同时各鳍状结构分隔为两部分，例如设于单扩散隔离结构 34 左侧的第一部分 28 与右侧的第二部分 30。

如图 7 所示，随后对栅极层 20 进行一图案转移制作工艺，例如先依序形成一第一硬掩模 36、第二硬掩模 38 以及一图案化掩模 40 于栅极层上且图案化掩模 40 较佳不覆盖单扩散隔离结构 34。在本实施例中，第一硬掩模 36 与第二硬掩模 38 较佳包含不同材料，例如第一硬掩模 36 较佳包含氮化硅而第二硬掩模 38 较佳包含氧化硅，但不局限于此。图案化掩模 40 可包含单一图案化光致抗蚀剂，或可与图 2 所形成的图案化掩模 22 包含相同材料，例如可包含一有机介电层(organic dielectric layer, ODL)、一含硅硬掩模与抗反射(silicon-containing hard mask bottom anti-reflective coating, SHB)层以及一图案化光致抗蚀剂等三层结构，这些实施例均属本发明所涵盖的范围。

如图 8 所示，接着利用图案化掩模 40 为掩模进行一次或多次蚀刻制作工艺，依序去除部分第二硬掩模 38、部分第一硬掩模 36、部分栅极层 20 以

及部分栅极介电层 18，以于单扩散隔离结构 34 旁形成一栅极结构 42。值得注意的是，在形成栅极结构 42 时单扩散隔离结构 34 上方并未形成任何栅极结构，但鳍状结构 14 的边缘处可设有虚置栅极(图未示)同时跨在鳍状结构 14 与浅沟隔离 16 上，虚置栅极上表面可切齐栅极结构 42 上表面，且以高度而言浅沟隔离 16 上表面较佳略低于鳍状结构 14 表面而单扩散隔离结构 34 上表面则同时高于鳍状结构 14 与浅沟隔离 16 上表面。此外，突出于鳍状结构 14 的单扩散隔离结构 34 会受此蚀刻制作工艺的影响而略低于栅极层 20 的上表面，但仍突出于鳍状结构 14。随后可形成一遮盖层 44 于鳍状结构 14 上并覆盖栅极结构 42 与单扩散隔离结构 34。在本实施例中，遮盖层 44 可包含氮化硅、氧化硅、氮氧化硅、氮碳化硅或其组合所构成，但不局限于此。

然后如图 9 所示，进行一蚀刻制作工艺去除部分遮盖层 44 以形成一第一间隙壁 46 于栅极结构 42 侧壁并同时形成第二间隙壁 48 于单扩散隔离结构 34 侧壁。接着于第一间隙壁 46 与第二间隙壁 48 两侧的鳍状结构 14 以及/或基底 12 中形成源极/漏极区域 50 及/或外延层(图未示)，并选择性于源极/漏极区域 50 及/或外延层的表面形成一金属硅化物(图未示)。在本实施例中，第一间隙壁 46 与第二间隙壁 48 虽分别以单一间隙壁为例，但又可各别为复合式间隙壁，例如可细部包含一偏位间隙壁以及一主间隙壁。其中偏位间隙壁与主间隙壁可包含相同或不同材料，且两者均可选自由氧化硅、氮化硅、氮氧化硅以及氮碳化硅所构成的群组。源极/漏极区域 50 可依据所置备晶体管的导电型式而包含不同掺质，例如可包含 P 型掺质或 N 型掺质。

随后形成一接触洞蚀刻停止层 52 于鳍状结构 14 表面并覆盖栅极结构 42 与单扩散隔离结构 34，再形成一层间介电层 54 于接触洞蚀刻停止层 52 上。然后进行一平坦化制作工艺，例如利用化学机械研磨去除部分层间介电层 54 与部分接触洞蚀刻停止层 52 并暴露出由多晶硅材料所构成的栅极层 20，使栅极层 20 上表面与层间介电层 52 上表面齐平。

随后进行一金属栅极置换制作工艺将栅极结构 42 转换为金属栅极。举例来说，可先进行一选择性的干蚀刻或湿蚀刻制作工艺，例如利用氨水(ammonium hydroxide, NH_4OH)或氢氧化四甲铵(Tetramethylammonium Hydroxide, TMAH)等蚀刻溶液来去除栅极结构 42 中的第二硬掩模 38、第一硬掩模 36、栅极层 20 甚至栅极介电层 18，以于层间介电层 54 中形成凹槽 56。

如图 10 所示, 之后依序形成一选择性介质层 58 或栅极介电层、一高介电常数介电层 60、一功函数金属层 62 以及一低阻抗金属层 64 于凹槽内, 然后进行一平坦化制作工艺, 例如利用 CMP 去除部分低阻抗金属层 64、部分功函数金属层 62 与部分高介电常数介电层 60 以形成金属栅极 66。随后可去除部分低阻抗金属层 64、部分功函数金属层 64 以及部分高介电常数介电层 60 以形成凹槽(图未示), 再填入一由例如氮化硅所构成的硬掩模 68 于凹槽内并使硬掩模 68 上表面切齐层间介电层 54 上表面。以本实施例利用后高介电常数介电层制作工艺所制作的栅极结构为例, 所形成的金属栅极 66 较佳包含一介质层 58 或栅极介电层、一 U 型高介电常数介电层 60、一 U 型功函数金属层 62 以及一低阻抗金属层 64。

在本实施例中, 高介电常数介电层 60 包含介电常数大于 4 的介电材料, 例如选自氧化铪(hafnium oxide, HfO_2)、硅酸铪氧化合物(hafnium silicon oxide, HfSiO_4)、硅酸铪氮氧化合物(hafnium silicon oxynitride, HfSiON)、氧化铝(aluminum oxide, Al_2O_3)、氧化镧(lanthanum oxide, La_2O_3)、氧化钽(tantalum oxide, Ta_2O_5)、氧化钇(yttrium oxide, Y_2O_3)、氧化锆(zirconium oxide, ZrO_2)、钛酸锶(strontium titanate oxide, SrTiO_3)、硅酸锆氧化合物(zirconium silicon oxide, ZrSiO_4)、锆酸铪(hafnium zirconium oxide, HfZrO_4)、锶铋钽氧化物(strontium bismuth tantalate, $\text{SrBi}_2\text{Ta}_2\text{O}_9$, SBT)、锆钛酸铅(lead zirconate titanate, $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$, PZT)、钛酸钡锶(barium strontium titanate, $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$, BST)、或其组合所组成的群组。

功函数金属层 62 较佳用以调整形成金属栅极的功函数, 使其适用于 N 型晶体管(NMOS)或 P 型晶体管(PMOS)。若晶体管为 N 型晶体管, 功函数金属层 62 可选用功函数为 3.9 电子伏特(eV)~4.3 eV 的金属材料, 如铝化钛(TiAl)、铝化锆(ZrAl)、铝化钨(WAl)、铝化钽(TaAl)、铝化铪(HfAl)或碳化钛铝(TiAlC)等, 但不以此为限; 若晶体管为 P 型晶体管, 功函数金属层 62 可选用功函数为 4.8 eV~5.2 eV 的金属材料, 如氮化钛(TiN)、氮化钽(TaN)或碳化钽(TaC)等, 但不以此为限。功函数金属层 62 与低阻抗金属层 64 之间可包含另一阻障层(图未示), 其中阻障层的材料可包含钛(Ti)、氮化钛(TiN)、钽(Ta)、氮化钽(TaN)等材料。低阻抗金属层 64 则可选自铜(Cu)、铝(Al)、钨(W)、钛铝合金(TiAl)、钴钨磷化物(cobalt tungsten phosphide, CoWP)等低电阻材料或其组合。

之后可进行一图案转移制作工艺，例如可利用一图案化掩模去除金属栅极 66 与单扩散隔离结构 34 旁的部分的层间介电层 54 以形成多个接触洞(图未示)并暴露出下面的源极/漏极区域 50。然后再于各接触洞中填入所需的金属材料，例如包含钛(Ti)、氮化钛(TiN)、钽(Ta)、氮化钽(TaN)等的阻障层材料以及选自钨(W)、铜(Cu)、铝(Al)、钛铝合金(TiAl)、钴钨磷化物(cobalt tungsten phosphide, CoWP)等低电阻材料或其组合的低阻抗金属层。之后进行一平坦化制作工艺，例如以化学机械研磨去除部分金属材料以分别形成接触插塞 70 于各接触洞内电连接源极/漏极区域 50。至此即完成本发明优选实施例的半导体元件的制作。

10 请继续参照图 10，图 10 另揭露本发明一实施例的一半导体元件的结构示意图。如图 10 所示，半导体元件主要包含一鳍状结构 14 设于基底 12 上，一单扩散隔离结构 34 设于鳍状结构 14 内且突出于鳍状结构 14 并将鳍状结构 14 分隔为第一部分 28 与第二部分 30 以及一栅极结构或金属栅极 66 设于第一部分 28 上，其中金属栅极 66 上表面可切齐或略高于单扩散隔离结构 34 上表面。在本实施例中，鳍状结构 14 沿着一第一方向延伸而单扩散隔离结构 34 沿着一第二方向延伸，且第一方向较佳垂直第二方向，例如图 5 的上视图所示。

此外，半导体元件又包含一第一间隙壁 46 设于金属栅极 66 侧壁、第二间隙壁 48 设于单扩散隔离结构 34 侧壁、接触洞蚀刻停止层 52 设于第一间隙壁 46 旁并延伸至第二间隙壁 48 与单扩散隔离结构 34 上且直接接触单扩散隔离结构 34、以及源极/漏极区域 50 分别设于第一间隙壁 46 两侧的鳍状结构 14 或基底 12 内与第二间隙壁 48 两侧的鳍状结构 14 内。

以上所述仅为本发明的优选实施例，凡依本发明权利要求所做的均等变化与修饰，都应属本发明的涵盖范围。

25

P17J27554

说明书附图

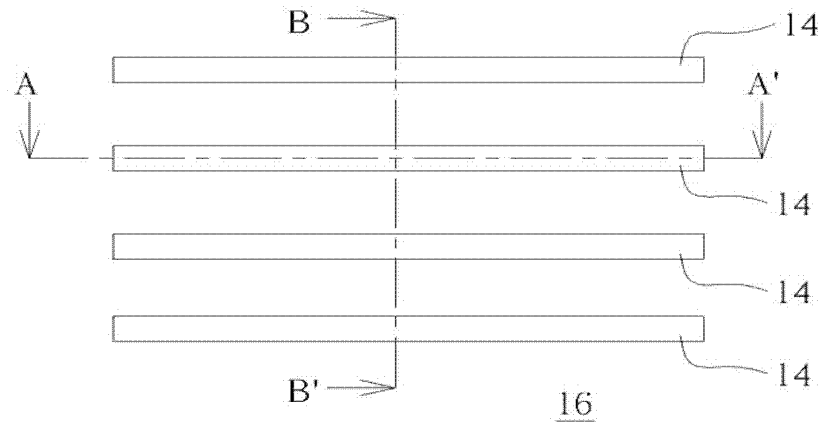


图 1

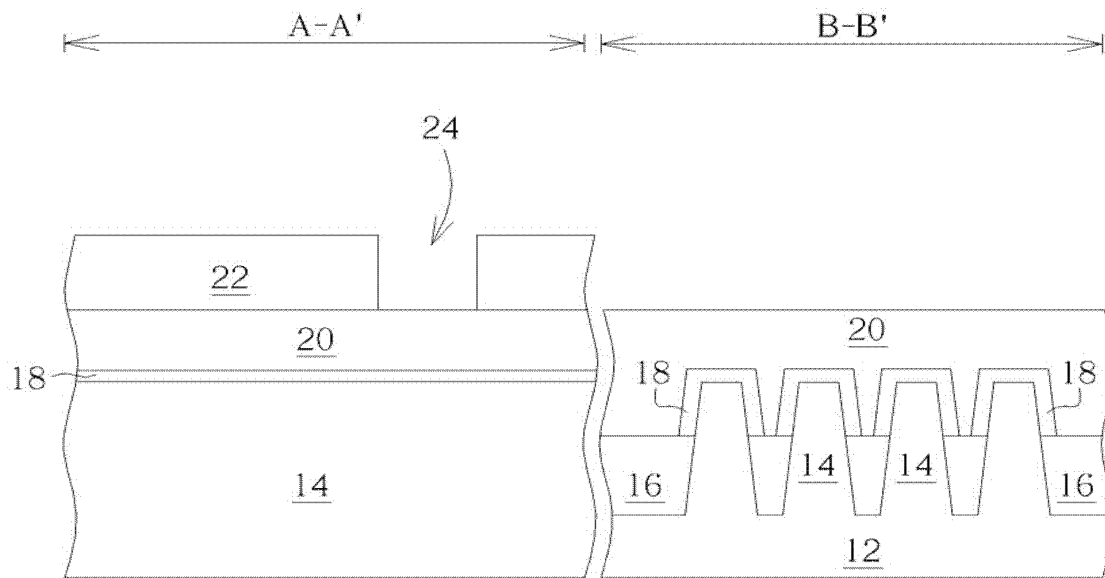
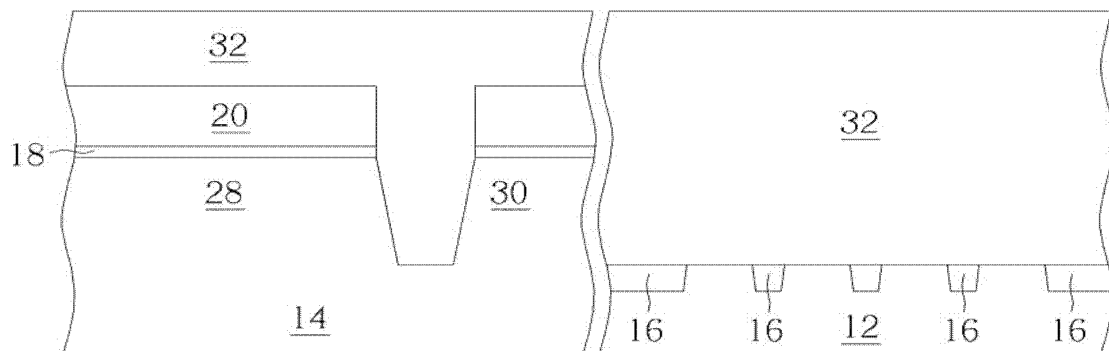


图 2



2

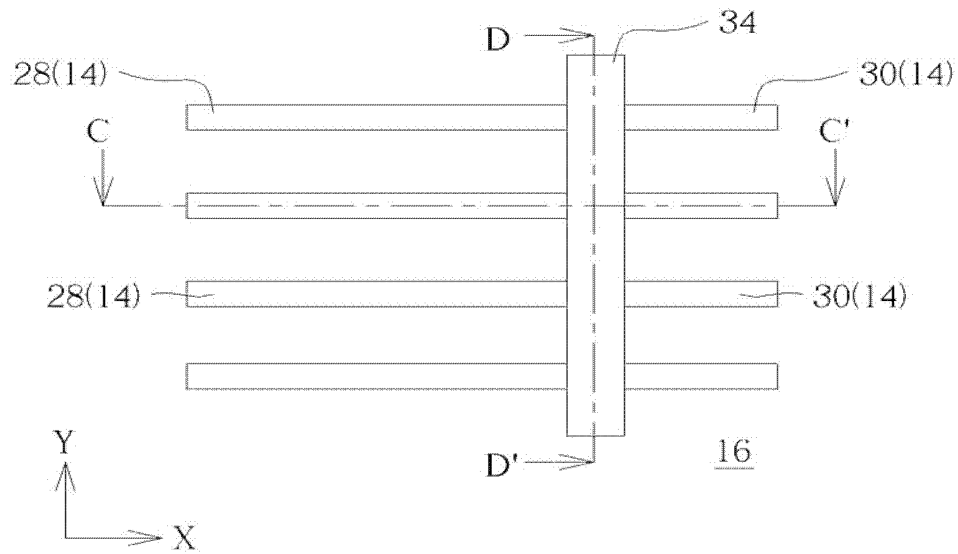


图 5

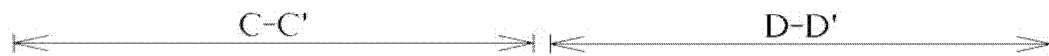


图 6

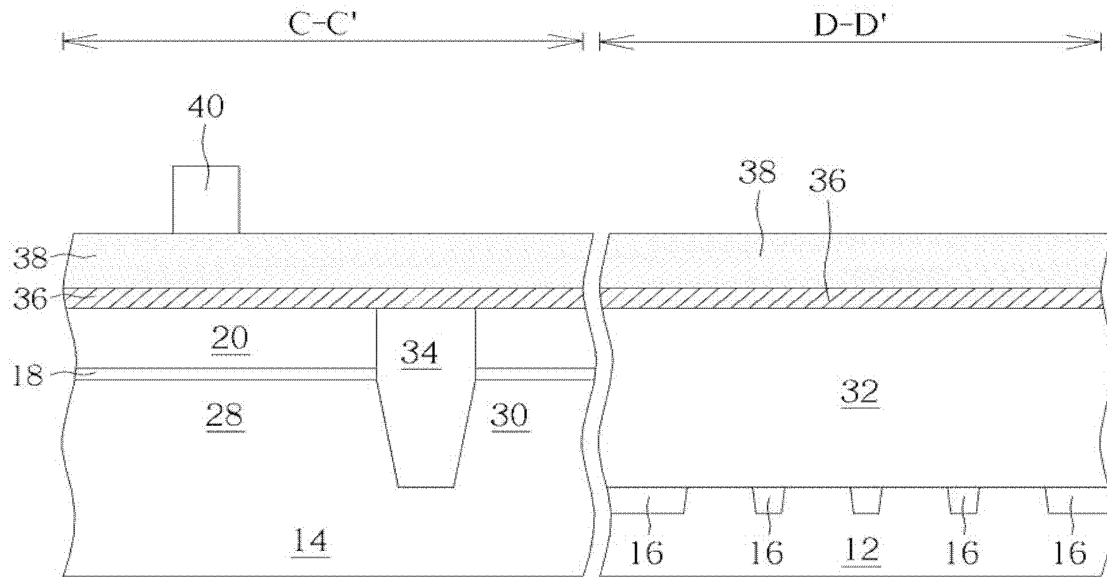


图 7

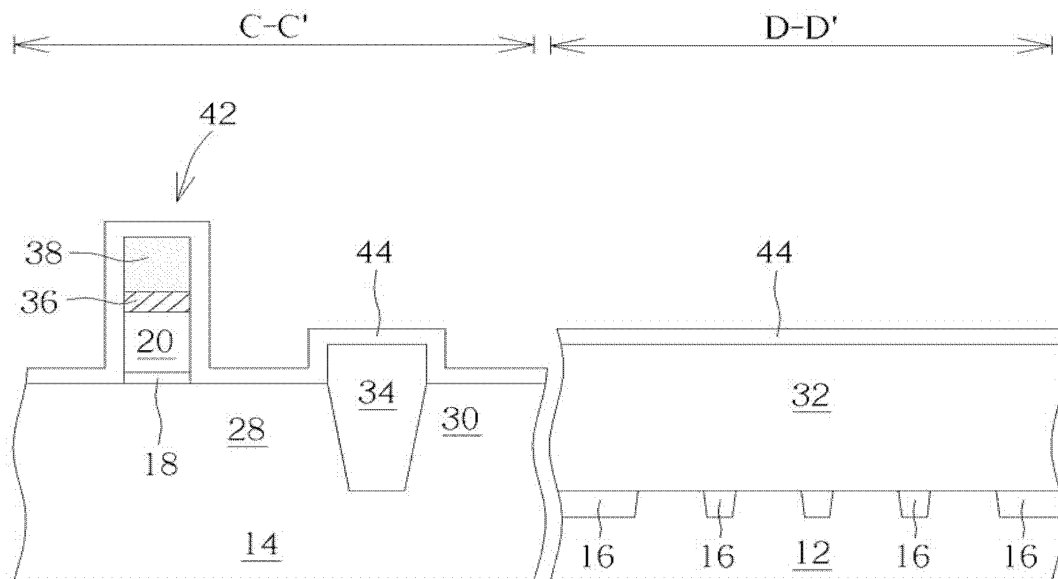


图 8

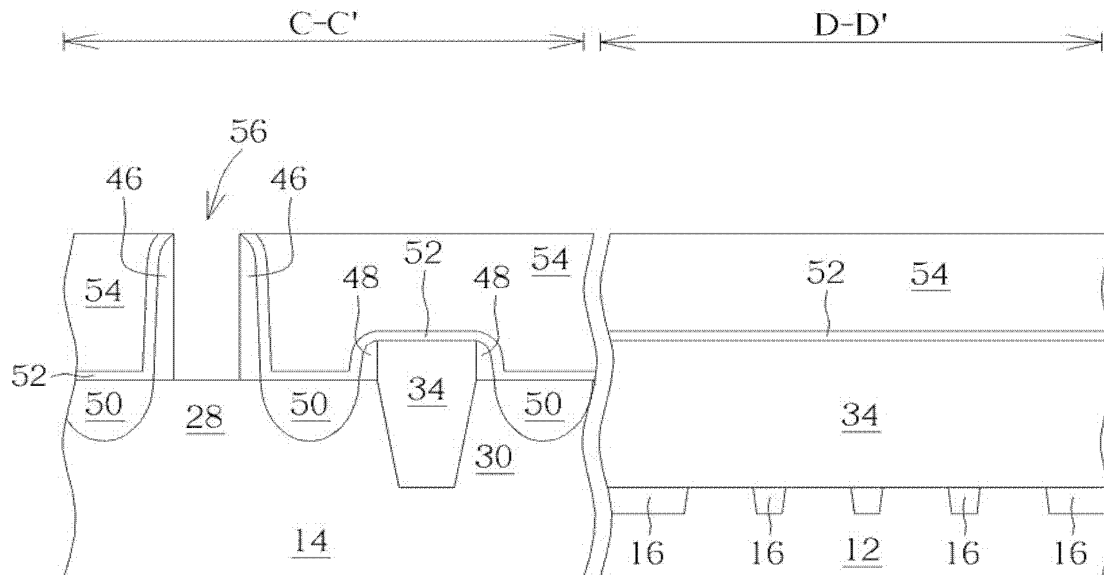


图 9

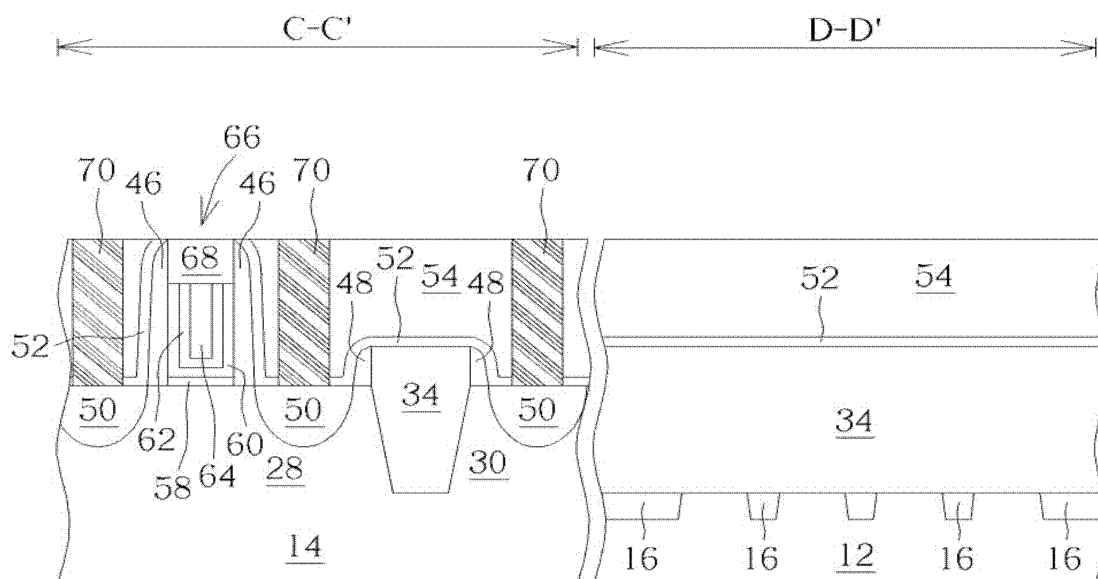


图 10



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/660,991	07/27/2017	Chun-Hao Lin	NAUP3064USA	8497
27765 7590 10/13/2017 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., No.389, Fuhe Rd., Yonghe Dist. New Taipei City, TAIWAN			EXAMINER AHMED, SHAHED	
			ART UNIT	PAPER NUMBER
			2823	
			NOTIFICATION DATE	DELIVERY MODE
			10/13/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 15/660,991	Applicant(s) LIN ET AL.	
	Examiner SHAHED AHMED	Art Unit 2823	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07/27/2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-18 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☐ Claim(s) ____ is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☒ Claim(s) 1-18 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

Art Unit: 2823

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 13-18, drawn to device, classified in H01L29/785.

II. Claims 1-12, drawn to method, classified in H01L21/823481.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the process as claimed can be used to make another and materially different product such that a contact etch stop layer is not formed.

Restriction for examination purposes as indicated is proper because all the inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

- (a) the inventions have acquired a separate status in the art in view of their different classification;
- (b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

Art Unit: 2823

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries).

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention.**

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAHED AHMED whose telephone number is (571)272-3477. The examiner can normally be reached on M-F 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SHAHED AHMED/

Examiner, Art Unit 2823

/SHAHED AHMED/
Examiner, Art Unit 2823

Application/Control Number: 15/660,991

Page 6

Art Unit: 2823

**SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE
SAME**

Appl. No. : 15/660,991 Confirmation No. 8497
First Named Inventor : Chun-Hao Lin
Filed : July 27, 2017
TC/A.U. : 2823
Examiner : AHMED, SHAHED
Docket No. : NAUP3064USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

In response to the Office action of October 13, 2017, please amend the
5 above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on
page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

5

Listing of Claims:

1. (original) A method for fabricating semiconductor device, comprising:
 - forming a fin-shaped structure on a substrate;
 - 10 forming a shallow trench isolation (STI) around the fin-shaped structure;
 - forming a gate layer on the fin-shaped structure and the STI;
 - removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench; and
 - forming a dielectric layer into the trench to form a single diffusion break (SDB)
 - 15 structure.
2. (original) The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.
- 20 3. (original) The method of claim 2, further comprising:
 - forming a patterned mask on the gate layer; and
 - using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.
- 25 4. (original) The method of claim 1, further comprising:
 - forming the dielectric layer into the trench and on the gate layer; and
 - planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.
- 30 5. (original) The method of claim 1, further comprising removing part of the gate layer

after forming the SDB structure to form a gate structure adjacent to the SDB structure.

6. (original) The method of claim 5, further comprising:

forming a cap layer on the gate structure and the SDB structure; and

5 removing part of the cap layer to form a first spacer adjacent to the gate structure
and a second spacer adjacent to the SDB structure.

7. (original) The method of claim 1, wherein the fin-shaped structure is disposed
extending along a first direction and the SDB structure is disposed extending along a
10 second direction.

8. (original) The method of claim 7, wherein the first direction is orthogonal to the
second direction.

15 9. (original) The method of claim 1, wherein the gate layer comprises amorphous
silicon.

10. (original) The method of claim 1, wherein the gate layer comprises polysilicon.

20 11. (original) The method of claim 1, wherein the dielectric layer comprises silicon
nitride.

12. (original) The method of claim 1, wherein the dielectric layer comprises silicon
oxide.

25

13. (withdrawn) A semiconductor device, comprising:

a fin-shaped structure on a substrate;

a single diffusion break (SDB) structure in the fin-shaped structure to divide the
fin-shaped structure into a first portion and a second portion;

30 a gate structure on the first portion; and

a contact etch stop layer (CESL) adjacent to the gate structure and extending to cover the SDB structure.

14. (withdrawn) The semiconductor device of claim 13, further comprising:

- 5 a first spacer on sidewalls of the gate structure; and
 a second spacer on sidewalls of the SDB structure, wherein the CESL is disposed on the first spacer and the second spacer.

15. (withdrawn) The semiconductor device of claim 14, further comprising a
10 source/drain region in the substrate adjacent to two sides of the first spacer.

16. (withdrawn) The semiconductor device of claim 14, further comprising a source/drain region in the substrate adjacent to two sides of the second spacer.

15 17. (withdrawn) The semiconductor device of claim 13, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.

 18. (withdrawn) The semiconductor device of claim 17, wherein the first direction is
20 orthogonal to the second direction.

Electronic Acknowledgement Receipt	
EFS ID:	30723512
Application Number:	15660991
International Application Number:	
Confirmation Number:	8497
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hao Lin
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Anna Lu
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	NAUP3064USA
Receipt Date:	24-OCT-2017
Filing Date:	27-JUL-2017
Time Stamp:	03:07:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2985424.PDF	581911 32666e88efad96aa6c9b02271d1c53db52b8802b	no	1

Warnings:

Information:					
2	Response to Election / Restriction Filed	2985423.PDF	74437	no	1
			1d126631d28a2ab1f84cdf1e192553bc8019ee1c		
Warnings:					
Information:					
3	Claims	2985422.PDF	77956	no	3
			05f76f2959c3b2ce31e28c12e533ec75815fbd99		
Warnings:					
Information:					
Total Files Size (in bytes):			734304		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application
5 by electronic mail. I understand that a copy of these communications will be made of record in the application file.

In response to the Election/Restriction requirement in the above-identified Office action, applicant hereby elects Invention II (claims 1-12) as the subject matter to be
10 examined in the present application. Claims 13-18 are withdrawn without prejudice or disclaimer to the merits thereof, as the applicant still reserves the right of filing divisional application(s) for prosecution of the non-elected species. No new claims are added in this reply.

15 Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

20 /Winston Hsu/ Date: 10/22/2017
Winston Hsu, Patent Agent No. 41,526
5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
25 e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

30

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 15/660,991		Filing Date 07/27/2017		☐ To be Mailed	
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ENTITY: ☒ **LARGE** ☐ **SMALL** ☐ **MICRO**

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	10/24/2017	CLAIMS REMAINING AFTER AMENDMENT					
	Total (37 CFR 1.16(i))	* 18	Minus	** 18	= 0	x \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***2	= 0	x \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
		CLAIMS REMAINING AFTER AMENDMENT					
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE							

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

LIE
ANTHONY TYSON



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/660,991	07/27/2017	Chun-Hao Lin	NAUP3064USA	8497
27765 7590 11/13/2017 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., No.389, Fuhe Rd., Yonghe Dist. New Taipei City, TAIWAN			EXAMINER AHMED, SHAHED	
			ART UNIT 2823	PAPER NUMBER
			NOTIFICATION DATE 11/13/2017	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 15/660,991	Applicant(s) LIN ET AL.	
	Examiner SHAHED AHMED	Art Unit 2823	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/24/2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-18 is/are pending in the application.
5a) Of the above claim(s) 13-18 is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-12 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 07/27/2017 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some** c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 07/27/2017.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

Art Unit: 2823

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

This action is responsive to application No. 15660991 filed on 07/27/2017.

Information Disclosure Statement

Acknowledgment is made of Applicant's Information Disclosure Statement (IDS) form PTO-1449. These IDS has been considered.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

Applicant's election without traverse of claims 1-12 in the reply filed on 10/24/2017 is acknowledged.

Notice re prior art available under both pre-AIA and AIA

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1-3, 5-11 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Xie et al. (US 2017/0243790).

Regarding independent claim 1, Xie et al. teach a method comprising:

forming a fin-shaped structure (Fig. 2A, element 205, paragraph 0020) on a substrate (Fig. 2A, element 210, paragraph 0020);

forming a shallow trench isolation (STI) (Fig. 2A, element 225, paragraph 0028) around the fin-shaped structure;

forming a gate layer (Fig. 2A, element 215, paragraph 0030) on the fin-shaped structure and the STI;

removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench (Figs. 2D-2F, element 265, paragraph 0025-0028); and

forming a dielectric layer (Fig. 2G, element 275, paragraph 0029) into the trench to form a single diffusion break (SDB) structure (Fig. 2G, element 272, paragraph 0029).

Regarding claim 2, Xie et al. teach further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer (paragraph 0023).

Regarding claim 3, Xie et al. teach further comprising: forming a patterned mask (Fig. 2B, element 250, paragraph 0024) on the gate layer; and using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench (Figs. 2D-2F, paragraph 0024-0028).

Regarding claim 5, Xie et al. teach further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure (Figs. 2I-2J, paragraph 0031-0032 disclose replacement gate process after the SDB structure 272 are formed).

Regarding claim 6, Xie et al. teach further comprising: forming a cap layer (Figs. 2A & 2G, element 235, paragraph 0023) on the gate structure and the SDB structure; and removing part of the cap layer to form a first spacer (Figs. 2A & 2J disclose removing part of element 235 and forming spacers 230 adjacent the gate and SDB) adjacent to the gate structure and a second spacer adjacent to the SDB structure.

Regarding claim 7, Xie et al. teach wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction (Fig. 2J).

Regarding claim 8, Xie et al. teach wherein the first direction is orthogonal to the second direction (Fig. 2J).

Regarding claim 9, Xie et al. teach wherein the gate layer comprises amorphous silicon (paragraph 0023).

Regarding claim 10, Xie et al. teach wherein the gate layer comprises polysilicon (paragraph 0005).

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Regarding claim 11, Xie et al. teach wherein the dielectric layer comprises silicon nitride (paragraph 0029).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 12 are rejected under 35 U.S.C. 103 as being unpatentable over Harada Xie et al. (US 2017/0243790).

Regarding claim 4, Xie et al. teach forming the dielectric layer into the trench and on the gate layer (Fig. 2G, paragraph 0029); and planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar (Fig. 4 and paragraph 0029 discloses that the dielectric layer and gate structure (including cap layer 235) are coplanar due to a planarization process. Accordingly, it would be a prima facie case of obviousness to planarize the dielectric layer such that the dielectric layer is coplanar with the gate layer 215).

Regarding claim 12, Xie et al. teach wherein the dielectric layer comprises silicon oxide (paragraph 0029 discloses the dielectric material can be formed by any known insulating material. Accordingly, It would have been obvious to one having ordinary skill in the art before the effective filling date of the invention to select a known insulating material silicon oxide as shown in paragraph 0005, since it has been held to

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be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art. In re Leshin, 125 USPQ 416).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAHED AHMED whose telephone number is (571)272-3477. The examiner can normally be reached on M-F 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SHAHED AHMED/

Examiner, Art Unit 2823

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/SHAHED AHMED/
Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 15/660,991		Applicant(s)/Patent Under Reexamination LIN ET AL.	
	Examiner SHAHED AHMED		Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2017/0243790 A1	08-2017	Xie; Ruilong	H01L21/823431	1/1
*	B	US-2017/0287933 A1	10-2017	CHEN; Xiangdong	H01L27/11807	1/1
*	C	US-9,368,496 B1	06-2016	Yu; Hong	H01L27/0886	1/1
*	D	US-9,524,911 B1	12-2016	Tsai; Hao-Cheng	H01L29/401	1/1
*	E	US-8,609,510 B1	12-2013	Banna; Srinvasa	H01L29/66545	257/E21.409
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Chun-Hao Lin
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP3064USA

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8502316		2013-08-06	Fung et al.	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20140027820		2014-01-30	Aquilino et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.A/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Chun-Hao Lin
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP3064USA

	1		
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

11/03/2017

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.A/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Chun-Hao Lin
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP3064USA

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2017-07-26
Name/Print	Winston Hsu	Registration Number	41526

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.A/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	14021	H01L21/823431.cpc. or H01L21/823437.cpc. or H01L21/823481.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:31
L4	54	L3 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:32
L5	21667	H01L21/308.cpc. or H01L21/31051.cpc. or H01L21/31144.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:33
L6	18	L5 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:34
L7	35394	H01L29/66545.cpc. or H01L21/76224.cpc. or H01L21/823475.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:35
L8	61	L7 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:35
L9	5372	H01L 29/66795.cpc. or H01L27/11807.cpc. or H01L29/0642.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
L10	6	L9 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
L11	19376	257/288,368,369.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
L12	3	L11 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
L13	16634	438/151,197,199.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38
L14	1	L13 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38

L15	246	(diffusion break or SDB or DDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38
L16	39	(diffusion break or SDB or DDB) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38
L17	70	(diffusion break or SDB or DDB) and (fin or mandrel) and (dummy or replacement) gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:40
S1	0	"15660991"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 11:55
S2	12	((("LIN") near3 ("Chun-Hao")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/11/02 12:43
S3	148	((("CHEN") near3 ("Hsin-Yu")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/11/02 12:44
S4	14	((("HSI EH") near3 ("Shou-Wei")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/11/02 12:44
S5	16550	UNITED MICROELECTRONICS CORP.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 12:44
S6	2	S5 and (diffusion break or SDB) and (fin or mandrel) and gate and STI	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 12:46
S7	2	("20140027820" "8502316").PN.	US-PGPUB; USPAT	ADJ	ON	2017/11/02 12:47
S8	29	(diffusion break or SDB) and (fin or mandrel) and gate and STI	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 13:23

EAST Search History (Interference)

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11/ 3/ 2017 10:49:45 AM**C:\ Users\ sahed3\ Documents\ EAST\ Workspaces\ 15660991.wsp**



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BIB DATA SHEET

CONFIRMATION NO. 8497

SERIAL NUMBER 15/660,991	FILING or 371(c) DATE 07/27/2017 RULE	CLASS 257	GROUP ART UNIT 2823	ATTORNEY DOCKET NO. NAUP3064USA	
APPLICANTS UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN; INVENTORS Chun-Hao Lin, Kaohsiung City, TAIWAN; Hsin-Yu Chen, Nantou County, TAIWAN; Shou-Wei Hsieh, Hsinchu City, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** CHINA 201710516576.7 06/29/2017 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/02/2017					
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/SHAHED AHMED/</u> Examiner's Signature	☐ Met after Allowance SA <u>SA</u> Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 5	TOTAL CLAIMS 18	INDEPENDENT CLAIMS 2
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., No.389, Fuhe Rd., Yonghe Dist. New Taipei City, TAIWAN					
TITLE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME					
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 15660991	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner SHAHED AHMED	Art Unit 2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L21/823431, H01L21/823437, H01L21/823481, H01L21/308	11/3/2017	SA
H01L21/31051, H01L21/31144, H01L29/66545, H01L21/76224	11/3/2017	SA
H01L21/823475, H01L 29/66795, H01L27/11807, H01L29/0642	11/3/2017	SA

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	288,368,369	11/3/2017	SA
438	151,197,199	11/3/2017	SA

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
searched EAST, Google, inventor, assignee	11/3/2017	SA
US class/subclass and CPC group/subgroup limited with text search (see EAST notes for details)	11/3/2017	SA

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/SHAHED AHMED/ Examiner.Art Unit 2823	
--	--

**SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE
SAME**

Appl. No. : 15/660,991 Confirmation No. 8497
First Named Inventor : Chun-Hao Lin
Filed : July 27, 2017
TC/A.U. : 2823
Examiner : AHMED, SHAHED
Docket No. : NAUP3064USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

5 In response to the Office action of November 13, 2017, please amend the
above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on
page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

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Listing of Claims:

1. (currently amended) A method for fabricating semiconductor device, comprising:
forming a fin-shaped structure on a substrate;
10 forming a shallow trench isolation (STI) around the fin-shaped structure;
forming a gate layer on the fin-shaped structure and the STI;
removing part of the gate layer, part of the fin-shaped structure, and part of the
STI to form a trench; [[and]]
forming a dielectric layer into the trench to form a single diffusion break (SDB)
15 structure; and
after forming the SDB structure forming an interlayer dielectric (ILD) layer on
the SDB structure.
2. (original) The method of claim 1, further comprising forming a gate dielectric layer
20 on the fin-shaped structure before forming the gate layer.
3. (original) The method of claim 2, further comprising:
forming a patterned mask on the gate layer; and
using the patterned mask as mask to remove part of the gate layer, part of the
25 gate dielectric layer, and part of the fin-shaped structure to form the trench.
4. (original) The method of claim 1, further comprising:
forming the dielectric layer into the trench and on the gate layer; and
planarizing the dielectric layer so that the top surfaces of the dielectric layer and
30 the gate layer are coplanar.

5. (original) The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure.
- 5 6. (original) The method of claim 5, further comprising:
 forming a cap layer on the gate structure and the SDB structure; and
 removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer adjacent to the SDB structure.
- 10 7. (original) The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.
- 15 8. (original) The method of claim 7, wherein the first direction is orthogonal to the second direction.
9. (original) The method of claim 1, wherein the gate layer comprises amorphous silicon.
- 20 10. (original) The method of claim 1, wherein the gate layer comprises polysilicon.
11. (original) The method of claim 1, wherein the dielectric layer comprises silicon nitride.
- 25 12. (original) The method of claim 1, wherein the dielectric layer comprises silicon oxide.
13. (withdrawn) A semiconductor device, comprising:
 a fin-shaped structure on a substrate;
30 a single diffusion break (SDB) structure in the fin-shaped structure to divide the

fin-shaped structure into a first portion and a second portion;
a gate structure on the first portion; and
a contact etch stop layer (CESL) adjacent to the gate structure and extending to
cover the SDB structure.

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14. (withdrawn) The semiconductor device of claim 13, further comprising:
a first spacer on sidewalls of the gate structure; and
a second spacer on sidewalls of the SDB structure, wherein the CESL is disposed
on the first spacer and the second spacer.

10

15. (withdrawn) The semiconductor device of claim 14, further comprising a
source/drain region in the substrate adjacent to two sides of the first spacer.

16. (withdrawn) The semiconductor device of claim 14, further comprising a
15 source/drain region in the substrate adjacent to two sides of the second spacer.

17. (withdrawn) The semiconductor device of claim 13, wherein the fin-shaped
structure is disposed extending along a first direction and the SDB structure is
disposed extending along a second direction.

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18. (withdrawn) The semiconductor device of claim 17, wherein the first direction is
orthogonal to the second direction.

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Electronic Acknowledgement Receipt	
EFS ID:	31125265
Application Number:	15660991
International Application Number:	
Confirmation Number:	8497
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hao Lin
Customer Number:	27765
Filer:	Roger Gwan-Jye Chen/Jessie Su
Filer Authorized By:	Roger Gwan-Jye Chen
Attorney Docket Number:	NAUP3064USA
Receipt Date:	05-DEC-2017
Filing Date:	27-JUL-2017
Time Stamp:	22:41:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	3022661.PDF	589396	no	2
			Bd387faae1c39d8554f58cbab0432116fc54cc6c		

Warnings:

Information:					
2	Amendment/Req. Reconsideration-After Non-Final Reject	3022660.PDF	80904	no	1
			1cb2878e2731499491afeb2f03cbab085b7c13e1		
Warnings:					
Information:					
3	Claims	3022659.PDF	84678	no	3
			b3c722a374b5001ee0aea65f53608ff87f69e8d		
Warnings:					
Information:					
Total Files Size (in bytes):			754978		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

Rejection of claims 1-3, 5-11 under 35 U.S.C. 102(a)(1) as being anticipated by Xie et al. (US 2017/0243790).

Claim 1 has been amended to specify that after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure.

Xie in Fig. 2G of the cited reference teaches the step of forming a dielectric layer into the trench to form a SDB structure (272). Xie however fails to disclose that an ILD layer is formed on the SDB structure (272) after forming the SDB structure (272), as recited in the amended claim 1 of the present invention. Instead, the ILD layer (245) is formed before forming the SDB structure (272) and no ILD layer is formed on the SDB structure whatsoever.

Since the cited Xie reference fails to disclose the above features, the amended claim 1 is patentable over the cited prior art. As claims 2-3, 5-11 are dependent on claim 1, they should be allowable if claim 1 is allowed.

Rejection of claims 4, 12 under 35 U.S.C. 103 as being unpatentable over Xie et al. (US 2017/0243790).

Since claims 4, 12 are dependent on claim 1, they should be allowable if claim 1 is allowed.

Appl. No. 15/660,991
Reply to Office action of November 13, 2017

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

5 Sincerely yours,

/Winston Hsu/

Date: 12/05/2017

Winston Hsu, Patent Agent No. 41,526

5F., No.389, Fuhe Rd., Yonghe Dist., New Taipei City, Taiwan

10 Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in

15 D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 15/660,991	Filing Date 07/27/2017	☐ To be Mailed
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)					
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A			N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL		
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT	12/05/2017	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

LIE
DEBORAH POLLARD



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 02/05/2018
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN

EXAMINER

AHMED, SHAHED

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 02/05/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/660,991	07/27/2017	Chun-Hao Lin	NAUP3064USA	8497

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0	\$0	\$1000	05/07/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27765 7590 02/05/2018
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.
New Taipei City,
TAIWAN

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/660,991	07/27/2017	Chun-Hao Lin	NAUP3064USA	8497

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0	\$0	\$1000	05/07/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
AHMED, SHAHED	2823	257-401000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/660,991	07/27/2017	Chun-Hao Lin	NAUP3064USA	8497
27765 7590 02/05/2018 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION 5F., No.389, Fuhe Rd., Yonghe Dist. New Taipei City, TAIWAN			EXAMINER AHMED, SHAHED	
			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 02/05/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/660,991	Applicant(s) LIN ET AL.	
	Examiner SHAHED AHMED	Art Unit 2823	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 12/05/2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-12. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☒ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	

/SHAHED AHMED/ Primary Examiner, Art Unit 2823	
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The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restrictions

This application is in condition for allowance except for the presence of claims 13-18 directed to a non-elected device claims without traverse. Accordingly, claims 13-18 have been cancelled.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows: **Cancel claims 13-18.**

Allowability Notice

Claims 1-12 are allowed.

The following is an examiner's statement of reasons for allowance:

The Applicants' replies make evident the reasons for allowance, satisfying the "record as a whole" provision of the rule 37 CFR 1.104(e). Specifically, the substance of applicants' remarks, filed 12/05/2017 with the amended claims, are persuasive, as such the reasons for allowance are in all probability evident from the record and no statement is deemed necessary (see MPEP 1302.14).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submission should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAHED AHMED whose telephone number is (571)272-3477. The examiner can normally be reached on M-F 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

Application/Control Number: 15/660,991
Art Unit: 2823

Page 4

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SHAHED AHMED/

Primary Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 15/660,991		Applicant(s)/Patent Under Reexamination LIN ET AL.	
	Examiner SHAHED AHMED		Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2017/0243790 A1	08-2017	Xie; Ruilong	H01L21/823431	1/1
*	B	US-2017/0287933 A1	10-2017	CHEN; Xiangdong	H01L27/11807	1/1
*	C	US-9,368,496 B1	06-2016	Yu; Hong	H01L27/0886	1/1
*	D	US-9,524,911 B1	12-2016	Tsai; Hao-Cheng	H01L29/401	1/1
*	E	US-8,609,510 B1	12-2013	Banna; Srinvasa	H01L29/66545	257/E21.409
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	32	(single diffusion break or SDB or DDB) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 13:58
L5	44	(diffusion break or SDB or DDB) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:02
L6	12	L5 not L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:02
L7	14569	H01L21/823431.cpc. or H01L21/823437.cpc. or H01L21/823481.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:03
L8	22	L7 and (diffusion break or SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:03
L9	22323	H01L21/308.cpc. or H01L21/31051.cpc. or H01L21/31144.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:03
L10	8	L9 and (diffusion break or SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:03
L11	36504	H01L29/66545.cpc. or H01L21/76224.cpc. or H01L21/823475.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:04
L12	24	L11 and (diffusion break or SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:04
L13	5492	H01L 29/66795.cpc. or H01L27/11807.cpc. or H01L29/0642.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:08

L14	3	L13 and (diffusion break or SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:08
L15	19439	257/288,368,369.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:08
L16	2	L15 and (diffusion break or SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:08
L17	16657	438/151,197,199.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:09
L18	0	L17 and (diffusion break or SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:09
L20	4	(SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI) and (interlayer dielectric or ILD)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:10
L21	30	(SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2018/01/03 14:12
S1	0	"15660991"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 11:55
S2	12	((("LIN") near3 ("Chun-Hao")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/11/02 12:43
S3	148	((("CHEN") near3 ("Hsin-Yu")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/11/02 12:44
S4	14	((("HSIEH") near3 ("Shou-Wei")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/11/02 12:44
S5	16550	UNITED MICROELECTRONICS CORP.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 12:44
S6	2	S5 and (diffusion break or SDB) and (fin or mandrel) and gate and STI	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 12:46
S7	2	("20140027820" "8502316").PN.	US-PGPUB; USPAT	ADJ	ON	2017/11/02 12:47

S8	29	(diffusion break or SDB) and (fin or mandrel) and gate and STI	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/02 13:23
S9	14021	H01L21/823431.cpc. or H01L21/823437.cpc. or H01L21/823481.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:31
S10	54	S9 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:32
S11	21667	H01L21/308.cpc. or H01L21/31051.cpc. or H01L21/31144.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:33
S12	18	S11 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:34
S13	35394	H01L29/66545.cpc. or H01L21/76224.cpc. or H01L21/823475.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:35
S14	61	S13 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:35
S15	5372	H01L 29/66795.cpc. or H01L27/11807.cpc. or H01L29/0642.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
S16	6	S15 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
S17	19376	257/288,368,369.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
S18	3	S17 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:37
S19	16634	438/151,197,199.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38

EAST Search History

S20	1	S19 and (diffusion break or SDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38
S21	246	(diffusion break or SDB or DDB) and (fin or mandrel) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38
S22	39	(diffusion break or SDB or DDB) and (fin or mandrel) and gate and (shallow trench isolation or STI)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:38
S23	70	(diffusion break or SDB or DDB) and (fin or mandrel) and (dummy or replacement) gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2017/11/03 10:40

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L19	0	((SDB or single diffusion break) and (fin or mandrel) and gate and (shallow trench isolation or STI) and (interlayer dielectric or ILD)).clm.	US-PGPUB; USPAT	ADJ	ON	2018/01/03 14:10

1/ 3/ 2018 2:36:34 PM

C:\Users\sahmed3\Documents\EAST\Workspaces\15660991.wsp

Issue Classification 	Application/Control No. 15660991	Applicant(s)/Patent Under Reexamination LIN ET AL.	
	Examiner SHAHED AHMED	Art Unit 2823	

CPC					
Symbol				Type	Version
H01L	21	/	823481	F	2013-01-01
H01L	21	/	76224	I	2013-01-01
H01L	29	/	66795	I	2013-01-01
H01L	29	/	66545	I	2013-01-01
H01L	21	/	823475	I	2013-01-01
H01L	21	/	31144	I	2013-01-01
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
		12	
(Assistant Examiner)	(Date)		
/SHAHED AHMED/ Primary Examiner.Art Unit 2823	01/03/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	10

Issue Classification 	Application/Control No. 15660991	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner SHAHED AHMED	Art Unit 2823

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION											
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED						
						H	O	I	L	29 / 76 (2006.01.01)							
CROSS REFERENCE(S)																	
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																
								</									

NONE		Total Claims Allowed:	
		12	
(Assistant Examiner)	(Date)		
/SHAHED AHMED/ Primary Examiner.Art Unit 2823	01/03/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	10

Search Notes 	Application/Control No. 15660991	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner SHAHED AHMED	Art Unit 2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L21/823431, H01L21/823437, H01L21/823481, H01L21/308	1/3/2018	SA
H01L21/31051, H01L21/31144, H01L29/66545, H01L21/76224	1/3/2018	SA
H01L21/823475, H01L 29/66795, H01L27/11807, H01L29/0642	1/3/2018	SA

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	288,368,369	1/3/2018	SA
438	151,197,199	1/3/2018	SA

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
searched EAST, Google, inventor, assignee	1/3/2018	SA
US class/subclass and CPC group/subgroup limited with text search (see EAST notes for details)	1/3/2018	SA
updated search	1/3/2018	SA

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	see EAST notes for inventor and claims search	1/3/2018	SA

/SHAHED AHMED/ Examiner.Art Unit 2823	/SHAHED AHMED/ Primary Examiner.Art Unit 2823
--	--

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS: (Note: Use Block 1 for any change of address.)

27765 7590 02/05/2018

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
5F., No.389, Fuhe Rd., Yonghe Dist.,
New Taipei City,
Taiwan

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Hitomi Lin	(Depositor's name)
/Hitomi Lin/	(Signature)
03/20/2018	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/660.991	07/27/2017	Chun-Hao Lin	NAUP3064USA	8497

TITLE OF INVENTION: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0	\$0	\$1000	05/07/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
AHMED, SHAHED	2823	257-401000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 Winston Hsu
 (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

UNITED MICROELECTRONICS CORP. Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-3105 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Winston Hsu/

Date 03/18/2018

Typed or printed name Winston Hsu

Registration No. 41526

Electronic Patent Application Fee Transmittal				
Application Number:		15660991		
Filing Date:		27-Jul-2017		
Title of Invention:		SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME		
First Named Inventor/Applicant Name:		Chun-Hao Lin		
Filer:		Winston Hsu/Hitomi Lin		
Attorney Docket Number:		NAUP3064USA		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt	
EFS ID:	32084234
Application Number:	15660991
International Application Number:	
Confirmation Number:	8497
Title of Invention:	SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME
First Named Inventor/Applicant Name:	Chun-Hao Lin
Customer Number:	27765
Filer:	Winston Hsu/Hitomi Lin
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP3064USA
Receipt Date:	20-MAR-2018
Filing Date:	27-JUL-2017
Time Stamp:	01:42:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	032018INTEFSW00008239503105
Deposit Account	503105
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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	3104812.PDF	154603	no	1
			684c17fe9eb5b11818e777395cac62da7878ebe0		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30366	no	2
			bc7efbabb121c655f6db6522bb0249e971593ccc		
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/660,991	04/24/2018	9953880	NAUP3064USA	8497

27765 7590 04/04/2018
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

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