

SEMICONDUCTOR MANUFACTURING TECHNOLOGY

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ADVANCED MICRO DEVICES



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Thin Film Metallization Work Bay
(Photo courtesy of Advanced Micro Devices)

CMOS MANUFACTURING STEPS

The remainder of this chapter focuses on the manufacturing steps that a wafer follows in a typical CMOS process. Although there are some operations in the process flow that can be performed in batches of wafers at one time, this process flow describes the manufacturing of a single wafer. For further simplification, this process describes the production of only a microscopic area of a single CMOS inverter consisting of two transistors—nMOS and pMOS. Cross-sectional views of the product will be provided for each major operation.

The CMOS manufacturing steps to be described are:

1. Twin Well Process
2. Shallow Trench Isolation Process
3. Poly Gate Structure Process
4. Lightly Doped Drain (LDD) Implant Processes
5. Sidewall Spacer Formation
6. Source/Drain (S/D) Implant Processes
7. Contact Formation
8. Local Interconnect Processes
9. Via-1 and Plug-1 Formation
10. Metal-1 Interconnect Formation
11. Via-2 and Plug-2 Formation
12. Metal-2 Interconnect Formation
13. Metal-3 to Pad Etch and Alloy
14. Parametric Testing

1. Twin Well Process

The first step in some CMOS wafer fabrication processes is to define the active regions of the MOSFETs. Many of today's sub-quarter micron processes use a *twin-well* (also referred to as *twin-tub*) approach to define the active regions of the nMOS and pMOS transistors. A twin-well consists of a p-well and an n-well, with each well requiring at least three to five major processing steps to fabricate. A *retrograde implant* technique is used to obtain optimum electrical characteristics for the FETs. This technique starts with a high-energy, high-dose implant that penetrates approximately 1 μm into the epilayer. Subsequent well implants are done at the same active site with a progressive

decrease in energy, junction depth, and dose of dopant material such as phosphorus or boron (measured in atoms/cm²). The results help set the threshold operating voltage for the FETs as well as prevent common CMOS problems, such as *latchup* and other reliability issues. Figure 9.8 and Figure 9.9 illustrate, respectively, the major steps required in the formation of the n-well and p-well.

n-well Formation ■ The five major steps in n-well formation are described below in the following process and illustrated in Figure 9.8.

Description of Five Major Steps in n-well Formation

Process Step	Description
1. Epitaxial Growth	The silicon wafer, having already a thin layer of <i>epitaxial</i> silicon (epilayer), arrives in the diffusion bay. The epilayer has the exact crystal structure as the substrate, except with improved purity and fewer crystal defects. The epilayer has already been lightly doped with p-type dopant (boron).
2. Initial Oxide Growth	In diffusion the wafer is cleaned in a series of chemical baths to remove particles, organic and inorganic contamination, and <i>native oxide</i> growth (natural silicon dioxide growth) from the wafers. After the wafer is rinsed and dried, the wafer is placed in a high temperature (~1000 °C) furnace process chamber. Oxygen is flowed into the process chamber to react with silicon to grow approximately 150 Å of oxide. This initial oxide serves several functions: (1) it protects the top surface of the epi silicon from contamination, (2) it prevents excessive damage to the silicon during implantation, and (3) as a screen oxide, it helps control the depth of the dopants during implantation.
3. 1st Mask, n-well Implant	In photolithography the wafer undergoes a series of process steps in the coater/developer track tool. The “tracks,” as commonly referred to, prime the top surface of the wafer, coat the wafer with photoresist (liquid photographic film), spin the wafer, and bake the wafer. An internal automatic wafer-handling system transfers the wafer between process stations within the tracks. Another wafer handler removes resist-coated wafers, one at a time, and transfers them to the <i>alignment-and-exposure system</i> (an extremely complex and precise camera). The alignment-and-exposure system photographs the image of a specific mask layer directly onto the resist-coated wafer. In this case, the mask layer defines the areas of the product that are to be implanted in order to form the n-wells for the pMOS transistors. The exposed wafer is then transferred back to the tracks, where the image first appears when the wafer is sprayed with the chemical developer. The developed wafer undergoes another bake step and is inspected before being transferred to the ion implant bay. The printed pattern is inspected for proper <i>linewidths</i> , called <i>critical dimensions</i> (CD). In the event of a major defect, the photoresist can be stripped off and the wafer can then be reworked. Photolithography is the only area in the fab where a wafer can be easily reworked.
4. n-well Implant (High energy)	The patterned wafer arrives in the ion implant bay. The photoresist pattern covers specific areas of the wafer that are to be protected from ion implantation. Windows, or openings, in the photoresist allow high-energy positive dopant ions to penetrate into the upper surface of the epilayer (~1 μm <i>junction depth</i>). In this case, phosphorus is the desired dopant. The <i>ion implanter</i> is the main process tool in this bay. Its purpose is to ionize dopant atoms, accelerate them with high voltage (~200 KeV), select the most appropriate dopant species to implant, focus the ions into a narrow beam, and, finally, scan the wafer to provide uniform doping across all unprotected areas of the wafer. At this point the dopant ions penetrate the crystal lattice of the silicon causing damage to the covalent atomic structure. This damage will be repaired later in a diffusion and annealing step. <i>Note:</i> After each ion implant operation, an oxygen-plasma reactor tool strips the photoresist off each implanted wafer. The wafer is then cleaned by a wet chemical process to remove residual photoresist and polymers created by the plasma process. This note applies to all subsequent implant operations but will be listed only this one time.
5. Anneal	The implanted wafer is transferred to diffusion where the wafer is cleaned before being inserted into an <i>anneal</i> furnace. Four things occur as a result of this anneal process. (1) A new barrier oxide layer is grown over the bare silicon. (2) The higher temperatures cause the movement of dopants further into the silicon (called diffusion). (3) The implant damage is repaired. (4) The bonds between the dopant atoms and the silicon atoms are activated, making the dopant atoms a part of the crystal lattice structure (electrical activation).

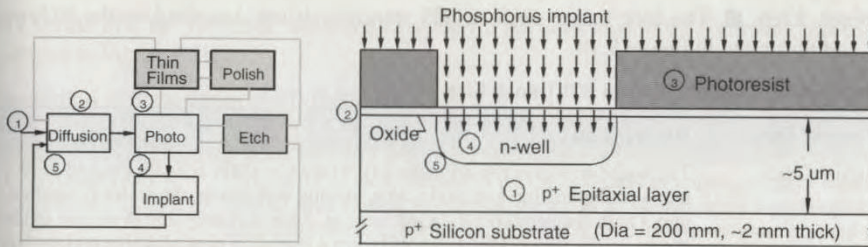


FIGURE 9.8 n-well Formation

p-well Formation ■ The three major steps in p-well formation are described in the following process and illustrated in Figure 9.9.

Description of Three Major Steps in p-well Formation

Process Step	Description
1. 2nd Mask, p-well Implant	The photolithography steps for the p-well implant mask are exactly the same as for the first mask. The only difference is the mask is the direct opposite of the n-well implant mask. Compare Figure 9.8 and Figure 9.9 to see the differences.
2. p-well Implant (High energy)	The retrograde p-well implant energy levels are considerably lower than the n-well. This condition is due to the difference in the masses of the elements being implanted. Comparing the atomic mass unit (amu) of boron (~11) to phosphorus (~31), boron is about one-third the mass of phosphorus. Thus, the energy needed to implant boron should only require about one-third of that used to implant phosphorus to the same junction depth.
3. Anneal	This anneal step is basically the same as the first annealing step.

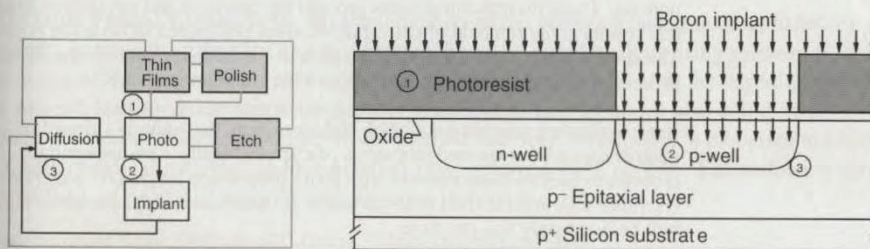


FIGURE 9.9 P-well Formation

2. Shallow Trench Isolation Process

Shallow trench isolation (STI) is an alternative method for creating isolation regions between active transistor areas on a substrate.¹ This method is especially useful in the manufacturing of quarter-micron devices. The preferred isolation technique up until the late 1990s had been the LOCOS (local oxidation of silicon) technique that was instituted in the early 1970s.² Despite its complexity, STI is gaining in popularity with ULSI chip manufacturing. STI formation is explained as follows in three major steps: trench etch (see Figure 9.10 on page 208), oxide fill (see Figure 9.11 on page 209), and oxide polish (see Figure 9.12 on page 209).

STI Trench Etch ■ The four major steps in STI trench etch are described in the following process and illustrated in Figure 9.10.

Description of Four Major Steps in STI Trench Etch

Process Step	Description
1. Barrier Oxide	The wafer arrives in the diffusion bay where the wafer is again cleaned to remove contamination and oxide. After rinsing and drying, the wafer is inserted into a high-temperature oxidation furnace. Approximately 150 Å of new oxide is grown on the wafer. This layer will form a barrier to protect active regions from chemical contamination during nitride strip.
2. Nitride Deposition	The wafer is inserted into a high-temperature (~750 °C) <i>LPCVD</i> (<i>low-pressure chemical vapor deposition</i>) furnace. Inside the process chamber ammonia and dichlorosilane gases react to form a thin layer of silicon nitride (nitride, Si_3N_4) on the wafer. The nitride will serve two functions throughout the STI formation process steps. (1) Nitride is a durable masking material, which protects active regions during the STI oxide deposition process and (2) nitride serves as a polish-stop material during the chemical mechanical planarization (CMP) step.
3. 3rd Mask, STI	The wafer arrives in photolithography from diffusion. This photolithography process step is similar to the previous masking step, except a different mask is used. This masking step is much more critical than the first mask due to the smaller dimensions. Inspection of the wafer includes CD measurements as well as checking for <i>defect inspection</i> (DI), and optical <i>visual inspection</i> (VI). These measurements require checking the accuracy of the alignment-exposure system relative to the written specifications.
4. STI Trench Etch	The photoresist pattern is designed to protect areas of the silicon that are not to be etched. The windows in the photoresist allow ions and highly reactive <i>radical chemicals</i> to etch nitride, oxide, and silicon in unprotected areas. The preferred tool for etching these deep trenches is the <i>dry plasma etcher</i> . The etcher uses high-powered radio frequency (RF) energy to ionize a fluorine- or chlorine-based gas inside a vacuum process chamber. The RF energy dissociates molecules and ionizes atoms to create a chamber filled with a variety of plasma components. These plasma components provide the chemical and physical etching that results in the removal of silicon in locations designated as <i>isolation regions</i> . The slanted profile and the rounded bottom of the trenches improve the filling process and the electrical characteristics of the isolation structure.

Note: Following completion of each etch operation, the wafer is stripped of photoresist and wet cleaned in a series of chemical baths. Key inspection procedures include measurements that verify proper step height (Å), etch rate (Å/min), CD, and DI. This note applies to all subsequent etch operations but will be listed only this one time.

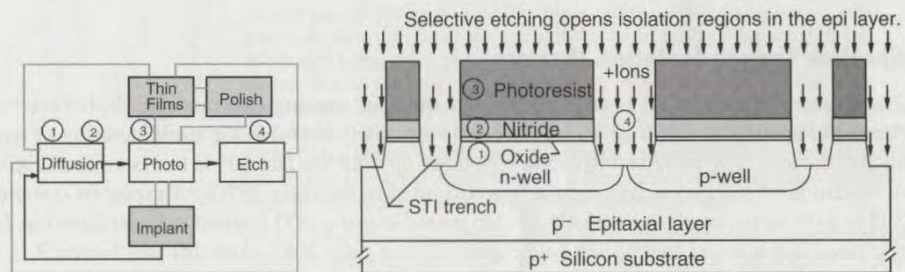


FIGURE 9.10 STI Trench Etch

STI Oxide Fill ■ The basic steps in STI oxide fill are described in the following process and illustrated in Figure 9.11.

Description of Basic Steps in STI Oxide Fill

Process Step	Description
1. Trench Liner Oxide	The wafer is again cleaned in the diffusion bay to remove contamination and oxide. After rinsing and drying, the wafer is inserted into a high-temperature oxidation furnace. Approximately 150 Å of oxide grows in the exposed walls of the isolation trenches. The nitride mask prevents oxygen diffusion into the active regions. The purpose of the liner oxide is to improve the interface between the silicon and the trench CVD oxide.
2. Trench Fill with CVD Oxide	This deposition process is performed either in diffusion using an LPCVD furnace or in thin films using a variety of oxide CVD systems. Higher throughput and deposition rates are obtained with the furnace.

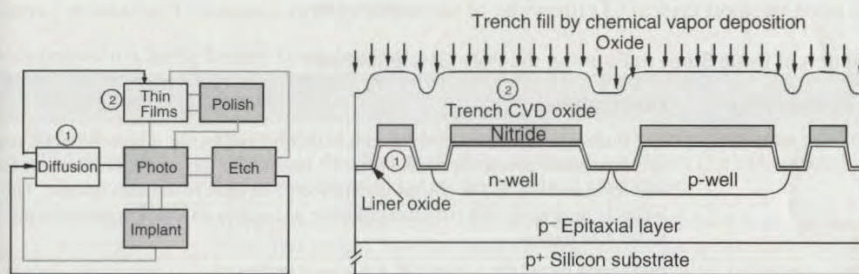


FIGURE 9.11 STI Oxide Fill

STI Oxide Polish-Nitride Strip ■ Planarization of the wafer surface is accomplished by several methods. In the past, filling the gap to planarize the wafer could be done using *spin-on-glass (SOG)*, consisting of 80% solvent and 20% silicon dioxide. Baking the SOG after the deposition evaporated the solvent, leaving oxide inside the gaps. A complete surface *etchback* also could be performed to reduce the overall thickness. However, no method has been as effective a planarization technique as CMP, chemical mechanical planarization (also referred to as *polish*). The following table and Figure 9.12 on page 210 describe and illustrate the process.

Description of Basic Steps in STI Oxide Polish and Nitride Strip

Process Step	Description
1. Trench Oxide Polish (CMP)	In the CMP area the wafer is turned upside down and held by vacuum to a wafer carrier. The wafer rotates in the same direction as a polishing pad attached to a rotating polishing table. A chemical slurry keeps the pad and wafer wet during the polishing process and provides reactants to help abrade the oxide surface. The nitride, being a harder material than the oxide, serves as the polish-stop material to prevent over-polishing the isolation structures. <i>Note:</i> The following statement applies to all polishing operations and will not be repeated again. The polishing process creates excessive particles and chemical contaminants that must be thoroughly removed before transferring the wafer to other areas in the wafer fab. Special scrub stations clean the top and bottom of the wafer and ensure it is rinsed and dried. Inspections for film thickness, particles, and defects are also conducted before wafer is transferred.
2. Nitride Strip	The diffusion bay is traditionally equipped with hot phosphoric acid stations for stripping the nitride from the wafer. In the diffusion bay the wafer is stripped, cleaned, rinsed, and dried, then inspected to check the thickness of the isolation oxide.

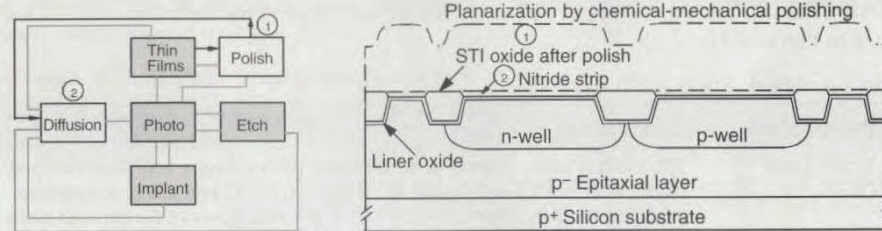


FIGURE 9.12 STI Formation

3. Poly Gate Structure Process

Forming the structure of the transistor gate is a critical step in the process because it includes thermally growing the thinnest *gate oxide* and patterning and etching the *polysilicon gate*, one of the smallest physical structures in the entire IC process (see Figure 9.13). The width of the polysilicon gate is often the most critical CD linewidth of the entire wafer.

Description of Basic Steps in Forming the Poly Gate Structure

Process Step	Description
1. Gate Oxide Growth	The wafer is cleaned to remove contamination and oxide. There is only a matter of a few hours before the wafer must be inserted in the oxidation furnace. Oxide will form as long as the silicon is exposed to oxygen in the atmosphere. The wafer is inserted in the oxidation furnace and a thin oxide of approximately 20 to 50 Å is grown.
2. Polysilicon Deposition	The wafer is immediately loaded into an LPCVD furnace where silane (SiH_4) is introduced into the process chamber. The silane dissociates and polysilicon is deposited on the wafer. Approximately 5000 Å of polysilicon (also referred to as poly) is deposited. Some processes may call for doping the polysilicon immediately following the deposition step. This action can be done in the same process chamber or in a separate furnace.
3. 4th Mask, Poly Gate	In photolithography, deep UV lithography (assuming sub-0.25 μm technology) techniques are used to pattern the fine structures of the polysilicon gates. An <i>antireflective coating</i> (ARC) is commonly applied between the poly and the photoresist to reduce undesirable reflections. The resist linewidths for the gates are the narrowest structures on the IC; therefore, various quality measurements are required, such as CD and overlay registration (OL), and defect inspection (DI).
4. Poly Gate Etch	By far one of the most critical etch steps in the IC process requires the use of the best <i>anisotropic plasma etchers</i> available in the fab. These single-direction etchers etch the polysilicon to provide the vertical profile as shown in Figure 9.13.

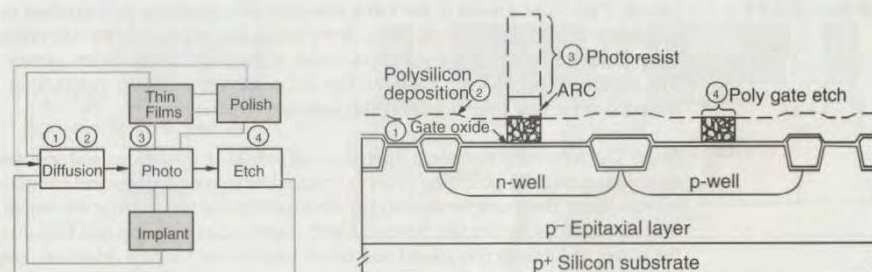


FIGURE 9.13 Poly Gate Structural Process

4. Lightly Doped Drain (LDD) Implant Process

As gate widths get smaller, the *channel length* below the gate structure (the silicon region between the source and drain) also decreases. This reduction increases the potential for charges to *punchthrough* the transistor source and drain and cause undesirable channel leakage current. There are techniques that are used to reduce the occurrence of this leakage in the channel.

The next series of ion implant steps begins to define the source and drain regions of transistors. Each pMOS and nMOS transistor will be implanted twice—once with a shallow implant called the *lightly doped drain (LDD) implant*, then followed by a medium or high dose *source/drain implant*. Lightly doped drain (LDD) implants (see Figure 9.14 below and Figure 9.15 on page 212) use the larger mass of arsenic and BF_3 dopant materials to create an *amorphous* (disorganized with no long-range order or crystal structure) upper layer of silicon. The combination of large mass and amorphous surface conditions helps maintain a shallow junction, which also helps reduce channel current leakage effects between the source and drain.

n⁻ LDD Implant ■ The steps for creating n⁻ lightly doped drain implants are described in the following process and illustrated in Figure 9.14.

Description of n- Lightly Doped Drain Implant

Process Step	Description
1. 5th Mask, n ⁻ LDD Implant	The purpose of this masking step is to pattern the wafer in a manner that opens windows in the photoresist where n-channel transistors can be implanted. All other areas are protected by the remaining photoresist.
2. n ⁻ LDD Implant (Low energy, shallow junction depth)	Arsenic ions are selectively implanted through the windows in the patterned resist. The energy, dose and depth are significantly lower than in the previous n-well implant steps. Arsenic is preferred over phosphorus because its larger mass amorphizes the silicon surface to create a more uniform dopant depth during implant.

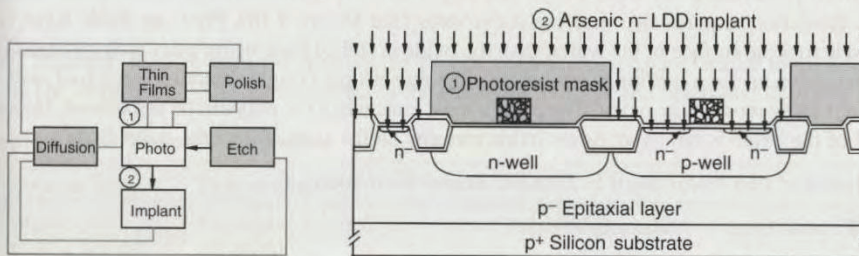


FIGURE 9.14 n⁻ LDD Implant

p⁻ LDD Implant ■ The steps for creating p⁻ lightly doped drain implants are described in the following process and illustrated in Figure 9.15.

Description of p- Lightly Doped Drain Implant

Process Step	Description
1. 6th Mask, p ⁻ LDD Implant	The purpose of this masking step is to pattern the wafer in a manner that opens windows in the photoresist where p-channel transistors can be implanted. All other areas are protected by the remaining photoresist.
2. p ⁻ LDD Implant (Low energy, shallow junction depth)	Boron difluoride, BF ₂ , is preferred over boron for this implant step. BF ₂ is a heavier substance than boron. The heavier BF ₂ helps amorphize the silicon surface.

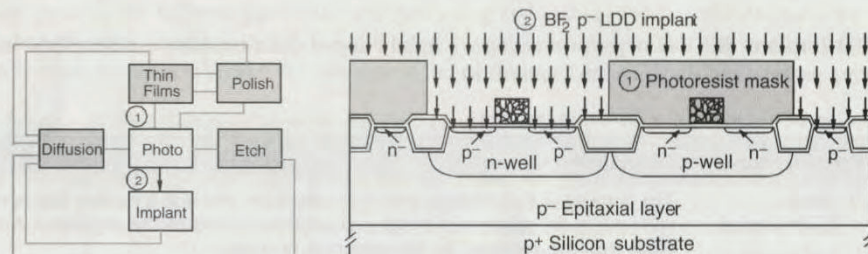


FIGURE 9.15 p⁻ LDD Implant

5. Sidewall Spacer Formation

Sidewall spacers will be used alongside the poly gates to prevent the higher source/drain (S/D) implant from penetrating too close to the channel where S/D punchthrough could occur. Sidewall spacer formation requires two major process steps (see Figure 9.16). First, an oxide layer is deposited across the surface of the wafer, then the oxide is etched back using a dry etch process. There is no requirement for a masking step because the anisotropic (single-direction) etch tool uses ions to sputter away most of the oxide. The etch process ends when the polysilicon is exposed. However, not all of the oxide is removed. Some oxide remains on the sidewalls of the polysilicon gates.

Description of Two Major Steps in Sidewall Spacer Formation

Process Step	Description
1. Spacer Oxide Deposition	This procedure is performed in the thin film bay. Approximately 1000 Å of oxide is deposited with a chemical vapor deposition (CVD) process. This layer will be used to form spacers on the sides of the polysilicon gates.
2. Spacer Oxide Etchback	The dry plasma etcher removes most of the CVD oxide leaving behind the thicker oxide on the sidewalls of the polysilicon gates.

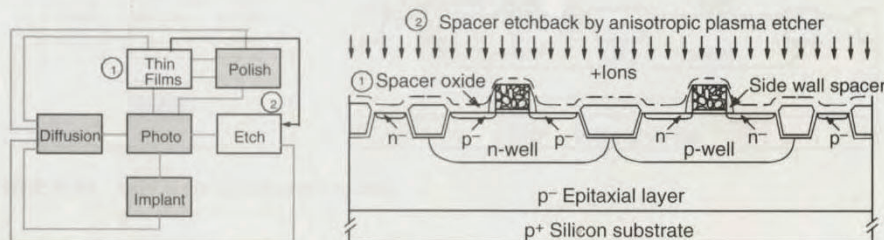


FIGURE 9.16 Sidewall Spacer Formation

6. Source/Drain (S/D) Implant Processes

To complete the retrograde implant technique, medium-dose implants are made to penetrate the silicon slightly beyond the LDD junction depth, but not as deep as the original twin-well implants (see Figure 9.17 and Figure 9.18). The spacer oxide from the previous step will protect the channel from the dopant atoms during the implant process.

n^+ S/D Implant ■ The steps for creating n^+ source/drain implants are described in the following process and illustrated in Figure 9.17.

Description of n^+ Source/Drain Implant

Process Step	Description
1. 7th Mask, n^+ S/D Implant	This masking step defines areas of the nMOS transistors that are to be implanted.
2. n^+ S/D Implant (Medium energy)	This is a medium-energy implant step that penetrates the silicon deeper than the LDD junction depth. Spacer oxide prevents the arsenic dopant from encroaching into the narrow channel.

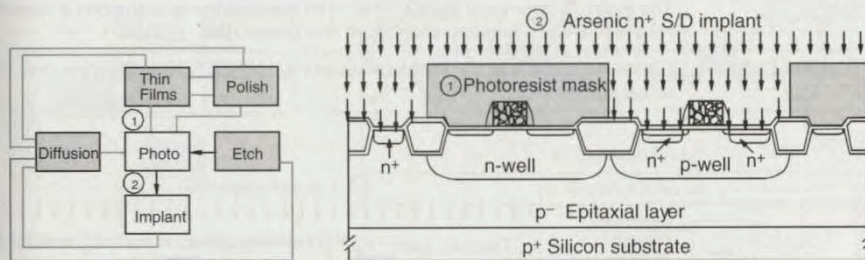


FIGURE 9.17 n^+ S/D Implant

p^+ S/D Implant ■ The steps for creating the p^+ source/drain regions are similar to n^+ S/D formation. The steps for p^+ S/D are described in the following process and illustrated in Figure 9.18.

Description of p^+ Source/Drain Implant

Process Step	Description
1. 8th Mask, p^+ S/D Implant	This masking step defines areas of the pMOS transistors that are to be implanted.
2. p^+ S/D Implant (Medium energy)	This implant step penetrates the silicon slightly beyond the LDD junction depth. Spacer oxide prevents boron dopant from encroaching into the narrow channel.
3. Anneal	The implanted wafer is annealed in a <i>rapid thermal process (RTP)</i> tool. RTP tools have the ability to quickly reach temperatures of $\sim 1000^\circ\text{C}$ and maintain the setpoint for several seconds. This condition is important to prevent structures from spreading and to control the diffusion of dopants in the S/D regions.

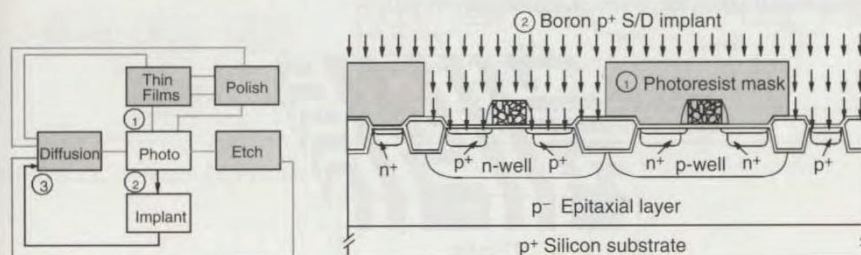


FIGURE 9.18 p^+ S/D Implant

7. Contact Formation

The purpose of the contact formation process steps is to form *metal contacts* on all active areas of silicon. These metal contacts serve to promote adhesion between the silicon and the metal conductor material that will be deposited later (see Figure 9.19). Titanium is a good choice for the metal contact material, although cobalt can also be used. Titanium has low resistivity characteristics and reacts very well with silicon. When raised to a temperature $>700^{\circ}\text{C}$, titanium bonds with silicon to form a *titanium silicide* (TiSi_2) compound, or *tisilicide*. Titanium and silicon dioxide do not react; therefore, no chemical bonding or physical connection is made between these two materials. Thus, titanium can be easily etched off the oxide without the need for a masking step. Tisilicide remains at all locations where active silicon exists (e.g. source, drain, and gate).

Description of Major Steps in Titanium Contact Formation

Process Step	Description
1. Titanium Deposition	The wafer is cleaned thoroughly to remove contaminants and oxides from the silicon. Titanium (Ti) is deposited on wafers using a sputtering process. <i>Sputtering</i> is a <i>physical vapor deposition (PVD)</i> process that is performed in a plasma process chamber where energetic argon ions bombard a metal target to release metal atoms, which deposit onto a wafer.
2. Anneal	The wafer is inserted in the RTP tool. The high temperature triggers a chemical reaction between titanium and silicon that forms TiSi_2 (tisilicide).
3. Titanium Etch	Chemicals etch away the unreacted titanium, leaving behind tisilicide over the active silicon areas.

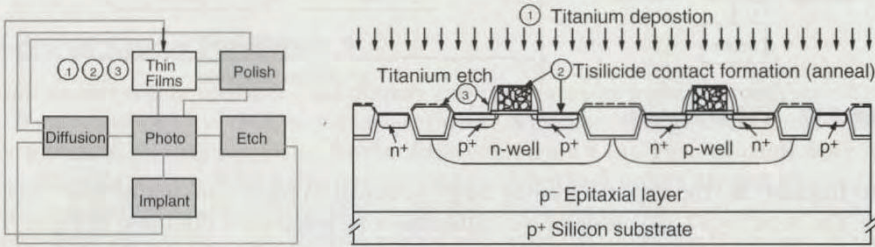


FIGURE 9.19 Contact Formation

8. Local Interconnect (LI) Process

The next step in the IC manufacturing process is to form metal connecting lines between transistors and other tisilicide contacts. The method used in this process flow is referred to as *local interconnect (LI)*. The steps leading up to the formation of LI are as complicated as the formation of the STI. The process begins with the deposition of dielectric films, followed by CMP, patterning, etch, and tungsten metal deposition and finished off with a metal polish (see Figure 9.20 and Figure 9.21). This process is referred to as *damascene*—a name adopted from a practice that began thousands of years ago by artisans in Damascus, Syria.³ The result of these steps produces a top surface that resembles intricate inlaid jewelry or artwork. The graphic in Figure 9.22 illustrates how the metal lines are formed within the walls of the etched oxide.

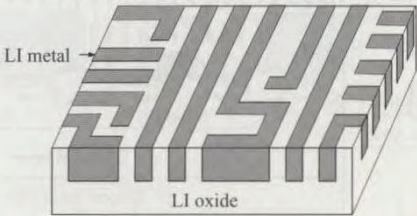


FIGURE 9.20 LI Oxide as a Dielectric for Inlaid LI Metal

Description of LI Oxide Dielectric Formation

Process Step	Description
1. Nitride (Si_3N_4) CVD	A barrier layer of silicon nitride is deposited using a CVD process. The nitride provides protection for the active regions from the dopants in the next film layer.
2. Doped Oxide CVD	The LI dielectric component of the local interconnect structure is formed from CVD oxide (SiO_2). This oxide is lightly doped with phosphorus or boron. The addition of dopants to the oxide improves the dielectric qualities of the glass. An additional RTP step allows the glass to flow and smooth the surface.
3. Oxide Polish (CMP)	CMP is used to planarize the LI oxide. The resulting thickness of the oxide after polish is $\sim 8000 \text{ \AA}$.
4. 9th Mask, LI Etch	The wafer is patterned in photolithography and then etched in the etch bay. Narrow trenches are created in the LI oxide that will serve as the forms for defining the paths for the LI metal.

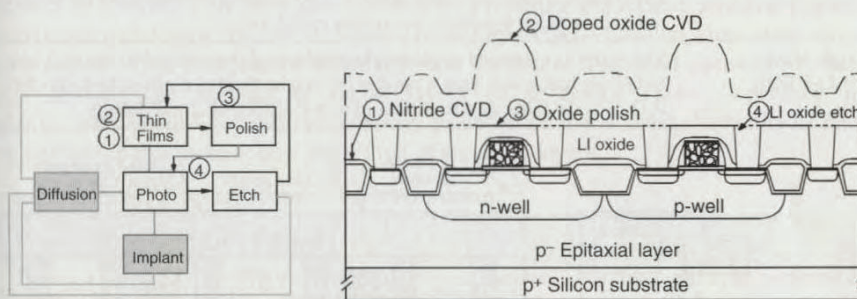


FIGURE 9.21 LI Oxide Dielectric Formation

Description of LI Metal Formation

Process Step	Description
1. Titanium Deposition (PVD process)	A thin barrier layer of titanium (Ti) lines the bottom and the inside of the LI walls. The Ti serves as a "double-adhesive tape" to hold the tungsten (W) to the SiO_2 .
2. Titanium Nitride Deposition	Titanium nitride (TiN) is deposited immediately over the Ti to serve as a diffusion barrier for the tungsten metal.
3. Tungsten Deposition (CVD process polish)	Tungsten fills the LI trenches and coats the entire wafer. Tungsten is preferred over aluminum for LI metal due to its ability to fill holes without leaving voids in the formed metal plug. Another reason is for its good polishing characteristics.
4. Tungsten polish	The tungsten is polished down to the upper surface of the LI oxide.

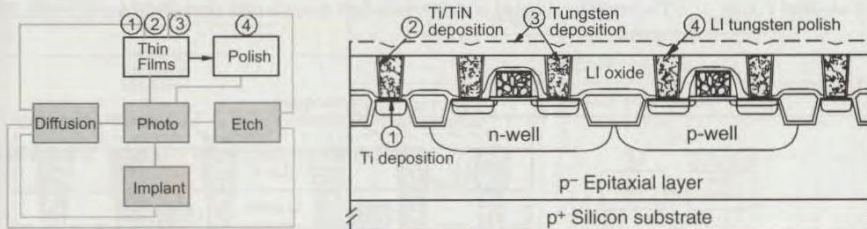


FIGURE 9.22 LI Metal Formation

9. Via-1 and Plug-1 Formation

The *interlayer dielectric (ILD)* serves as an insulator material between each metal layer or between the first metal layer and silicon. The ILD will have many small *vias*, which are small openings in the ILD that provide an electrical pathway from one metal layer to adjacent metal layers. Vias are filled with a conductive metal (usually tungsten, and referred to as a *tungsten plug*) and are placed at the appropriate locations to form the electrical circuit between metal layers (see Figure 9.23 and Figure 9.24). ILD-1 is the first of a series of interconnection process to be described.

Description of Major Steps in Via-1 Formation

Process Step	Description
1. ILD-1 Oxide Deposition (CVD)	Oxide is deposited across the surface of the wafer with a CVD tool in thin films. This layer (ILD-1) will serve as the dielectric material from which vias are to be formed.
2. Oxide Polish	CMP is used to planarize the ILD-1 oxide. The resulting thickness of the oxide after polish is approximately 8000 Å. The wafer is scrubbed and cleaned to remove particles generated during the polish step.
3. 10th Mask, ILD-1 Etch	The wafer is patterned in photolithography and then etched in the etch bay. Small via holes, less than a quarter micron in diameter, are etched into the ILD-1 oxide. This step is critical in terms of CD, OL, and defects.

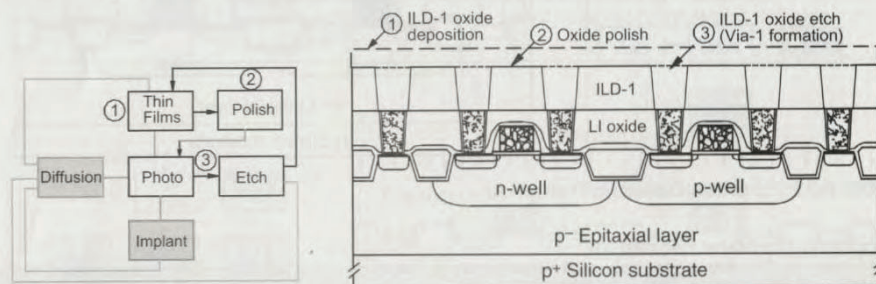


FIGURE 9.23 Via-1 Formation

Description of Major Steps in Plug-1 Formation

Process Step	Description
1. Titanium Barrier Metal Deposition (PVD)	A thin layer of titanium is deposited across the surface of the wafer with a PVD tool in thin films. Titanium lines the bottom and the walls of the via holes. The Ti serves as the glue that holds the tungsten plug inside the hole.
2. Titanium Nitride Deposition (CVD)	TiN is thinly deposited on top of the Ti layer. The TiN serves as a diffusion barrier for the tungsten in the next deposition step.
3. Tungsten Deposition (CVD)	Another CVD tool is used to deposit tungsten on the wafer. Tungsten fills the small openings to form the plug.
4. Tungsten Polish	The tungsten-coated wafer is polished down to the upper surface of the ILD-1 oxide.

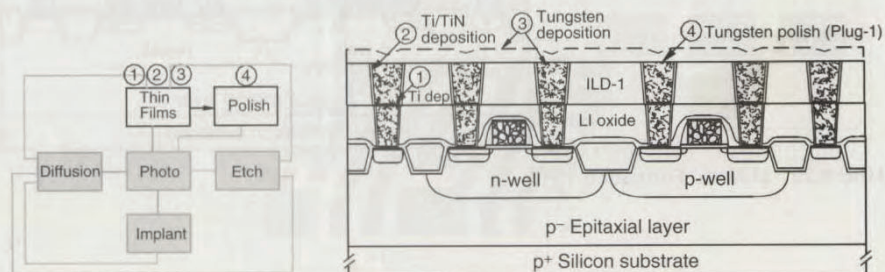
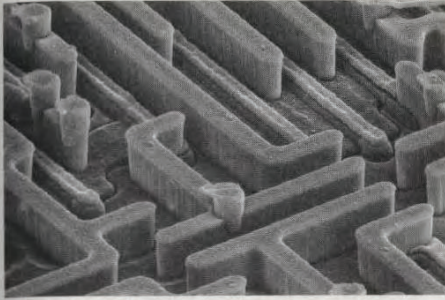


FIGURE 9.24 Plug-1 Formation



SEM Micrograph of Polysilicon, Tungsten LI and Tungsten Plugs (Polysilicon is represented by the thin lines between the taller LI lines). (Micrograph courtesy of Integrated Circuit Engineering)

10. Metal-1 Interconnect Formation

The next series of operations has to do with depositing a three-layer metal film, referred to as a *metal stack* or *sandwich*, on the wafer, followed by a masking and etching step (see Figure 9.25). The multilayer metal stack consists of different refractory metals—titanium, aluminum/copper, and titanium nitride. When finished, the wafer will have the first of five metal stacks to be constructed on the device. The number of metal layers on a device varies depending on die complexity, with advanced die currently having around eight metal layers. Including LI metal, the device covered in this process flow has a total of six metal layers.

Description of Steps in Metal-1 Interconnect Formation

Process Step	Description
1. Titanium Barrier Metal Deposition (PVD)	As with other metal processes, titanium is the first metal to be deposited on the entire wafer. It provides a good bond between the tungsten plugs and the next metal, aluminum. It also bonds well to the interlayer dielectric material and improves the reliability of the metal stack.
2. Aluminum-Copper Deposition (PVD)	The aluminum-copper (99% Al, 1% Cu) metal is sputtered onto the titanium-coated wafer by a PVD tool in thin films. The 1% Cu is added to the aluminum to improve the reliability of the aluminum.
3. Titanium Nitride Deposition (PVD)	TiN is thinly deposited on top of the aluminum-copper layer to serve as an antireflective coating for the next photomasking step.
4. 11th Mask, Metal Etch	The wafer is patterned with photoresist, then the three-layer metal stack is etched using a plasma etcher.

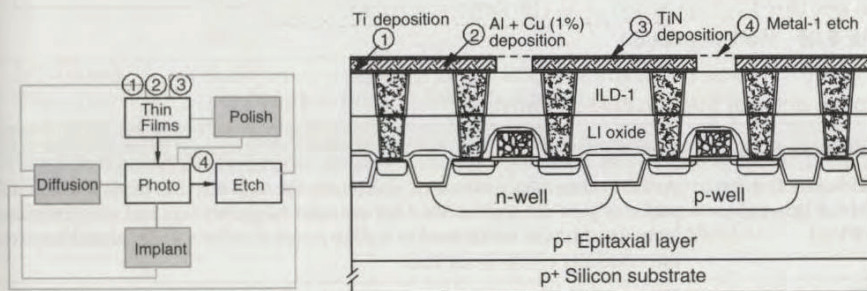


FIGURE 9.25 Metal-1 Interconnect Formation

11. Via-2 and Plug-2 Formation

The next four operations will result in the formation of the second interlayer dielectric (ILD-2) and the via openings (see Figure 9.26 and Figure 9.27). ILD-2 is similar to ILD-1 except for the very first step of filling small and large gaps that were etched into Metal-1. *Gap fill* is the filling of these gaps with a dielectric material that can be placed into the narrow spaces without creating voids or other defects that could affect electrical performance. There are two common methods for filling gaps—spin-on-glass (SOG) with etchback and *high-density plasma chemical vapor deposition* (HDPCVD). HDPCVD is the preferred method for sub-quarter micron processes. Once the gaps are filled, a plasma-enhanced CVD (PECVD) system finishes depositing the remainder of the ILD-2 oxide. Following the deposition of the ILD-2, the oxide is polished, patterned, and then etched to open the vias for the tungsten plugs to be formed.

Description of Major Steps in Via-2 Formation

Process Step	Description
1. ILD-2 Gap Fill	The latest gap-fill method for ULSI devices utilizes a high-density plasma process to alternately deposit and etch the interlayer oxide as its being deposited. The result is a dense oxide with few or no voids in the metal gaps.
2. ILD-2 Oxide Deposition	A PECVD system is used to deposit the remainder of the ILD-2 oxide layer.
3. ILD-2 Oxide Polish	The wafer is polished to planarize the surface prior to the next patterning step.
4. 12th Mask, ILD-2 Etch	The wafer is patterned with photoresist, then the ILD-2 oxide is etched using a plasma etcher.

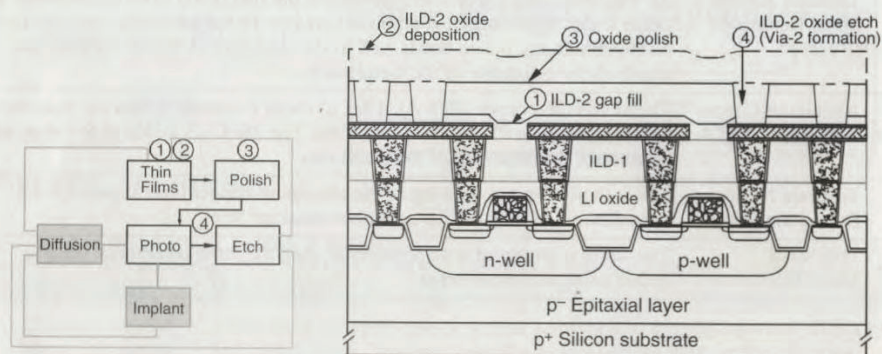


FIGURE 9.26 Via-2 Formation

Description of Major Steps in Plug-2 Formation

Process Step	Description
1. Titanium Barrier Metal Deposition (PVD)	As with other metal processes, titanium is the first metal to be deposited on the wafer. It provides a good bond between the tungsten plugs and the next metal, aluminum. It also bonds well to the interlayer dielectric material and improves the reliability of the metal stack.
2. Titanium Nitride Deposition (CVD)	TiN is thinly deposited on top of the Ti layer. The TiN serves as a diffusion barrier for the tungsten in the deposition step.
3. Tungsten Deposition (CVD)	Another CVD tool is used to deposit tungsten on the wafer. Tungsten fills the small via openings to form the plug.
4. Tungsten Polish	The tungsten-coated wafer is polished down to the upper surface of the ILD-2 oxide, leaving the tungsten plugs in the vias.

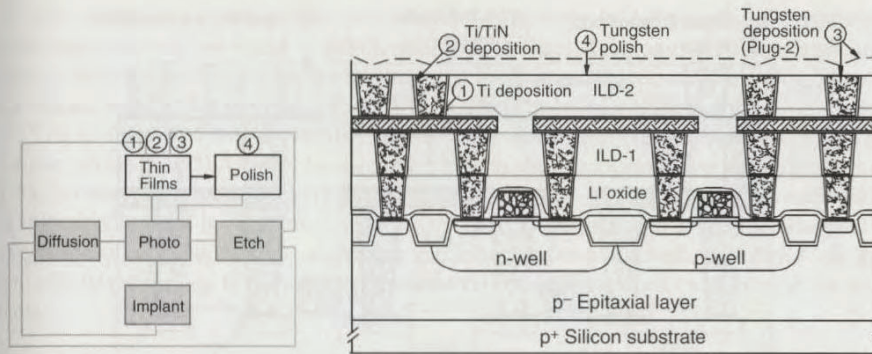
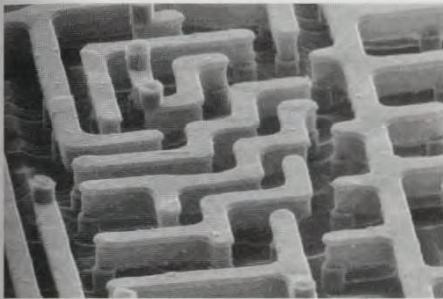


FIGURE 9.27 Plug-2 Formation



SEM Micrograph of First Metal Layer over First Set of Tungsten Vias (Note TiN Cap over Aluminum)
(Micrograph courtesy of Integrated Circuit Engineering)

12. Metal-2 Interconnect Formation

The next series of operations describes the process of forming the interconnects between layers (see Figure 9.28 on page 220). The process is repeated in the same manner for all remaining metal stacks.

Description of Major Steps in Metal-2 Interconnect Formation

Process Step	Description
1. Metal-2 Deposition to Etch	The second metal stack is deposited exactly as the first metal stack. The stack is a composite of three layers—Ti, Al/Cu, and TiN. A plasma etcher is used to etch the Metal-2 lines through windows in the patterned resist.
2. ILD-3 Gap Fill	Following the Metal-2 etch, HDPCVD is used to fill the metal gaps with dense oxide.
3. ILD-3 Oxide Deposition to Polish	ILD-3 oxide is deposited using a PECVD method. This action is followed by polishing the oxide to attain surface planarity.
4. Via-3 Etch, Ti/TiN Deposition, Tungsten Deposition, Polish	Via-3 openings are etched, then these are filled with barrier metal (Ti/TiN). Tungsten is deposited across the wafer surface. The tungsten is polished off the wafer until the ILD-3 oxide layer is reached. Tungsten plugs are left in the vias to provide the interconnect between Metal-2 and Metal-3.

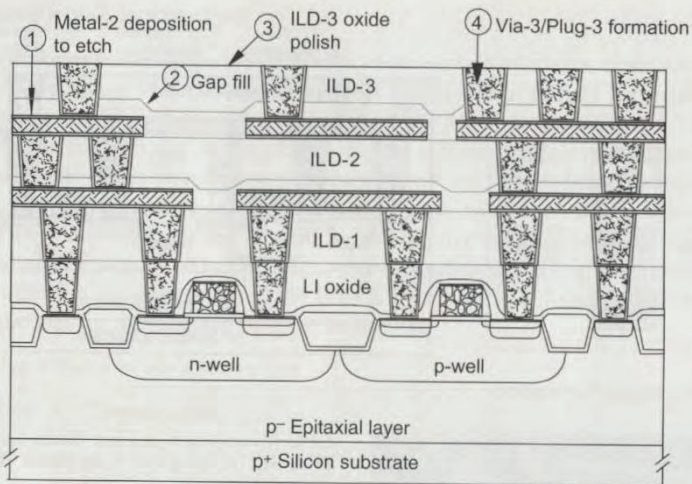
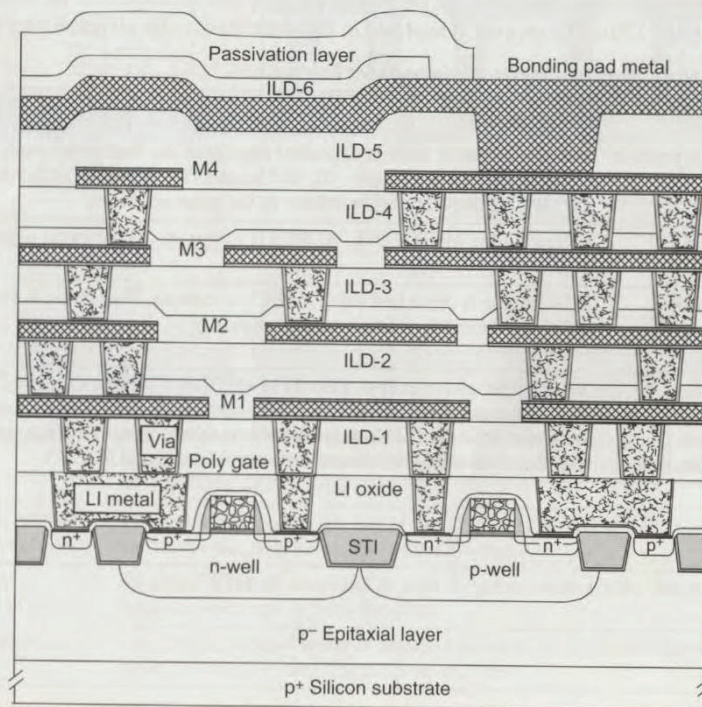


FIGURE 9.28 Metal-2 Interconnect Formation

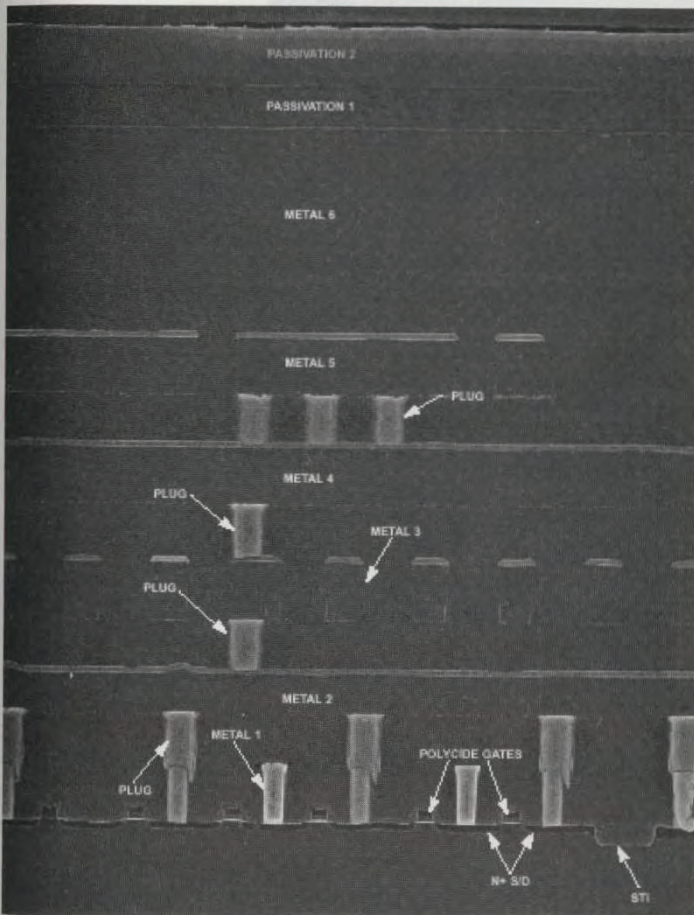
13. Metal-3 to Pad Etch and Alloy

After repeating the layering process for layers 3 and 4 and at the completion of the Metal-4 etch, $ILD-5$ oxide is deposited using the thin film process (Figure 9.29). CMP is not required for this dielectric layer because the structures to be patterned are much larger than the quarter micron dimensions formed earlier in the process. The $ILD-5$ layer is etched to allow metal filling by the Metal-5 deposition. The Metal-5 layer is etched as necessary to form bonding pads and to remove metal from areas where it is not needed.

FIGURE 9.29 Full 0.18 μm CMOS Cross Section

This product incorporates 0.18 μm processing technology, including twin-tub technology, retrograde implants, shallow trench isolation, shallow S/D diffused regions, sidewall spacers, titanium silicide contacts, titanium barrier metal, tungsten local interconnect, tungsten plugs, three-layer metal stacks, HDP oxide gap fill, and PECVD oxide as the interlayer dielectric.

The final steps of the process include one more oxide layer (ILD-6) followed by a top layer of silicon nitride ($\sim 2000 \text{ \AA}$). This layer is referred to as the *passivation layer*. Its purpose is to protect the product from moisture, scratches, and contamination. A final low-temperature alloy step in a diffusion furnace is performed. This heat treatment helps improve the metallurgical bonds between metal connections, thus improving electrical performance and reliability. Care must be taken with this alloy step to prevent overheating the product, which can cause permanent structural defects.



SEM Micrograph of Cross-section of Microprocessor (Micrograph courtesy of Integrated Circuit Engineering)

14. Parametric Testing

The wafer is tested twice to determine its product-worthiness—once when the wafer completes the first metal etch and again after the completion of the last wafer fab process step. Following metal etch, special microprobes connected to electronic test instruments are used to measure certain electrical parameters of specific device test structures on the wafer. This in-line parametric testing procedure is also referred to as *wafer electrical test*, or WET.