UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-00797
U.S. Patent No. 9,953,880 B2

Declaration of Shauna L. Wiest regarding *Colinge 2008*

I, Shauna L. Wiest, state and declare as follows:

I. Introduction

1. I have prepared this Declaration in connection with a petition for *inter partes* review of U.S. Patent No. 9,953,880 B2, which I understand will be filed concurrently with this Declaration.

2. I am currently a senior research analyst with the Research & Information Services team at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP located at 3300 Hillview Avenue, Palo Alto, CA 94304.

3. I am over eighteen years of age, and I am competent to make this Declaration. I make this Declaration based upon my own personal knowledge, and my professional knowledge of library science practices.

4. I earned a Master of Science in Library Science degree from the University of North Carolina at Chapel Hill in 1999, and a Bachelor of Arts in Political Science degree from the University of California at San Diego in 1989. I have worked as a law librarian for over eighteen years. I have been employed in the Research & Information Services Department at Finnegan, Henderson, Farabow, Garrett & Dunner, LLP since 2021. Before that, from 2000-2015, I was employed as a Law Librarian at Stoel Rives LLP, and from 2015-2016, I was employed as a Competitive Intelligence Specialist for Nossaman LLP. Additionally, as a graduate student at the University of North

Carolina at Chapel Hill, I served as an intern at the Environmental Protection Agency at Research Triangle Park ("EPA-RTP") where one of my rotations included original cataloging for EPA technical documents, state agency reports and documents, international organization documents, dissertations, and, on occasion, monographs. In this role, I accessed OCLC, MARC records, and the EPA National Library Catalog daily.

II. Standard Library Practice for Receiving, Cataloging, and Making Materials, including Books and Monographs, Publicly Available

5. I have knowledge of and experience with standard library practices regarding the receipt, cataloging, shelving, and making materials, including books and monographs, available to the public. I have knowledge of and experience with the Machine-Readable Cataloging (MARC) system, an industry-wide standard that libraries use to catalog materials. I also have knowledge of and experience with OCLC (previously called Online Computer Library Center, Inc.) and OCLC Control Numbers, which are unique accession numbers assigned by the OCLC system when a bibliographic record is catalogued and made accessible and available to the public through WorldCat. OCLC control numbers are often used by the public to search for specific records within WorldCat, the latter being an online global catalog of 586,648,074 bibliographic records and 3,521,359,124 holdings in libraries all

over the world (as of December 2024) (Source: https://www.oclc.org/en/worldcat/inside-worldcat.html).

6. Based on standard library practice, when a library receives a print item, the cataloguer or cataloguer's assistant will examine the item and date-stamp and/or affix a label to the item with the library name and/or barcode with the date it was received. Next, the library will catalog the item within a few days of receiving it. As a general practice, cataloguing is centralized and performed by a cataloguing department within a library or university setting.

7. Normally, after an item is cataloged, the public may access the item by searching a library online catalog, browsing the physical library shelves, searching a physical card catalog, or by seeking assistance from a Librarian to identify and/or pull the item from storage. Standard library practice is to make an item available to the public within several weeks of cataloging it.

III. Ownership and Date-Stamp

8. Libraries have different policies on whether to date-stamp received publications. It is becoming increasingly common for libraries to no longer date-stamp the publications they receive. Historically, it was common practice to affix an ownership and date stamp somewhere within the publication, usually on the cover page, verso of the cover page, or a designated page within the publication.

The timing of when an ownership/date stamp is placed on the monograph or periodical can vary from one library to another. It could occur when the item is received in acquisitions after shipment to the library, or at the time of cataloging.

IV. MARC Records

9. The MARC system was developed during the 1960s to standardize bibliographic catalog records so they could be read by computers and shared among libraries. By the mid-1970s, MARC had become the international standard for cataloging bibliographic materials and is still used today. Many libraries provide public access to their MARC records via their electronic cataloging systems at the library. In a MARC record, each field provides specific information about the cataloged item, including how materials are held, and how and when they were made available and accessible to the public.

10. The MARC record system uses specific three-digit numeric codes ("field tags") (from 001-999) to identify each field in a catalog record. For example, MARC field tag 008 provides the six-digit date an item was catalogued (*Date entered on file*). The first six characters of MARC field tag 008 are always in the "**YYMMDD"** format. Descriptions and definitions of all the character positions of field tag 008 are outlined here: https://www.loc.gov/marc/bibliographic/bd008a.html.

11. As is relevant to this Declaration, MARC field tag 020 sets forth the International Standard Book Number ("ISBN"), a unique identification number assigned to every book or monograph publication. MARC field tag 050 sets forth call number and classification information so that an item can be found within a library. MARC field tag 245 sets forth the title and statement of responsibility for a work. MARC field tag 260 sets forth information relating to the place of publication, publisher, and copyright date. MARC field tag 505 sets forth notes regarding a work's formatted contents, including the individual titles of separate works, contained within a single work. Finally, the 900 (9XX) field tags are typically reserved for local use by the individual library holding the item described in the MARC record.

V. Public Availability of *Colinge 2008*

12. This Declaration relates to the date of receipt, public accessibility, and public availability of the following reference: Jean-Pierre Colinge, Ed., *FinFETs and Other Multi-Gate Transistors*," Hardcover ISBN 978-0-387-71751-7, Springer Science+Business Media, LLC, New York, 2008 including pages 8-17 and pages 49-70 (*"Colinge 2008"*). I understand that *Colinge 2008* is being submitted as **Ex-1006** in this proceeding.

13. As detailed below, I have reviewed the print *Colinge 2008* reference, which was supplied to me from the Library of Congress by the University of

Wisconsin at Madison, Wisconsin TechSearch document delivery service on March 26, 2025; the *Colinge 2008* Library of Congress public catalog and holdings records; and the *Colinge 2008* Library of Congress MARC record to determine the date of public accessibility and availability for *Colinge 2008*.

14. **Appendix A** to this Declaration is a true and accurate copy of the cover page, title page, preface, and table of contents for the print hardcover book Jean-Pierre Colinge, Ed., "FinFETs and Other Multi-Gate Transistors," Hardcover ISBN 978-0-387-71751-7, Springer Science+Business Media, LLC, New York, 2008, ("*Colinge 2008")* including pages 8-17 and pages 49-70 held by the Library of Congress. **Appendix A** contains an LC Copyright bar code sticker on the back cover bearing number 00328971239. **Appendix A** also contains two spine stickers donating the *Colinge 2008* Call Number as TK 7872 .T73 F56 2008 Copy 1 and the location of the book as CBN BRNCH GenColl. Finally, **Appendix A** sets forth the unique International Standard Book Number (ISBN) assigned to the hardcover print copy of *Colinge 2008* as 978-0-387-71751-7.

15. **Appendix B** to this Declaration is a true and accurate copy of the Library of Congress public catalog record for its copy of *Colinge 2008*, which was downloaded from https://lccn.loc.gov/2007935904 on March 27, 2025.

16. The Library of Congress public catalog record (**Appendix B**) sets forth the publication title, description, contents, call number, and

availability/holdings information for its copy of *Colinge 2008*. The public catalog record indicates that one copy of the hardback print book of *Colinge 2008* is located at Call Number TK7872.T73 F56 2008 CABIN BRANCH and should be requested in the Library of Congress Jefferson or Adams Building Reading Rooms as it is currently held offsite in the Cabin Branch Collection.

17. **Appendix C** to this Declaration is a true and accurate copy of the Library of Congress MARC record for its holdings of *Colinge 2008*, which was downloaded from https://catalog.loc.gov/vwebv/staffView?searchId=20158&recPointer=0&recCount=25&searchType=2&bibId=14976954 (Click on "MARC Tags") on March 27, 2025.

18. **Appendix C** confirms the fixed data elements of MARC field tag 008 as 070823s2008nyu0010eng. As discussed above, the first six characters of MARC field tag 008 are always in the "YYMMDD" format. The MARC field tag 008 070823s2008nyu0010eng indicates that *Colinge 2008* was received and catalogued by the Library of Congress University on or around August 23, 2007 and bears a single known publication date and copyright date of 2008.

19. MARC record (**Appendix C**) field tag 020 sets forth the unique ISBN number belonging to the Library of Congress copy of *Colinge 2008* as 9780387717517 (hdbk. : acid-free paper). MARC field tag 050 sets forth the

Library of Congress call number for *Colinge 2008* as **|a TK7872.T73 |b F56 2008**. MARC field tag 245 sets forth the title and statement of responsibility for *Colinge 2008* as **|a FinFETs and other multi-gate transistors / |c Jean-Pierre Colinge, editor**. MARC field tag 260 sets forth information relating to the place of publication, publisher, and copyright date for *Colinge 2008* as **|a New York : |b Springer, |c c2008**. MARC field tag 505 in **Appendix C** sets forth the full contents contained within the print hardbound copy of *Colinge 2008* held by the Library of Congress. Finally, MARC field tags 955 provide information as to the local holdings and copies of *Colinge 2008* held and managed over time by the Library of Congress. MARC field tags 955 indicate that two copies of *Colinge 2008* (August 23, 2007) were sent to USPL/STM on 12-9-2011 and two copies received on 6-27-2012 were sent to BCCD on 6-28-2012.

20. Based on the information set forth in **Appendices A, B, and C** attached to this Declaration, standard library practices, and my experience as a librarian, *Colinge 2008* was received and catalogued by the Library of Congress on or around August 23, 2007.

21. Accordingly, the print hardcover copy of *Colinge 2008* described herein would have subsequently been made available to the public at the Library of Congress within a few weeks of being checked-in and catalogued. The interested public could have accessed *Colinge 2008* within a few weeks of August 23, 2007

by (i) searching the Library of Congress catalog, visiting the Cabin Branch and searching the stacks at Call Number TK7872.T73 F56 2008; or (ii) by asking a Library of Congress staff member in the Jefferson or Adams Building Reading Rooms and requesting the item be obtained from offsite storage.

VI. Conclusion

22. In signing this Declaration, I understand it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I understand I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

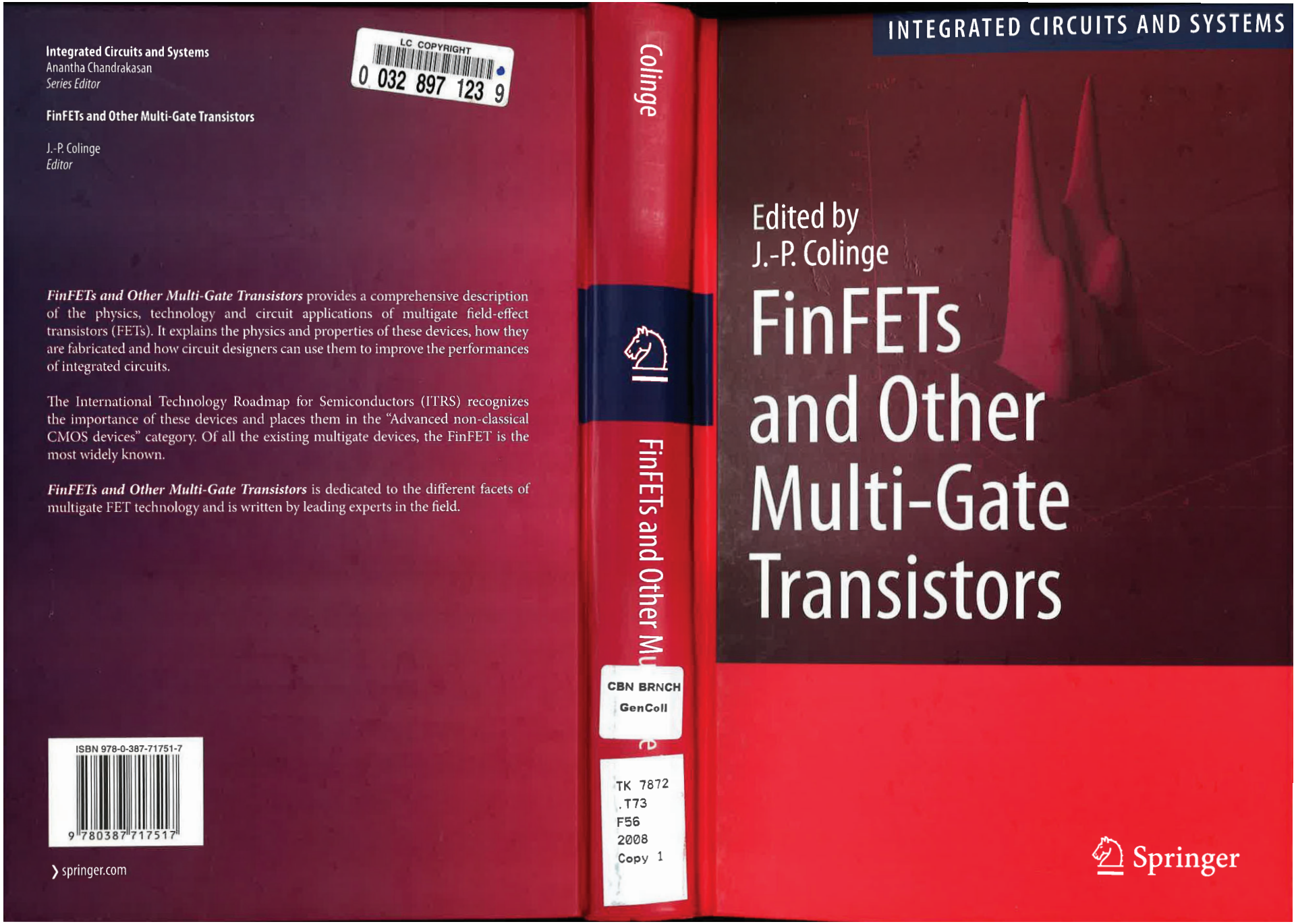
23. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on March 28, 2025 in Palo Alto, California

/Shauna L. Wiest/

Shauna L. Wiest

Appendix A


Integrated Circuits and Systems
Anantha Chandrakasan
Series Editor
FinFETs and Other Multi-Gate Transistors
J.-P. Colinge
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FinFETs and Other Multi-Gate Transistors provides a comprehensive description of the physics, technology and circuit applications of multigate field-effect transistors (FETs). It explains the physics and properties of these devices, how they are fabricated and how circuit designers can use them to improve the performances of integrated circuits.
The International Technology Roadmap for Semiconductors (ITRS) recognizes the importance of these devices and places them in the "Advanced non-classical CMOS devices" category. Of all the existing multigate devices, the FinFET is the most widely known.
FinFETs and Other Multi-Gate Transistors is dedicated to the different facets of multigate FET technology and is written by leading experts in the field.
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and Other
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FinFETs and Other Multi-Gate Transistors

Series on Integrated Circuits and Systems

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Jean-Pierre Colinge (Ed.)
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Gi-Joon Nam and Jason Cong
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Hakho Lee, Donhee Ham and Robert M. Westervelt
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Continued after index

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FinFETs and Other Multi-Gate Transistors



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Preface

The adoption of Silicon-on-Insulator (SOI) substrates for the manufacturing of mainstream semiconductor products such as microprocessors has given SOI research an unprecedented impetus. In the past, novel transistor structures proposed by SOI scientists were often considered exotic and impractical, but the recent success of SOI in the field of microprocessor manufacturing has finally given this technology the credibility and acceptance it deserves.

The classical CMOS structure is reaching its scaling limits and "end-of-roadmap" alternative devices are being investigated. Amongst the different types of SOI devices proposed, one clearly stands out: the multigate field-effect transistor (multigate FET). This device has a general "wire-like" shape with a gate electrode that controls the flow of current between source and drain. Multigate FETs are commonly referred to as "multi(ple)-gate transistors", "wrapped-gate transistors", "double-gate transistors", "FinFETs", "tri(ple)-gate transistors", "Gate-all-Around transistors", etc. The International Technology Roadmap for Semiconductors (ITRS) recognizes the importance of these devices and calls them "Advanced non-classical CMOS devices".

There exists a number of textbooks on SOI technology. Some of these books tackle the subject of multigate FETs, but there is no book that contains a comprehensive description of the physics, technology and circuit applications of this new class of devices. This is why we decided to compile chapters dedicated to the different facets of multigate FET technology, written by world-leading experts in the field. This book contains seven chapters:

- *Chapter 1:* ***The SOI MOSFET: from Single Gate to Multigate***, by Jean-Pierre Colinge, is a general introduction that shows the evolution of the SOI MOS transistor and retraces the history of the multigate concept. The advantages of multigate FETs in terms of electrostatic integrity and short-channel control are described, and the challenges posed by the appearance of novel effects, some of quantum-mechanical origin, are outlined.

- *Chapter 2:* ***Multigate MOSFET Technology***, by Weize (Wade) Xiong, outlines the issues associated with multigate FET manufacturing. This chapter describes thin-fin formation techniques, advanced gate stack deposition and source/drain resistance reduction techniques. Issues related to fin crystal orientation and mobility enhancement via strain engineering are tackled as well.

- *Chapter 3:* ***BSIM CMG: A Compact Model for Multi-Gate Transistors***, by Mohan Vamsi Dunga, Chung-Hsun Lin, Ali M. Niknejad and Chenming Hu, describes the physics behind the BSIM-CMG (Berkeley Short-channel IGFET Model – Common Multi-Gate) compact models for multigate MOSFETs. A compact model serves as a link between process technology and circuit design. It is a concise mathematical description of the device physics in the transistor. Some simplifications in the physics, however, can be made to enable fast computer analysis of device/circuit behavior.

- *Chapter 4:* ***Physics of the Multigate MOS System***, by Bogdan Majkusiak, analyzes the electrostatics of the multigate MOS system. Using quantum-mechanical concepts, it describes electron energy quantization and the properties of a one-dimensional and two-dimensional electron gas. The effects of tunneling through thin gate dielectrics on the electron population of a device are studied as well.

- *Chapter 5:* ***Mobility in Multigate MOSFETs***, by Francisco Gámiz and Andrés Godoy, analyzes the behavior of electron mobility in different multigate structures comprising double-gate transistors, FinFETs, and silicon nanowires. Mobility in multiple gate devices is compared to that in single-gate devices and different approaches for improving the mobility in these devices, such as different crystallographic orientations and strained Si channels, are studied.

- *Chapter 6:* ***Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs***, by Véronique Ferlet-Cavrois, Philippe Paillet and Olivier Faynot, describes the effects of ionizing radiations such as gamma rays and cosmic rays on SOI MOSFETs. These effects are extremely important in military, space and avionics applications. Multi-gate FETs show exceptional resistance to total-dose and single-event effects and could become the new standard in radiation-hardened electronics.

- *Chapter 7:* ***Multigate MOSFET Circuit Design***, by Gerhard Knoblinger, Michael Fulde and Christian Pacha, describes the interrelationship between the multi-gate FET device properties and elementary digital and analog circuits, such as CMOS logic gates, SRAM cells, reference circuits, operational amplifiers, and mixed-signal building blocks. This approach is motivated by the observation that a cost-efficient, heterogeneous SoC integration is a key factor in modern IC design.

Jean-Pierre Colinge, August 2007

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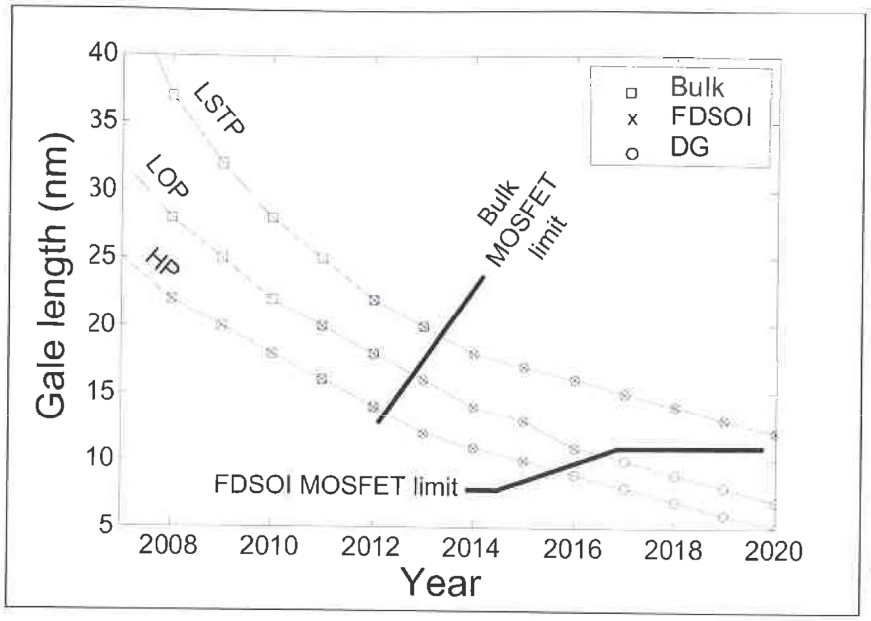


Fig. 1.5. Evolution of gate length predicted by the 2005 ITRS for high-performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits.

1.4 A Brief History of Multiple-Gate MOSFETs

In a continuous effort to increase current drive and better control short-channel effects, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (double-, triple- or quadruple- gate devices). It is worth noting that, in most cases, the term "double gate" refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term "triple gate" is used for a single gate electrode that is folded over three sides of the transistor. One remarkable exception is the MIGFET (Multiple Independent Gate FET) where two separate gate electrodes can be biased with different potentials. It is also worth pointing out that one device may have several different names in the literature (Table 1.1).

Table 1.1. Device names found in the literature.

Acronym	Also known as
MuGFET (Multiple-Gate FET)	Multi-gate FET, Multigate FET
MIGFET (Multiple Independent Gate FET)	Four-terminal (4T) FinFET
Triple-gate FET	Trigate FET
Quadruple-gate FET	Wrapped-Around Gate FET Gate-All-Around FET Surrounding-Gate FET
FinFET	DELTA (fully DEpleted Lean channel TrAnsistor)
FDSOI (Fully Depleted SOI)	Depleted Silicon Substrate
PDSOI (Partially depleted SOI)	Non-Fully Depleted SOI
Volume Inversion	Bulk Inversion
DTMOS (Dual Threshold Voltage MOS)	VTMOS (Varied Threshold MOS) MTCMOS (Multiple Threshold CMOS) VCBM (Voltage-Controlled Bipolar MOS) Hybrid Bipolar-MOS Device

1.4.1 Single-gate SOI MOSFETs

Figure 1.6 shows the "Family Tree" of SOI MOSFETs and shows the evolution from partially depleted, single-gate devices to multi-gate, fully depleted structures. Partially depleted silicon MOSFETs are the successors of earlier SOS (Silicon-On-Sapphire) devices. PDSOI MOSFETs were first used for niche applications such as radiation-hardened or high-temperature electronics. At the turn of the century PDSOI technology became mainstream as major semiconductor manufacturers started to use it to fabricate high-performance microprocessors. The low-voltage performance of PDSOI devices can be enhanced by creating a contact between the gate electrode and the floating body of the device. Such a contact improves the subthreshold slope, body factor and current drive, but limits the device operation to sub-1V supply voltages. [15-23] Fully depleted SOI devices have a better electrostatic coupling between the gate and the channel. This results in a better linearity, subthreshold slope, body coefficient and current drive. FDSOI technology is used in a number of applications ranging from low-voltage, low-power to RF integrated

circuits. There exists a series of textbooks on SOI devices and technology, [24-26] as well as on SOI circuit design.[27-29]

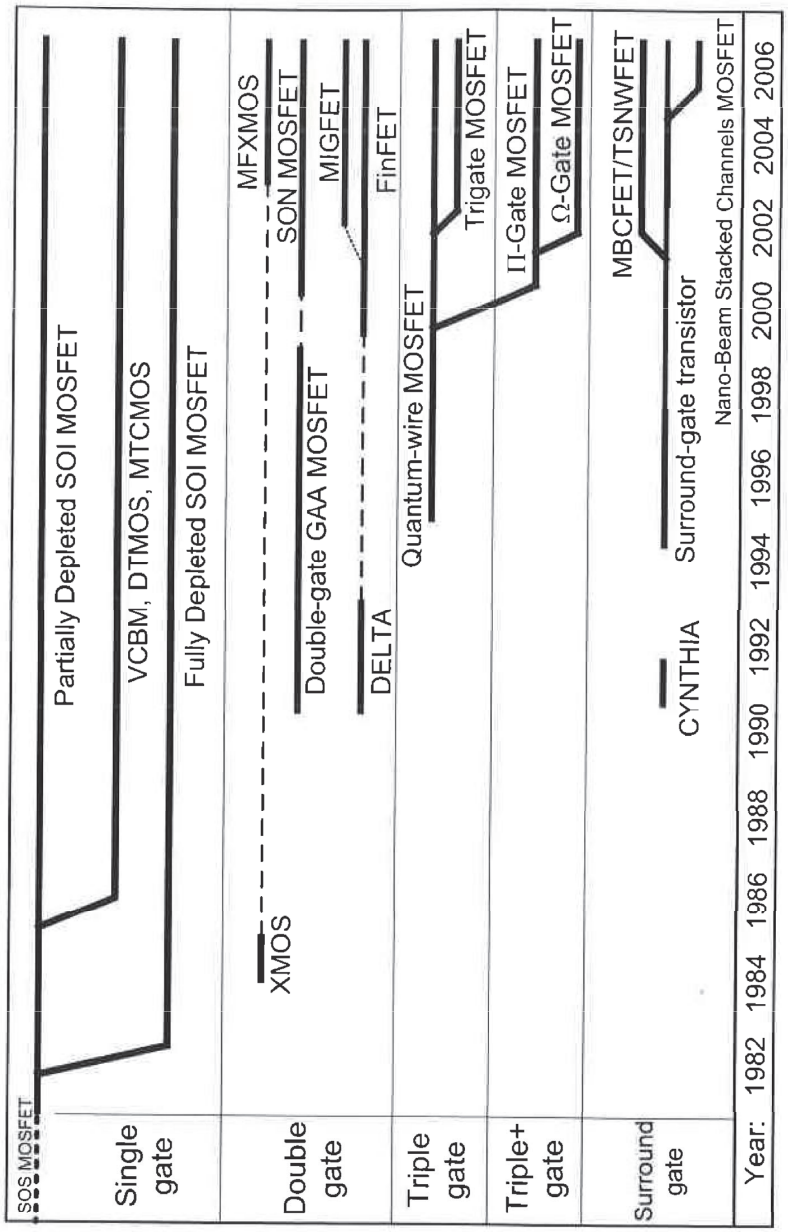


Fig. 1.6. "Family tree" of SOI and multigate MOSFETs.

1.4.2 Double-gate SOI MOSFETs

The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi 1984.[30] That paper shows that one can obtain significant reduction of short-channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (*Xi*). Using this configuration, a better control of the channel depletion region is obtained than in a "regular" SOI MOSFET, and, in particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel.[31] A more complete modeling that includes Monte-Carlo simulations, was published by Frank, Laux and Fischetti in 1992 in a paper that explores the ultimate scaling of the silicon MOSFET.[32] According to that article, the ultimate silicon device is a double-gate SOI MOSFET with a gate length of 30 nm, an oxide thickness of 3 nm, and a silicon film thickness of 5 to 20 nm. Such a (simulated) device shows no short-channel effects for gate lengths larger than 70 nm, and provides transconductance values up to 2300 mS/mm. The first fabricated double-gate SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)",[33] where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin" (Figure 1.7). The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin. [34-38] The hard mask is used to prevent the formation of parasitic inversion channels at the top corners of the device.

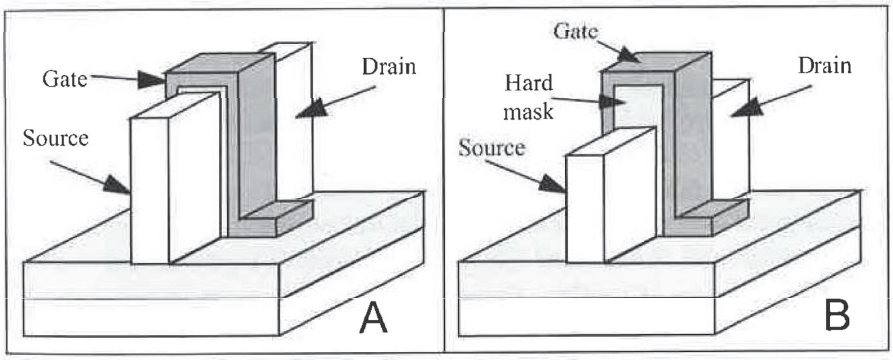


Fig. 1.7. Examples of double-gate MOS structure: A: DELTA MOSFET; B: FinFET.

Other implementations of vertical-channel, double-gate SOI MOSFETs include the "Gate-All-Around device" (GAA), which is a planar MOSFET with the gate electrode wrapped around the channel region (Figure

1.8.A)[39], the Silicon-On-Nothing (SON) MOSFET,[40-42] the Multi-Fin XMOS (MFXMOS) [43], the triangular-wire SOI MOSFET [44] and the Δ-channel SOI MOSFET.[45] It is worth noting that the original GAA device was a double-gate device, even though the gate was wrapped around all sides of the channel region, because the silicon island was much wider than thick. Nowadays, most people use the GAA acronym for quadruple-gate or surrounding-gate devices having a width-to-height ratio much closer to unity.[46-48]

The MIGFET (Multiple Independent Gate FET) is a double-gate device in which the two gate electrodes are not connected together and can, therefore, be biased with different potentials.[49-52,160] The main feature of the MIGFET is that the threshold voltage of one of the gates can be modulated by the bias applied to the other gate. This effect is similar to the body effect in FDSOI MOSFETs.[53] An application using MIGFET is signal modulation. A simple square law mixer can be formed using a single MIGFET by applying a small RF signal to one gate and a large low-frequency signal to the other gate. This single-device modulation is possible because the channel is fully depleted and the gates are perfectly symmetrical and aligned. This signal modulation circuit reduces transistor counts and rail-to-rail transistor stack, making it possible to design compact low-power mixers.[54]

1.4.3 Triple-gate SOI MOSFETs

The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides.[55] Implementations include the quantum-wire SOI MOSFET (Figure 1.8.B) [56-57] and the trigate MOSFET.[58-59]

The Electrostatic Integrity of triple-gate MOSFETs can be improved by extending the sidewall portions of the gate electrode to some depth in the buried oxide and underneath the channel region (Π-gate device [60-61] and Ω-gate device [62-64]). From an electrostatic point of view, the Π-gate and Ω-gate MOSFETs have an effective number of gates between three and four. The use of strained silicon, a metal gate and/or high-k dielectric as gate insulator can further enhance the current drive of the device.[65-68]

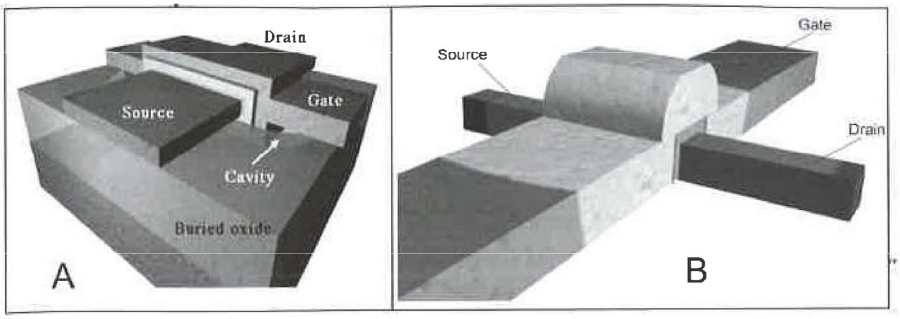


Fig. 1.8. A: Gate-All-Around (GAA) MOSFET; B: Triple-gate MOSFET.

1.4.4 Surrounding-gate (quadruple-gate) SOI MOSFETs

The structure that theoretically offers the best possible control of the channel region by the gate, and hence the best possible Electrostatic Integrity is the surrounding-gate MOSFET. The first surrounding-gate MOSFETs were fabricated by wrapping a gate electrode around a vertical silicon pillar. Such devices include the CYNTHIA device (circular-section device) [69-70] and the pillar surrounding-gate MOSFET (square-section device).[71] More recently, planar surrounding-gate devices with square or circular cross sections have reported.[72-73] Surrounding-gate SOI MOSFETs with a gate length as small as 5 nm and a diameter of 3 nm have shown to be fully functional.[74-75]

To increase the current drive per unit area, multiple surrounding-gate channels can be stacked on top of one another, while sharing common gate, source and drain. Such devices are called the Multi-Bridge Channel MOSFET (MBCFET), [76-77] the Twin-Silicon-Nanowire MOSFET (TSNWFET) [78], or the Nano-Beam Stacked Channels (GAA) MOSFET.[79] Analytical models for the electrical characteristics of cylindrical surrounding-gate MOSFETs can be found in the literature.[80-83]

Schematic cross sections corresponding to the different gate structures described in the previous sections are shown in Figure 1.9.

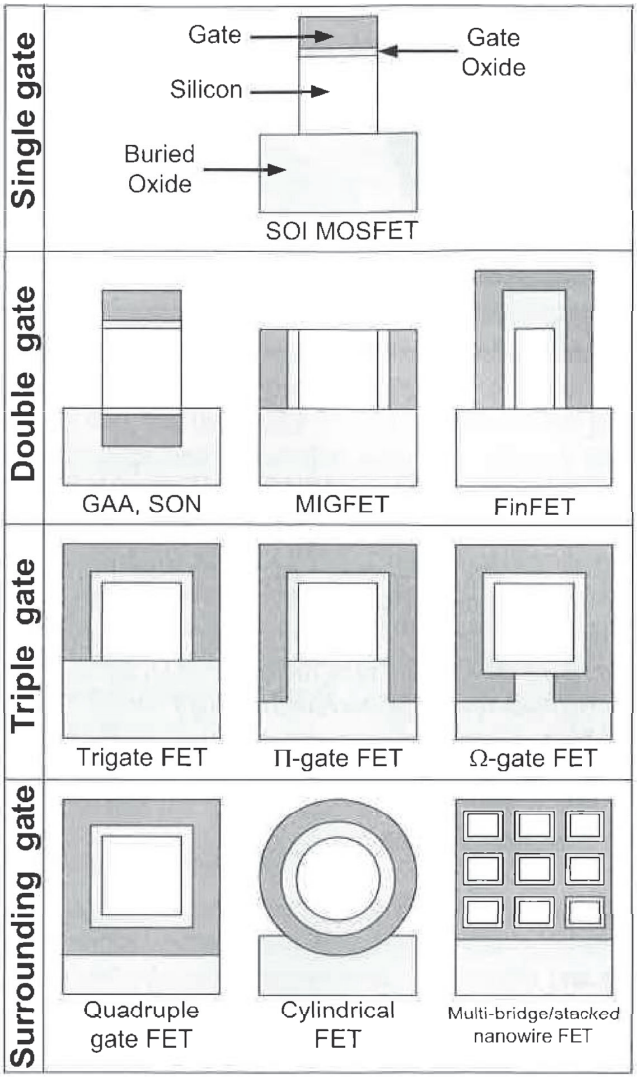


Fig. 1.9. Different gate structures.

1.4.5 Other multigate MOSFET structures

The Inverted T-channel FET (ITFET) combines a thin-film planar SOI device with a trigate transistor (Figure 1.10.A). [84-85] It comprises planar horizontal channels and vertical channels in a single device. The devices have multi-gate control around these channels. The Inverted T-gate

structure has several advantages: the large base helps the fins from falling over during processing; it also allows for transistor action in the space between the fins, which is left unused in other MuGFET configurations. These additional channels increase the current drive. Numerical simulation of an N-channel ITFET reveals different turn-on mechanisms in different parts of the device. The corners of the device turn on first, immediately followed by the surface of the planar regions and the vertical channel. Since each ITFET has about seven corner elements they constitute a significant current to each ITFET device and in a well-designed device can yield substantially more current than a planar device of equivalent area.

The bulk FinFET is a FinFET made on bulk silicon instead of an SOI wafer. Fins are etched on a bulk silicon wafer and trimmed using an oxidation step. Field oxide is deposited to avoid inversion between the fins (Figure 1.10.B). Device with fin width down to 10 nm have shown to have good punchthrough immunity down to the sub-20nm gate length regime.[86-87]

The multi-channel Field Effect Transistor (McFET) is a modified bulk FinFET where a trench is etched in the center of the fin.[88] The trench is filled by the growth of a gate oxide and the deposition of gate material. This process produces a device having two very thin "twin" fins running from source to drain (Figure 1.10.C).

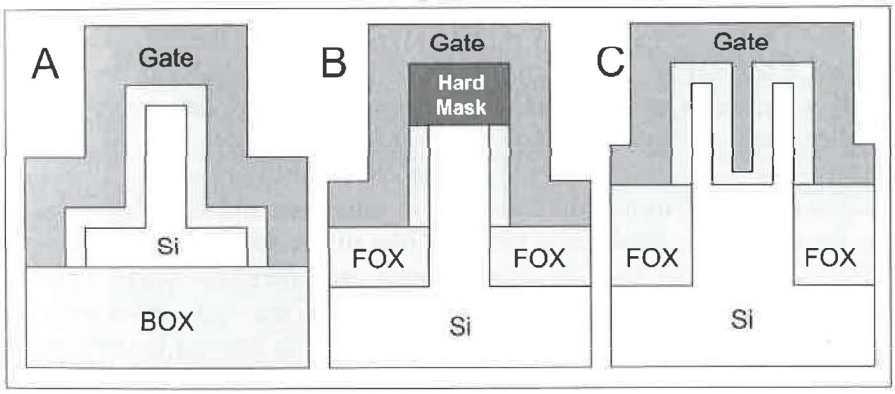


Fig. 1.10. Cross section of A: Inverted T channel FET; B: Bulk FinFET; C: Multi-channel Field Effect Transistor.

The 4-gate transistor (G^4 FET) has two (top and bottom) MOS gates and two (lateral) JFET gates. It is operated in accumulation mode and has the same structure as an inversion-mode partially depleted SOI MOSFET with

two independent body contacts. These lateral contacts play the role of source and drain in the G^4 FET, while the junctions are used as lateral gates. The current in the body of the device is controlled by the front and back MOS gates, and by the two lateral junctions. The height and width of the conductive path is modulated by a mix of MOS and JFET effects. Each gate has the ability of switching the transistor on and off.[89-91] A model for the G^4 FET has been published In the literature.[92]

1.4.6 Multigate MOSFET memory devices

SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) devices are non-volatile flash memory devices. They are essentially used in mobile applications. Flash devices have a small form factor, high storage density and low power consumption. For logic applications FinFET type devices are known to have good scalability down to 10-nm gate length. The FinFET device architecture combined with an ONO trapping layer as gate dielectric enables memory cells with feature sizes well below 50-nm. SONOS FinFET cells are programmed and erased using Fowler–Nordheim tunneling. SONOS FinFET memory devices show excellent functionality down to 20 nm channel length. [93-94] As an alternative to the ONO layer, nanocrystals embedded within the gate dielectric can be used to trap charges and achieve a similar memory effect. FinFET flash memory devices with a V_{TH} window larger than 1 volt have been demonstrated using silicon nanocrystals embedded in the gate oxide.[95]

The SOI Zero-capacitor RAM (ZRAM) memory cell consists of a single PDSOI transistor in the floating body of which a charge can be stored. Such a capacitorless, one-transistor memory cell is, of course much smaller than a classical DRAM cell that requires the use of both a transistor and a storage capacitor. In the ZRAM memory cell a "1" binary state is stored by biasing the transistor in saturation and injecting holes in the floating body. Applying a negative bias to the bit line (device source) removes the charge from the floating body and, therefore, stores a binary "0" in the device. Since the threshold voltage of the FET varies with the charge stored in the body the logic state can easily be read by measuring the drain current when the device is turned on. Even though the storage of a charge requires a floating body, and, therefore, a partially depleted device, it is possible to realize ZRAM cells in fully depleted FinFETs of trigate devices. By applying a back-gate bias to the device, a floating body can be created at the bottom of the otherwise fully depleted fin and ZRAM operation can be activated.[96] Retention times of few tens of milliseconds are observed at room temperature on FinFETs with 300 nm channel length.

These values suit well typical embedded DRAM specification. FinFETs provide better retention characteristics than trigate devices which have a retention time of approximately 2 ms. Retention time decreases at shorter channel length but even 100 nm devices still show retention time of few milliseconds.[97]

When a positive bias is applied to the underlying silicon substrate (back gate) and a negative bias is applied to the gate of a MuGFET, it is possible to create an inversion layer at the bottom of the device and accumulation at the other interfaces. In that case, the so-called "MetaStable Dip" (MSD) effect can be observed, in which the transconductance as a function of the gate voltage increases, then drops, and then increases again. This effect is time-dependent and presents an hysteresis effect which depends whether the gate voltage is scanned in the forward or reverse mode.[98] The hysteretic nature of the phenomenon makes it useful for potential single-transistor memory applications.[99]

1.5 Multigate MOSFET Physics

1.5.1 Classical physics

1.5.1.1 Natural length and short-channel effects

The Electrostatic Integrity (*EI*), which we know to be related to short channel effects, was compared between a bulk transistor, a FDSOI MOSFET, and a double-gate device in Figure 1.3. It was shown that the *EI* can be improved by reducing the gate oxide thickness and/or by decreasing the silicon film thickness (the junction depth in the case of a bulk device). We are now going to extend the analysis to all types of multigate MOSFETs.

The potential distribution in the channel of a fully depleted multigate MOSFET can be obtained by solving Poisson's equation using the depletion approximation:

$$\frac{d^2\Phi(x,y,z)}{dx^2}+\frac{d^2\Phi(x,y,z)}{dy^2}+\frac{d^2\Phi(x,y,z)}{dz^2}=\frac{qN_a}{\varepsilon_{si}} \tag{1.7}$$

Let us first understand the meaning of this equation. It can be rewritten in the form:

2 Multigate MOSFET Technology

Weize (Wade) Xiong

2.1 Introduction

Manufacturing a self-aligned double-gate MOSFET has been the holy grail of device engineers and researchers ever since it was proposed by Sekigawa and Hayashi in 1984.[1] The first modern self-aligned vertical multi-gate MOSFET was called DELTA (fully **DE**pleted **L**ean channel **T**r**A**nsistor).[2] This device was proposed by D. Hisamoto *et al.* in 1989. Figure 2.1 shows a cross section of the DELTA MOSFET.

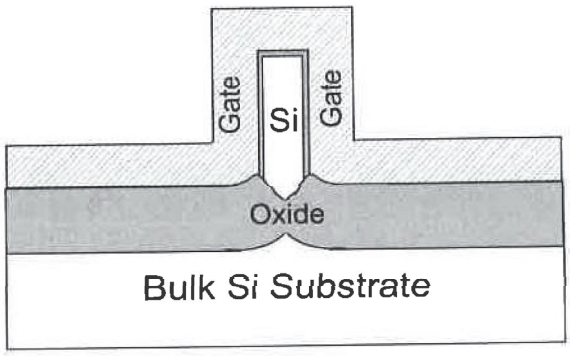


Fig. 2.1. DELTA MOSFET [1-2]. The oxide under the Si fin was formed through LOCOS oxidation while the Si fin was protected by the nitride hard mask and a nitride spacer prior to the oxidation process.

The two key features of the DELTA MOSFET are: 1) front and back MOSFET gates are inherently self-aligned and 2) the channels are on the sidewall of the silicon body/fin. The compatibility of the DELTA FET with existing planar CMOS processing is the main reason why it was

adopted as the mainstream multi-gate structure. FinFETs, Tri-gate and Π/Ω gate devices have all evolved from of this original concept [3-8].

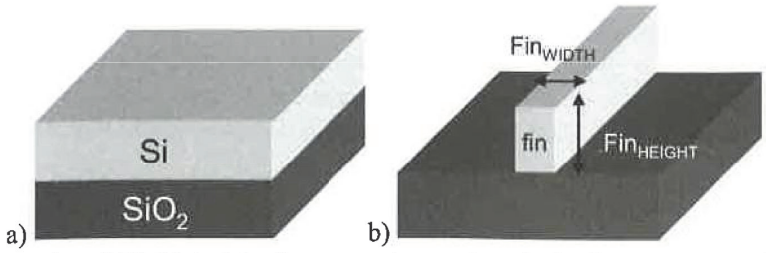
The critical fabrication steps in the front-end processing of a multi-gate MOSFET include, sequentially: 1) fin formation, 2) gate stack formation, 3) source and drain extension implant, 4) spacer formation, 5) epitaxial raised source/drain formation, and 6) deep source/drain implantation and activation anneal.

The fabrication flow of a Tri-gate MOSFET on an SOI substrate is shown in Figure 2.2. The SOI silicon top layer (T_{si}) thickness defines the fin height (Fin_{HEIGHT}). The fin pattern and the critical dimension of fin width (Fin_{WIDTH}) can be defined by optical lithography or by spacer image transfer (*SIT*) [9-10], followed by plasma etching.

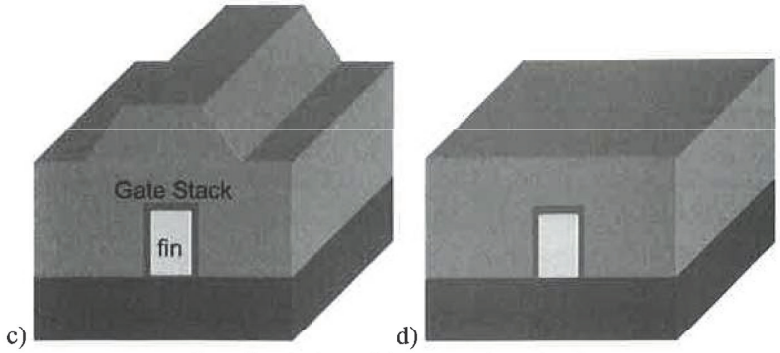
After fin etch, the fin sidewall surfaces are rough. Therefore, oxidation and H_2 annealing are often used to smooth the sidewalls.[11-12] Next, the gate dielectric is grown and metal gate is deposited. It is suitable to tune the threshold voltage (V_{th}) of the MOSFET by using a gate material that has the appropriate effective workfunction rather than by doping the channel. Sections 2.3, 2.5 and 2.6 will show that it is highly desirable to have intrinsic or lightly doped channels.

Since the gate stack is over the fin topography, a planarization step is desirable to flatten the gate surface, which reduces the burden on photolithography and gate etch. Significant overetch of the gate material is required to clear the bottom of the fins. As a result, the gate etch must have a high selectivity to the gate dielectric on top of the fin, if one wants to avoid damage to the fin during gate etch. Source and drain (S/D) extensions are formed after gate patterning using low-energy and large-tilt angled implants.[13-14] Next, S/D offset spacers are formed along the sidewalls of the gate and fin. The sidewall spacers on the fins are subsequently removed to expose the fin to grow raised source and drain using selective epitaxy.[13-15] The raised source and drain structure helps to reduce the parasitic resistance associated with thin fins.[13]

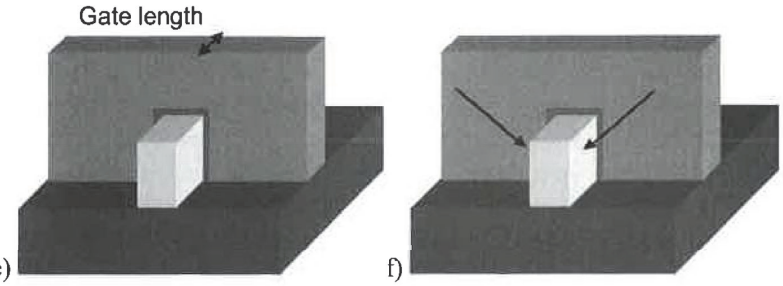
The rest of this chapter is divided into sections according to multi-gate device fabrication sequences. Section 2.2 covers fin formation, Section 2.3 describes gate stack structures, Section 2.4 describes source and drain formation and Section 2.5 highlights mobility and strain engineering.



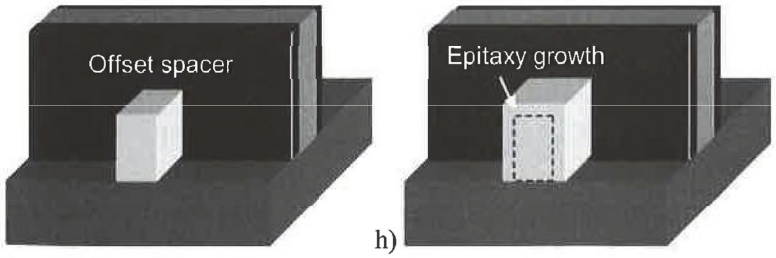
Starting SOI Material; fin patterning and etch. Define Fin_{WIDTH}; the fin height is the thickness of the silicon top SOI layer.



Gate Stack deposition and planarization



Gate etch and source and drain extension implant



Spacer formation and selective epitaxal growth. Removing the spacer on the sidewall of the fin while keeping the gate spacer is a critical step.

Fig. 2.2. General Fabrication Sequence of a Tri-gate MOSFET.

2.2 Active Area: Fins

2.2.1 Fin Width

As the MOSFET gate length, L_g, continues to shrink, year after year, the drain starts to compete with the gate electrode for control of the channel potential. The resulting "short-channel effects" (SCE) are: 1) higher sub-threshold leakage, 2) a threshold voltage (V_{th}) roll-off, and 3) a form of punch-through between the drain and source when V_{DS} is equal to the supply voltage.[16]

To reduce the drain influence in the channel, scaled planar bulk MOSFETs and PDSOI MOSFETs rely on: 1) gate oxide thickness reduction and 2) higher channel doping. The use of a thinner gate oxide increases the gate-to-channel capacitance. A higher channel doping concentration reduces charge sharing between the gate and drain in the channel, and it creates a large potential barrier between source and drain.

However, in modern MOSFETs, direct tunneling current through the gate dielectric prevents further scaling of the gate oxide thickness. The use of high channel doping concentrations reduces carrier mobility and increases Gate Induced Drain Leakage (GIDL).[17-18]

Another way to control SCEs is to use two or more gate electrodes and a thin, fully depleted semiconductor body. The idea is to create a large potential curvature in the source and drain direction by introducing a large electrical field gradient in the direction vertical to the gate. The key parameter in this approach is the thickness of the thin, fully depleted semiconductor body. In the case of the multi-gate technologies, the fin width is the thickness of the thin, fully depleted semiconductor body.

Chapter 1 introduced a powerful concept called natural length, λ, with:

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox}} \quad \text{for a double-gate MOSFET} \tag{2.1}$$

λ is a measure of the short-channel effect. It represents the distance of penetration of the drain electric field in the channel. A small value λ is desirable to minimize the SCE.

λ is proportional to the square root of the product of the device body thickness t_{si}, (or Fin_{WIDTH} in multi-gate technology) and gate oxide thickness t_{ox}. Thus, one can trade off t_{ox} scaling with Fin_{WIDTH} reduction. This approach is not possible for bulk or PDSOI MOSFETs.[17]

In a double-gate MOSFET, the center of the fin is the furthest away from the gate electrodes. Therefore, gate control is the weakest at this point. Should punchthrough occur, it would be in the center of the fin.[20] This implies using a slightly different boundary condition than Equation 2.1, which assumes the punch through is along the channel surfaces.

In this section, we will derive a new value for λ based on the assumption that punchthrough occurs in the center of the channel. The new λ has the same physical meaning as Equation 2.1, but it can better explain some of the experimental results shows later in this section. We will use the same coordinate system as in Figure 1.11. Starting with Poisson's equation, we can write:

$$\frac{d^2\Phi(x,y,z)}{dx^2}+\frac{d^2\Phi(x,y,z)}{dy^2}+\frac{d^2\Phi(x,y,x)}{dz^2}=\frac{qN_{sub}}{\varepsilon_{si}} \tag{2.2}$$

For single-gate or double-gate devices $\frac{d\phi}{dz}=0$, such that Equation 2.2 is reduced to:

$$\frac{d^2\Phi(x,y)}{dx^2}+\frac{d^2\Phi(x,y)}{dy^2}=\frac{qN_{sub}}{\varepsilon_{si}} \tag{2.3}$$

Assuming a parabolic potential distribution in the y-direction [21] we can write:

$$\Phi(x,y)\approx c_0(x)+c_1(x)y+c_2(x)y^2 \tag{2.4}$$

We now apply the boundary condition $\left.\frac{d\Phi(x,y)}{dy}\right|_{y=0}=0$ at $y=\frac{t_{si}}{2}$,

which yields:

$$\Phi(x,y)=\Phi_f(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi_s(x)-\Phi_{gs}}{t_{ox}}y-\frac{1}{t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\Phi_s(x)-\Phi_{gs}}{t_{ox}}y^2 \tag{2.5}$$

where $\Phi_s(x)$ is the front- and back-surface potential and $\Phi_{gs} = V_{gs} - V_{FBF}$ is the front gate voltage V_{gs} minus the flat-band voltage, V_{FB}. Since the potential at the center of the fin, $\Phi_c(x)$, is the most relevant to SCE, we extract a relationship between $\Phi_c(x)$ and $\Phi_s(x)$ from 2.5 by substituting $y = \frac{t_{si}}{2}$ as follows:

$$\Phi_s(x) = \frac{1}{1 + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}}} \left(\Phi_c(x) + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}} \Phi_{gs} \right) \tag{2.6}$$

Expressing $\Phi(x, y)$ as a function of $\Phi_c(x)$ we obtain:

$$\Phi(x,y) = \left(1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y}{t_{ox}} - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y^2}{t_{ox} t_{si}} \right) \cdot \left(\frac{\Phi_c(x) + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}} \Phi_{gs}}{1 + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}}} \right) - \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y}{t_{ox}} \Phi_{gs} - \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{y^2}{t_{ox} t_{si}} \Phi_{gs} \right) \tag{2.7}$$

Substituting 2.7 back in 2.3 we get:

$$\frac{d^2 \Phi_c(x)}{dx^2} + \frac{\Phi_{gs} - \Phi_c(x)}{\lambda^2} = \frac{qN_A}{\varepsilon_{si}} \tag{2.8}$$

where natural length λ is now written:

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox}}{4\varepsilon_{si}} \frac{t_{si}}{t_{ox}} \right) t_{si} t_{ox}} \tag{2.9}$$

Numerical simulations in [17] show that for reasonable short-channel effect control, the gate length needs to be 5-10 times greater than λ.

We have established a theoretical relationship between L_g and λ. For a device designer, it would be more relevant to establish a guideline for the L_g to t_{si} ratio to control short-channel effects. Equation 2.9 does not separate the effects of t_{si} and t_{ox}. To walk around the problem, let us

assume a good SCE control can be achieved with $L_g = n\lambda$, where n is some arbitrary number. We now have:

$$\frac{L_g}{n} = \lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox}} \tag{2.10}$$

In the limiting case when $L_g = 0$, we can write:

$$\frac{\varepsilon_{si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{4\varepsilon_{si}}\frac{t_{si}}{t_{ox}}\right)t_{si}t_{ox} = 0 \tag{2.11A}$$

which implies:

$$t_{si} = -4\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox} \tag{2.11B}$$

The right-hand term of Equation 2.11B represents the intercept point of the L_g *vs.* Fin_{WIDTH} plot for $L_g = 0$. Thus, one can define an effective fin width, $FinW_{eff}$, as:

$$FinW_{eff} = Fin_{WIDTH} + 4\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox} \tag{2.12}$$

Equation 2.12 shows that the impact of gate oxide can be considered equivalent to a constant offset of physical fin width. The validity of Equation 2.12 was demonstrated in reference [22]. Fig 2.3 shows contours of subthreshold swing on a L_g *vs.* Fin_{WIDTH} plot with 48 devices having 6 different Fin_{WIDTH} values and 8 different gate lengths. Each line represents a fixed short channel effect control. Since all devices have the same gate oxide (1.6nm oxynitride), they all intercept L_g =0 at the same point. This point is approximately equal to $-4\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}$.

Figure 2.4 shows the experimental double-gate FinFET results of $L_g/FinW_{eff}$ *vs.* subthreshold swing (or Subthreshold Slope, SS).[22] If we assume that a SS value of 90mV/dec is acceptable, then $L_g/FinW_{eff}$ is ~ 1.5. A triple-gate MOSFET with enhanced gate electrostatic control of the channel provides a lower L_g/Fin_{WIDTH} ratio than a double-gate FinFET for a same SCE control.[23] L_g/Fin_{WIDTH} as low as 1.0 was reported for Ω-Gate devices in [8]. *It is worthwhile noting that the minimum feature size in multi-gate technology is the fin width (Fin_{WIDTH}), and not the gate length.*

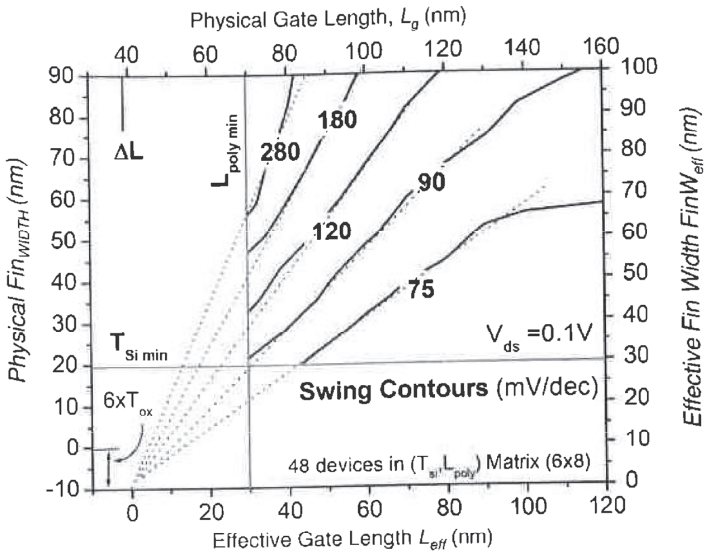


Fig. 2.3. Subthreshold swing contours for NMOS FinFET devices, V_d=0.1V. Fin_{WIDTH} varies from 20nm to 82.5nm in steps of 12.5nm, physical gate length; L_g varies from 70nm to 157.5nm in steps of 12.5nm. Contours are extrapolated with dotted lines to a common origin.[22] Copyright© 2001 IEEE.

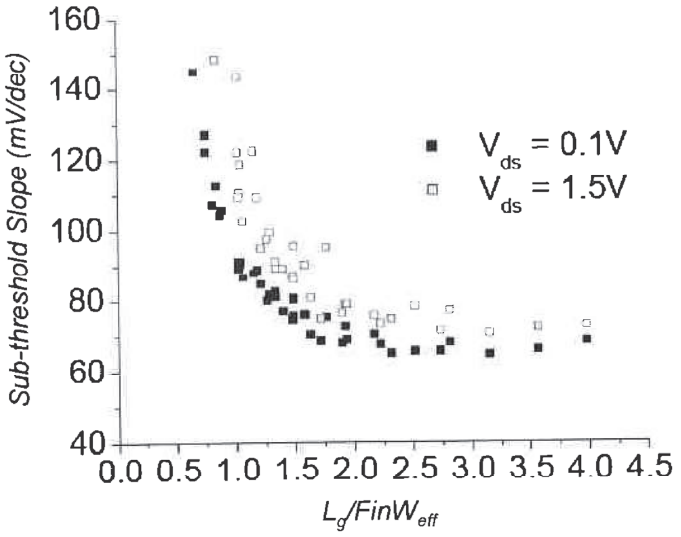


Fig. 2.4. Measured subthreshold swing *vs.* $L_g/FinW_{eff}$. Fin_{WIDTH} varies from 20nm to 90nm; L_g varies from 30nm to 120nm. The subthreshold slope is shown for both for V_d=0.1V and 1.5V.[22] Copyright© 2001 IEEE.

2.2.2 Fin Height and Fin Pitch

Having understood the requirements on Fin_{WIDTH} for SCE control, let us look at how fin pitch and fin height affect the drive current. For a double-gate FinFET, the channels are on the sidewalls of the fins. The effective channel width is thus equal to: [24]

$$W_{eff} = 2\,n\,Fin_{HEIGHT} \tag{2.13}$$

Where n is an integer number that is equal to the number of fins in a device. W_{eff} of multi-gate devices can only be increased or decreased by a discrete amount equal to $2\times Fin_{HEIGHT}$.[25]

The fin pitch, P_{FIN}, is the spacing between the fins plus the fin width. P_{FIN} is limited by the lithography pattern capability. Exactly one fin can be placed in one P_{FIN}. Therefore, the effective channel width per pitch is $2\times Fin_{HEIGHT}$. Figure 2.5 shows the layout comparison between a planar device and a FinFET. For the planar MOSFET, the effective device channel width, W_{eff}, is equal to the footprint on the substrate, W_{foot}. For FinFET, W_{eff} is related to W_{foot} through:

$$W_{eff} = 2Fin_{HEIGHT}\frac{W_{foot}}{P_{FIN}} \tag{2.14}$$

If we want the FinFET layout to be "competitive", we need $W_{eff} \geq W_{foot}$, or:

$$2Fin_{HEIGHT} \geq P_{FIN} \tag{2.15}$$

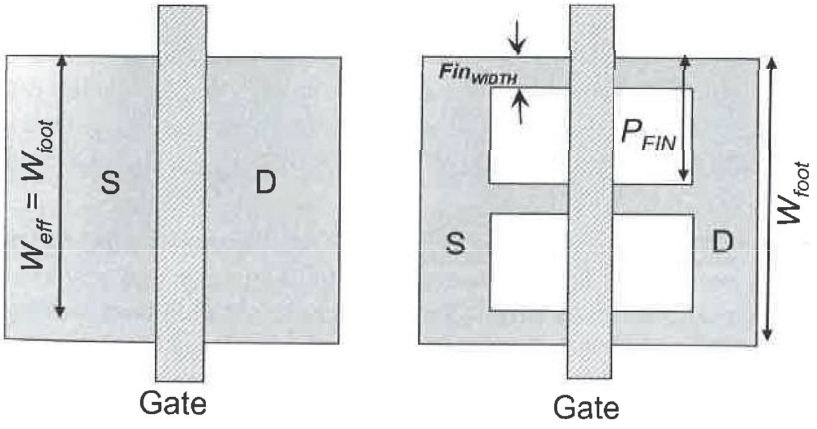


Fig. 2.5. Layout comparison between a planar MOSFET and a typical FinFET.

The analysis of the tri-gate channel width is further complicated by the "volume inversion" or "bulk inversion" effect reported in [26]. For thin fins, the inversion charge is not limited to the device surfaces. A large portion of the inversion charge is in the bulk of the fins, even at high gate voltages. Thus, without activating the top gate, multi-gate devices already have a significant charge at the top surface of the fins. Figure 2.6 shows the two-dimensional numerical simulation of carrier density on the top surface of 1) a tri-gate, 2) a double-gate and 3) a FinFET with a hard mask on top of the fin.

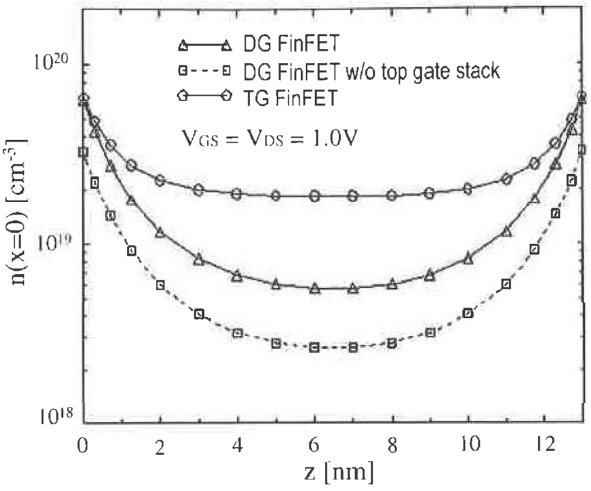


Fig. 2.6. Davinci prediction of on-state electron density along the top fin surface at the center of the channel (x =1/2 L_{eff}). DG stands for double gate. TG stands for tri-gate. Due to bulk inversion, the electron density on the top fin surface for DG FinFET is comparable to that in the TG device [26]. Copyright© 2005 IEEE.

Due to this "bulk inversion", the effective width, ΔW_{eff}, of the top gate in a tri-gate MOSFET is only a fraction of the physical top gate width. Numerical simulation in [26] shows ΔW_{eff} is a function of fin height and fin width.

For tri-gate devices, Equation 2.12 becomes: $2Fin_{HEIGHT} + \Delta W_{eff} \geq P_{FIN}$

Fins can be defined by conventional photolithography and reactive ion etch. Fins with width less than 20nm have been reported with 193nm dry photolithography processing.[27-28] Figure 2.7 shows the TEM cross section of some of these fins.[27-31] Continuing advances in lithography pitch and line dimension, including emerging 193nm photolithography and Extreme UV (EUV) lithography pave the way for further Fin_{WIDTH} and P_{FIN} reduction.

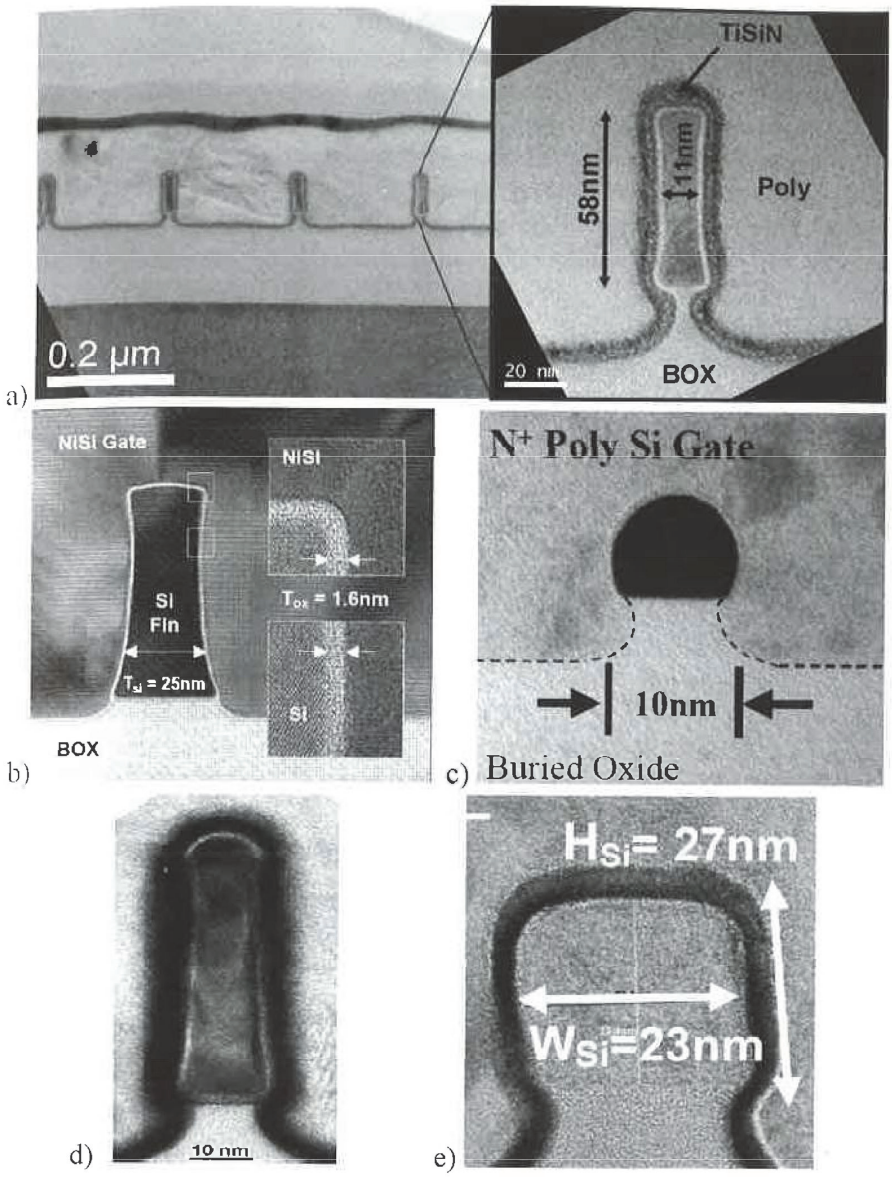


Fig. 2.7. Cross-sectional TEM of fins under gates. a) [27] Copyright© 2006 IEEE, b) [28] Copyright© 2002 IEEE, c) [29] Copyright© 2004 IEEE, d) [30] Copyright© 2005 IEEE, e) [31] Copyright© 2006 IEEE.

To increase the current drive per unit W_{foot}, we can increase Fin_{HEIGHT}, or reduce P_{FIN}. Both options have practical limitations. Increasing Fin_{HEIGHT} undermines the fin stability and increases the difficulty of gate patterning.

P_{FIN} is limited by the optical lithography capability. In order to improve P_{FIN} beyond optical lithography capability, spacer-defined fin patterning has been proposed.[32] Figure 2.8 shows the general concept. First a sacrificial pattern is defined with conventional optical lithography. Then spacers are formed on the sidewalls of the sacrificial pattern through thin film deposition and anisotropic reactive ion etch (RIE). The sacrificial pattern is subsequently selectively removed leaving the remaining spacers to serve as hard mask for fin etch.

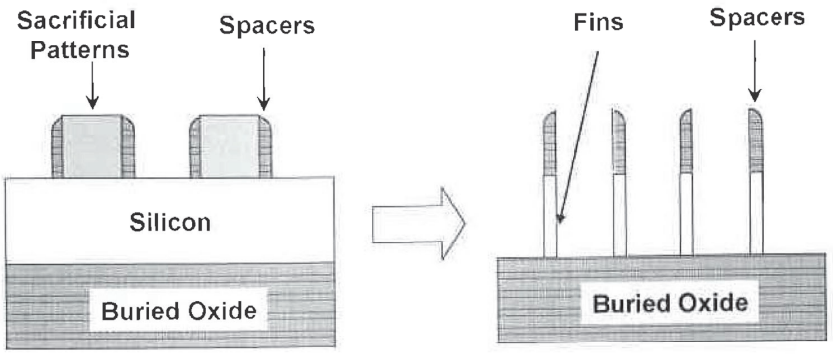


Fig. 2.8. Illustration of a spacer-defined fin formation process.

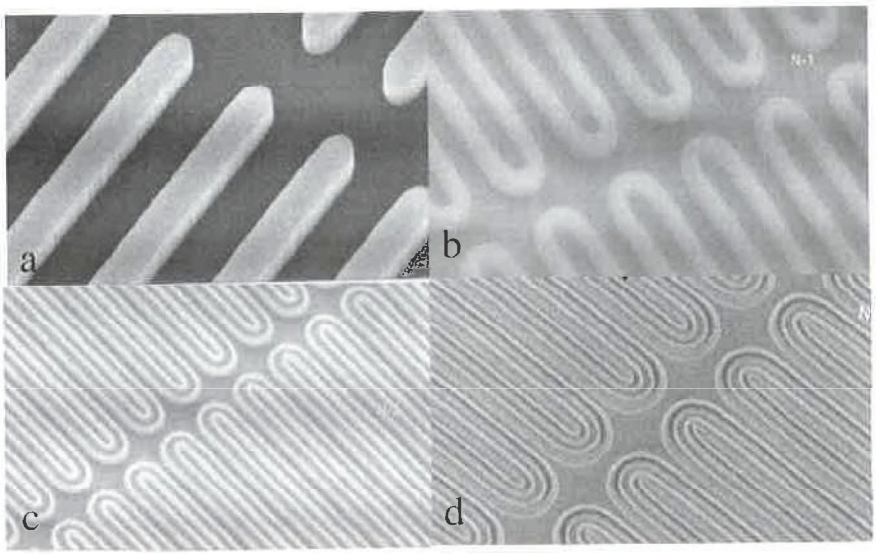


Fig. 2.9. SEM pictures of three progressive spacer-defined fin formation processes. a) initial optical lithography of sacrificial pattern. b) after first spacer imaging; c) after second spacer imaging; and d) after third spacer imaging. The final pattern pitch is 6 times smaller than the optical lithography pitch. REPRINTED WITH PERMISSION FROM [33]. COPYRIGHT 2003 AMERICAN INSTITUTE OF PHYSICS.

There are two advantages to spacer-defined fin formation. First, it doubles the number of fins for a given lithography pitch, *i.e.*: it reduces the fin pitch to half of the lithography pitch. In fact, when the spacer process is used twice, the pitch can be reduced by a factor of four. Figure 2.9 shows the SEM images of spacer imaging technique progressively being used three times.[33] Second, the fin width is defined by the thickness of deposited film, which has the potential to 1) be narrower than a lithography-defined fin, 2) have better CD control and 3) have reduced line-edge roughness.[32] The disadvantage of spacer-defined fin is that a clean-up mask is required to remove the fins where designers do not want them.[25] CMOS FinFET devices have been successfully fabricated using this imaging technique. Successful conversion of a planar microprocessor design into a spacer-defined FinFET microprocessor was also demonstrated in [25].

2.2.3 Fin Surface Crystal Orientation

Electrons and holes mobility depends on the orientation of the silicon surface as well as on the current flow direction.[34-36] Figure 2.10 shows the measured surface mobility of electrons and holes as a function of the inversion layer charge density.[37] For electrons, the highest mobility surface is (100) and the lowest mobility surface is (110). For holes, the (110) surface has the highest mobility and the (100) surface has the lowest mobility. Electrons and holes at a (111) surface have mobilities laying somewhere between those at (100) and (110) surfaces. The origins of the above differences are due to the anisotropy of effective mass and surface scattering.[35,36]

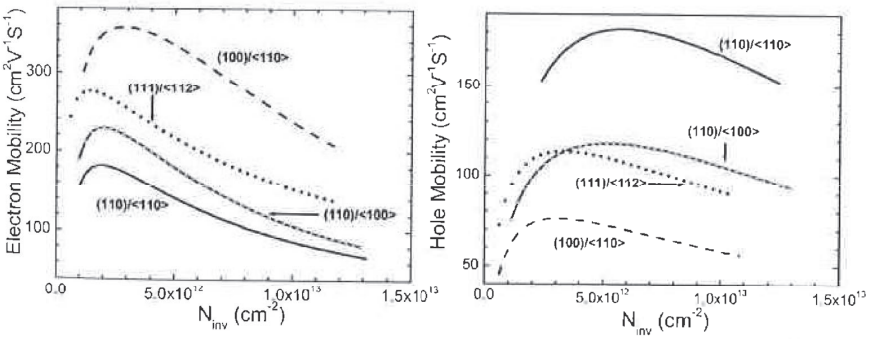


Fig. 2.10. Effective surface mobility of electrons and holes as a function of inversion layer charge density, for different surface orientations.[37] Copyright© 2003 IEEE.

Multi-gate MOSFETs have been fabricated on all 3 major Si surfaces [27,32,19]. The directions of the current flow for the respective surfaces are <100> for (100), <110> for (110) and <112> for (111). (110) Fin sidewall surfaces are made by patterning fins at 0 or 90 degrees with respect to the <110> notch on silicon wafers with a (001) surface orientation. This layout style is the same as for conventional planar devices. (100) fin surfaces are made by rotating the fin layout by a 45 degree angle with respect to the <110> notch direction. Figure 2.11 shows the layout directions of (100) fin surfaces and (110) fin surfaces.[38] Alternately, the Si top layer of the SOI wafers can be rotated by a 45 degree angle with respect to the substrate during bonding, to have the (100) surface fin layout at 0 and 90 degrees and the (110) surface at a 45 degree rotation.[39]

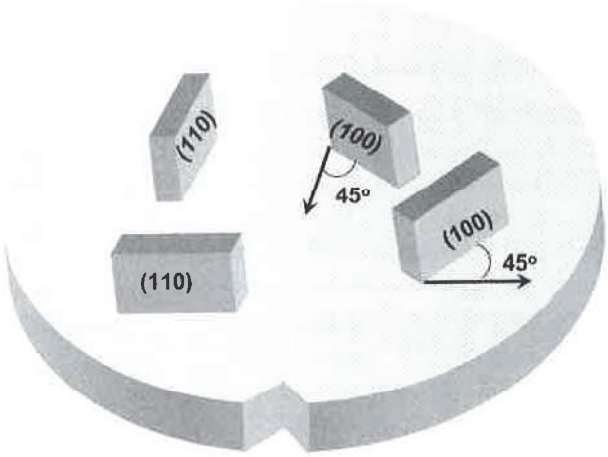


Fig. 2.11. Fins with (110)/<110> and (100)/<100> surfaces/directions can be readily made using standard Si substrate by rotating the fin layout by 45 degrees.

Having fins with both (110) and (100) surface orientation on the same chip allows one to optimize electron (NMOS) and hole (PMOS) mobility simultaneously. The price to pay for such devices is an increased layout area [41] and a higher photolithography process complexity. Optimizing optical lithography lines at 0, 90 and 45 degree angles is challenging. Figure 2.12 shows the comparison of a 6-transistor SRAM cell layout containing both (110) and (100) fins directions (mixed layout) with a standard layout with only one fin orientation. The mixed layout results in a 16.6% larger cell area.[41]

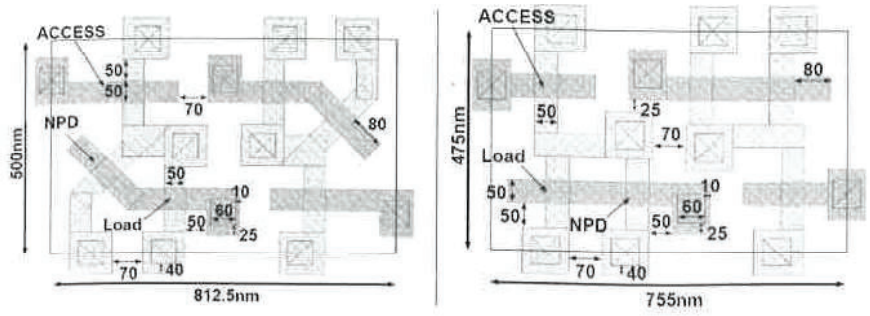


Fig. 2.12. 6-transistor SRAM cell layout comparison: standard layout (right) and layout with NMOS pull-down transistors rotated by 45 degrees (left).[41] Copyright© 2005 IEEE.

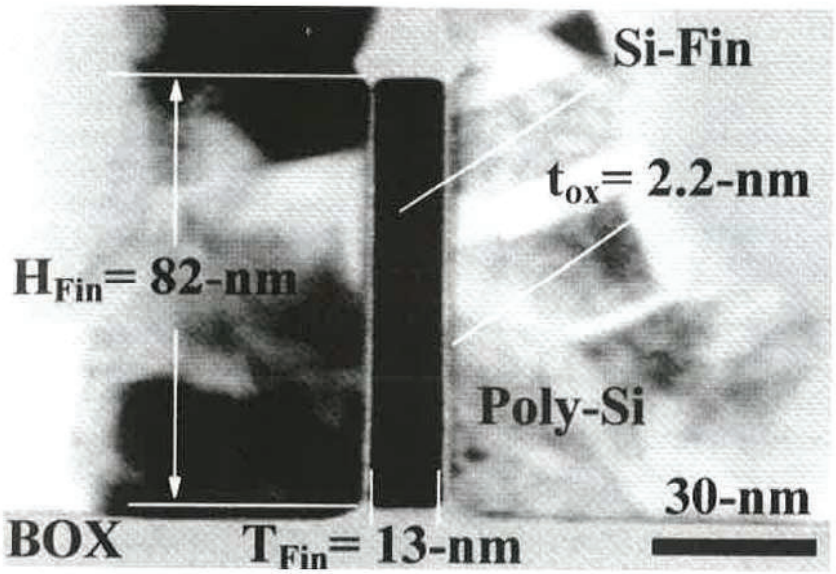


Fig. 2.13. Cross-sectional TEM of a (111)-surface sidewall fin. The smooth rectangular shaped fins were formed using surface-orientation dependent wet etch chemistry.[19] Copyright© 2003 IEEE.

The formation of (111) surface fins on (110) surface SOI substrates has been demonstrated.[19,42] In this experiment, fin patterns were aligned parallel to the <112> direction. The advantage of the (111) surface fins is that very smooth and straight fins can be formed by a wet etch process. The (111) surface silicon has an extremely low etch rate in tetramethylammonium hydroxide (TMAH) solution, compared with other crystallographic planes. The etch rate ration at 50°C for (110) planes