

versus (111) planes is 20:1. Thus, after initial plasma fin etch, an additional wet etch in TMAH can ensure very straight and smooth (111)-surface fins. Figure 2.13 shows the TEM of a smooth and vertical (111)-sidewall surface fin. One can appreciate the nearly perfect rectangular shape of the fin. The smoothness of the (111) surface fin using surface orientation dependent wet etch chemistry is very attractive. However, the drawback of this technique is that (111) surface carriers mobility is rather low. Furthermore, the mobility enhancement with strain engineering is not currently as well characterized on (111) as on the other two surfaces. Strain engineering will be further discussed in Section 2.5.

2.2.4 Fin Surface Preparation

The fin surfaces exhibit significant roughness right after plasma etch. In addition, the fin corners are sharp. Gate oxide grown on these surfaces is prone to defects and localized thinning. Without proper treatments, silicon crystal defects such as twin formation in the fin corners could happen.[40] Sharp corners also result in a kink in the subthreshold region if the fin doping level is high.[43] Such kinks are caused by parasitic corner devices, which have a lower threshold voltage than the sidewalls due to the higher electrical field in the corners. The fin corner problem is similar to the parasitic STI edge device effect that can be found in planar CMOS technologies.

Carrier mobility along the fin sidewalls without treatment is rather poor.[44] The simplest way to repair surface roughness and damage from the plasma etch is through oxidation. The requirement for fin sidewall smoothing oxidation is similar to STI liner oxidation. It is desirable to have conformal oxidation with a growth rate that is insensitive to the fin surface orientation. In-Situ-Steam-Generated (ISSG) rapid thermal oxidation has such desired properties.[45-46]. ISSG typically uses pressure above 5 Torr. Hydrogen and oxygen are introduced simultaneously into the chamber. The reactants remain as free species (O_2 and H_2) until they reach the wafer surface, where heat induces a local reaction. O_2 and H_2 react to form steam and oxygen radicals. The unstable oxygen radicals promote further oxidation. As a result, the oxidation is conformal and has no surface orientation preference. In addition, ISSG has the advantage of being insensitive to the doping level in the silicon and it provides better corner rounding than conventional oxidation.

The sacrificial smoothing oxide is typically removed using a hydrofluoride (HF)-based isotropic wet etch step.[40] Some of the buried oxide

in the SOI substrate is etched at the same time as the sacrificial oxide. As a result, buried oxide recesses below the bottom fin surface and creates the Π/Ω -shaped gate (See Fig. 2.8a). Π/Ω -Gate MOSFETs take advantage of such buried oxide recess to improve the gate electro-static control of the channel.[7-8] However, such a recess can undermine the fin stability if the fin width is scaled below 10nm.

H₂ annealing is another way to smooth the fin surfaces and round the corners. H₂ annealing has been shown to: 1) improve electron mobility, 2) reduce gate leakage and 3) lower 1/f noise.[11,12,47] The H₂ annealing process conditions have a great impact on the final shape of the fins. If the temperature is too high and/or the pressure is too low, the Si fins can agglomerate and break. The narrower the fins, the more sensitive they are to the H₂ annealing conditions.

2.2.5 Fins on Bulk Silicon

The fins we described so far are fabricated on SOI wafers. MuGFETs can also be made on bulk silicon wafers.[48-53] In some references they are called body-tied FinFETs or bulk FinFETs. The main advantages of using bulk silicon over SOI substrates are 1) lower wafer cost and 2) better substrate heat transfer rate. However, bulk multi-gate MOSFET require additional isolation steps, which increase the cycle time and cost. Furthermore, the fin height of bulk-based multi-gate devices are entirely determined by the fin etch step. This puts more pressure on etch variation control, since any fin height variation translates into transistor width variation.

The control of the electrical potential by the gate in bulk fins is as good as in their SOI counterparts. But underneath the fin, in bulk devices, the source and drain have to be separated by heavy channel stop implants to prevent sub-surface punchthrough. As a result, multi-gate devices made on bulk silicon suffer from higher source and drain diode leakage and higher junction capacitance than devices made in SOI.

The bulk silicon under the fin can be accessed by a body contact. But the body factor of a bulk FinFET is very low, since the electrostatic potential inside the fins is dominated by the gate, not by the body. Therefore, body bias is not effective in changing the threshold voltage of a bulk multi-gate MOSFET. Figure 2.14 illustrates the general fabrication process of a bulk MuGFET.

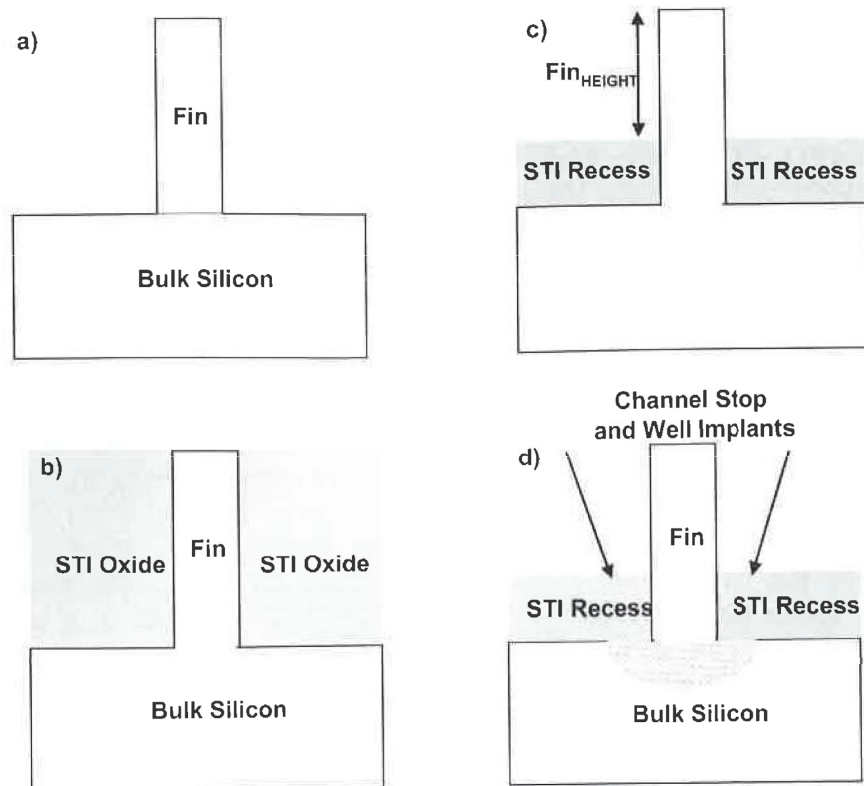


Fig. 2.14. General process flow for making a FinFET on a bulk silicon bulk wafer. a) Fin etched in bulk silicon, the initial Fin_{HEIGHT} is greater than final device Fin_{HEIGHT} to allow some STI (Shallow trench Isolation) oxide. b) STI oxide deposition and planarization. c) STI oxide recess to expose silicon fin with desired Fin_{HEIGHT} . d) Channel stop and Well implants. Channel stop is needed to prevent the source and drain punch through below the fin in the bulk silicon.

2.2.6 Nano-wires and Self-Assembled Wires

The ultimate MOSFET structure is a cylindrical wire-like gate all-around device, as show in Figure 2.15. This structure provides the best electrostatic control of the channel by the gate [54]. The natural length, λ , for such a device is given by Equation 2.16.

$$\lambda = \sqrt{\frac{2\epsilon_{si}t_{si}^2 \ln(1 + \frac{2t_{ox}}{t_{si}}) + \epsilon_{ox}t_{si}^2}{16\epsilon_{ox}}} \quad (2.16)$$

where t_{si} is the diameter of the wire. To keep short-channel effects under control, t_{si} shrinks with gate length. When t_{si} is below 10nm, the device structure is typically called a “nanowire MOSFET”.

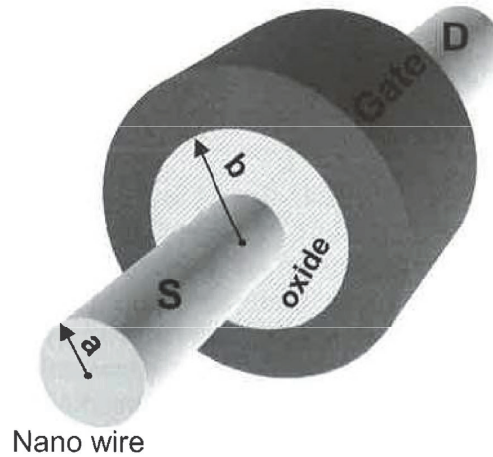


Fig. 2.15. Illustration of a silicon nanowire transistor. The gate stack is wrapped around the semiconductor nanowire. a is the radius of the nanowire.

Because the nanowire transistor has a cylindrical cross section, its capacitance can no longer be calculated using a simple parallel-plate model. Considering Figure 2.15, the inversion charge in the nanowire can be approximated by a charge sheet on the outer surface of the wire. The charge on the gate is on the inner wall of the gate electrode. The capacitance can be obtained by calculating the voltage drop across the gate oxide. Applying Gauss’s law to an infinitely long cylinder one can find the electrical field outside the cylindrical wire:

$$E = \frac{Q}{2\pi\epsilon_{ox}r} \quad (2.17)$$

Where Q is the charge per unit length at the surface of the wire, and r is the radius of the wire. The voltage drop across the gate oxide can be found by integrating the electrical field along a radial line:

$$\Delta V = \frac{Q}{2\pi\epsilon_0 r} \int_a^b \frac{1}{r} dr = \frac{Q}{2\pi\epsilon_{ox} r} \ln\left(\frac{b}{a}\right) \quad (2.18)$$

where a is the nanowire radius, and $b = a + t_{ox}$. The capacitance per unit gate length is:

$$\frac{C_g}{L_g} = \frac{Q}{\Delta V} = \frac{2\pi\epsilon_{ox}}{\ln(\frac{b}{a})} \quad (2.19)$$

Converting Equation 2.19 to a capacitance per unit area of the nanowire surface, we obtain:

$$\frac{C}{A} = \frac{2\pi\epsilon_{ox}}{\pi a \ln(\frac{b}{a})} = \frac{2\epsilon_{ox}}{a \ln(\frac{b}{a})} \quad (2.20)$$

Equation 2.20 indicates the effective gate capacitance of the nanowire transistor is a function of the nanowire radius as well as the gate oxide thickness. This relationship can be exploited to reduce the effective gate oxide thickness without using higher k dielectric. As an example, a nanowire MOSFET with $a=4\text{nm}$, $t_{ox} = 2\text{nm}$, the effective gate oxide thickness is 1.62nm. The above calculation does not take bulk inversion or quantum-induced volume inversion effects into account. In those cases, the effective nanowire radius is decreased, since the charges are not limited to the nanowire surface.

Silicon nanowires can be made with conventional patterning described in section 2.2.2. A circular cross section can be made by first removing the buried oxide below the silicon, and then rounding of the wires to an approximately circular cross section can be achieved using H_2 annealing.[29]

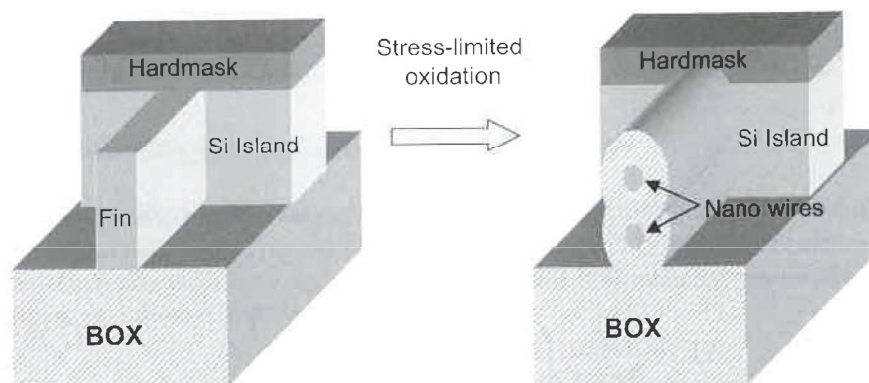


Fig. 2.16: Twin Si nanowires formed through stress-limited oxidation. A hard mask is needed to keep the Si island region from oxidizing. The presence of Si island at the end of the wires is needed to anchor the wires.

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A twin-wire structure has been made using stress-limited oxidation of tall fins. The stress-limited oxidation oxidizes the wire slower than planar silicon, which produces a final structure comprising two Si wires, one on the top of the fin, and the one other at the bottom of the fin (Figure 2.16). It is important to protect the source and drain region during the oxidation. After removing the oxide, two silicon wires are formed.[55] Twin nanowires can also be formed by oxidation using doping-dependent oxidation rate effects.[126]

The formation of high-density, self-assembled nanowires has been demonstrated using cylindrical-phase diblock copolymers.[56] The polymer has the ability to divide a lithographic pattern (W) into integer number of sub-unit with a distance, l , between cylinders. l is intrinsic length of the polymer which determine the number of sub-units (n) fits in W . The relationship between n and l is defined by Equation 2.21.

$$n = \frac{2}{\sqrt{3}} \left(\frac{W}{l} \right) \quad (2.21)$$

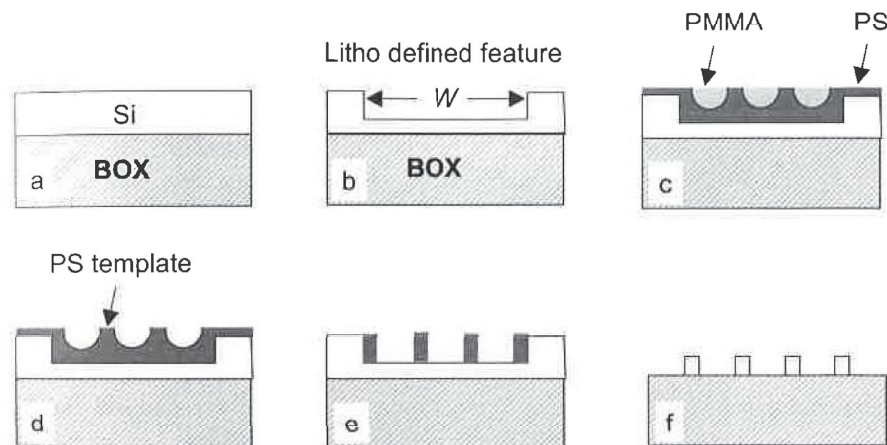


Fig. 2.17: Self-assembled nanowire formation. The initial lithothography-defined pattern on an SOI wafer (a,b) is divided into self-aligned patterns by cylindrical-phase diblock copolymers (c). d) PS template formation for plasma etching (e). The remaining PS features are used as mask to etch the silicon nanowires (f).

The self-assembly process is illustrated in Figure 2.17. The sidewalls of the lithography-defined trench initiate the assembly of the polymer domain. In Reference 56, diblock copolymers composed of 70% polystyrene (PS) and 30% poly (methyl-methacrylate) (PMMA) (70:30 PS:PMMA) with total molecular weight $M_n=64$ kg/mol are shown to form

hexagonal lattices of 20 nm diameter cylindrical PMMA domains ($l = 35$ nm) in a matrix of PS. After film assembly, PMMA is removed from the half-cylinder domains by immersing the substrate in acetic acid. Plasma etch is then used to define the Si nanowires.

2.3 Gate Stack

2.3.1 Gate Patterning

This section presents the process steps used in the gate formation of a multi-gate MOSFET. The topography created by the fins presents many challenges. One of these challenges is illustrated in Figure 2.18: photoresist has a surface planarization effect when deposited on a non-planar topography. The wavy gate material stepping over the fins results in different photoresist thickness along the width of the transistor. The photoresist critical dimension (CD) after exposure is a function of the resist thickness. This effect is known as “swing curves”. Without gate planarization, gate CD will vary periodically through the entire width of the device, with a period equal to the fin pitch (Figure 2.18). Therefore, the use of a planarized gate is highly desirable.

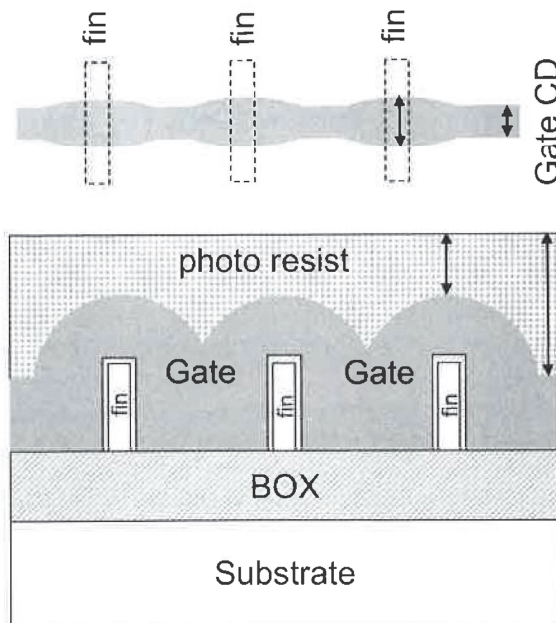


Fig. 2.18. Patterning gate on an irregular topography results in wavy gate CD due to the variation in resist thickness. A planarization step is required.

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