

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd. and Apple Inc.,

Petitioners

v.

Marlin Semiconductor Ltd.,

Patent Owner

Patent No. 9,953,880 B1

Filing Date: July 27, 2017

Issue Date: April 24, 2018

Title: SEMICONDUCTOR DEVICE
AND METHOD FOR MANUFACTURING THE SAME

Inter Partes Review No. IPR2025-00848

**DECLARATION OF DR. SUMAN DATTA, PH.D.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 9,953,880**

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I, Dr. Suman Datta, Ph.D., declare as follows:

I. Introduction

1. My name is Dr. Suman Datta. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in connection with a petition for *inter partes* review of U.S. Patent No. 9,953,880 (’880 Patent), which I have been told is being submitted to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-12 of the ’880 Patent (Challenged Claims).

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the bases for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the ’880 Patent is unpatentable for at least the reasons I discuss below.

II. Background and Qualifications

A. Education and Career

5. I have over 20 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of transistors.

6. I received a Ph.D. degree in Electrical Engineering from the University of Cincinnati in 1999. Before that, I received a Bachelor's degree of Electrical Engineering from the Indian Institute of Technology in 1995.

7. I was employed at Intel Corporation ("Intel") in the Advanced Transistor and Novel Device Group from 1999 to 2007. During that time, I developed multiple generations of high-performance logic transistor technologies including high-k/metal gate, tri-gate (FinFET), and non-silicon CMOS transistors. In 2002, I received the Intel Logic Technology Quality Award. In 2003, I received the Intel Achievement Award.

8. From 2007 to 2011, I was the Monkowski Associate Professor of Electrical Engineering at the Pennsylvania State University. From 2011 to 2015, I was a Professor of Electrical Engineering at the Pennsylvania State University. In 2012, I received the Penn State Engineering Alumni Association Outstanding Research Award. In 2015, I received the Penn State Engineering Alumni Premier

Research Award. Between 2015 and 2022, I was the Stinson Professor of Nanotechnology in the Department of Electrical Engineering at the University of Notre Dame in Notre Dame, Indiana.

9. Since 2022, I have been the Joseph M. Pettit Chair in Advanced Computing, a Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology in Atlanta, Georgia, and a Georgia Research Alliance (GRA) Eminent Scholar.

10. From 2015 till 2022, I served as the Director of the SRC/DARPA sponsored Applications and Systems-driven Center for Energy-efficient integrated NanoTechnologies (ASCENT). I also served as the Director of the SRC/NSF sponsored Center for Extremely Energy Efficient Collective Electronics (EXCEL). Currently, I serve as the Thrust Leader in the Center for Processing with Intelligent Storage and Memory (PRISM), one of the DARPA-SRC sponsored JUMP 2.0 research centers.

11. I have chaired IEEE conferences and served on the Technical Program Committee of various top-tier IEEE conferences, including International Electron Device Meeting, VLSI Technology Symposium, Device Research Conference and International Reliability Physics Symposium. In 2013, I was named an IEEE Fellow for my contributions to high-performance advanced silicon and compound semiconductor transistor technologies. In 2016, I was named a Fellow of the

National Academy of Inventors (NAI) in recognition of my inventions that made a tangible impact on quality of life, economic development, and the welfare of society.

12. As a result of my industry work, I am familiar with various areas of integrated circuit technology. I have worked extensively on the use of shallow trench isolation (“STI”) and device isolation in FinFET manufacturing processes, novel low resistance source and drain regions, gate stacks, silicides (titanium, cobalt, and nickel silicide), and low resistance tungsten plugs. Throughout 1991-2004, I was part of the Intel research team that experimentally demonstrated high-performance NMOS and PMOS tri-gate (i.e., FinFET) transistors in which the channel strain, high-k gate dielectric, gate electrode work functions, epitaxial source-drain regions were co-optimized together with the fin dimensions and the fin shape.¹ My work experience has also extended to layout design rules, oxide and nitride spacer formation, FinFET gate and fin patterning, gate oxides, gate electrodes, contacts, silicide, copper interconnects, process integration (lithography, etch, diffusion, thin film deposition, and chemical mechanical polishing), and yield and reliability.

13. In addition, I am familiar with FinFET technology and manufacturing techniques. A “FinFET” (a combination of “Fin” and Field Effect Transistor (FET))

¹ See, e.g., J. Kavalieros, S. Datta et al., “Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering,” Digest of Technical Papers, 2006 Symposium on VLSI Technology, 2006, Honolulu, HI, pp. 50-51 (2006).

is a three-dimensional transistor fabricated on vertical fins instead of a flat surface like a planar transistor. I was honored at the 2022 IEEE Symposium on VLSI Technology and Circuits, along with my co-authors and former colleagues at Intel Corporation for my 2006 research paper titled, “Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering” (*see footnote 1 above*). True to its name, the Test of Time Award recognizes papers that have established their significance in history by standing the test of time.² The goal of the award is to honor impactful papers and promote their recognition in the Symposia’s community.

14. I have also developed and taught graduate level courses on FinFETs, transistor layout, and fabrication at Pennsylvania State University, the University of Notre Dame, and Georgia Tech, including a course covering FinFET technologies and another course covering scaling and limits of FinFETs and transistor options such as Gate-All-Around (GAA) FETs that might replace FinFETs during the second half of the current decade.

15. I have experience analyzing transmission electron microscope (“TEM”) images at Intel, Pennsylvania State University, University of Notre Dame, and Georgia Tech.

² <https://ece.gatech.edu/news/2023/12/datta-receives-vlsi-technology-and-circuits-test-time-award>.

B. Publications

16. I am a named inventor on 187 granted United States patents and have authored more than 475 peer-reviewed academic journal publications. I have also co-authored 11 book chapters.

17. In 2010 and 2011, I received the Best Paper Award from the Device Research Conference and in 2022 I received the Test-of-time award from VLSI Technology Symposium.

18. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which I understand is being included as Exhibit 1004. Additional details about my employment history, fields of expertise, awards, publications, and other activities are further included in my curriculum vitae.

19. I am being compensated for services provided in this matter at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the Challenged Claims. I have no financial interest in the outcome of this matter or in any litigation involving the '880 patent."

20. I have no financial interest in the outcome of this matter or in any litigation involving the '880 patent. I also do not have any financial interest in the

Patent Owner. I do not have any financial interest in the '880 Patent and have not had any contact with any of the named inventors of the '880 Patent (Chun-Hao Lin, Hsin-yu Chen, Shou-Wei Hsieh) about the '880 Patent or any issues in this Investigation.

III. Materials Reviewed

21. In forming my opinions regarding the '880 Patent, I reviewed the references listed in Appendix A. All citations to page numbers in the references listed in Appendix A are to the page numbers of the original references, not the stamped exhibit page numbers.

IV. Legal Standards

22. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '880 Patent are patentable, I have been told that I am obliged to follow existing law.

A. Anticipation

23. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. §102, a provision in the patent law regarding anticipation. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

24. I have been told that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

25. I have been told that under 35 U.S.C. §103(a), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in Section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

26. When considering the issues of obviousness, I have been told that I am to do the following:

- a. Determine the scope and content of the prior art;
- b. Ascertain the differences between the prior art and the claims at issue;
- c. Resolve the level of ordinary skill in the pertinent art; and
- d. Consider evidence of secondary indicia of non-obviousness (if available).

27. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the effective filing date of the '880 Patent, which I have been asked to assume is June 29, 2017.

28. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and any objective indications of non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '880 Patent).

29. I have been told that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed as of the effective filings date.

30. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper obviousness analysis requires determining whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

31. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art.

In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

32. I have been told the reasons a person of ordinary skill in the art would have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

33. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields there may be little discussion of obvious combinations, and, in these fields, market demand—not scientific literature—may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

34. I have been told that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine them. But I also understand that any “teaching, suggestion, or motivation” present in the prior art may be useful in establishing a rationale for combining aspects of the prior art. I have been told this “teaching, suggestion, or motivation” test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis (i.e., viewing the question of patentability based on knowledge that a person of ordinary skill in the art would not have possessed as of the effective filing date).

35. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

36. I have been told that when there is a known technique to address a known problem using prior art elements according to their established functions, then a person of ordinary skill in the art would have had a motivation to combine.

37. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference

is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address; or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

V. Level of Ordinary Skill in the Art

38. In my view, a person having ordinary skill in the art for the '880 Patent would have had a master's degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing, as of June 29, 2017. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for less formal education.

39. Again, I have been asked to assume the effective filing date for the '880 Patent is June 29, 2017. All the prior art discussed in this declaration predates June 29, 2017, so I have been asked to assume it qualifies as prior art. I have also been asked to treat June 29, 2017, as the date from which to assess the knowledge available to a person of ordinary skill in the art.

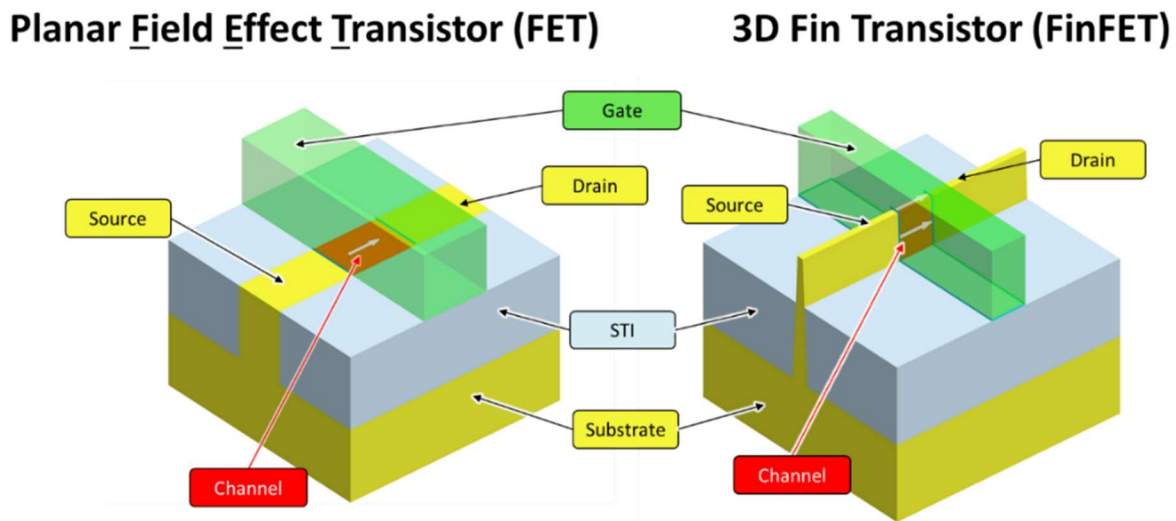
VI. Technological Background

40. In my opinion, all the elements in claims 1-12 of the '880 Patent were well known before June 29, 2017. A person of ordinary skill in the art at that time

would have been familiar with the background information described in subsections A through D below.

A. Planar and Non-Planar FETs

41. Two types of transistors common in the semiconductor industry are planar Field Effect Transistors (“FETs”) and Fin-shaped Field Effect Transistors (“FinFETs”). Other than the protruding “fin” illustrated on the right below, planar FETs and FinFETs are the same. The two simplified diagrams below illustrate a basic planar FET design (on the left) and a basic FinFET design (on the right).



42. The basic operation of both planar FET and FinFET structures is likewise the same. A “Gate” is positioned between the “Source” and “Drain” regions. (Sze at 433-34.) During operation of the transistor, current flows between the source and drain regions through a channel underneath the gate represented by the arrow above between “Source” and “Drain.” (Sze at 433-34 (“When a

sufficiently large positive bias is applied to the gate so that a surface inversion layer (or channel) is formed between the two n^+ regions, the source and the drain are then connected by a conducting-surface n channel through which a large current can flow.”), 438 (“If a small drain voltage is applied, a current will flow from the source to the drain through the conducting channel.”), Figs. 3, 6.)

43. Similarly, the underlying physics of the current flow through the channel is not affected by whether the channel is in the plane of a shallow trench isolation (“STI”) in the substrate, as in the planar FET, or the channel is in the fin, as in the FinFET. Current flow dictates whether the transistor is “on” (current) or “off” (no current). A typical transistor can be thought of in simple terms as a switch turned off and on by a voltage applied to the gate. (Plummer at 71-82 (“Probably the single most important parameter in both the NMOS and PMOS devices is the turn-on or threshold voltage, discussed in Chapter 1 and usually called V_{TH} In modern CMOS circuits, the target threshold voltage is generally around 0.5-0.8 volts for both the NMOS and PMOS devices. (The threshold voltage is positive for the NMOS devices and negative for the PMOS devices so that both transistors are normally off, enhancement mode devices.).”).)

44. The basic fabrication of planar FETs and FinFETs is similar, except for the formation of the fin shape. As one author correctly summarized: “The process flow starts the fin formation similarly as the formation of active area (in planar

CMOS) and followed by STI gap-fill and planarization and oxide recessing to reveal the fins. Then the rest of flow proceeds to similar steps (e.g. well, gate, epi-S/D, etc.) as the planar CMOS with gate-last high-k and metal-gate (HKMG) flow.” (Chi at 1.) As the original FinFET patent (filed in 2000) states in the very first sentence of its abstract, “A FinFET device is fabricated using conventional planar MOSFET technology.” (Hu at Abstract; *see also* Hu at 2:11-14 (explaining that FinFETs are just “an extension of conventional planar MOSFET technology”), 5:37-40 (explaining that FinFETs are made using a process that “is compatible with conventional planar MOSFET fabrication techniques”); Doyle at 133 (explaining that a FinFET “very much resembles [a] bulk transistor from the processing point-of-view”).) This allowed FinFETs to succeed commercially because they could be integrated using existing planar technology.

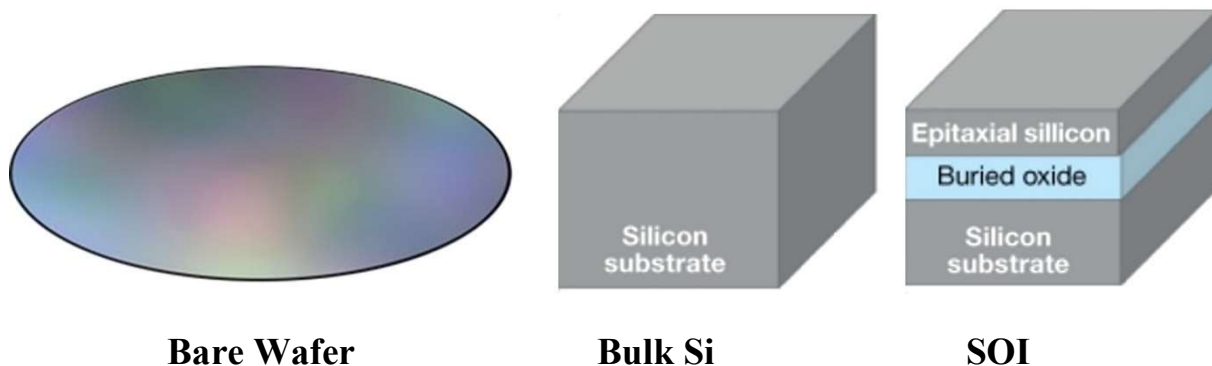
45. The invention of the FinFET around the year 1999 was led by Chenming Hu, who also served as Chief Technology Officer of TSMC. Dr. Hu was awarded by President Obama the National Medal of Technology and Innovation for his FinFET invention. (<https://nationalmedals.org/laureate/chenming-hu/>.)

B. Bulk Silicon FinFETs vs. SOI FinFETs

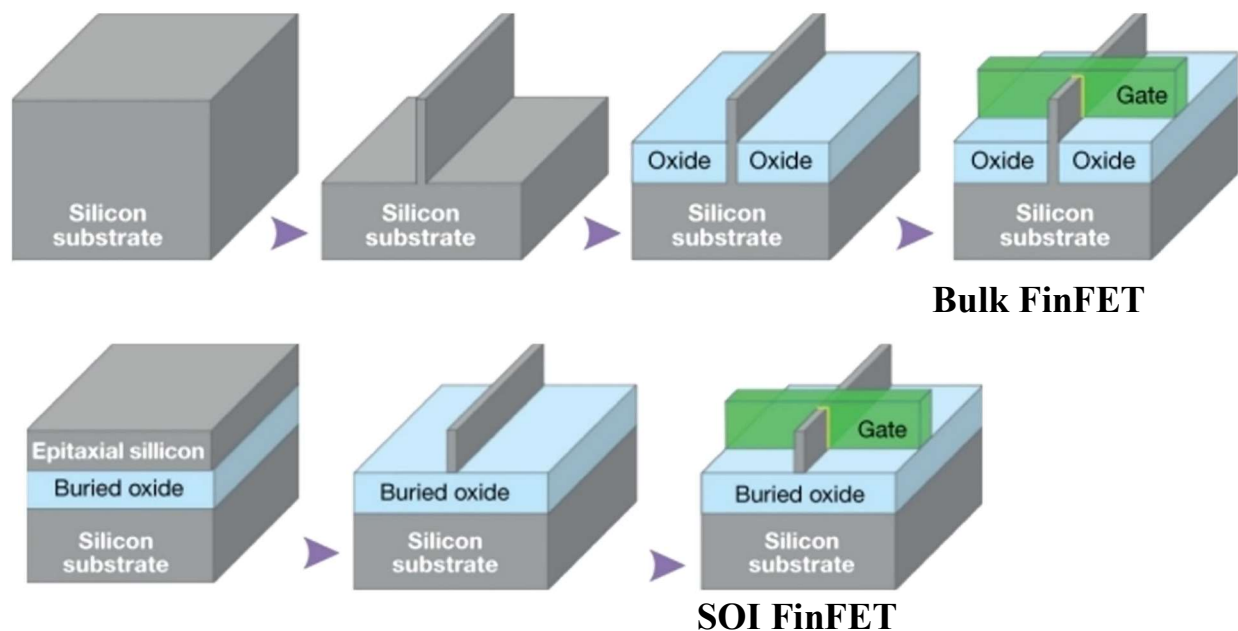
46. Substrates in semiconductor manufacturing are generally in the form of a disk called a “wafer.” (Colinge at 15 (“The bulk FinFET is a FinFET made on bulk silicon instead of an SOI wafer. Fins are etched on a bulk silicon wafer and trimmed

using an oxidation step.”), 65 (“The fins we described so far are fabricated on SOI wafers. [They] can also be made on bulk silicon wafers.”), FIG. 2.14 (“General process flow for making a FinFET on a bulk silicon bulk wafer.”); Ha ¶[0066] (“The substrate 100 may include a silicon wafer.”), ¶[0092] (“The substrate 100 may include one of a single crystal silicon wafer, a silicon germanium (SiGe) wafer, and a silicon on insulator (SOI) wafer.”).)

47. As shown below, a “bulk” silicon wafer is made only of silicon while a silicon-on-insulator (“SOI”) wafer includes a buried silicon oxide layer between a bulk silicon substrate below and another epitaxial silicon layer above. (Colinge at 50-51, 65-66, FIGS. 2.2, 2.14.)

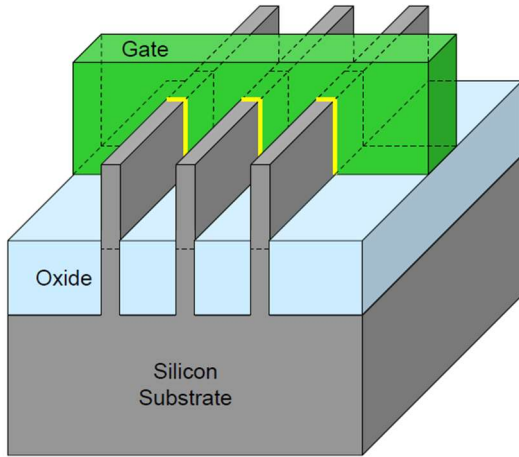


48. As shown below,³ the only notable difference between FinFETs made using a bulk silicon wafer and FinFETs made using an SOI wafer is that fins in bulk silicon are electrically isolated by a shallow trench isolation (“STI”) oxide that surrounds the fins, whereas the fins made using an SOI wafer are electrically isolated by the buried oxide layer underneath the fins. (Colinge at 50-51, 65-66, FIGS. 2.2, 2.14.) Once the fins and isolation are formed, the same basic process flow can typically be applied to either substrate type. (See Chi at 1-2, Fig. 1; Hu at 4:51-65; Zhao at 5:29-34; Xie616 at 7:41-48; Xie078 ¶[0027]; Xie790 ¶[0021].) This allowed FinFETs to succeed commercially because they could be integrated using existing planar technology.

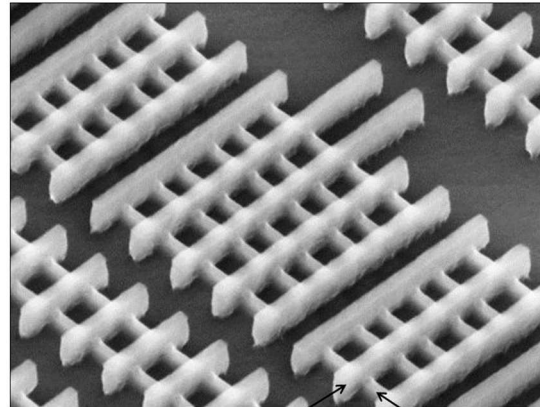


³ M. Swinnen & R. Duncan, “Physical Verification of FinFET and FD-SOI Devices,” Tech Design Forum (May 2, 2013), <https://www.techdesignforums.com/practice/technique/physical-verification-design-finfet-fd-soi/>.

49. The first commercial FinFETs in 2011 (see below)⁴ used bulk silicon substrates, and they have been widely used in the industry for FinFETs ever since.



Intel_22nm_Details at 7



Intel_22nm_Details at 8

C. Diffusion Breaks

50. When fabricating a FinFET integrated circuit, the fin structures are initially formed as long strips in large areas of the substrate. (Xie616 at 2:62-64 (“In one illustrative prior art process flow, the fins for an integrated circuit are initially formed uniformly across the entire substrate (i.e., a ‘sea of fins’).”); Wu at 1:44-49 (“One manufacturing technique that is employed in manufacturing FinFET devices is to initially form the trenches 14 in the substrate 12 to define multiple ‘fins’ that extend across the entire wafer or substrate 12, and thereafter remove some of the fins 16 where isolation structures will be formed.”).) Those long strips are then “cut” by etching trenches through them, yielding shorter strips suitable for transistors.

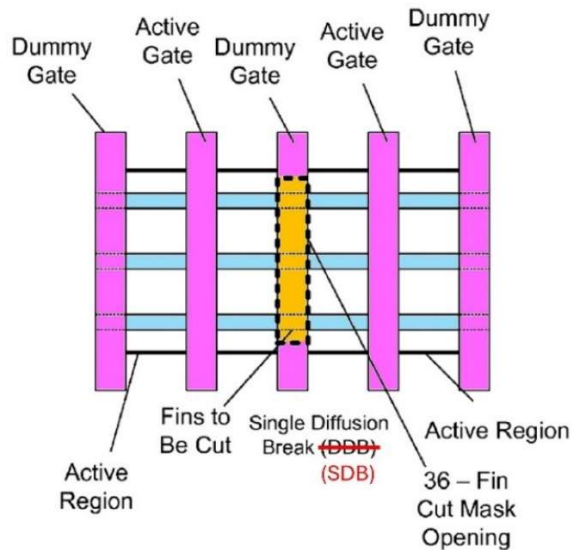
⁴ Intel_Newsroom; Intel_Announcement at 5, 8, 10-12, 16, 24; Intel_22nm_Details at 2, 5-10, 14, 22-23, 27.

51. Because the transistors must be electrically isolated from one another, those fin-cutting trenches are filled with an insulator (e.g., silicon oxide or silicon nitride). (Xie616 at 2:48-3:4 (“The various transistor devices that are formed for an IC product must be electrically isolated from one another to properly function in an electrical circuit. Typically, this is accomplished by forming a trench in the substrate 12, and filling the trench with an insulating material, such as silicon dioxide. . . . Cutting the desired portions of the fins is typically accomplished by forming a so-called ‘fin cut’ patterned etch mask with openings corresponding to the portions of the fins to be removed. The space previously occupied by the removed portions of the fins is then filled with an insulating material.”).) In the industry, these insulating fin-cutting structures are sometimes called “diffusion breaks.” (Xie616 at 2:48-54 (“Within the industry, these isolation regions may sometimes be referred to as ‘diffusion breaks.’”)).)

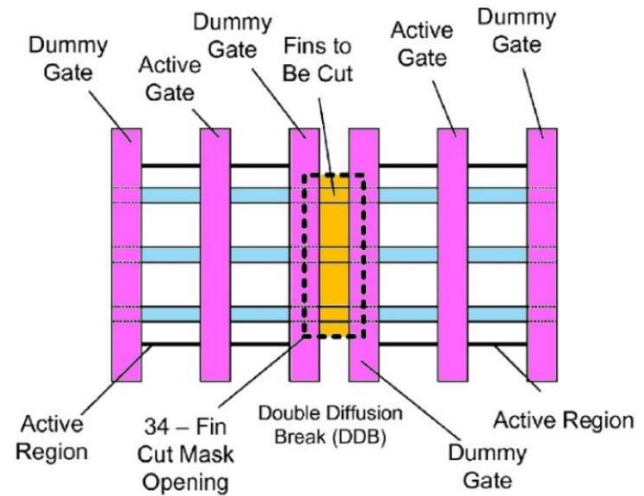
52. Single diffusion breaks (“SDBs”) and double diffusion breaks (“DDBs”) were both well known before the ’880 Patent. (Xie616 at 3:49-59, FIGS. 1C-1H.) In the figures below, the initial fin structures (blue) run horizontally; the gate structures (magenta) run vertically; and the orange highlights indicate the diffusion breaks.⁵ (Xie616 at FIGS. 1E, 1H.) The double diffusion break (DDB)

⁵ Note that the “DDB” parenthetical in FIG. 1H is a typographical error. It should read “SDB.”

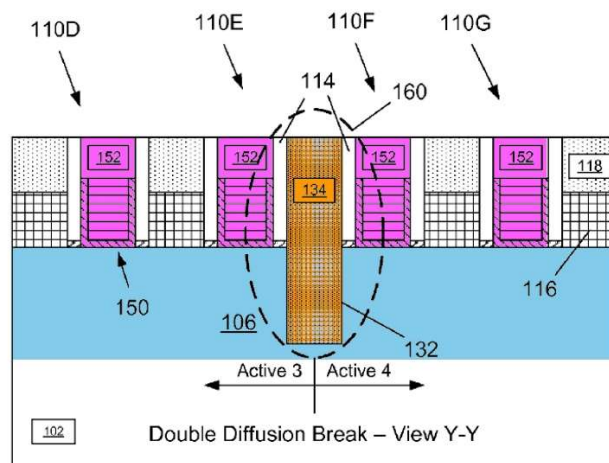
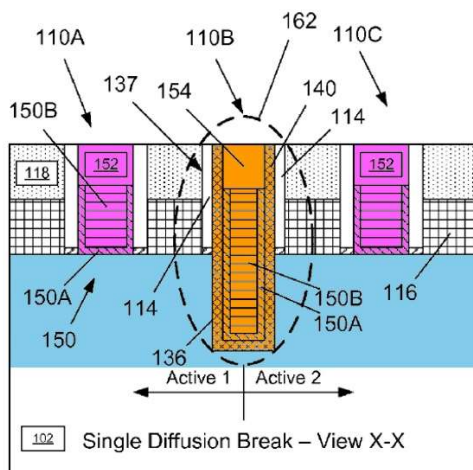
below is positioned adjacent to dummy gates 152, but the single diffusion break (SDB) is positioned adjacent to source/drain regions 116.



Xie616, FIG. 1H⁶



Xie616, FIG. 1E



Xie616, FIG. 2S

⁶ Throughout this declaration, I have added colors to certain figures for emphasis.

53. Although DDBs are generally easier to fabricate, SDBs are preferable for device scaling because they allow for increased packing density. (Xie616 at 3:59-67 (“In general, it is easier to form a double diffusion break (DDB) isolation structure than it is to form a single diffusion break (SDB) due to the relatively larger size of the double diffusion break (DDB) isolation structure. However, the use of such double diffusion break (DDB) isolation structures consumes more of the available plot space on a substrate than does the use of single diffusion break (SDB) isolation structures, thereby leading to reduced packing densities.”), FIGS. 1C-1H.)

D. Replacement Metal Gates

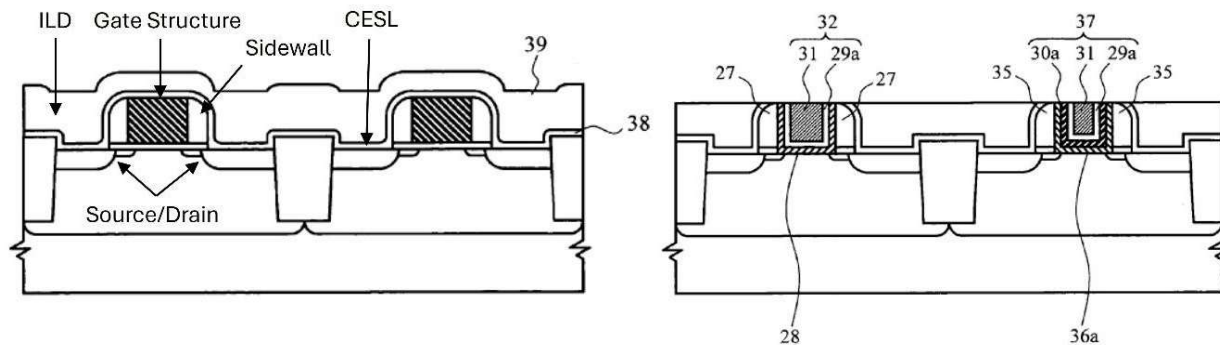
54. In early MISFETs, the gate electrode was typically composed of polysilicon. But a depletion region (effectively, an insulating barrier) forms at the polysilicon-gate dielectric interface, increasing resistance and reducing drive current. (Saito at 1:26-31; Hou at 1:25-35.) As gate dielectrics became thinner, the increased effect of depletion in polysilicon gate electrodes and reduced drive current became an intolerable problem requiring a solution. (Saito at 1:31-34 (“With progress in the miniaturization of the gate insulating film, the decrease of the drive current of transistor brings about a problem that cannot be neglected.”); Hou at 1:36-44 (“As a result, the carrier depletion effect in the gate electrodes limits device scalability by imposing a lower bound on how much the effective gate dielectric thickness can be reduced.”).) To address this issue, the industry added metals to gate

electrodes. (Saito at 1:35-37; Iriyama at 1:28-34, 1:41-42; Mistry_Paper at 247 (“Metal gate electrodes not only eliminate the poly depletion effect, but enable high-k dielectrics by screening the SO phonons that cause mobile degradation.”); Mistry_Presentation at 14-16, 35.)

55. Suitable metals for n-type devices were known, but options for p-type devices had less thermal stability. (Hou at 1:45-57 (“[T]hese materials have poor thermal stability.”); Iriyama at 1:41-48 (“When the gate electrodes are formed of a metal, the heat processing for activating the sources/drains often damages the gate electrodes”).) The solution was to use replacement metal gates, a “gate-last” approach. Because the metals are added near the end of the process, the more sensitive metal materials are not subjected to high temperatures. (Iriyama at 2:22-29 (“In the semiconductor device fabricated by the proposed fabrication method, after the high-temperature thermal processing for activating the sources/drains, the dummy gate electrodes and the dummy gate insulation film are etched, and then the gate insulation film and the gate electrodes are formed, whereby even in a case that the gate electrodes are formed of a metal, the gate electrode damage and gate leak current increase can be precluded.”).) This way, p-type and n-type devices can use individually tailored work functions. (Hou at 2:11-14 (“The dummy gates of PMOS and NMOS devices are then removed, and metals with different work functions are then filled into the openings for PMOS and NMOS devices.”); Iriyama at 13:10-28

(explaining that the gate electrodes of the p-channel and the n-channel may be formed of different materials so that they have different work functions); Mistry_Paper at 247 (“Metal gate materials are chosen with optimal workfunctions for NMOS and PMOS performance.”).)

56. Replacement metal gates first appeared in high-volume commercial devices in 2007 (in Intel’s first 45 nm devices). (Mistry_Paper at 247; Mistry_Presentation at 14-16, 35.) By 2017 (ten years later, when the application for the ’880 Patent was filed), this technology was standard in the industry.



Akasaka, FIG. 11C (annotated)

Akasaka, FIG. 12

57. The figures above show a typical replacement metal gate fabrication process. The figure on the left above shows the formation of polysilicon gate structures and insulating films (labeled “CESL” and “ILD”). (Akasaka ¶¶[0076]-[0078]; see also Aoyama ¶[0113], FIG. 6K; Mistry_Presentation at 15b.) After planarizing the CESL and ILD to expose the polysilicon gate structures, the polysilicon gate structures are removed and replaced with a high-k gate dielectric film 28/36a and metal layers 29a/30a/31. (Akasaka ¶¶[0078]-[0089], FIGS. 11D-12;

see also Aoyama ¶¶[0113]-[0119], FIGS. 6K-6Q; Mistry_Presentation at 15c-16.)

The figure on the right above illustrates the resulting structure.

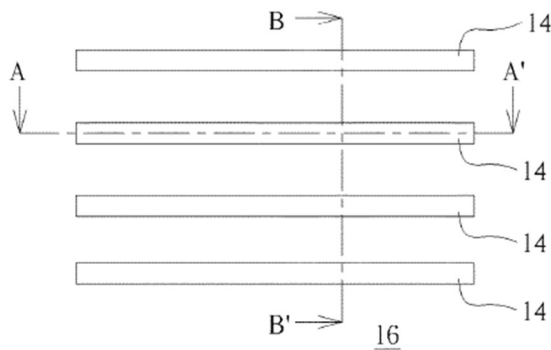
58. Although this metal gate process flow was originally developed for planar MOSFETs, it was also implemented in FinFETs from their inception. (See Xie616 at 3:6-10 (“In the case where a replacement gate process is used to manufacture the FinFET devices, the initial gate structures are sacrificial gate structures that will subsequently be removed and replaced with final gate structures for the devices.”); Intel_22nm_Details at 23 (describing Intel’s “22 nm Tri-Gate Circuits” as having “3rd generation high-k + metal gate transistors”).)

VII. The '880 Patent

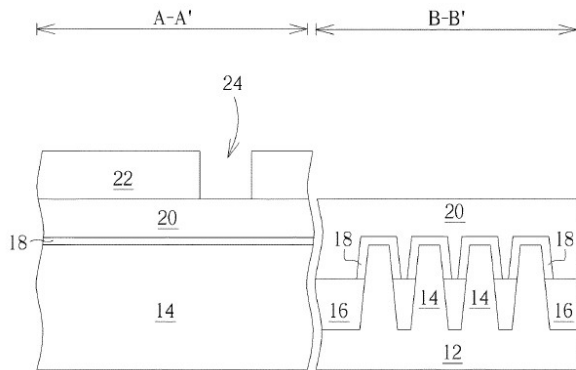
A. A Description of the Claimed Embodiments of the '880 Patent

59. The '880 Patent is titled “Semiconductor Device and Method for Fabricating the Same.” It describes a method for fabricating a FinFET semiconductor device and dividing the “fin-shaped structure to form [a] single diffusion break (SDB) structure.” ('880 Patent at 1:10-16.)

60. Figures 1 and 2 below show the formation of fin-shaped structures 14 on substrate 12. Cross-section A–A' shows a slice along the fin direction, and cross-section B–B' shows a slice perpendicular to that. ('880 Patent at 2:9-12.)



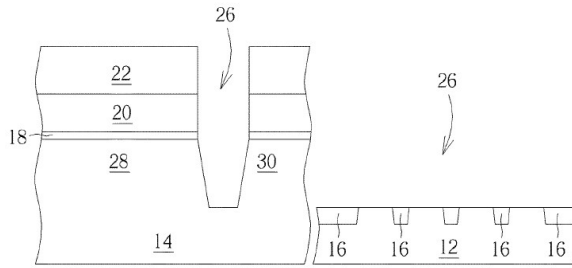
'880 Patent, FIG. 1



'880 Patent, FIG. 2

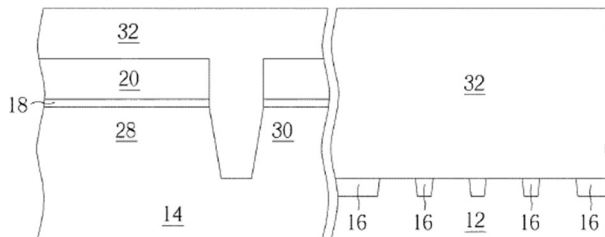
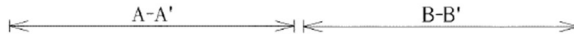
- 12:** substrate
- 14:** fin-shaped structures
- 16:** shallow trench isolation (“STI”)
- 18:** gate dielectric layer
- 20:** gate layer
- 22:** patterned mask
- 24:** opening

61. After the fin-shaped structures 14 have been formed, “a shallow trench isolation (STI) 16 is formed around the fin-shaped structures 14.” ('880 Patent at 2:59-60.) Then, a “gate dielectric layer 18 and a gate layer 20 are formed to cover the fin-shaped structures 14 and the STI 16 entirely, and a patterned mask 22 is formed on the gate layer 20.” ('880 Patent at 3:3-7.) Patterned mask 22 includes an opening 24 that exposes part of gate layer 20. ('880 Patent at 3:3-7.)



- 26:** trench
- 28:** first portion
- 30:** second portion
- 32:** dielectric layer

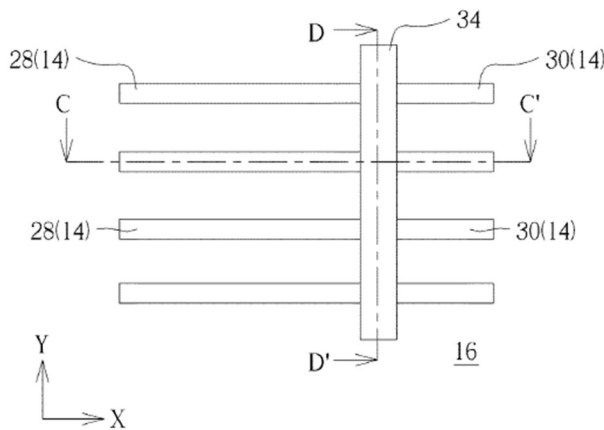
'880 Patent, FIG. 3



'880 Patent, FIG. 4

62. As FIG. 3 shows above, an etching process is performed through opening 24 to remove part of gate layer 20, part of gate dielectric 18, and part of fin-shaped structures 14, thus forming a trench 26. ('880 Patent at 3:17-20.) Trench 26 divides fin-shaped structures 14 into two portions: first portion 28 on the left and second portion 30 on the right. ('880 Patent at 3:20-24.) Dielectric layer 32 is then deposited, filling trench 26 as in FIG. 4 above and covering the remnants of gate layer 20. ('880 Patent at 3:25-38.) Planarizing dielectric layer 32 as FIGS. 5 and 6 show below,⁷ results in an insulating SDB structure 34. ('880 Patent at 3:39-59.)

⁷ Dielectric layer 32 on the right side of FIG. 6 is drawn too high. It should be coplanar with gate layer 20. (See '880 Patent at 3:44-48, FIG. 4.)



'880 Patent, FIG. 5

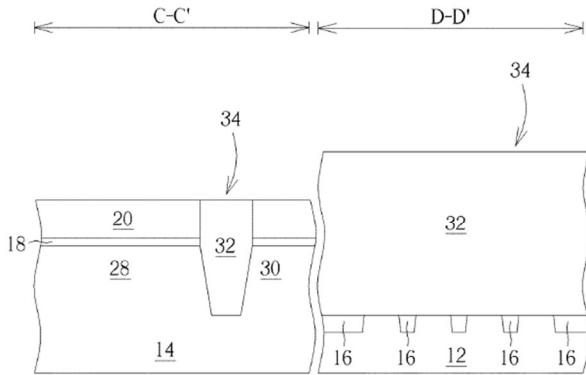
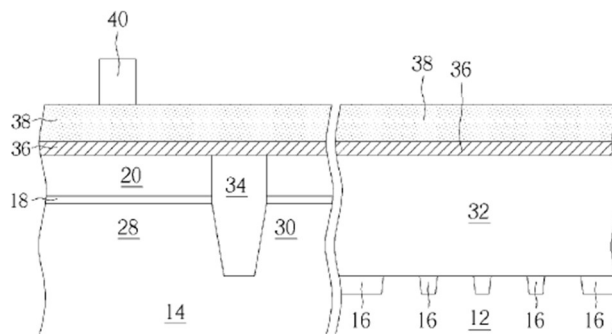


FIG. 6

'880 Patent, FIG. 6

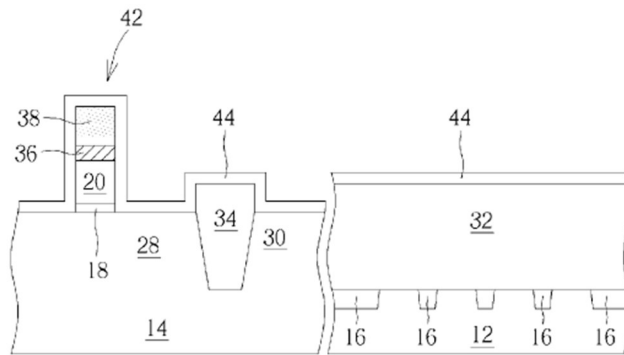
63. After the SDB is formed, the operative FinFETs components are made by patterning dummy gates and using a replacement metal gate process flow. As in FIG. 7, first and second hard masks 36 and 38 are formed, topped by a patterned mask 40 to define the dummy gate structures. ('880 Patent at 3:60-4:7.)



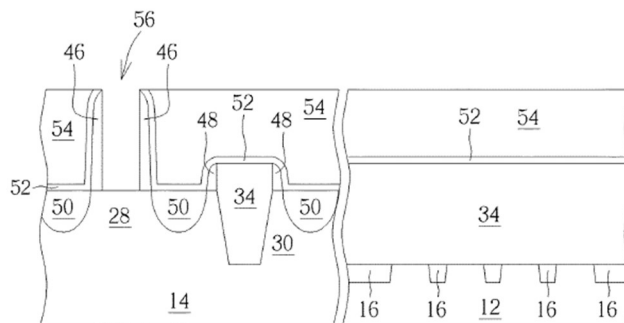
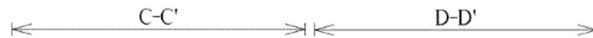
'880 Patent, FIG. 7

- 34:** single diffusion break (SDB)
- 36:** first hard mask
- 38:** second hard mask
- 40:** patterned mask

64. Next, as FIG. 8 shows below, an etching process transfers the shape of patterned mask 40 into the hard mask layers. ('880 Patent at 4:8-29.) Then, an insulating cap layer 44 “is formed on the fin-shaped structures 14 to cover the gate structure 42 and the SDB structure 34 at the same time.” ('880 Patent at 4:29-34.)



'880 Patent, FIG. 8

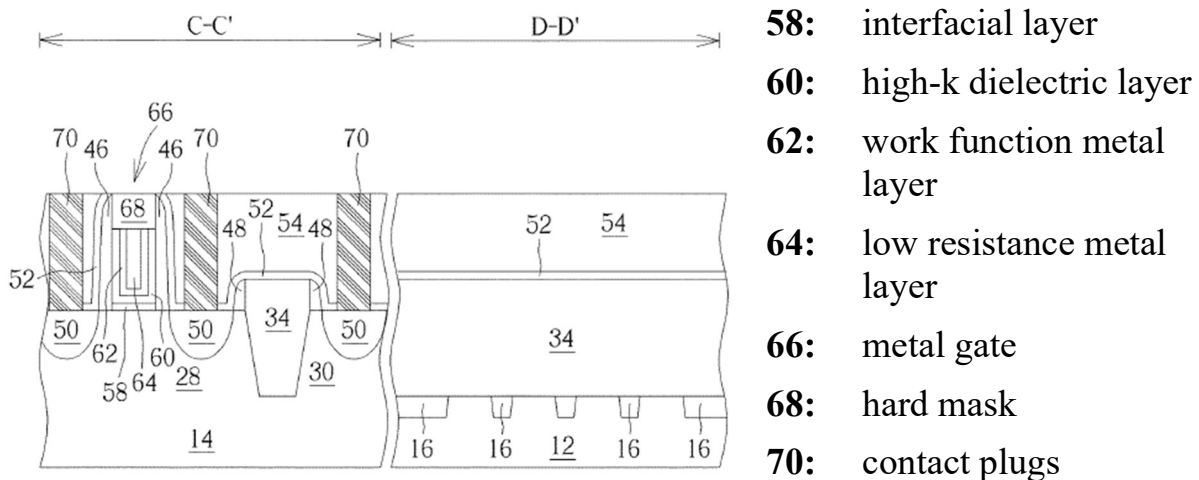


'880 Patent, FIG. 9

- 42:** gate structure
- 44:** cap layer
- 46:** first spacers
- 48:** second spacers
- 50:** source/drain regions
- 52:** contact etch stop layer (CESL)
- 54:** interlayer dielectric (ILD)
- 56:** recess

65. As illustrated in FIG. 9 above, an anisotropic etch is performed to remove cap layer 44 except where it overlays the sidewalls of gate structure 42 and SDB 34, leaving behind first spacers 46 on gate structure 42 and second spacers 48 on SDB 34. ('880 Patent at 4:35-39.) These sidewalls define where source/drain regions 50 are formed. ('880 Patent at 4:39-58.) Then, contact etch stop layer ("CESL") 52 and interlayer dielectric ("ILD") 54 are formed covering the wafer and then planarized to the top of gate layer 20, thereby exposing gate layer 20. ('880 Patent at 4:59-67.) Gate layer 20 is removed, leaving a recess 56. ('880 Patent at 5:1-10.)

66. As FIG. 10 below shows, replacement metal gate 66 is completed by filling recess 56 with an interfacial layer 58, high-k dielectric layer 60, work function metal layer 62, low-resistance metal layer 64, and hard mask 68. ('880 Patent at 5:11-63.) Finally, contact plugs 70 for the source/drain regions are added by etching ILD 54 and filling the contact openings with metal. ('880 Patent at 5:64-6:11.)



'880 Patent, FIG. 10

B. Prosecution History

67. Based on my review of the prosecution file history for the '880 Patent, I understand that the Patent Examiner rejected the original claims based on the Xie790 reference (U.S. Patent Application Pub. No. 2017/0243790). (File History, Office Action dated Nov. 13, 2017.)

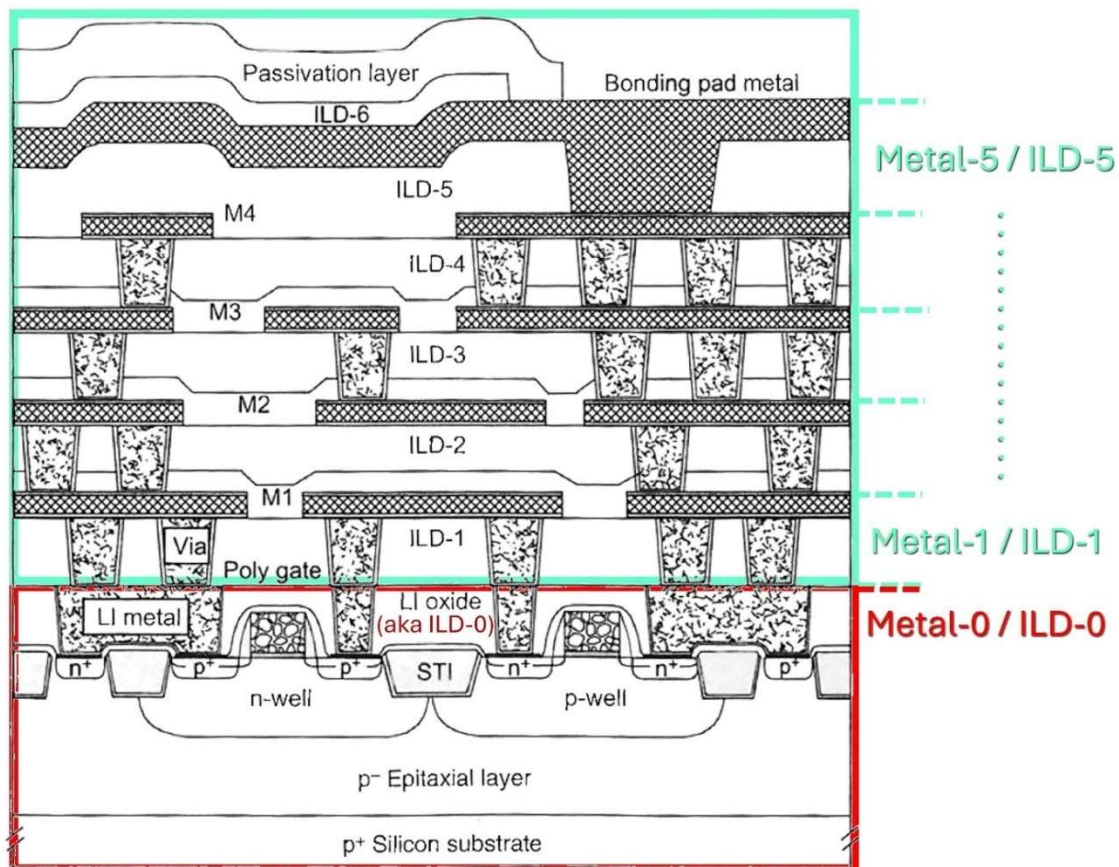
68. In response, I understand that the Applicant did not challenge the Examiner's rejections based on the Xie790 reference. (File History, Amendment

dated Dec. 5, 2017.) Instead, my understanding is that the Patent Applicant limited the independent claim 1 by adding the following language: “after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure.” The Patent Applicant then argued that the Xie790 reference does not satisfy that language because it disclosed forming the ILD layer *before* the SDB structure, not *after* the SDB structure. The Patent Applicant did not offer any other arguments.

69. The Examiner then allowed the claims and stated the following: “[T]he substance of applicants’ remarks, filed 12/05/2017 with the amended claims, are persuasive, as such the reasons for allowance are in all probability evident from the record and no statement is deemed necessary.” (File History, Notice of Allowability dated Feb. 2, 2018.)

70. I have been told that I should consider the File History from the perspective of a person of ordinary skill in the art at the time, so I would like to offer some context in that regard. A person of ordinary skill in the art would have understood, as a matter of introductory semiconductor manufacturing principles taught to undergraduates, that multiple ILD layers are used in any FET integrated circuit. As shown below in a 2001 textbook on semiconductor manufacturing, the ILD layers (labeled “LI oxide” and “ILD-1” through “ILD-6”) “serve[] as an insulator material between each metal layer or between the first metal layer and silicon [i.e., transistor layer].” (Quirk at 216.) Each “ILD will have many small vias,

which are small openings in the ILD that provide an electrical pathway from one metal layer to adjacent metal layers.” (Quirk at 216; *see also* Quirk at 214-21, Figs. 9.21-9.29; Ha ¶¶[0077]-[0080], ¶¶[0122]-[0125], FIGS. 2A-2C.) Thus, in addition to the ILD layer at the transistor level (like “ILD-0” below and the ILD layer at issue in prosecution), integrated circuits have additional ILD layers (analogous to “ILD-1” through “ILD-6” below) formed above the transistor level, between each metal layer. (Quirk at 216; *see also* Quirk at 214-21, Figs. 9.21-9.29.)



Quirk, Fig. 9.29 (annotated)

71. In the Xie790 reference, the *lowest* ILD layer (analogous to “ILD-0” above, at the transistor level) is formed *before* forming the SDB structure. (Xie790

¶[0023], ¶[0029], FIGS. 2A, FIG. 2G; *see also* Xie616 at 8:49-53, 11:1-13, FIGS. 2B, 2N (same); Shieh ¶[0022], ¶¶[0034]-[0035], FIGS. 3-6 (same); Ha ¶[0098], ¶¶[0110]-[0111], FIGS. 4A-4B, 9A-9C (same).) But the Xie790 reference “relates to the fabrication of integrated circuits” (Xie790 ¶[0002]), which means that **additional** ILD layers—like the additional ILD layers ILD-1 through ILD-6 depicted above—would be formed **after** (and on) the SDB structure. (See Quirk at 214-21 (“The interlayer dielectric (ILD) serves as an insulator material between each metal layer or between the first metal layer and silicon.”), Figs. 9.21-9.29; Ha ¶¶[0077]-[0080], ¶¶[0122]-[0125], FIGS. 2A-2C.)

72. The layer labeled “LI oxide” in Quirk’s Fig. 9.29 above is also commonly referred to as “ILD-0.” Paio, which was contemporaneous with Quirk’s textbook, explains:

Multilayer integrated circuit devices generally include several interconnect layers (metal layer 1, metal layer 2, metal layer 3, etc.) stacked upon each other. The interconnect layers are separated from each other by interlevel dielectric layers (ILD 1, ILD2, ILD3, etc.) . . .

According to conventional integrated circuit process flow, **transistors are** manufactured on or within a semiconductor substrate and **covered with an interlevel dielectric layer (ILD 0).**

(Paio at 1:25-43 (emphases added).) That terminology has been and remains common in the industry.

73. As another example (in the FinFET context and contemporaneous with the '880 Patent), Tsai similarly explains that the term ILD-0 identifies the insulating layer between neighboring transistors:

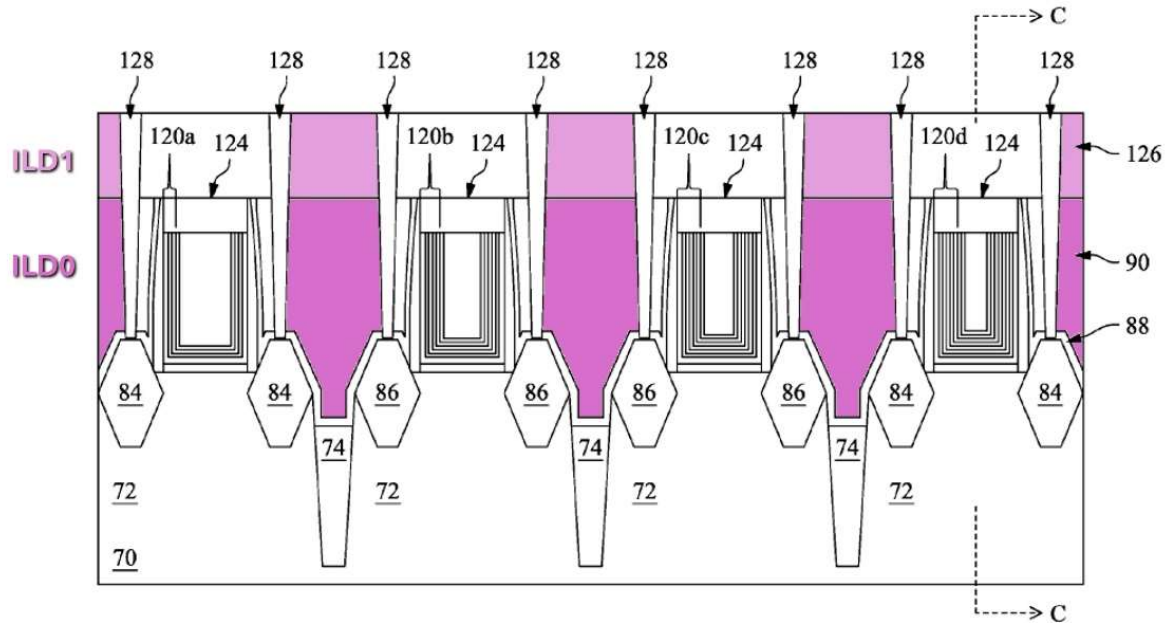
A bottom inter-layer dielectric (ILD0) 90 is deposited
[A] planarization process, such as a CMP, is performed to level the top surface of ILD0 90 with the top surfaces of the dummy gates 78. . . . Accordingly, top surfaces of the dummy gates 78 are exposed through the ILD0 90. The dummy gates 78 and the dummy gate dielectrics 76 are removed in an etching step(s), so that openings through the ILD0 90 and defined by the gate spacers 82 are formed to the fins 72.

(Tsai at 8:23-39.) Tsai goes on to describe ILD-1:

An upper ILD (ILD1) 126 is deposited over the ILD0 90 and the dielectric caps 124, and contacts 128 are formed through the ILD1 126, ILD0 90, and ESL 88 to the epitaxial source/drain regions 84 and 86. . . . A planarization process, such as a CMP, may be performed to remove excess material from a surface of the ILD1 126. The remaining liner and conductive material form contacts 128 in the openings.

(Tsai at 13:13-32.) Tsai's FIG. 17 below shows ILD0 layer 90 and ILD1 layer 126.

As FIG. 17 shows, ILD0 is the transistor-level ILD, and ILD1 is at a higher level.



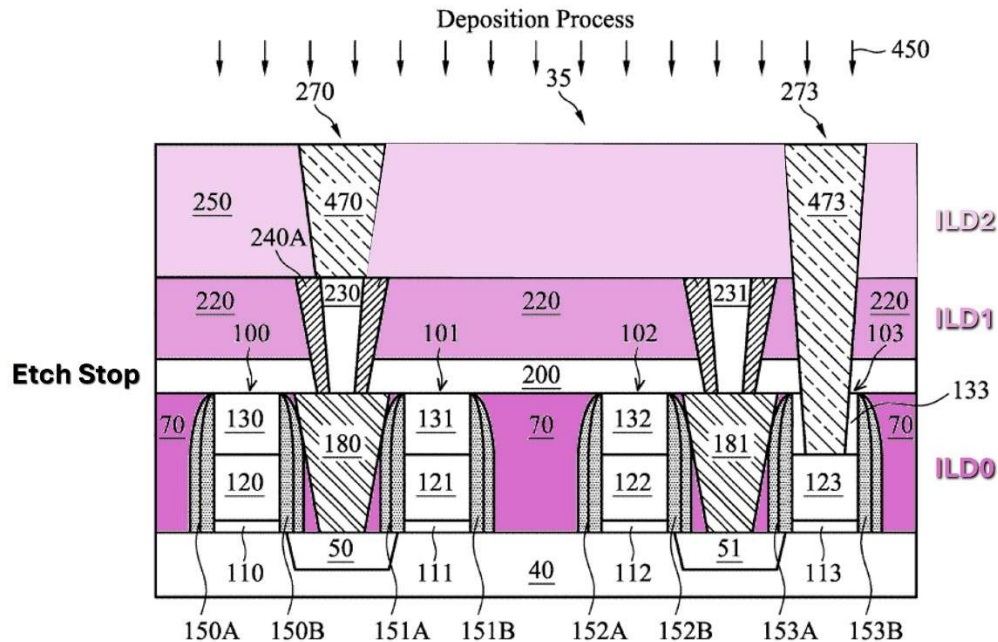
Tsai, FIG. 17 (annotated)

Tsai also explains that this process continues, as Quirk illustrates in Fig. 9.29, to form additional layers of metal interconnections above ILD1:

Although not explicitly shown, a person having ordinary skill in the art will readily understand that further processing steps may be performed on the structure in FIG. 17. For example, various Inter-Metal Dielectrics (IMD) and their corresponding metallizations may be formed over ILD1 126.

(Tsai at 13:51-55.) Hsu's FIG. 6 below shows a similar example, including "interlayer dielectric (ILD) 70 ... referred to as an **ILD0** layer," "interlayer dielectric (ILD) 220 ... referred to as an **ILD1** layer," and "interlayer dielectric

(ILD) 250 ... referred to as an *ILD2* layer.” (Hsu ¶[0015], ¶[0023], ¶[0025] (emphases added).)



Hsu, FIG. 6 (annotated)

74. As these materials demonstrate, a person of ordinary skill in the art would have understood it is common to describe only transistor-level fabrication (the so-called “front-end of line” (“FEOL”) fabrication steps), because it was understood that an entire set of “back-end of line” (“BEOL”) fabrication steps—which do not generally depend on the transistor structure itself—will take place to complete the integrated circuit. This is a fundamental concept in the art of semiconductor integrated circuit manufacturing.

75. In view of this basic understanding, if forming the claimed “interlayer dielectric (ILD) layer” in claim 1 of the ’880 Patent referred to anything other than

forming the lowest ILD layer (labeled “LI oxide” in Quirk’s image above, and commonly referred to as “ILD0”), then the alleged distinction between the ’880 Patent and the Xie790 reference would not have been a distinction at all. In fact, this lowest ILD layer is the *only* ILD layer discussed in the ’880 Patent and Xie790 reference.

76. It is therefore my opinion that a person of ordinary skill in the art would have understood the claimed step of “forming an interlayer dielectric (ILD) layer on the SDB structure” (which the claim says must be performed “after forming the SDB structure”) does not encompass forming *any* ILD layer after and on the SDB structure—only the *lowest* ILD layer (analogous to the “LI oxide above,” commonly referred to as “ILD0”).

C. Claim Construction

77. I have been told that claim terms are construed with the meanings they would have to a person of ordinary skill in the art in the context of the patent’s written description and its prosecution history. In my analysis of the Challenged Claims, I have therefore applied the meanings of the claim terms as understood by a person of ordinary skill in the art in the context of the ’880 Patent and its prosecution history, which I discuss in the preceding subsection.

78. The Patent Owner stated in its complaint filed in the ITC that “the inventors of the ’880 Patent recognized that the method of forming SDB structures

could be improved by performing the SDB trench etching step after the formation of the polysilicon gate layer and before the final metal gate formation.” (ITC Complaint ¶89 (citing ’880 Patent at 3:3-5:10).) Under this view, which I disagree with, “forming an interlayer dielectric (ILD) layer on the SDB structure” after the SDB structure is formed, as recited in claim 1, could be regarded as encompassing the formation of *any* ILD layer after and on the SDB structure. (See Section VII.B above.) Or it is possible the Patent Owner could argue the claims should be applied in other ways that seem to differ from the ’880 Patent, so long as the process is generally consistent with the Patent Owner’s characterization.

79. I have been asked to apply the ILD formation step of claim 1 under two constructions: (1) it refers to forming the *lowest* ILD layer (which is consistent with the prosecution history and embodiments described in the ’880 Patent) and (2) it includes forming *any* ILD layer (which matches the Patent Owner’s broader view of the claims but is inconsistent with my understanding of the prosecution history and the descriptions of the ’880 Patent). My analysis of the Ha reference (Grounds 2A through 2D) proceeds according to the latter construction. My analysis of the Doris reference (Grounds 1A and 1B) proceeds according to the former construction, but the Doris grounds also satisfy the claims under the latter construction as well. Either way, my conclusion is the same: all Challenged Claims are unpatentable.

80. If the Patent Owner offers constructions of any other terms, I intend to address those constructions and related arguments at the appropriate time.

VIII. Descriptions of Asserted Prior Art References

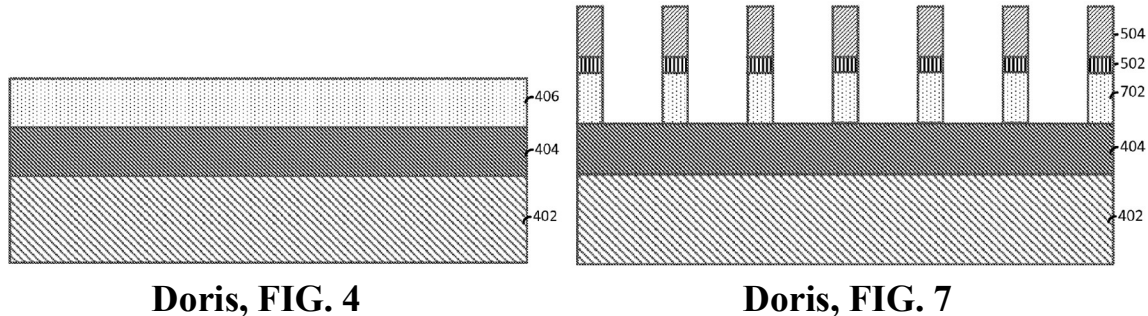
A. U.S. Patent Application Pub. No. 2017/0054002 A1 (“Doris”)

81. Doris was filed on August 20, 2015, and published on February 23, 2017. I have been told this qualifies Doris as prior art.

82. In my opinion, applying the standard as stated in Section IV.B above, Doris is analogous art to the ’880 Patent because Doris is in the same field of endeavor as the ’880 Patent (semiconductor FinFET devices and methods for fabricating them). (*See* ’880 Patent at 1:9-67; Doris ¶¶[0001]-[0003].) In my opinion, Doris is also analogous art to the ’880 Patent because a POSITA would have found it reasonably pertinent to at least one problem the ’880 Patent purports to address, for example, fabricating FinFET semiconductor devices. (*See* ’880 Patent at 1:9-67; Doris ¶¶[0001]-[0003].)

83. Doris discloses methods for making FinFETs. (Doris at Abstract (“A method for forming a fin on a substrate comprises patterning and etching a layer of a first semiconductor material to define a strained fin . . .”), ¶[0001] (“The present invention relates to field effect transistor (FET) devices, and more specifically, to finFET devices.”).) Doris starts with a substrate like the one in FIG. 4. (Doris ¶[0043] (“FIG. 4 illustrates a side cut-away view of a substrate 402 that may

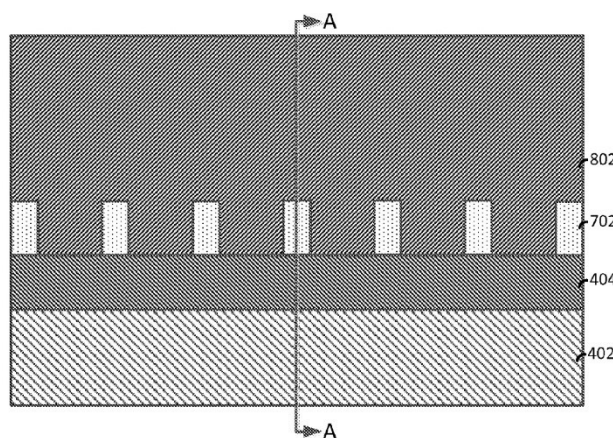
be formed from, for example, a silicon material.”), FIG. 4.) Although substrate depicted in FIG. 4 is a silicon-on-insulator (“SOI”) substrate comprising a silicon layer 402, insulator layer 404, and semiconductor layer 406 (e.g., silicon), Doris states that “alternate exemplary embodiments may include a *bulk silicon* . . . arrangement.” (Doris ¶[0043] (emphasis added); *see also* Doris ¶[0040] (“The substrate 101 may include, a *bulk silicon substrate*, [or] a silicon on insulator substrate, ...” (emphasis added)).)



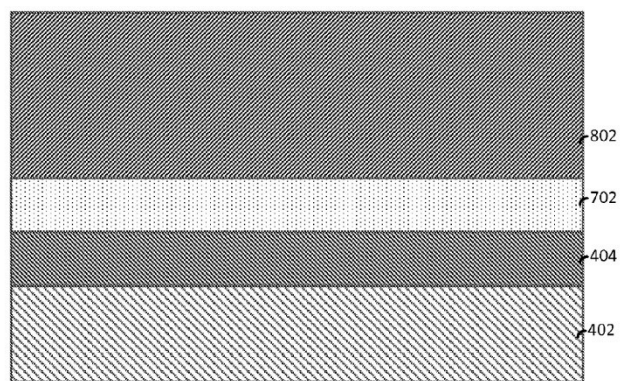
84. Doris’s process begins by depositing an oxide layer 502 and a nitride hardmask layer 504 over the substrate. Those layers are then patterned into fin shapes. (Doris ¶¶[0044]-[0045] (“A hardmask layer 504 is deposited over the oxide layer 502, where the hardmask layer 504 may include, for example a nitride material. FIG. 6 illustrates the patterning of the hardmask layer 504 and oxide layer 502 to expose portions of the semiconductor material 406.”), FIGS. 5-6.) As FIG. 7 above shows, the fin pattern is then transferred into semiconductor layer 406 by etching to form fins 702 and expose insulator layer 404. (Doris ¶[0046] (“FIG. 7 illustrates the fabrication of fins 702 with the patterned hardmask layer 504 and oxide layer 502

using an etching process such as, for example, a reactive ion etch (RIE) process. The etching process defines the fins 702 by removing exposed semiconductor material 406 (of FIG. 6) and exposing portions of the insulator layer 404.”.) Next, the remnants of oxide layer 502 and hardmask layer 504 are removed. (Doris ¶[0047] (“In the illustrated embodiment, the hardmask layer 504 and the oxide layer 502 have been removed prior to depositing the α -Si layer 802.”).)

85. Next, an amorphous silicon (α -Si) or polysilicon layer 802 is deposited over fins 702 and exposed portions of insulator layer 404. (Doris ¶[0047], FIGS. 8-9.) Additionally, “a layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802.” (Doris ¶[0047].) Doris’s FIG. 8 below illustrates how this might appear when looking down fins 702, whereas Doris’s FIG. 9 depicts the cross-section A–A from FIG. 8. (Doris ¶[0047].)

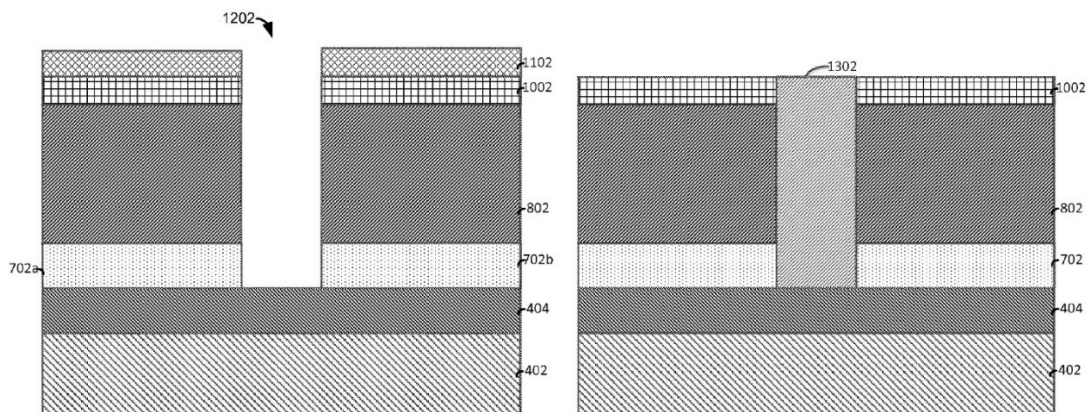


Doris, FIG. 8



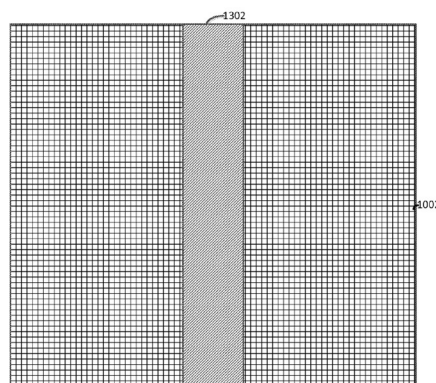
Doris, FIG. 9

86. A hardmask layer 1002 is then formed. (Doris ¶[0048], FIG. 10.) Using a photolithography mask 1102, hardmask layer 1002 is patterned to include an opening perpendicular to the fins. (Doris ¶[0049], FIGS. 11, 14.) An anisotropic etch is then performed through the opening to create a cavity 1202, as Doris's FIG. 12 shows in cross-section below. (Doris ¶[0050], FIG. 12.) This etch cuts the fins. (Doris ¶[0050] (“As discussed above with FIG. 2, when the fins 102 are etched or cut into segments 702a and 702b”)) The cavity 1202 is then filled with an insulator material 1302 comprising “an oxide or a nitride material” that, as FIGS. 13 and 14 show below, is planarized. (Doris ¶[0051], FIGS. 13-14.)



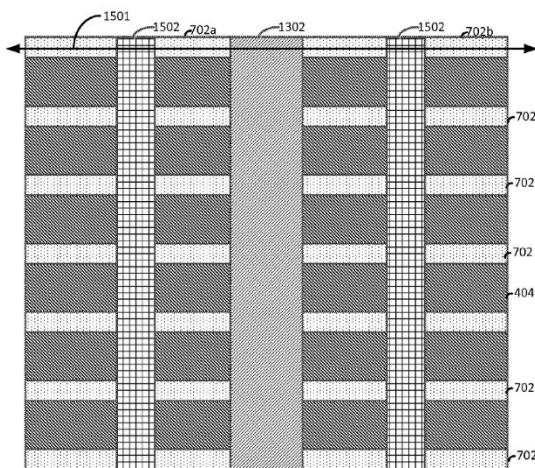
Doris, FIG. 12

Doris, FIG. 13

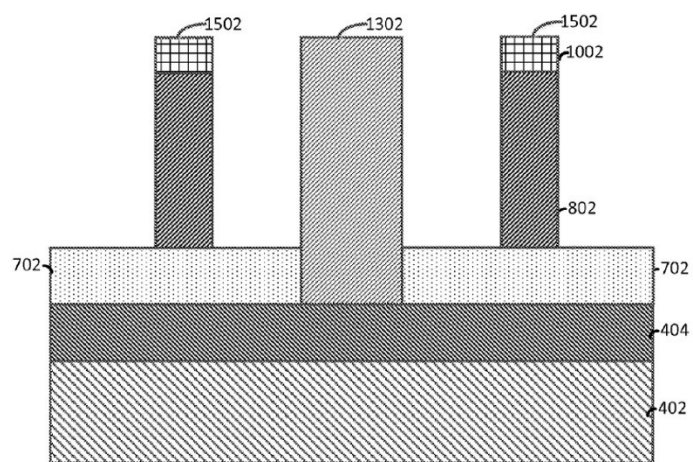


Doris, FIG. 14

87. Next, the structure is patterned to define dummy gate stacks 1502, as FIGS. 15 and 16 show below. “The dummy gate stacks 1502 define channel regions of the fins 702” and “may be formed using a suitable lithographic patterning and etching process.” (Doris ¶[0052].) As FIG. 15 shows in plan view, the fins run horizontally, and dummy gate patterns 1502 run vertically, parallel to insulator material 1302. (Doris ¶[0052] (“The fins 702a and 702b are arranged along a common longitudinal axis shown by the arrow 1501.”), FIG. 15.) Doris’s FIG. 16 shows the structure in a cross-section along a fin 702, such as along arrow 1501 in FIG. 15. (Doris ¶¶[0052]-[0053] (“FIG. 16 illustrates a side cut-away view of the dummy gate stacks 1502 on the fins 702 and the insulator material 1302 arranged between the fins 702.”), FIG. 16.)



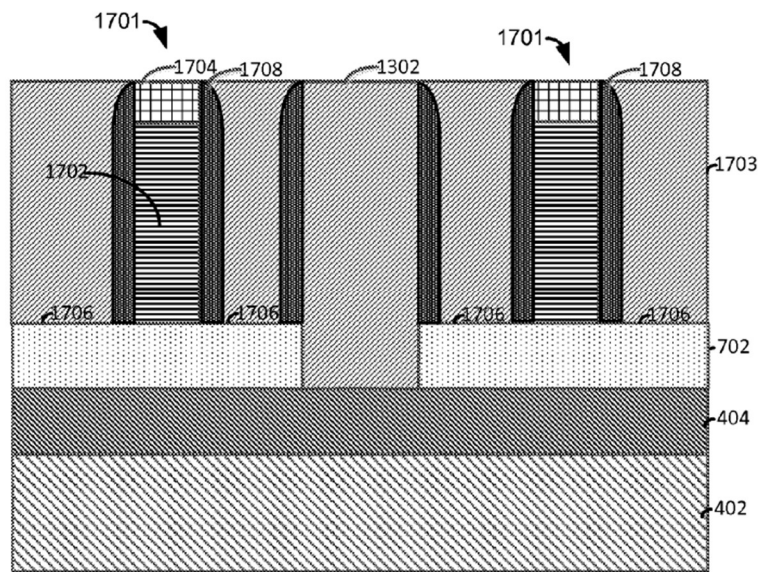
Doris, FIG. 15



Doris, FIG. 16

88. After the dummy gate patterning, spacers 1708 are formed on dummy gate stacks 1502 and insulator material 1302. (Doris ¶[0054] (“The gates 1701 of the FET devices may be formed following the formation of spacers 1708 that formed

adjacent to the dummy gate stacks 1502 (of FIG. 16).”), FIG. 17.) Then, active regions 1706 (e.g., source/drain regions) are formed by ion implantation and/or epitaxial growth in fins 702. (Doris ¶[0054].) An insulator 1703 (e.g., an oxide) is then formed to fill the spaces, then planarized, and a replacement gate process replaces dummy gate structures 1502 with metal gate structures 1701 comprising a gate dielectric layer, metal gate layer 1702, and cap layer 1704 (see FIG. 17 below). (Doris ¶[0054] (“In the illustrated embodiment, the gate stacks 1702 include a dielectric layer and a gate metal layer 1702 and a cap layer 1704.”), FIG. 17.)



Doris, FIG. 17

B. J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors* (2008) (“Colinge”)

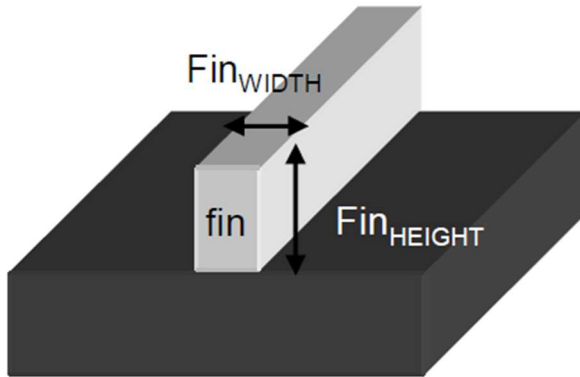
89. Colinge was published and publicly available by 2008. I have been told this qualifies Colinge as prior art.

90. In my opinion, applying the standard as stated in Section IV.B above, Colinge is analogous art to the '880 Patent because Doris is in the same field of endeavor as the '880 Patent (semiconductor FinFET devices and methods for fabricating them). (See '880 Patent at 1:9-67; Colinge at 50-51, 65-66, Figs. 2.2, 2.14.) In my opinion, Colinge is also analogous art to the '880 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '880 Patent purports to address, for example, fabricating FinFET semiconductor devices. (See '880 Patent at 1:9-67; Colinge at 50-51, 65-66, Figs. 2.2, 2.14.)

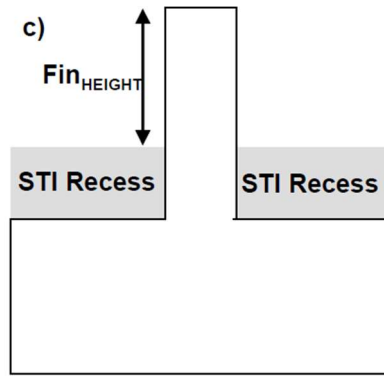
91. Colinge is a textbook from 2008 that describes many aspects of FinFETs. In relevant part, Colinge explains the difference between FinFETs made using an SOI substrate and FinFETs made using a bulk silicon substrate. (Colinge at 50-51 (“The fabrication flow of a Tri-gate MOSFET on an SOI substrate is shown in Figure 2.2.”), 65-66 (“The main advantages of using bulk silicon over SOI substrates are 1) lower wafer cost and 2) better substrate heat transfer rate.”), Figs. 2.2, 2.14.)

92. FinFETs formed using an SOI substrate are electrically isolated from one another using a buried oxide (sometimes called “BOX”) layer, shown below on the left in dark gray, that underlies the fins. (Colinge at 50-51, Fig. 2.2.) FinFETs formed using a bulk silicon substrate are electrically isolated from one another using

a recessed shallow trench isolation (“STI”) that surrounds the fins, as shown on the right below in light gray. (Colinge at 65-66, Fig. 2.14.)



Colinge, Fig. 2.2(b) (SOI)



Colinge, Fig. 2.14(c) (Bulk Si)

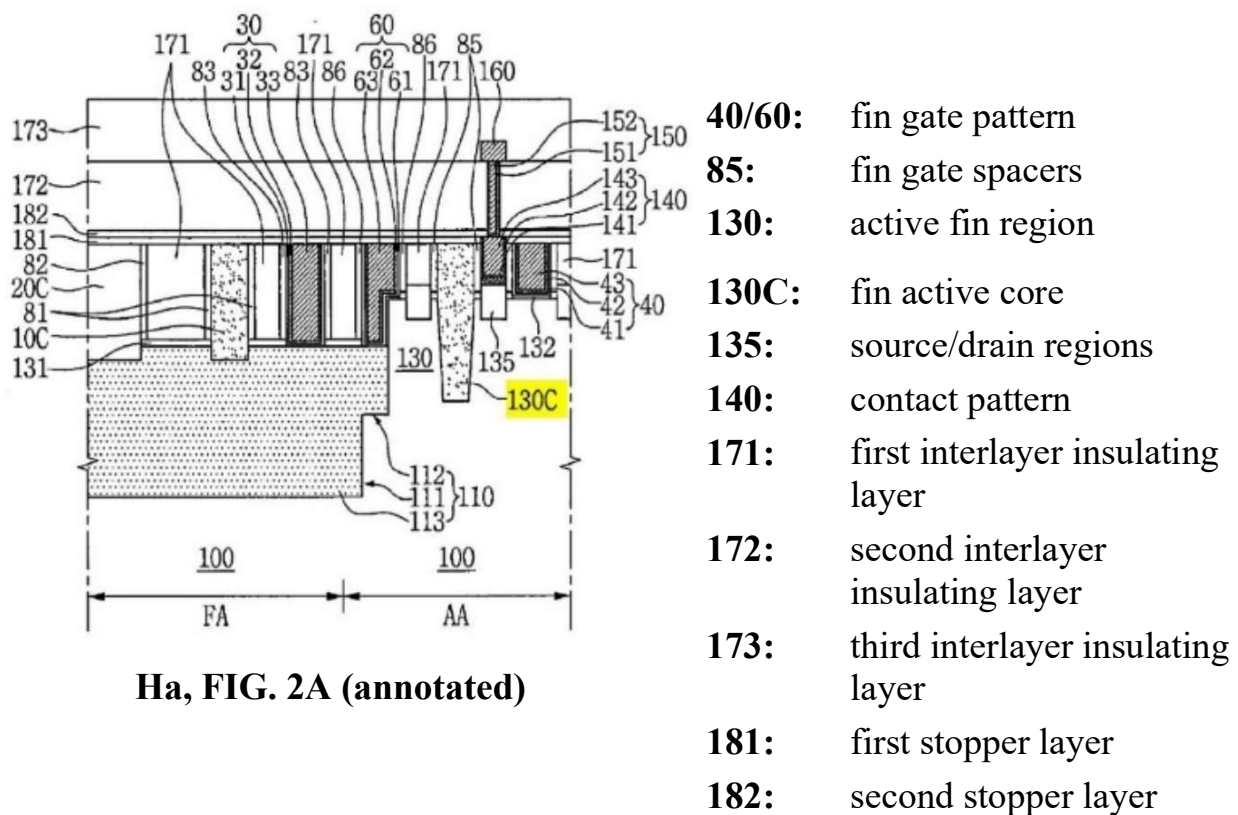
C. U.S. Patent Application Pub. No. 2016/0111524 A1 (“Ha”)

93. Ha was filed on August 7, 2015, and published on April 21, 2016. I have been told this qualifies Ha as prior art.

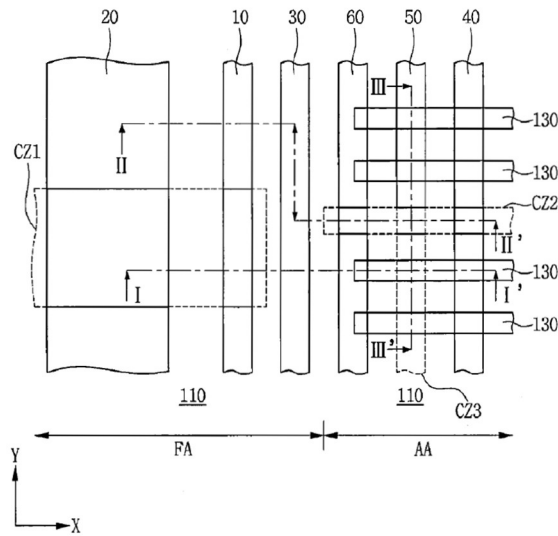
94. In my opinion, applying the standard as stated in Section IV.B above, Ha is analogous art to the ’880 Patent because Ha is in the same field of endeavor as the ’880 Patent (semiconductor FinFET devices and methods for fabricating them). (See ’880 Patent at 1:9-67; Ha ¶¶[0002]-[0003], ¶¶[0129]-[0131].) In my opinion, Ha is also analogous art to the ’880 Patent because a POSITA would have found it reasonably pertinent to at least one problem the ’880 Patent purports to address, for example, fabricating FinFET semiconductor devices. (See ’880 Patent at 1:9-67; Ha ¶¶[0002]-[0003], ¶¶[0129]-[0131].)

95. As shown in Figure 2A below, Ha describes FinFETs with “a fin active core and methods of fabricating the same.” (Ha ¶[0002].) Ha explains that “a single

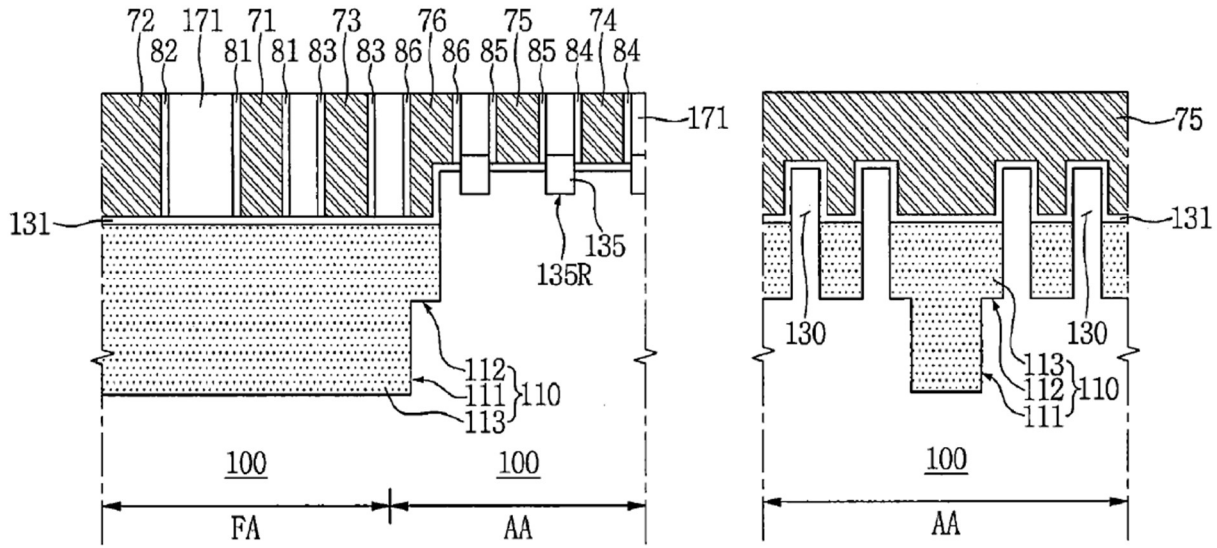
diffusion break (SDB) structure can be implemented using [its] fin active cutting method.” (*Id.* ¶[0129].) For example, Ha’s insulating “fin active core” (130C), which breaks up adjacent to source/drain regions 135, “fill[s] . . . [a] fin active cut space” to serve form an SDB structure. (*Id.* ¶[0109]; *see id.* ¶[0099], ¶[0129].)



96. Each of Ha’s figures shows a cross-section through a particular region of FIG. 1 (below). Specifically, figure numbers ending in “A” lie along cross-section I–I’; figure numbers ending in “B” lie along cross-section II–II’; and figure numbers ending in “C” lie along cross-section III–III’. (Ha ¶¶[0043]–[0044], ¶[0090].)

**Ha, FIG. 1**

97. As Figures 4A and 4C below demonstrate, Ha's process begins by forming an isolation region 110 around the active fins 130. (Ha ¶[0091], ¶[0093]-[0094] ("The isolation region 110 may include a trench insulation material 113 which fills a deep trench 111 and a shallow trench 112.")) In the regions corresponding to features 10-60 of FIG. 1, sacrificial gate structures 71-76 and gate spacers 81-86 are then formed on a base insulating layer 131. (Ha ¶[0091], ¶[0095].) Then, source/drain regions 135 are formed between the gate spacers in the fin active area (AA), and a first interlayer insulating layer 171 is formed covering the entire substrate and then planarized to the tops of sacrificial gate structures 71-76. (Ha ¶[0096]-[0098].)

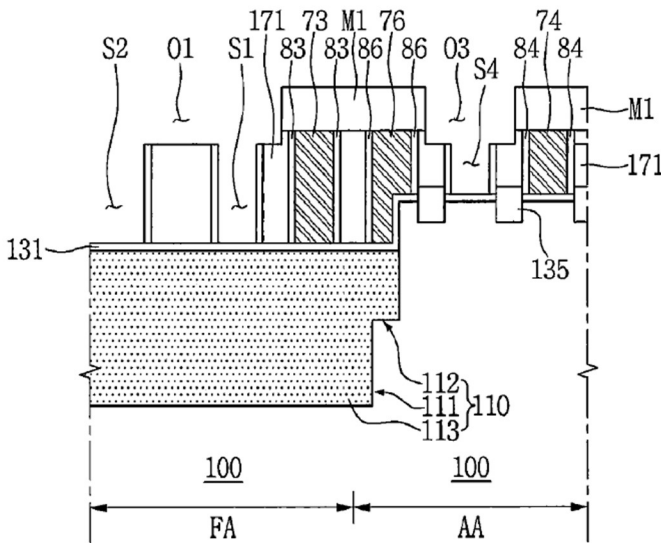


Ha, FIG. 4A

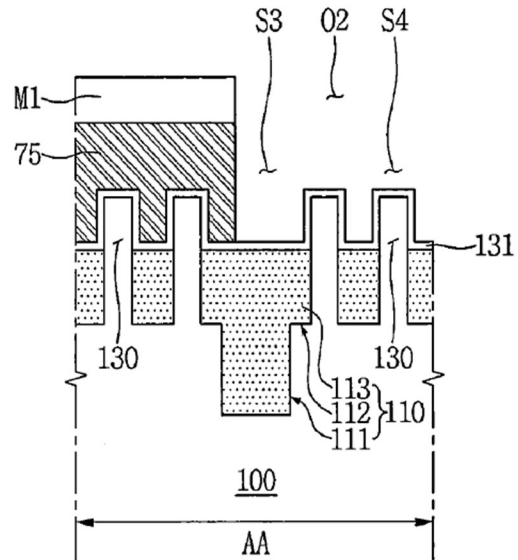
Ha, FIG. 4C

98. Next, as FIGS. 5A and 5C show, a mask pattern M1 is formed over the substrate. (Ha ¶[0099].) Mask M1 includes several openings, including “a fin active cut space opening O3” that corresponds to “the fin active cut-zone CZ3 of FIG. 1.”⁸ (Ha ¶[0100]). Sacrificial gate structure 75 is etched away through mask M1, leaving behind several spaces, including “fin active cut space S4.” (Ha ¶[0099]-[0102].) This etching process also removes parts of first interlayer insulating layer 171 and fin gate spacers 85. (Ha ¶[0103] (“Upper portions of the first interlayer insulating layer 171 and the gate spacers 81, 82, 84, 85, and 86, which are exposed in the field gate cut opening O1, the fin gate cut opening O2, and the fin active cut opening O3 may be recessed.”), FIGS. 5A-5C.)

⁸ Fin active cut space opening O3 overlaps with a fin gate cut opening O2 where fin active cut-zone CZ3 and fin gate cut-zone CZ2 intersect. (See Ha ¶[0063], FIG. 1.)

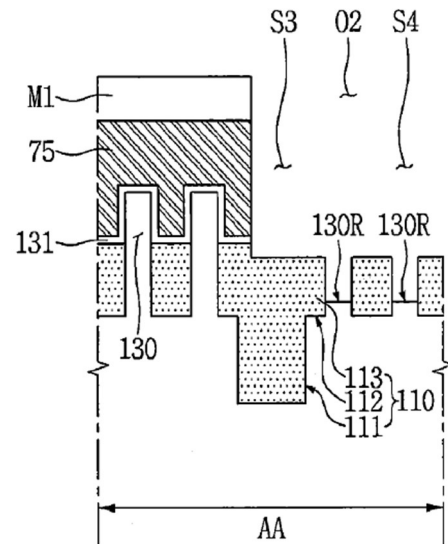
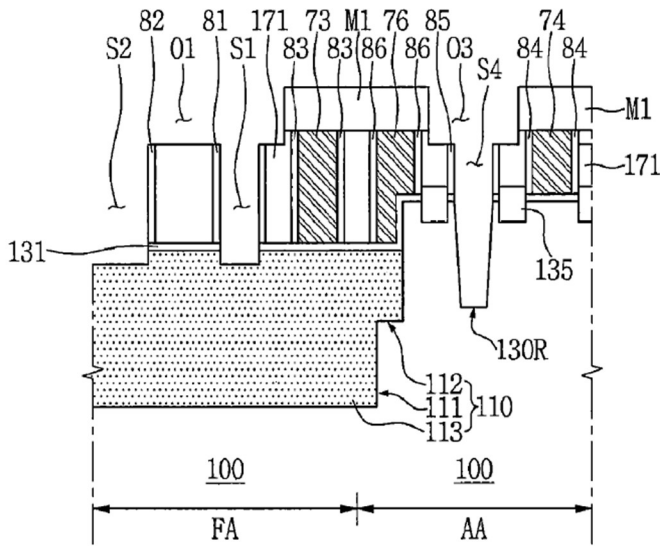


Ha, FIG. 5A

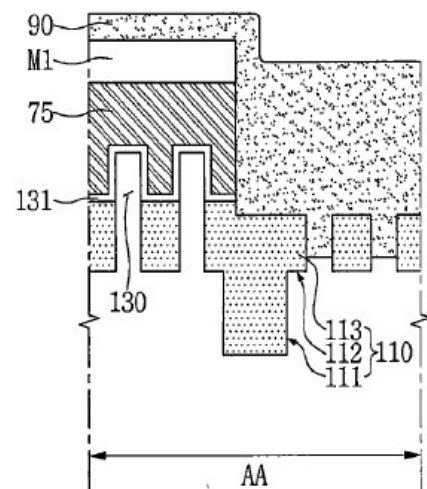
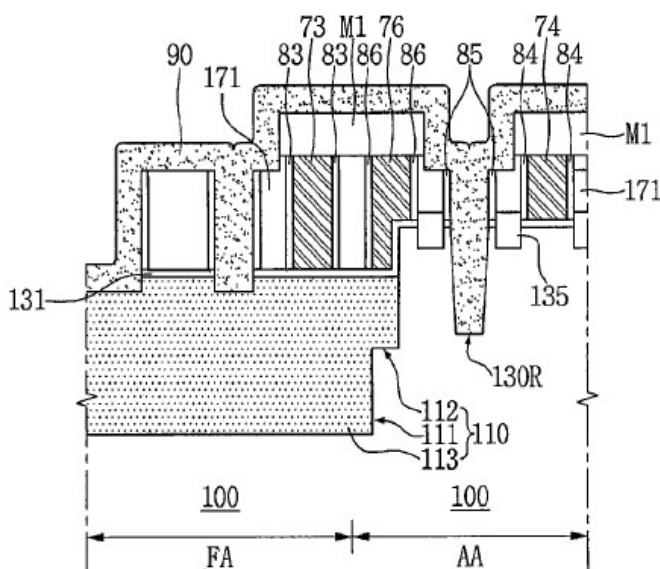


Ha, FIG. 5C

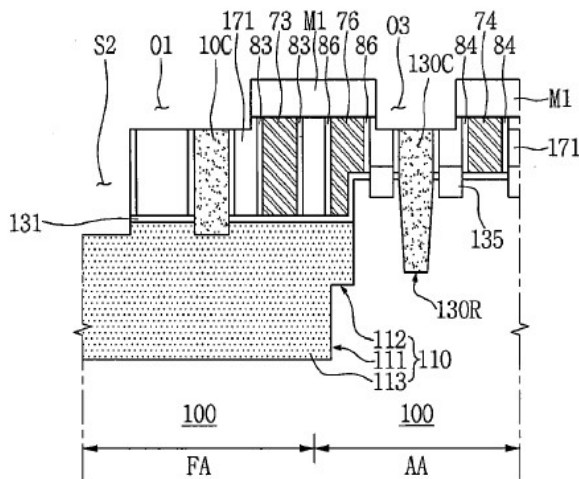
99. Next, a fin active recess 130R is formed in space S4 by etching away the exposed portions of base insulating layer 131 and recessing fin active region 130. (Ha ¶[0104].) As illustrated below, because base insulating layer 131 and isolation region 110 are made of similar materials (e.g., silicon oxide), this process also recesses isolation region 110, which ensures that the exposed base insulating layer 131 is adequately removed. (Ha ¶[0089] (“The base insulating layer 131 may include silicon oxide.”), ¶[0093] (“The trench insulation material 113 may include silicon oxide . . .”), ¶[0105] (“The isolation region 110 . . . may be recessed.”).)



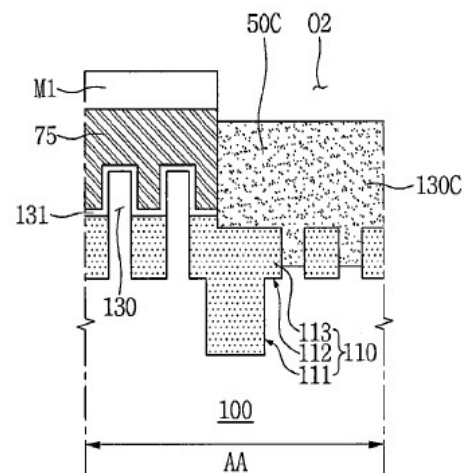
¶¶[0106]-[0107] (“[T]he method may include forming an insulating core layer 90 which completely or partially fills . . . the fin active cut space S4, and the fin active recess 130R. . . . The core layer 90 may include, for example, silicon nitride.”).)



101. Next, a portion of the dielectric layer is removed, thus forming a fin active core 130C. (Ha ¶¶[0108]-[0109] (“[T]he method may include forming a first cut field gate core 10C, a first fin gate core 40C, a second fin gate core 50C, a butting gate core 60C, and a fin active core 130C by partially removing the core layer 90 by performing a chamfering process.”).)

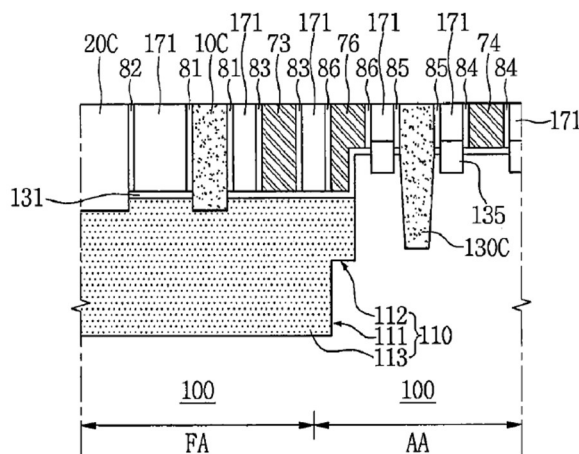


Ha, FIG. 8A

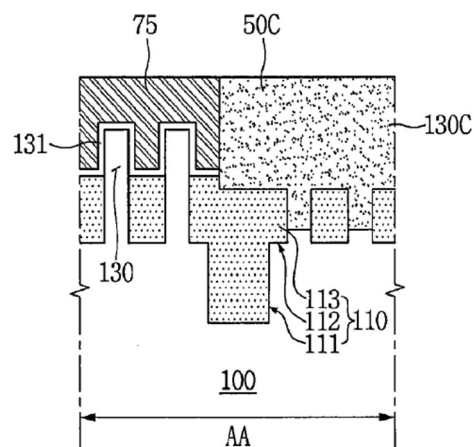


Ha, FIG. 8C

102. Then, as in FIGS. 9A and 9C below, the mask pattern is removed, and the structure is planarized. (Ha ¶¶[0110]-[0111].)

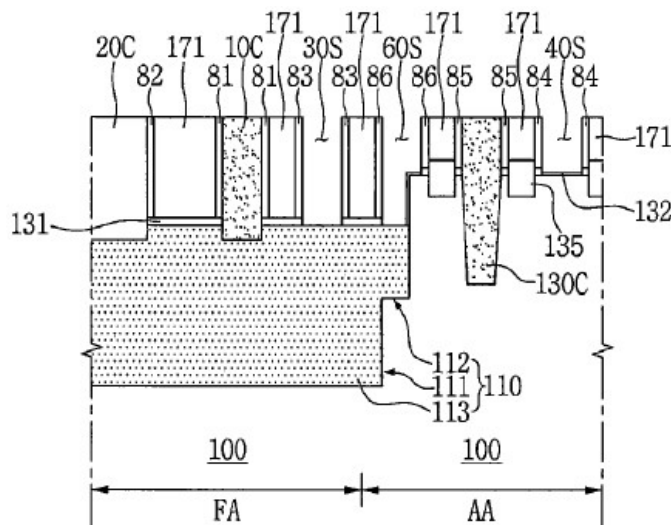


Ha, FIG. 9A

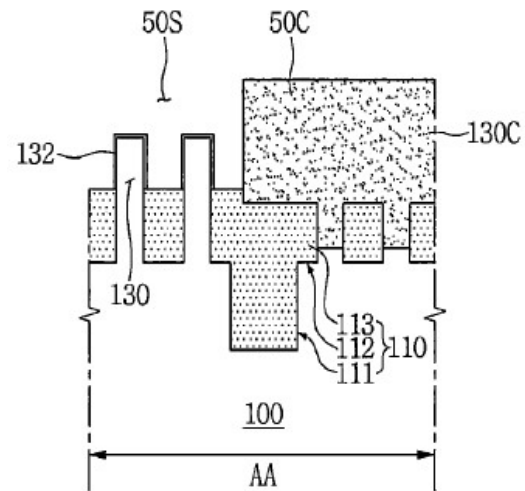


Ha, FIG. 9C

103. Ha's method continues by forming gate electrode spaces. To do this, the remnants of sacrificial gate structures 71-76 are removed, as in FIGS. 10A and 10C below. (Ha ¶[0112] (“[T]he method may include forming gate electrode spaces 10S, 20S, 30S, 40S, 50S, and 60S by removing the exposed sacrificial gate patterns 71 to 76 by performing a silicon etching process, and forming a thin surface insulating layer 132 on the surface of the fin active region 130 exposed in the fin gate electrode spaces 40S, 50S, and 60S by performing a washing process or a wet oxidation process.”).)



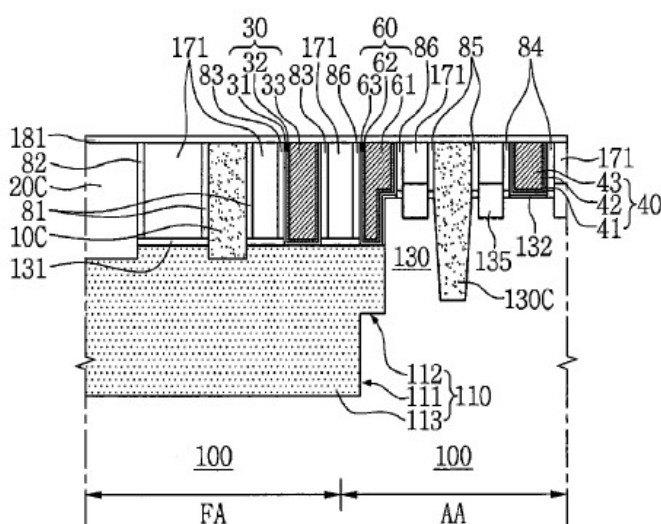
Ha, FIG. 10A



Ha, FIG. 10C

104. Replacement gate patterns are then formed in the gate electrode spaces, as in FIGS. 11A and 11C below. (Ha ¶¶[0113]-[0115] (“[T]he method may include forming gate patterns 10, 20, 30, 40, 50, and 60 in the gate electrode spaces 10S, 20S, 30S, 40S, 50S, and 60S The gate patterns 10, 20, 30, 40, 50, and 60 may include gate insulating layers 11, 21, 31, 41, 51, and 61, gate barrier layers 12, 22,

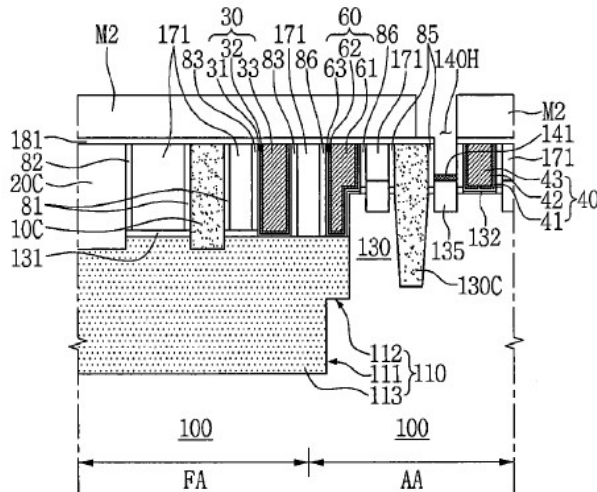
32, 42, 52, and 62, and gate electrodes 13, 23, 33, 43, 53, and 63, respectively.”.)



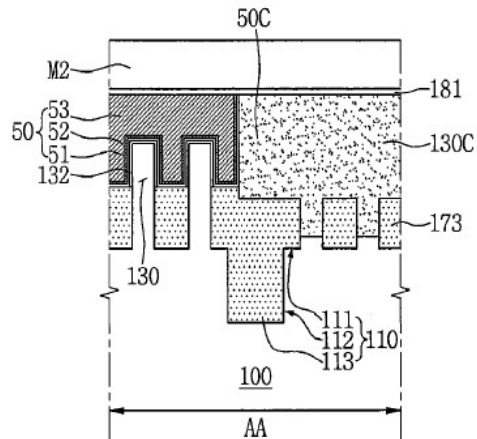
Ha, FIG. 11A

105. Next, a second mask pattern is formed on the first stopper layer 181. (Ha ¶[0116] (“[T]he method may include forming a second mask pattern M2 on the first stopper layer 181”).) An etching process is performed using the second mask pattern to remove part of the first stopper layer 181 and the interlayer insulating layer 171, thus exposing the source/drain region. (Ha ¶¶[0116]-[0118].) Then, a silicide layer 141 may be formed on the source/drain region, as in FIGS. 12A and 12C below. (Ha ¶¶[0116]-[0118] (“The forming of the silicide layer 141 may

include siliciding a surface of the exposed source/drain region 135 by performing a silicidation process.”.)

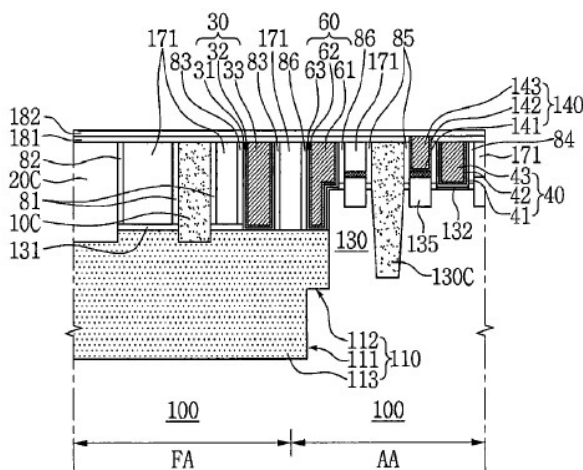


Ha, FIG. 12A

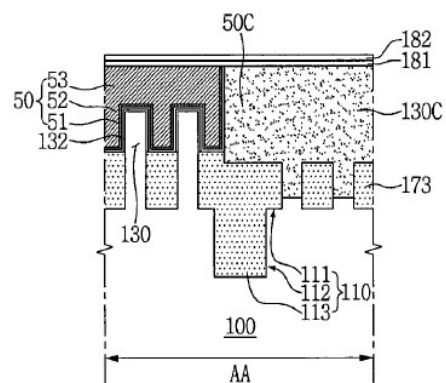


Ha, FIG. 12C

106. Next, a contact pattern may be formed into the hole and a second stopper layer may be formed on the contact pattern, as in FIGS. 13A and 13C below. (Ha ¶¶[0119]-[0121] (“[T]he method may include forming a contact pattern 140 in the contact hole 140H using a CMP process, and forming a second stopper layer 182 on the contact pattern 140.”).)

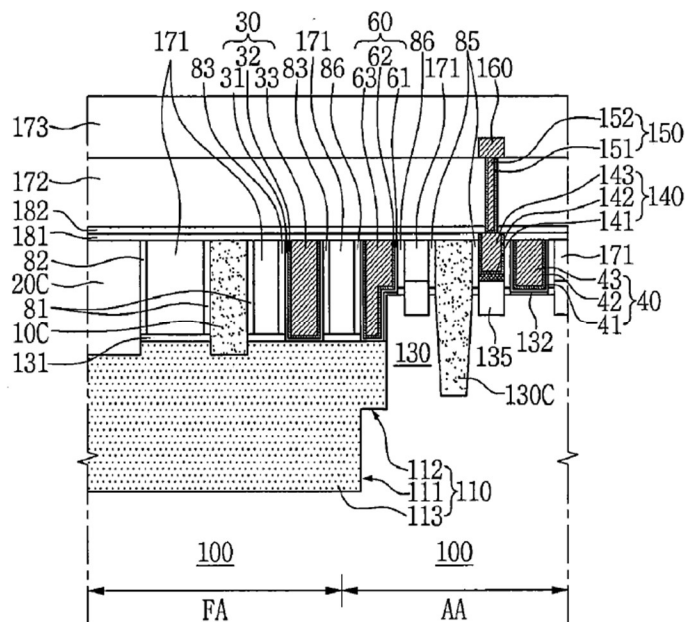


Ha, FIG. 13A

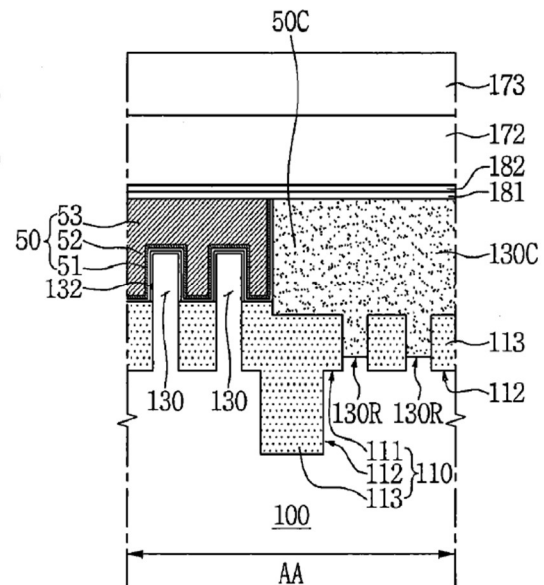


Ha, FIG. 13C

107. Finally, additional interlayer insulating layers may be formed above fin active core 130C, as shown below. (Ha ¶¶[0122]-[0125] (“[T]he method may include forming a second interlayer insulating layer 172 on the second stopper layer 182, and forming a via pattern 150 that connects to the contact pattern 140 and vertically extends through the second interlayer insulating layer 172. . . . Then, as described with reference to FIGS. 2A to 2C, the method may include forming a metal interconnection 160 on the via pattern 150, and forming a third interlayer insulating layer 173 which covers the metal interconnection 160.”).)



Ha, FIG. 2A

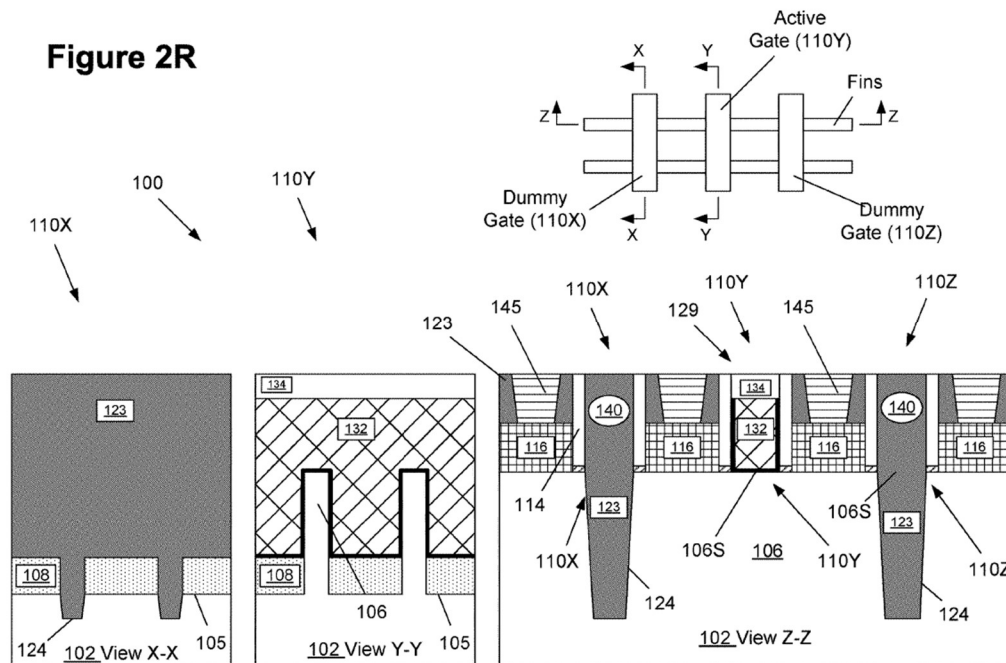


Ha, FIG. 2C

D. U.S. Patent No. 9,653,583 B1 (“Zhao”)

108. Zhao was filed on August 2, 2016, and issued on May 16, 2017. I have been told this qualifies Zhao as prior art.

109. In my opinion, applying the standard as stated in Section IV.B above, Zhao is analogous art to the '880 Patent because Zhao is in the same field of endeavor as the '880 Patent (semiconductor FinFET devices and methods for fabricating them). (See '880 Patent at 1:9-67; Zhao at 1:8-12, 3:40-60.) In my opinion, Zhao is also analogous art to the '880 Patent because a POSITA would have found it reasonably pertinent to at least one problem the '880 Patent purports to address, for example, fabricating FinFET semiconductor devices. (See '880 Patent at 1:9-67; Zhao at 1:8-12, 3:40-60.)



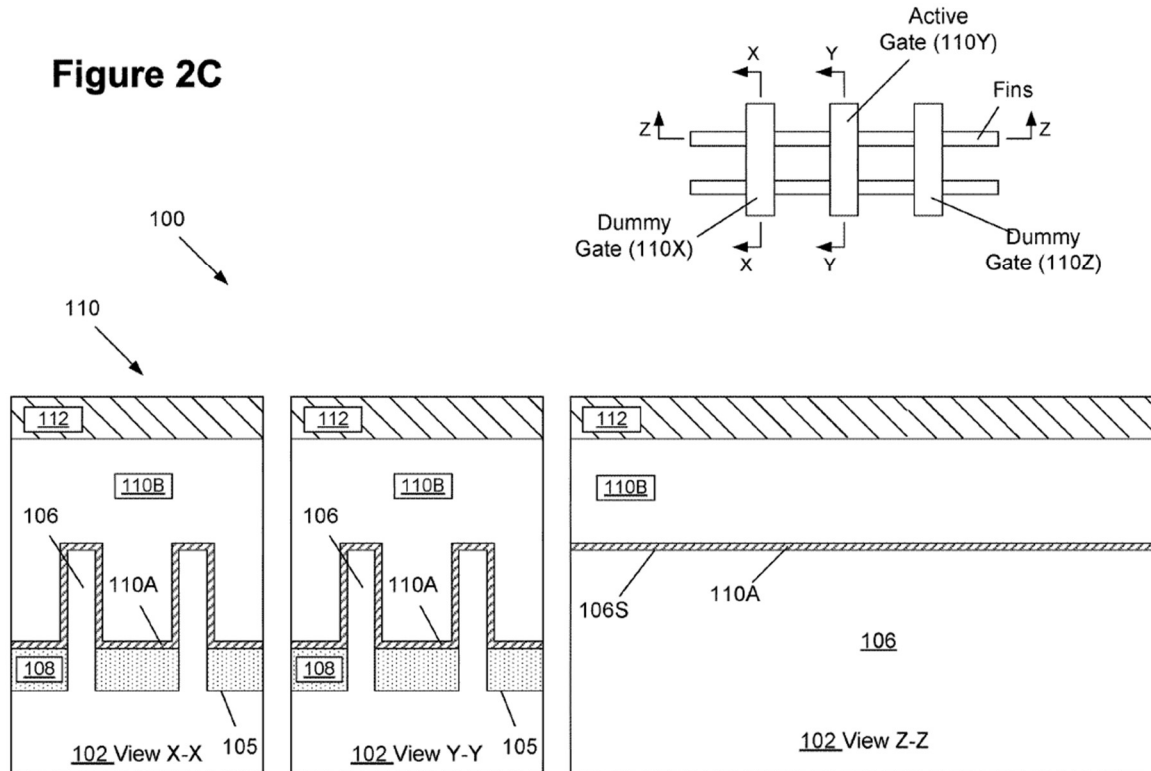
102: substrate	116: epi semiconductor	132: conductive materials
105: fin formation trenches	123: insulating material	134: gate cap layer
106: fins	124: isolation trenches	140: isolation structure
108: insulating material	129: replacement gate	145: conductive contacts
114: sidewall spacers		

110. Zhao describes “the manufacture of semiconductor devices, and, more specifically, . . . various novel methods of forming diffusion breaks [140] on integrated circuit (IC) products comprised of FinFET devices.” (Zhao at 1:8-12; *see also* Zhao at 4:3-5 (“forming diffusion breaks on IC products comprised of FinFET devices”), 5:8-26 (“forming a diffusion break on an integrated circuit product 100 comprised of FinFET devices”), 9:10-14 (“[I]nsulation material 123 positioned in the trenches 124 constitutes an isolation structure 140, or diffusion break, for the active FinFET device.”).)

111. Zhao’s process starts by patterning a semiconductor substrate 102 to include a plurality of fins 106 separated by trenches 105. (Zhao at 5:40-6:14 (“[O]ne or more etching processes were performed through the patterned etch mask 104 so as to define a plurality of fin-formation trenches 105 in the substrate 102. This results in the formation of a plurality of fins 106.”), FIG. 2A.)

112. Insulating material 108 (e.g., SiO₂) is formed into trenches 105 and is then subsequently recessed below the tops of fins 106. (Zhao at 6:15-27 (“The recessed layer of insulating material 108 may be formed by over-filling the trenches 105 with an insulating material, performing a chemical mechanical planarization (CMP) process . . . , and performing a recess etching process on the layer of insulating material 108 so as to recess the upper surface 108S of the layer of insulating material 108 to a desired height level within the trenches 105.”), FIG. 2B.)

113. Next, as Zhao's FIG. 2C shows below, a sacrificial gate insulation layer 110A (e.g., SiO_2), a sacrificial electrical gate electrode material 110B (polysilicon or amorphous silicon), and a gate cap layer 112 (e.g., silicon nitride) are deposited, as shown below in FIG. 2C. (Zhao at 6:28-42.)

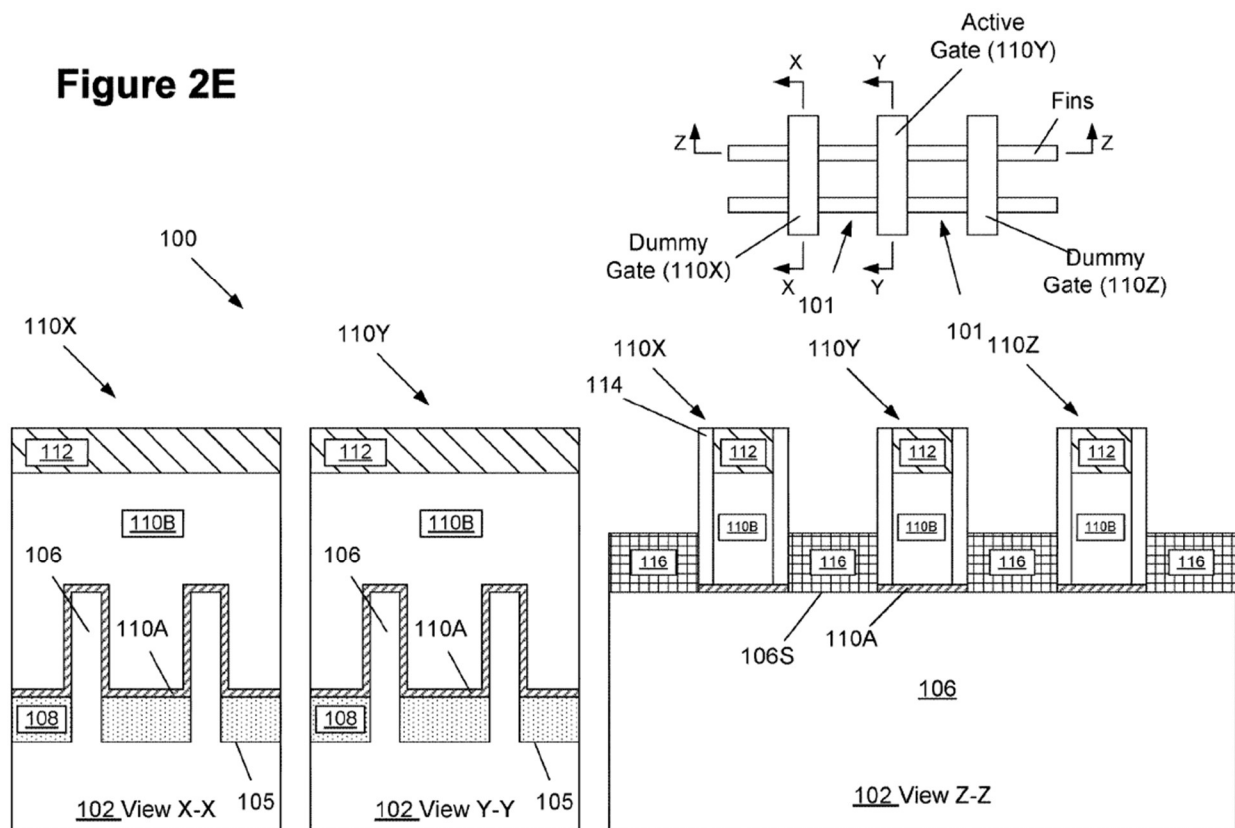


Zhao, FIG. 2C

114. Next, an etching process is performed on layers 110A, 110B, and 112 to form sacrificial gate structures 110X-110Z. (Zhao at 6:43-52, FIG. 2D.) Sacrificial gate structures 110X and 110Z are dummy gates, and sacrificial gate structure 110Y is used to define the location of an active gate for an active FinFET. (Zhao at 6:43-52.)

115. Then, as in FIG. 2E below, sidewall spacers 114 are created adjacent to sacrificial gate structures 110X-110Z, and an epi semiconductor material 116 is grown on fins 106 in the source/drain regions 101. (Zhao at 6:53-64 (“First, simplistically depicted sidewall spacers 114 were formed adjacent the sacrificial gate structures 110X-Z. Thereafter, epi semiconductor material 116 was grown on the portions of the fins 106 positioned in the source/drain regions 101 of the active FinFET device, i.e., on the portions of the fins 106 positioned laterally outside of the spacers 114 on the sacrificial gate structure 110Y for the active gate.”), FIG. 2E.)

Figure 2E

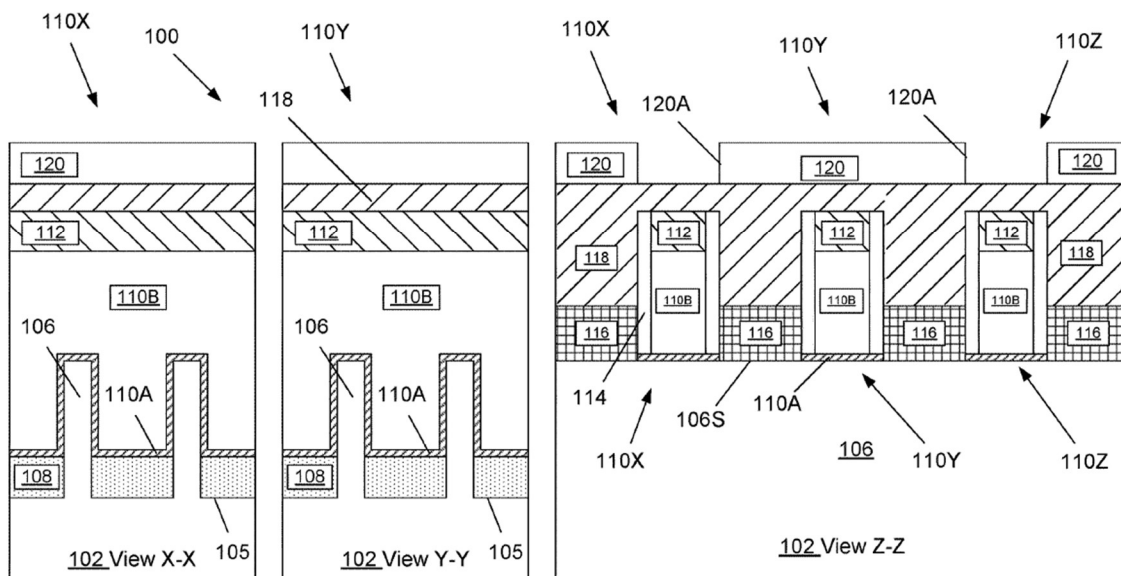


Zhao, FIG. 2E

116. Sacrificial material 118 is then formed over the substrate, and it fills the spaces between and above sacrificial gate structures 110X-110Z. (Zhao at 6:65-7:19 (“[T]he sacrificial layer of material 118 is formed on and in contact with the epi material 116 so as to overfill the lateral spaces between the gate structures 110X-Z.”), FIG. 2F.)

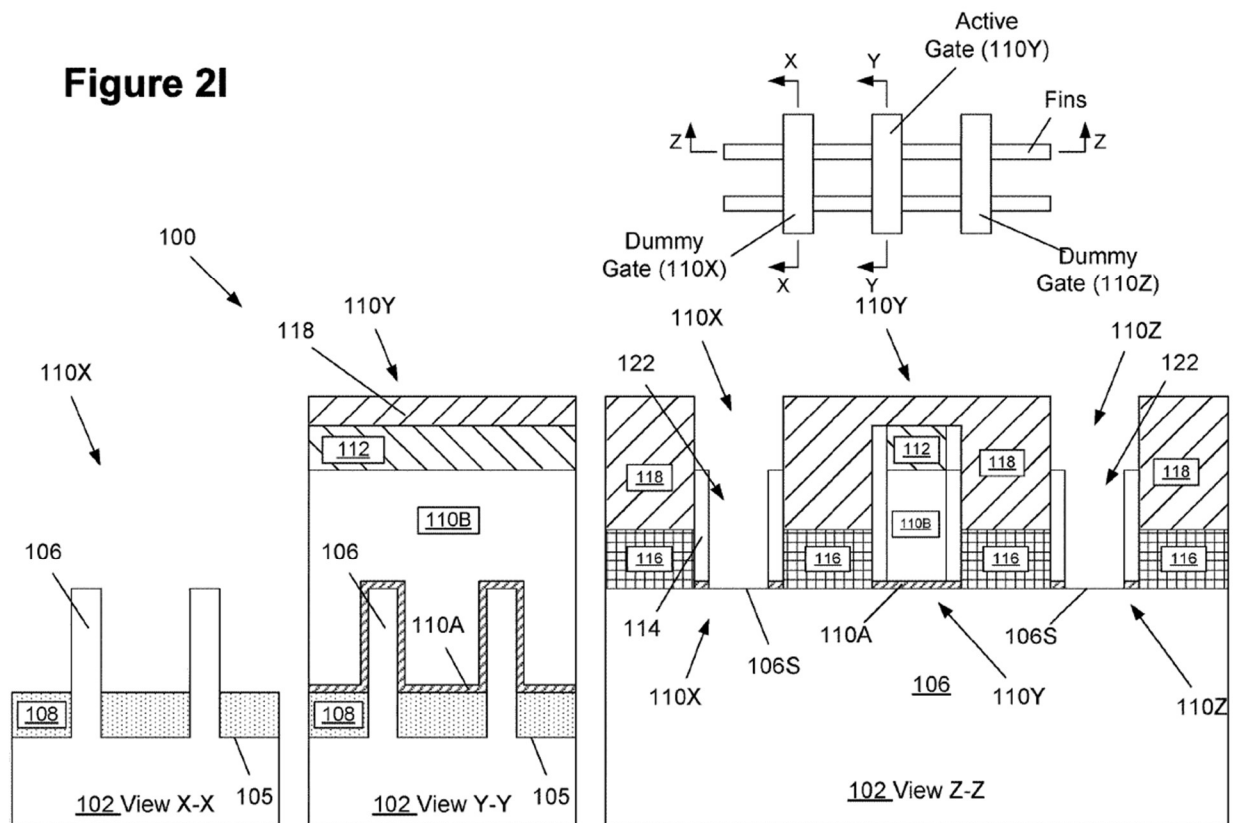
117. A patterned masking layer 120 with openings 120A is then formed over the sacrificial material 118. (Zhao at 7:20-26 (“FIG. 2G depicts the product 100 after a patterned masking layer 120, e.g., a patterned layer of photoresist, was formed above the product depicted in FIG. 2F.”), FIG. 2G.) As in FIG. 2G below, openings 120A expose the areas above dummy gate structures 110X and 110Z, and masking layer 120 covers active gate structure 110Y. (Zhao at 7:20-26.)

Figure 2G



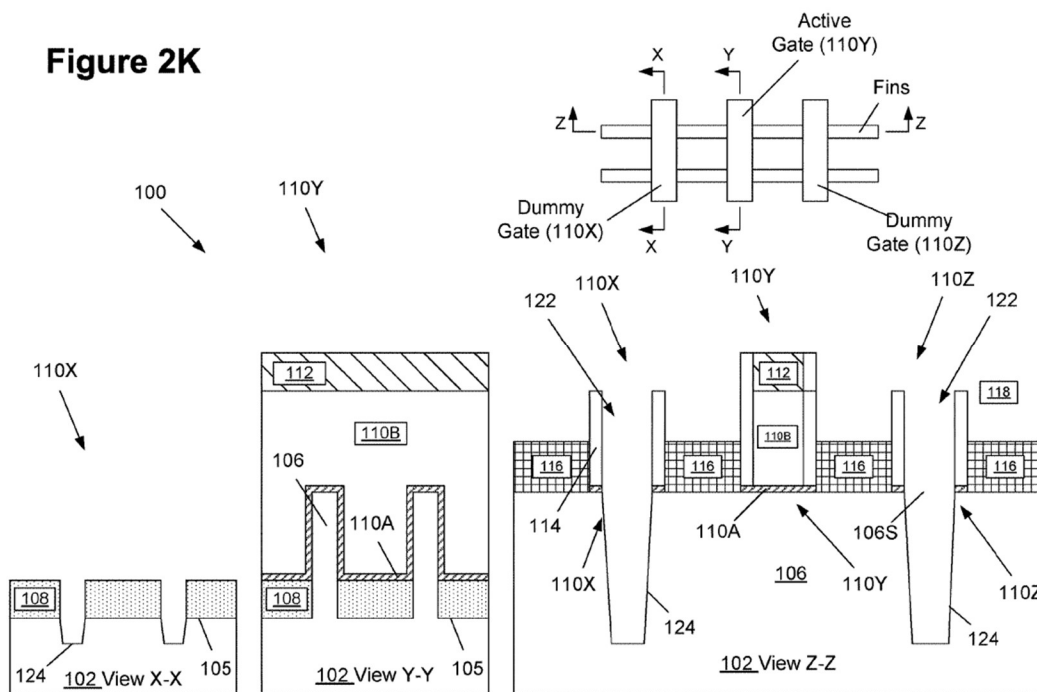
Zhao, FIG. 2G

118. The exposed sacrificial material 118 is removed by a recess etch through openings 120A, and a selective etching process is performed to remove gate cap layers 112 and part of the adjacent sidewalls 114. (Zhao at 7:27-39, FIG. 2H.) Then, patterned mask 120 and sacrificial gate layer 110 in openings 120A are also selectively removed. (Zhao at 7:40-57, FIG. 2I.) As FIG. 2I shows below, the result is that isolation cavities 122 are formed in openings 102A, and surfaces 106S of the fins are exposed. (Zhao at 7:40-57 (“These process operations result in the formation of isolation cavities 122 that expose the surface 106S of the fins 106 within the isolation cavities 122.”).)



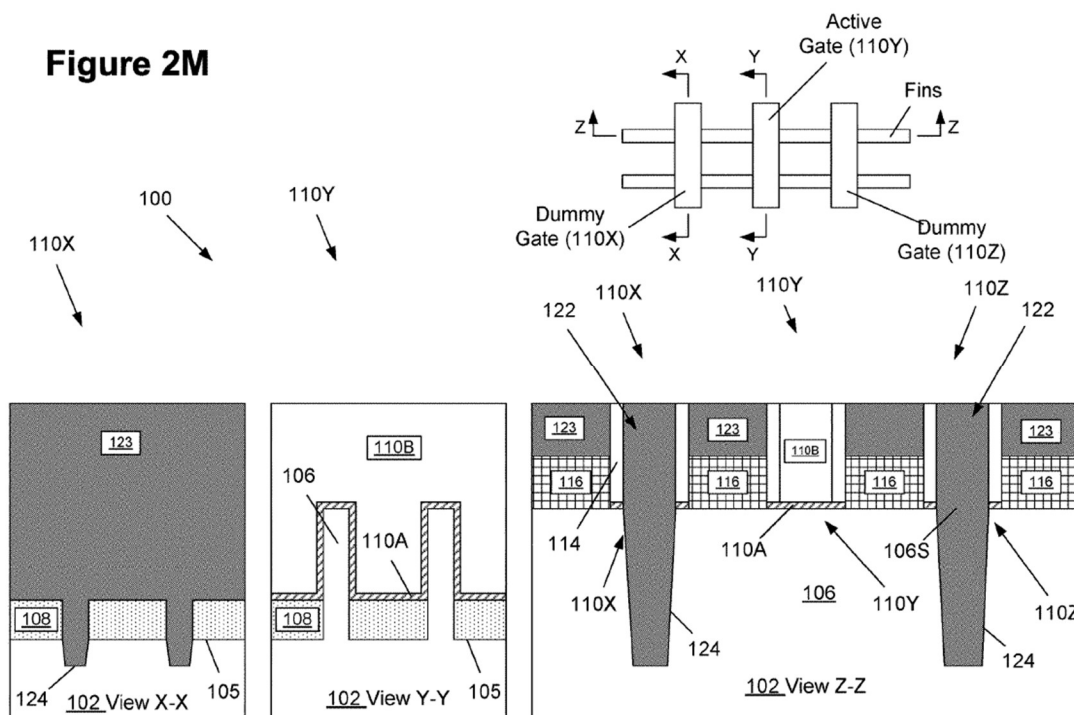
Zhao, FIG. 2I

119. Next, isolation trenches 124 are created by performing an anisotropic etch through isolation cavities 122 to remove a portion of the exposed fins 106. (Zhao at 7:58-8:5 (“[A] timed, anisotropic etching process was performed through the isolation cavities 122 to remove a portion of the fins 106 and thereby define isolation trenches 124 in the fins 106, and perhaps in the substrate 102.”), FIG. 2J.) “[T]his effectively removes or cuts the fin 106 in the areas of the fins 106 exposed by the isolation cavities 122 of the dummy gate structures 110X, 110Z.” (Zhao at 7:67-8:3.) Thereafter, as shown below in FIG. 2K, the epi semiconductor material 116 is exposed by selectively removing sacrificial layer 118. (Zhao at 8:6-8 (“FIG. 2K depicts the product 100 after the sacrificial layer of material 118 was removed, thereby exposing the epi semiconductor material 116.”), FIG. 2K.)



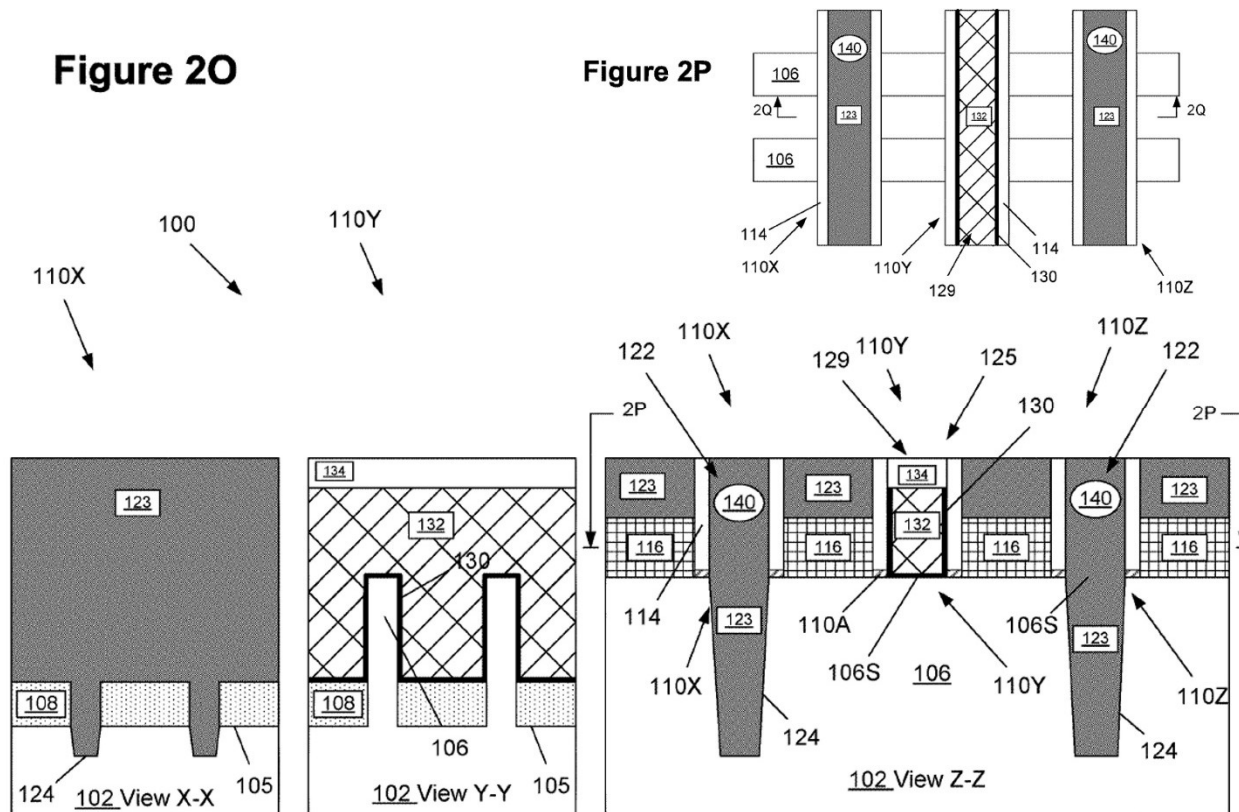
Zhao, FIG. 2K

120. Next, insulating material 123 (e.g., SiO₂) overfills trenches 124 and the areas previously occupied by sacrificial layer 118 to extend above the upper surface of sacrificial gate structure 110Y. (Zhao at 8:9-13 (“First, a layer of insulating material 123 such as silicon dioxide, was formed across the substrate 102 so as to overfill the trenches 124 and the cavities 122.”).) The layer of insulating material 123 is then planarized by CMP. (Zhao at 8:13-16, FIG. 2L.) As shown below, additional polishing then planarizes the structure to the top surface of sacrificial gate material 110B of sacrificial gate structure 110Y. (Zhao at 8:23-34 (“FIG. 2M depicts the product 100 after one or more planarization processes were performed that ultimately stops on the sacrificial gate material 110B of the sacrificial gate structure 110Y.”), FIG. 2M.)



Zhao, FIG. 2M

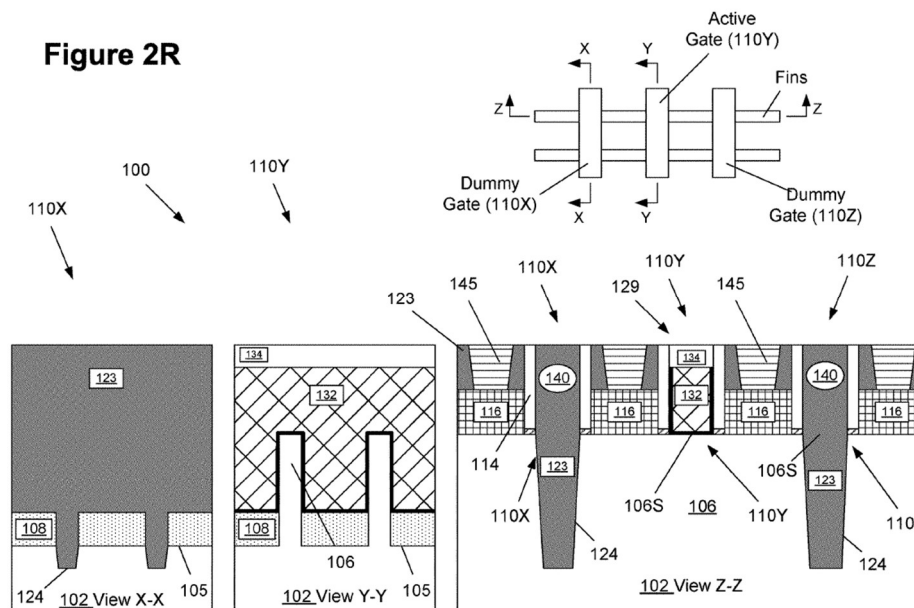
121. Next, one or more etching process are performed to remove sacrificial gate material 110B and, optionally, sacrificial gate insulation layer 110A from sacrificial gate structure 110Y. (Zhao at 8:35-45 (“[O]ne or more etching processes were performed to remove the sacrificial gate material 110B and the sacrificial gate insulation layer 110A of the active gate 110Y”), FIG. 2N.) This results in a replacement gate cavity 125 for a replacement gate structure. (Zhao at 8:35-45 (“[T]hese operations result in the exposure of the surface 106S of the fin 106 for the active gate 110Y, and the formation of a replacement gate cavity 125 for the active gate 110Y where a replacement gate structure will be formed.”).)



Zhao, FIGS. 20 (excerpted) & 2P

122. Next, as in FIG. 2O above, a replacement gate structure 129 is formed, comprising a high-k gate dielectric insulation layer 130, conductive materials 132, and a gate cap layer 134, and the structure is planarized using a CMP process. (Zhao at 8:46-9:9, FIGS. 2O-2Q.) Figure 2P below shows a plan view of the structure (omitting epi semiconductor material 116). (Zhao at 9:14-16 (“FIG. 2P is a simplistic plan view of a portion of the product 100 taken where indicated in FIG. 2O with the epi semiconductor material omitted.”); *see also* Zhao at 9:16-28.)

123. Zhao explains: “As will be appreciated by those skilled in the art after a complete reading of [Zhao], the insulation material 123 positioned in the trenches 124 constitutes an isolation structure 140, or [single] diffusion break, for the active FinFET device.” (Zhao at 9:10-14; *see also* Zhao at 9:21-23 (“As can be seen, the isolation structures 140 laterally isolate the active FinFET device 110Y.”).)



Zhao, FIG. 2R

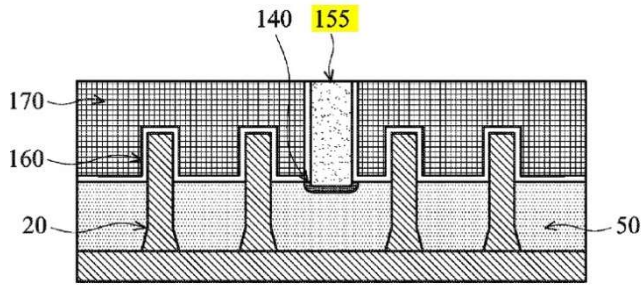
124. Finally, as shown above in FIG. 2R, conductive contacts 145 are formed in insulating material 123 to provide electrical contact to the source/drain regions where epi semiconductor material 116 is located. (Zhao at 9:29-45, FIG. 2R.)

E. U.S. Patent Application No. 2017/0125411 A1 (“Yu”)

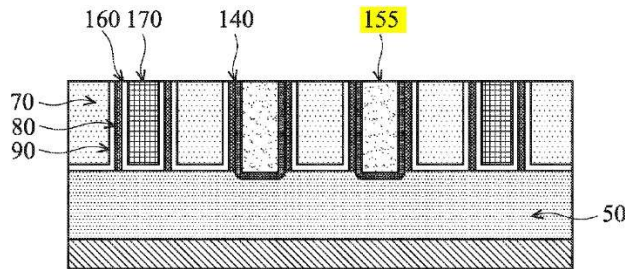
125. Yu was filed on November 4, 2015, and published on May 4, 2017. I have been told this qualifies Yu as prior art.

126. In my opinion, applying the standard as stated in Section IV.B above, Yu is analogous art to the ’880 Patent because Yu is in the same field of endeavor as the ’880 Patent (semiconductor FinFET devices and methods for fabricating them). (See ’880 Patent at 1:9-67; Yu ¶¶[0001]-[0002], ¶¶[0129]-[0131].) In my opinion, Yu is also analogous art to the ’880 Patent because a POSITA would have found it reasonably pertinent to at least one problem the ’880 Patent purports to address, for example, fabricating FinFET semiconductor devices. (See ’880 Patent at 1:9-67; Yu ¶¶[0001]-[0002], ¶¶[0055].)

127. Yu describes “a semiconductor device having a fin structure and its manufacturing process.” (Yu ¶[0001].) As the figures below show, this involves fabricating first and second gate structures that “are separated by a separation plug [155] made of an insulating material.” (Yu at Abstract, FIGS. 10A-10B.)



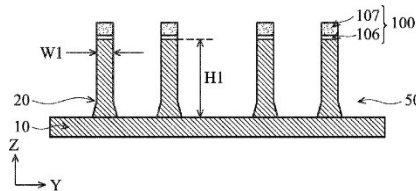
Yu, FIG. 10A (looking down the fins)



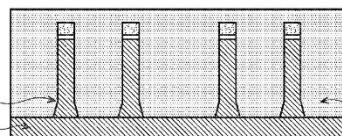
Yu, FIG. 10B (fins running left/right)

- 20:** fin structures
- 50:** isolation insulating layer
- 70:** interlayer dielectric layer (ILD)
- 80:** sidewall insulating layers
- 90:** CESL layer
- 140:** thin insulating layer
- 155:** separation plug
- 160:** gate dielectric layer
- 170:** gate electrode layer

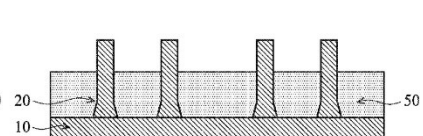
128. As the figures below demonstrate, the first step in Yu's process is to form an STI isolation insulating layer 50 (made of a silicon oxide, for example) around fin structures 20 etched into a substrate 10 (made of silicon, for example). (Yu ¶¶[0011]-[0022], FIGS. 1-3.) This is another good example of the STI formation process I describe in Section VI.B for making bulk silicon FinFETs.



Yu, FIG. 1



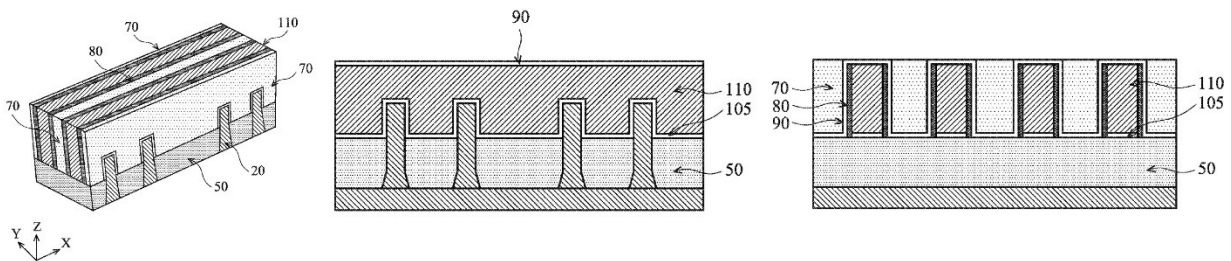
Yu, FIG. 2



Yu, FIG. 3

129. Next, "a gate insulating layer 105 and a poly silicon layer are formed over the isolation insulating layer 50 and the exposed fin structures 20, and then patterning operations are performed so as to obtain a gate layer 110." (Yu ¶[0023].)

The fin regions that were not covered by the gate are made into source/drain regions. (Yu ¶[0029] (“The fin structures not covered by the gate layers will become source/drain regions by appropriate source/drain fabrication operations.”).) Then, “sidewall insulating layers 80 (sidewall spacers) are also formed”; “a contact-etch stop layer (CESL) [90] is formed over the polysilicon layer 110 and the sidewall insulating layer 80”; and “an interlayer dielectric layer (ILD) 70 is formed in spaces between the gate layers 110.” (Yu ¶[0024]-[0026].) As shown below, the structure is then planarized. (Yu ¶[0027] (“Planarization operations, such as an etch-back process and/or a chemical mechanical polishing (CMP) process, are performed, so as to obtain the structure shown in FIGS. 4A-4D.”).) Yu’s ILD layer 70 may be made of “silicon oxide, silicon nitride, silicon oxynitride (SiON), SiOCN,” or another related material. (Yu ¶[0027].) Moreover, “[t]he insulating material for the isolation insulating layer 50 may be the same as or different from that for the ILD 70.” (Yu ¶[0026].)



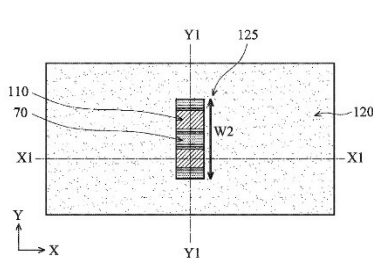
Yu, FIG. 4B

Yu, FIG, 4C (X-Z plane)

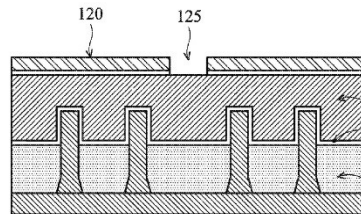
Yu, FIG, 4D (Y-Z plane)

130. As shown below, a mask pattern 120 with an opening 125 defines the regions in which the separation plug will eventually be formed. (Yu ¶[0030] (“Next,

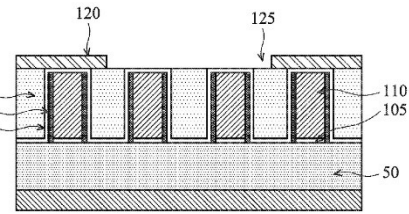
as shown in FIGS. 5A-5C, a mask pattern 120 is formed over the structure shown in FIGS. 4A-4D.”.) “The width W2 of the opening 125 along the Y direction is adjusted to expose a desired number of gate structures.” (Yu ¶[0030].)



Yu, FIG. 5C (X-Y)

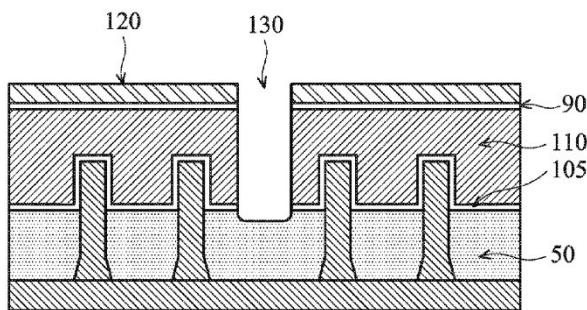


Yu, FIG. 5A (X-Z)

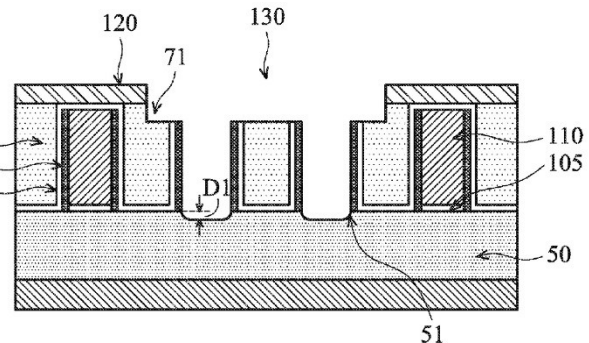


Yu, FIG. 5B (Y-Z)

131. The structure is then etched through openings 125 in the mask pattern 120. (Yu ¶[0031].) In doing so, “part of gate layer 110 and the gate insulating layer 105 are removed, so as to obtain a separation opening 130 that separates the gate layers 110.” (Yu ¶[0031].) Yu explains that “the upper portion 71 of the ILD 70 and the surface portion 51 of the isolation insulating layer 50 are also etched, as shown in FIGS. 6A and 6B.” (Yu ¶[0032].) “The depth D1, which is an etched depth of the surface portion 51 of the isolation insulating layer 50 is in a range from about 1 nm to about 10 nm.” (Yu ¶[0032].)

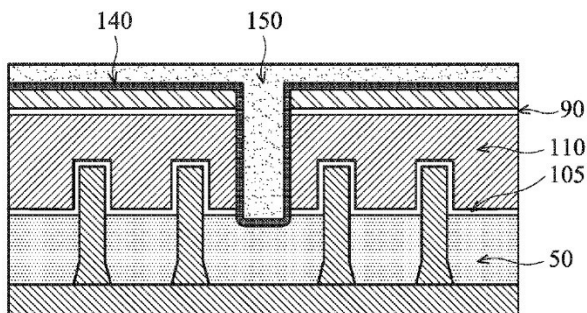


Yu, FIG. 6A (X-Z plane)

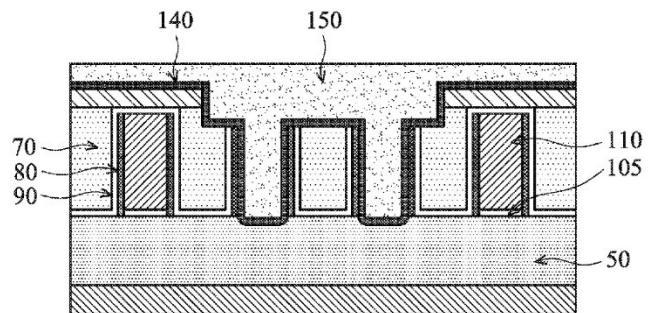


Yu, FIG. 6B (Y-Z plane)

132. Next, as shown below, thin and thick insulating films 140 and 150, respectively, are formed over the structure, filling the openings 130. (Yu ¶¶[0034]-[0037].) Thin insulating material 140 is the same material used for gate insulating layer 105 (e.g., silicon oxide), and thick insulating material 150 is a “silicon oxide or silicon nitride based material[] such as SiN, SiCN, SiON or SiOCN.” (Yu ¶¶[0035]-[0036].)

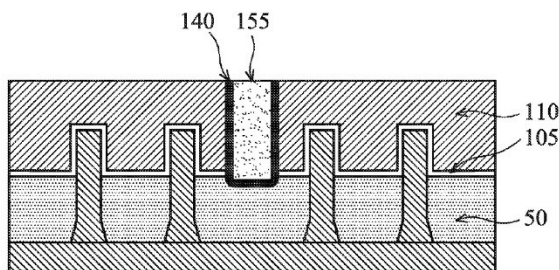


Yu, FIG. 7A (X-Z plane)

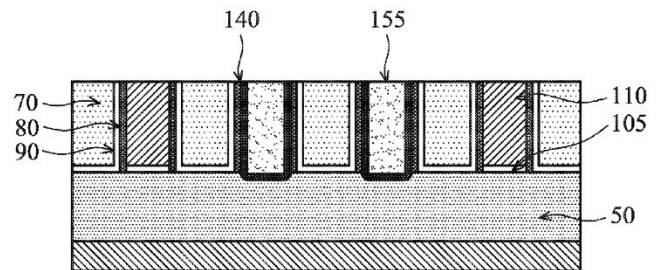


Yu, FIG. 7B (Y-Z plane)

133. After filling opening 130, “a planarization operation such as a CMP process is performed to expose the upper surface of the gate layers 110, as shown in FIGS. 8A and 8B” below. (Yu ¶[0037].)



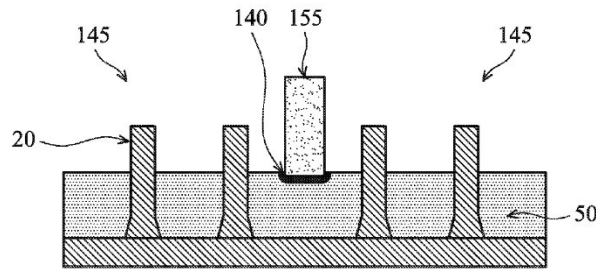
Yu, FIG. 8A (X-Z plane)



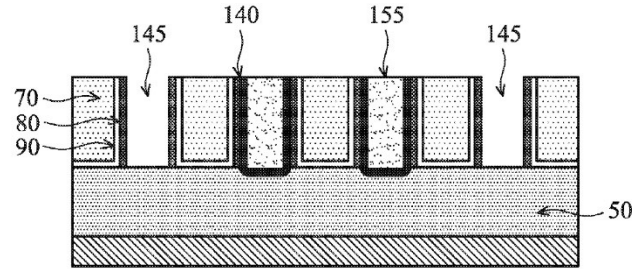
Yu, FIG. 8B (Y-Z plane)

134. Gate layers 110 and gate insulating layer 105, which serve as dummy layers, are then removed by selective etching, creating gate openings 145. (Yu

¶[0038] (“After the planarization operation to expose the gate layers 110, the gate layers 110 and gate insulating layer 105 (i.e., dummy layers) are removed . . .”).



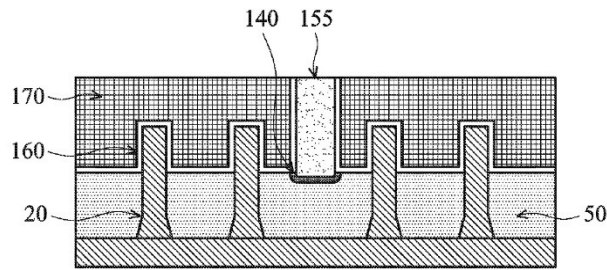
Yu, FIG. 9A (X-Z plane)



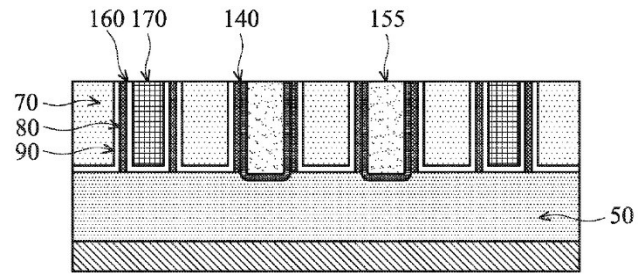
Yu, FIG. 9B (Y-Z plane)

135. (Note that I have omitted the axes in FIGS. 9A and 9B above because those axes, as they appear in Yu, are inconsistent with the axes identified in FIGS. 4A and 4B. As can be seen in FIG. 4A, the fins extend parallel to the Y-axis, whereas the gate structures extend parallel to the X-axis. However, in FIGS. 9A and 9B, the fins extend parallel to the X-axis while the gate structures extend parallel to the Y-axis. For consistency and clarity, I use labels above consistent with the axes from Yu’s FIGS. 4A and 4B.)

136. Next, a replacement metal gate stack, including gate dielectric layer 160 and metal gate electrode layer 170, is formed in gate openings 145. (Yu ¶[0039]-[0042].) Gate dielectric layer 160 may comprise a high-k dielectric layer, and metal gate electrode layer 170 may comprise a suitable work function metal. (Yu ¶[0040]-[0042].) The structure is then planarized, as in FIGS. 10A and 10B below, which removes any remaining metal from the upper surface of the structure. (Yu ¶[0043].)



Yu, FIG. 10A (X-Z plane)



Yu, FIG. 10B (Y-Z plane)

137. Though not shown above, electrical contacts and interconnections would then be formed, as in any integrated circuit. (Yu ¶[0045] (“It is understood that the structure shown in FIGS. 10A-10D undergoes further CMOS processes to form various features such as interconnect vias, interconnect metal layers, passivation layers, etc.”).)

IX. The Challenged Claims of the '880 Patent are Unpatentable

138. By June 29, 2017, FinFETs like the ones described in the '880 Patent were already known and used extensively throughout the semiconductor industry. As I explain above in Sections VI.B through VI.D, for example, bulk silicon FinFETs, single diffusion breaks (“SDBs”), and replacement metal gates were well-known. So were various ways for manufacturing them. For reasons I explain in greater detail below, it is my opinion that a person of ordinary skill in the art would have understood the '880 Patent describes a pre-existing method for forming a FinFET device with an SDB. The chart below summarizes my opinions.

Ground	Unpatentable Claim(s)	Basis	Reference(s)
1A	1-12	Obviousness	Doris, Ha
1B	1-12	Obviousness	Doris, Ha, Colinge
2A	1-5, 7-8, 10-11	Anticipation	Ha
2B	1-5, 7-8, 10-11	Obviousness	Ha
2C	9	Obviousness	Ha, Zhao
2D	12	Obviousness	Ha, Yu

A. Ground 1A: The Combination of Doris and Ha Renders Obvious Claims 1-12

139. The combination of Doris and Ha involves only minor, textbook variations of Doris that would have been obvious, as Ha demonstrates, for example.

140. First, my analysis of Ground 1A relies on Doris’s disclosed “bulk silicon . . . arrangement.” (Doris ¶[0043].) This simply means that Doris’s fin isolation regions 404 would not be a buried oxide layer underneath the fins, but rather an STI oxide that surrounds the fins. (*See* Section VIII.B above and Section IX.A.1.a-b below.) This distinction is trivial. In fact, as I explain in Section VI.B, it is the textbook distinction between SOI FinFETs and bulk silicon FinFETs. (*See* Colinge at 50-51, 65-66, Figs. 2.2, 2.14.) This difference does not alter any other aspects of Doris’s structure or process flow. Indeed, Doris’s process flow can be applied to “a bulk silicon substrate, a silicon on insulator substrate or a SiGe on insulator substrate.” (Doris ¶[0040].) A person of ordinary skill in the art would have understood that, other than the distinction described in Section VI.B, Doris’s process

flow would have been the same for a bulk silicon substrate. A person of ordinary skill in the art would have possessed this knowledge.

141. Second, my analysis of Ground 1A appreciates that the etching sequence used to cut Doris's fins will remove some of the fin isolation oxide. This would have been an obvious and thoroughly expected consequence of removing one silicon oxide layer (Doris's dummy gate oxide layer) from directly on top of, and in contact with, another silicon oxide layer (Doris's fin isolation layer). (*See* Section IX.A.1.c below.) Again, this is something anyone who took an introductory semiconductor processing course would have learned.

1. The Doris-Ha Combination

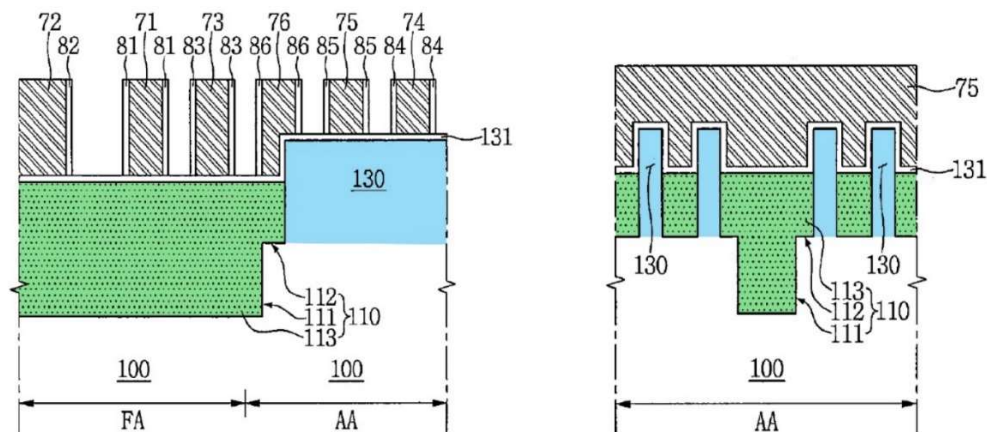
a. Doris expressly discloses a bulk silicon embodiment, which a POSITA would have known involves forming STI surrounding the fins

142. Doris explains the following about its embodiments:

FIGS. 4-18 illustrate an exemplary method of forming a finFET device having stressed fins. . . . The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however alternate exemplary embodiments may include a **bulk silicon**, a bulk SiGe arrangement or a SiGe on insulator arrangement.

(Doris ¶[0043] (emphasis added); *see also* Doris ¶[0040] (“The substrate 101 may include, a **bulk silicon substrate**, [or] a silicon on insulator substrate” (emphasis added))).

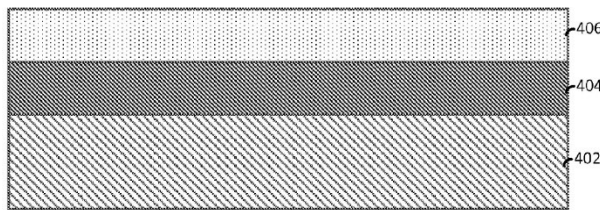
143. A person of ordinary skill in the art would have understood what Doris means by “bulk silicon substrate,” including how Doris’s illustrated SOI embodiment would be adapted in that context. (See Section VI.B above (explaining the difference between SOI and bulk silicon FinFETs).) For example, a person of ordinary skill in the art would have known that FinFETs formed using a bulk silicon substrate are electrically isolated from one another by forming a recessed shallow trench isolation (“STI”) surrounding the fins. (Colinge at 65-66, Fig. 2.14.) Ha does this, for example, as shown below. Ha’s 130 (blue) are surrounded by insulation material 113 that fills shallow trenches 112 (i.e., an STI) (green). (Ha ¶[0093], FIGS. 3A, 3C.) (Ha also has a deep trench 111, which is immaterial here.)



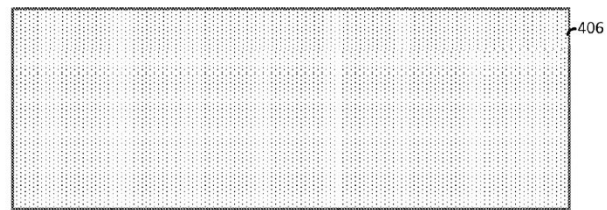
Ha, FIG. 3A (Fin Oriented Left-Right) Ha, FIG. 3C (Fin In/Out of Page)

144. Doris’s FIG. 4, on the left below, shows an SOI substrate with a silicon layer 402, insulator layer 404, and semiconductor layer 406 (e.g., silicon). (Doris ¶[0043].) A person of ordinary skill in the art would have understood, however, that in an embodiment using a bulk silicon substrate, FIG. 4 would depict

just a bulk silicon wafer. (See Doris ¶[0040] (“The substrate 101 may include, a bulk silicon substrate, a silicon on insulator substrate or a SiGe on insulator substrate.”), ¶[0043] (“The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however alternate exemplary embodiments may include a bulk silicon, a bulk SiGe arrangement or a SiGe on insulator arrangement.”).)

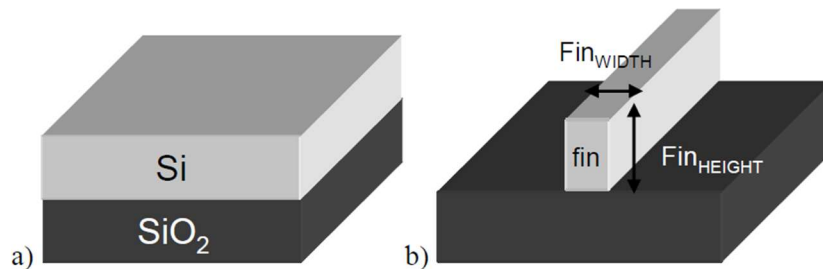


Doris, FIG. 4 (SOI)

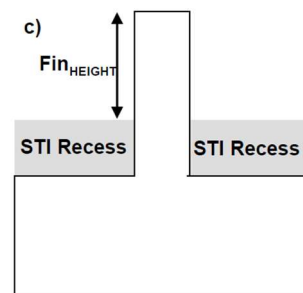


Alternative FIG. 4 (Bulk Si)

145. A person of ordinary skill in the art would have known from prior training that the basic structural difference between SOI FinFETs and bulk silicon FinFETs is their initial fin insulation layers. (See Section §VI.B above.) SOI FinFETs include a buried oxide isolation layer (shown on the left below in dark gray) beneath the fins. (Colinge at 50-51, FIG. 2.2.) Bulk silicon FinFETs include a recessed STI layer (shown on the right below in light gray) surrounding the fins. (Colinge at 65-66, Fig. 2.14.)

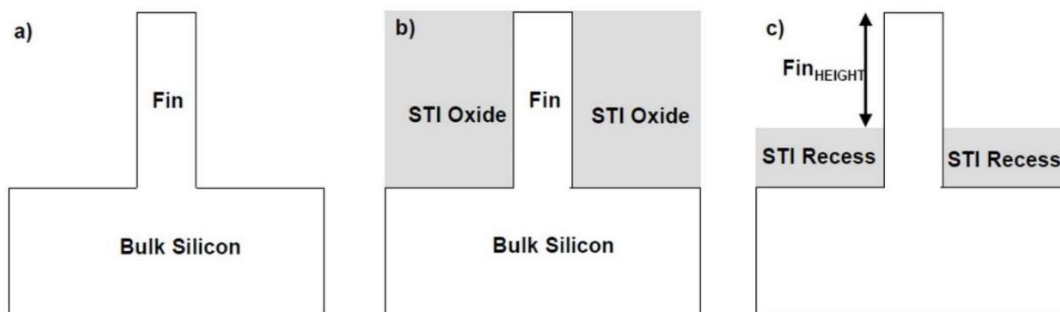


Colinge, Fig. 2.2(a)-(b) (SOI)



Colinge, Fig. 2.14(c) (Bulk Si)

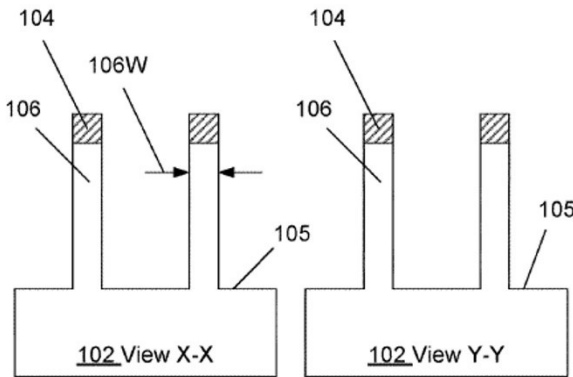
146. A person of ordinary skill in the art would have recognized that Doris’s disclosure of bulk silicon FinFETs implies certain associated fabrication steps for isolating the bulk silicon fins, illustrated below. (See Doris ¶[0069] (stating that “steps may be added”); Ha ¶¶[0091]-[0093], FIGS. 3A-3C.) First, fins are formed by patterning a bulk silicon substrate. (Colinge at Fig. 2.14(a) (“Fin etched in bulk silicon, the initial Fin_{HEIGHT} is greater than final device Fin_{HEIGHT} to allow some STI (Shallow trench Isolation) oxide.”).) Second, a silicon oxide STI is deposited on the substrate, extending above the initial fin height, and is planarized to the top of the fins. (Colinge at Fig. 2.14(b) (“STI oxide deposition and planarization.”).) Third, a recess etch is performed in the STI to yield a fin with the desired height, surrounded by recessed STI. (Colinge at 2.14(c) (“STI oxide recess to expose silicon fin with desired Fin_{HEIGHT} .”).)



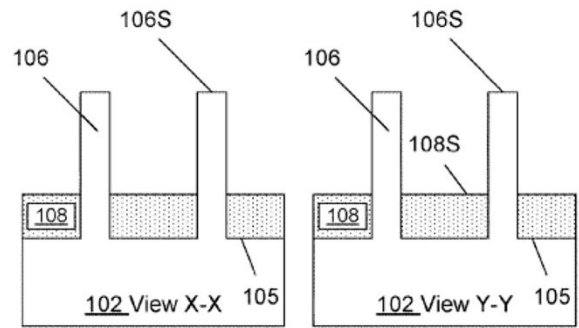
Colinge, Fig. 2.14(a)-(c)

Zhao and Yu also confirm this fundamental aspect of making bulk silicon FinFETs. Zhao explains a “recessed layer of insulating material 108 may be formed by over-filling the trenches 105 with an insulating material, performing a chemical

mechanical planarization (CMP) process . . . and performing a recess etching process” (Zhao at 6:15-27.) Zhao’s FIGS. 2A and 2B below illustrate this.

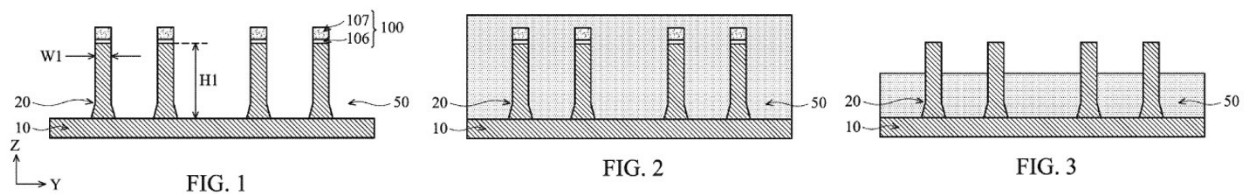


Zhao, FIG. 2A (excerpted)



Zhao, FIG. 2B (excerpted)

Yu similarly explains “an insulating material layer 50 to form an isolation insulating layer is formed over the substrate 10 so as to fully cover the fin structures 20. . . . [A] planarization operation is performed so as to remove upper part of the isolation insulating layer 50 Then, the isolation insulating layer 50 is further removed so that an upper part of the fin structures 20, which is to become a channel region, is exposed” (Yu ¶¶[0019]-[0021].) Yu’s FIGS. 1-3 below illustrate this process.

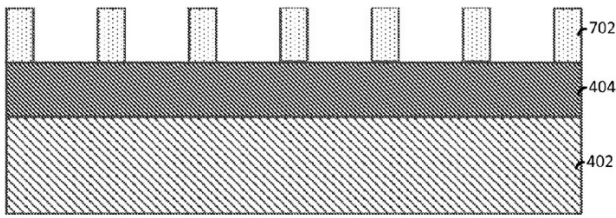


Yu, FIGS. 1-3

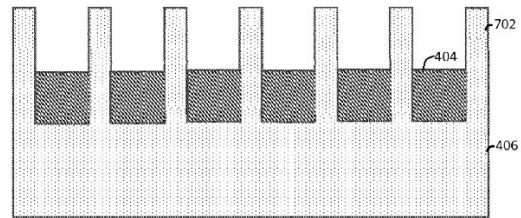
b. A POSITA understood Doris's process flow as applied to a bulk silicon substrate

147. Doris discloses that fins 702 are etched into an SOI substrate using an oxide layer 502 and hardmask layer 504 as a mask. (Doris ¶¶[0044]-[0046], FIGS. 5-7.) Then, the remnants of oxide layer 502 and hardmask layer 504 are removed, as shown below in modified FIG. 7. (Doris ¶¶[0046]-[0047], FIG. 7.) A person of ordinary skill in the art would have understood that the same process flow would apply in a bulk silicon arrangement, without meaningfully altering any other aspects of Doris's structure or process flow. (See Section VI.B above; Colinge at 65-66, Fig. 2.14.)

148. A bulk silicon wafer, unlike an SOI wafer, lacks insulator a buried oxide layer 404. A person of ordinary skill in the art would have known that a recessed STI layer would be formed around fins 702 in Doris's disclosed bulk silicon arrangement, performing the same isolation function as SOI insulator layer 404. (Colinge at Figs. 2.2, 2.14; *see also* Section VI.B above.) The alternative figure below on the right shows a bulk silicon substrate 406 with fins 702 surrounded by an STI layer 404. For a bulk silicon substrate, a person of ordinary skill in the art would have understood Doris's process flow would then proceed identically as described in the specification for an SOI substrate, and this would be the only material difference. (See Section VI.B above.)



**Based on Doris, FIG. 7 (SOI)
(modified to remove masks)**

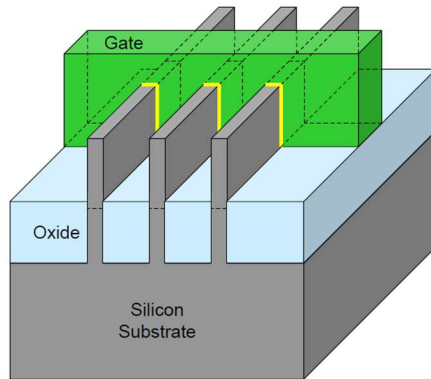


**Alternative Figure (Bulk Si)
(modified to remove masks)**

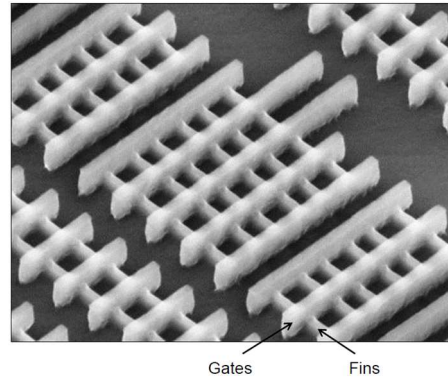
149. A person of ordinary skill in the art would have been motivated to perform the steps described above in the context of Doris’s disclosed process flow because Doris expressly teaches applying this process flow using a bulk silicon substrate. (Doris ¶[0040] (“The substrate 101 may include, a bulk silicon substrate, a silicon on insulator substrate or a SiGe on insulator substrate.”), ¶[0043] (“The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however alternate exemplary embodiments may include a bulk silicon, a bulk SiGe arrangement or a SiGe on insulator arrangement.”).) A person of ordinary skill in the art would have understood Doris’s process flow is applicable to both SOI and bulk silicon substrates simply by accounting for the basic difference between SOI FinFETs and the more prevalent bulk silicon FinFETs. (See Section VI.B above.)

150. Additionally, a person of ordinary skill in the art would have had a reasonable expectation of success. In fact, Doris expressly encourages the use of its process flow with a bulk silicon substrate. (Doris ¶[0040], ¶[0043].) Additionally, FinFETs made using bulk silicon substrates were commonly used commercially beginning in 2011, long before the application for the ’880 Patent was filed (see

below). For example, by 2011 Intel was using tri-gate transistors (i.e., FinFETs) for its 22 nm logic technology. (Intel_22nm_Details at 2.) As shown below, Intel's FinFETs were formed from bulk silicon substrates using the same textbook STI process I describe in Section VI.B. (Intel_22nm_Details at 7-8.)



Intel_22nm_Details, 7



Intel_22nm_Details, 8

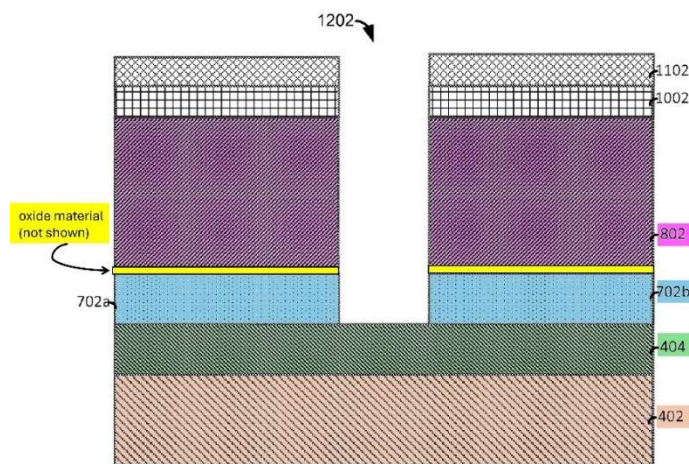
151. In my opinion, a person of ordinary skill in the art thus would have readily understood and found it obvious, based on textbook knowledge of SOI and bulk silicon FinFETs, how to apply Doris's disclosed process flow to a bulk silicon substrate, as I describe above.

152. Applying the legal standards explained to me, as summarized above in Section IV.B, it is my opinion that a person of ordinary skill in the art would have viewed this as an obvious example of the following: (1) a simple adoption of one disclosed and well-known element (bulk silicon substrate) instead of another (SOI substrate) to obtain predictable results (e.g., lower wafer cost and better substrate heat transfer rate, *see* Colinge at 65); (2) a choice from among two identified, predictable solutions (SOI or bulk substrate), with a reasonable expectation of

success; and (3) a teaching, suggestion, or motivation in the prior art, (Doris ¶[0040], ¶[0043] (bulk silicon may be used), ¶[0069] (variations acceptable)) that would have led a person of ordinary skill in the art to arrive at the claimed invention.

c. A POSITA would have found it obvious that etching Doris's cavity 1202 would partially etch the STI in Doris's bulk silicon embodiment, as it does in Ha

153. Doris deposits an amorphous silicon (α -Si) or polysilicon layer 802 (magenta) covering the fins 702 (blue). (Doris ¶[0047], FIGS. 8-9.) Additionally, “a layer of oxide material [added in yellow] may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802.” (Doris ¶[0047].) Doris then discloses cutting the fins with a cavity 1202 by “a dry etching or RIE process that removes exposed portions of the hardmask 1002, exposed portions of the α -Si layer 802, and the fins 702.” (Doris ¶[0050], FIGS. 12, 14.)



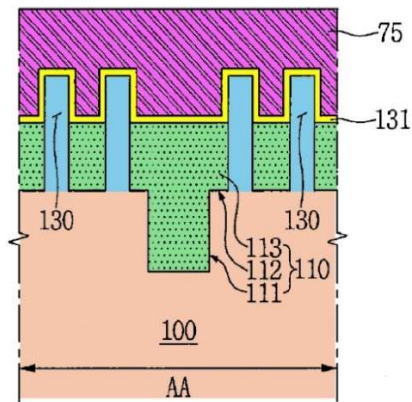
Doris, FIG. 12 (annotated)

154. A person of ordinary skill in the art would have understood the “layer of oxide material (not shown)” (added in yellow above) must also be removed to

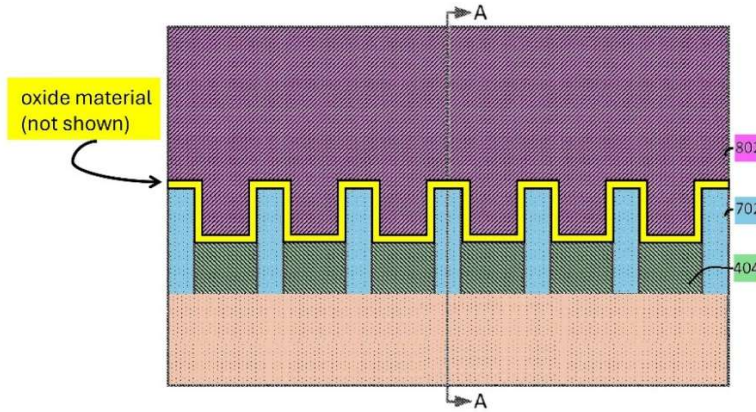
form cavity 1202 since it overlays fins 702, and the exposed portions of those fins are removed by etching. (Doris ¶[0047] (“[A] layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802.”), ¶[0050] (“FIG. 12 illustrates . . . a dry etching or RIE process that removes exposed portions of . . . the fins 702. The etching process results in a cavity 1202.”), FIGS. 8, 12.)

155. A person of ordinary skill in the art would have understood the same etching sequence applies to Doris’s bulk silicon arrangement. (Doris ¶[0043] (“The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however alternate exemplary embodiments may include a bulk silicon . . . arrangement.”).) But because the STI of a bulk silicon FinFET surrounds the fins rather than being positioned below them, a person of ordinary skill in the art would have understood the etching process appears as in Ha (see below). (Ha ¶¶[0099]-[0105] (“The isolation region 110 . . . may be recessed.”), FIGS. 5A-6C.)

156. Ha confirms by analogy that it would have been obvious to remove part of the STI when etching Doris’s layer of gate oxide material. (Ha ¶[0105] (“The isolation region 110 . . . may be recessed.”).) As illustrated below in Ha’s FIG. 4C and the analogous version of Doris’s FIG. 8 (modified to show Doris’s bulk silicon arrangement), Doris and Ha begin with the same layers.



Ha, FIG. 4C



Alternative to Doris, FIG. 8 (Bulk Silicon)

157. Ha's silicon substrate 100 corresponds to Doris's disclosed (but not illustrated) bulk silicon substrate 402 (both in peach above).⁹ Ha's fin active regions 130 correspond to Doris's fins 702 (both in blue above).¹⁰ Ha's silicon oxide base insulating layer 131 corresponds to Doris's "layer of oxide material (not shown)" (both in yellow above).¹¹ And Ha's fin gate pattern 75 corresponds to Doris's amorphous silicon (α -Si) or polysilicon layer 802 (both in magenta above).¹²

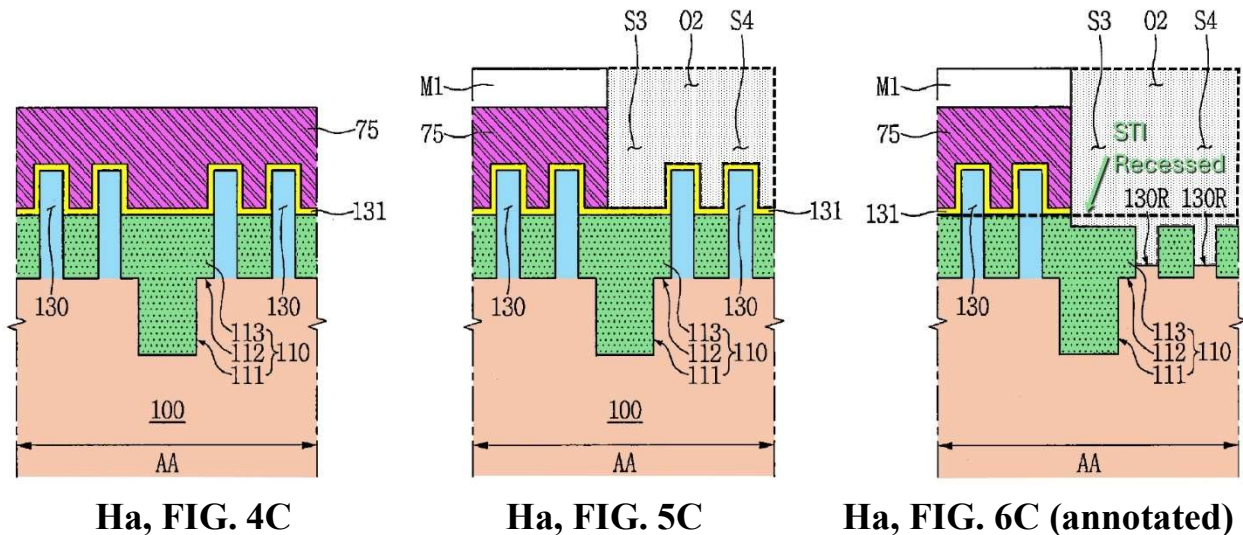
⁹ See Ha ¶[0066] ("The substrate 100 may include a silicon wafer."); Doris ¶[0040] ("The substrate 101 may include, a bulk silicon substrate . . ."), ¶[0043] ("The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however alternate exemplary embodiments may include a bulk silicon . . . arrangement.").

¹⁰ See Ha ¶[0067] ("The fin active region 130 may be a portion of the substrate 100."); Doris ¶[0046] ("The etching process defines the fins 702 by removing exposed semiconductor material 406 . . ."); Section IX.A.1.a-b above.

¹¹ See Ha ¶[0089] ("The base insulating layer 131 may include silicon oxide."); Doris ¶[0047] ("[A] layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 . . .").

¹² See Ha ¶[0095] ("sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon"); Doris ¶[0047] ("FIG. 8 illustrates the deposition of an

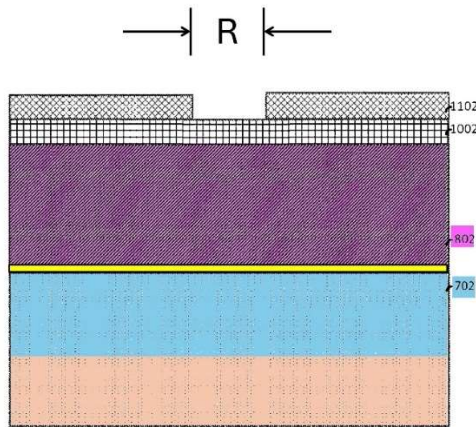
158. To form fin active cut-zone CZ3 (shaded in gray below), Ha forms mask M1 and etches through the openings of mask M1—first through fin gate pattern 75 (magenta below), then base insulating layer 131 (yellow below), and then through part of fin active regions 130 (blue below). (Ha ¶¶[0096]-[0105], FIGS. 4A-6C.) Notably, Ha explains that the exposed portions of the isolation region 110 “may be recessed,” as FIG. 6C below indicates. (Ha ¶[0105]; *see also* Ha at FIGS. 6A-6C.) Ha’s FIGS. 4C, 5C, and 6C below illustrate this etching sequence.



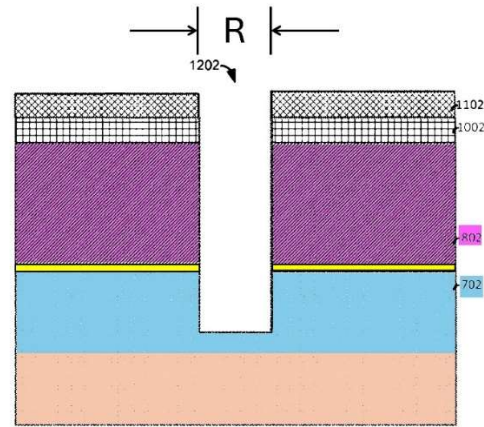
159. A person of ordinary skill in the art would have understood, or at least found obvious, that Doris’s cavity 1202 should be formed by the same etch sequence. (Doris ¶[0050] (“[A] dry etching or RIE process . . . removes exposed

amorphous silicon (α -Si) layer 802 over the fins 702 and exposed portions of the insulator layer 404.”).

portions of the hardmask 1002, exposed portions of the α -Si layer 802, and the fins 702. The etching process results in a cavity 1202.”), FIGS. 11-12.)

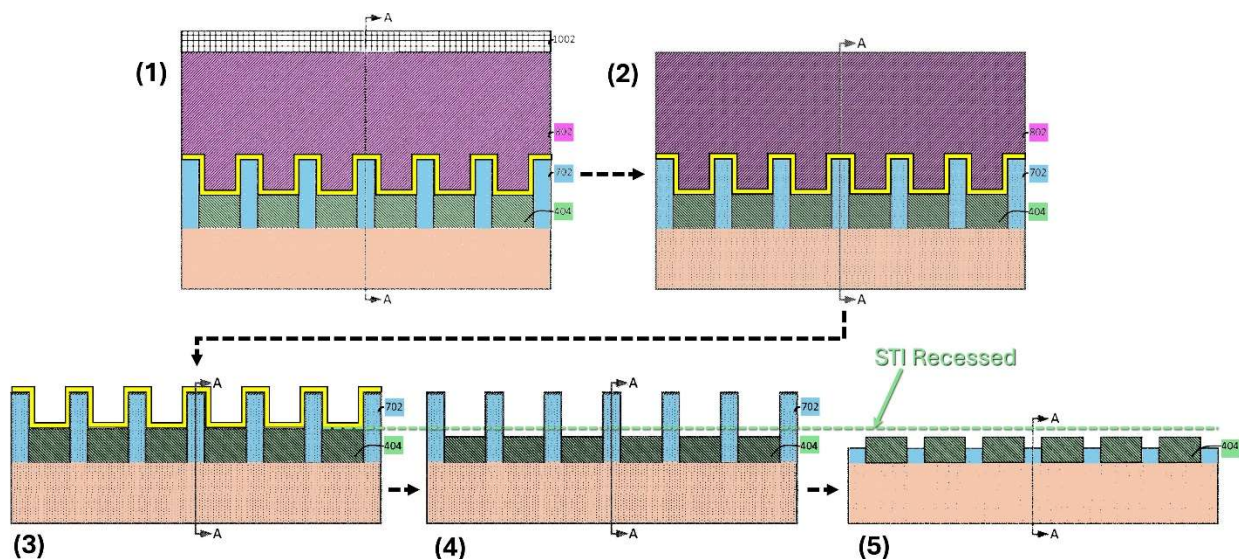


Alternative FIG. 11 (Step 1 Below)



Alternative FIG. 12 (Step 5 Below)

Etch Sequence in Region R
(Perpendicular to the A-A Cross-Section Shown Above)



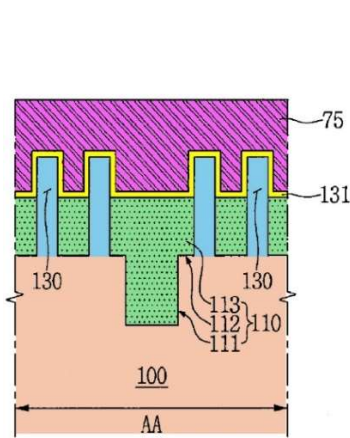
160. With Doris’s bulk silicon arrangement (see Doris ¶[0040], ¶[0043]), the etching sequence would appear as shown in the figures above, corresponding to how it appears in Ha. (See Ha ¶[0105], FIGS. 4C, 5C, 6C; Colinge, FIG. 2.14 & caption.)

Because Doris's "layer of oxide material" (yellow) and STI (green) are both made of silicon oxide, a person of ordinary skill in the art would have understood that—as in Ha—the exposed STI (green) "may be recessed" to some degree in order to ensure that Doris's layer of oxide material (yellow) is adequately removed. (Ha ¶[0105] ("The isolation region 110 . . . may be recessed."), FIG. 6C.)

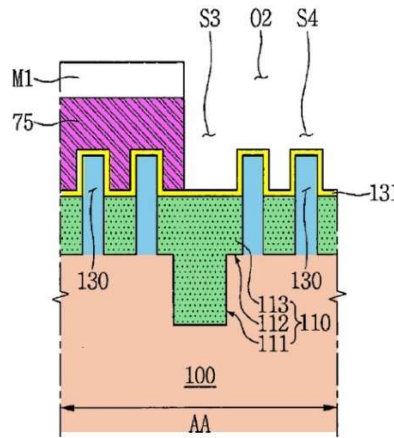
161. In the regions under mask 1102, no etching is performed. In region R, where cavity 1202 is to be formed, the exposed portion of hardmask 1002 is removed, followed by silicon layer 802 (magenta), then the "layer of oxide material" (yellow) and then part of fins 702 (blue). (Doris ¶[0047], ¶[0050], FIG. 12.) Since the STI (green) is also made of silicon oxide,¹³ a person of ordinary skill in the art would have understood that removing Doris's "layer of oxide material" (yellow) would etch part of the STI underneath (green). (Plummer at Fig. 10-23 ("Overetching of a film over a step would be required to remove material at a corner."); *see also* Plummer at 613 ("[A]ll etch processes generally employ some amount of overetching in order to ensure that the desired etching process has gone to completion. Thus underlying films are normally subjected to the etchant for some period of time toward the end of the etch period. The selectivity for the material

¹³ *See* Colinge at FIG. 2.14 ("STI oxide deposition and planarization"); Doris ¶[0043] ("[I]nsulator layer 404 may include, for example, an oxide material. . .").

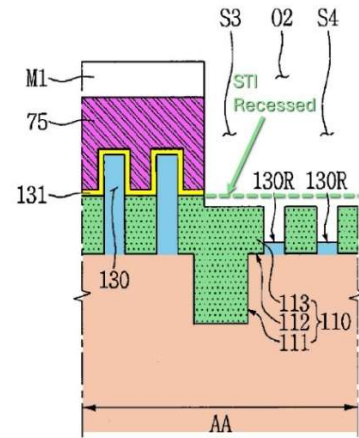
being etched . . . determines how much etching of the underlying material occurs.”),
 614 (“Some amount of overetching is normally part of every etch process.”).



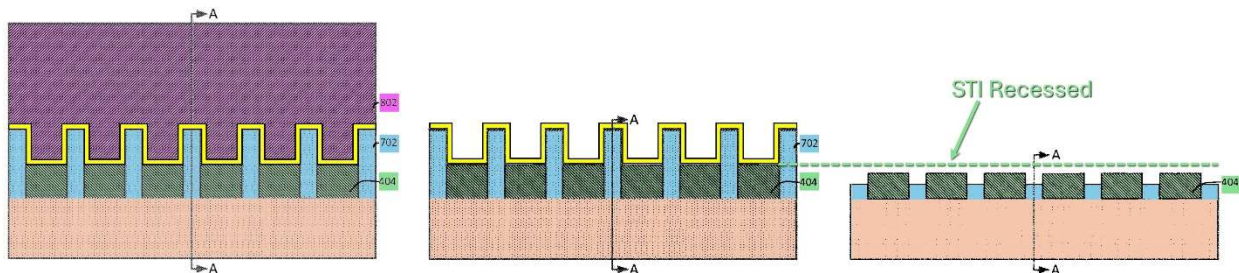
Ha, FIG. 4C



Ha, FIG. 5C



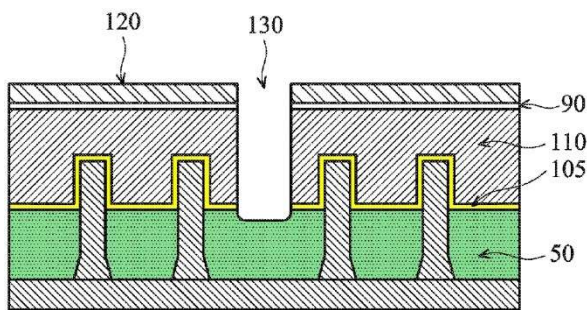
Ha, FIG. 6C (annotated)



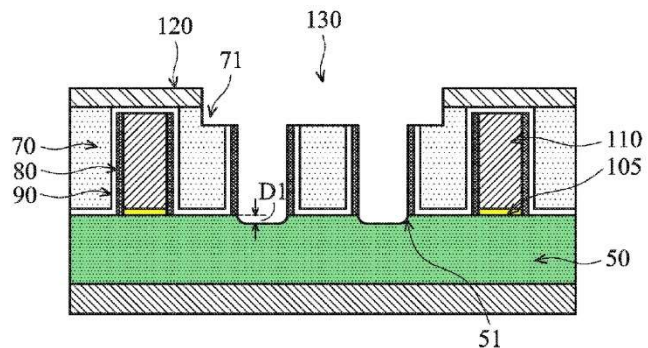
Analogous Etch Sequence in Doris's Bulk Silicon Embodiment

162. A person of ordinary skill in the art would have understood that any etch chemistry used to remove Doris's layer of oxide material (yellow) would also remove a portion of the oxide STI (green). (Ha ¶¶[0099]-[0105] (“The isolation region 110 . . . may be recessed.”), FIGS. 5A-6C; Yu ¶[0023] (“The gate insulating layer 105 may be silicon oxide . . .”), ¶¶[0031]-[0032] (“The etching of the gate layer 110 accompanies etching the oxide layers (with different etching conditions than the poly silicon etching) including the gate insulating layer 105.”), FIGS. 6A-6B; Plummer at Fig. 10-23 & caption, 613-14.)

163. Yu further confirms that recessing the STI, as in Ha, was well-known in such an etching sequence. Like Ha and Doris, Yu discloses a silicon oxide gate insulating layer 105 (yellow) and silicon oxide isolation insulating layer 50 (green). Yu ¶[0020] (“The insulating material for the isolation insulating layer 50 is made of for example, silicon dioxide . . .”), ¶[0023] (“[A] gate insulating layer 105 and a poly silicon layer are formed over the isolation insulating layer 50 and the exposed fin structures 20 The gate insulating layer 105 may be silicon oxide . . .”). Yu explains that, when etching gate insulating layer 105, “the surface portion 51 of the isolation insulating layer 50 [is] also etched.” (Yu ¶[0032].) “The depth D1, which is an etched depth of the surface portion 51 of the isolation insulating layer 50 is in a range from about 1 nm to about 10 nm.” (Yu ¶[0032].)



Yu, FIG. 6A



Yu, FIG. 6B

164. A person of ordinary skill in the art would have been motivated to follow the same over-etching process as Ha and Yu when etching Doris’s “layer of [gate] oxide material” (Doris ¶[0047])—that is, to slightly over-etch Doris’s layer of gate oxide material so as to remove part of the STI underneath in order to ensure that

the gate oxide material is adequately removed, especially over the non-planar fin structure. (See Ha ¶¶[0104]-[0105] (“The isolation region 110 . . . may be recessed.”), FIG. 6C; Yu ¶¶[0031]-[0032] (“During the oxide etching, the upper portion 71 of the ILD 70 and the surface portion 51 of the isolation insulating layer 50 are also etched . . .”), FIGS. 6A-6B; Plummer at Fig. 10-23 (“Overetching of a film over a step would be required to remove material at a corner.”), 613 (“[A]ll etch processes generally employ some amount of overetching in order to ensure that the desired etching process has gone to completion. Thus underlying films are normally subjected to the etchant for some period of time toward the end of the etch period. The selectivity for the material being etched . . . determines how much etching of the underlying material occurs.”), 614 (“Some amount of overetching is normally part of every etch process.”).) As these materials I have cited confirm, it would have been obvious to do this to ensure adequate removal of Doris’s layer of gate oxide material over the fin to allow for the subsequent fin etching. (See Doris ¶[0047].)

165. A person of ordinary skill in the art would have understood that doing this in Doris would remove part of the underlying silicon oxide STI because, like Doris’s oxide gate layer, it is made of silicon oxide and is therefore vulnerable to the same etchants. (Doris ¶[0043] (“[T]he insulator layer 404 may include, for example, an oxide material.”), ¶[0047] (“In an alternate embodiment, a layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 and insulator

layer 404 prior to depositing the α -Si layer 802.”); Ha ¶[0067] (“The trench insulation material 113 may include, for example, silicon oxide.”).)

166. I have been told that if there’s a known technique to address a known problem using prior art elements according to their established functions, then there is a motivation to combine. Here, the technique to address the problem of adequately removing a film, especially one formed over a stepped geometry, is to over-etch. (Plummer at 613-614, Fig. 10-23 & caption.) And when the film being removed is the same type of material as the underlying film. The known result would be partial removal of the underlying film. (*See* Plummer at 613 (The selectivity for the material being etched . . . determines how much etching of the underlying material occurs.”).) It is therefore my opinion that a person of ordinary skill in the art would have had a motivation to combine Ha’s disclosure of over-etching and recessed STI with Doris’s process of removing “a layer of oxide material (not shown) . . . deposited over . . . the fins 702 and insulator layer 404 [i.e., STI for a bulk silicon arrangement].” (Doris ¶[0047]; *see also* Doris ¶[0043].)

167. A person of ordinary skill in the art would have had a reasonable expectation of success when doing this because it would not have been expected to affect any other steps in Doris’s process flow or to materially affect the final device. For example, the resulting cavity 1202 still would be filled with dielectric material. (Doris ¶[0051].) A person of ordinary skill in the art would have recognized that

replacing the recessed portion of the STI with that insulator material would have had no effect on the rest of the process.

168. Additionally, routine experimentation would readily identify the proper timing of the SiO₂ etch used to remove Doris's oxide gate layer, ensuring its adequate removal and resulting in a slight amount of over-etch into the silicon oxide STI underneath. (See Ha ¶¶[0104]-[0105] ("The isolation region 110 . . . may be recessed."), FIGS. 6A-6C; Yu ¶¶[0031]-[0032] ("During the oxide etching, the upper portion 71 of the ILD 70 and the surface portion 51 of the isolation insulating layer 50 are also etched, as shown in FIGS. 6A and 6B."), FIGS. 6A-6B; Plummer at 613-14, Fig. 10-23 ("Overetching of a film over a step would be required to remove material at a corner.")) Indeed, a person of ordinary skill in the art would have found it obvious that, to ensure adequate removal of Doris's oxide gate layer, some removal of the STI underneath would be appropriate and expected because the two structures are both made of silicon oxide.

169. Applying the legal standards explained to me, as summarized above in Section IV.B, it is my opinion that a person of ordinary skill in the art would have viewed the partial removal of Doris's STI layer described above as an obvious example of the following: (1) using a known technique (over-etching, as in Ha) to improve similar methods or products in the same way; (2) performing routine experimentation (to select a suitable etch recipe that completely removes the oxide

gate layer from over the fins), with a reasonable expectation of success; and (3) a teaching, suggestion, or motivation in the prior art (*see* Ha ¶¶[0104]-[0105], FIGS. 6A-6C; Yu ¶¶[0031]-[0032], FIGS. 6A-6B) that would have led a person of ordinary skill in the art to arrive at the claimed invention.

2. Independent Claim 1

a. [1pre]: “[a] method for fabricating semiconductor device”

170. In my opinion, Ground 1A renders obvious [1pre].

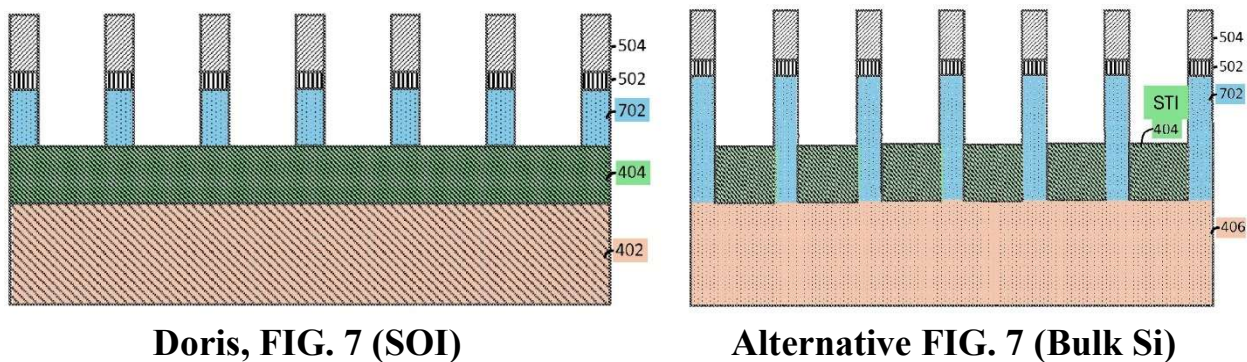
171. Specifically, Doris describes “a method for fabricating a field effect transistor device.” (Doris ¶[0004]; *see also* Ha ¶[0005] (describing “a method of fabricating semiconductor devices including a gate core and a fin active core”).)

b. [1a]: “forming a fin-shaped structure on a substrate”

172. In my opinion, Ground 1A renders obvious [1a].

173. Doris describes “the fabrication of fins 702 with the patterned hardmask layer 504 and oxide layer 502 using an etching process such as, for example, a reactive ion etch (RIE) process.” (Doris ¶[0046], FIGS. 5-7; *see also* Ha ¶¶[0091]-[0092] (“Referring to FIGS. 3A to 3C, the method of fabricating the semiconductor device in accordance with some embodiments of the inventive concept may include providing a substrate 100 including a field area FA and an active area AA, forming an isolation region 110 which defines a fin active region 130 on the substrate 100 . . .”), FIGS. 3A-3C.)

174. Although Doris’s FIGS. 4-17 depict an embodiment that uses an SOI substrate with buried insulator layer 404, Doris expressly states that the same process flow may be applied to a bulk silicon substrate instead. (Doris ¶[0040] (“The substrate 101 may include, a *bulk silicon substrate*, a silicon on insulator substrate or a SiGe on insulator substrate.”), ¶[0043] (“The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however alternate exemplary embodiments may include a *bulk silicon*, a bulk SiGe arrangement or a SiGe on insulator arrangement.”).) As explained above, such an embodiment would involve etching fins (blue) on a bulk silicon wafer (peach), as shown on the right below. (See Section IX.A.1.a-b; Colinge at 65-66, Fig. 2.14.)

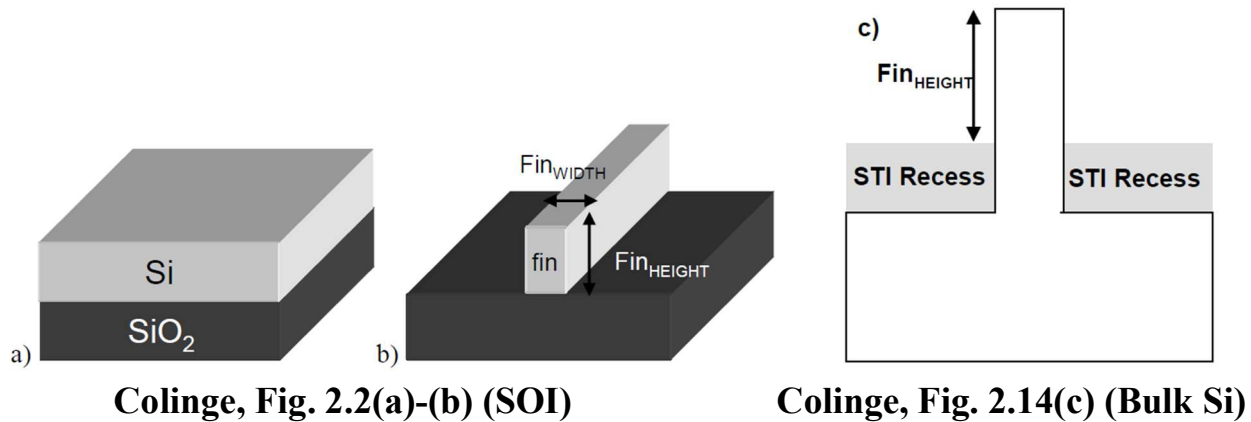
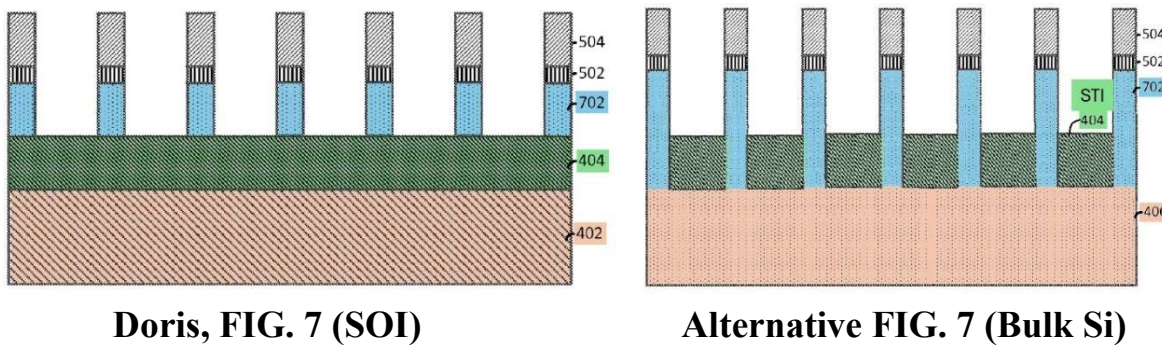


c. [1b]: “forming a shallow trench isolation (STI) around the fin-shaped structure”

175. In my opinion, Ground 1A renders obvious [1b].

176. Doris’s “illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement,” such that “[a]n insulator layer 404 is arranged on the substrate 402, where the insulator layer 404 may include, for example, an oxide

material.” (Doris ¶[0043].) But Doris also discloses that “alternate exemplary embodiments may include a bulk silicon . . . arrangement.” (Doris ¶[0043].) My analysis of Ground 1A centers on Doris’s disclosed (but not pictured) bulk silicon arrangement, as I show on the right below. (*See* Section IX.A.1.a-b above; Colinge at 65-66, FIG. 2.14.)



177. A person of ordinary skill in the art would have understood—as a matter of textbook knowledge—that Doris’s “bulk silicon . . . arrangement” (Doris ¶[0043]) involves “STI oxide deposition and planarization,” followed by “STI oxide recess to expose silicon fin with desired FinHEIGHT.” (Colinge, Fig. 2.14 & caption.) This would form a shallow trench isolation (“STI”) oxide (in

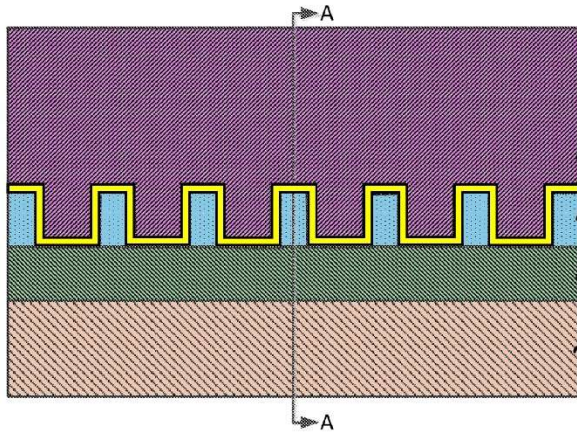
green above) around the fins (in blue above), as shown in the alternative bulk silicon version of Doris's FIG. 7, rather than having a buried oxide layer under the fins, as Doris's original FIG. 7 shows. (*See* Colinge at Fig. 2.2(a)-(b) and Fig. 2.14.)

d. [1c]: "forming a gate layer on the fin-shaped structure and the STI"

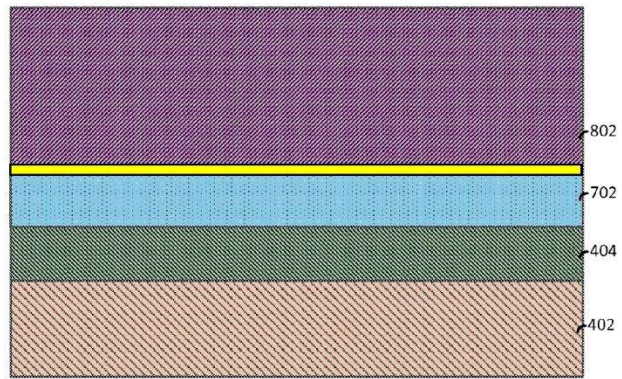
178. In my opinion, Ground 1A renders obvious [1c].

179. Doris discloses "the deposition of an amorphous silicon (α -Si) layer 802 over the fins 702 and exposed portions of the insulator layer 404." (Doris ¶[0047]; *see also* Doris at FIGS. 8-9; Ha ¶[0091] ("forming sacrificial gate patterns 71 to 76"), FIGS. 3A-3C.) Silicon layer 802 is later patterned into "dummy gate stacks 1502" and is thus a gate layer. (Doris ¶[0053] ("dummy gate stacks 1502"), FIG. 16.)

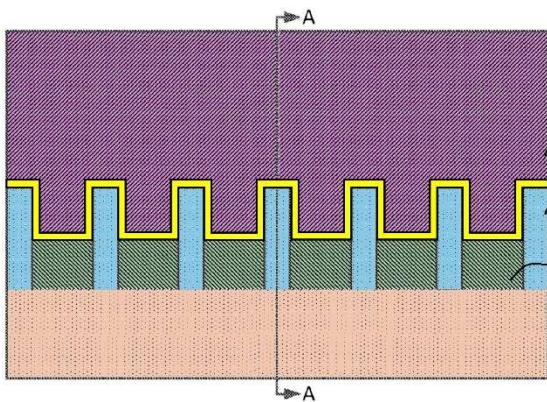
180. Doris additionally explains that "a layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802." (Doris ¶[0047]; *see also* Ha ¶[0091] ("forming a base insulating layer 131 on surfaces of the fin active region 130 and the isolation region 110"), FIGS. 3A-3C.) The "not shown" layer has been added below in yellow for completeness.



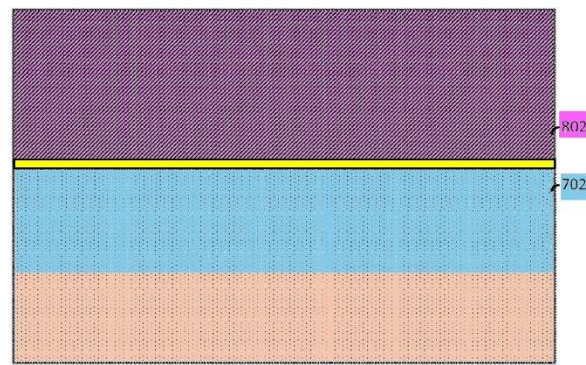
Doris, FIG. 8 (yellow oxide added)



Doris, FIG. 9 (A-A, yellow oxide added)



Alternative FIG. 8 (Bulk Si)



Alternative FIG. 9 (A-A Bulk Si)

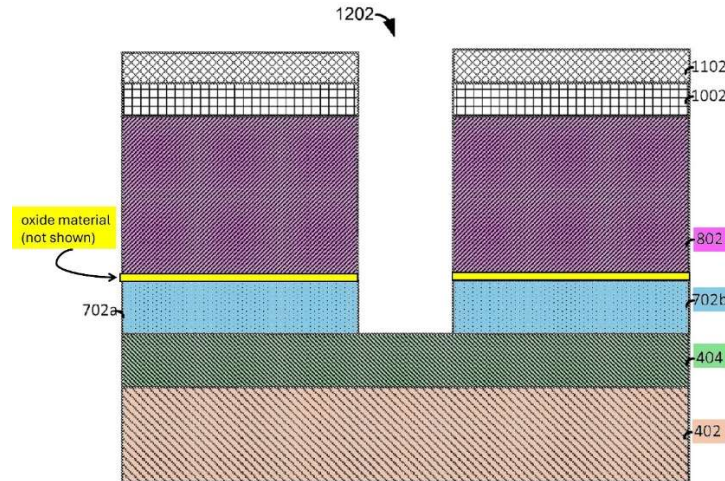
181. Doris's FIG. 8 looks down the fins running into the page, and Doris's FIG. 9 shows the A–A cross-section of FIG. 8, with the fins running right/left. (Doris ¶[0047].) The alternative versions of Doris's FIGS. 8 and 9 shown above illustrate Doris's "bulk silicon . . . arrangement." (Doris ¶[0043]; *see also* Section IX.A.1.a-b above.) As the alternative figures above show for Doris's bulk silicon arrangement, silicon layer 802 (magenta) is a gate layer formed on fins 702 (blue) and the STI (green). (Doris ¶[0047].)

e. **[1d]: “removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench”**

182. In my opinion, Ground 1A renders obvious [1d].

183. Doris discloses “formation of a hardmask layer 1002 over the α -Si layer 802,” “formation of a mask 1102 that is lithographically patterned over the hardmask layer 1002,” and “an etching process . . . that removes exposed portions of the hardmask 1002, exposed portions of the α -Si layer 802, and the fins 702.” (Doris ¶¶[0048]-[0050]; *see also* Doris at FIGS. 10-12; Ha ¶¶[0099]-[0105] (“[T]he method may include forming a fin active recess 130R by removing the base insulating layer 131 exposed in the fin active cut space S4 and recessing the fin active region 130. The isolation region 110 . . . may be recessed.”), FIGS. 5A-6C.)

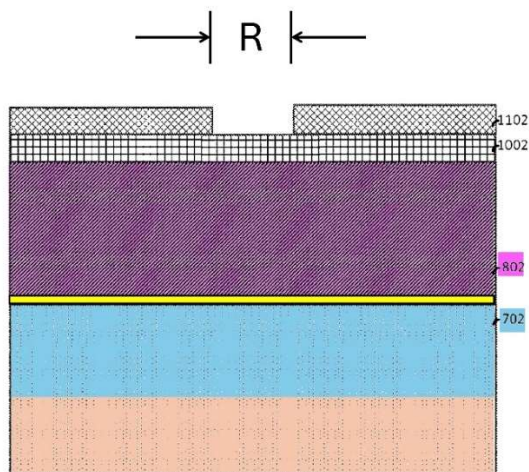
184. As Doris’s FIG. 12 shows below, a cavity 1202 is created by etching the pattern of mask 1102 first into hardmask 1002, then into silicon layer 802 (magenta), then into the “layer of oxide material” (yellow) (*see* Doris ¶[0047]), and finally into fins 702 (blue). (Doris ¶[0050] (“FIG. 12 illustrates the resultant structure following an etching process . . . that removes . . . exposed portions of the α -Si layer 802, and the fins 702 [to create] a cavity 1202.”). This process cuts fins 702 into two segments. (Doris ¶[0050] (“[W]hen the fins 102 are etched or cut into segments 702a and 702b”).)



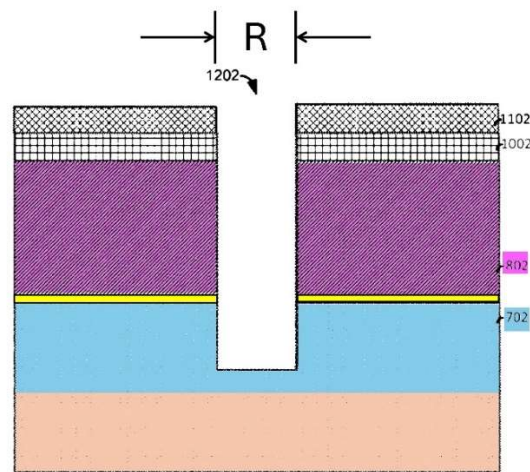
Doris, FIG. 12 (yellow gate oxide added)

185. Doris thus discloses removing part of the gate layer (layer 802) and fin-shaped structure (fins 702) to form a trench (cavity 1202).

186. Whether using an SOI or bulk silicon substrate, a person of ordinary skill in the art would have found it obvious that forming this trench (cavity 1202) further involves removing part of the isolation oxide (buried oxide or STI). (See Section IX.A.1.c above; Ha ¶[0105] (“The isolation region 110 ... may be recessed.”), FIGS. 5A-6C.) The figures below depict the etch sequence in Region R.

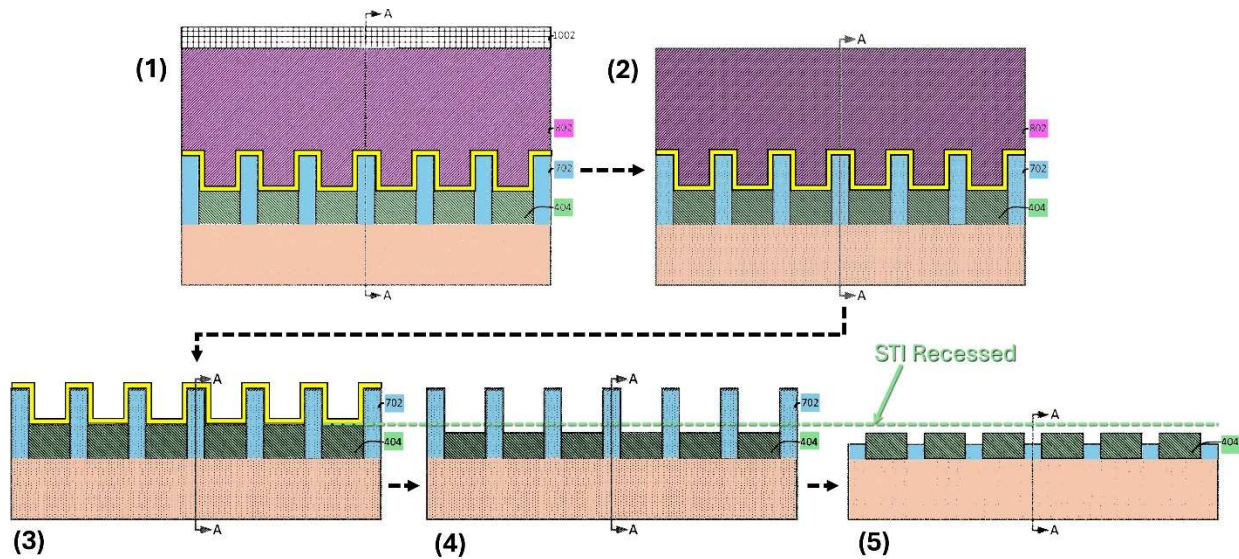


Alternative FIG. 11 (Step 1)



Alternative FIG. 12 (Step 5)

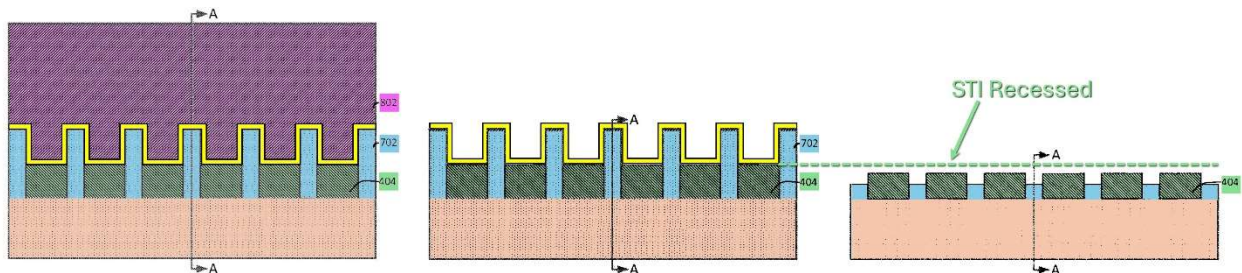
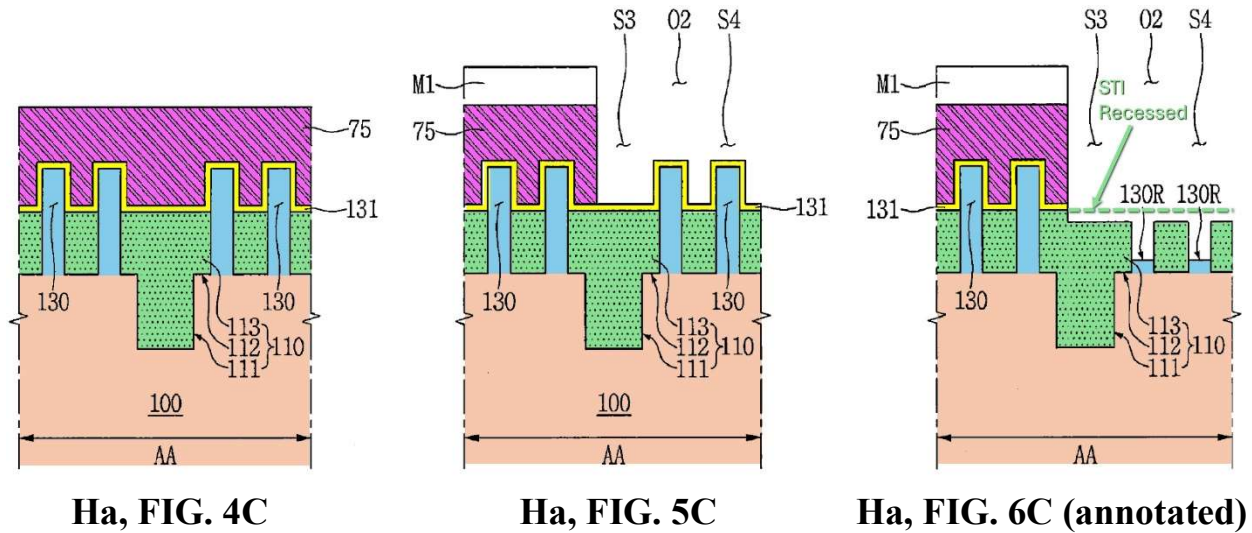
Etch Sequence in Region R



187. Outside Region R, nothing is etched. Inside Region R, as shown above, the etch proceeds as Ha discloses—by removing the gate layer (magenta), the gate oxide (yellow), a portion of the STI (green), and a portion of the fins (blue). (See Ha ¶¶[0099]-[0105], FIGS. 5A-6C.)

188. Like Doris, Ha discloses “forming a first mask pattern M1” and “removing portions of the . . . gate pattern[] [75]” (magenta). (Ha ¶¶[0099], FIG. 5C.) Ha also discloses “forming a fin active recess 130R by . . . recessing the fin active region 130” (blue), and that “isolation region 110 [green] . . . may be recessed.” (Ha ¶¶[0104]-[0105]; *see also* Yu ¶¶[0031]-[0032] (“During the oxide etching, the upper portion 71 of the ILD 70 and the surface portion 51 of the isolation insulating layer 50 are also etched, as shown in FIGS. 6A and 6B.”), FIGS. 6A-6B.) The figures

below show this sequence both for Ha and for Doris's disclosed bulk silicon arrangement. (See Section IX.A.1.c above.)



189. As I explain in Section IX.A.1.c, a person of ordinary skill in the art would have found it obvious (as taught by Ha and Yu, for example) that when removing Doris's gate oxide layer, some portion of the STI would be removed as well. This is because Doris's gate oxide layer (yellow) and the STI layer (green) are in direct contact, and both are made of silicon oxide. (See Section IX.A.1.c above; Colinge at Fig. 2.14 ("STI oxide"); Doris ¶[0043] ("insulator layer 404 may include, for example, an oxide material"), ¶[0047] ("[A] layer of oxide material (not shown)"))

may be deposited over . . . insulator layer 404”); Ha ¶[0105] (“The isolation region . . . may be recessed.”), FIG. 6C; Yu ¶[0032] (“During the oxide etching, . . . isolation insulating layer 50 [is] also etched”), FIGS. 6A-6B.)

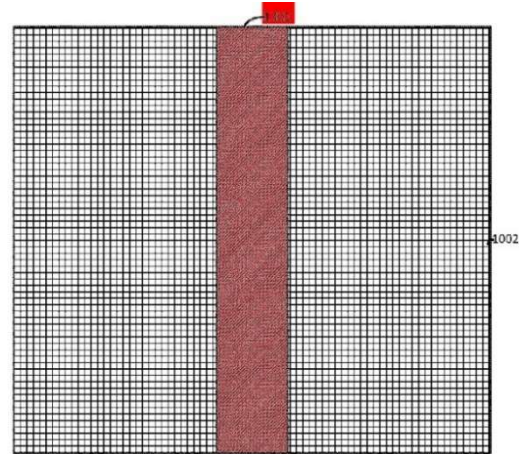
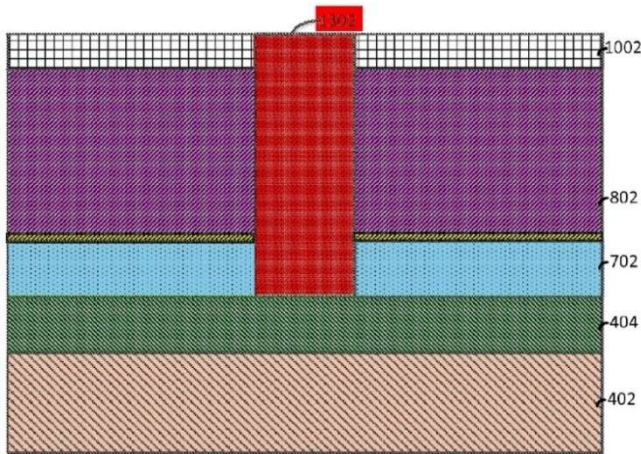
190. Accordingly, it is my opinion that a person of ordinary skill in the art would have found it obvious under the Ground 1A to remove part of the STI (green) when forming the trench (cavity 1202).

f. [1e]: “forming a dielectric layer into the trench to form a single diffusion break (SDB) structure”

191. In my opinion, Ground 1A renders obvious [1e].

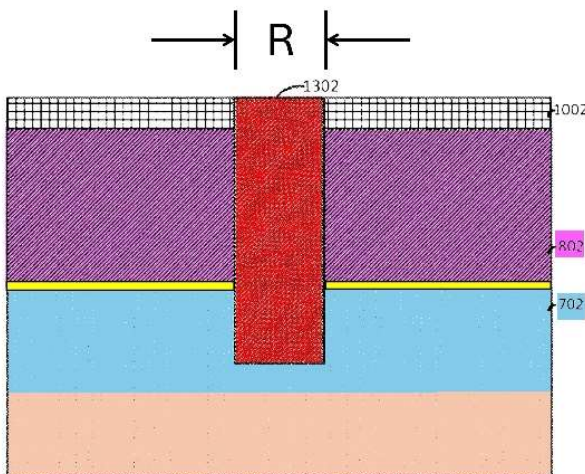
192. Doris explains that cavity 1202 “cut[s]” the fins. (Doris ¶[0050] (“[T]he fins 102 are etched or cut into segments 702a and 702b”).) Doris further discloses “the deposition of an insulator material 1302 in the cavity 1202.” (Doris ¶[0051]; *see also* Doris at FIG. 13; Ha ¶¶[0106]-[0111] (“forming an insulating core layer 90 which completely or partially fills . . . the fin active recess 130R”), FIGS. 7A-9C.)

193. Doris’s FIG. 13 below illustrates this processing step in cross-section, with the fins running horizontally, and Doris’s FIG. 14 below shows this step from above, illustrating the shape of cavity 1202, which is filled with insulator material 1302. (Doris ¶[0051] (“FIG. 13 illustrates the resultant structure following the deposition of an insulator material 1302 in the cavity 1202 (of FIG. 12) such as, for example an oxide or a nitride material.”).)

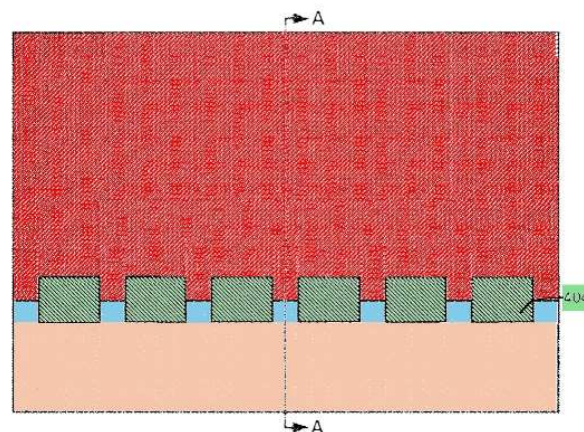


Doris, FIG. 13 (Cross-Section) Doris, FIG. 14 (Plan View)

194. In Doris's bulk silicon arrangement (Doris ¶[0043]), the cross-section for this step would appear as below, with cavity 1202 filled by insulator 1302. (See Sections IX.A.1.c and §IX.A.2.e above; Doris ¶[0051] ("FIG. 13 illustrates the resultant structure following the deposition of an insulator material 1302 in the cavity 1202 (of FIG. 12) such as, for example an oxide or a nitride material.")) The plan view would be identical to FIG. 14, with the insulator in cavity 1202.

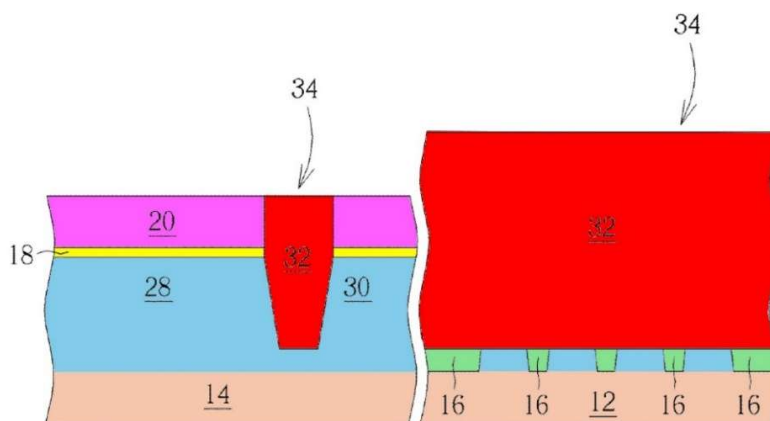


A-A Cross-Section



Inside Region R

195. The result of this process is an SDB structure like the one the '880 Patent describes in FIG. 6 (below).¹⁴ (See '880 Patent at 3:39-59, FIG. 6.) Thus, Ground 1A renders obvious forming a dielectric layer (Doris's insulator material 1302) into the trench (Doris's cavity 1202) to form an SDB structure.



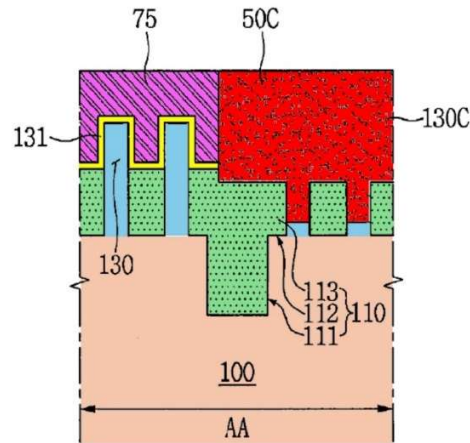
'880 Patent, FIG. 6^[15]

196. Ha's FIG. 9C below, analogous to the ones above from the '880 Patent and for Doris's bulk silicon embodiment, confirms the trench would be filled with a dielectric layer and planarized to form "a single diffusion break (SDB) structure." (Ha ¶[0129] ("[A] single diffusion break (SDB) structure can implemented");

¹⁴ Like the SDB structure in the '880 Patent, and characteristic of any SDB structure, Doris's SDB structure (i.e., insulator material 1302) separates the fins and sits directly adjacent to "[a]ctive regions" 1706 (i.e., source/drain regions) in the final structure, not directly next to dummy gates. (See Doris ¶[0054], FIG. 17; '880 Patent at 4:39-44, FIG. 10; *see also* Section §VI.C above (describing diffusion breaks.)

¹⁵ Dielectric layer 32 on the right is drawn too high. Its upper surface should be coplanar with the upper surface of gate layer 20. (See '880 Patent at 3:44-48 ("[T]he top surface of the remaining dielectric layer 32 is even with the top surface of the gate layer 20."), FIG. 4.) My color annotations to FIG. 6 above are based on the structures as shown in FIG. 2 of the '880 Patent.

see also Ha ¶¶[0106]-[0111] (“[T]he method may include forming silicon oxide, removing the first mask pattern M1 and exposing the sacrificial gate patterns 71 to 76 by performing a planarization process . . .”), FIGS. 7A-9C.)

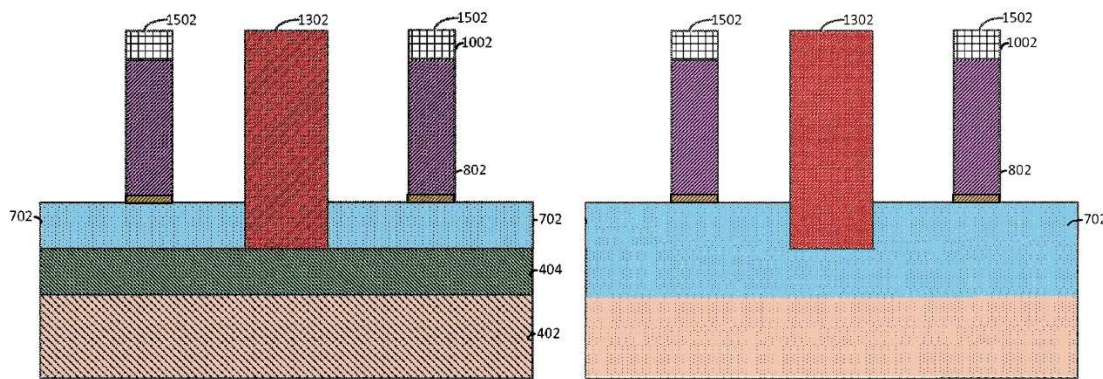


Ha, FIG. 9C

g. [1f]: “after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure”

197. In my opinion, Ground 1A renders obvious [1f].

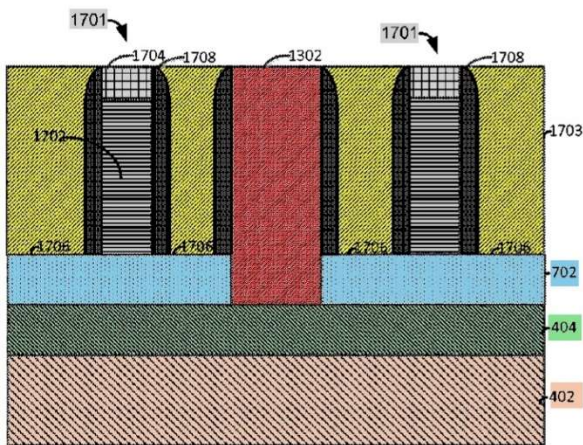
198. After the step in Doris’s process flow I describe in the preceding subsection, Doris discloses a process for patterning and etching dummy gate structures, as shown below. (See Doris ¶¶[0052]-[0053], FIG. 16.)



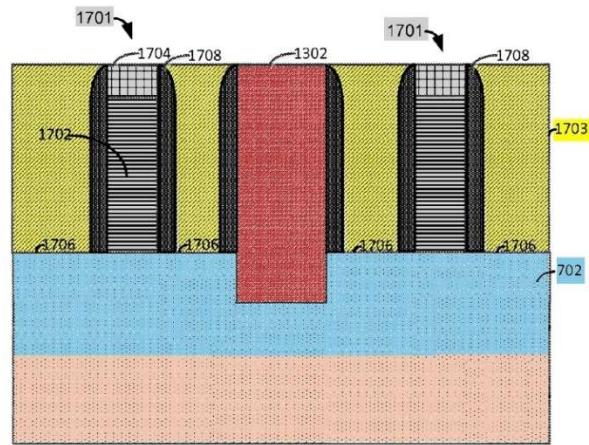
Doris, FIG. 16

Alternative FIG. 16 (Bulk Si)

199. Doris then discloses forming “[a] layer of insulator material 1703 such as, for example, an oxide material . . . over exposed portions of the insulator layer 404, the fins 702 and adjacent to the gate stacks 1701.” (Doris ¶[0054].) As FIG. 17 shows below, insulator material 1703 (yellow) is coplanar with insulator material 1302 (SDB structure). (Doris at FIG. 17.) The same would be true for Doris’s bulk silicon arrangement, shown below on the right, which would follow the same insulator material deposition process. (Doris ¶[0040] (“The substrate 101 may include, *a bulk silicon substrate*, a silicon on insulator substrate or a SiGe on insulator substrate.”), ¶[0043] (“The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however alternate exemplary embodiments may include a *bulk silicon*, a bulk SiGe arrangement or a SiGe on insulator arrangement.”)).



Doris, FIG. 17



Alternative FIG. 17 (Bulk Si)

200. A person of ordinary skill in the art would have understood how to make such a coplanar structure, as Ha shows, for example. Ha describes “forming a

first interlayer insulating layer 171 [ILD] between the sacrificial gate patterns.” (Ha ¶[0096]; *see also* Yu ¶[0026] (“Further, an interlayer dielectric layer (ILD) 70 is formed in spaces between the gate layers 110 with the side-wall insulating layers 80 and the CESL 90 and over the gate layer 110.”).) It is accomplished by “forming silicon oxide to cover the sacrificial gate patterns,” “fill[ing] gaps between the sacrificial gate patterns,” and “performing a planarization process such as a chemical mechanical polishing (CMP) process or an etch-back process.” (Ha ¶[0098]; *see also* Ha at FIGS. 3A-4C; Yu ¶¶[0026]-[0027] (“Planarization operations, such as an etch-back process and/or a chemical mechanical polishing (CMP) process, are performed, so as to obtain the structure shown in FIGS. 4A-4D.”), FIG. 4D.)

201. In the context of Doris’s FIG. 17, a person of ordinary skill in the art would have understood, or at least found it obvious, to follow the same basic process flow Ha describes: “forming [insulator material 1703] to cover the [dummy gate stacks 1502 and insulator material 1302] and fill gaps between the[m],” then “performing a planarization process” so that insulator material 1703, dummy gate stacks 1502, and insulator material 1302 are coplanar. (Ha ¶[0098]; *see also* Yu ¶¶[0026]-[0027]; Xie616 at 8:49-53; Xie790 ¶[0023].) Then, “[t]he dummy gate stacks 1502 are removed and replaced by the gate stacks 1701,” as FIG. 17 shows above. (Doris ¶[0054].) Thus, as Doris’s FIG. 17 indicates, Ground 1A renders

obvious forming an ILD layer (Doris's insulator material 1703) on the SDB structure (Doris's insulator material 1302 in cavity 1202) after forming the SDB structure.

3. Claim 2: “The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.”

202. Claim 2 depends from claim 1. I understand that means claim 2 requires all the same features as claim 1, plus the additional features recited in claim 2. Ground 1A renders obvious the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

203. In my opinion, Ground 1A also renders claim 2 obvious.

204. Doris discloses forming a gate dielectric layer on fins 702 before forming silicon layer 802 (the gate layer). Doris explains that “a layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802.” (Doris ¶[0047].) This layer of oxide material (a dielectric) not shown in Doris's figures is a gate dielectric layer because it lies on top of the fins under silicon layer 802 (the gate layer) and is thus located in the position of a FinFET gate dielectric. (See Section IX.A.2.d above (depicting Doris's layer of oxide material in yellow); Doris ¶[0047].)

- 4. Claim 3: “The method of claim 2, further comprising: forming a patterned mask on the gate layer; and using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.”**

205. Claim 3 depends from claim 2. I understand that means claim 3 requires all the same features as claim 2, plus the additional features recited in claim 3. Ground 1A renders obvious all the features recited in claim 2 for the reasons I provide in Sections IX.A.1-3 above.

206. In my opinion, Ground 1A also renders claim 3 obvious.

207. For the reasons I explain in Section IX.A.2.e above, Ground 1A renders obvious forming a patterned mask (mask 1102 and/or hardmask 1002) on the gate layer (silicon layer 802) and then removing part of the gate layer, part of the gate dielectric layer (Doris’s “layer of oxide material (not shown),” Doris ¶[0047]), and part of the fin-shaped structure (fins 702) to form the trench (cavity 1202). (*See* Section IX.A.2.e above; Doris ¶¶[0048]-[0050], FIGS. 10-12.) Thus, in my opinion, Ground 1A satisfies claim 3.

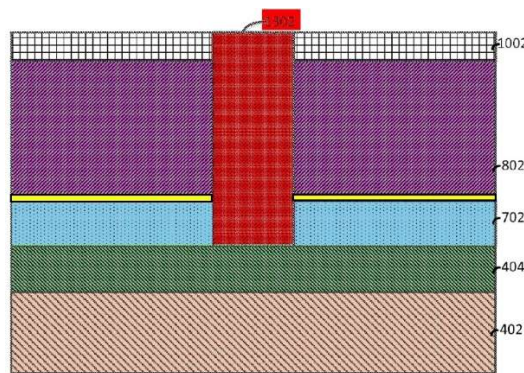
- 5. Claim 4: “The method of claim 1, further comprising: forming the dielectric layer into the trench and on the gate layer; and planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.”**

208. Claim 4 depends from claim 1. I understand that means claim 4 requires all the same features as claim 1, plus the additional features recited in claim 4.

Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

209. In my opinion, Ground 1A also renders claim 4 obvious.

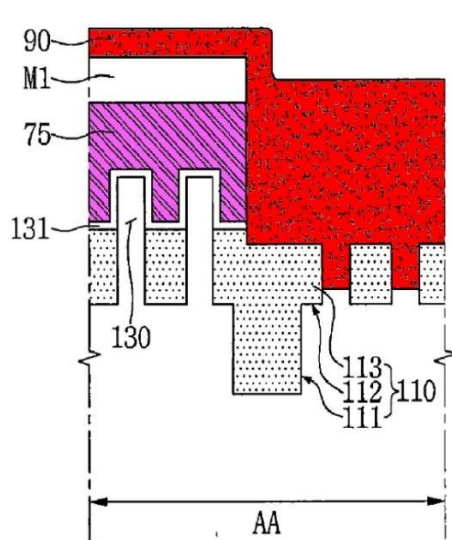
210. Doris discloses that insulator material 1302 (red) would be coplanar with hardmask 1002 (see FIG. 13 below). A person of ordinary skill in the art would have understood this requires over-filling cavity 1202 with insulator material 1302, such that it also forms on hardmask 1002, and then performing planarization to remove the insulator material 1302 from hardmask 1002.¹⁶



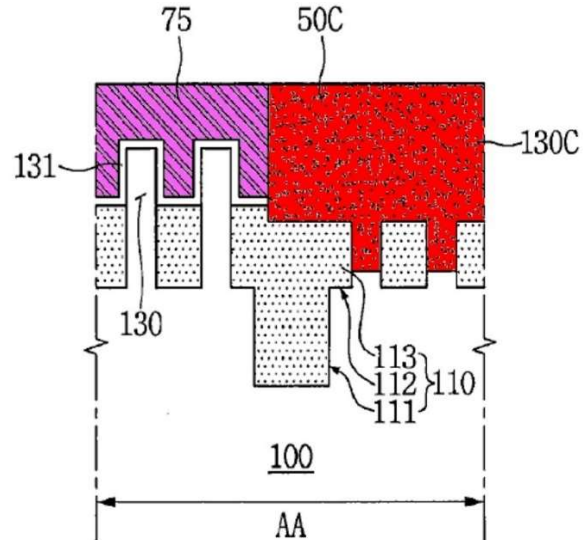
Doris, FIG. 13

¹⁶ See Zhao at 8:9-16 (“First, a layer of insulating material 123, such as silicon dioxide, was formed across the substrate 102 so as to overfill the trenches 124 and the cavities 122. Thereafter, a CMP process operation was performed to planarize the upper surface of the layer of insulating material 123 using the gate cap layer 112 as a polish-stop.”), FIGS. 2L-2M; Yu ¶¶[0036]-[0037] (“After the opening 130 is filled by the thin filling insulating layer 140 and the thick filling insulating layer 150, a planarization operation such as a CMP process is performed to expose the upper surface of the gate layers 110, as shown in FIGS. 8A and 8B.”), FIGS. 7A-8B; Ha ¶[0106] (“[T]he method may include forming an insulating core layer 90 which completely or partially fills the first and second field gate cut spaces S1 and S2, the fin gate cut space S3, the fin active cut space S4, and the fin active recess 130R.”), FIGS. 7A-7C.

211. A person of ordinary skill in the art would have found it obvious to perform an additional planarization step to remove hardmask 1002, leaving Doris's insulator material 1302 (red) coplanar with silicon layer 802 (magenta). A person of ordinary skill in the art would have found this to be a routine design choice, as Ha discloses. (See Ha ¶¶[0108]-[0111] ("Upper surfaces of the remaining sacrificial gate patterns 71 to 76 ... and the fin active core 130C may be coplanar."), FIGS. 7A-9C.)



Ha, FIG. 7C



Ha, FIG. 9C

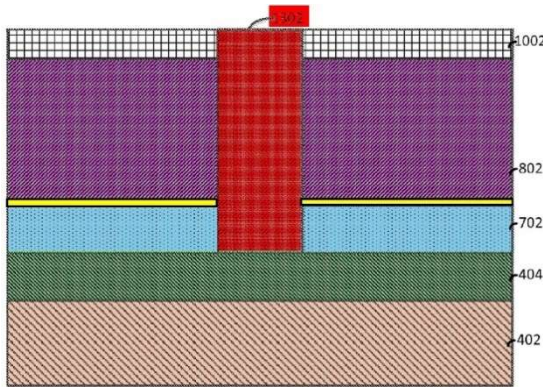
212. As figures 7C and 9C above illustrate, Ha discloses filling the SDB trench with "an insulating core layer 90" that "may be formed semi-conformally" to additionally cover sacrificial gate layer 75. (Ha ¶[0106].) Ha then discloses "removing [the] portions of the core layer 90 formed on the first mask pattern M1" and "removing the first mask pattern M1 and exposing the sacrificial gate patterns 71 to 76 by performing a planarization process." (Ha ¶¶[0109]-[0110].) As a result,

“the remaining sacrificial gate patterns 71 to 76 . . . and the fin active core 130C may be coplanar,” as shown on the right below. (Ha ¶[0111].) Once dummy gate patterns 71 to 76 have been exposed in this way, they can be replaced using a replacement metal gate process. (See Ha ¶¶[0112]-[0115], FIGS. 10A-11C; Section VI.D above.)

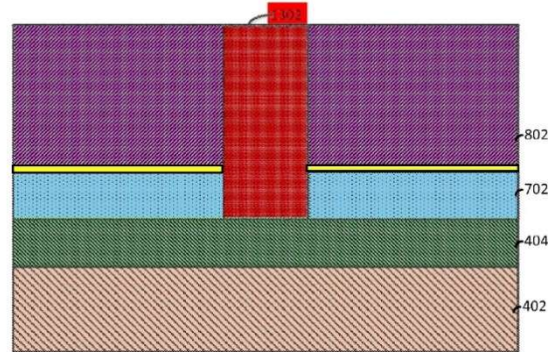
213. Like Ha, Doris discloses that a typical replacement metal gate process may be performed to replace its dummy gate stacks 1502 with gate stacks 1701 comprising “a dielectric layer and a gate metal layer 1702.” (Doris ¶[0054].) This would necessarily involve removing hardmask 1002. (See Doris ¶[0053] (“[H]ardmask layer 1002 [is] removed when the dummy gate stacks 1502 are formed.”).) For example, Doris explains that hardmask 1002 may be removed before patterning the dummy gate stacks. (See Doris ¶[0052] (“[H]ardmask layer 1002 may be replaced with another hardmask layer that is suitable for patterning.”).)

214. To remove hardmask 1002 in accordance with Doris’s disclosure, a person of ordinary skill in the art would have been motivated simply to perform additional planarization, as Ha discloses (illustrated below) by further planarizing the structure in Doris’s FIG. 13 to be level with silicon layer 802 (magenta). (See Ha ¶¶[0108]-[0111] (“[T]he method may include forming silicon oxide, removing the first mask pattern M1 and exposing the sacrificial gate patterns 71 to 76 by performing a planarization process such as a CMP process. Upper surfaces

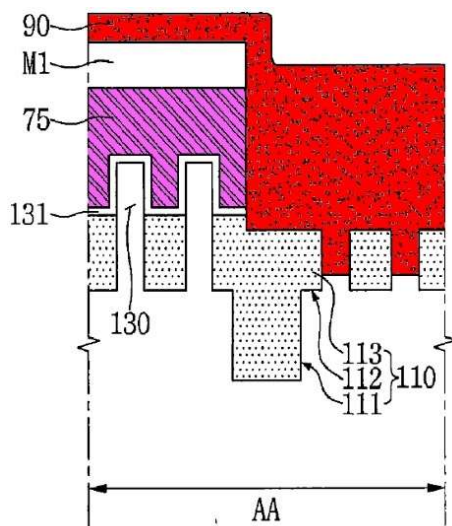
of the remaining sacrificial gate patterns 71 to 76 . . . and the fin active core 130C may be coplanar.”), FIGS. 7A-9C.)



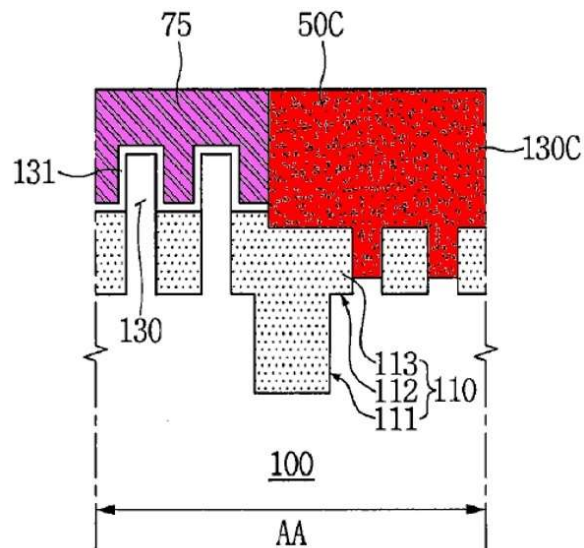
Doris, FIG. 13



Alternative, FIG. 13



Ha, FIG. 7C



Ha, FIG. 9C

215. More references, in addition to Ha, also disclose such a polishing step. Zhao, for example, also discloses “one or more planarization processes” to “remove the gate cap layer . . . and ultimately expose the sacrificial gate material” for the purpose of forming a replacement metal gate. (Zhao at 8:26-34; *see also* Zhao at 8:9-16, 8:35-49, FIGS. 2L-2M.) Yu and Xie⁶¹⁶ each disclose the same. (*See* Yu

¶[0037] (“[A] CMP process is performed to expose the upper surface of the gate layers 110, as shown in FIGS. 8A and 8B. In other words, the gate layers 110 function as a stopper for the CMP process.”); *see also* Yu ¶¶[0036]-[0039], FIGS. 7A-8B; Xie616 at 11:44-55 (disclosing “one or more CMP process operations . . . to effectively expose the upper surface of the sacrificial gate electrodes” by “remov[ing] . . . gate cap layers 112 and . . . portions of the [SDB] layers of material 142 [and] 140” to facilitate “the replacement gate process”), FIGS. 2P-2Q.)

216. I have been told that if there is a known technique to address a known problem using prior art elements according to their established functions, then there is a motivation to combine. Here, the problem is how in particular to remove a hard mask like Doris’s hard mask 1002. And, as I explain above, the known technique for doing this was to perform a planarization step, such as chemical-mechanical polishing (“CMP”), according to its established function. A person of ordinary skill in the art thus would have been motivated to remove Doris’s hardmask 1002 (which Doris discloses) by performing planarization, such as CMP. The ordinary and expected result would be coplanar SDB and gate layers.

217. A person of ordinary skill in the art would have reasonably expected to succeed at this because Ha’s and Doris’s respective structures may be made from identical materials. Like Ha’s sacrificial gate layer 75, Doris’s layer 802 is made of

silicon.¹⁷ Like Ha's mask M1, Doris's hardmask 1002 may be made of silicon nitride.¹⁸ And like Ha's fin active core 130C, Doris's insulating material 1302 may be made of silicon nitride.¹⁹ Thus, a person of ordinary skill in the art would have found it obvious to apply Ha's "CMP process" (i.e., chemical-mechanical polishing) (Ha ¶[0111]) to Doris's structure in FIG. 13 to remove hard mask 1002. (*See* Doris ¶[0052] ("[T]he hardmask layer 1002 may be replaced with another hardmask layer that is suitable for patterning.").)

218. A person of ordinary skill in the art also would have understood that Ha's CMP process is consistent with Doris's disclosures. As I explain above, Doris's hardmask 1002 must be removed before the replacement gate process can be performed. (*See* Doris ¶¶[0052]-[0054] ("The dummy gate stacks 1502 are removed and replaced by the gate stacks 1701.").) This is why Ha discloses using a CMP process to planarize its analogous dummy gate layer 75 and SDB structure 130C. (*See* Ha ¶¶[0108]-[0115], FIGS. 10A-11C.) Thus, a person of ordinary skill in the art would have understood that performing Ha's CMP planarization step facilitates

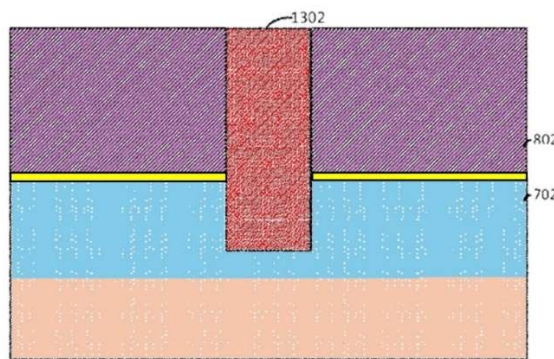
¹⁷ *See* Doris ¶[0047] ("amorphous silicon" or "polysilicon"); Ha ¶[0095] ("polycrystalline silicon").

¹⁸ *See* Doris ¶[0048] ("silicon nitride"); Ha ¶[0095] ("silicon oxide, silicon nitride, or spin on hardmask (SOH)").

¹⁹ *See* Doris ¶[0051] ("an oxide or a nitride material"); Ha ¶[0072] ("for example, silicon nitride").

Doris's disclosed goal of creating a replacement metal gate stack. (See Doris ¶[0054], FIG. 17.)

219. Thus, in my opinion, a person of ordinary skill in the art would have found it obvious to remove Doris's hardmask layer 1002 using Ha's CMP planarization process, thereby making Doris's insulator material 1302 and silicon layer 802 coplanar.



Alternative FIG. 13 (Hardmask 1002 Removed, Bulk Si)

220. Applying the legal standards explained to me, as summarized above in Section IV.B, it is my opinion that a person of ordinary skill in the art would have viewed this as an obvious example of the following: (1) combining prior art elements according to known methods (Ha's CMP process) to yield predictable results; (2) using a known technique (Ha's CMP process) to improve similar methods in the same way; (3) choosing from among a finite number of identified, predictable solutions (either Ha's CMP process or a selective etch), with a reasonable expectation of success; and (4) a teaching, suggestion, or motivation in the prior art (see Doris ¶¶[0052]-[0054], FIG. 13; Ha ¶¶[0110]-[0115], FIGS. 7A-9C; Zhao at

8:9-49, FIGS. 2L-2M; Yu ¶¶[0036]-[0039], FIGS. 7A-8B) that would have led a person of ordinary skill in the art to arrive at the claimed invention.

221. Accordingly, in my opinion, Ground 1A renders obvious forming the dielectric layer (Doris's insulator material 1302) into the trench (Doris's cavity 1202) and on the gate layer (Doris's silicon layer 802) and planarizing the dielectric layer (using Ha's CMP process, for example) so that the top surfaces of the dielectric layer and the gate layer are coplanar, as in alternative FIG. 13 above.

6. Claim 5: "The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure."

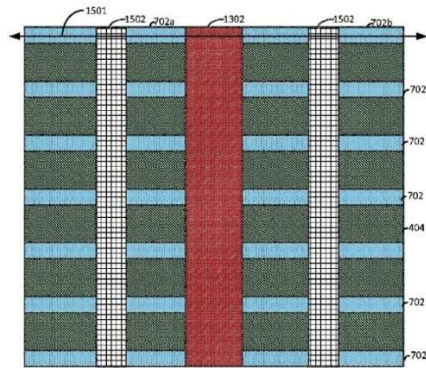
222. Claim 5 depends from claim 1. I understand that means claim 5 requires all the same features as claim 1, plus the additional features recited in claim 5. Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

223. In my opinion, Ground 1A also renders claim 5 obvious.

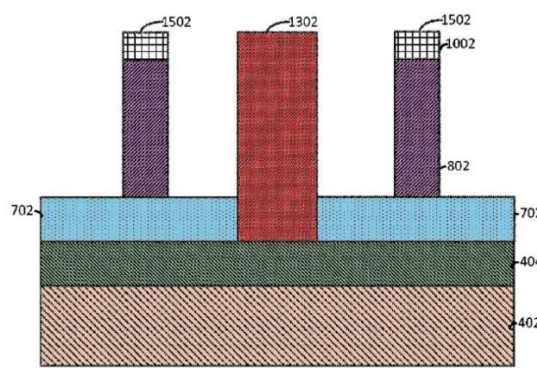
224. Doris discloses "the patterning and etching of portions of the hardmask layer 1002 and the α -Si layer 802 to define dummy gate stacks 1502" that "define channel regions of the fins 702." (Doris ¶[0052]; *see also* Doris ¶[0053], FIGS. 15-16.) In other words, Doris discloses removing part of the gate layer (silicon layer 802) after forming the SDB structure (cavity 1202 filled with insulator material 1302) to form a gate structure (dummy gate stacks 1502) adjacent to the

SDB structure. This is done “using a suitable lithographic patterning and etching process.” (Doris ¶[0052].)

225. Doris’s FIG. 16 below on the right shows this processing step in cross-section, with the fins running horizontally. Doris’s FIG. 15 below on the left shows this step from above. (Doris ¶¶[0052]-[0053] (“FIG. 16 illustrates a side cut-away view of the dummy gate stacks 1502 on the fins 702 and the insulator material 1302 arranged between the fins 702.”).)

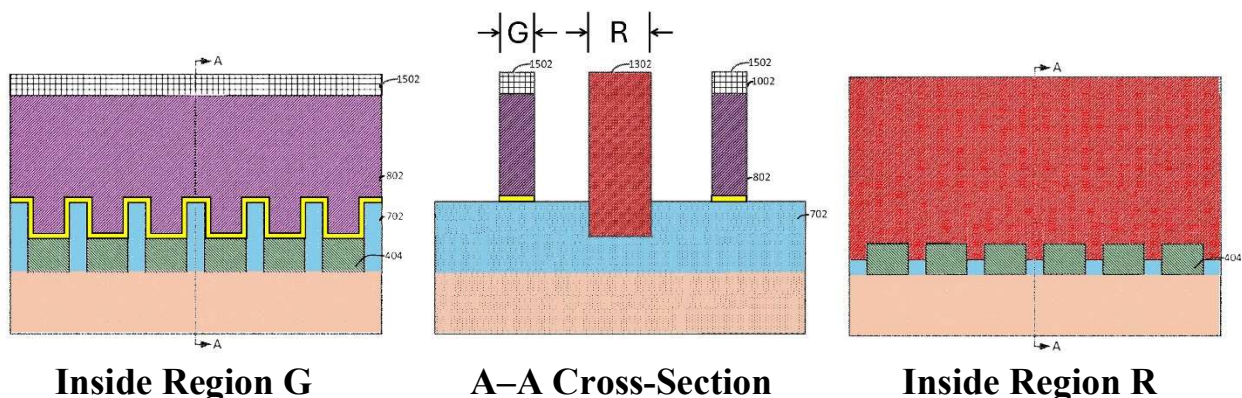


Doris, FIG. 15



Doris, FIG. 16

226. In Doris’s disclosed bulk silicon arrangement (Doris ¶[0043]), the cross-sections for this step would appear as below. (See Sections IX.A.1.c and IX.A.2.f above.) The plan view would be identical to FIG. 15.



Inside Region G

A-A Cross-Section

Inside Region R

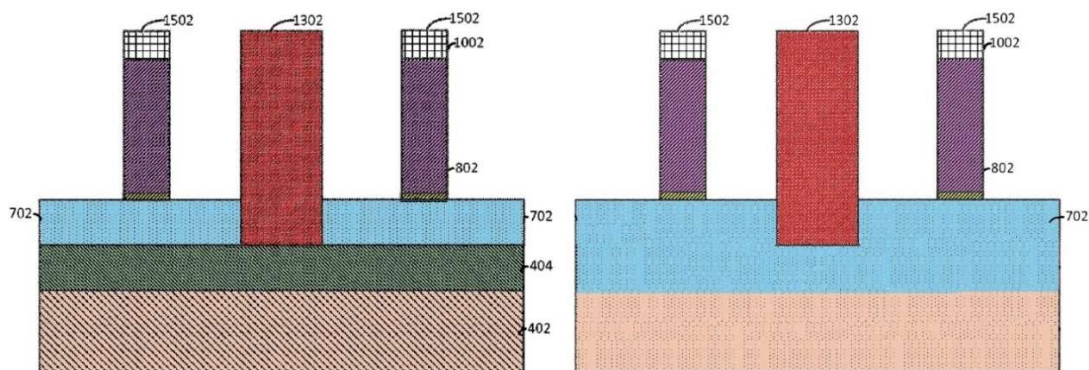
227. Accordingly, Ground 1A renders obvious removing part of the gate layer (silicon layer 802) after forming the SDB structure (cavity 1202 filled with insulator material 1302) to form a gate structure (dummy gate stacks 1502) adjacent to the SDB structure.

7. Claim 6: “The method of claim 5, further comprising: forming a cap layer on the gate structure and the SDB structure; and removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer adjacent to the SDB structure.”

228. Claim 6 depends from claim 5. I understand that means claim 6 requires all the same features as claim 5, plus the additional features recited in claim 6. Ground 1A renders obvious all the features recited in claim 5 for the reasons I provide in Sections IX.A.1-2 and IX.A.6 above.

229. In my opinion, Ground 1A also renders claim 6 obvious.

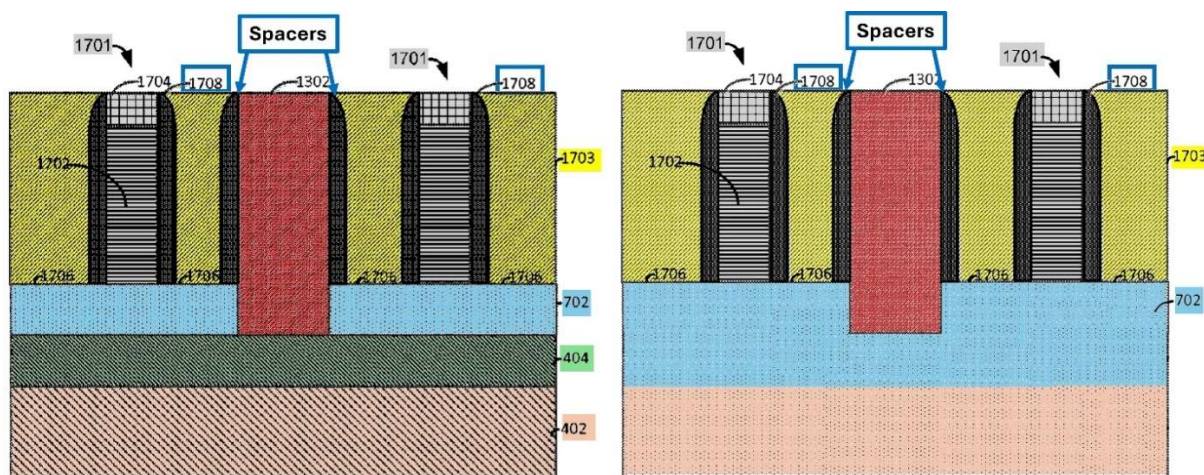
230. Doris discloses the “formation of spacers 1708 [circled below in dark blue] . . . adjacent to the dummy gate stacks 1502.” (Doris ¶[0054]; *see also* Doris at FIGS. 16-17.)



Doris, FIG. 16 (SOI)

Alternative FIG. 16 (Bulk Si)

Then, after forming insulator material 1703 (yellow, *see* Section IX.A.2.g above), “[t]he dummy gate stacks 1502 are removed and replaced by the gate stacks 1701,” as shown below. (Doris ¶[0054].)

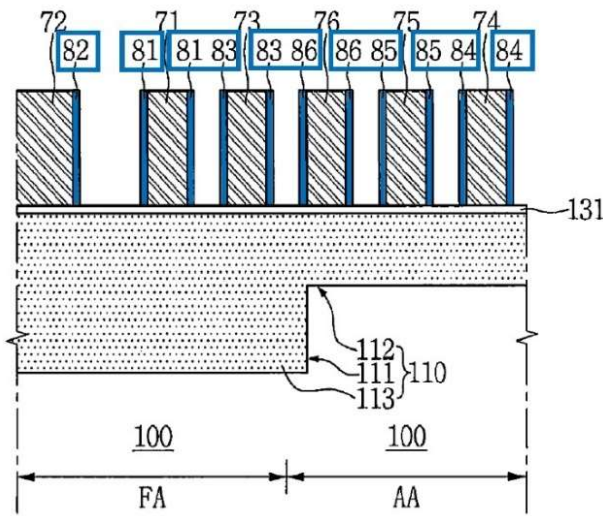


Doris, FIG. 17 (SOI, annotated)

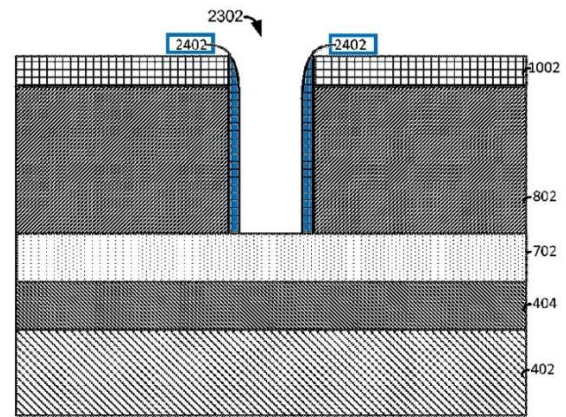
Alternative FIG. 17 (Bulk Si)

231. A person of ordinary skill in the art would have readily understood how to make spacers 1708 using the same textbook method for forming spacers that had been taught to semiconductor processing students for decades. (*See* Wolf³ at 595-96, FIG. 9-31(d); Quirk at 212, FIG. 9.16.) First, a layer of insulating material is conformally deposited over the protruding structures (i.e., Doris’s dummy gate stacks 1502 and insulation material 1302), and then an anisotropic etch is performed to remove the deposited material from the horizontal surfaces, leaving vertical spacers on the sidewalls of the protruding structures. (*See* Quirk at 212 (“Sidewall spacer formation requires two major process steps (see Figure 9.16). First, an oxide layer is deposited across the surface of the wafer, then the oxide is etched back using a dry etch process.”), FIG. 9.16.)

232. For example, Ha discloses the same textbook procedure for forming its analogous spacers 81-86: “The forming of the gate spacers 81 to 86 may include forming a silicon nitride layer by performing an ALD process, and then performing an etch-back process.” (Ha ¶[0095], FIGS. 3A-3C.) And Doris itself describes the same textbook procedure in another context: “The spacers 2402 [of FIG. 24] may be formed by, for example, depositing a nitride material . . . and performing a RIE process” (Doris ¶[0060], FIG. 24.) The figures below illustrate these examples.



Ha, FIG. 3B



Doris, FIG. 24

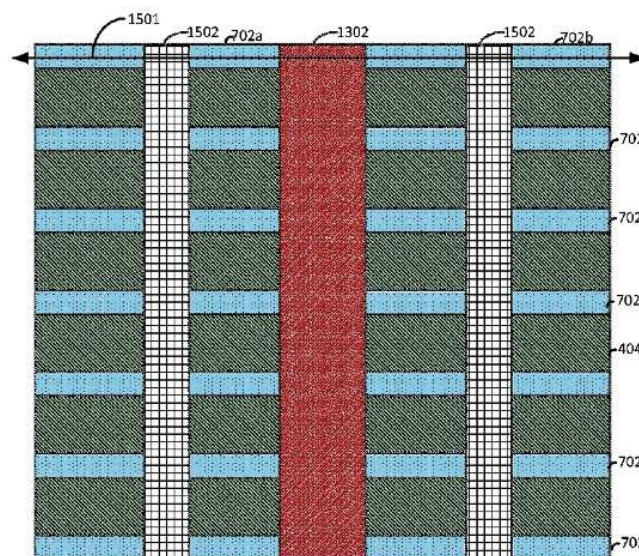
233. Thus, in my opinion, Ground 1A renders obvious forming a cap layer on the gate structure (dummy gate stacks 1502) and the SDB structure (insulating material 1302 filled into cavity 1202) and removing part of the cap layer to form a first spacer (spacers 1708) adjacent to the gate structure and a second spacer (labeled “Spacers” in annotated FIG. 17 above) adjacent to the SDB structure.

8. Claim 7: “The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.”

234. Claim 7 depends from claim 1. I understand that means claim 7 requires all the same features as claim 1, plus the additional features recited in claim 7. Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

235. In my opinion, Ground 1A also renders claim 7 obvious.

236. Doris explains that the fin-shaped structure (any of the fins 702, blue) is disposed extending along a first direction (horizontal), and the SDB structure (insulator material 1302, red) is disposed extending along a second direction (vertical), as Doris’s FIG. 15 below illustrates. (Doris ¶[0052] (“FIG. 15 illustrates a top view of the resultant structure The fins 702a and 702b are arranged along a common longitudinal axis shown by the arrow 1501.”), FIG. 15.)



Doris, FIG. 15

9. Claim 8: “The method of claim 7, wherein the first direction is orthogonal to the second direction.”

237. Claim 8 depends from claim 7. I understand that means claim 8 requires all the same features as claim 7, plus the additional features recited in claim 8. Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 and IX.A.8 above.

238. In my opinion, Ground 1A also renders claim 8 obvious. As I explain in the subsection immediately above, the first direction (horizontal) is orthogonal to the second direction (vertical). (*See* Section IX.A.8 above; Doris at FIG. 15.)

10. Claim 9: “The method of claim 1, wherein the gate layer comprises amorphous silicon.”

239. Claim 9 depends from claim 1. I understand that means claim 9 requires all the same features as claim 1, plus the additional features recited in claim 9. Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

240. In my opinion, Ground 1A also renders claim 9 obvious. Doris discloses “the deposition of an amorphous silicon (α -Si) layer 802 over the fins 702.” (Doris ¶[0047].) Thus, the gate layer (layer 802) comprises amorphous silicon.

11. Claim 10: “The method of claim 1, wherein the gate layer comprises polysilicon.”

241. Claim 10 depends from claim 1. I understand that means claim 10 requires all the same features as claim 1, plus the additional features recited in

claim 10. Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

242. In my opinion, Ground 1A also renders 10 obvious.

243. While Doris discloses “the deposition of an amorphous silicon (α -Si) layer 802 over the fins 702,” Doris also refers to layer 802 as “the α -Si (*polysilicon*) layer 802.” (Doris ¶[0047] (emphasis added).) Accordingly, Doris discloses that the gate layer (layer 802) may also be composed of polysilicon, a known substitute for amorphous silicon in this context. (See Shieh ¶[0013] (“The dummy gate structure 220 includes a dummy gate layer 221, such as polysilicon, amorphous silicon or other appropriate materials.”); Zhao at 6:36-42 (“In general, . . . the sacrificial gate electrode material 110B is comprised of a material such as polysilicon or amorphous silicon”); Section IX.D below.)

12. Claim 11: “The method of claim 1, wherein the dielectric layer comprises silicon nitride.”

244. Claim 11 depends from claim 1. I understand that means claim 11 requires all the same features as claim 1, plus the additional features recited in claim 11. Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

245. In my opinion, Ground 1A also renders 11 obvious.

246. Doris discloses “the deposition of an insulator material 1302 in the cavity 1202 (of FIG. 12) such as, for example . . . a nitride material.”

(Doris ¶[0051].) Although not necessarily limited to *silicon* nitride, a person of ordinary skill in the art would have understood that to be, by far, the most obvious choice of “nitride material” in this context. This is a convention in the field of Si semiconductor processing. (See Xie078 ¶[0032] (“The gate separation structure 114 may be comprised of a variety of materials, e.g., silicon dioxide, silicon nitride, etc.”); Yu ¶[0036] (explaining “insulating layer 150 is made of silicon oxide or silicon nitride based materials”); Ha ¶[0107] (explaining “core layer 90 may include, for example, silicon nitride”); Zhao, 8:10-13 (disclosing “a layer of insulating material 123, such as silicon dioxide”); Shieh ¶[0030] (“The isolation feature 275 is formed by filling in isolation trench 260 with dielectric materials such as silicon oxide, silicon nitride, or silicon oxynitride.”).)

247. Accordingly, Ground 1A renders obvious, and render obvious, that the dielectric layer (insulator material 1302) comprises silicon nitride.

13. Claim 12: “The method of claim 1, wherein the dielectric layer comprises silicon oxide.”

248. Claim 12 depends from claim 1. I understand that means claim 12 requires all the same features as claim 1, plus the additional features recited in claim 12. Ground 1A renders obvious all the features recited in claim 1 for the reasons I provide in Sections IX.A.1-2 above.

249. In my opinion, Ground 1A also renders 12 obvious.

250. Doris discloses “the deposition of an insulator material 1302 in the cavity 1202 (of FIG. 12) such as, for example an oxide ... material.” (Doris ¶[0051].) Although not necessarily limited to *silicon* oxide, a person of ordinary skill in the art would have understood that to be, by far, the most obvious choice of “oxide material” in this context. This is a convention in the field of Si semiconductor processing. (See Xie078 ¶[0032] (“The gate separation structure 114 may be comprised of a variety of materials, e.g., silicon dioxide, silicon nitride, etc.”); Yu ¶[0036] (explaining “insulating layer 150 is made of silicon oxide or silicon nitride based materials”); Ha ¶[0107] (explaining “core layer 90 may include, for example, silicon nitride”); Zhao, 8:10-13 (disclosing “a layer of insulating material 123, such as silicon dioxide”); Shieh ¶[0030] (“The isolation feature 275 is formed by filling in isolation trench 260 with dielectric materials such as silicon oxide, silicon nitride, or silicon oxynitride.”).)

251. Accordingly, Ground 1A renders obvious that the dielectric layer (insulator material 1302) comprises silicon oxide.

B. Ground 1B: The Combination of Doris and Ha, Further in View of Colinge, Renders Obvious Claims 1-12

252. For the same reasons I explained above in Sections IX.A.1.a-b, it is my opinion that a person of ordinary skill in the art would have found it obvious to combine the teachings in Colinge, a FinFET textbook, with the disclosures in Doris and Ha.

253. For the reasons I explain above in Sections IX.A.2-13, it is also my opinion that a person of ordinary skill in the art would have found claims 1-12 obvious in view of the combined teachings of Doris, Ha, and Colinge.

254. While Ground 1A simply points to Colinge as evidence of what a person of ordinary skill in the art would have known at the time, Ground 1B expressly relies on Colinge itself as part of the combination. But my analysis of both combinations—which focus on how a person of ordinary skill in the art would have understood Doris’s “bulk silicon” disclosure—is the same either way. In other words, it is my opinion that a person of ordinary skill in the art already would have possessed the knowledge Colinge teaches about SOI and bulk silicon FinFETs (Ground 1A) as a matter of prior training and education. But it is also my opinion that a person of ordinary skill in the art would have found it obvious how to implement Doris’s process flow in the context of a bulk silicon FinFET by referencing Colinge specifically (Ground 1B). My analysis of claims 1-12 above would not change either way.

C. Grounds 2A and 2B: Ha Anticipates (Ground 2A) and Renders Obvious (Ground 2B) Claims 1-5, 7-8, and 10-11

1. Independent Claim 1

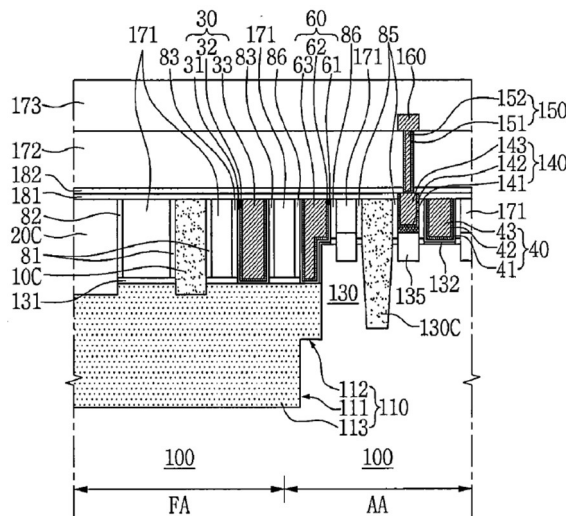
255. Ha discloses claim 1 under a broad understanding of the claims that is consistent with the Patent Owner’s apparent view. (*See* Section VII.C above.).

a. **[1pre]: “A method for fabricating semiconductor device”**

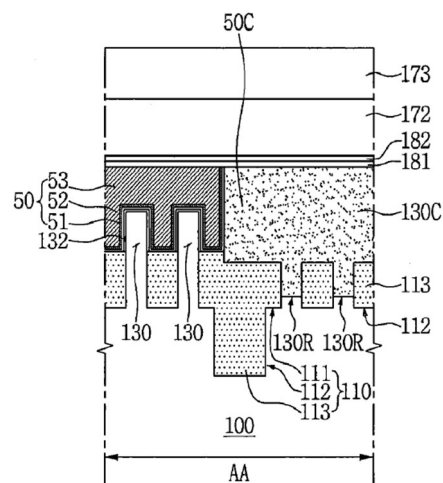
256. In my opinion, Ha discloses the preamble of claim 1 (i.e., [1pre]).

257. Ha discloses “semiconductor devices including a gate core and a fin active core and methods of fabricating the same.” (Ha ¶[0002].) Ha explains: “Some embodiments of the inventive concept provide a method of fabricating semiconductor devices including a gate core and a fin active core.” (Ha ¶[0005].)

FIGS. 2A and 2C show an exemplary semiconductor device made by Ha's method.



Ha, FIG. 2A



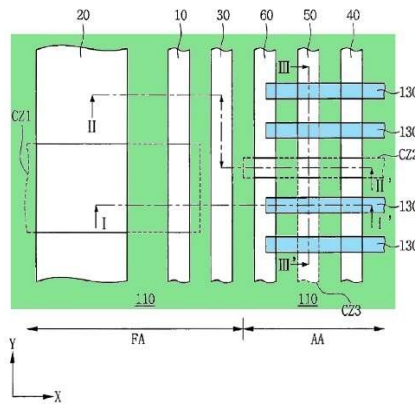
Ha, FIG. 2C

**b. [1a]: “forming a fin-shaped structure on a substrate”
[1b]: “forming a shallow trench isolation (STI) around the fin-shaped structure”**

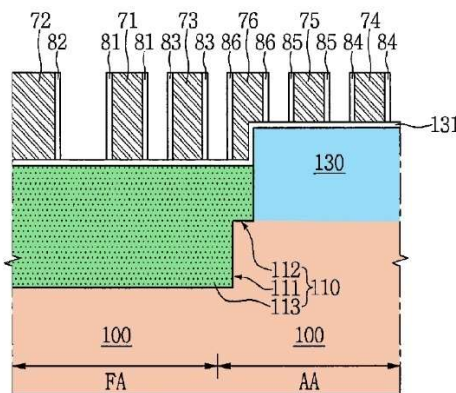
258. In my opinion, Ha discloses [1a] and [1b].

259. Ha explains that its “method of fabricating the semiconductor device . . . may include providing substrate 100 including a field area FA and an active area AA, [and] forming an isolation region 110 which defines a fin active region 130 on

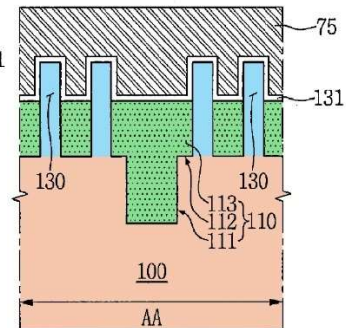
the substrate 100” (Ha ¶[0091].) As shown in the figures below,²⁰ for example, the fin active region 130 is a fin-shaped structure formed on a substrate 100.



Ha, FIG. 1



Ha, FIG. 3A



Ha, FIG. 3C

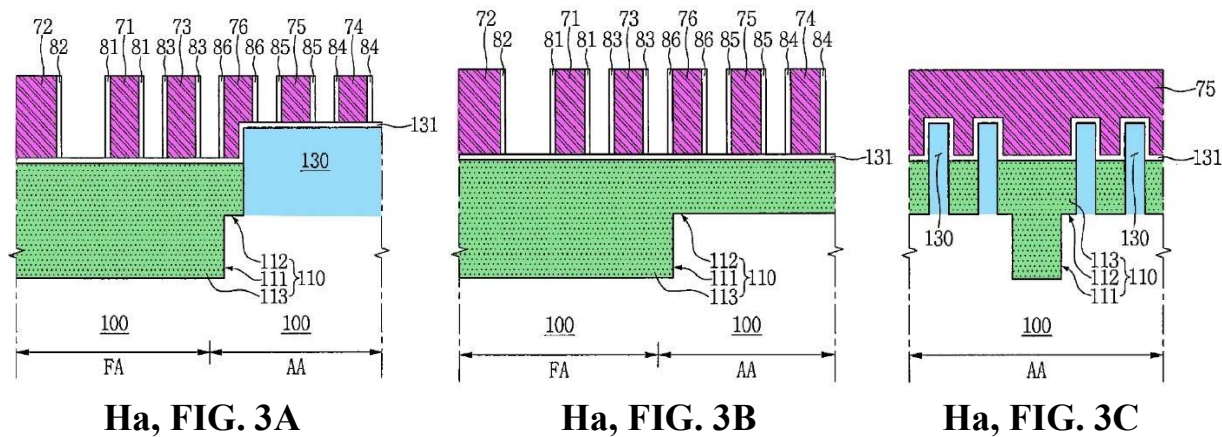
260. Ha’s substrate 100 is patterned to make trenches, including shallow trenches 112 that define active fin regions 130. That is, Ha discloses forming a active fin regions 130 (fin-shaped structures) on a substrate 100. Ha thus satisfies [1a].

261. Then, trench insulation material 113 is deposited into Ha’s trenches, including shallow trenches 112, to form isolation region 110. (Ha ¶[0093] (“The isolation region 110 may include a trench insulation material 113 which fills a deep trench 111 and a shallow trench 112.”).) Forming isolation region 110 therefore includes depositing insulation material 113 into shallow trenches 112 (i.e., forming a shallow trench isolation (STI)) around fin active regions 130 (fin-shaped structures). Ha thus satisfies [1b].

²⁰ Ha’s figure numbers that end in “A” lie along cross-section I–I’ of FIG. 1; those ending in “B” lie along cross-section II–II’; and those ending in “C” lie along cross-section III–III’. (Ha ¶¶[0043]–[0044], ¶[0090].)

c. [1c]: “forming a gate layer on the fin-shaped structure and the STI”

262. In my opinion, Ha discloses (Ground 2A), and at least renders obvious (Ground 2B), step [1c].



263. Ha’s process flow includes “forming a base insulating layer 131 on surfaces of the fin active region 130 and the isolation region 110, and forming sacrificial gate patterns 71 to 76 and gate spacers 81 to 86 on the base insulating layer 131.” (Ha ¶[0091].) Sacrificial gate patterns 71-76 include, for example, “a sacrificial first fin gate pattern 74, a sacrificial second fin gate pattern 75, and a sacrificial butting gate pattern 76,” each of which is formed on the fin active region 130 (fin-shaped structure) and insulation material 113 in shallow trenches 112 (STI), as shown in the figures above. (Ha ¶[0095]; *see also* Ha at FIGS. 3A-3C.)

264. There are three ways to consider the claimed “gate layer” in the context of Ha.

265. First, a person of ordinary skill in the art would have understood (Ground 2A), and at least found obvious (Ground 2B), that sacrificial gate patterns 71-76 are each patterned from the same initial layer (i.e., the same gate layer). (See Ha ¶[0095] (“The sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon.”).) This would be a “gate layer” as claimed, because it is the same structure the ’880 Patent describes. (See ’880 Patent at 3:3-10 (“[A] gate layer 20 [is] formed to cover the fin-shaped structures 14 and the STI 16 entirely [T]he gate layer 20 is selected from the group consisting of amorphous silicon and polysilicon.”).)

266. Second, under a broad view of the claims that is consistent a view the Patent Owner’s may advocate (*see* Section VII.C above), Ha’s sacrificial gate patterns 71 to 76 themselves could be considered a “gate layer” because they are made from the actual gate layer that was deposited. (See Ha ¶[0095] (“The sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon.”).)

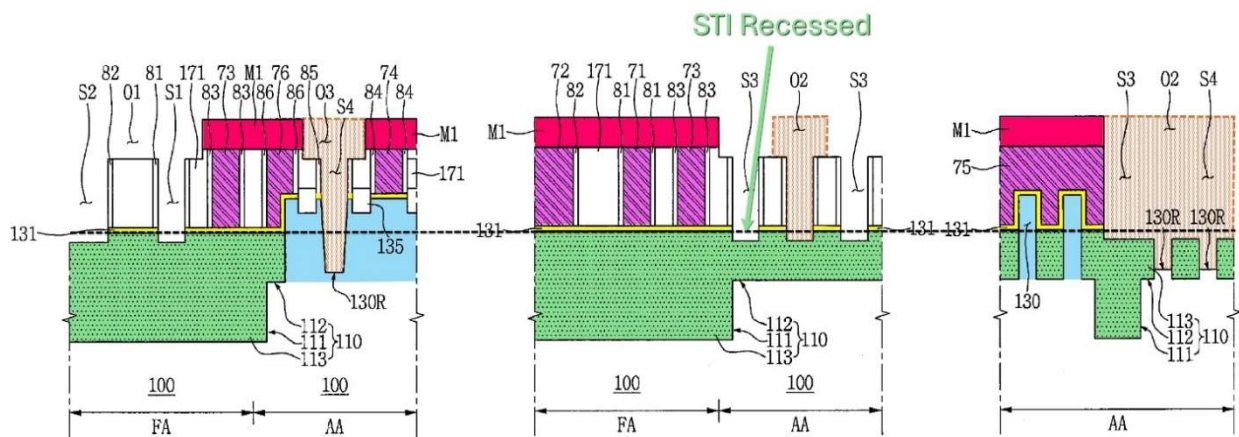
267. Third, by that same logic, and also under a broad view of the claims that is consistent with a view the Patent Owner may advocate (*see* Section VII.C above), sacrificial gate pattern 75 alone may be considered a gate layer.

268. Under these views, Ha discloses (Ground 2A), and at least renders obvious (Ground 2B), forming a gate layer (the polysilicon film to create gate patterns 71-76, gate patterns 71-76 themselves, or gate pattern 75 alone) on fin active

region 130 (a fin-shaped structure) and the insulation material 113 in shallow trenches 112 (an STI). Ha thus satisfies [1c].

d. [1d]: “removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench”

269. In my opinion, Ha discloses [1d] under a broad view of the claim consistent with a view the Patent Owner may advocate. (*See* ITC Complaint ¶89.)

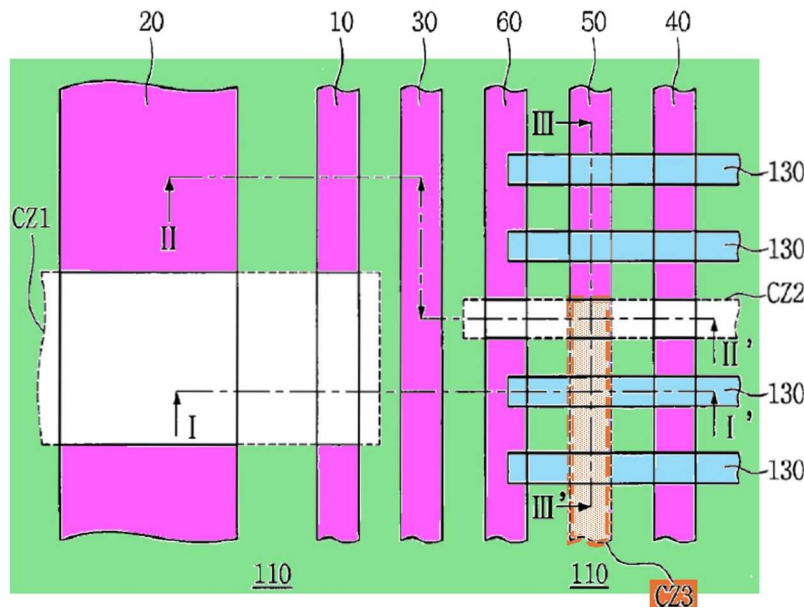


Ha, FIGS. 6A, 6B, 6C (all annotated)

270. Ha discloses “forming a first mask pattern M1” and “removing portions of the sacrificial gate patterns 71 to 76 . . . using the first mask pattern M1 as an etch mask.” (Ha ¶[0099]; *see also* Ha at FIGS. 5A-6C.) As Ha’s figures below show,²¹ mask M1 includes “a fin active cut opening O3 corresponding to . . . the fin active cut-zone CZ3 of FIG. 1.” (Ha ¶¶[0100]-[0101].) Ha further discloses “forming a fin

²¹ Ha’s figure numbers that end in “A” lie along cross-section I–I’ of FIG. 1; those ending in “B” lie along cross-section II–II’; and those ending in “C” lie along cross-section III–III’. (Ha $\llbracket 0043 \rrbracket$ – $\llbracket 0044 \rrbracket$, $\llbracket 0090 \rrbracket$.)

active recess 130R by . . . recessing the fin active region 130” and also explains the exposed portions of isolation region 110 “may be recessed.” (Ha ¶¶[0104]-[0105].)



Ha, FIG. 1

271. If removing a dummy gate pattern qualifies as removing part of the gate layer (as Patent Owner may assert),²² Ha discloses removing part of the gate layer, part of the fin-shaped structure (fin active region 130), and part of the STI (insulation material 113 in shallow trenches 112) to form a trench (orange) in fin active cut-zone CZ3²³ that includes fin active recess 130R. (Ha ¶¶[0099]-[0105], FIGS. 1, 5A-6C.)

²² See Section IX.C.1.c above (discussing the possible mappings of “gate layer” in the context of step [1c].)

²³ Fin gate cut-zone CZ2 and fin active cut-zone CZ3 overlap where cross-sections II–II' and III–III' intersect (fin gate core 50C). (Ha ¶[0063] (“The fin gate cut-zone CZ2 and the fin active cut-zone CZ3 may partially overlap.”), ¶[0083] (noting that “a second fin gate core 50C and a fin active core 130C” co-exist “in a region which overlaps the fin active cut-zone CZ3 of FIG. 1”).)

e. [1e]: “forming a dielectric layer into the trench to form a single diffusion break (SDB)”

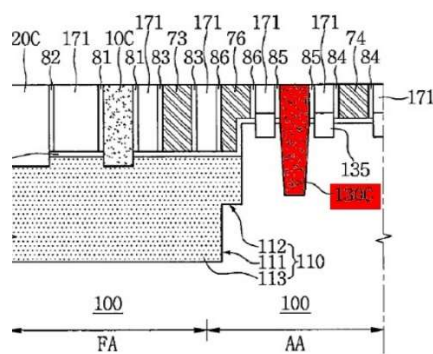
272. In my opinion, Ha discloses (Ground 2A), and at least renders obvious (Ground 2B), step [1e].

273. Ha discloses “forming an insulating core layer 90 which completely or partially fills . . . the fin active cut space S4, and the fin active recess 130R.” (Ha ¶[0106], FIGS. 7A-7C.) Insulating core layer 90 may be silicon nitride, for example, which is a well-known dielectric layer. (Ha ¶[0107] (“The core layer 90 may include, for example, silicon nitride.”); *see also* Shieh ¶[0030] (“The isolation feature 275 is formed by filling in isolation trench 260 with dielectric materials such as silicon oxide, silicon nitride, or silicon oxynitride.”); Xie790 ¶[0029] (“A deposition process was performed to form an insulating material layer 275 (e.g., silicon nitride) in the gate cut cavities 265 and the fin cut cavities 270.”).)

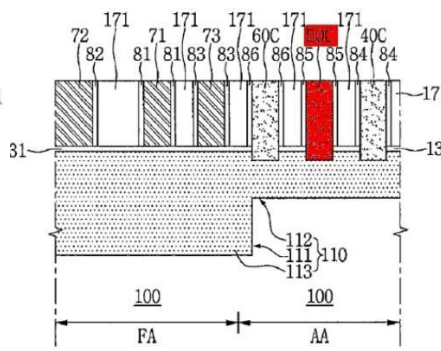
274. Ha further discloses “forming . . . a fin active core 130C by partially removing the core layer 90.” (Ha ¶[0108].) Fin active core 130C thus “fill[s] . . . the fin active cut space S4, [and] the fin active recess 130R” in fin active cut-zone CZ3 (where the trench is formed). (Ha ¶[0109]; *see also* Ha at FIGS. 1, 6A-8C.) Ha explains: “[A] *single diffusion break (SDB) structure* can be implemented using [this] *fin active cutting* method.” (Ha ¶[0129] (emphases added).) From these descriptions, a person of ordinary skill in the art would have understood (Ground 2A), and at least found obvious (Ground 2B), that fin active core 130C is

an SDB structure. Moreover, as with any SDB, fin active core 130C cuts fins 130 and lies immediately adjacent to source/drain regions 135. (See Section VI.C above.)

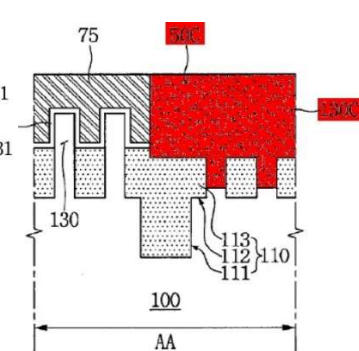
275. Next, Ha discloses removing mask pattern M1 and planarizing the wafer to expose the remaining portions sacrificial gate patterns 71-76, as in FIGS. 9A-9C below. (Ha ¶¶[0110]-[0111] (“[T]he method may include forming silicon oxide, removing the first mask pattern M1 and exposing the sacrificial gate patterns 71 to 76 by performing a planarization process such as a CMP process.”), FIGS. 9A-9C.)



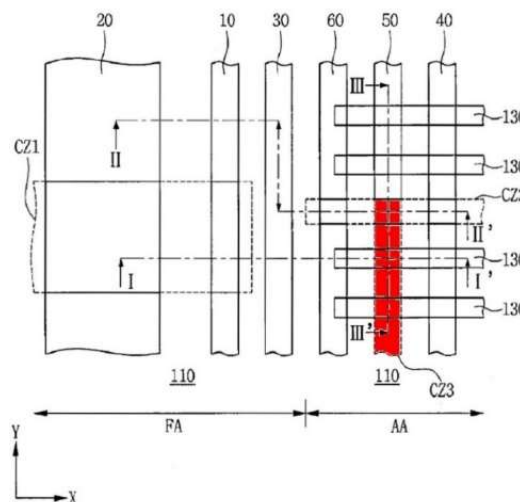
Ha, FIG. 9A



Ha, FIG. 9B



Ha, FIG. 9C

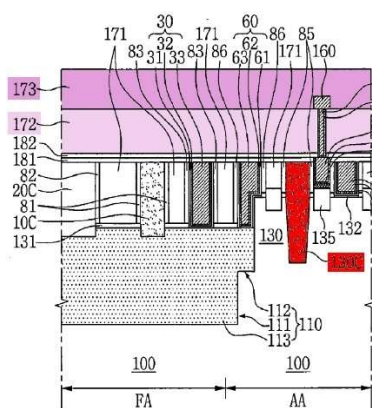
**Ha, FIG. 1**

276. Ha thus discloses (Ground 2A), and at least renders obvious (Ground 2B), forming a dielectric layer (e.g., silicon nitride) into the trench (formed in fin active cut-zone CZ3) to form what Ha itself seems to characterize as “a single diffusion break (SDB) structure” (e.g., fin active core 130C, highlighted above in red) (Ha ¶[0129]; *see also* ’880 Patent at 3:39-59, FIGS. 5-6.)

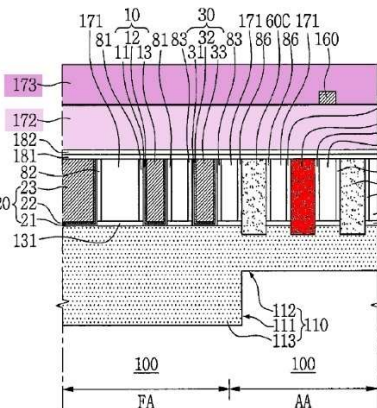
f. [1f]: “after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure”

277. In my opinion, Ha discloses [1f] under a broad view of the claimed ILD layer consistent with the Patent Owner's apparent understanding of the claim. (*See* Section VII.C above.)

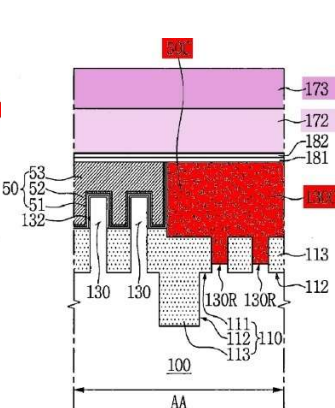
278. Ha discloses “forming a second interlayer insulating layer 172” made of silicon oxide and “forming a third interlayer insulating layer 173” made of silicon oxide or silicon nitride. (Ha ¶[0122], ¶[0124]; *see also* Ha at FIGS. 2A-2C.)



Ha, FIG. 2A



Ha, FIG. 2B



Ha, FIG. 2C

279. As FIGS. 2A-2C above indicate,²⁴ interlayer insulating layers 172 and 173 (ILD layers) are thus formed after—and on top of—fin active core 130C (the SDB structure). (Ha ¶¶[0122]-[0125], FIGS. 2A-2C, 14A-14C; *see* Section IX.C.1.e above.) A person of ordinary skill in the art would have understood that *interlayer insulating layers* 172 and 173, together or individually, are *interlayer dielectric layers* (“ILD” layers) because silicon oxide and silicon nitride are well-known dielectric materials. (*See*, for example, Shieh ¶[0030] (“The isolation feature 275 is formed by filling in isolation trench 260 with dielectric materials such as silicon oxide, silicon nitride, or silicon oxynitride.”).)

280. Under the Patent Owner’s apparent understanding of [1f], *any* ILD layer, including Ha’s ILD layers 172 and/or 173, formed after (and on) the SDB may satisfy claim 1. (*See* Section VII.C above.) Applying that understanding, Ha discloses forming an ILD layer (Ha’s ILD layer 172 and/or 173) on the SDB structure (fin active core 130C) after forming the SDB structure.

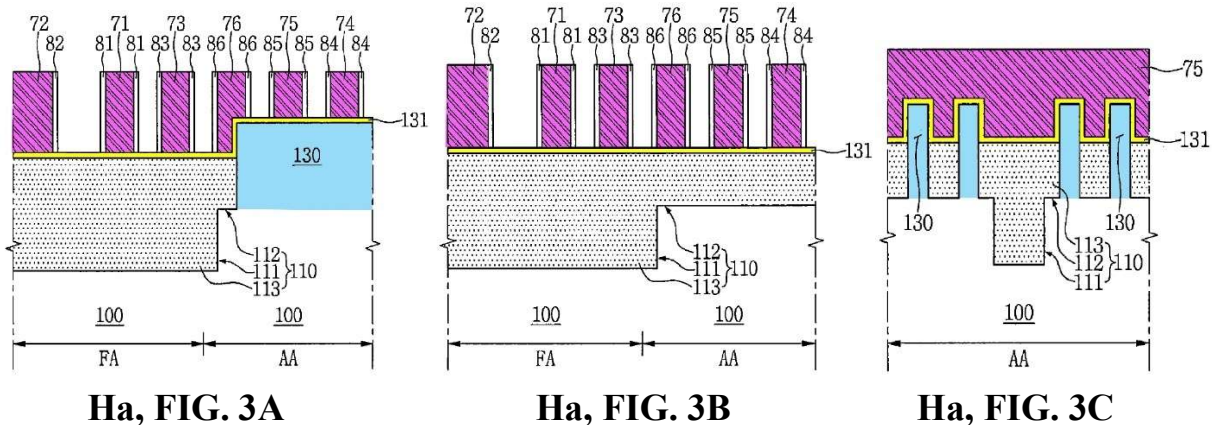
2. Claim 2: “The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.”

281. Claim 2 depends from claim 1. I understand that means claim 2 requires all the same features as claim 1, plus the additional features recited in claim 2. Under

²⁴ Ha’s figure numbers that end in “A” lie along cross-section I–I' of FIG. 1; those ending in “B” lie along cross-section II–II'; and those ending in “C” lie along cross-section III–III'. (Ha ¶¶[0043]-[0044], ¶[0090].)

a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

282. It is my opinion that Ha discloses the additional features of claim 2.



283. Ha discloses “forming a base insulating layer 131 on surfaces of the fin active region 130 and the isolation region 110, and forming sacrificial gate patterns 71 to 76 and gate spacers 81 to 86 on the base insulating layer 131.” (Ha ¶[0091].) “The base insulating layer 131 may include silicon oxide.” (Ha ¶[0094].)

284. Thus, as FIGS. 3A-3C above indicate, Ha discloses forming a gate dielectric layer (base insulating layer 131) on the fin-shaped structure (fin active region 130) before forming the gate layer.²⁵ Accordingly, Ha satisfies claim 2.

²⁵ Depending how the claim language is applied, Ha’s “gate layer” may be (A) the polysilicon film used to form sacrificial gate patterns 71-76, (B) the sacrificial gate patterns 71-76 themselves, or (C) sacrificial gate pattern 75 alone. (*See* Section IX.C.1.c above (discussing [1c]).)

285. A person of ordinary skill in the art would have understood base insulating layer 131 is a gate dielectric layer because it underlies the gate patterns and sets on top of fin active region 130 (where a FinFET gate dielectric layer resides), and silicon oxide is a dielectric material. This is precisely what the '880 Patent describes. (*See* '880 Patent at 3:3-10 (“Next, a gate dielectric layer 18 and a gate layer 20 are formed to cover the fin-shaped structures 14 and the STI 16 [T]he gate dielectric layer 18 preferably includes silicon oxide”), FIG. 2; Ha ¶[0091] (“The method of forming the semiconductor device . . . may include . . . forming a base insulating layer 131 on surfaces of the fin active region 130 and the isolation region 110”), ¶[0094] (“The base insulating layer 131 may include silicon dioxide.”), FIGS. 3A-3C.)

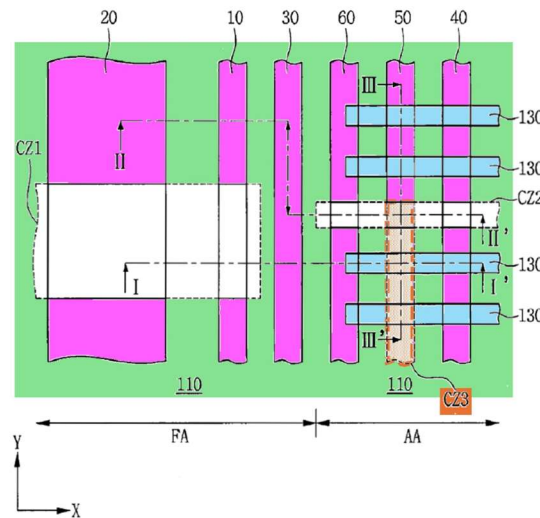
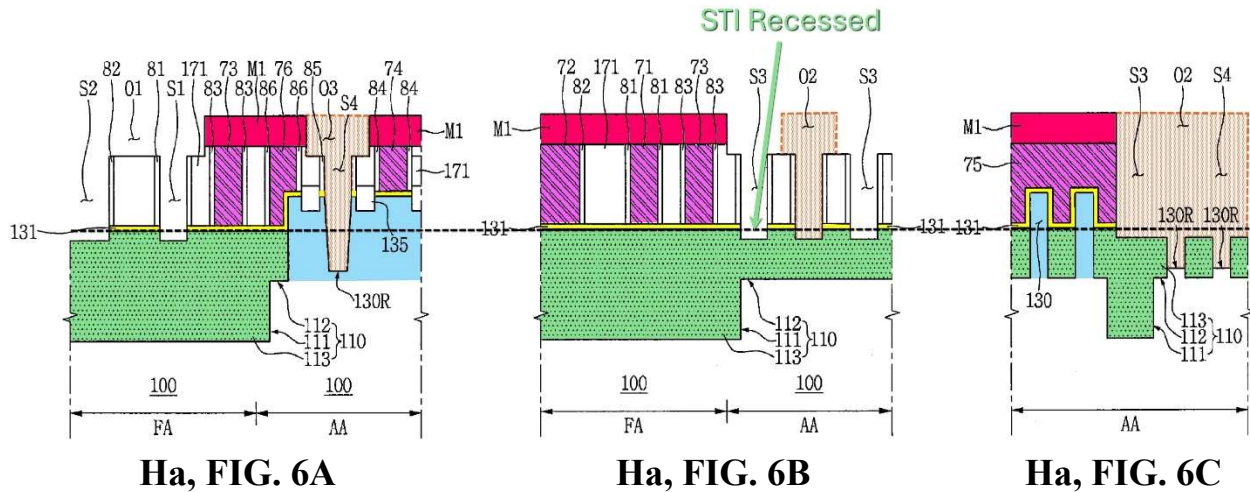
286. Although base insulating layer 131 is replaced by a high-k gate dielectric layer in the final device structure (*see* Ha ¶¶[0112]-[0115], FIGS. 11A-11C), this is no different than the claimed gate dielectric layer 18 of the '880 Patent, which is itself replaced by a high-k dielectric layer in the final device structure (*see* '880 Patent at 5:11-42, FIG. 10).

- 3. Claim 3: “The method of claim 2, further comprising: forming a patterned mask on the gate layer; and using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.”**

287. Claim 3 depends from claim 2. I understand that means claim 3 requires all the same features as claim 2, plus the additional features recited in claim 3. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 2 for the reasons I state in Section IX.C.2 above.

288. It is my opinion that Ha discloses the additional features of claim 3.

289. Ha discloses “forming a first mask pattern M1” and “removing portions of the sacrificial gate patterns 71 to 76 . . . using the first mask pattern M1 as an etch mask” to define gate cut spaces S1-S4. (Ha ¶[0099], FIGS. 5A-6C.) According to Ha, “[t]he base insulating layer 131 may be exposed by removing the portions of . . . the sacrificial second fin gate pattern 75 . . . which are exposed in . . . the fin active cut opening O3.” (Ha ¶[0101].) Then, “the method may include forming a fin active recess 130R by removing the base insulating layer 131 exposed in the fin active cut space S4 and recessing the fin active region 130.” (Ha ¶[0104].)



290. Thus, as illustrated above, Ha discloses forming a patterned mask (mask pattern M1, red) on the gate layer²⁶ and using the patterned mask as a mask to remove part of the gate layer (magenta), part of the gate dielectric layer (base insulating layer 131) (yellow), and part of the fin-shaped structure (fin active

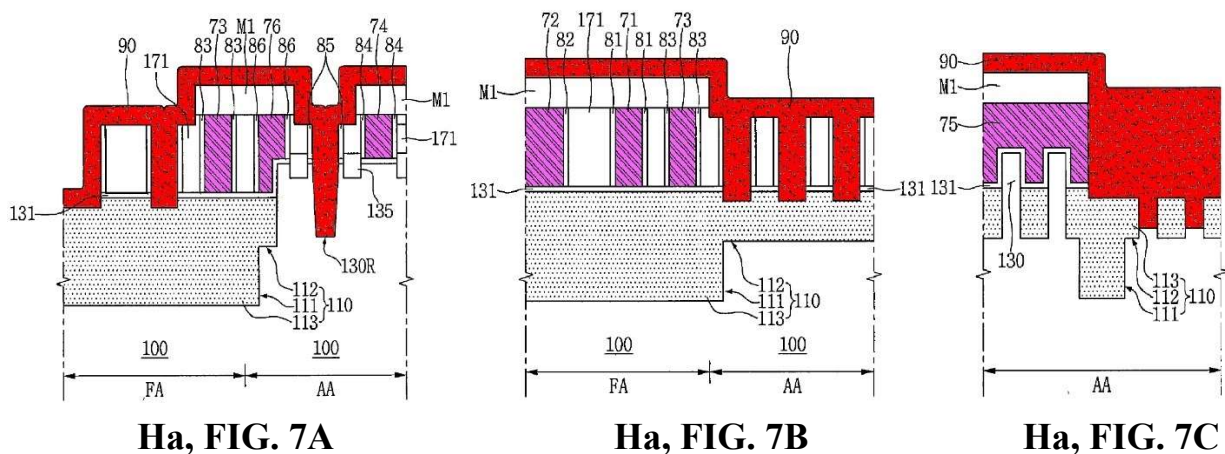
²⁶ Depending how the claim language is applied, Ha's "gate layer" may be (A) the polysilicon film used to form sacrificial gate patterns 71-76, (B) the sacrificial gate patterns 71-76 themselves, or (C) sacrificial gate pattern 75 alone. (See Section IX.C.1.c above (discussing [1c]).)

region 130) (blue) to form the trench (orange). (Ha ¶¶[0099]-[0105], FIGS. 5A-6C; *see* Section IX.C.1.d above (discussing this etching sequence).) Ha therefore satisfies claim 3.

4. **Claim 4: “The method of claim 1, further comprising: forming the dielectric layer into the trench and on the gate layer; and planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.”**

291. Claim 4 depends from claim 1. I understand that means claim 4 requires all the same features as claim 1, plus the additional features recited in claim 4. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

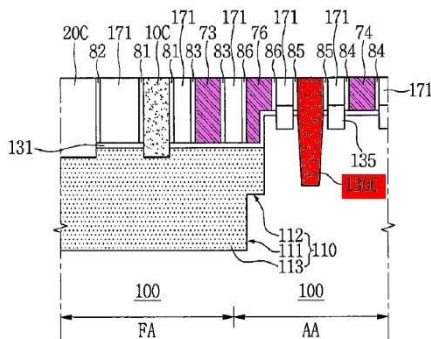
292. It is my opinion that Ha discloses the additional features of claim 4.



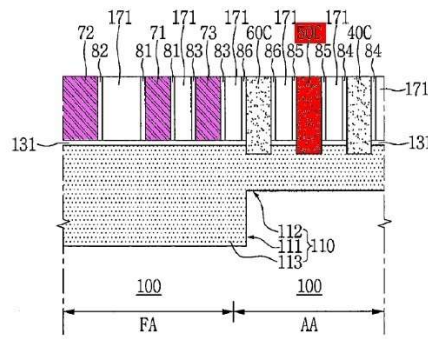
293. Ha discloses “forming an insulating core layer 90 which completely or partially fills . . . the fin active cut space S4, and the fin active recess 130R” (i.e., the trench in fin active cut-zone CZ3). (Ha ¶[0106].) “[T]he insulating core layer 90

[dielectric layer, red] may be formed semi-conformally,” such that it (A) fills the trench (*see* Section IX.C.1.e above) and (B) forms on the gate layer²⁷ (magenta), as shown above. (Ha ¶[0106]; *see also* Ha at FIGS. 7A-7C.)

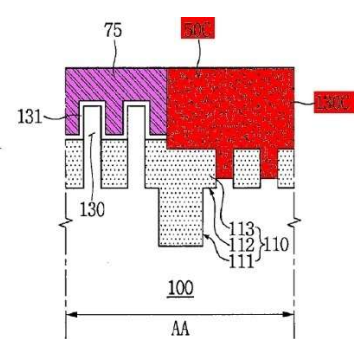
294. Ha further discloses “forming silicon oxide, removing the first mask pattern M1 and exposing the sacrificial gate patterns 71 to 76 by performing a planarization process such as a CMP process.” (Ha ¶[0110].) Accordingly, “[u]pper surfaces of the remaining sacrificial gate patterns 71 to 76, . . . the first and second and the fin active core 130C may be coplanar.” (Ha ¶[0111]; *see also* Ha at FIGS. 9A-9C.)



Ha, FIG. 9A



Ha, FIG. 9B



Ha, FIG. 9C

295. Thus, as in FIGS. 9A-9C above, Ha discloses planarizing the dielectric layer (red) so that the top surfaces of the dielectric layer and the gate layer (magenta) are coplanar. (Ha ¶[0110]-[0111].) Accordingly, Ha discloses claim 4.

²⁷ Depending how the claim language is applied, Ha’s “gate layer” may be (A) the polysilicon film used to form sacrificial gate patterns 71-76, (B) the sacrificial gate patterns 71-76 themselves, or (C) sacrificial gate pattern 75 alone. (*See* Section IX.C.1.c above (discussing [1c]).)

5. Claim 5: “The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure.”

296. Claim 5 depends from claim 1. I understand that means claim 5 requires all the same features as claim 1, plus the additional features recited in claim 5. Under a broad view of the claims that is consistent with a view the Patent Owner may advocate (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

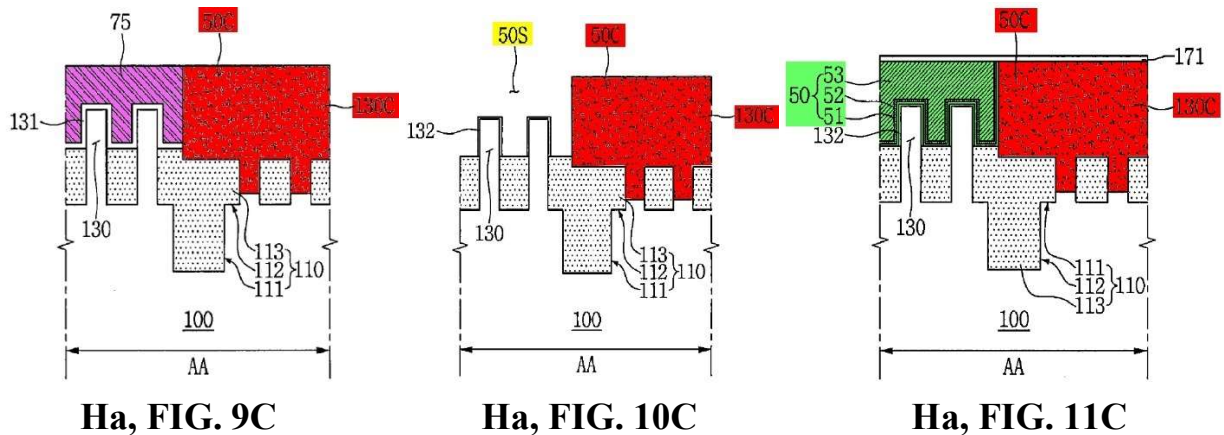
297. Assuming claim 1 is satisfied, it is also my opinion that Ha discloses the additional features of claim 5.

298. First, I present my analysis assuming the claimed “gate layer” may be satisfied by sacrificial gate pattern 75. (*See* Sections IX.C.1.c-d above.) As can be seen in part from the transition between Ha’s FIG. 9C and Ha’s FIG. 10C (shown below), Ha discloses “forming gate electrode space[] . . . 50S . . . by removing the exposed sacrificial gate pattern[] [75] by performing a silicon etching process.” (Ha ¶[0112].) And as can be seen in part from the transition between Ha’s FIG. 10C and Ha’s FIG. 11C (shown below), Ha further discloses “forming gate pattern[] . . . 50 . . . in the gate electrode space[] . . . 50S” (Ha ¶[0113]; *see also* Ha ¶¶[0114]-[0115].)

299. Ha thus discloses removing part of the gate layer (part of sacrificial gate pattern 75) (magenta) after forming the SDB structure (red) to form a gate structure

(gate pattern 50) (green) adjacent to the SDB structure. (Ha ¶¶[0112]-[0115].)

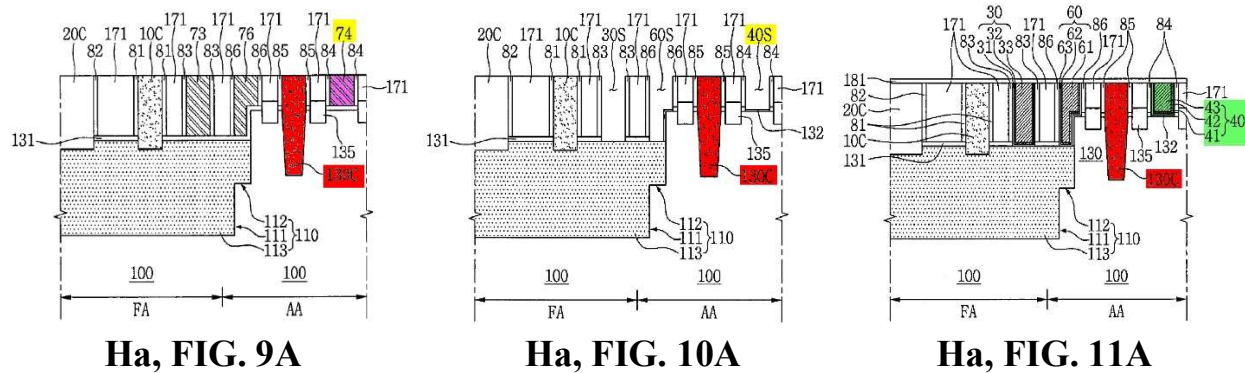
Accordingly, Ha satisfies claim 5.



300. Second, I present my analysis assuming the claimed “gate layer” is the polysilicon film used to create gate patterns 71-76. (See Section IX.C.1.c above.) Ha satisfies claim 5 under my second analysis for the same reasons described above, because sacrificial gate pattern 75 is made of that same polysilicon film.

301. Under this analysis, applying a broad view of the claims that is consistent with a view the Patent Owner may advocate (see Section VII.C above (discussing ITC Complaint ¶89)), Ha also satisfies claim 5 for an additional reason. As shown in FIGS. 9A, 10A, and 11A below, Ha discloses removing part of the gate layer (for example, part of sacrificial gate pattern 74) (magenta) after forming the SDB structure (red) to form a gate structure (gate pattern 40) (green) adjacent to the SDB structure. (Ha ¶¶[0112]-[0115] (“[T]he method may include forming gate electrode spaces 10S, 20S, 30S, 40S, 50S, and 60S by removing the exposed sacrificial gate patterns 71 to 76 by performing a silicon etching process The

method may include forming gate patterns 10, 20, 30, 40, 50, and 60 in the gate electrode spaces 10S, 20S, 30S, 40S, 50S, and 60S . . .”), FIGS. 9A-11C.)



302. Although this analysis views the final metal gate structure as the claimed “gate structure,” whereas the ’880 Patent contemplates the gate structure as being the dummy gate structure (*see* ’880 Patent at 4:8-14, FIG. 8), this analysis is consistent with a view the Patent Owner may advocate.

6. **Claim 7: “The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.”**

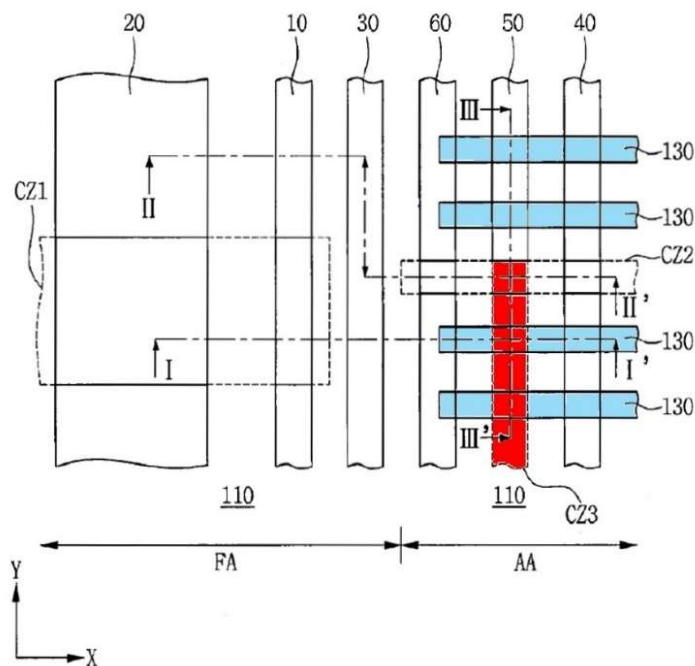
303. Claim 7 depends from claim 1. I understand that means claim 7 requires all the same features as claim 1, plus the additional features recited in claim 7. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

304. It is my opinion that Ha discloses the additional features of claim 7.

305. Ha discloses that “fin active regions 130 . . . extend in parallel in the X direction” and that “fin active cut-zone CZ3 . . . extend[s] in the Y direction.” (Ha

¶[0058], ¶[0062]; *see also* Ha ¶[0028].) As Ha's FIG. 1 indicates below, the fin-shaped structure (active fin 130) (blue) extends along a first direction (X direction), and the SDB structure (fin active recess 130C, i.e., active fin cut-zone CZ3 filled with core layer 90) (red) extends along a second direction (Y direction). (*See* Section IX.C.1.e above (discussing Ha's SDB formation).)

Accordingly, H_a satisfies claim 7. $\square$

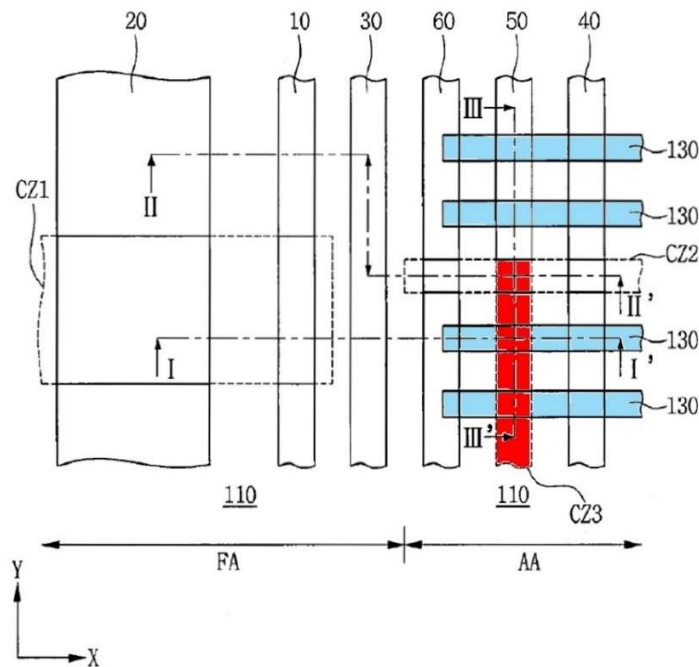


Ha, FIG. 1

7. Claim 8: “The method of claim 7, wherein the first direction is orthogonal to the second direction.”

306. Claim 8 depends from claim 7. I understand that means claim 8 requires all the same features as claim 7, plus the additional features recited in claim 8. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 7 for the reasons I state in Section IX.C.6 above.

307. It is my opinion that Ha discloses the additional features of claim 8.



Ha, FIG. 1

308. As illustrated in FIG. 1 above, the first direction (X direction of active fins 130 in blue) is orthogonal (perpendicular) to the second direction (Y direction of active fin cut-zone CZ3 and fin active recess 130C in red). (Ha $\overline{100}$ [0028], $\overline{100}$ [0058], $\overline{100}$ [0062], FIG. 1; *see* Section IX.C.6 above.)

8. Claim 10: “The method of claim 1, wherein the gate layer comprises polysilicon.”

309. Claim 10 depends from claim 1. I understand that means claim 10 requires all the same features as claim 1, plus the additional features recited in claim 10. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

310. It is my opinion that Ha discloses the additional features of claim 10.

311. Ha discloses a polysilicon gate layer.²⁸ (*See* Section IX.C.1.c above (discussing the claimed “gate layer”).) Ha states that “sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon.” (Ha ¶[0095].) Polycrystalline silicon and polysilicon are synonymous. (Ha ¶[0009] (“[T]he fin gate pattern may include polysilicon . . .”), claim 4 (“[T]he sacrificial fin gate pattern comprise[s] polysilicon . . .”).) A person of ordinary skill in the art thus would have understood that the material used to create Ha’s sacrificial gate patterns 71 to 76 (gate layer) may be polysilicon. Accordingly, Ha satisfies claim 10.

9. Claim 11: “The method of claim 1, wherein the dielectric layer comprises silicon nitride.”

312. Claim 11 depends from claim 1. I understand that means claim 11 requires all the same features as claim 1, plus the additional features recited in claim 11. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

313. It is my opinion that Ha discloses the additional features of claim 11.

314. Ha explains: “The core layer 90 may include, for example, silicon nitride.” (Ha ¶[0107]; *see also* Ha ¶[0017] (“[T]he fin active core may include silicon nitride . . .”), ¶[0072] (“The fin active core 130C may include, for example, silicon

²⁸ Depending how the claim language is applied, Ha’s “gate layer” may be (A) the polysilicon film used to form sacrificial gate patterns 71-76, (B) the sacrificial gate patterns 71-76 themselves, or (C) sacrificial gate pattern 75 alone. (*See* Section IX.C.1.c above (discussing [1c]).)

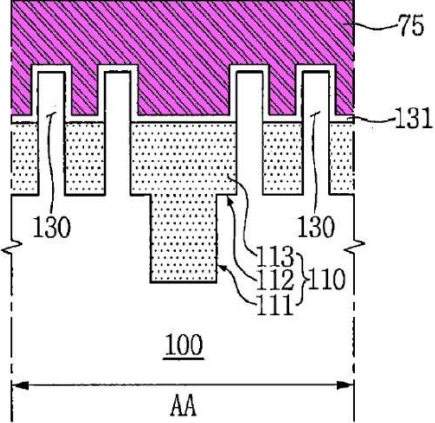
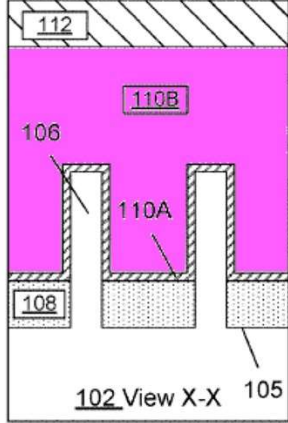
nitride.”), claim 4 (“[T]he fin active core comprise[s] silicon nitride.”), claim 12 (same).) Because Ha’s core layer 90 fills fin active cut-zone CZ3 to make fin active core 130C, Ha’s dielectric layer may be silicon nitride, satisfying claim 11.

D. Ground 2C: The Combination of Ha and Zhao Renders Obvious Claim 9

1. A person of ordinary skill in the art would have found it obvious to make Ha’s sacrificial gate structures using amorphous silicon, as Zhao discloses

315. According to Ha, sacrificial gate patterns 71-76 “may include” polysilicon, “for example.” (Ha ¶[0009] (“[T]he sacrificial fin gate pattern *may include* polysilicon” (emphasis added)), ¶[0095] (“The sacrificial gate patterns 71 to 76 each *may include, for example*, polycrystalline silicon.” (emphasis added)); *see also* Section IX.C.8 above (discussing claim 10).) Amorphous silicon was a well-known substitute for polysilicon with very similar properties. (See Shieh ¶[0013] (“The dummy gate structure 220 includes a dummy gate layer 221, such as polysilicon, amorphous silicon or other appropriate materials.”); Doris ¶[0047] (referencing “an amorphous silicon (α -Si) layer 802” that also may be an “ α -Si (polysilicon) layer 802”).) Zhao explains, for example, that its sacrificial gate electrode material 110B (equivalent to the material used to make Ha’s sacrificial gate patterns 71-76) “is comprised of a material such as polysilicon or amorphous silicon.” (Zhao at 6:36-42.)

316. As the table below demonstrates, Ha and Zhao disclose very similar sacrificial / dummy gate structures for forming SDBs:

Ha	Zhao
 Ha, FIG. 9B	 Zhao, FIG. 2C (excerpted)
“[T]he sacrificial fin gate pattern may include polysilicon . . .” (Ha ¶[0009].) “The sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon.” (Ha ¶[0095].)	“[T]he sacrificial gate electrode material 110B is comprised of a material such as polysilicon or amorphous silicon . . .” (Zhao, 6:36-42.) “[S]acrificial gate materials of said first, second and third gate structures are comprised of one of polysilicon or amorphous silicon . . .” (Zhao, claim 16.)

317. Both Ha and Zhao disclose sacrificial gate material deposited on the fin structures and STI. (See Ha ¶[0091], ¶[0095], FIGS. 1, 3A-3C; Zhao at 6:28-42, FIG. 2C.) Although the example specifically described for Ha’s sacrificial gate patterns 71-76 is polysilicon, a person of ordinary skill in the art would have understood it is only one example. (See Ha ¶[0009] (“[T]he sacrificial fin gate

pattern *may* include polysilicon” (emphasis added)), ¶[0095] (“The sacrificial gate patterns 71 to 76 each *may include, for example*, polycrystalline silicon.” (emphasis added)).)

318. Zhao explains that amorphous silicon, which was a well-known substitute for polysilicon in such dummy gates, may also be used for sacrificial gate structures when forming SDBs. (See Zhao at 6:36-42 (“[T]he sacrificial gate electrode material 110B is comprised of a material such as *polysilicon or amorphous silicon*” (emphasis added)), claim 16 (same); Shieh ¶[0013] (“The dummy gate structure 220 includes a dummy gate layer 221, such as *polysilicon, amorphous silicon* or other appropriate materials.” (emphasis added)); Doris ¶[0047] (describing “an *amorphous silicon* (α -Si) layer 802,” which can also be an “ α -Si (*polysilicon*) layer 802” (emphases added)).)

319. A person of ordinary skill in the art would have been motivated to use amorphous silicon for Ha’s sacrificial gate patterns 71-76 since polysilicon and amorphous silicon have similar chemical properties, allowing them to be used as substitutes in this application. (See, for example, Shieh ¶[0013] (“The dummy gate structure 220 includes a dummy gate layer 221, such as polysilicon, amorphous silicon or other appropriate materials.”).) A person of ordinary skill in the art would have understood it does not matter whether Ha’s sacrificial gate patterns 71-76 are made of polysilicon or made of amorphous silicon since both were known materials

for forming FinFET dummy gates. (*See* Zhao at 6:36-42, claim 16, FIG. 2C; Shieh ¶[0013]; Doris ¶[0047].)

320. I have been told that if there's a known technique to address a known problem using prior art elements according to their established functions, then there is a motivation to combine. Here, the technique to address the problem of which material to use for a sacrificial FinFET gate layer is to use either polysilicon or amorphous silicon. (Zhao at 6:36-42; *see also* Shieh ¶[0013]; Doris ¶[0047].) Accordingly, a person of ordinary skill in the art would have been motivated to use either one, including amorphous silicon, in Ha's FinFETs.

321. Additionally, a person of ordinary skill in the art would have had a reasonable expectation of success when using amorphous silicon as the material in Ha's sacrificial gates 71-76 because it would not have been expected to affect any other steps in Ha's process flow or to materially affect the final device. For example, there is no reason amorphous silicon sacrificial gates 71-76 would not be equally suitable for removal as shown in Ha's FIGS. 5A-5C, for planarization as shown in Ha's FIGS. 9A-9C, or for removal and replacement with metal gate structures as shown in Ha's FIGS. 10A-11C. (*See* Ha ¶[0099], ¶[0110], ¶¶[0112]-[0115].)

322. Applying the legal standards explained to me, as summarized above in Section IV.B, it is my opinion that a person of ordinary skill in the art would have viewed using amorphous silicon to make Ha's sacrificial gate patterns 71-76 (as

Zhao discloses) as an obvious example of the following: (1) substituting one known element for another (amorphous silicon for polysilicon) to obtain predictable results; (2) a choice from among a finite number of identified, predictable solutions, (polysilicon or amorphous silicon), with a reasonable expectation of success; and (3) a teaching, suggestion, or motivation in the prior art (*see* Zhao, 6:28-42) that would have led a person of ordinary skill in the art to arrive at the claimed invention.

2. Claim 9: “The method of claim 1, wherein the gate layer comprises amorphous silicon.”

323. Claim 9 depends from claim 1. I understand that means claim 9 requires all the same features as claim 1, plus the additional features recited in claim 9. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

324. Assuming claim 1 is satisfied, it is also my opinion that Ha discloses the additional features of claim 9. Combining Zhao with Ha in the way I describe in the preceding subsection does not affect my analysis of claim 1 for the Ha reference.

325. In the combination of Ha and Zhao I describe in the preceding subsection, Ha’s gate layer²⁹ comprises amorphous silicon. (*See* Section IX.D.1 above (describing the combination of Ha and Zhao); Zhao at 6:36-42 (“[T]he

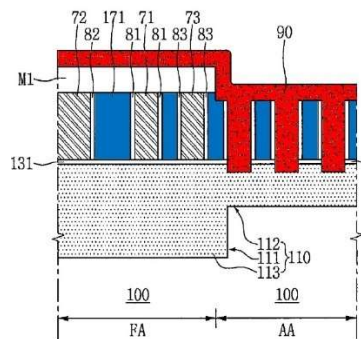
²⁹ Depending how the claim language is applied, Ha’s “gate layer” may be (A) the polysilicon film used to form sacrificial gate patterns 71-76, (B) the sacrificial gate patterns 71-76 themselves, or (C) sacrificial gate pattern 75 alone. (*See* Section IX.C.1.c above (discussing [1c]).)

sacrificial gate electrode material 110B is comprised of a material such as polysilicon or amorphous silicon . . .”).) Accordingly, the combination of Ha and Zhao satisfies claim 9.

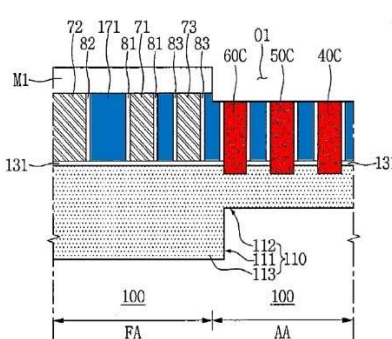
E. Ground 2D: The Combination of Ha and Yu Renders Obvious Claim 12

1. A person of ordinary skill in the art would have found it obvious to make Ha’s fin gate core and fin active core using silicon oxide, as Yu discloses

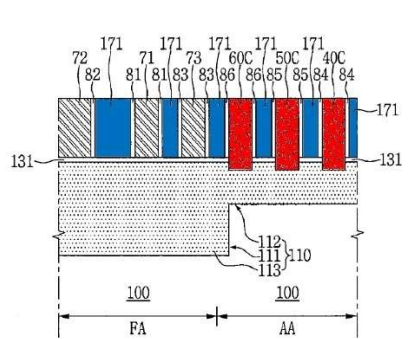
326. To perform Ha’s planarization sequence, depicted below in FIGS. 7B-9B, a person of ordinary skill in the art would have understood that Ha’s core layer 90 (red) and Ha’s first interlayer insulating layer 171 (blue) must be made using different materials, such that core layer 90 may be selectively removed relative to first interlayer insulating layer 171.



Ha, FIG. 7B



Ha, FIG. 8B



Ha, FIG. 9B

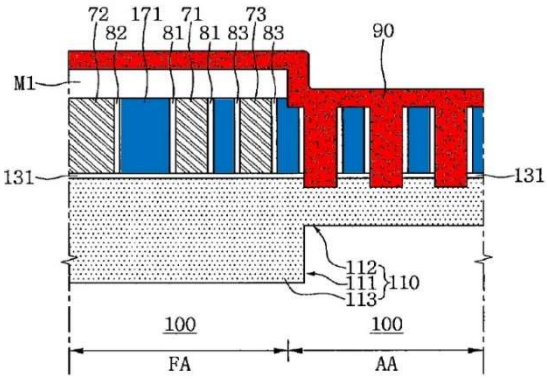
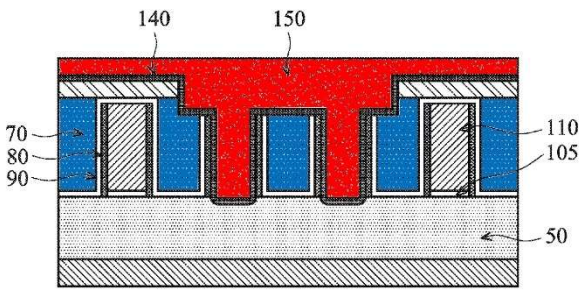
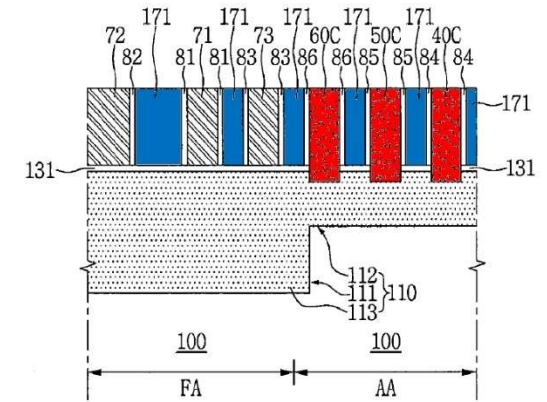
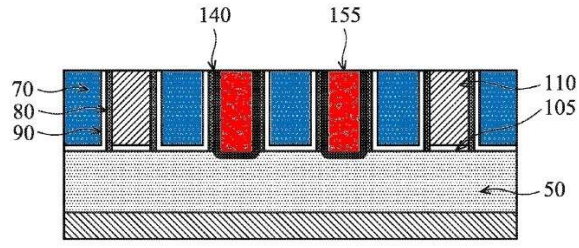
327. Ha discloses, for example, “an isotropic etch-back process” that “remov[es] portions of the core layer 90 formed on the first mask pattern M1 or the first interlayer insulating layer 171” and “a planarization process such as a CMP

process.” (Ha ¶¶[0109]-[0110]; *see also* Ha ¶¶[0108]-[0111], FIGS. 7A-9C.)

A person of ordinary skill in the art would have understood this is preferably done by exploiting the etch selectivity between core layer 90 and first interlayer insulating layer 171.

328. Ha discloses one embodiment that achieves such selectivity: making core layer 90 out of silicon nitride and making first interlayer insulating layer 171 out of silicon oxide. (Ha ¶[0074] (“The first interlayer insulating layer 171 may include, for example, silicon oxide.”), ¶[0107] (“The core layer 90 may include, for example, silicon nitride.”).) Silicon oxide and silicon nitride are commonly used insulators that can be removed selectively with respect to one another. (*See* Plummer at 645 & Tbl. 10-3 (providing exemplary selective plasma etch chemistries for SiO₂ and Si₃N₄).) A person of ordinary skill in the art would have understood that these materials could be reversed in Ha, i.e., that core layer 90 may comprise silicon oxide, and first interlayer insulating layer 171 may comprise silicon nitride. (*See* Yu ¶[0026] (“The ILD 70 may include . . . silicon nitride . . .”), ¶[0036] (“[I]nsulating layer 150 is made of silicon oxide . . .”).) A person of ordinary skill in the art would have found this modification obvious because both silicon oxide and silicon nitride were commonly used insulating materials.

329. As this table shows, Yu and Ha describe similar structures and process flows. (*See* Ha ¶¶[0106]-[0111], FIGS. 7A-9C; Yu ¶¶[0034]-[0038], FIGS. 7A-8B.)

Ha	Yu
 Ha, FIG. 7B	 Yu, FIG. 7B
 Ha, FIG. 9B	 Yu, FIG. 8B
“The first interlayer insulating layer 171 may include, for example, silicon oxide.” (Ha ¶[0074].)	“The ILD 70 may include silicon oxide, silicon nitride, silicon oxynitride (SiON), SiOCN, fluorine-doped silicate glass (FSG), or a low-K dielectric material, and may be made of CVD or other suitable process.” (Yu ¶[0026].)
“The core layer 90 may include, for example, silicon nitride.” (Ha ¶[0107].)	“The thick filling insulating layer 150 is made of silicon oxide or silicon nitride based materials such as SiN, SiCN, SiON or SiOCN.” (Yu ¶[0036].)

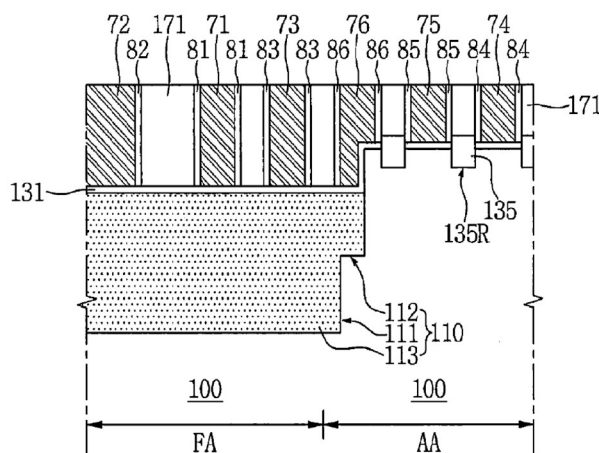
330. Yu’s insulating layer 150 (corresponding to Ha’s core layer 90) and Yu’s interlayer dielectric layer 70 (corresponding to Ha’s first interlayer insulating

layer 171) may include either silicon nitride or silicon oxide (or other related materials). (Yu ¶[0026], ¶[0036].) In view of those disclosures, a person of ordinary skill in the art would have found it obvious that Ha's core layer 90 may comprise silicon oxide while Ha's first interlayer insulating layer 171 may comprise silicon nitride, because both were common dielectric materials used for electrical insulation. (See Xie078 ¶[0032] ("The gate separation structure 114 may be comprised of a variety of materials, e.g., silicon dioxide, silicon nitride, etc."); Yu ¶[0036] (explaining "insulating layer 150 is made of silicon oxide or silicon nitride based materials"); Zhao at 8:10-13 (disclosing "a layer of insulating material 123, such as silicon dioxide"); Shieh ¶[0030] ("The isolation feature 275 is formed by filling in isolation trench 260 with dielectric materials such as silicon oxide, silicon nitride, or silicon oxynitride.").)

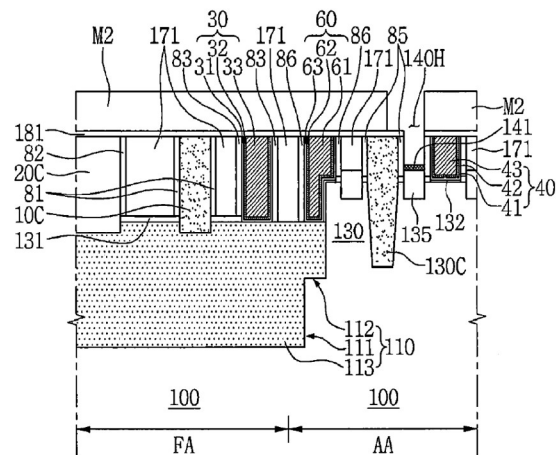
331. In my opinion, a person of ordinary skill in the art would have been motivated to make such a modification since Ha's process will work properly so long as Ha's core layer 90 is made of an insulating material that can be selectively removed with respect to Ha's insulating first interlayer insulating layer 171. (See Ha FIGS. 7A-9C (showing a planarization process whereby the core layer 90 becomes coplanar with the first interlayer insulating layer 171).) Whether core layer 90 is made of silicon nitride and first interlayer insulating layer 171 is made of silicon oxide, or the other way around, is not critical. Both were known techniques for

achieving this same, well-known function. (See Xie078 ¶[0032]; Yu ¶[0026], ¶[0036]; Zhao at 8:10-13; Shieh ¶[0030].)

332. I have been told that if there's a known technique to address a known problem using prior art elements according to their established functions, then there is a motivation to combine. Here, the technique to address the problem of which materials to use for the ILD layer and SDB structure was to use silicon oxide or silicon nitride. (See Xie078 ¶[0032]; Yu ¶[0026], ¶[0036]; Zhao at 8:10-13; Shieh ¶[0030].) And either choice would work in Ha's process flow so long as Ha's ILD layer (first interlayer insulating layer 171) and Ha's SDB structure (core layer 90) are not both made from the same one of these two materials. Thus, a person of ordinary skill in the art would have been motivated to use a silicon nitride first interlayer insulating layer 171 and a silicon oxide core layer 90, for example.



Ha, FIG. 4B



Ha, FIG. 12A

333. A person of ordinary skill in the art would have had a reasonable expectation of success when doing this because it would not have been expected to

inhibit any other steps in Ha's process flow or to materially affect the final device. For example, there is no reason a silicon nitride first interlayer insulating layer 171 would be incompatible with source/drain regions 135. (See Ha ¶[0097], FIG. 4B (above).) A person of ordinary skill in the art would have known how to selectively remove certain portions of a silicon nitride first interlayer insulating layer 171 when contacting source/drain regions 135. (See Ha ¶[0116], FIG. 12A (above); Plummer at 645 (Tbl. 10-3) (explaining that CHF_3/O_2 and CH_2F_2 plasma chemistries for Si_3N_4 are both "[v]ery anisotropic; selective over Si and SiO_2).)

334. Applying the legal standards explained to me, as summarized above in Section IV.B, it is my opinion that a person of ordinary skill in the art would have viewed using a silicon nitride first interlayer insulating layer 171 and a silicon oxide core layer 90 in Ha's process flow as an obvious example of the following: (1) substituting one known element for another (silicon oxide for silicon nitride, and vice versa) to obtain predictable results; (2) choosing from among a finite number of identified, predictable solutions (using silicon oxide for one of the two layers and using silicon nitride for the other), with a reasonable expectation of success; and (3) a teaching, suggestion, or motivation in the prior art (*see* Yu ¶[0026], ¶[0036]) that would have led a person of ordinary skill in the art to arrive at the claimed invention.

2. Claim 12: “The method of claim 1, wherein the dielectric layer comprises silicon oxide.”

335. Claim 12 depends from claim 1. I understand that means claim 12 requires all the same features as claim 1, plus the additional features recited in claim 12. Under a broad view of the claims (*see* Section VII.C above), Ha discloses all the features recited in claim 1 for the reasons I state in Section IX.C.1 above.

336. Assuming claim 1 is satisfied, it is also my opinion that Ha discloses the additional features of claim 12. Combining Yu and Ha in the way I describe in the preceding subsection does not affect my analysis of claim 1 for the Ha reference.

337. In the combination of Ha and Yu I describe in the preceding subsection, Ha’s dielectric layer (core layer 90) comprises silicon oxide. (*See* Section IX.E.1 above (describing the combination of Ha and Yu); Yu ¶[0036] (“[I]nsulating layer 150 is made of silicon oxide”).) Accordingly, the combination of Ha and Yu satisfies claim 12.

X. Conclusion

338. As discussed above, it is my opinion that the Challenged Claims of the ’880 Patent (i.e., claims 1-12) are unpatentable.

339. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place

within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

340. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

341. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 17th day of April, in 2025.

By: Suman Datta.

Dr. Suman Datta, Ph.D.

Appendix A

Exhibit	Description
Ex-1001	U.S. Patent No. 9,953,880 B1 to Lin et al. (“’880 Patent”).
Ex-1002	Prosecution File History of the ’880 Patent (“File History”).
Ex-1005	U.S. Pat. Appl. Pub. No. 2017/0054002 A1 to Doris et al. (“Doris”).
Ex-1006	U.S. Pat. Appl. Pub. No. 2016/0111524 A1 to Ha et al. (“Ha”).
Ex-1007	J.-P. Colinge, <i>FinFETs and Other Multi-Gate Transistors</i> (2008) (excerpted) (“Colinge”).
Ex-1008	U.S. Pat. No. 9,653,583 B1 to Zhao et al. (“Zhao”).
Ex-1009	U.S. Pat. Appl. Pub. No. 2017/0125411 A1 to Yu et al. (“Yu”).
Ex-1010	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted) (“Sze”).
Ex-1011	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted) (“Plummer”).
Ex-1012	M.-H. Chi, “Challenges in Manufacturing FinFET at 20nm Node and Beyond,” <i>Technology Development</i> , Global Foundries, Malta, NY, USA, 2012 (2012). (“Chi”).
Ex-1013	U.S. Patent No. 6,413,802 to Hu et al. (“Hu”).
Ex-1014	B. Doyle et al., <i>Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout</i> , Digest of the 2003 Symposium on VLSI Technology, pp. 133-34 (2003) (“Doyle”).
Ex-1015	U.S. Pat. No. 9,412,616 B1 to Xie et al. (“Xie616”).

Exhibit	Description
Ex-1016	U.S. Pat. Appl. Pub. No. 2015/0054078 A1 to Xie et al. (“Xie078”).
Ex-1017	U.S. Pat. Appl. Pub. No. 2017/0243790 A1 to Xie et al. (“Xie790”).
Ex-1018	Intel Newsroom, <i>Intel 22nm 3-D Tri-Gate Transistor Technology</i> , https://web.archive.org/web/20110507231236/http://newsroom.intel.com/docs/DOC-2032 (archived by the Internet Archive on May 7, 2011) (“Intel_Newsroom”).
Ex-1019	Intel Newsroom, <i>Intel Announces New 22nm 3D Tri-gate Transistors</i> , https://web.archive.org/web/20110516102045/http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Announcement_Presentation.pdf (archived by the Internet Archive on May 16, 2011) (“Intel_Announcement”).
Ex-1020	Intel Newsroom, <i>Intel’s Revolutionary 22 nm Transistor Technology</i> , https://web.archive.org/web/20110516103214/http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf (archived by the Internet Archive on May 16, 2011) (“Intel_22nm_Details”).
Ex-1021	U.S. Patent No. 6,881,631 B2 to Saito et al. (“Saito”).
Ex-1022	U.S. Patent No. 7,812,414 B2 to Hou et al. (“Hou”).
Ex-1023	U.S. Patent No. 6,849,511 B2 to Iriyama et al. (“Iriyama”).
Ex-1024	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007) (“Mistry_Paper”).

Exhibit	Description
Ex-1025	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007) (“Mistry_Presentation”).
Ex-1026	U.S. Pat. Appl. Pub. No. 2006/0081939 A1 to Akasaka et al. (“Akasaka”).
Ex-1027	U.S. Pat. Appl. Pub. No. 2007/0215950 A1 to Aoyama (“Aoyama”).
Ex-1028	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (2001) (excerpted) (“Quirk”).
Ex-1029	U.S. Pat. No. 9,947,540 to Tsai et al. (“Tsai”).
Ex-1030	U.S. Pat. Appl. No. 2018/0151445 A1 to Hsu et al. (“Hsu”).
Ex-1031	U.S. Pat. No. 6,458,686 B1 to Piao (“Piao”).
Ex-1033	S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET</i> (1995) (excerpted) (“Wolf3”).
Ex-1034	U.S. Pat. Appl. Pub. No. 2013/0140639 to Shieh et al. (“Shieh”).
Ex-1035	Complaint Under Section 337 of the Tariff Act of 1930, as Amended, <i>In re Certain Foreign-Fabricated Semiconductor Devices, Products Containing the Same, and Components Thereof</i> (Feb. 14, 2025) (“ITC Complaint”).

Appendix B

Claim 1	
[1pre]	A method for fabricating semiconductor device, comprising:
[1a]	forming a fin-shaped structure on a substrate;
[1b]	forming a shallow trench isolation (STI) around the fin-shaped structure;
[1c]	forming a gate layer on the fin-shaped structure and the STI;
[1d]	removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench;
[1e]	forming a dielectric layer into the trench to form a single diffusion break (SDB) structure; and
[1f]	after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure.
Claim 2	
The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.	
Claim 3	
The method of claim 2, further comprising: forming a patterned mask on the gate layer; and using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.	

Claim 4

The method of claim 1, further comprising: forming the dielectric layer into the trench and on the gate layer; and planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.

Claim 5

The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure.

Claim 6

The method of claim 5, further comprising: forming a cap layer on the gate structure and the SDB structure; and removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer adjacent to the SDB structure.

Claim 7

The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.

Claim 8

The method of claim 7, wherein the first direction is orthogonal to the second direction.

Claim 9

The method of claim 1, wherein the gate layer comprises amorphous silicon.

Claim 10

The method of claim 1, wherein the gate layer comprises polysilicon.

Claim 11

The method of claim 1, wherein the dielectric layer comprises silicon nitride.

Claim 12

The method of claim 1, wherein the dielectric layer comprises silicon oxide.