

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd., and Apple Inc.

Petitioners,

v.

Marlin Semiconductor Ltd.,

Patent Owner.

Patent No. 9,953,880 B2

Filing Date: July 27, 2017

Issue Date: April 24, 2018

Title: SEMICONDUCTOR DEVICE
AND METHOD FOR FABRICATING THE SAME

Inter Partes Review No. IPR2025-00848

PETITION FOR *INTER PARTES* REVIEW

TABLE OF CONTENTS

I.	RELIEF REQUESTED	1
II.	STATE OF THE ART	1
	A. Planar and Non-Planar FETs	1
	B. Bulk Silicon FinFETs vs. SOI FinFETs	2
	C. Diffusion Breaks	4
	D. Replacement Metal Gates	5
III.	THE '880 PATENT	7
	A. Overview	7
	B. Prosecution History	9
	C. Claim Construction	12
IV.	Ordinary Skill	13
V.	PRIOR ART	14
VI.	THE CHALLENGED CLAIMS ARE UNPATENTABLE	14
	A. Ground 1A: Doris and Ha Renders Claims 1-12 Obvious	14
	1. The Ground 1A Combination	18
	a. Doris expressly discloses a bulk silicon embodiment, which a POSITA would have known involves forming STI surrounding the fins.....	18
	b. A POSITA understood Doris's process flow as applied to a bulk silicon substrate	20
	c. A POSITA would have found it obvious that etching Doris's cavity 1202 would partially etch the STI in Doris's bulk silicon embodiment, as it does in Ha	22

2. Independent Claim 1	29
a. [1pre]: “[a] method for fabricating semiconductor device”	29
b. [1a]: “forming a fin-shaped structure on a substrate”	29
c. [1b]: “forming a shallow trench isolation (STI) around the fin-shaped structure”	30
d. [1c]: “forming a gate layer on the fin-shaped structure and the STI”	31
e. [1d]: “removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench”	33
f. [1e]: “forming a dielectric layer into the trench to form a single diffusion break (SDB) structure”	36
g. [1f]: “after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure”	38
3. Claim 2: “The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.”	40
4. Claim 3: “The method of claim 2, further comprising: forming a patterned mask on the gate layer; and using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.”	41
5. Claim 4: “The method of claim 1, further comprising: forming the dielectric layer into the trench and on the gate layer; and planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.”	41

6. Claim 5: “The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure.”	47
7. Claim 6: “The method of claim 5, further comprising: forming a cap layer on the gate structure and the SDB structure; and removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer adjacent to the SDB structure.”	49
8. Claim 7: “The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.”	51
9. Claim 8: “The method of claim 7, wherein the first direction is orthogonal to the second direction.”	52
10.Claim 9: “The method of claim 1, wherein the gate layer comprises amorphous silicon.”	52
11.Claim 10: “The method of claim 1, wherein the gate layer comprises polysilicon.”	52
12.Claim 11: “The method of claim 1, wherein the dielectric layer comprises silicon nitride.”	52
13.Claim 12: “The method of claim 1, wherein the dielectric layer comprises silicon oxide.”	53
B. Ground 1B: Doris and Ha, Further in View of Colinge, Renders Claims 1-12 Obvious	54
C. Grounds 2A and 2B: Ha Anticipates (Ground 2A) and Renders Obvious (Ground 2B) Claims 1-5, 7-8, and 10-11	54
1. Independent Claim 1	59
a. [1pre]	59
b. [1a] and [1b]	59

c. [1c]	61
d. [1d]	62
e. [1e]	64
f. [1f]	66
2. Claim 2	67
3. Claim 3	68
4. Claim 4	69
5. Claim 5	71
6. Claim 7	72
7. Claim 8	73
8. Claim 10	74
9. Claim 11	74
D. Ground 2C: The Combination of Ha and Zhao Renders Obvious	
Claim 9	74
1. A POSITA would have found it obvious to make Ha's sacrificial gate structures using amorphous silicon, as Zhao discloses	76
2. Claim 9	79
E. Ground 2D: The Combination of Ha and Yu Renders Obvious	
Claim 12	79
1. A POSITA would have found it obvious to make Ha's fin active core using silicon oxide, as Yu discloses	83
2. Claim 12	87
VII. TRIAL SHOULD BE INSTITUTED	87
VIII. MANDATORY NOTICES	90

A.	Real Parties-in-Interest.....	90
B.	Related Matters	90
C.	Lead and Back-Up Counsel	92
D.	Service Information	92
IX.	PAYMENT OF FEES	93
X.	GROUND FOR STANDING.....	93
XI.	CERTIFICATION UNDER 37 C.F.R. §42.24(d).....	93
XII.	CONCLUSION.....	93

TABLE OF AUTHORITIES

Cases

<i>3Shape A/S v. Align Tech., Inc.</i> , IPR2020-00223, Paper 12 (May 26, 2020).....	89
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, Paper 11 (Mar. 20, 2020)	88
<i>Beloit Corp. v. Valmet Oy</i> , 742 F.2d 1421 (Fed. Cir. 1984)	90
<i>Blackbird Tech LLC v. ELB Elecs., Inc.</i> , 895 F.3d 1374 (Fed. Cir. 2018)	10, 12
<i>Emerson Electric Co., v. Sipco, LLC</i> , IPR2019-00547, Paper 15 (Aug. 30, 2019).....	89-90
<i>Intel Corp. v. Qualcomm Inc.</i> , 21 F.4th 784 (Fed. Cir. 2021)	28, 45, 78, 86
<i>Intel Corp. v. XPP Schweiz AG</i> , 61 F.4th 1373 (Fed. Cir. 2023)	28, 45, 78, 86
<i>KSR Int’l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	<i>passim</i>
<i>Medrad, Inc. v. MRI Devices Corp.</i> , 401 F.3d 1313 (Fed. Cir. 2005)	12
<i>Philip Morris Products, S.A. v. Rai Strategic Holdings, Inc.</i> , IPR2020-00921, Paper 13 (Aug. 5, 2021)	13
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (en banc)	12, 13
<i>SharkNinja v. iRobot Corp.</i> , IPR2021-00545, Paper 11 (Sept. 8, 2021).....	88

Statutes

35 U.S.C. § 102..... *passim*

35 U.S.C. § 103 1

Rules

37 C.F.R. §42.24(d) 93

TABLE OF EXHIBITS

Exhibit	Description
Ex-1001	U.S. Patent No. 9,953,880 B1 to Lin et al. (“’880 Patent”).
Ex-1002	Prosecution File History of the ’880 Patent.
Ex-1003	Declaration of Dr. Suman Datta, Ph.D.
Ex-1004	Curriculum Vitae of Dr. Suman Datta, Ph.D.
Ex-1005	U.S. Pat. Appl. Pub. No. 2017/0054002 A1 to Doris et al. (“Doris”).
Ex-1006	U.S. Pat. Appl. Pub. No. 2016/0111524 A1 to Ha et al. (“Ha”).
Ex-1007	J.-P. Colinge, <i>FinFETs and Other Multi-Gate Transistors</i> (2008) (excerpted) (“Colinge”).
Ex-1008	U.S. Pat. No. 9,653,583 B1 to Zhao et al. (“Zhao”).
Ex-1009	U.S. Pat. Appl. Pub. No. 2017/0125411 A1 to Yu et al. (“Yu”).
Ex-1010	S.M. Sze, <i>Physics of Semiconductor Devices</i> (2d ed. 1981) (excerpted).
Ex-1011	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted).
Ex-1012	M.-H. Chi, “Challenges in Manufacturing FinFET at 20nm Node and Beyond,” <i>Technology Development</i> , Global Foundries, Malta, NY, USA, 2012 (2012).
Ex-1013	U.S. Patent No. 6,413,802 to Hu et al.

Exhibit	Description
Ex-1014	B. Doyle et al., <i>Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout</i> , Digest of the 2003 Symposium on VLSI Technology, pp. 133-34 (2003).
Ex-1015	U.S. Pat. No. 9,412,616 B1 to Xie et al.
Ex-1016	U.S. Pat. Appl. Pub. No. 2015/0054078 A1 to Xie et al.
Ex-1017	U.S. Pat. Appl. Pub. No. 2017/0243790 A1 to Xie et al.
Ex-1018	Intel Newsroom, <i>Intel 22nm 3-D Tri-Gate Transistor Technology</i> , https://web.archive.org/web/20110507231236/http://newsroom.intel.com/docs/DOC-2032 (archived by the Internet Archive on May 7, 2011).
Ex-1019	Intel Newsroom, <i>Intel Announces New 22nm 3D Tri-gate Transistors</i> , https://web.archive.org/web/20110516102045/http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Announcement_Presentation.pdf (archived by the Internet Archive on May 16, 2011).
Ex-1020	Intel Newsroom, <i>Intel's Revolutionary 22 nm Transistor Technology</i> , https://web.archive.org/web/20110516103214/http://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf (archived by the Internet Archive on May 16, 2011).
Ex-1021	U.S. Patent No. 6,881,631 B2 to Saito et al.
Ex-1022	U.S. Patent No. 7,812,414 B2 to Hou et al.
Ex-1023	U.S. Patent No. 6,849,511 B2 to Iriyama et al.

Exhibit	Description
Ex-1024	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” Technical Digest of the of the 2007 IEEE International Electron Devices Meeting (IEDM), pp. 247-50 (Dec. 2007).
Ex-1025	K. Mistry, et al., “A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging,” presented at 2007 IEEE International Electron Devices Meeting (IEDM), pp. 1-37 (Dec. 2007).
Ex-1026	U.S. Pat. Appl. Pub. No. 2006/0081939 A1 to Akasaka et al.
Ex-1027	U.S. Pat. Appl. Pub. No. 2007/0215950 A1 to Aoyama.
Ex-1028	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> (2001) (excerpted).
Ex-1029	U.S. Pat. No. 9,947,540 to Tsai et al.
Ex-1030	U.S. Pat. Appl. No. 2018/0151445 A1 to Hsu et al.
Ex-1031	U.S. Pat. No. 6,458,686 B1 to Piao.
Ex-1032	Declaration of Shauna Wiest in support of public availability of Colinge (2008).
Ex-1033	S. Wolf, <i>Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET</i> (1995) (excerpted).
Ex-1034	U.S. Pat. Appl. Pub. No. 2013/0140639 to Shieh et al.

Exhibit	Description
Ex-1035	Complaint Under Section 337 of the Tariff Act of 1930, as Amended, <i>In re Certain Foreign-Fabricated Semiconductor Devices, Products Containing the Same, and Components Thereof</i> (Feb. 14, 2025).

***NOTE:** All citations herein to page numbers identify the stamped page numbers of the cited exhibit, not the page numbers of the original reference.

LIST OF CHALLENGED CLAIMS

Claim 1	
[1pre]	A method for fabricating semiconductor device, comprising:
[1a]	forming a fin-shaped structure on a substrate;
[1b]	forming a shallow trench isolation (STI) around the fin-shaped structure;
[1c]	forming a gate layer on the fin-shaped structure and the STI;
[1d]	removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench;
[1e]	forming a dielectric layer into the trench to form a single diffusion break (SDB) structure; and
[1f]	after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure.
Claim 2	
The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.	
Claim 3	
The method of claim 2, further comprising: forming a patterned mask on the gate layer; and using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.	

Claim 4

The method of claim 1, further comprising: forming the dielectric layer into the trench and on the gate layer; and planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.

Claim 5

The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure.

Claim 6

The method of claim 5, further comprising: forming a cap layer on the gate structure and the SDB structure; and removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer adjacent to the SDB structure.

Claim 7

The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.

Claim 8

The method of claim 7, wherein the first direction is orthogonal to the second direction.

Claim 9

The method of claim 1, wherein the gate layer comprises amorphous silicon.

Claim 10

The method of claim 1, wherein the gate layer comprises polysilicon.

Claim 11

The method of claim 1, wherein the dielectric layer comprises silicon nitride.

Claim 12

The method of claim 1, wherein the dielectric layer comprises silicon oxide.

I. RELIEF REQUESTED

Applying the following grounds, Co-Petitioners request *inter partes* review of the '880 Patent¹ and cancellation of claims 1-12:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A	1-12	103	Doris, Ha
1B	1-12		Doris, Ha, Colinge
2A/2B	1-5, 7-8, 10-11	102/103	Ha
2C	9	103	Ha, Zhao
2D	12		Ha, Yu

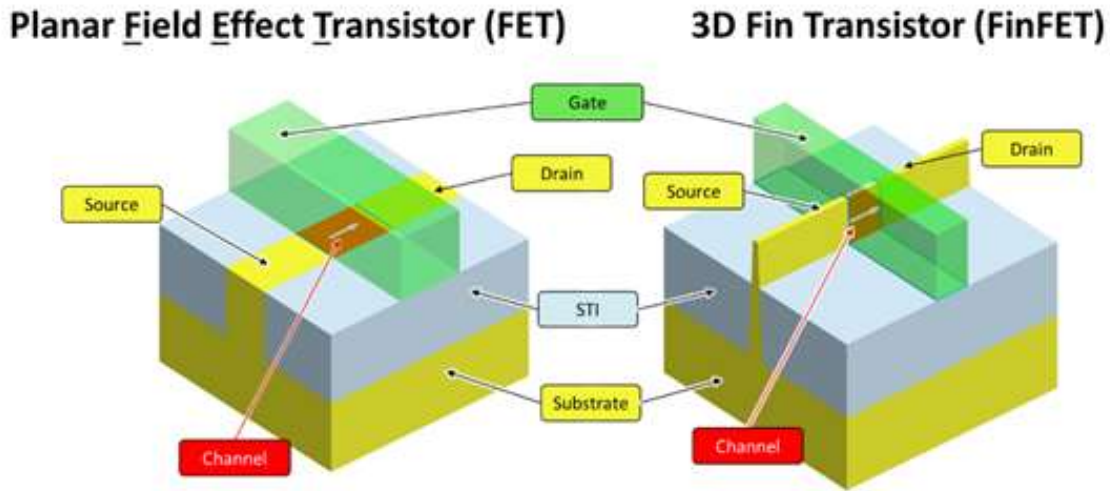
II. STATE OF THE ART

The '880 Patent describes a method for dividing fin-shaped metal-insulator-semiconductor field-effect transistors (“FinFETs”) with a single diffusion break (“SDB”). Such methods were already known.

A. Planar and Non-Planar FETs

FETs are switches operated by voltage applied to a “gate” between “source” and “drain” regions. (Ex-1003 ¶42; Ex-1010, 9-10; Ex-1011, 11-22.) When turned on, current flows between the source and drain regions through a “channel” operated by the gate. (Ex-1003 ¶42; Ex-1010, 9-10, 14; Ex-1011, 11-16.) The figures below show a planar FET and a non-planar FinFET. (Ex-1003 ¶41.)

¹ U.S. Patent No. 9,953,880 (Ex-1001).

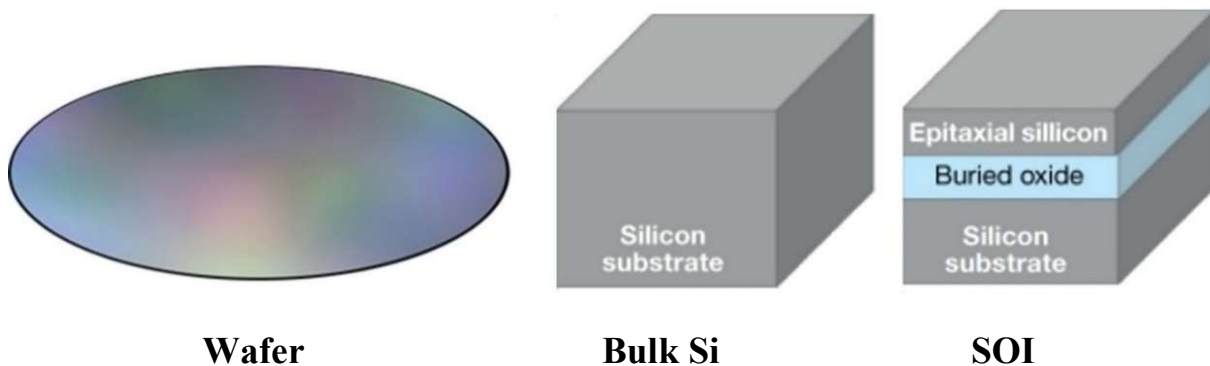


Ex-1003 ¶41

Basic operation of both is the same. (Ex-1003 ¶¶42-43.) Except for creating a fin in the latter, their fabrication is also generally the same. (Ex-1003 ¶44; *see* Ex-1012, 1; Ex-1013, Abstract, 2:11-14, 5:37-40; Ex-1014, 1.)

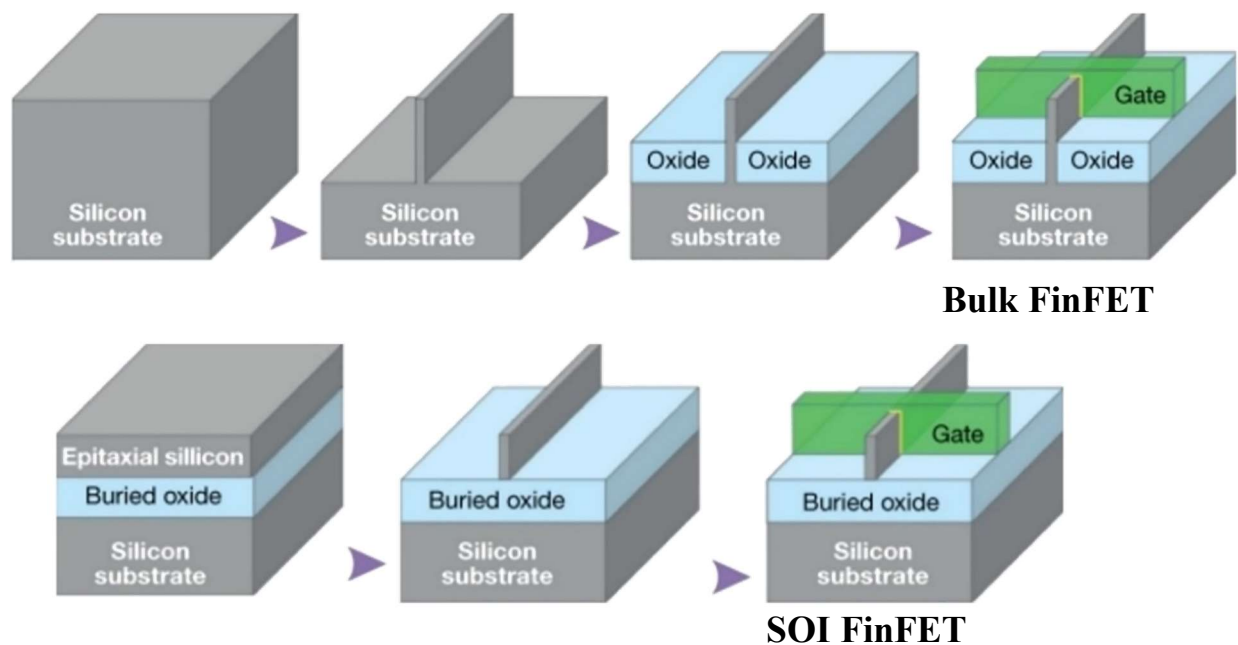
B. Bulk Silicon FinFETs vs. SOI FinFETs

Semiconductor substrates are typically wafers. (Ex-1003 ¶46.) A bulk silicon wafer is made of silicon, whereas a silicon-on-insulator (“SOI”) wafer further includes a buried oxide layer. (Ex-1003 ¶47.)



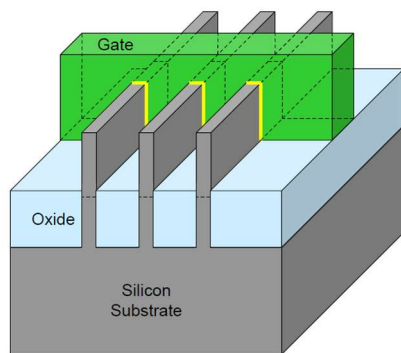
Ex-1003 ¶47

Because of this, SOI FinFETs and bulk silicon FinFETs differ slightly: the former includes oxide *underlying* the fins whereas the latter includes shallow trench isolation (“STI”) oxide *surrounding* the fins. (Ex-1003 ¶48; *see* Colinge, 22-23, 37-38, Figs. 2.2, 2.14.) After forming the initial fins and isolation oxide, the same basic process flow generally can be applied to either substrate type. (Ex-1003 ¶48; *see* Ex-1012, 1-2, Fig. 1; Zhao, 5:29-34; Ex-1015, 7:41-48; Ex-1016 ¶[0027]; Ex-1017 ¶[0021].)

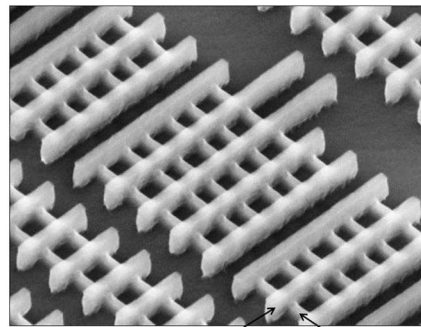


Ex-1003 ¶48

Ever since commercial FinFETs debuted in 2011 (see below), bulk silicon FinFETs have been routine and more prevalent than SOI FinFETs. (*See* Ex-1018, 1; Ex-1019, 5, 8, 10-12, 16, 24; Ex-1020, 2, 5-10, 14, 22-23, 27; Ex-1003 ¶49.)



Ex-1020, 7

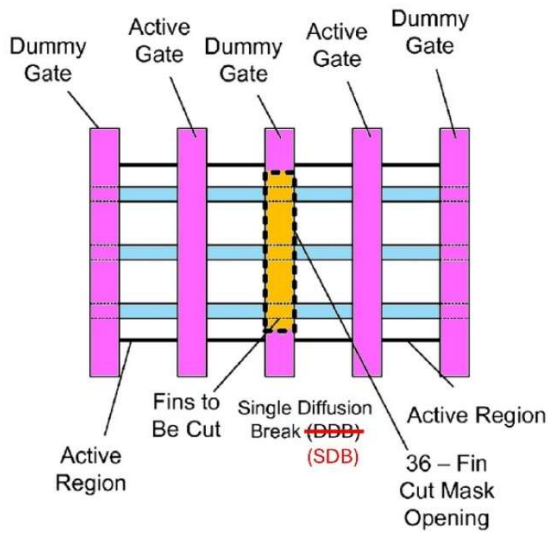


Ex-1020, 8

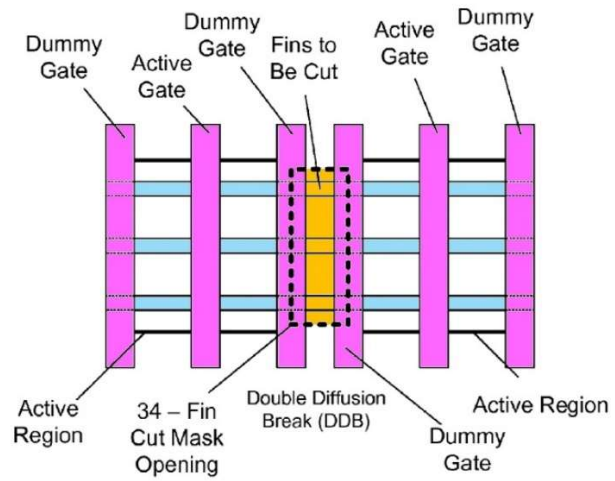
C. Diffusion Breaks

In a FinFET integrated circuit, fins are initially formed as long strips over large areas. (Ex-1015, 2:62-64; Ex-1003 ¶50.) Those long strips are then “cut” by trenches filled with an insulating material (silicon oxide or nitride), yielding shorter strips suitable for transistors. (Ex-1015, 2:48-3:4; Ex-1003 ¶¶50-51.) These fin-cutting structures are called “diffusion breaks.” (Ex-1015, 2:48-54; Ex-1003 ¶51.)

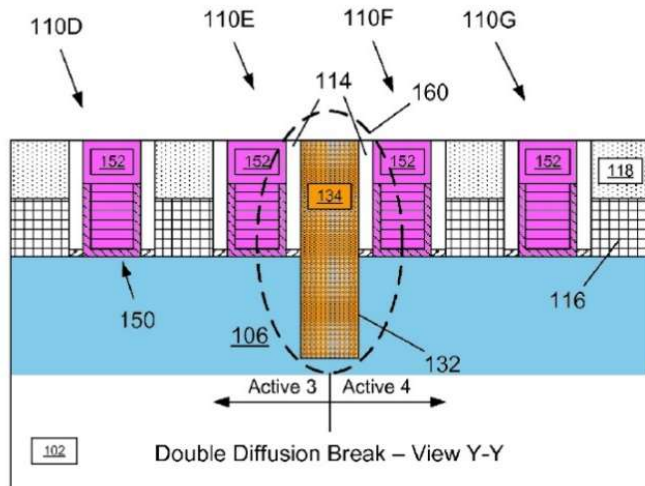
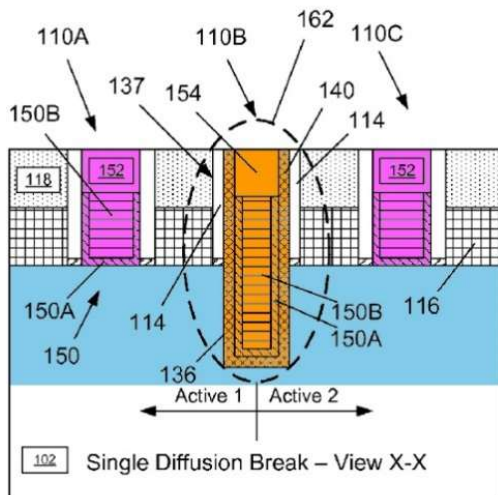
Single diffusion breaks (“SDBs”) and double diffusion breaks (“DDBs”) were common before the ’880 Patent. (Ex-1015, 3:42-59, FIGS. 1C-1H; Ex-1003 ¶52.) Below, the fins (blue) run horizontally; gate structures (magenta) run vertically; and diffusion breaks are orange. (Ex-1015, FIGS. 1E, 1H; Ex-1003 ¶52.) The SDB lies adjacent to source/drain regions 116, whereas the DDB lies adjacent to dummy gates 152. (Ex-1003 ¶¶52-53.)



Ex-1015, FIG. 1H² (corrected)



Ex-1015, FIG. 1E



Ex-1015, FIG. 2S

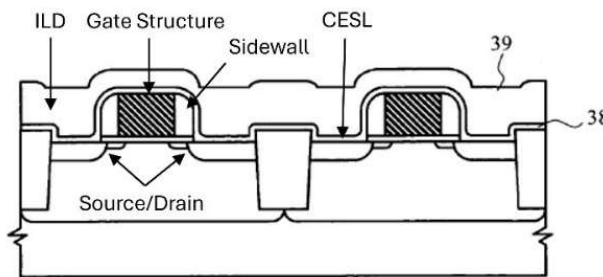
D. Replacement Metal Gates

In highly scaled transistors, polysilicon gates are not viable. (Ex-1021, 1:24-34; Ex-1022, 1:25-44.) They require metal gates. (Ex-1021, 1:31-34; Ex-1023,

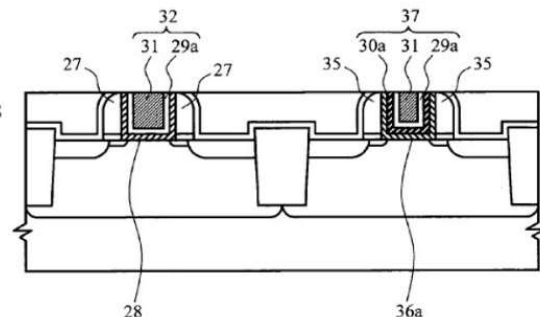
² Coloring has been added throughout for emphasis.

1:28-34, 1:41-42; Ex-1024, 1; Ex-1025, 14-25, 45; Ex-1003 ¶54.) Suitable metals for n-type devices were known, but options for p-type devices exhibited less thermal stability. (Ex-1022, 1:45-57; Ex-1023, 1:41-48.) The solution was **replacement** metal gates, a gate-last process that avoids subjecting sensitive metals to high temperatures. (Ex-1023, 2:22-29; Ex-1003 ¶55.) This technology debuted commercially in 2007 and quickly became ubiquitous. (Ex-1024, 1; Ex-1025, 14-25, 45; Ex-1003 ¶56.)

In a typical replacement metal gate process, insulating films (“CESL” and “ILD” below) are planarized to expose “dummy” gates, which are removed and replaced with a high-k gate dielectric film (28/36a) and metal layers (29a/30a/31). (Ex-1026 ¶¶[0079]-[0089], FIGS. 11D-12; *see* Ex-1027 ¶¶[0113]-[0119], FIGS. 6K-6Q; Ex-1025, 17-25; Ex-1003 ¶57.)



Ex-1026, FIG. 11C (annotated)



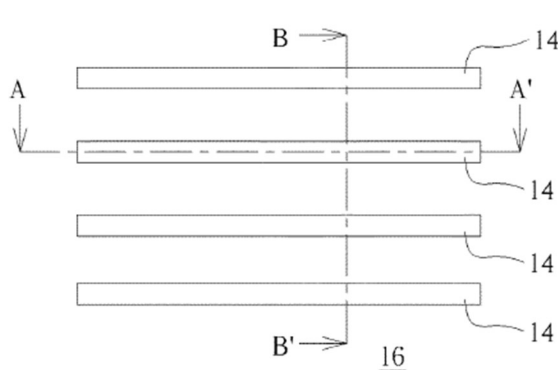
Ex-1026, FIG. 12

Commercial FinFETs have used replacement metal gates since they debuted. (Ex-1020, 23; Ex-1015, 3:6-10; Ex-1003 ¶58.)

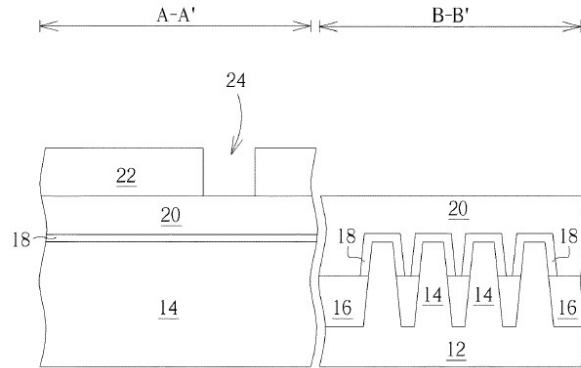
III. THE '880 PATENT

A. Overview

The '880 Patent describes how to make FinFETs with a “single diffusion break (SDB).” (Ex-1001, 1:10-13.)

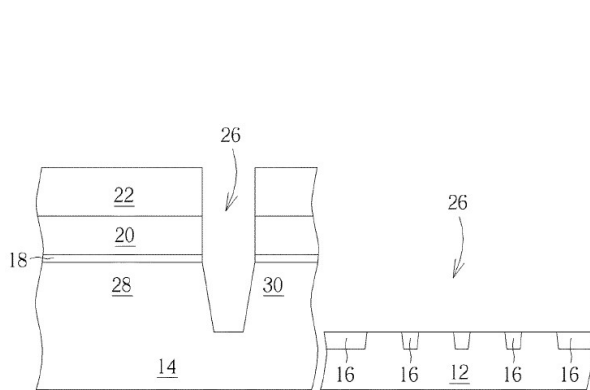


Ex-1001, FIG. 1

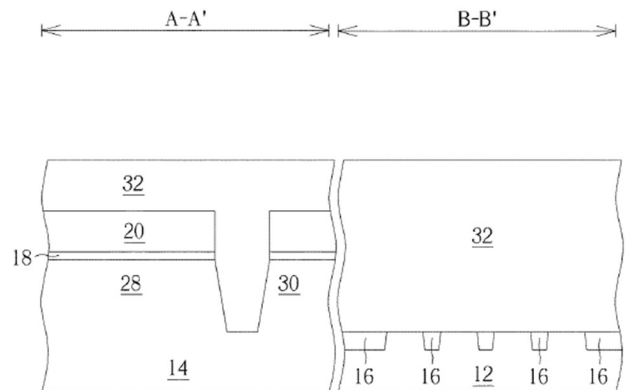


Ex-1001, FIG. 2

FIGS. 1-2 above show fin-shaped structures 14 formed on substrate 12, then surrounded by “shallow trench isolation (STI) 16.” (*Id.*, 2:9-21, 2:59-60; *see id.*, 2:27-58.) “[A] gate dielectric layer 18 and a gate layer 20 are formed to cover the fin-shaped structures 14 and the STI 16 entirely, and a patterned mask 22 is formed on the gate layer 20.” (*Id.*, 3:3-7.) Opening 24 exposes part of gate layer 20. (*Id.*)

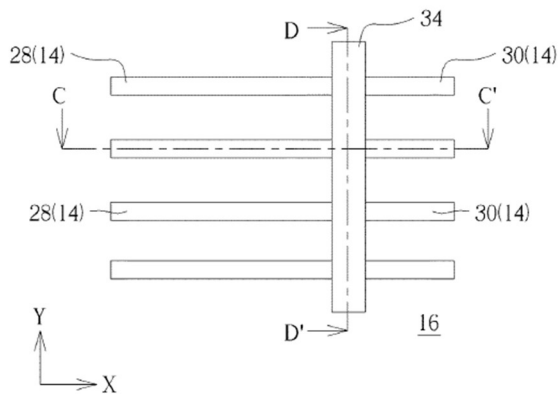


Ex-1001, FIG. 3



Ex-1001, FIG. 4

FIG. 3 above shows a trench 26 etched through opening 24 to cut into fins 14, and dielectric layer 32 is deposited to fill trench 26 as in FIG. 4. (*Id.*, 3:17-38.) Then, as FIGS. 5 and 6 show, dielectric layer 32 is planarized, leaving “SDB” structure 34 in trench 26.³ (*Id.*, 3:39-59.)



Ex-1001, FIG. 5

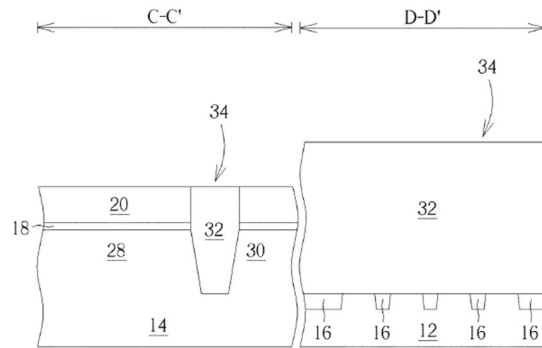
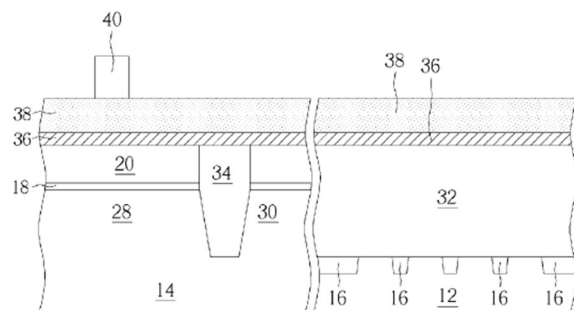


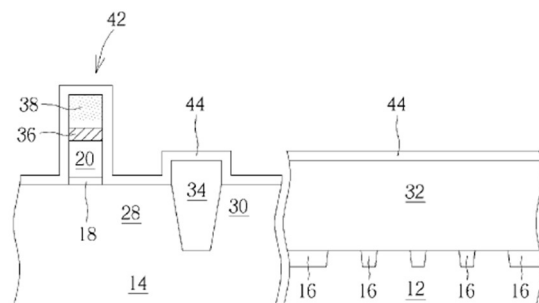
FIG. 6

Ex-1001, FIG. 6

Next, as FIG. 7 shows, mask 40 overlays hard masks 36 and 38. (*Id.*, 3:60-4:7.) Etching forms gate structure 42 (*id.*, 4:8-29), and cap layer 44 “is formed to cover the gate structure 42 and the SDB structure 34,” as in FIG. 8 (*id.*, 4:29-34).



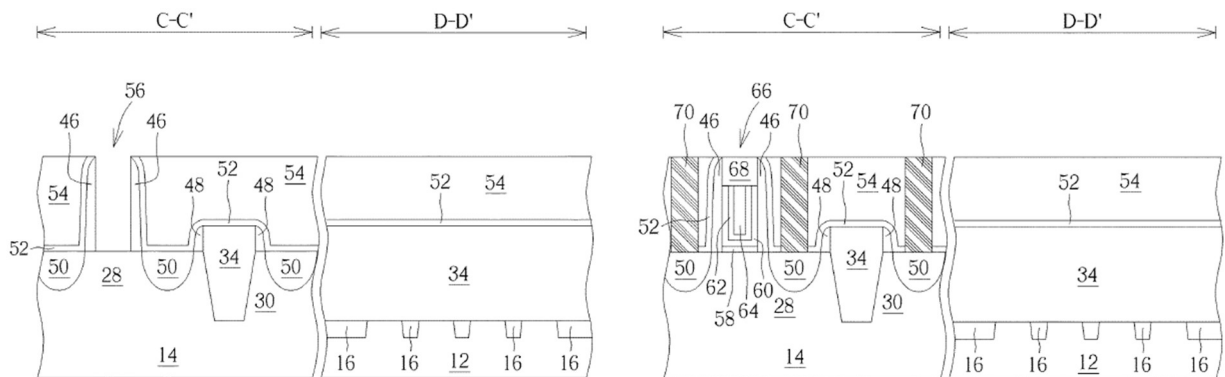
Ex-1001, FIG. 7



Ex-1009, FIG. 8

³ Dielectric layer 32 on the right side of FIG. 6 is too high. It should be coplanar with gate layer 20. (See Ex-1001, 3:44-48, FIG. 4; Ex-1003 ¶62 & n.7, ¶195 n.15.)

After anisotropic etching, part of cap layer 44 remains on the sidewalls of gate structure 42 and SDB 34, leaving first and second spacers 46 and 48, respectively. (*Id.*, 4:35-39.) Contact etch stop layer (“CESL”) 52 and interlayer dielectric (“ILD”) layer 54 are then deposited and planarized to expose gate layer 20. (*Id.* 4:59-67.) Gate layer 20 is removed, leaving recess 56, as in FIG. 9. (*Id.*, 5:1-10.) As FIG. 10 shows, a replacement metal gate forms in recess 56. (*Id.*, 5:11-63.)



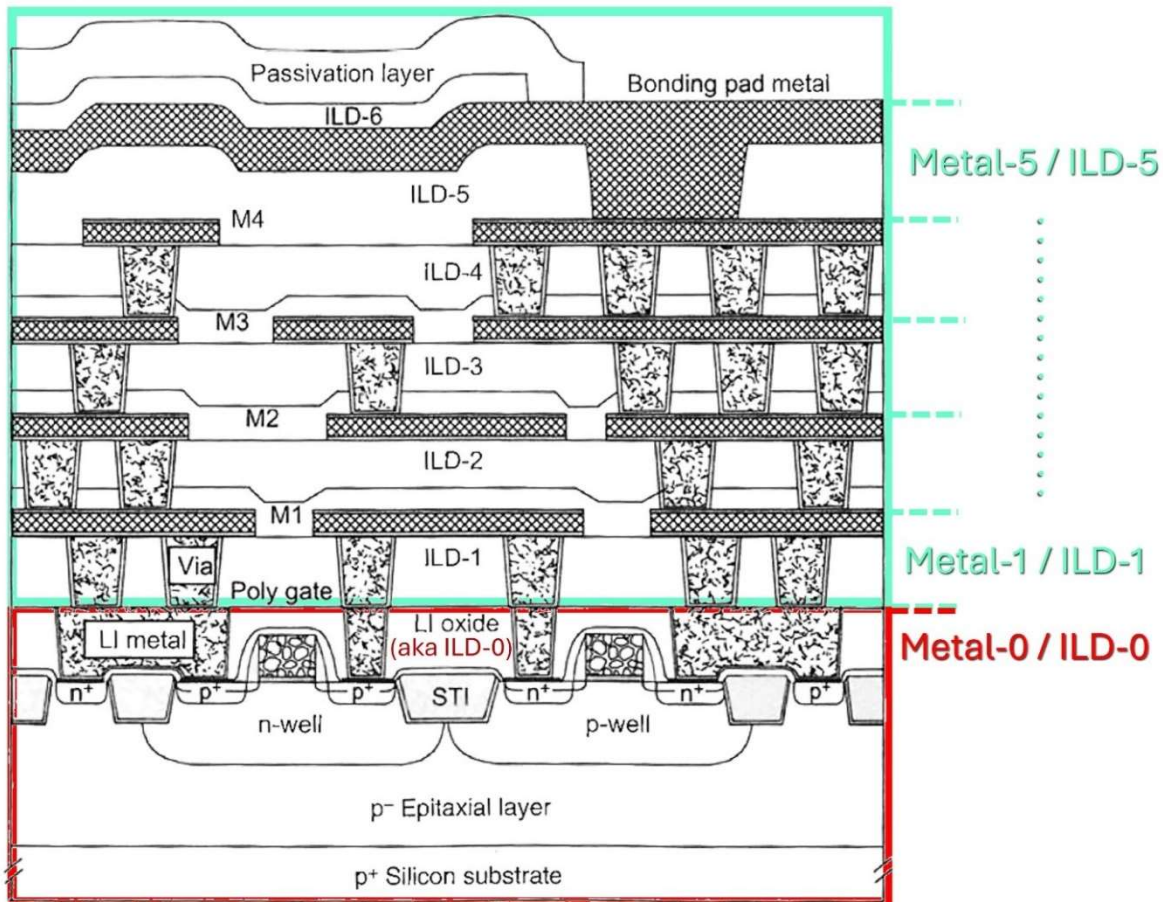
Ex-1001, FIG. 9

Ex-1001, FIG. 10

B. Prosecution History

The Examiner rejected the original claims over Xie790 (Ex-1017). (Ex-1002, 83-89.) The Applicant did not challenge the Examiner’s findings. (*Id.*, 104-05.) Instead, the Applicant further limited independent claim 1 by adding: “after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure” (*id.*, 99), arguing that Xie790 is distinguishable because it disclosed forming the ILD layer **before** the SDB, not **after** (*id.*, 104). The Examiner allowed the amended claim, stating that “the reasons for allowance are in all probability

evident from the record and no statement is deemed necessary” based on “the substance of applicants’ remarks.” (*Id.*, 112.)



Ex-1028, Fig. 9.29 (annotated)

To understand this exchange, it must be viewed in context. (*See Blackbird Tech LLC v. ELB Elecs., Inc.*, 895 F.3d 1374, 1378 (Fed. Cir. 2018) (prosecution history understood from the perspective of a POSITA).) A POSITA would have understood a basic textbook concept: In addition to the ILD layer at the transistor level (like “ILD-0” above and the ILD layer at issue in prosecution), integrated circuits have additional ILD layers (analogous to “ILD-1” through “ILD-6” above)

formed above the transistor level, between each metal layer. (Ex-1028, 22; *see id.*, 20-27, Figs. 9.21-9.29; Ex-1003 ¶70.)

In Xie790, the *lowest* ILD layer (analogous to “ILD-0” above) is formed *before* the SDB structure. (Ex-1017 ¶[0023], ¶[0029], FIGS. 2A, FIG. 2G; *see* Ex-1015, 8:49-53, 11:1-13, FIGS. 2B, 2N; Ex-1034 ¶[0022], ¶¶[0034]-[0035], FIGS. 3-6; Ha ¶[0098], ¶¶[0110]-[0111], FIGS. 4A-4B, 9A-9C; Ex-1003 ¶71.) But because Xie790 “relates to the fabrication of integrated circuits,” a POSITA would have understood *additional* ILD layers—like ILD-1 through ILD-6 above—would be formed *after* (and on) Xie790’s SDB structure. (Ex-1017 ¶[0002]; *see* Ex-1028, 20-27, Figs. 9.21-9.29; Ha ¶¶[0077]-[0080], ¶¶[0122]-[0125], FIGS. 2A-2C; Ex-1003 ¶¶71-76.)

Thus, if the claimed step of “forming an interlayer dielectric (ILD) layer on the SDB structure” referred to forming anything other than the *lowest* ILD layer (the one at the transistor level, labeled “LI oxide” above and sometimes called “ILD-0”), the alleged distinction over Xie790 during prosecution would have been illusory. (Ex-1003 ¶¶71-76 (discussing Ex-1028, Fig. 9.29; Ex-1029, 8:23-39, 13:13-32, 13:51-55, FIGS. 9-10, 17; Ex-1030 ¶[0015], ¶[0023], ¶[0025], FIG. 6; Ex-1031, 1:25-43).) Indeed, the lowest ILD layer is the *only* ILD layer the ’880 Patent and Xie790 expressly describe and the *only* ILD layer discussed during prosecution. (*See id.* ¶75; Ex-1002, 104; Ex-1001, 4:59-5:10, 5:64-6:11; Ex-1017 ¶¶[0023]-[0024].)

C. Claim Construction

Claim construction does not take place in vacuum. “Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history.” (*Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005); *accord Phillips v. AWH Corp.*, 415 F.3d 1303, 1313, 1317 (Fed. Cir. 2005) (en banc).)

According to Patent Owner, “the ’880 Patent recognized that the method of forming SDB structures could be improved by performing the SDB trench etching step after the formation of the polysilicon gate layer and before the final metal gate formation.” (Ex-1035 ¶89 (citing Ex-1001, 3:3-5:10).) Applying this broad view, Patent Owner’s litigation allegations suggest that “forming an interlayer dielectric (ILD) layer” after and on the SDB structure (claim 1) should encompass forming *any* ILD layer, not just the *lowest* one, after and on the SDB. As the preceding subsection explains, Patent Owner’s position undermines the prosecution history and would vitiate the only allegedly distinguishing feature. (*See Blackbird*, 895 F.3d at 1378-79 (“We look at what an ordinarily skilled artisan would understand about claim scope from reading the prosecution history.”); *supra* §III.B; Ex-1028, Fig. 9.29.) Co-Petitioners disagree with that view.

This Petition presents two sets of Grounds—one based on Doris (Grounds 1A-1B) and one based on Ha (Grounds 2A-2D). The Ha grounds are based

on Patent Owner’s view of the claims, which regards claim 1 as encompassing **any** ILD layer formed after and on the SDB. (*See Philip Morris Products, S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00921, Paper 13, at 42-44 (Aug. 5, 2021) (explaining petitioner may “rely[] on claim constructions that it believes are incorrect”).) The Doris grounds also satisfy the Challenged Claims under Patent Owner’s view. But they also satisfy the Challenged Claims under the view that most naturally aligns with the specification and prosecution history. (*See, e.g., Phillips*, 415 F.3d at 1316.) For example, Doris’s **lowest** ILD layer is formed after and on the SDB. If the Board finds the Challenged Claims unpatentable based on the Doris grounds, it need not reach the claim construction issue.

IV. ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor device manufacturing, such as, for example, in integrated circuit device (or transistor) design and/or manufacturing, as of June 29, 2017. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for less formal education. (Ex-1003 ¶38.)

V. PRIOR ART

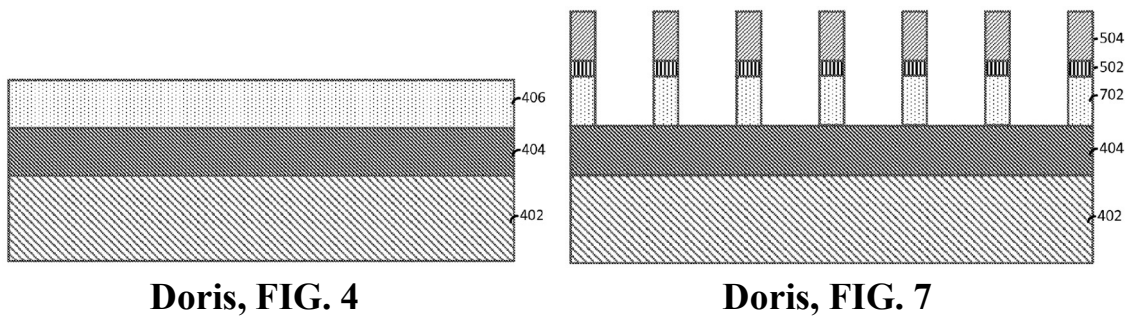
Reference	Effective Filing	Published/Available	AIA Qualification
Doris (Ex-1005)	August 20, 2015	February 23, 2017	§§102(a)(1), (a)(2)
Ha (Ex-1006)	October 17, 2014	April 21, 2016	§§102(a)(1), (a)(2)
Colinge (Ex-1007)	N/A	~August 23, 2007	§102(a)(1)
Zhao (Ex-1008)	August 2, 2016	May 16, 2017	§§102(a)(1), (a)(2)
Yu (Ex-1009)	November 4, 2015	May 4, 2017	§§102(a)(1), (a)(2)

VI. THE CHALLENGED CLAIMS ARE UNPATENTABLE

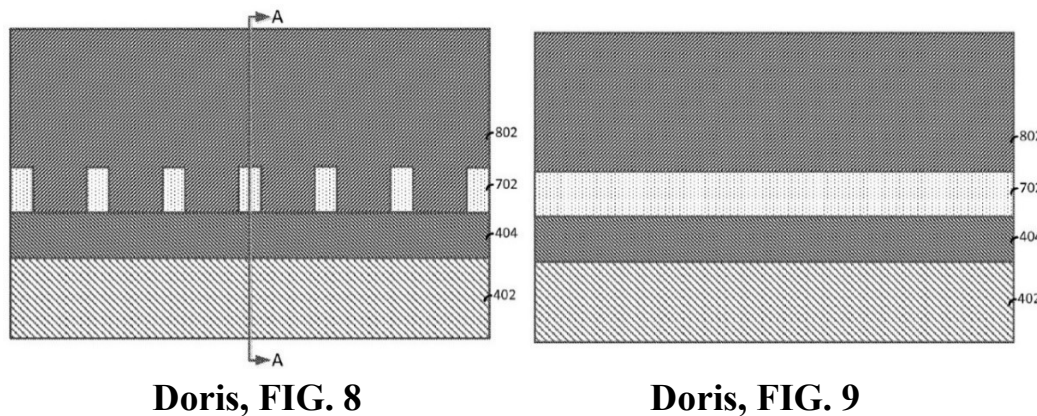
A. Ground 1A: Doris and Ha Renders Claims 1-12 Obvious

Doris discloses FinFET manufacturing methods. (Doris, Abstract, ¶[0001].) Doris begins with a substrate. (*Id.* ¶[0043], FIG. 4.) Although FIG. 4 depicts an SOI substrate comprising silicon layer 402, insulator layer 404, and semiconductor layer 406, Doris explains “alternate exemplary embodiments may include a **bulk silicon** ... arrangement.” (*Id.* ¶[0043] (emphasis added); *see id.* ¶[0040] (similar).)

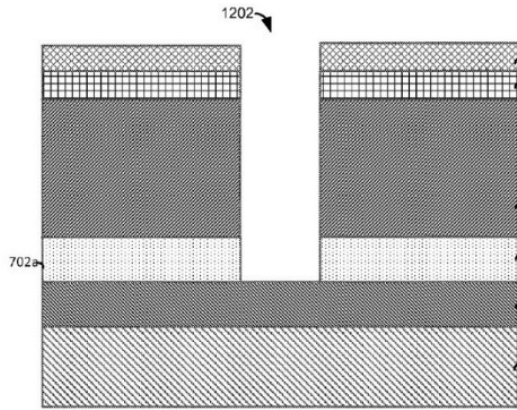
After patterning an oxide layer 502 and nitride hardmask layer 504 into strips, an etch of semiconductor layer 406 yields fins 702. (Doris ¶¶[0044]-[0046]; *see id.*, FIGS. 4-7.) Oxide layer 502 and hardmask layer 504 are then removed. (*Id.* ¶[0047].)



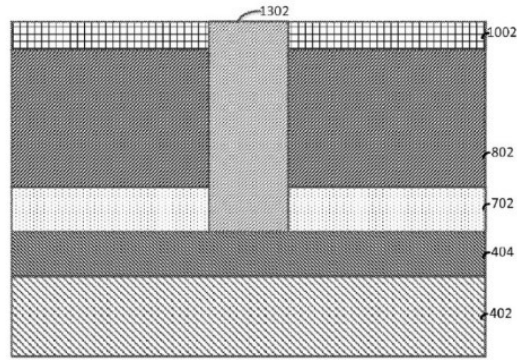
Next, “a layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 and insulator layer 404.” (*Id.* ¶[0047].) An amorphous silicon (α -Si) or polysilicon layer 802 is then deposited over fins 702 and insulator layer 404. (*Id.* ¶[0047], FIGS. 8-9.) Below, FIG. 8 shows how this appears when looking down fins 702; FIG. 9 depicts cross-section A–A of FIG. 8. (*Id.*)



A hardmask layer 1002 is formed over the wafer. (*Id.* ¶[0048], FIG. 10.) Using photolithographic mask 1102 with a striped opening perpendicular to the fins, hardmask layer 1002 is patterned. (*Id.* ¶[0049], FIGS. 11, 14.) Anisotropic etching creates a cavity 1202 that cuts the fins, as FIG. 12 shows in cross-section below. (*Id.* ¶[0050].) Cavity 1202 is filled with insulator material 1302 comprising “an oxide or a nitride material,” then planarized as in FIG. 13. (*Id.* ¶[0051].)

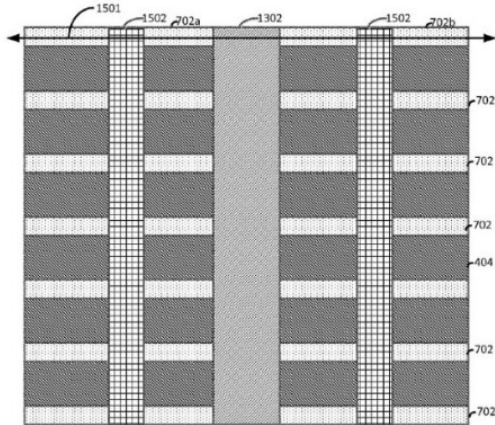


Doris, FIG. 12

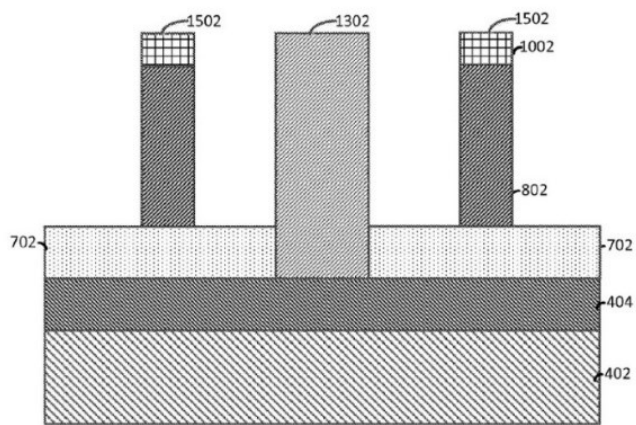


Doris, FIG. 13

Next, the structure is patterned to define dummy gates 1502. “[D]ummy gate stacks 1502 define channel regions of the fins 702” and “may be formed using a suitable lithographic patterning and etching process.” (*Id.* ¶[0052].) As FIG. 15 shows in plan view, fins 702 run horizontally, whereas insulator material 1302 and dummy gates 1502 run vertically. (*Id.* ¶[0052].) FIG. 16 below shows the structure in cross-section along arrow 1501. (*Id.* ¶¶[0052]-[0053].)



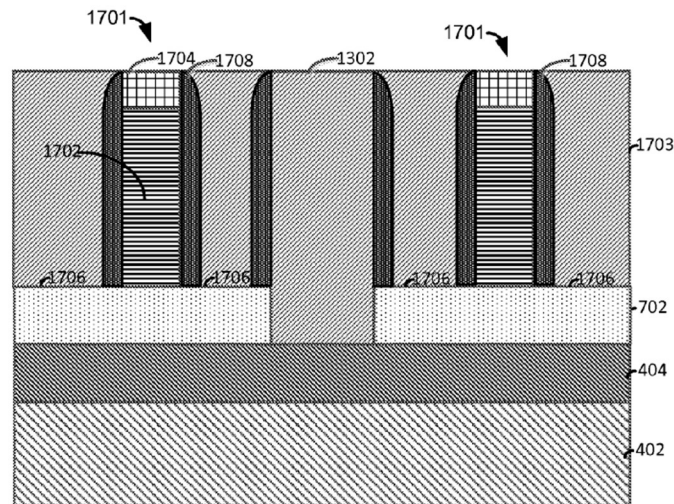
Doris. FIG. 15



Doris. FIG. 16

Spacers 1708 are then formed on dummy gate stacks 1502 and insulator material 1302, and active regions 1706 (source/drain regions) are formed adjacent

to dummy gates 1502 and insulator material 1302. (*Id.* ¶[0054], FIG. 17.) An insulator 1703 (e.g., oxide) then fills the space over active regions 1706 and is planarized. (*Id.*) Lastly, dummy gates 1502 are replaced with metal gate structures 1701, as FIG. 17 shows below. (*Id.*)



Doris, FIG. 17

Because Doris is in the same field (FinFETs) and reasonably pertinent to a problem the '880 Patent purports to address (FinFET fabrication), Doris is analogous art. (*See* Ex-1001, 1:9-67; Doris ¶¶[0001]-[0003]; Ex-1003 ¶82.)

Ground 1A involves only trivial, textbook variations of Doris that would have been obvious, as evidenced by Ha. First, Ground 1A implements Doris's expressly disclosed "bulk silicon ... arrangement" (Doris ¶[0043]), meaning simply that fin isolation regions 404 would not be buried under the fins, but would be an STI surrounding them. (*Supra* §II.B; *infra* §§VI.A.1.a-b.) That difference is trivial—in fact, textbook. Using a bulk silicon substrate would not alter any other aspect of

Doris's structure or process flow. (Ex-1003 ¶140.) Second, Ground 1A involves removing some of Doris's STI when cutting the fins—an obvious and borderline inherent consequence of removing one oxide layer (dummy gate oxide) from directly above another oxide layer (STI). (*Infra* §VI.A.1.c; Ex-1003 ¶141.) Again, this is textbook.

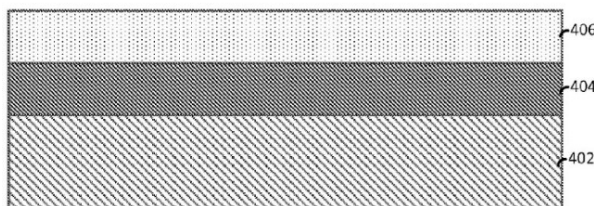
1. The Ground 1A Combination

- a. **Doris expressly discloses a bulk silicon embodiment, which a POSITA would have known involves forming STI surrounding the fins**

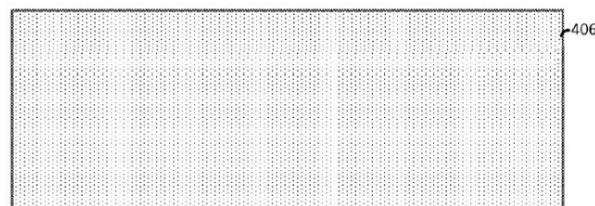
Doris explains:

FIGS. 4-18 illustrate an exemplary method of forming a finFET device having stressed fins. ... The illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement, however *alternate exemplary embodiments may include a bulk silicon . . . arrangement.*

(Doris ¶[0043] (emphasis added); *see id.* ¶[0040] (“The substrate 101 may include, a bulk silicon substrate, [or] a silicon on insulator substrate ...”).) Thus, Doris expressly discloses applying its process to bulk silicon.



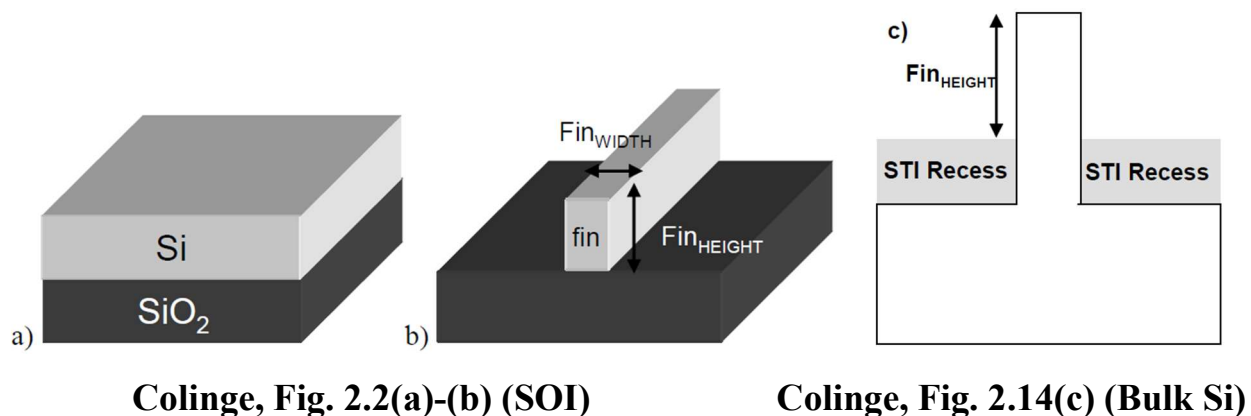
Doris, FIG. 4 (SOI)



Alternative FIG. 4 (Bulk Si)

A POSITA would have understood Doris's bulk silicon arrangement involves forming STI around the fins. (*Supra* §II.B; Ex-1003 ¶¶142-143; Ha ¶¶0093, FIGS. 3A-3B.) Doris's FIG. 4 shows an SOI substrate comprising silicon layer 402, insulator layer 404, and semiconductor layer 406. (Doris ¶¶0043.) A bulk silicon substrate would just be a silicon wafer. (*See id.*, ¶¶0040, ¶¶0043; Ex-1003 ¶144.)

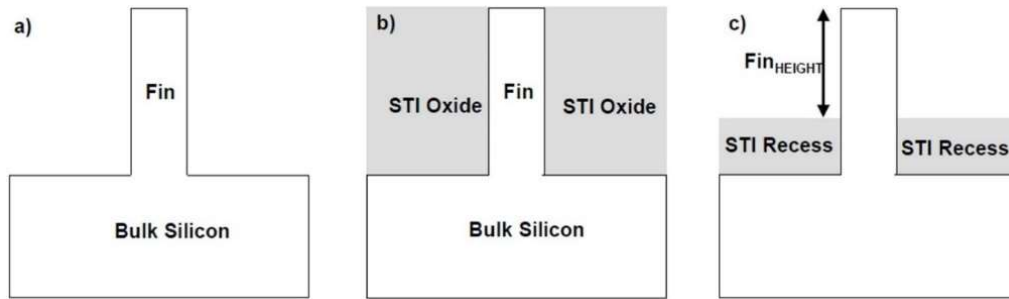
A POSITA would have known the basic structural difference between SOI FinFETs and bulk silicon FinFETs is their isolation. (*Supra* §II.B; Ex-1003 ¶¶143-145.) SOI FinFETs include a buried oxide underlying the fins (Colinge, 22-23, Fig. 2.2), whereas bulk silicon FinFETs include a recessed STI oxide surrounding the fins (*id.*, 37-38, Fig. 2.14).



A POSITA thus would have known Doris's "bulk silicon" implies certain steps to make STI. (*See* Doris ¶¶0069] ("[S]teps may be added"); Ex-1003 ¶146; Ha ¶¶[0091]-[0093]; Colinge, Fig. 2.14; Zhao, 6:15-27, FIGS. 2A-2B; Yu ¶¶[0019]-[0021], FIGS. 1-3.) First, fins are patterned. (Colinge, Fig. 2.14(a).) Second, oxide

is deposited thicker than the fins and then planarized. (*Id.*, Fig. 2.14(b) & caption.)

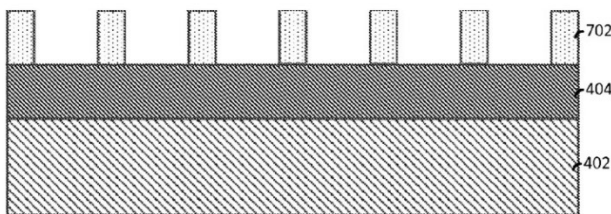
Third, the oxide is recessed until the fin has a desired height. (*Id.*, Fig. 2.14(c).)



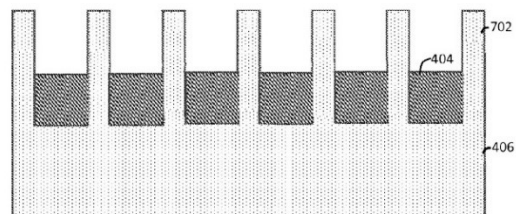
Colinge, Fig. 2.14(a)-(c)

b. A POSITA understood Doris's process flow as applied to a bulk silicon substrate

In exemplary figures, Doris's fins 702 are etched into an SOI substrate using mask layers that are then removed (*see* FIG. 7, below left). (*See id.* ¶¶[0044]-[0046], FIGS. 5-7.) The same would be true in Doris's bulk silicon arrangement. (*See* Doris, ¶[0043]; Ex-1003 ¶147.) Then, because bulk silicon lacks insulator layer 404, a recessed STI oxide would be formed around fins 702 to perform the same function. (Colinge, Figs. 2.2, 2.14; *supra* §II.B; Ex-1003 ¶148; Ha ¶[0093], FIGS. 3A-3C.)



Doris, FIG. 7 (modified)

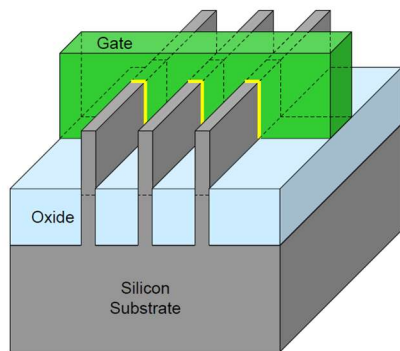


Alternative FIG. 7

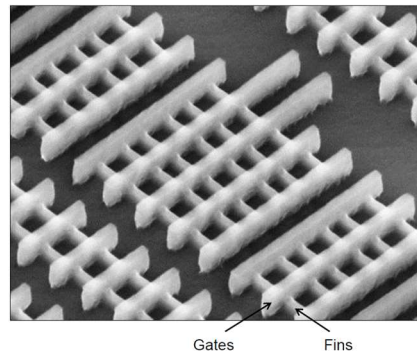
Alternative FIG. 7 above shows a bulk silicon substrate with fins 702 surrounded by STI 404. From that point on, a POSITA would have understood Doris's process flow

would proceed as described for the SOI substrate, this being the only notable difference. (*Supra* §II.B; Ex-1003 ¶148.)

A POSITA would have been motivated to perform the steps above to achieve Doris's *expressly disclosed* bulk silicon arrangement, a well-known and more prevalent alternative to SOI. (See Doris ¶[0040], ¶[0043]; *supra* §VI.A.1.a; Ex-1003 ¶146, ¶149.) And a POSITA would have reasonably expected success both because *Doris expressly discloses it* and because bulk silicon FinFETs began widespread commercial use from the outset, when FinFETs first launched in 2011 (see below), long before the '880 Patent. (*Supra* §II.B; Ex-1003 ¶150.)



Ex-1020, 7



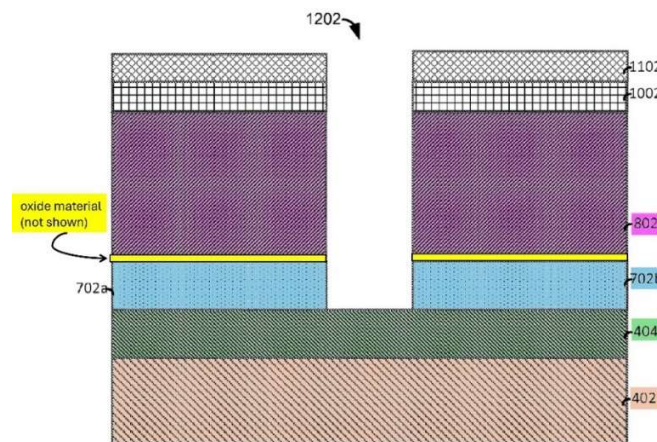
Ex-1020, 8

A POSITA thus would have readily known and found it obvious—from textbook familiarity with bulk silicon FinFETs (including Ha's and Colinge's examples)—how to apply Doris's FinFET process flow in a bulk silicon arrangement, as described above. This would have been viewed this as (1) simply adopting one disclosed and well-known element (bulk silicon substrate) instead of another (SOI substrate) to obtain predictable results (e.g., lower wafer cost and better

substrate heat transfer rate, *see* Colinge, 37); (2) choosing from among two identified, predictable solutions (SOI or bulk substrate), with reasonable expectation of success; and (3) a teaching, suggestion, or motivation in the prior art (*see* Doris ¶[0040], ¶[0043], ¶[0069]; Ha ¶[0093]; Zhao, 6:15-27, Yu ¶¶[0019]-[0021]) that would have led a POSITA to modify Doris and arrive at the claimed invention. (*See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-21 (2007); Ex-1003 ¶¶151-152.)

c. A POSITA would have found it obvious that etching Doris's cavity 1202 would partially etch the STI in Doris's bulk silicon embodiment, as it does in Ha

Doris forms an amorphous silicon (α -Si) or polysilicon layer 802 (magenta below) over fins 702 (blue below). (Doris ¶[0047], FIGS. 8-9.) “[A] layer of oxide material [added in yellow] may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802.” (*Id.* ¶[0047].)

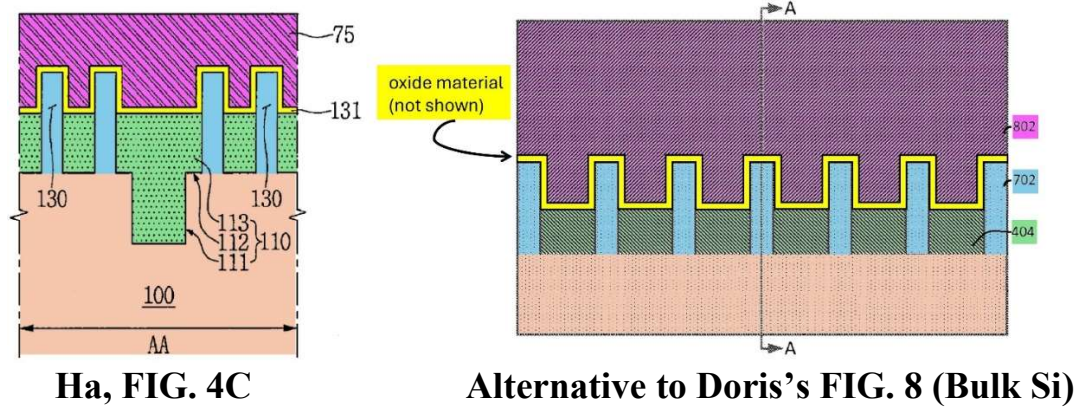


Doris, FIG. 12 (annotated)

Doris cuts the fins with a cavity 1202 formed by “a dry etching or RIE process that removes exposed portions of the hardmask 1002, exposed portions of the α -Si

layer 802, and the fins 702.” (Doris ¶[0050], FIGS. 12, 14.) A POSITA would have understood the “layer of oxide material” (yellow) also must be removed to form cavity 1202 since it overlays fins 702. (Ex-1003 ¶¶153-154.)

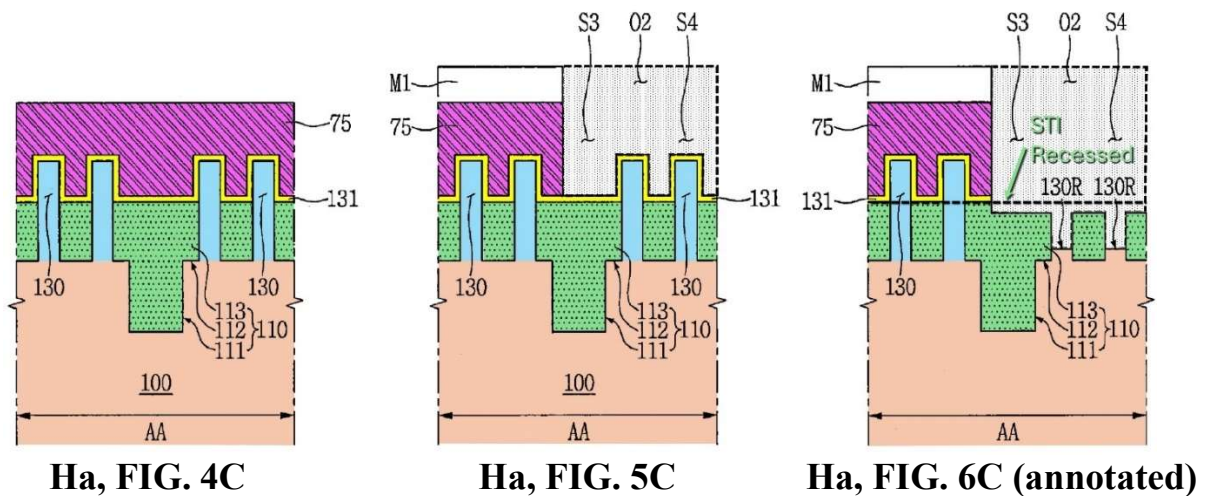
A POSITA would have understood the same etching sequence applies to bulk silicon. (Ex-1003 ¶155; *see* Doris ¶[0040], ¶[0043].) But because the STI surrounds the fins rather than underlying them, the etching process would appear similar to Ha. (Ex-1003 ¶155; *see* Ha ¶¶[0099]-[0105], FIGS. 5A-6C.) As shown here, Doris and Ha share the same layers. (Ex-1003 ¶156.)



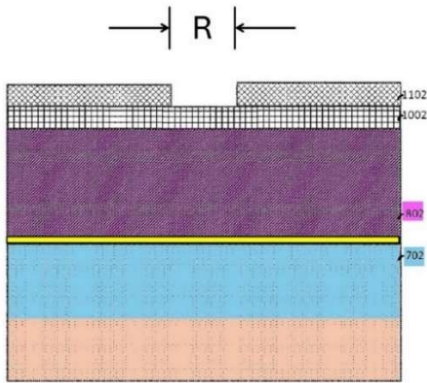
Ha’s silicon substrate corresponds to Doris’s silicon substrate (peach). (Ha ¶[0066]; Doris ¶[0040], ¶[0043]; Ex-1003 ¶157.) Ha’s fins 130 correspond to Doris’s fins 702 (blue). (Ha ¶[0067]; Doris ¶[0046]; Ex-1003 ¶159.) Ha’s insulation material 113 in shallow trench 112 corresponds to the STI (green) of Doris’s bulk silicon arrangement. (Ha ¶[0067]; Doris ¶[0040], ¶[0043]; *supra* §VI.A.1.a-b; Ex-1003 ¶157.) Ha’s silicon oxide layer 131 corresponds Doris’s “layer of oxide material” (yellow). (Ha ¶[0089]; Doris ¶[0047]; Ex-1003 ¶157.) And Ha’s fin gate

pattern 75 corresponds Doris's silicon layer 802 (magenta). (Ha ¶[0095]; Doris ¶[0047]; Ex-1003 ¶157.)

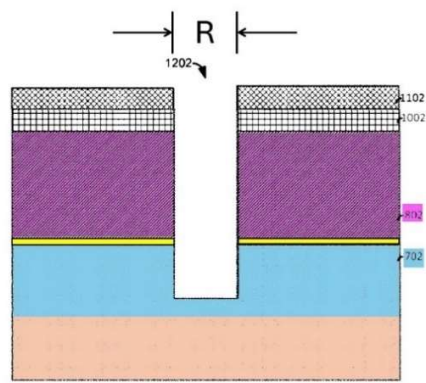
To form Ha's fin active cut-zone CZ3 (shaded in gray below), Ha first etches through fin gate pattern 75 (magenta), then base insulating layer 131 (yellow), then part of fins 130 (blue). (Ha ¶[0063], ¶[0096]-[0105], FIGS. 4A-6C.) Ha's figures below depict this sequence, showing the STI (green) "may be recessed." (Ha ¶[0105]; *see id.*, FIGS. 6A-6C.)



A POSITA would have understood, and found obvious, that Doris discloses the same etch sequence to form cavity 1202. (Doris ¶[0050], FIGS. 11-12; Ex-1003 ¶[158-159].) Doris's FIGS. 11 and 12 are analogous to Ha's FIGS. 4C and 6C, above, respectively, except they show a different cross-section. Ha's figures above show a cross-section with the fins running in and out of the page, whereas Doris's FIGS. 11 and 12 show a cross-section with a fin running horizontally.

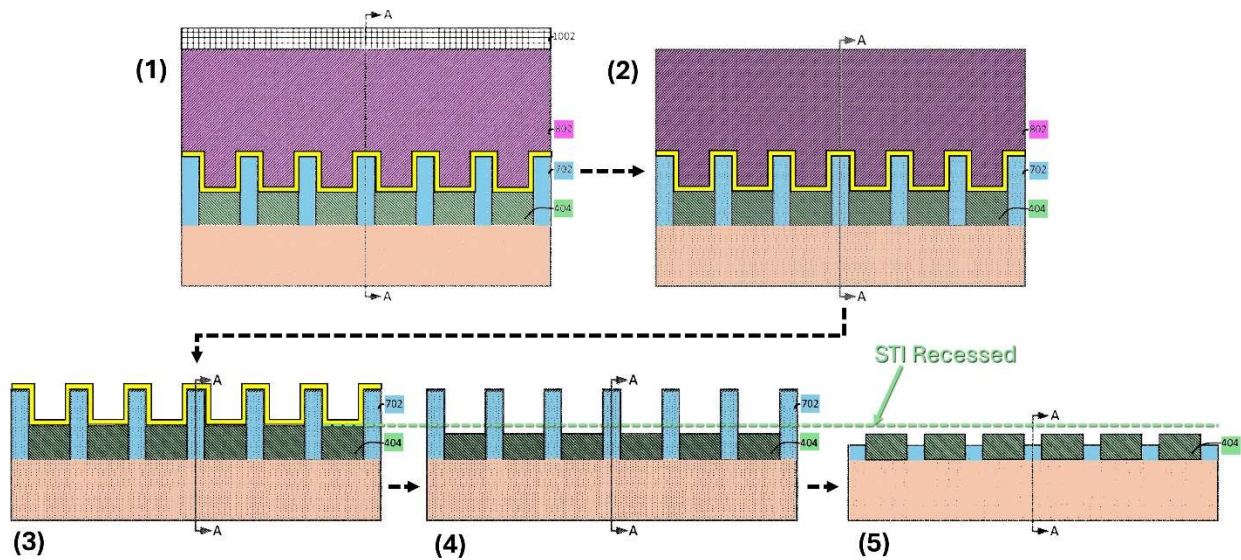


Alternative FIG. 11 (Step 1 below)



Alternative FIG. 12 (Step 5 below)

In bulk silicon, Doris's cavity etch would proceed as in Ha, as shown here. (Ex-1003 ¶160; Ha ¶[0105], FIGS. 4C, 5C, 6C; Colinge, Fig. 2.14.) The figures below show Doris's etching sequence in region R above, and the fins run in and out of the page. The figures above depict the A–A cross-section of the figures below, and the fin runs horizontally.

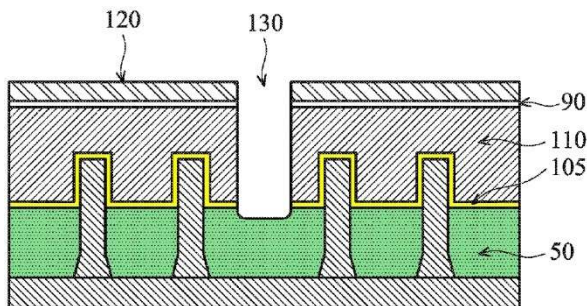


Ex-1003 ¶160

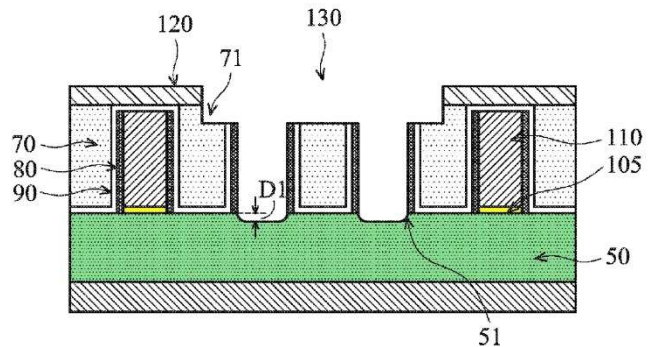
First, hardmask 1002 is removed, followed by silicon layer 802 (magenta), then the “layer of oxide material” (yellow), and then a portion of fins 702 (blue). (Ex-1003

¶161; *see* Doris ¶[0050], FIG. 12.) Because the “layer of oxide material” (yellow) and STI (green) are both silicon oxide, a POSITA would have understood, as in Ha, that the STI (green) “may be recessed” when removing the gate oxide (yellow). (Ha ¶[0105]; *see id.*, FIG. 6C; Ex-1003 ¶162.)

Yu further confirms that recessing the STI, as Ha discloses, was well known. (Ex-1003 ¶163.) Like Ha and Doris, Yu discloses a silicon oxide gate insulating layer 105 (yellow) and silicon oxide isolation insulating layer 50 (green). (Yu ¶[0020], ¶[0023].)



Yu, FIG. 6A



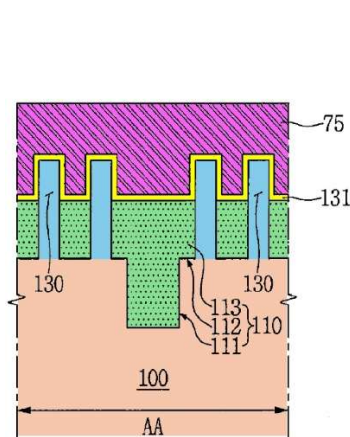
Yu, FIG. 6B

Yu explains that, when etching gate insulating layer 105, “the surface portion 51 of the isolation insulating layer 50 [is] also etched” to a depth D1. (*Id.* ¶[0032].) “The depth D1 ... is in a range from about 1 nm to about 10 nm.” (*Id.*)

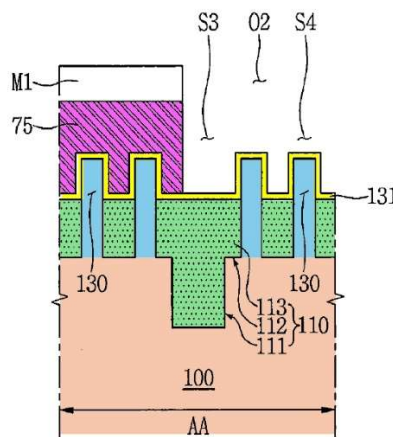
This would have been expected in Doris, too. It is a textbook concept that “[s]ome amount of overetching is normally part of every etch process,” such that “underlying films are normally subjected to the etchant for some period of time.” (Ex-1011, 24-25; *see* Ex-1003 ¶161.) Over a fin, which is non-planar, this is

especially true. (Ex-1011, 36 (Fig. 10-23) (“Overetching of a film over a corner would be required to remove material at the corner.”).) “The selectivity ... with respect to the underlying material determines how much etching of the underlying materials occurs.” (*Id.*, 24.)

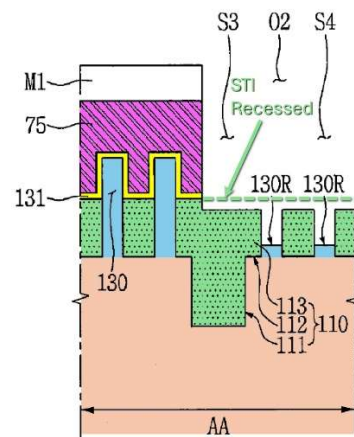
In Doris, there is no selectivity since the “layer of oxide material” (yellow) and the STI (green) are both silicon oxide. (Doris ¶¶[0047]; *see id.* ¶¶[0043]; Colinge, Fig. 2.14; Zhao, 6:15-27, FIG. 2B.) Thus, a POSITA would have found it obvious when etching the oxide material (yellow) to partially remove the underlying STI (green). (Ex-1003 ¶162; Ha ¶¶[0099]-[0105], FIGS. 5A-6C; Yu ¶[0023], ¶¶[0031]-[0032], FIGS. 6A-6B.)



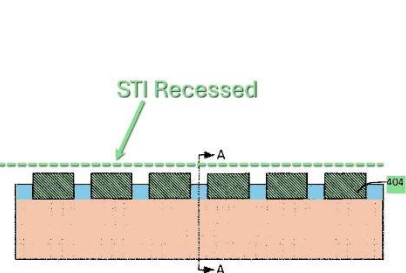
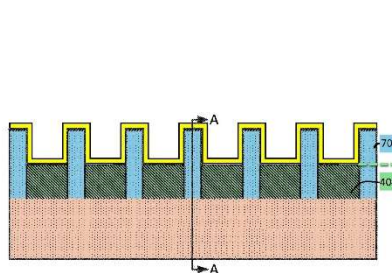
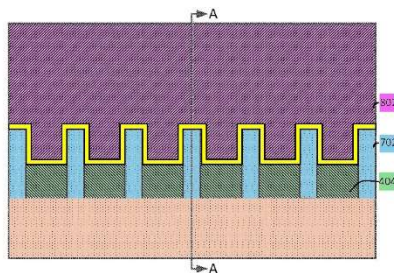
Ha, FIG. 4C



Ha, FIG. 5C



Ha, FIG. 6C (annotated)



Ex-1003 ¶162 (Doris's analogous etch sequence)

A POSITA would have been motivated to over-etch Doris’s “layer of [gate] oxide material” (Doris ¶[0047]) to ensure its adequate removal. (Ex-1003 ¶164; *see* Ex-1011, 24-25, 36 (Fig. 10-23); Ha ¶¶[0104]-[0105], FIG. 6C; Yu ¶¶[0031]-[0032], FIGS. 6A-6B.) In doing so, removing part of the underlying STI would have been expected because, like Doris’s gate oxide material, it is made of silicon oxide and vulnerable to the same etchants. (Ex-1003 ¶¶165-166.) Accordingly, there would have been motivation to include this feature in Doris or an understanding that it would be present. (*See Intel Corp. v. XPP Schweiz AG*, 61 F.4th 1373, 1379-81 (Fed. Cir. 2023) (“[I]f there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is a motivation to combine.” (quoting *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 799-800 (Fed. Cir. 2021))).)

A POSITA would have reasonably expected success because this would not have affected any other steps in Doris’s process flow or the final device. (Ex-1003 ¶167.) Routine experiments would have readily identified the proper timing of the etch used to remove Doris’s gate oxide material, ensuring adequate removal and resulting in some amount of over-etch into the silicon oxide STI underneath, as expected. (Ex-1003 ¶168; *see* Ex-1011, 24-25, 36 (Fig. 10-23); Ha ¶¶[0104]-[0105], FIGS. 6A-6C; Yu ¶¶[0031]-[0032], FIGS. 6A-6B.)

Consistent with Ha’s disclosures (as Yu further confirms), a POSITA thus would have found it obvious to partially remove the exposed STI in Doris’s bulk silicon FinFETs (Doris ¶¶[0040], ¶¶[0043]; Colinge, Fig. 2.14) when etching Doris’s oxide gate layer (Doris ¶¶[0047]). This would have been viewed as an obvious example of (1) using a known technique (over-etching) to improve similar methods or products in the same way; (2) performing routine experimentation (to select a suitable etch recipe that completely removes the oxide gate layer from over the fins), with reasonable expectation of success; and (3) a teaching, suggestion, or motivation in the prior art (*see* Ha ¶¶[0104]-[0105], FIGS. 6A-6C; Yu ¶¶[0031]-[0032], FIGS. 6A-6B; Ex-1011, 24-25, 36 (Fig. 10-23)) that would have led a POSITA to arrive at the claimed invention. (*See KSR*, 550 U.S. at 416-21; Ex-1003 ¶169.)

2. Independent Claim 1

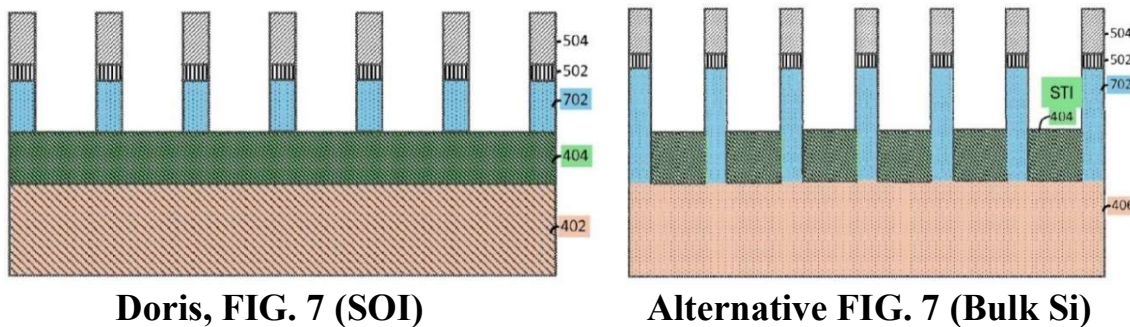
a. [1pre]: “[a] method for fabricating semiconductor device”

Doris describes “a method for fabricating a field effect transistor device.” (Doris ¶[0004]; Ha ¶[0005] (“a method of fabricating semiconductor devices including a gate core and a fin active core”); Ex-1003 ¶¶170-171.)

b. [1a]: “forming a fin-shaped structure on a substrate”

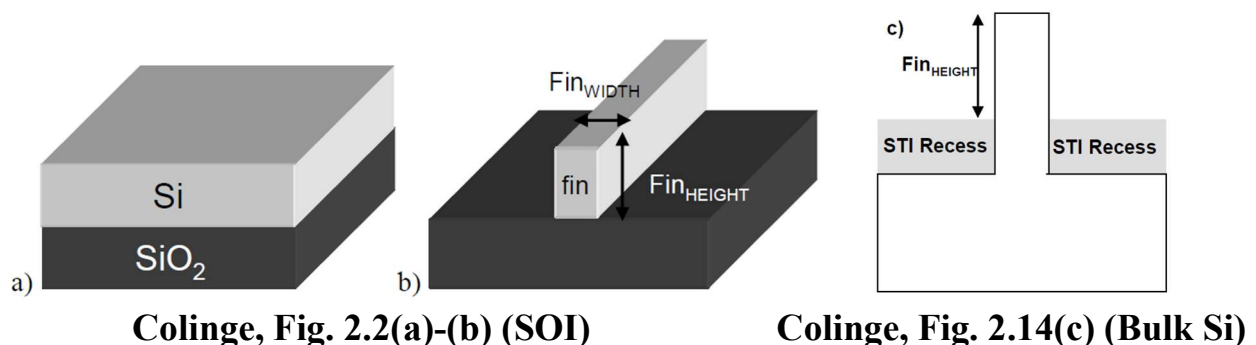
Doris describes “the fabrication of fins 702 ... using an etching process.” (Doris ¶[0046]; *see id.* FIGS. 5-7; Ha ¶¶[0091]-[0092], FIGS. 3A-3C.) Although Doris’s FIGS. 4-17 depict an SOI embodiment with buried insulator layer 404, Doris

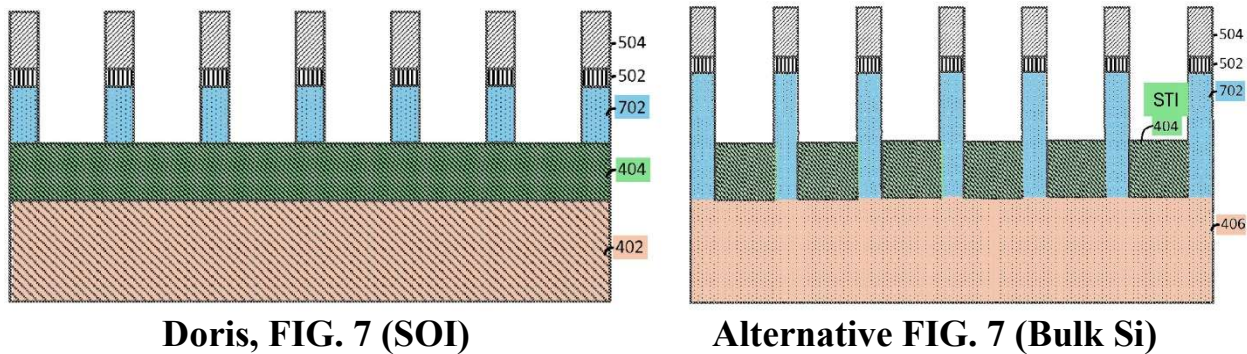
expressly states that the same process flow also may be applied to a “bulk silicon” FinFET. (Doris ¶[0040]; *see id.* ¶[0043].) As explained above, such an embodiment involves etching fins (blue) into a bulk silicon substrate (peach), as shown on the right below. (*Supra* §VI.A.1.a-b; Colinge, 37-38, Fig. 2.14; Ex-1003 ¶¶171-174.)



c. [1b]: “forming a shallow trench isolation (STI) around the fin-shaped structure”

Doris’s “illustrated exemplary embodiment shows a silicon on insulator (SOI) arrangement,” such that “[a]n insulator layer 404 is arranged on the substrate 402, where the insulator layer 404 may include, for example, an oxide material.” (Doris ¶[0043].) But Doris expressly states “alternate exemplary embodiments may include a bulk silicon ... arrangement.” (*Id.*) Ground 1A analyzes Doris’s bulk silicon FinFETs. (*Supra* §VI.A.1.a-b; Colinge, 37-38, Fig. 2.14; Ex-1003 ¶¶175-177.)



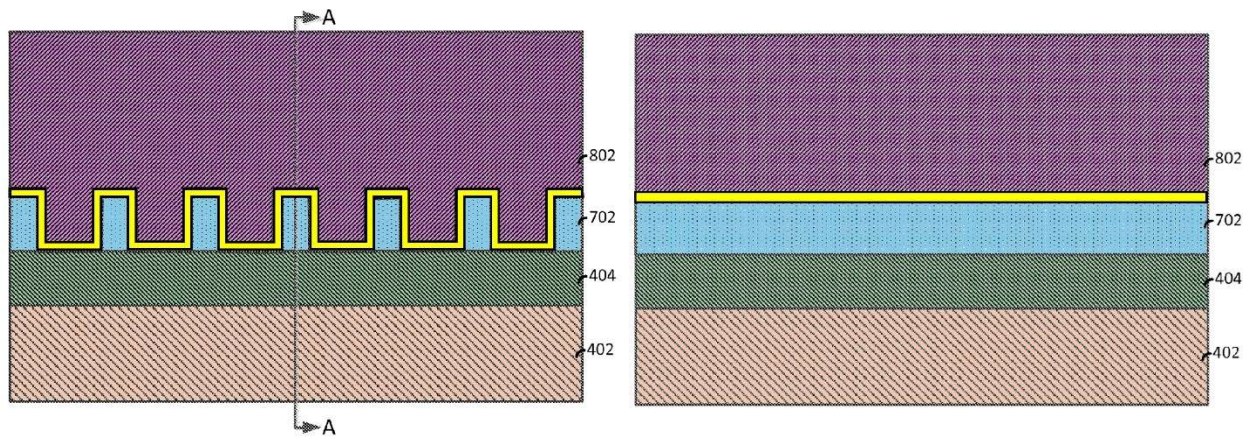


A POSITA would have understood, and found obvious, that Doris’s “bulk silicon ... arrangement” (Doris ¶[0043]) involves “STI oxide deposition and planarization,” followed by “STI oxide recess to expose silicon fin with desired [fin height].” (Colinge, 38 (Fig. 2.14); *see* Ex-1003 ¶177.) This would form STI oxide (green) around the fins (blue), shown on the right above, rather than having a buried oxide layer under the fins, shown on the left. (*Supra* §VI.A.1.a-b; Ex-1003 ¶¶176-177; *compare* Colinge, Fig. 2.2(a)-(b), *with* Colinge, Fig. 2.14.)

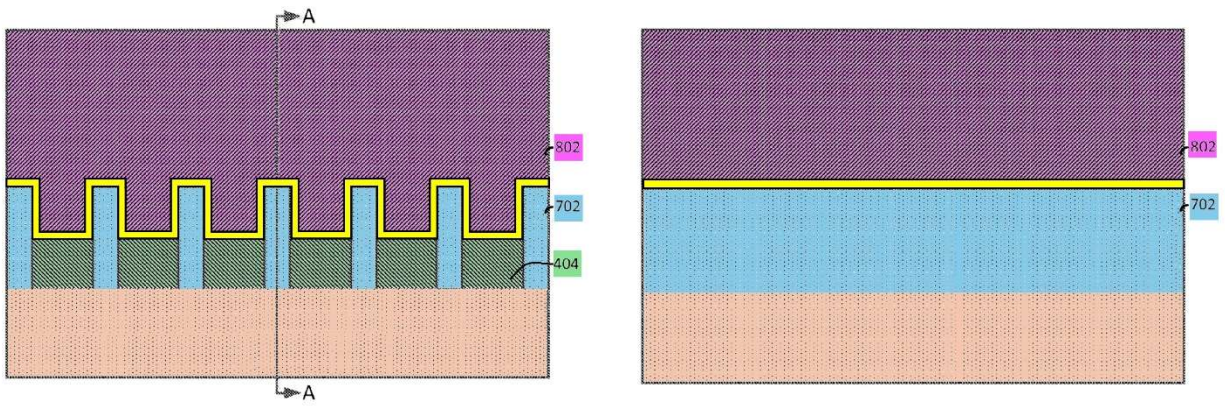
d. [1c]: “forming a gate layer on the fin-shaped structure and the STI”

Doris discloses “deposition of an amorphous silicon (α -Si) layer 802 over the fins 702 and exposed portions of the insulator layer 404.” (Doris ¶[0047]; *see id.*, FIGS. 8-9; Ha ¶[0091], FIGS. 3A-3C.) Doris further explains “a layer of oxide material [added in yellow below] may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802.” (Doris ¶[0047]; *see* Ha ¶[0091], FIGS. 3A-3C.) Silicon layer 802 is later patterned into

“dummy gate stacks 1502” (a gate structure) and is thus a gate layer. (Doris ¶[0053]; *see id.*, FIG. 16; Ex-1001, 3:7-10, 4:8-14.)



Doris, FIG. 8 (yellow oxide added) Doris, FIG. 9 (A-A, yellow oxide added)



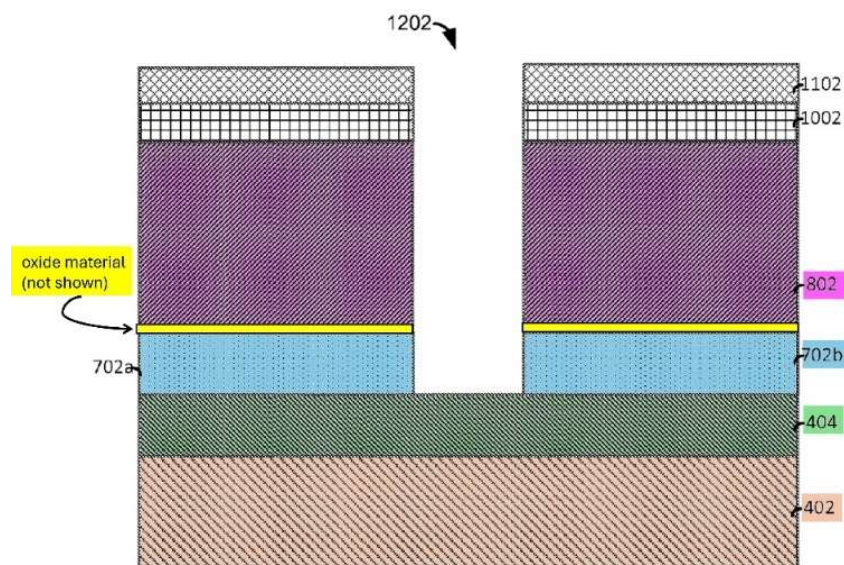
Alternative FIG. 8 (Bulk Si)

Alternative FIG. 9 (A-A, Bulk Si)

Doris’s FIG. 8 looks down the fins, and Doris’s FIG. 9 shows the A–A cross-section, with a fin running horizontally. (Doris ¶[0047].) Alternative FIGS. 8 and 9 show Doris’s “bulk silicon” arrangement. (*Id.* [0043]; *see supra* §VI.A.1.a-b; Ex-1003 ¶¶180-181.) In the bulk silicon arrangement, silicon layer 802 (magenta) is a gate layer formed on the fins 702 (blue) and the STI (green). (Ex-1003 ¶¶178-181.)

e. [1d]: “removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench”

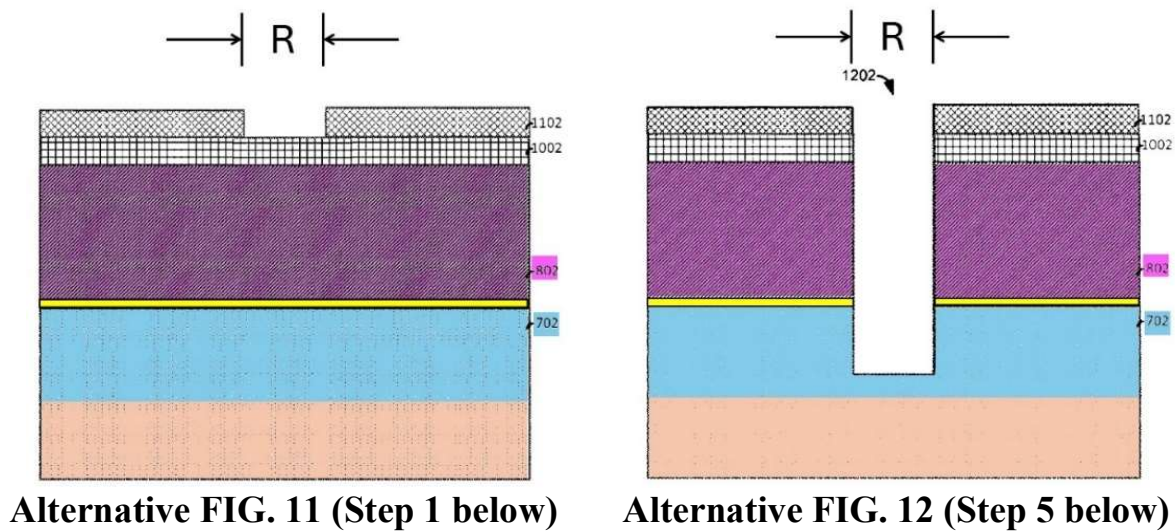
Doris discloses “formation of a hardmask layer 1002 over the α -Si layer 802,” “formation of a mask 1102 that is lithographically patterned over the hardmask layer 1002,” and “an etching process ... that removes exposed portions of the hardmask 1002, exposed portions of the α -Si layer 802, and the fins 702.” (Doris ¶¶[0048]-[0050]; *see id.* FIGS. 10-12; Ha ¶¶[0099]-[0105], FIGS. 5A-6C.) As Doris’s FIG. 12 shows, this creates a cavity 1202 by etching through hardmask 1002, then through silicon layer 802 (magenta), then through the gate oxide layer (yellow, Doris ¶[0047]), and finally into fins 702 (blue). (Doris ¶[0050].) Fins 702 are thereby cut into two segments 702a and 702b. (*Id.*) Accordingly, Doris discloses removing part of the gate layer (silicon layer 802) and fin-shaped structure (fins 702) to form a trench (cavity 1202). (Ex-1003 ¶¶183-185.)



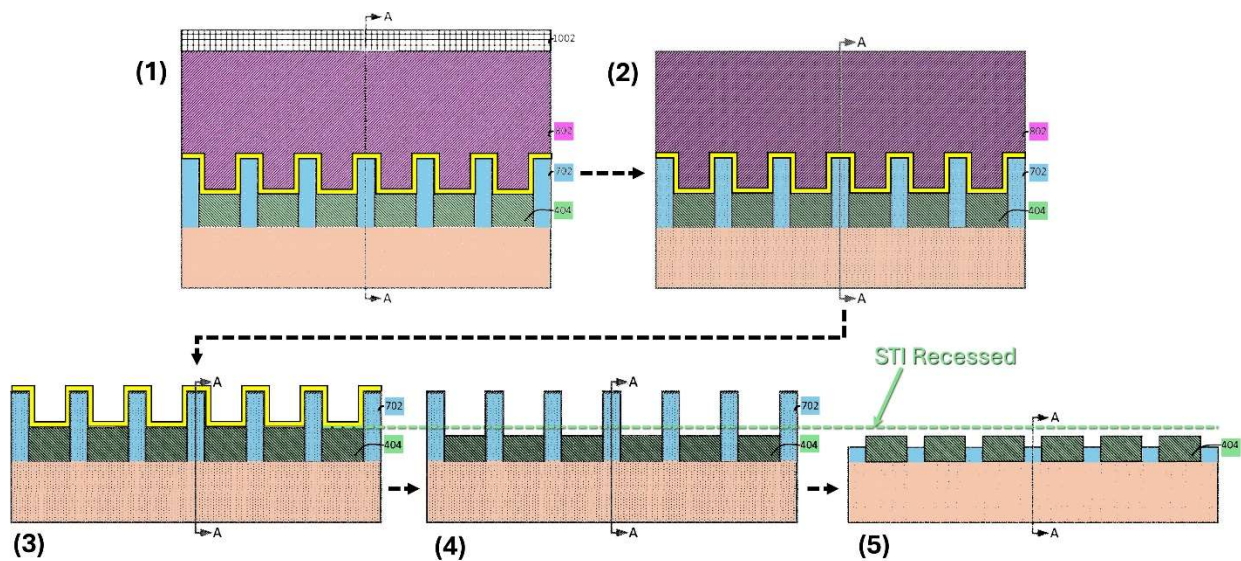
Doris, FIG. 12 (yellow gate oxide added)

A POSITA would have found it obvious that forming cavity 1202 further involves removing part of the isolation oxide (STI in the bulk silicon embodiment) (green). (Ex-1003 ¶186; *supra* §VI.A.1.c.)

The figures below depict how Doris's cavity is etched in Doris's bulk silicon arrangement. (See Doris ¶[0043]); *supra* §VI.A.1.c; Ex-1003 ¶186.)



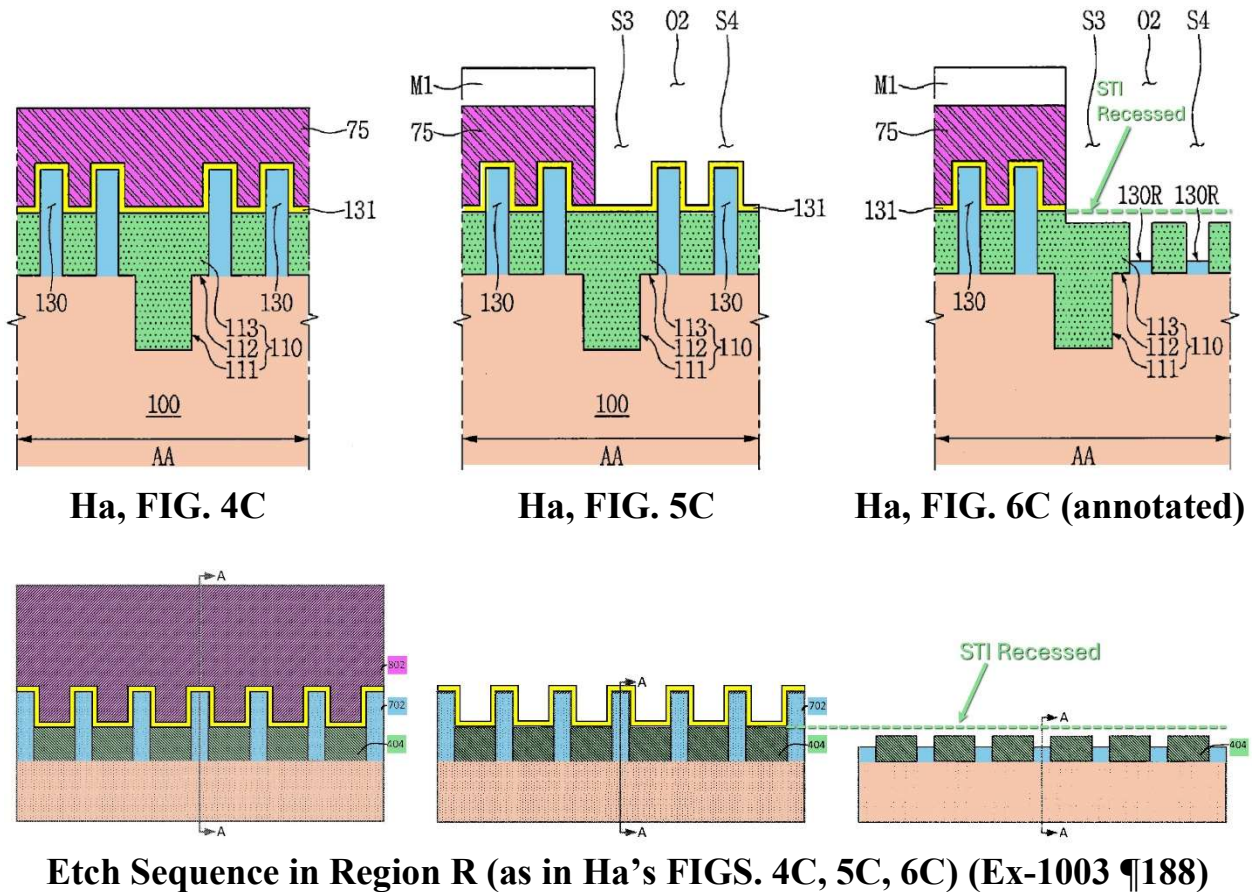
Etch Sequence in Region R



Ex-1003 ¶186

Doris's disclosed etch proceeds in region R like Ha's. (Ha ¶¶[0099]-[0105], FIGS. 5A-6C; Ex-1003 ¶187.) Like Doris, Ha discloses "forming a first mask pattern M1" and "removing portions of the ... gate pattern[] [75]" (magenta). (Ha ¶[0099], FIG. 5C.) Ha also discloses "forming a fin active recess 130R by ... recessing the fin active region 130" (blue) and explains that "isolation region 110 [green] ... may be recessed." (Ha ¶¶[0104]-[0105]; *accord* Yu ¶¶[0031]-[0032], FIGS. 6A-6B.)

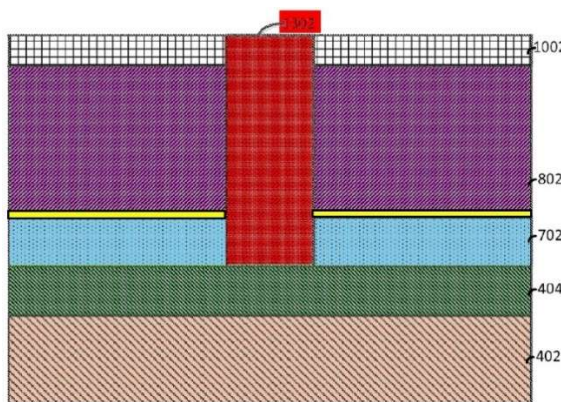
The figures below compare this sequence both for Ha and Doris's bulk silicon arrangement. (*Supra* §VI.A.1.c; Ex-1003 ¶188.)



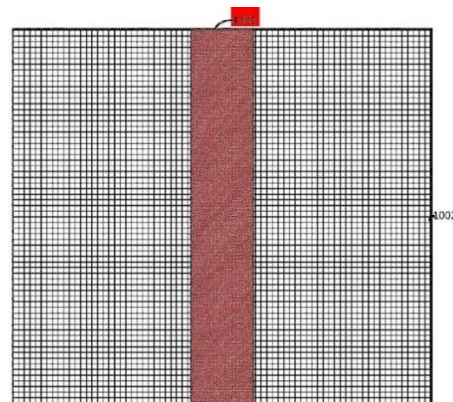
As Section VI.A.1.c explains, a POSITA would have found it obvious to recess the STI in Doris's bulk silicon arrangement when removing the gate oxide layer (yellow) since both films are in direct contact and made of silicon oxide. (*Supra* §VI.A.1.c; Colinge, Fig. 2.14; Doris ¶[0047]; Ha ¶[0105] ("The isolation region ... may be recessed."), FIG. 6C; Yu ¶[0032] ("During the oxide etching, ... isolation insulating layer 50 [is] also etched"), FIGS. 6A-6B; Ex-1003 ¶189.) Accordingly, Ground 1A further renders obvious removing part of the STI (green) to form the trench (cavity 1202). (Ex-1003 ¶¶182-190.)

f. [1e]: "forming a dielectric layer into the trench to form a single diffusion break (SDB) structure"

Doris's cavity 1202 "cut[s]" the fins. (Doris ¶[0050].) Then, Doris discloses "deposition of an insulator material 1302 [red] in the cavity 1202." (Doris ¶[0051]; *see id.*, FIG. 13; Ha ¶¶[0106]-[0111], FIGS. 7A-9C.) Doris's FIG. 13 shows this step in cross-section, with a fin (blue) running horizontally. Doris's FIG. 14 shows this step from above. (Doris ¶[0051].)

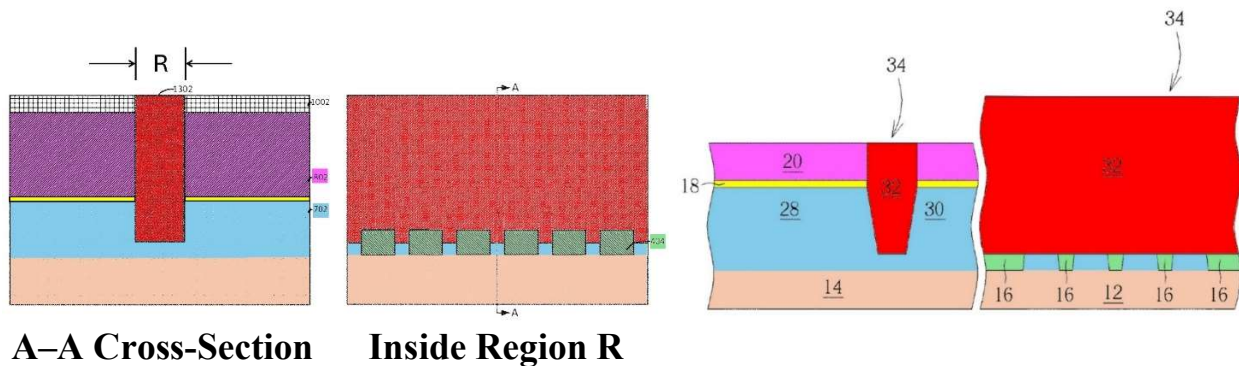


Doris, FIG. 13 (Cross-Section)



Doris, FIG. 14 (Plan View)

In Doris’s bulk silicon arrangement, cross-sections for this step would appear as on the left below. (*See supra* §VI.A.1.c, §VI.A.2.e; Ex-1003 ¶¶192-194.) The plan view would be identical to FIG. 14. (Ex-1003 ¶194.) The result is a single diffusion break (“SDB”) structure as the ’880 Patent discloses (below right).⁴ (Ex-1003 ¶195; *see* Ex-1001, 3:39-59, FIG. 6.)



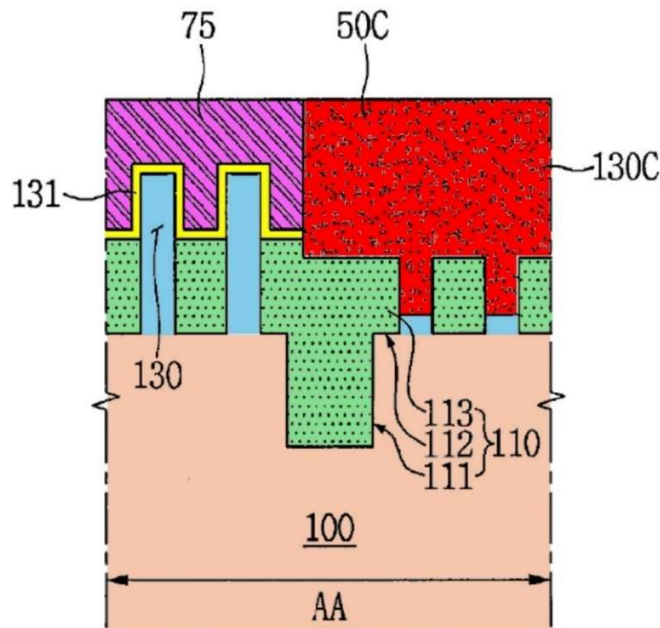
Ex-1003 ¶194 (Doris Bulk Si)

'880 Patent, FIG. 6^[5]

Ha’s analogous “single diffusion break (SDB) structure” (red) in FIG. 9C (below) further confirms that Doris’s insulator material 1302 forms an SDB structure. (Ha ¶[0129]; *see id.* ¶¶[0106]-[0111], FIGS. 7A-9C; Ex-1003 ¶196.)

⁴ As in the ’880 Patent, and characteristic of any SDB, Doris’s SDB (insulator material 1302) separates the fins and sits directly adjacent to “[a]ctive regions” 1706 (source/drain regions) in the final structure. (*Compare* Doris ¶[0054], FIG. 17, with Ex-1001, 4:39-44, FIG. 10; *see supra* §II.C; Ex-1003 ¶195 & n.14.)

⁵ *Supra* note 3.

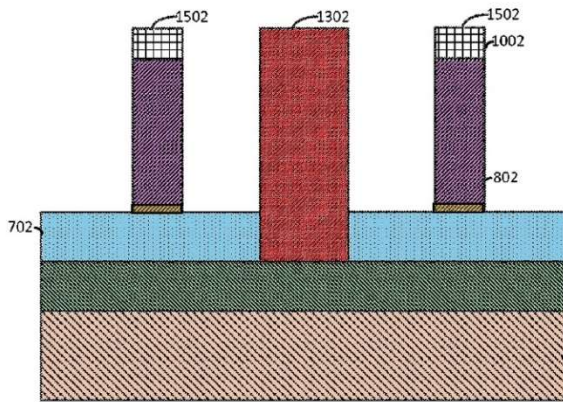


Ha, FIG. 9C

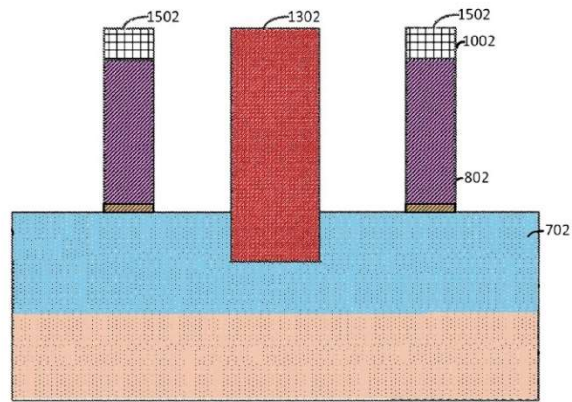
Thus, Ground 1A renders obvious forming a dielectric layer (insulator material 1302) into the trench (cavity 1202) to form a single diffusion break (SDB) structure. (Ex-1003 ¶¶191-196.)

g. [1f]: “after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure”

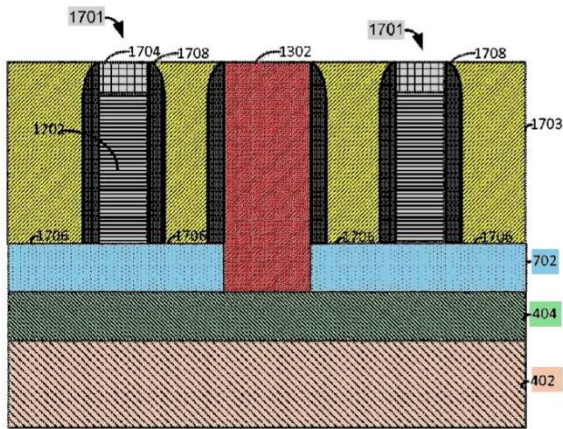
After patterning dummy gates 1502 (Doris ¶¶[0052]-[0053], FIG. 16), Doris discloses forming “[a] layer of insulator material 1703 such as, for example, an oxide material ... over exposed portions of the insulator layer 404, [and] the fins 702 and adjacent to the gate stacks 1701.” (Doris ¶[0054].) As FIG. 17 shows below, insulator material 1703 (yellow) is coplanar with insulator material 1302 (SDB structure). (*Id.*, FIG. 17.) The same would be true for Doris’s bulk silicon arrangement, shown in alternative FIG. 17. (*Id.* ¶[0043]; see Ex-1003 ¶¶198-199.)



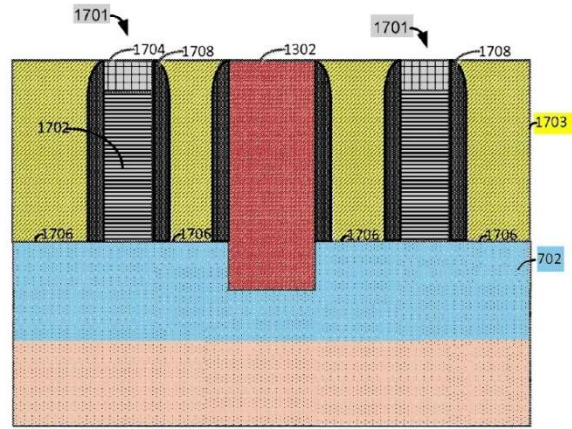
Doris, FIG. 16



Alternative FIG. 16 (Bulk Si)



Doris, FIG. 17



Alternative FIG. 17 (Bulk Si)

A POSITA would have understood how to make this coplanar structure, as evidenced by Ha, for example. (Ex-1003 ¶200.) Ha describes “forming a first interlayer insulating layer 171 [ILD] between the sacrificial gate patterns.” (Ha ¶[0096]; *accord* Yu ¶[0026].) This involves “forming silicon oxide to cover the sacrificial gate patterns ... and fill gaps between the sacrificial gate patterns ... and performing a planarization process such as a chemical mechanical polishing (CMP) process or an etch-back process.” (Ha ¶[0098]; *see id.*, FIGS. 3A-4C; Yu ¶[0026]-[0027], FIG. 4D.)

In Doris, a POSITA would have understood, and found it obvious, to do what Ha describes because that is how such layers are made: by “forming [insulator material 1703] to cover the [dummy gate stacks 1502 and insulator material 1302] and fill gaps between the[m],” then “performing a planarization process” so that insulator material 1703 and insulator material 1302 are coplanar. (Ha ¶[0098]; *accord* Yu ¶¶[0026]-[0027]; Ex-1015, 8:49-53; Ex-1017 ¶[0023]; Ex-1003 ¶201.) Then, Doris’s “dummy gate stacks 1502 are removed and replaced by the gate stacks 1701,” as FIG. 17 shows above. (Doris ¶[0054]; *see* Ex-1003 ¶201.)

Ground 1A thus renders obvious forming an ILD layer (insulator material 1703) on the SDB structure (insulator material 1302) after forming the SDB structure. (Ex-1003 ¶¶197-201.)

3. Claim 2: “The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.”

Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.)

Additionally, Doris discloses forming a gate dielectric layer on fins 702 before forming silicon layer 802 (gate layer). (Ex-1003 ¶204.) Doris explains that “a layer of oxide material (not shown) may be deposited over the exposed portions of the fins 702 and insulator layer 404 prior to depositing the α -Si layer 802.” (Doris ¶[0047].) This layer of oxide (a dielectric) is a gate dielectric layer because it underlies silicon layer 802 (gate layer) and is located in the position of a FinFET

gate dielectric. (*See supra* §VI.A.2.d (showing Doris’s gate oxide layer in yellow); Ex-1001, 3:3-7, FIG. 2; Ex-1003 ¶¶202-204.)

4. **Claim 3: “The method of claim 2, further comprising: forming a patterned mask on the gate layer; and using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.”**

Ground 1A satisfies claim 2. (*Supra* §§VI.A.1-3.)

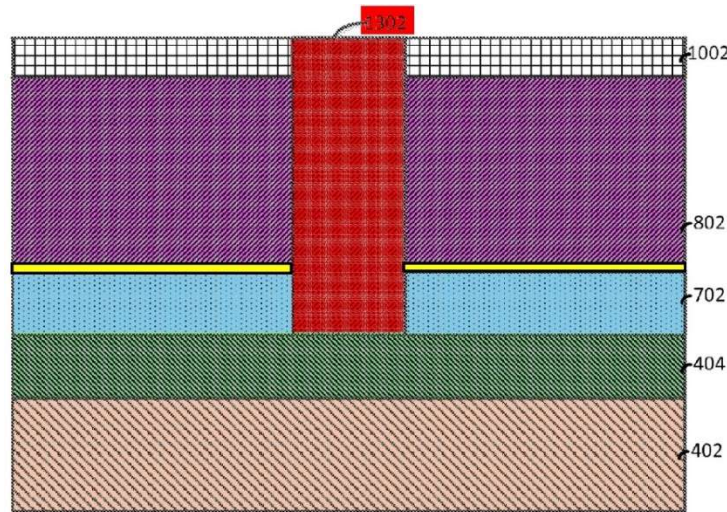
Further, for the reasons described regarding [1d], Doris discloses forming a patterned mask (mask 1102 and/or hardmask 1002) on the gate layer (silicon layer 802) and using it as a mask to remove part of the gate layer, part of the gate dielectric layer (Doris’s “layer of oxide material (not shown)” ¶[0047]), and part of the fin-shaped structure (fins 702), to form the trench (cavity 1202). (*Supra* §VI.A.2.e; Doris ¶¶[0048]-[0050], FIGS. 10-12; Ex-1003 ¶¶205-207.)

5. **Claim 4: “The method of claim 1, further comprising: forming the dielectric layer into the trench and on the gate layer; and planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.”**

Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.)

Additionally, Doris discloses insulator material 1302 (red) being coplanar with hardmask 1002 (see below). A POSITA would have understood this requires depositing insulator material 1302 into cavity 1202—which would also deposit on hardmask 1002—and then performing planarization to remove insulator

material 1302 from hardmask 1002. (Ex-1003 ¶210 & n.16; *see* Ha ¶[0106], FIGS. 7A-7C; Zhao, 8:9-16, FIGS. 2L-2M; Yu ¶¶[0036]-[0037], FIGS. 7A-8B.)

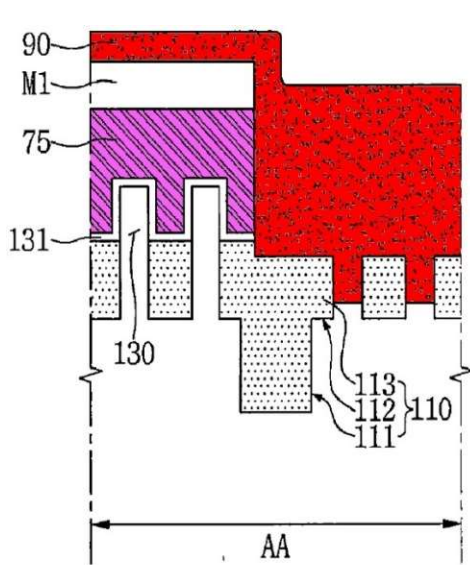


Doris, FIG. 13

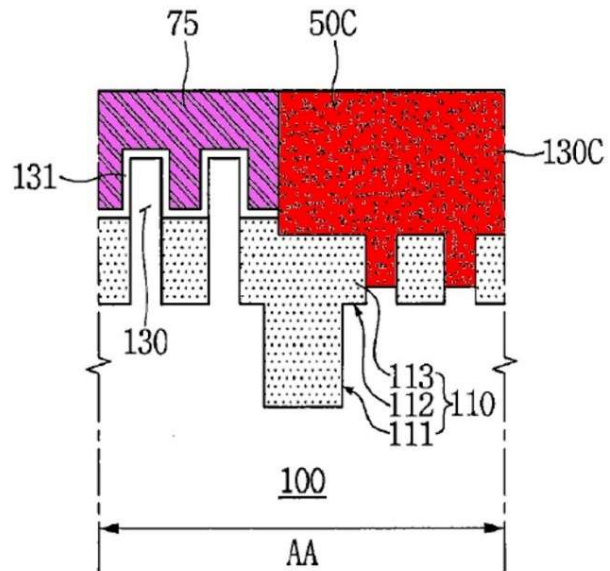
A POSITA would have found it obvious then to perform an additional planarization step to remove hardmask 1002 itself, leaving Doris’s insulator material 1302 (red) coplanar with silicon layer 802 (magenta). (Ex-1003 ¶213.) Moreover, this would have been a routine design choice, consistent with Ha. (*Id.*; *see* Ha ¶¶[0108]-[0111], FIGS. 7A-9C.)

As the figures below illustrate, Ha discloses filling the SDB trench with “an insulating core layer 90” that “may be formed semi-conformally” to extend onto sacrificial gate layer 75. (Ha ¶[0106].) Ha then discloses “removing [the] portions of the core layer 90 formed on the first mask pattern M1” and “removing the first mask pattern M1 and exposing the sacrificial gate patterns 71 to 76 by performing a planarization process.” (Ha ¶¶[0109]-[0110].) Consequently, “the remaining

sacrificial gate patterns 71 to 76 ... and the fin active core 130C may be coplanar,” as below. (*Id.* ¶[0111].) Exposing dummy gate patterns 71 to 76 allows for them to be replaced with a replacement metal gate. (*See* Ha ¶¶[0112]-[0115], FIGS. 10A-11C; *supra* §II.D; Ex-1003 ¶[212].)

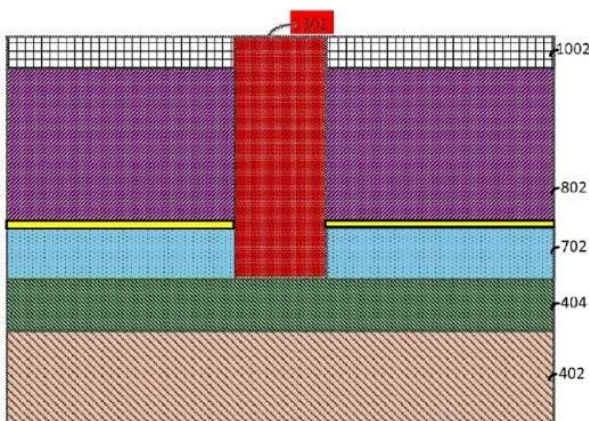


Ha, FIG. 7C

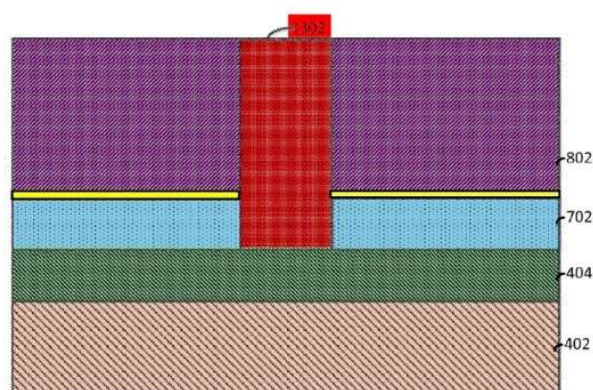


Ha, FIG. 9C

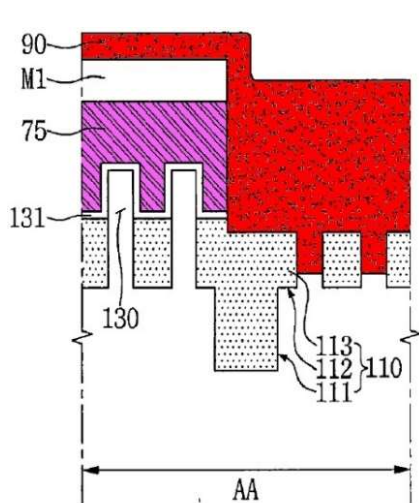
Like Ha, Doris replaces its dummy gate stacks 1502 with gate stacks 1701 comprising “a dielectric layer and a gate metal layer 1702.” (Doris ¶[0054]; *see* Ex-1003 ¶[213].) This involves removing hardmask 1002. (Doris ¶[0053] (“[H]ardmask layer 1002 [is] removed when the dummy gate stacks 1502 are formed.”).) For example, Doris explains that hardmask 1002 may be removed before patterning the dummy gate stacks. (*See id.* ¶[0052] (“[H]ardmask layer 1002 may be replaced with another hardmask layer that is suitable for patterning.”).)



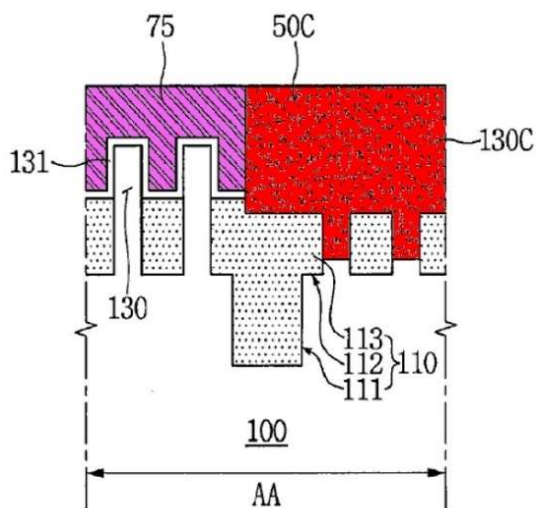
Doris, FIG. 13



Modified FIG. 13 (Polished to Si)



Ha, FIG. 7C



Ha, FIG. 9C

To remove hardmask 1002, as Doris discloses, a POSITA would have been motivated simply to perform additional planarization, as in Ha (illustrated above), to further planarize the structure in Doris's FIG. 13 to be level with silicon layer 802 (magenta). (Ex-1003 ¶214; *see* Ha ¶¶[0108]-[0111], FIGS. 7A-9C.)

Additional references confirm this was a routine step. Zhao, for example, discloses “one or more planarization processes” to “remove the gate cap layer ... and ultimately expose the sacrificial gate material” for the purpose of forming a

replacement metal gate. (Zhao, 8:26-34; *see id.*, 8:9-16, 8:35-49, Figs. 2L-2M.) Yu discloses the same. (See Yu ¶[0037] (“[A] CMP process is performed to expose the upper surface of the gate layers 110, as shown in FIGS. 8A and 8B. In other words, the gate layers 110 function as a stopper for the CMP process.”); *see id.* ¶¶[0036]-[0039], FIGS. 7A-8B; *accord* Ex-1015, 11:44-55, FIGS. 2P-2Q.) A POSITA thus would have been motivated to do the same when removing Doris’s hardmask 1002, as disclosed. (See *Intel*, 61 F.4th at 1379-81 (“[I]f there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is a motivation to combine.” (quoting *Intel*, 21 F.4th at 799-800)); Ex-1003 ¶¶215-216.)

A POSITA would have reasonably expected success because Ha and Doris disclose structures comprising identical materials. (Ex-1003 ¶217.) Like Ha’s sacrificial gate layer 75, Doris’s layer 802 is made of silicon. (*Compare* Doris ¶[0047] (“amorphous silicon” or “polysilicon”), *with* Ha ¶[0095] (“polycrystalline silicon”).) Like Ha’s mask M1, Doris’s hardmask 1002 may be made of silicon nitride. (*Compare* Doris ¶[0048] (“silicon nitride”), *with* Ha ¶[0095] (“silicon nitride”).) And like Ha’s fin active core 130C, Doris’s insulating material 1302 may be made of silicon nitride. (*Compare* Doris ¶[0051] (“nitride material”), *with* Ha ¶[0072] (“for example, silicon nitride”).) Thus, it would have been understood that

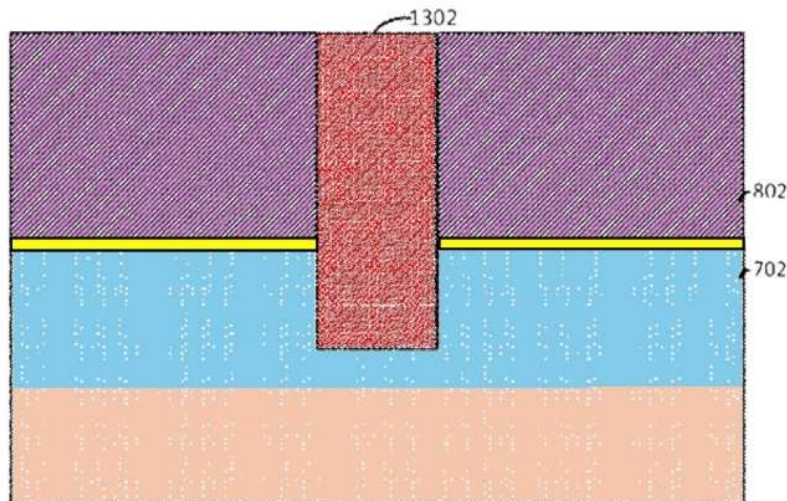
Ha's "CMP process" (i.e., chemical-mechanical polishing) (Ha ¶[0111]) applies equally to Doris's structure in FIG. 13. (Ex-1003 ¶217.)

A POSITA also would have understood Ha's planarization process matches Doris's disclosures. (Ex-1003 ¶218.) As explained above, Doris's hardmask 1002 must be removed before the replacement gate process can be performed. (*See* Doris ¶¶[0052]-[0054].) This is exactly why Ha planarizes analogous dummy gate layer 75 and SDB structure 130C. (*See* Ha ¶¶[0112]-[0115], FIGS. 10A-11C.) Performing Ha's planarization step therefore furthers Doris's goal to create a replacement metal gate stack. (*See* Doris ¶[0054] (explaining how to create a replacement "gate metal layer 1702"), FIG. 17.)

A POSITA thus would have found it obvious to remove Doris's hardmask 1002 using Ha's planarization, thereby making Doris's insulator material 1302 and silicon layer 802 coplanar. It would have been viewed as an obvious example of the following: (1) combining prior art elements according to known methods (Ha's planarization) to yield predictable results; (2) using a known technique (Ha's planarization) to improve similar methods in the same way; and (3) a teaching, suggestion, or motivation in the prior art (*compare* Doris ¶¶[0052]-[0054], *with* Ha ¶¶[0110]-[0115], Zhao, 8:9-49, Figs. 2L-2M; Yu ¶¶[0036]-[0039], FIGS. 7A-8B; *and* Ex-1015, 11:44-55, FIGS. 2P-2Q) that

would have led a POSITA to arrive at the claimed invention. (*See KSR*, 550 U.S. at 416-21; Ex-1003 ¶¶219-220.)

Accordingly, Ground 1A renders obvious forming the dielectric layer (Doris's insulator material 1302) into the trench (Doris's cavity 1202) and on the gate layer (Doris's silicon layer 802) and planarizing the dielectric layer (using Ha's additional planarization step, for example) so that the top surfaces of the dielectric layer and the gate layer are coplanar, as shown below. (Ex-1003 ¶¶208-221.)



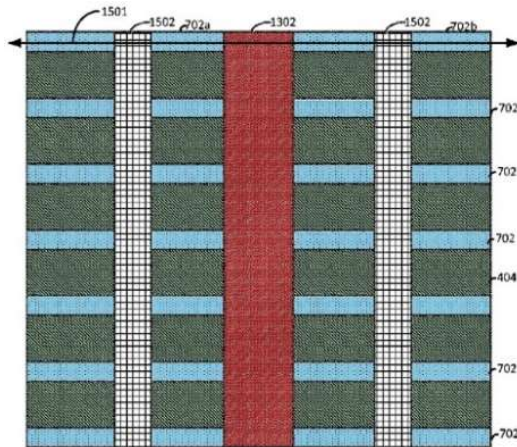
Alternative FIG. 13 (Hardmask 1002 Removed, Bulk Si)

- 6. Claim 5: “The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure.”**

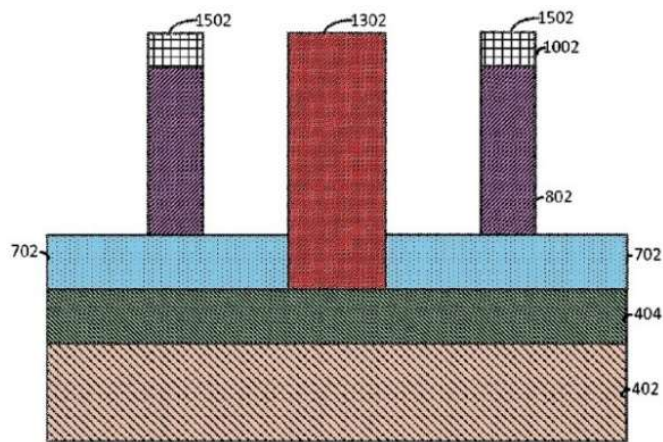
Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.)

Doris further discloses “the patterning and etching of portions of the hardmask layer 1002 and the α -Si layer 802 to define dummy gate stacks 1502” that “define channel regions of the fins 702.” (Doris ¶[0052]; *see id.* ¶[0053], FIGS. 15-16.) That

is, Doris discloses removing part of the gate layer (layer 802) after forming the SDB structure (insulator material 1302) to form a gate structure (dummy gate stacks 1502) adjacent to the SDB. Doris's FIG. 16 shows this in cross-section (with a fin running horizontally), and Doris's FIG. 15 shows it from above. (*Id.* ¶¶[0052]-[0053].)

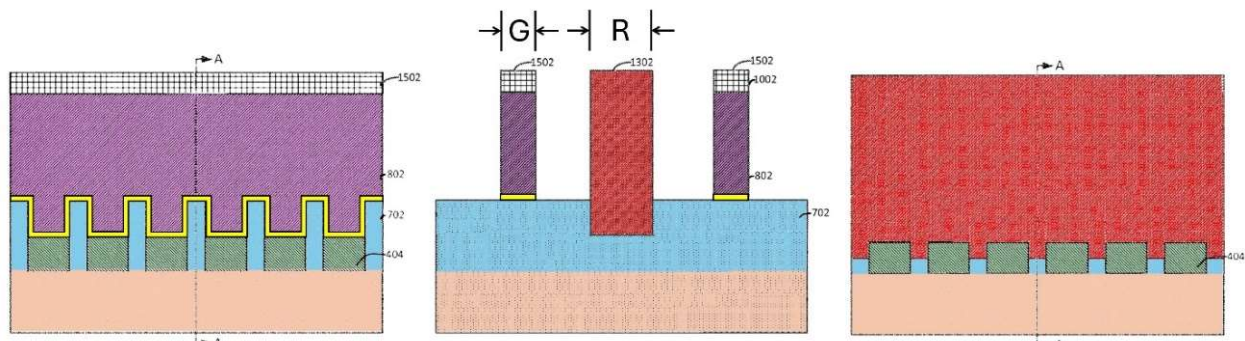


Doris, FIG. 15



Doris, FIG. 16

In Doris's bulk silicon arrangement (Doris ¶[0043]), the cross-sections for this step would appear as below. (*See supra* §VI.A.1.c, §VI.A.2.f; Ex-1003 ¶¶224-226.) The plan view would be identical to FIG. 15. (Ex-1003 ¶226.)



Inside Region G

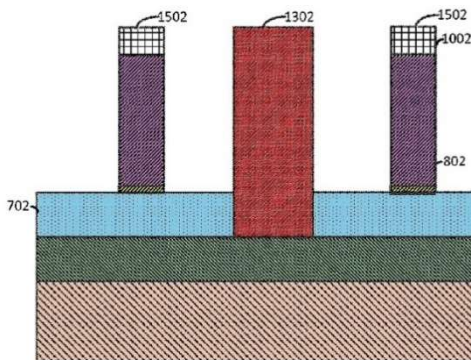
A-A Cross-Section

Inside Region R

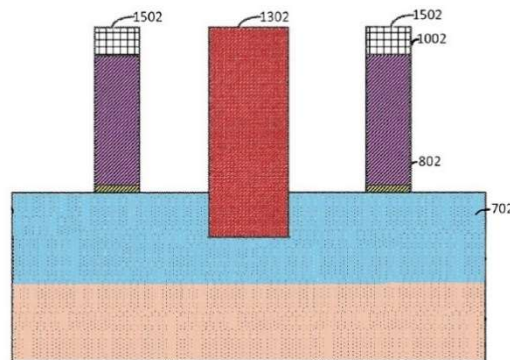
Ex-1003 ¶226

7. **Claim 6:** “The method of claim 5, further comprising: forming a cap layer on the gate structure and the SDB structure; and removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer adjacent to the SDB structure.”

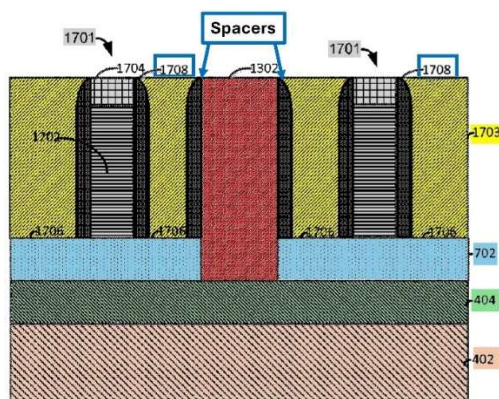
Ground 1A satisfies claim 5. (*Supra* §§VI.A.1-2, §VI.A.6.) Doris further discloses the “formation of spacers 1708 [circled in dark blue] ... adjacent to the dummy gate stacks 1502 (of FIG. 16).” (Doris ¶[0054]; *see id.*, FIGS. 16-17.) After also forming insulator material 1703 (yellow, *see supra* §VI.A.2.g), “[t]he dummy gate stacks 1502 are removed and replaced by the gate stacks 1701,” as shown below. (Doris ¶[0054]; *see Ex-1003* ¶[230].)



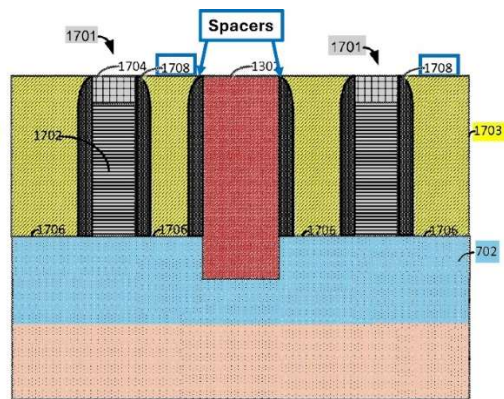
Doris, FIG. 16 (SOI)



Alternative FIG. 16 (Bulk Si)



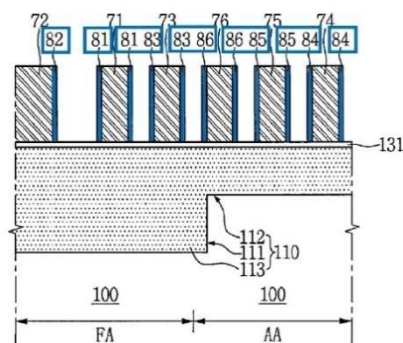
Doris, FIG. 17 (annotated)



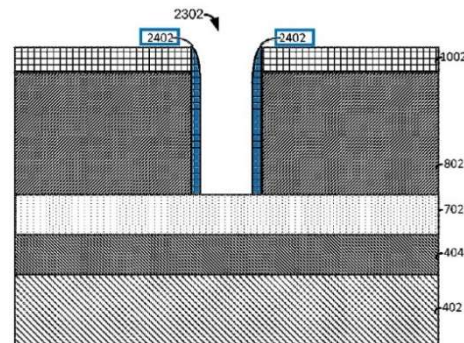
Alternative FIG. 17 (Bulk Si)

A POSITA would have understood how to make spacers 1708 using the same textbook semiconductor processing method for forming spacers that had been taught to students for decades. (Ex-1003 ¶231.) A layer of insulating material is conformally deposited over the protruding structures (dummy gate stacks 1502 and insulation material 1302), and then an anisotropic etch removes the deposited material from the horizontal surfaces, leaving vertical spacers on the sidewalls of the protruding structures. (Ex-1033, 19-20, Fig. 9-31(d); Ex-1028, 18, Fig. 9.16; Ex-1003 ¶231.)

Ha discloses the same textbook procedure for forming its analogous spacers 81-86: “The forming of the gate spacers 81 to 86 may include forming a silicon nitride layer by performing an ALD process, and then performing an etch-back process.” (Ha ¶[0095], FIGS. 3A-3C.) And Doris itself describes the same textbook procedure in a similar context: “The spacers 2402 [of FIG. 24] may be formed by, for example, depositing a nitride material ... and performing a RIE process” (Doris ¶[0060], FIG. 24; Ex-1003 ¶232.)



Ha, FIG. 3B

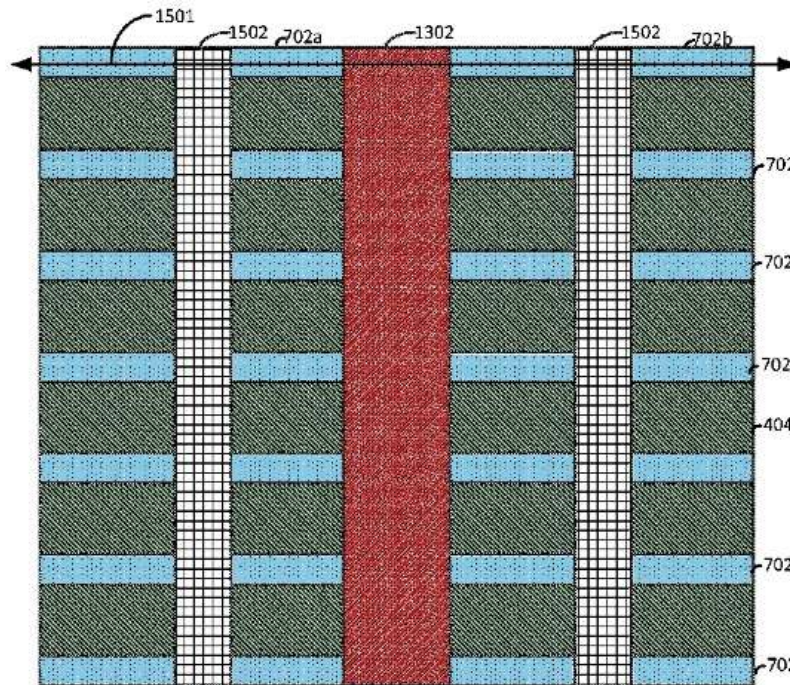


Doris, FIG. 24

Ground 1A thus renders obvious forming a cap layer on the gate structure (dummy gate stacks 1502) and the SDB structure (insulating material 1302) and removing part of the cap layer to form a first spacer (spacers 1708) adjacent to the gate structure and a second spacer (labeled “Spacers” in FIG. 17 above) adjacent to the SDB structure. (Ex-1003 ¶¶228-233.)

8. Claim 7: “The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.”

Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.) Further, Doris discloses that the fin-shaped structure (any of fins 702, blue) is disposed along a first direction (horizontal), and the SDB structure (insulator material 1302, red) is disposed along a second direction (vertical), as in FIG. 15. (Doris, FIG. 15; *see* Ex-1003 ¶¶234-236.)



Doris, FIG. 15

9. Claim 8: “The method of claim 7, wherein the first direction is orthogonal to the second direction.”

Ground 1A satisfies claim 7. (*Supra* §VI.A.1-2, §VI.A.8.) Further, as the preceding subsection demonstrates, the first direction (horizontal) is orthogonal to the second direction (vertical). (Doris, FIG. 15; Ex-1003 ¶¶237-238.)

10. Claim 9: “The method of claim 1, wherein the gate layer comprises amorphous silicon.”

Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.) Further, Doris discloses “the deposition of an amorphous silicon (α -Si) layer 802 over the fins 702.” (Doris ¶[0047].) Accordingly, the gate layer (layer 802) comprises amorphous silicon. (Ex-1003 ¶¶239-240.)

11. Claim 10: “The method of claim 1, wherein the gate layer comprises polysilicon.”

Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.) While Doris discloses “the deposition of an amorphous silicon (α -Si) layer 802 over the fins 702,” Doris also refers to layer 802 as “the α -Si (polysilicon) layer 802.” (Doris ¶[0047].) Accordingly, Doris discloses, and at least renders obvious, that the gate layer (layer 802) may comprise polysilicon, a known substitute for amorphous silicon in this context. (Ex-1003 ¶¶241-243; *infra* §VI.D.)

12. Claim 11: “The method of claim 1, wherein the dielectric layer comprises silicon nitride.”

Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.)

Further, Doris discloses “the deposition of an insulator material 1302 in the cavity 1202 (of FIG. 12) such as, for example an oxide or a nitride material.” (Doris ¶[0051].) Although not necessarily limited to *silicon* oxide and *silicon* nitride, a POSITA would have understood those to be, by far, the most evident “oxide or nitride material” disclosed. (Ex-1003 ¶246; *see* Doris ¶[0044] (referencing an “oxide material such as, for example silicon dioxide”); Ex-1016 ¶[0032] (“The gate separation structure 114 may be comprised of a variety of materials, e.g., silicon dioxide, silicon nitride, etc.”); Yu ¶[0036] (explaining “insulating layer 150 is made of silicon oxide or silicon nitride based materials”); Ha ¶[0107] (explaining “core layer 90 may include, for example, silicon nitride”); Zhao, 8:10-13 (disclosing “a layer of insulating material 123, such as silicon dioxide”).) Accordingly, Ground 1A discloses, and renders obvious, that the dielectric layer (insulator material 1302) comprises silicon nitride. (Ex-1003 ¶¶244-247.)

13. Claim 12: “The method of claim 1, wherein the dielectric layer comprises silicon oxide.”

Ground 1A satisfies claim 1. (*Supra* §§VI.A.1-2.) For the reasons in the preceding subsection, Doris discloses, and renders obvious, that the dielectric layer (insulator material 1302) comprises silicon oxide. (*Supra* §VI.A.12; Ex-1003 ¶¶248-251.)

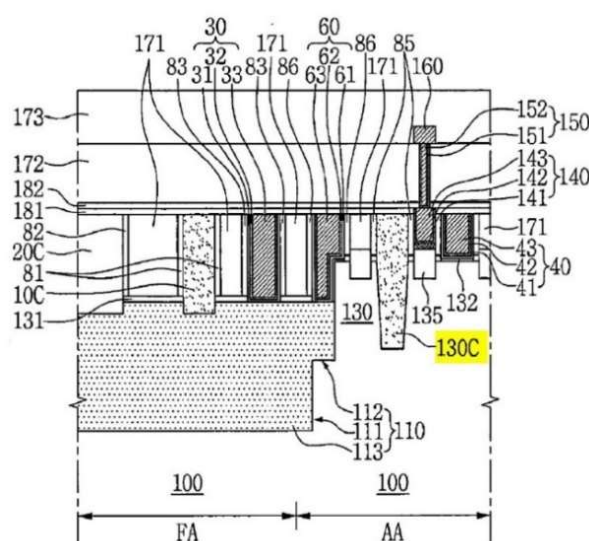
B. Ground 1B: Doris and Ha, Further in View of Colinge, Renders Claims 1-12 Obvious

Colinge was publicly accessible “within a few weeks of August 23, 2007” by “searching the Library of Congress catalog” and pulling “Call Number TK7872.T73 F56 2008.” (Ex-1032 ¶21; *see generally id.*) It is thus prior art under AIA §102(a)(1). Since Colinge is in the same field (FinFETs) and reasonably pertinent to a problem the ’880 Patent purports to address (FinFET fabrication), Colinge is analogous art. (*See* Ex-1001, 1:9-67; Colinge, 22-23, 37-38, Figs. 2.2, 2.14; Ex-1003 ¶90.)

For the reasons stated in Sections VI.A.1a-b, it would have been obvious to combine the teachings in Colinge, a FinFET textbook, with Doris and Ha. (Ex-1003 ¶252.) And for the reasons stated in Sections VI.A.2-13, claims 1-12 would have been obvious in view of such combination. (Ex-1003 ¶253.) The only difference is Ground 1A points to Colinge as evidence of POSITA knowledge, whereas Ground 1B expressly relies on Colinge itself. The arguments and rationales for both combinations, centering on Doris’s “bulk silicon” disclosure, is the same. (Ex-1003 ¶254.)

C. Grounds 2A and 2B: Ha Anticipates (Ground 2A) and Renders Obvious (Ground 2B) Claims 1-5, 7-8, and 10-11

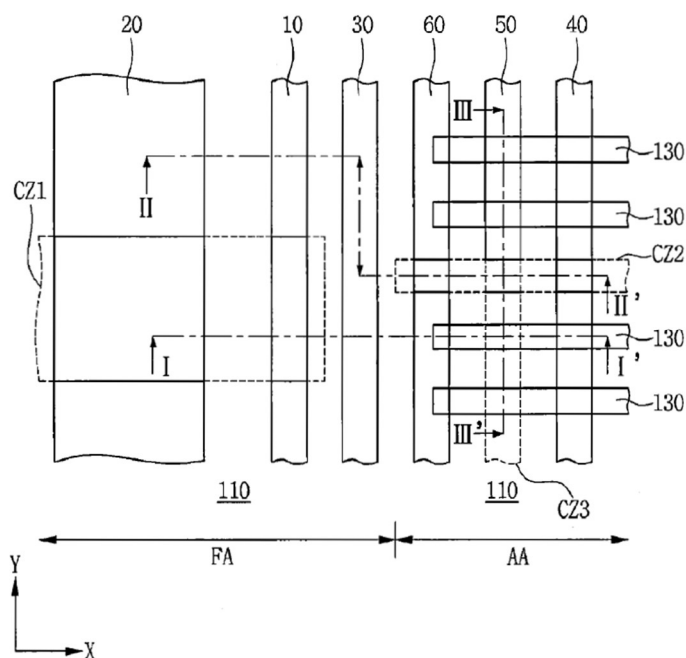
Ha describes FinFETs with “a fin active core and methods of fabricating the same.” (Ha ¶[0002].)



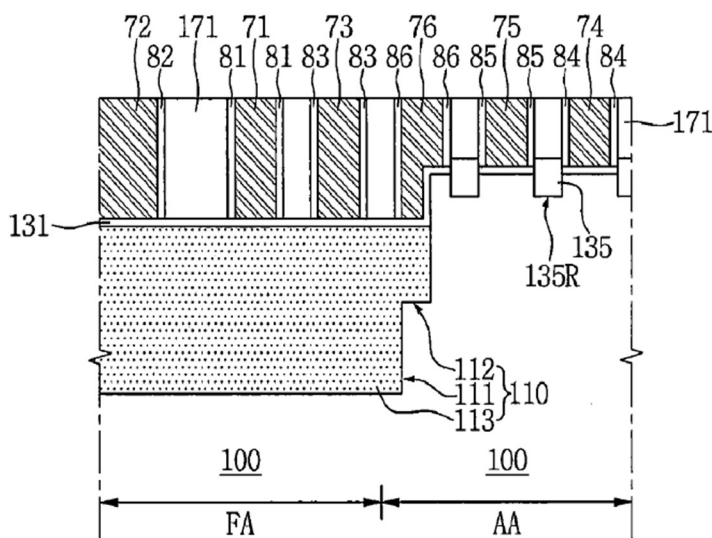
Ha, FIG. 2A

- | | |
|---------------|---------------------------------|
| 40/60: | fin gate pattern |
| 85: | fin gate spacers |
| 130: | active fin region |
| 130C: | fin active core |
| 135: | source/drain regions |
| 140: | contact pattern |
| 171: | 1st interlayer insulating layer |
| 172: | 2nd interlayer insulating layer |
| 173: | 3rd interlayer insulating layer |
| 181: | first stopper layer |
| 182: | second stopper layer |

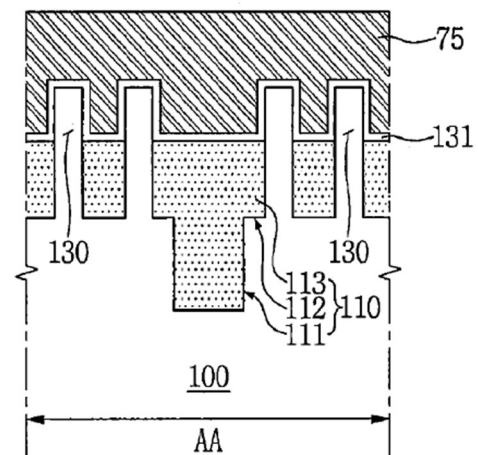
Ha's figures show cross-sections through FIG. 1. Figure numbers ending in A, B, or C shows cross-sections I–I', II–II', or III–III', respectively. (*Id.* ¶¶[0043]–[0044], ¶[0090].)

**Ha, FIG. 1**

Ha begins by forming isolation regions 110 around active fin 130, shown below. (*Id.* ¶¶[0091], ¶¶[0093]-[0094].) Sacrificial gate structures 71-76 (corresponding, respectively, to features 10-60 of FIG. 1) and gate spacers 81-86 are formed on a base insulating layer 131. (*Id.* ¶¶[0091], ¶¶[0095].) Source/drain regions 135 are formed between the gate spacers in the fin active area (AA), and a first interlayer insulating layer 171 is deposited and planarized. (*Id.* ¶¶[0096]-[0098], FIGS. 4A-4C.)

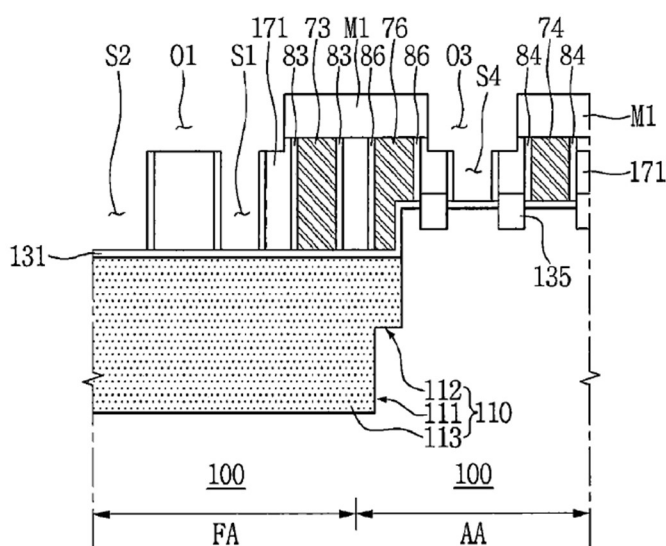


Ha, FIG. 4A

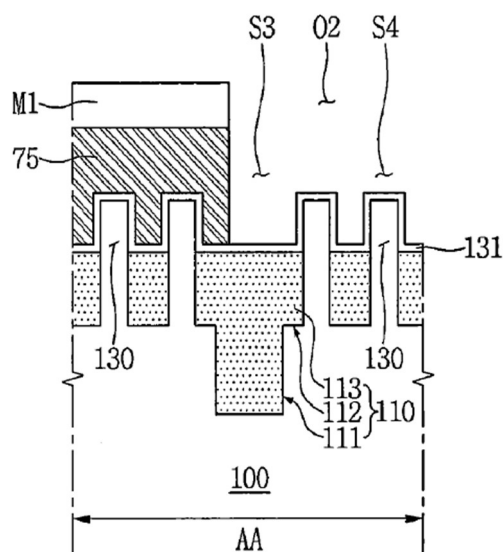


Ha, FIG. 4C

After patterning mask M1 with a fin active cut space opening O3 (which overlaps with fin gate cut opening O2 below), the exposed sacrificial gate structures are etched, as shown below. (*Id.* ¶¶0063, ¶¶0083, ¶¶0099]-[0102].)

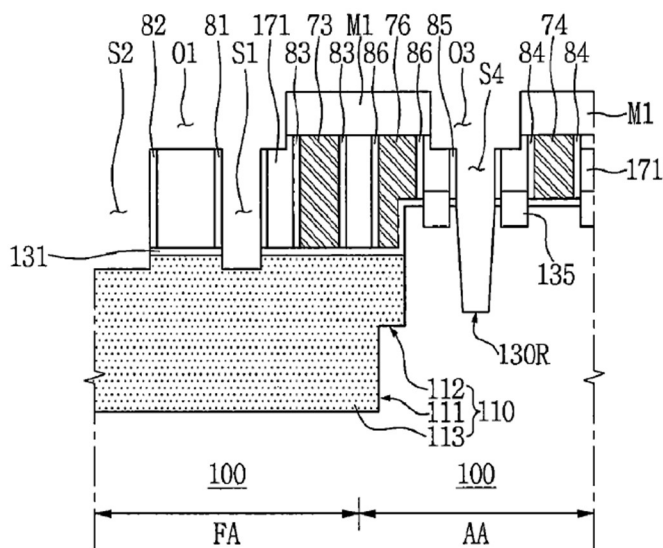


Ha, FIG. 5A

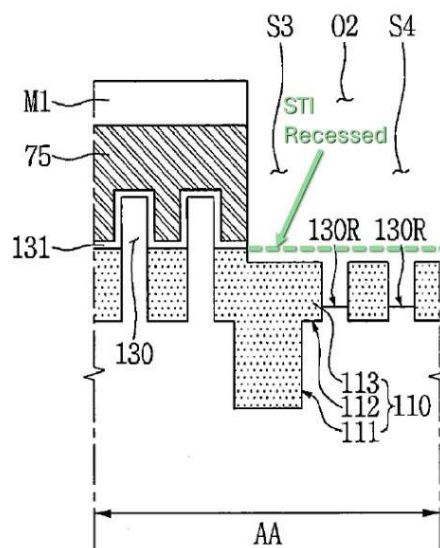


Ha, FIG. 5C

Next, fin active recesses 130R are formed by further etching fin active cut spaces S4, removing the exposed portions of base insulating layer 131 and recessing fin active region 130. (*Id.* ¶[0104].) This also recesses isolation region 110. (*Id.* ¶[0105].)

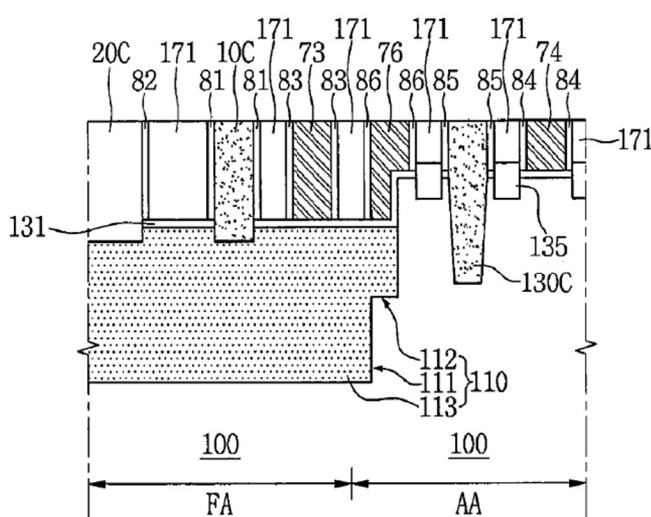


Ha, FIG. 6A

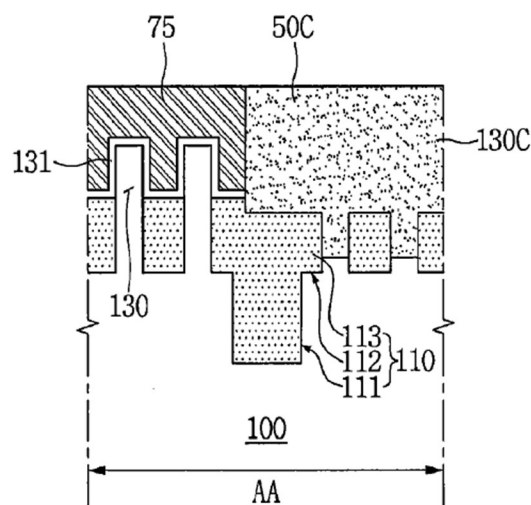


Ha, FIG. 6C

As shown below, dielectric material (e.g., silicon nitride) fills these openings and is planarized. (*Id.* ¶¶[0106]-[0111], FIGS. 7A-9C.) Ha explains: “[A] single diffusion break (SDB) structure can be implemented using [this] fin active cutting method.” (*Id.* ¶[0129].) For example, Ha’s “fin active core” (130C) “fill[s] ... [a] fin active cut space” to form an SDB structure. (*Id.* ¶[0109]; *see id.* ¶[0099].)

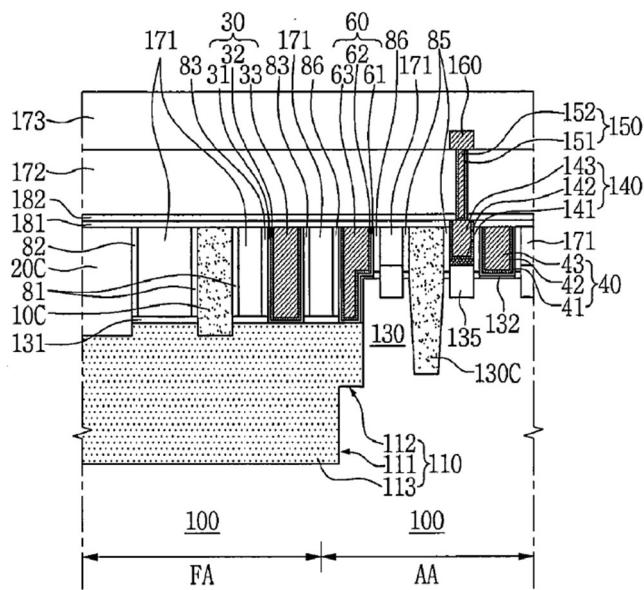


Ha, FIG. 9A

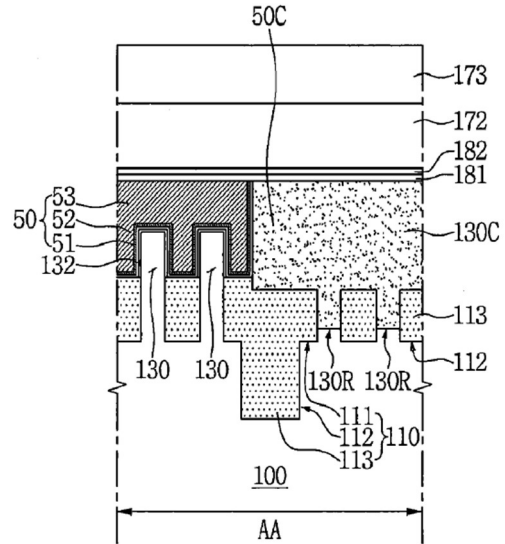


Ha, FIG. 9C

The remaining sacrificial gate structures are replaced with metal gates (e.g., gate pattern 40), and electrical contacts (contact pattern 140, via pattern 150, and interconnection 160) are made to source/drain regions 135. (*Id.* ¶¶[0112]-[0125], FIGS. 10A-14C.) This includes forming interlayer insulating layers 172 and 173. (*Id.*, ¶[0113], ¶¶[0119]-[0125].)



Ha, FIG. 2A



Ha, FIG. 2C

Because Ha is in the same field (FinFETs) and reasonably pertinent to a problem the '880 Patent purports to address (FinFET fabrication), Ha is analogous art. (*See* Ex-1001, 1:9-67; Ha ¶¶[0002]-[0003], ¶¶[0129]-[0131]; Ex-1003 ¶94.)

1. Independent Claim 1

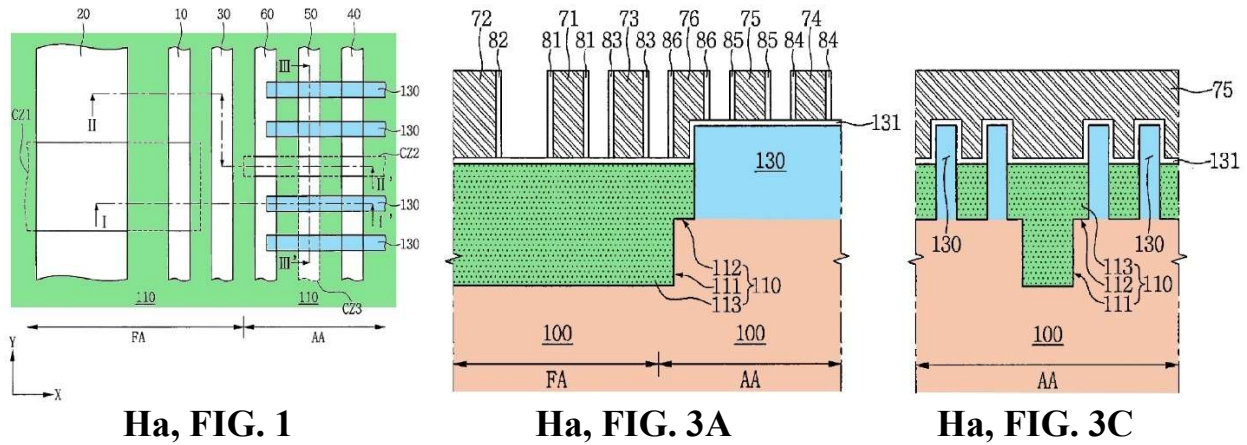
a. [1pre]

As shown above, Ha discloses “semiconductor devices ... and methods of fabricating the same.” (Ha, ¶[0002]; *see id.*, ¶¶[0071]-[0125], FIGS. 2A-14C; Ex-1003 ¶¶256-257.)

b. [1a] and [1b]

Ha discloses “forming an isolation region 110 which defines a fin active region 130 on the substrate 100.” (Ha, ¶¶[0091]; *see id.*, ¶¶[0092]-[0093], FIGS. 1,

3A-3C.) Thus, as shown below,⁶ Ha discloses [1a]: forming a fin-shaped structure (fin active region 130, blue) on substrate 100 (peach). (Ex-1003 ¶259.)

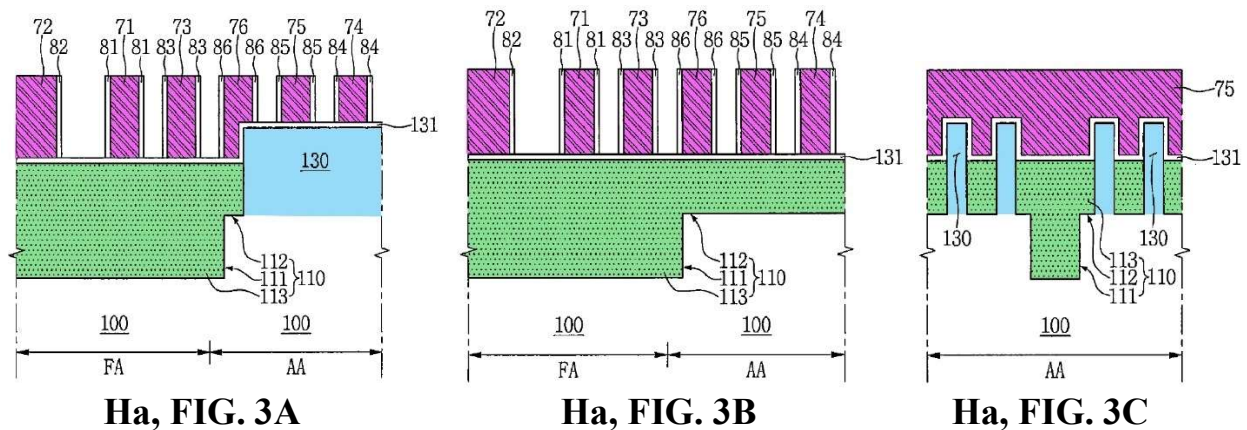


The substrate is first patterned to establish trenches, including shallow trenches 112 that define fins 130. Trench insulation material 113 is deposited into those trenches to form isolation region 110. (Ha ¶[0093] (“The isolation region 110 may include a trench insulation material 113 which fills ... shallow trench 112.”).) Accordingly, Ha also discloses [1b]: forming insulation material 113 in shallow trenches 112 (STI) around the fin active region 130 (fin-shaped structure). (Ex-1003 ¶¶258-261.)

⁶ Ha’s figures ending in A, B, or C lie on cross-sections I–I’, II–II’, or III–III’, respectively. (*Id.* ¶¶[0043]–[0044], ¶[0090].)

c. [1c]

Ha's discloses "forming a base insulating layer 131 on surfaces of the fin active region 130 and the isolation region 110, and forming sacrificial gate patterns 71 to 76 and gate spacers 81 to 86 on the base insulating layer 131." (Ha ¶[0091].) Sacrificial gate patterns 71-76 include "a sacrificial first fin gate pattern 74, a sacrificial second fin gate pattern 75, and a sacrificial butting gate pattern 76," each formed on the fin active region 130 (fin-shaped structure) and shallow trenches 112 (STI), as shown below. (*Id.* ¶[0095]; *see id.*, FIGS. 3A-3C.)



A POSITA would have understood (Ground 2A), and at least found obvious (Ground 2B), that sacrificial gate patterns 71-76 are patterned from the same layer (i.e., from the same gate layer). (*See* Ha ¶[0095] ("The sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon."); Ex-1003 ¶[265].) Additionally, although inconsistent with the '880 Patent's only supporting embodiment (*see* Ex-1001, 3:3-10, 4:8-14), sacrificial gate patterns 71 to 76, or

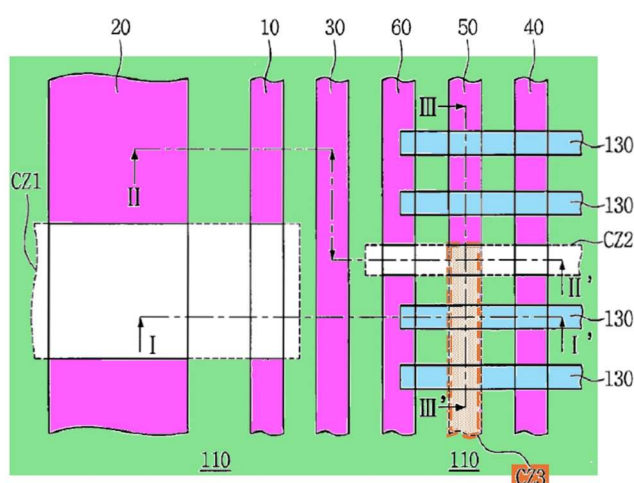
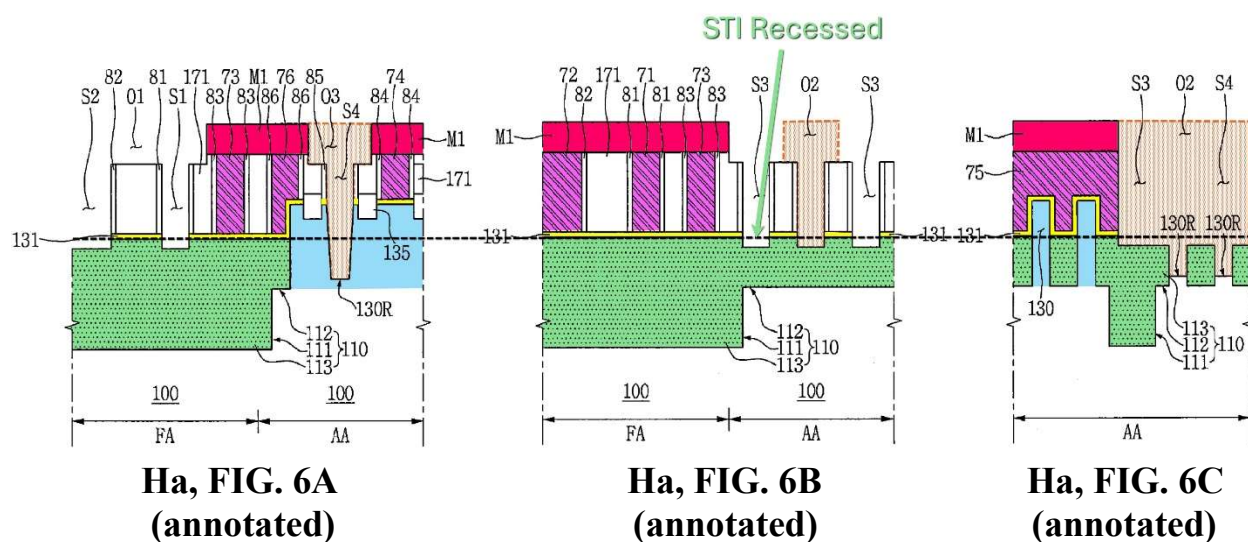
sacrificial gate pattern 75 alone, may be considered a “gate layer” under a broad interpretation of the claims Patent Owner may assert (*see* Ex-1035 ¶89; Ex-1003 ¶¶266-267).

Regardless, Ha discloses (Ground 2A), and at least renders obvious (Ground 2B), forming a gate layer (polysilicon film for gate patterns 71-76, gate patterns 71-76 themselves, or gate pattern 75 alone) on fin active region 130 (fin-shaped structure) and insulation material 113 in shallow trenches 112 (STI). (Ex-1003 ¶¶262-268.)

d. [1d]

Ha discloses “forming a first mask pattern M1” and “removing portions of the sacrificial gate patterns 71 to 76 ... using the first mask pattern M1 as an etch mask.” (Ha ¶[0099]; *see id.*, FIGS. 5A-6C.) As shown below, mask pattern M1 includes “a fin active cut opening O3 corresponding to ... the fin active cut-zone CZ3 of FIG. 1.”⁷ (*Id.* ¶¶[0100]-[0101].) Ha further discloses “forming a fin active recess 130R by ... recessing the fin active region 130” and that, additionally, “isolation region 110 ... may be recessed.” (Ha ¶¶[0104]-[0105].)

⁷ Fin active cut-zone CZ3 and fin gate cut-zone CZ2 intersect where cross-sections II–II' and III–III' intersect. (Ha ¶[0063], ¶[0083], FIG. 1.)

**Ha, FIG. 1**

Thus, if removing a dummy gate pattern qualifies as removing part of the gate layer (as Patent Owner may assert), Ha discloses removing part of the gate layer,⁸ part of the fin-shaped structure (fin active region 130), and part of the STI (insulation material 113 in shallow trenches 112) to form a trench (orange) in fin active cut-

⁸ See *supra* §VI.C.1.c (discussing mappings of “gate layer” in the context of [1c]).

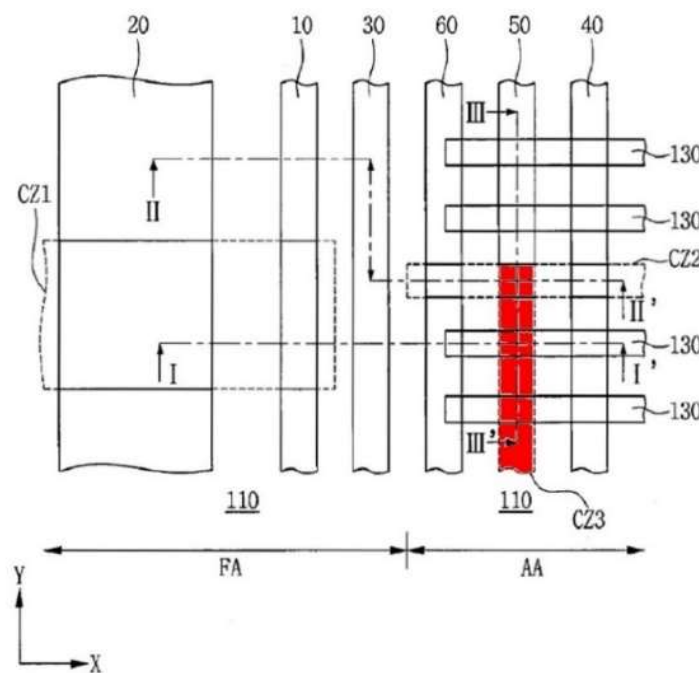
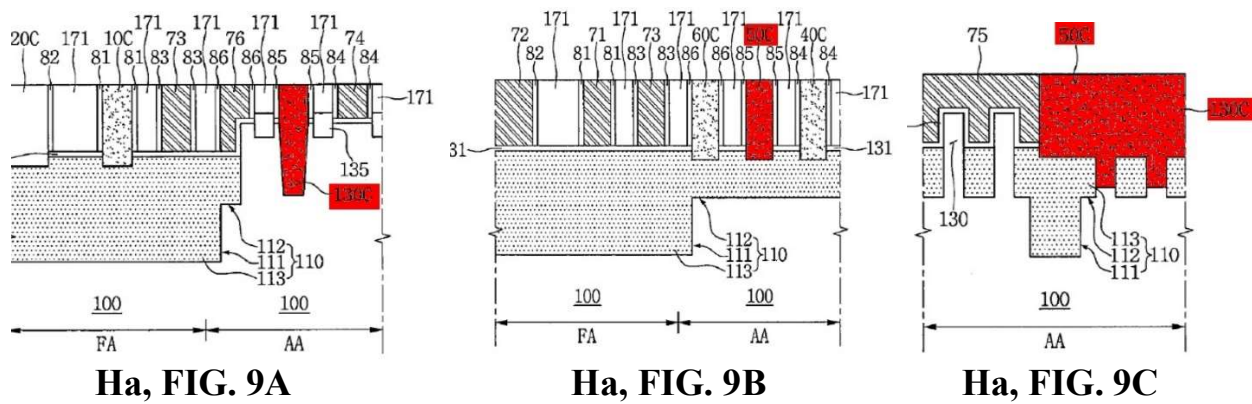
zone CZ3 that includes fin active recess 130R. (Ha ¶¶[0099]-[0105], FIGS. 1, 5A-6C; Ex-1003 ¶¶269-271.)

e. [1e]

Ha explains: “[A] single diffusion break (SDB) structure can be implemented using [its] *fin active cutting* method.” (*Id.* ¶[0129] (emphasis added).) A POSITA would have understood (Ground 2A), and at least found obvious (Ground 2B), that Ha describes such an SDB structure when it discloses “forming an insulating core layer 90 which completely or partially fills ... the *fin active cut space* S4, and the *fin active recess* 130R.” (Ha ¶[0106] (emphases added); *see id.*, FIGS. 7A-7C.) Insulating core layer 90 may be a layer of silicon nitride (a dielectric). (*Id.* ¶[0107]; *see* Ex-1003 ¶273.)

Ha further discloses “forming ... a *fin active core* 130C by partially removing the core layer 90.” (*Id.* ¶[0108] (emphasis added).) *Fin active core* 130C “fill[s] ... the *fin active cut space* S4, [and] the *fin active recess* 130R” in *fin active cut-zone* CZ3 (comprising the trench). (*Id.* ¶[0109] (emphases added); *see id.* ¶[0083], FIGS. 1, 6A-8C.)

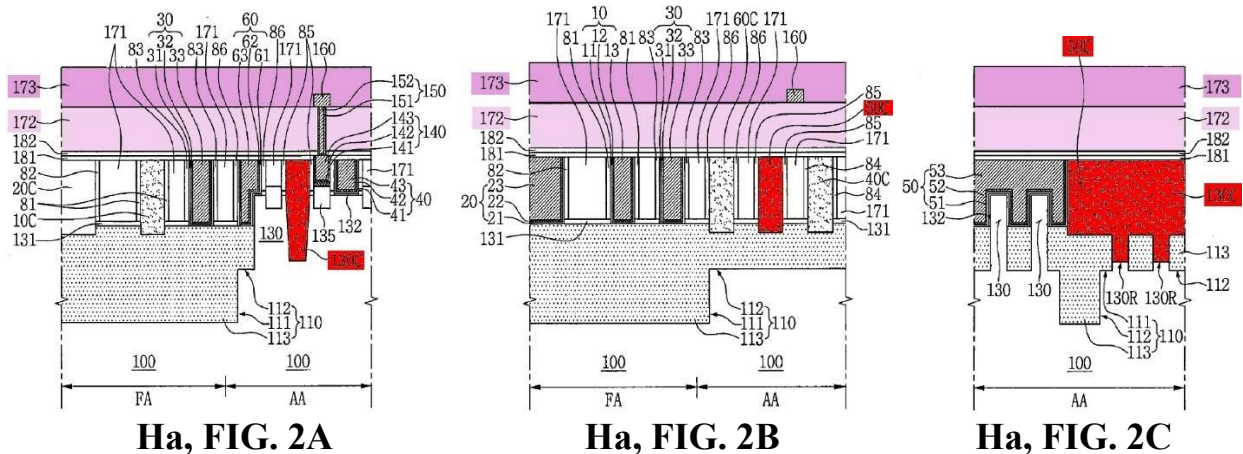
Ha then discloses removing mask pattern M1 and performing planarization to expose the remaining portions sacrificial gate patterns 71-76 (see below). (Ha ¶¶[0110]-[0111], FIGS. 9A-9C.)



Ha thus discloses (Ground 2A), and at least renders obvious (Ground 2B), forming a dielectric layer (e.g., silicon nitride) into the trench (fin active cut-zone CZ3) to form what Ha characterizes as “a single diffusion break (SDB) structure” (fin active core 130C) (red above). (Ha ¶[0129]; *see* Ex-1001, 3:39-59, FIGS. 5-6; Ex-1003 ¶¶272-276.) As in any SDB, Ha’s fin active core 130C cuts fins 130 and lies directly adjacent to source/drain regions 135. (*See supra* §II.C; Ex-1003 ¶274.)

f. [1f]

Ha discloses “forming a second interlayer insulating layer 172” made of silicon oxide and “forming a third interlayer insulating layer 173” made of silicon oxide or silicon nitride. (Ha ¶[0122], ¶[0124]; *see id.*, FIGS. 2A-2C, 14A-14C.)



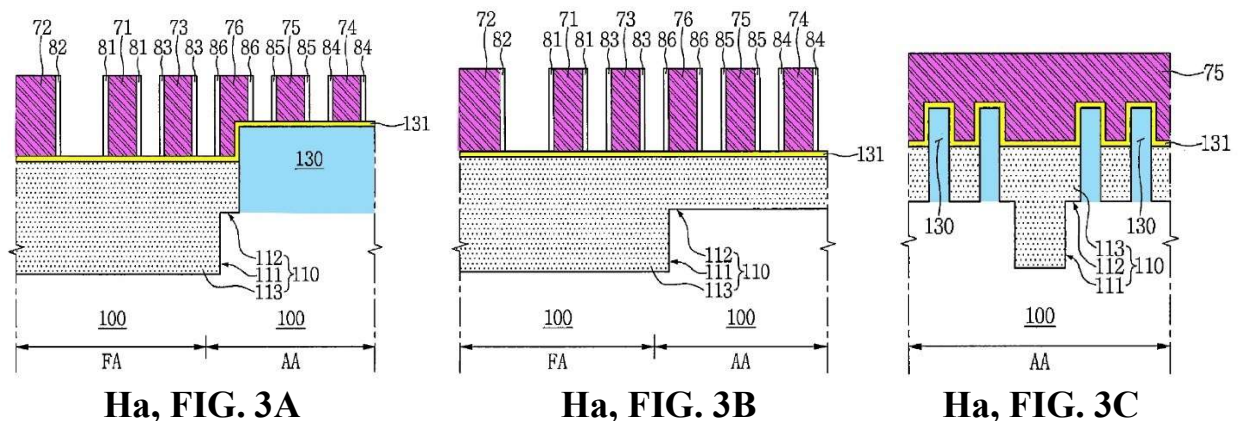
As shown above, interlayer insulating layers 172 and 173 are formed after— and on—fin active core 130C (the SDB structure). (*See id.* ¶¶[0122]-[0125], FIGS. 2A-2C, 14A-14C; *supra* §VI.C.1.e; Ex-1003 ¶279.) A POSITA would have understood *interlayer insulating layers* 172 and 173 are *interlayer dielectric layers* (“ILD” layers) because silicon oxide and nitride are dielectrics. (Ex-1003 ¶279.)

Applying Patent Owner’s litigation position (*supra* §III.C), *any* ILD layer, including Ha’s ILD layers 172 and/or 173, would satisfy claim 1. Under that view, Ha discloses forming an ILD layer (Ha’s ILD layer 172 and/or 173) on the SDB structure (fin active core 130C) after forming the SDB structure. (Ex-1003 ¶¶277-280.)

2. Claim 2

Ha discloses claim 1 under Patent Owner's apparent view. (*Supra* §VI.C.1.)

Additionally, Ha discloses “forming a base insulating layer 131 on surfaces of the fin active region 130 and the isolation region 110, and forming sacrificial gate patterns 71 to 76 and gate spacers 81 to 86 on the base insulating layer 131.” (Ha ¶[0091].) “The base insulating layer 131 may include silicon oxide.” (*Id.* ¶[0094].) Thus, as shown below, Ha discloses forming a gate dielectric layer (base insulating layer 131) on the fin-shaped structure (fin active region 130) before forming the gate layer (polysilicon film for gate patterns 71-76, gate patterns 71-76 themselves, or gate pattern 75 alone). (Ex-1003 ¶¶281-284.)

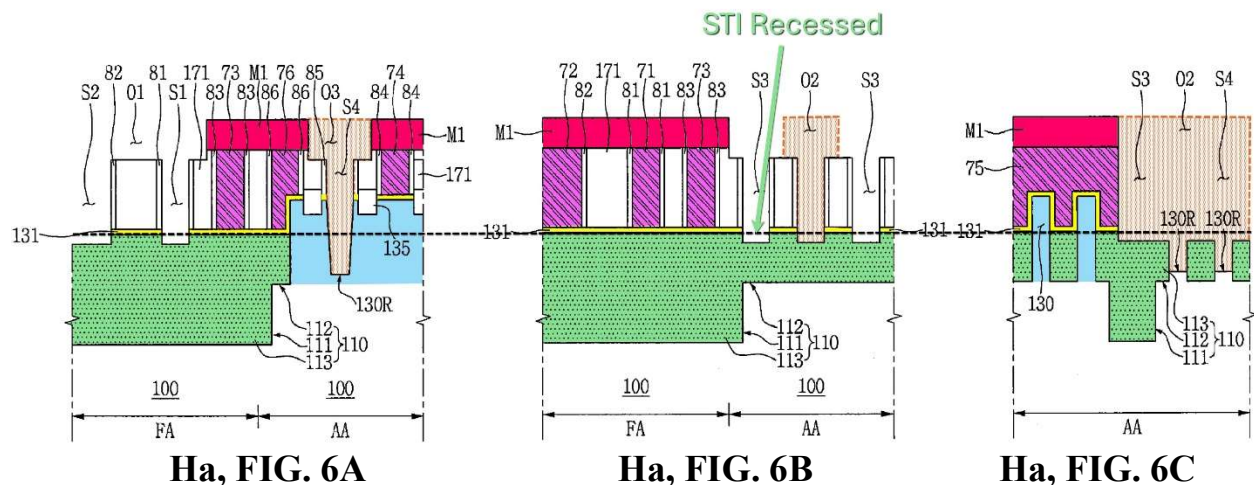


A POSITA would have understood base insulating layer 131 (yellow) is a gate dielectric layer because it sits between the fins 130 (blue) and the gate patterns (magenta), where a FinFET gate dielectric layer resides, and silicon oxide is a dielectric. (Ex-1001, 3:3-10, FIG. 2; Ex-1003 ¶285.) Although base insulating

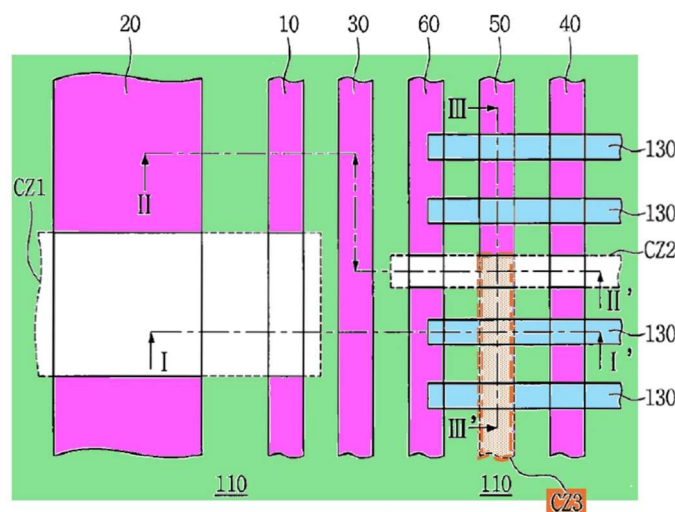
layer 131 is replaced by a high-k gate dielectric in the final structure, the '880 Patent is no different. (*Compare* Ha, ¶[0091], ¶[0094], ¶¶[0112]-[0115], FIGS. 3A-3C, 11A-11C, *with* Ex-1001, 3:3-10, 5:11-42, FIGS. 2, 10; *see* Ex-1003 ¶286.)

3. Claim 3

Ha discloses claim 2 under Patent Owner's apparent view. (*Supra* §§VI.C.1-2.) Ha further discloses "forming a first mask pattern M1" and "removing portions of the sacrificial gate patterns 71 to 76 ... using the first mask pattern M1 as an etch mask." (Ha ¶[0099]; *see id.*, FIGS. 5A-6C.) Moreover, "[t]he base insulating layer 131 may be exposed by removing the portions of ... the sacrificial second fin gate pattern 75 ... which are exposed in ... the fin active cut opening O3." (Ha ¶[0101].) Then, "the method may include forming a fin active recess 130R by removing the base insulating layer 131 exposed in the fin active cut space S4 and recessing the fin active region 130." (*Id.* ¶[0104].)



Thus, Ha discloses forming a patterned mask (mask pattern M1, red) on the gate layer (magenta) and using the patterned mask as a mask to remove part of the gate layer, part of the gate dielectric layer (base insulating layer 131, yellow), and part of the fin-shaped structure (fin 130, blue) to form the trench (orange). (Ha ¶¶[0099]-[0105], FIGS. 5A-6C; *supra* §VI.C.1.d; Ex-1003 ¶¶287-290.)

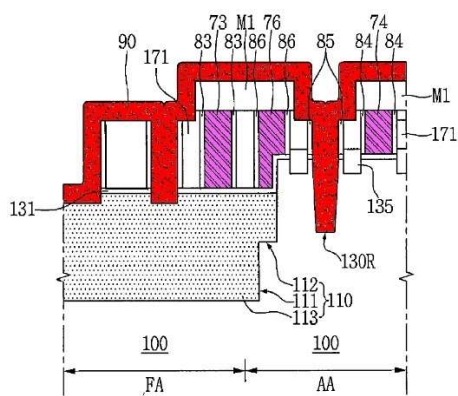


Ha, FIG. 1

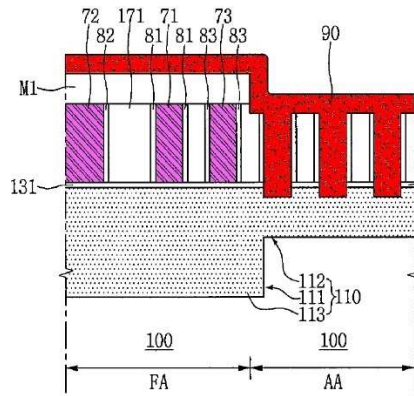
4. Claim 4

Ha discloses claim 1 under Patent Owner's apparent view. (*Supra* §VI.C.1.)

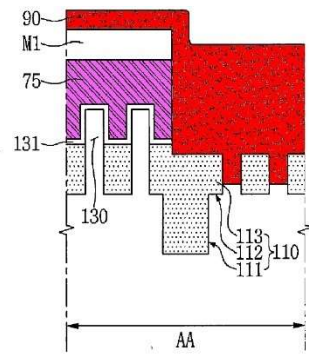
Ha further discloses “forming an insulating core layer 90 which completely or partially fills ... the fin active cut space S4, and the fin active recess 130R” (comprising the trench). (Ha ¶[0106].) “[T]he insulating core layer 90 [dielectric layer, red] may be formed semi-conformally,” such that it (a) fills the trench (*supra* §VI.C.1.e) and (b) forms on the gate layer (magenta), as shown below. (Ha ¶[0106]; *see id.*, FIGS. 7A-7C; Ex-1003 ¶293.)



Ha, FIG. 7A

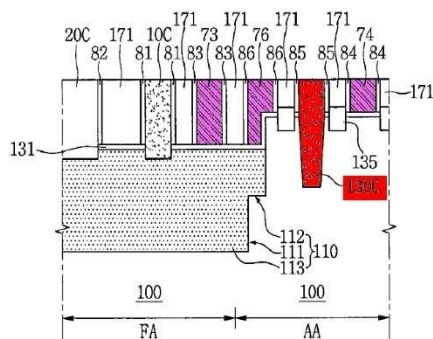


Ha, FIG. 7B

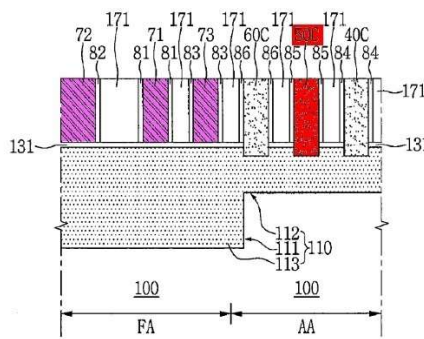


Ha, FIG. 7C

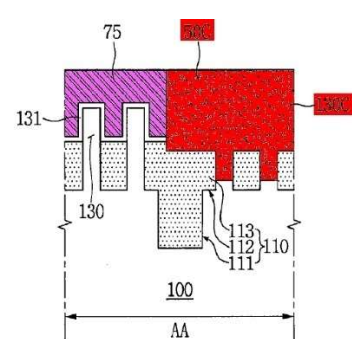
Additionally, Ha discloses “forming silicon oxide, removing the first mask pattern M1 and exposing the sacrificial gate patterns 71 to 76 by performing a planarization process.” (Ha ¶[0110].) Accordingly, “[u]pper surfaces of the remaining sacrificial gate patterns 71 to 76, ... the first and second fin gate cores 40C and 50C, ... and the fin active core 130C may be coplanar.” (*Id.* ¶[0111]; *see id.*, FIGS. 9A-9C.) Thus, Ha discloses planarizing the dielectric layer so the top surfaces of the dielectric layer (red) and the gate layer (magenta) are coplanar, as shown below. (Ex-1003 ¶¶291-295.)



Ha, FIG. 9A



Ha, FIG. 9B

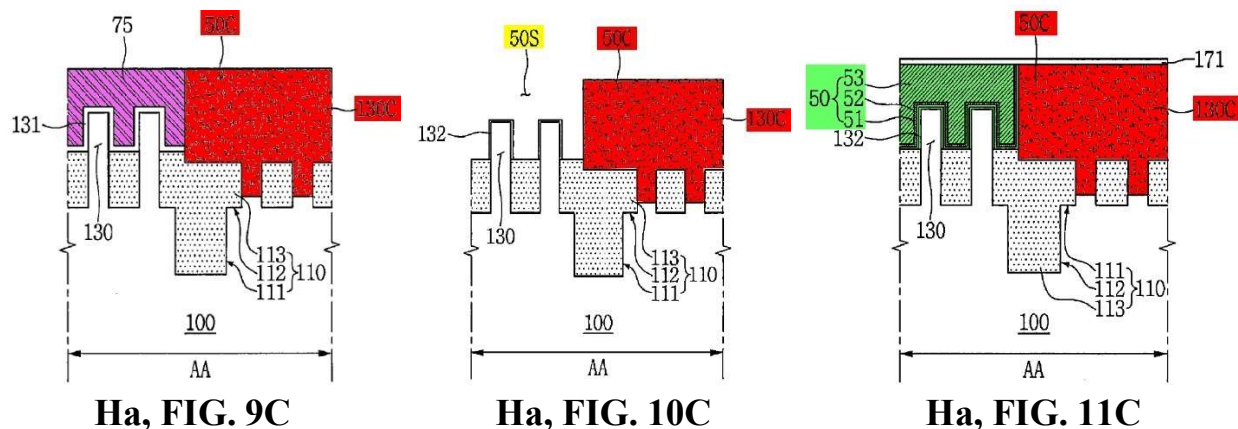


Ha, FIG. 9C

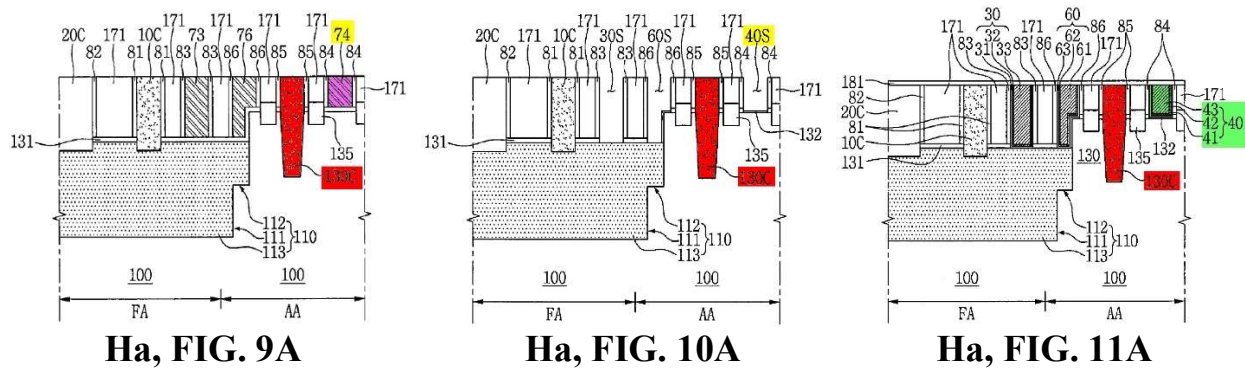
5. Claim 5

Ha discloses claim 1 under a view Patent Owner may assert. (*Supra* §VI.C.1.)
Ha discloses the additional features of claim 5 under that view, too. (Ex-1003 ¶¶296-302; *see supra* §VI.C.1.d ([1d]).)

Under one mapping, the gate layer is gate pattern 75. (*Supra* §VI.C.1.c.) As the transition from FIG. 9C to FIG. 10C shows in part, Ha discloses “forming gate electrode spaces 10S, 20S, 30S, 40S, 50S, and 60S by removing the exposed sacrificial gate patterns 71 to 76.” (Ha ¶[0112].) And as the transition from FIG. 10C to FIG. 11C shows in part, Ha further discloses “forming gate patterns 10, 20, 30, 40, 50, and 60 in the gate electrode spaces.” (*Id.* ¶[0113]; *see id.* ¶¶[0114]-[0115].) Ha thus discloses removing part of the gate layer (sacrificial gate pattern 75, magenta) after forming the SDB structure (red) to form a gate structure (gate pattern 50, green) adjacent to the SDB structure. (Ex-1003 ¶¶297-299.)



Under another mapping, the gate layer is the silicon film for gate patterns 71-76, collectively. (*Supra* §§VI.C.1.c-d.) Ha thus would satisfy claim 5 under the second mapping for the same reason it would satisfy claim 5 under the first mapping. (Ex-1003 ¶300.)



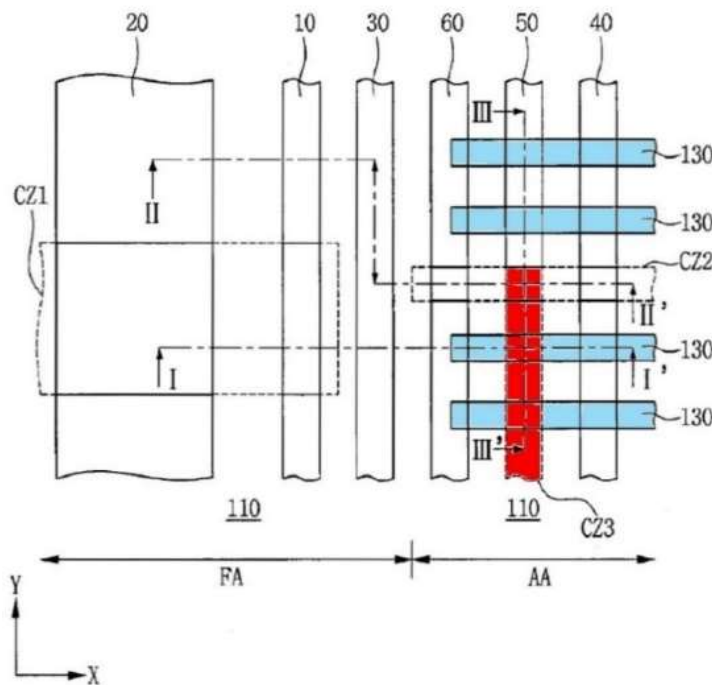
Additionally, Ha satisfies claim 5 under this mapping as shown above. Ha discloses removing part of the gate layer (part of sacrificial gate pattern 74, magenta) after forming the SDB structure (red) to form a gate structure (gate pattern 40, green) adjacent to the SDB structure. (Ha ¶¶[0112]-[0115], FIGS. 9A-11C; Ex-1003 ¶¶301-302.)

Although these mappings view the final metal gate as the claimed “gate structure,” whereas the ’880 Patent contemplates a dummy gate (*see* Ex-1001, 4:8-14, FIG. 8), these mappings are consistent with a view Patent Owner may assert (*see supra* §III.C; Ex-1035 ¶89.)

6. Claim 7

Ha discloses claim 1 under Patent Owner’s apparent view. (*Supra* §VI.C.1.)

Additionally, Ha discloses that “fin active regions 130 ... extend in parallel in the X direction” and that “fin active cut-zone CZ3 ... extend[s] in the Y direction.” (Ha ¶¶0058], ¶¶0062]; *see id.* ¶¶0028].) Thus, as FIG. 1 shows below, the fin-shaped structure (active fin 130, blue) extends along a first direction (X), and the SDB structure (coincident with fin active cut-zone CZ3, red) extends along a second direction (Y). (*See supra* §VI.C.1.e; Ex-1003 ¶¶303-305.)



Ha, FIG. 1

7. Claim 8

Ha discloses claim 7 under Patent Owner's apparent view. (*Supra* §VI.C.1, §VI.C.6.) Additionally, as illustrated above, the first direction (X) is orthogonal to the second direction (Y). (Ha ¶[0028], ¶[0058], ¶[0062], FIG. 1; *supra* §VI.C.6; Ex-1003 ¶¶306-308.)

8. Claim 10

Ha discloses claim 1 under Patent Owner's apparent view. (*Supra* §VI.C.1.) Ha further discloses that the gate layer (polysilicon film for gate patterns 71-76, collectively, gate patterns 71-76 themselves, or the gate pattern 75 alone) comprises polysilicon. (*Supra* §VI.C.1 ([1c]); Ex-1003 ¶311 n.28.) Ha explains "sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon" (i.e., polysilicon). (Ha ¶[0095]; *see id.*, ¶[0009] ("[T]he sacrificial fin gate pattern may include polysilicon"), claim 4 (similar); Ex-1003 ¶¶309-311.)

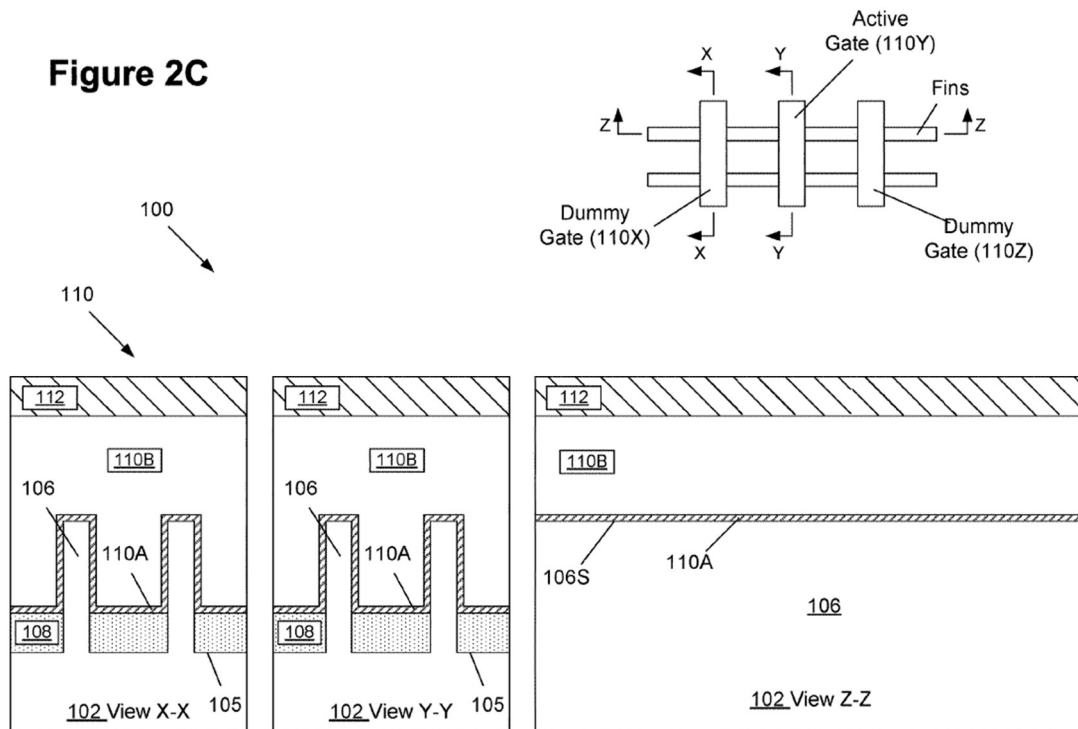
9. Claim 11

Ha discloses claim 1 under Patent Owner's apparent view. (*Supra* §VI.C.1.) Additionally, Ha discloses that the dielectric layer (insulating core layer 90) "may include ... silicon nitride." (Ha ¶[0107]; *see id.* ¶[0017], ¶[0072], ¶[0083], claims 4, 12; *supra* §VI.C.1.e; Ex-1003 ¶¶312-314.)

D. Ground 2C: The Combination of Ha and Zhao Renders Obvious Claim 9

Zhao describes "the manufacture of semiconductor devices, and, more specifically, ... various novel methods of forming diffusion breaks [140] on integrated circuit (IC) products comprised of FinFET devices." (Zhao, 1:8-12; *see id.*, 4:3-5, 5:8-26, 9:10-14.)

Figure 2C



Zhao, FIG. 2C

Zhao’s structure is completed by replacing dummy gates 110X and 110Z with “an isolation structure 140, or [single] diffusion break” and performing a metal gate process in dummy gate 110Y. (*Id.*, 9:10-14; *see id.*, FIG. 2R; *see id.*, 6:43-9:45, FIGS. 2D-2R.)

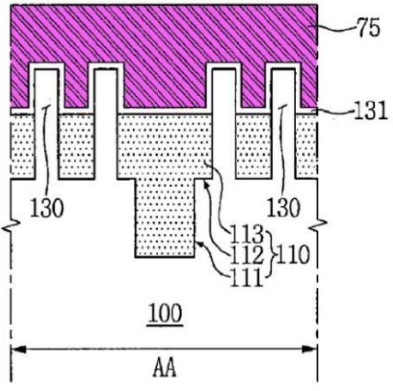
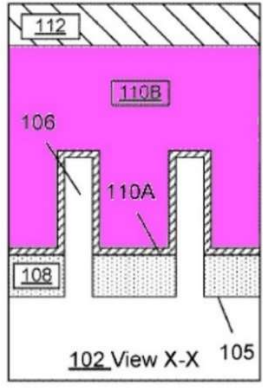
Because Zhao is in the same field (FinFETs) and reasonably pertinent to a problem the ’880 Patent purports to address (FinFET fabrication), Zhao is analogous art. (*See* Ex-1001, 1:9-67; Zhao, 1:8-12, 3:40-60; Ex-1003 ¶109.)

1. A POSITA would have found it obvious to make Ha’s sacrificial gate structures using amorphous silicon, as Zhao discloses

According to Ha, sacrificial gate patterns 71-76 “may include” polysilicon, “for example.” (Ha, ¶[0009], ¶[0095]; *supra* §VI.C.8 (claim 10).) A well-known

substitute for polysilicon was amorphous silicon, which is very similar. (Ex-1003 ¶315; *see* Ex-1034 ¶[0013].) Zhao, for example, explains that its sacrificial gate electrode material 110B (equivalent to the material for Ha’s sacrificial gate patterns 71-76) comprises “polysilicon or amorphous silicon.” (Zhao, 6:36-42.)

As the table below demonstrates, Ha and Zhao disclose similar dummy gate structures. (*Compare* Ha ¶[0009], ¶[0095], FIGS. 1, 3A-3C, *with* Zhao, 6:28-42, FIG. 2C; Ex-1003 ¶¶315-316.) Although the exemplary material for Ha’s sacrificial gate patterns 71-76 is polysilicon, it is just that—exemplary. (Ha ¶[0009], ¶[0095].) Zhao makes clear that amorphous silicon, a well-known polysilicon substitute, also may be used for sacrificial gate structures when forming SDBs. (*See* Zhao, 6:36-42; *see* Ex-1034 ¶[0013]; Ex-1003 ¶¶317-318.)

Ha	Zhao
 Ha, FIG. 9B	 Zhao, FIG. 2C (excerpted)
“[T]he sacrificial fin gate pattern may include polysilicon” (Ha ¶[0009].)	“[T]he sacrificial gate electrode material 110B is comprised of a material such as polysilicon or amorphous silicon” (Zhao, 6:36-42.)

Ha	Zhao
“The sacrificial gate patterns 71 to 76 each may include, for example, polycrystalline silicon.” (Ha ¶[0095].)	“[S]acrificial gate materials of said first, second and third gate structures are comprised of one of polysilicon or amorphous silicon” (Zhao, claim 16.)

A POSITA would have been motivated to make that substitution since polysilicon and amorphous silicon have similar properties. (Ex-1003 ¶319.) Whether Ha’s gate layer is polysilicon or amorphous silicon is immaterial. Both were known for forming FinFET dummy gates. (Ex-1003 ¶¶319-320; *see* Zhao, 6:36-42, claim 16, FIG. 2C; Ex-1034 ¶[0013].) And “if there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is a motivation to combine.” (*Intel*, 61 F.4th at 1379-81 (quoting *Intel*, 21 F.4th at 799-800).)

A POSITA would have reasonably expected success because such substitution would not have been expected to affect any other steps in Ha’s process or to materially affect the final device. (Ex-1003 ¶321.) For example, amorphous silicon sacrificial gates 71-76 would be equally suitable for removal as shown in FIGS. 5A-5C, planarization as shown in FIGS. 9A-9C, and removal and replacement with metal gates as shown in FIGS. 10A-11C. (Ex-1003 ¶321.)

Consistent with Zhao’s disclosures, a POSITA thus would have found it obvious to make Ha’s sacrificial gate patterns 71-76 using amorphous silicon rather than polysilicon. (Ex-1003 ¶322.) Such a substitution would have been viewed as an obvious example of (1) substituting one known element for another (amorphous silicon for polysilicon) to obtain predictable results; (2) a choice from among a finite number of identified, predictable solutions (polysilicon or amorphous silicon (*see* Zhao, 6:28-42, claim 16)), with reasonable expectation of success; and (3) a teaching, suggestion, or motivation in the prior art (*see id.*) that would have led a POSITA to modify Ha and arrive at the claimed invention. (*See KSR*, 550 U.S. at 416-21; Ex-1003 ¶322.)

2. Claim 9

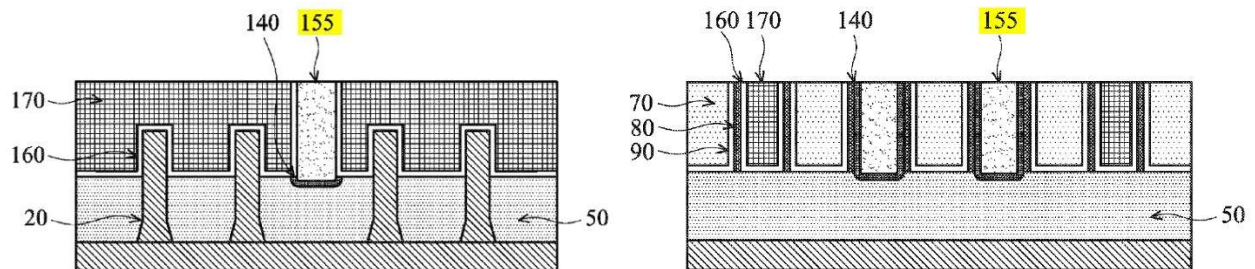
Ha discloses claim 1 under Patent Owner’s apparent view. (*Supra* §VI.C.1.) The combination of Ha and Zhao does not materially affect that analysis. (Ex-1003 ¶324.) Additionally, in the combination of Ha and Zhao, Ha’s gate layer comprises amorphous silicon. (*Supra* §VI.D.1, Ex-1003 ¶¶323-325.)

E. Ground 2D: The Combination of Ha and Yu Renders Obvious Claim 12

Yu describes “a semiconductor device having a fin structure and its manufacturing process.” (Yu ¶[0001].) This involves fabricating first and second

gate structures “separated by a separation plug [155] made of an insulating material.”

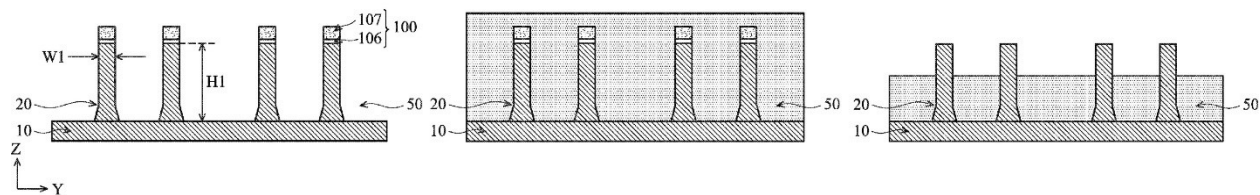
(*Id.*, Abstract, FIGS. 10A-10B.)



Yu, FIG. 10A (looking down the fins) Yu, FIG. 10B (fins running left/right)

- | | |
|--|-----------------------------------|
| 20: fin structures | 90: CESL layer |
| 50: isolation insulating layer | 140: thin insulating layer |
| 70: interlayer dielectric layer (ILD) | 155: separation plug |
| 80: sidewall insulating layers | 160: gate dielectric layer |
| | 170: gate electrode layer |

First, fins 20 are etched into substrate 10, and isolation insulating layer 50 (e.g., silicon oxide) is formed around them. (Yu ¶¶[0011]-[0022], FIGS. 1-3.)



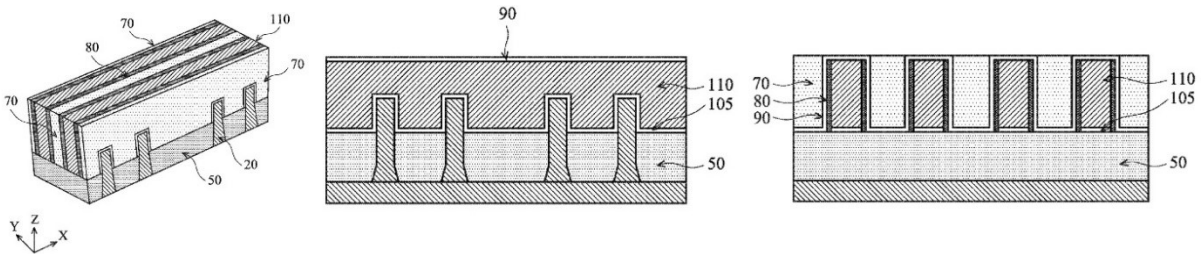
Yu, FIG. 1

Yu, FIG. 2

Yu, FIG. 3

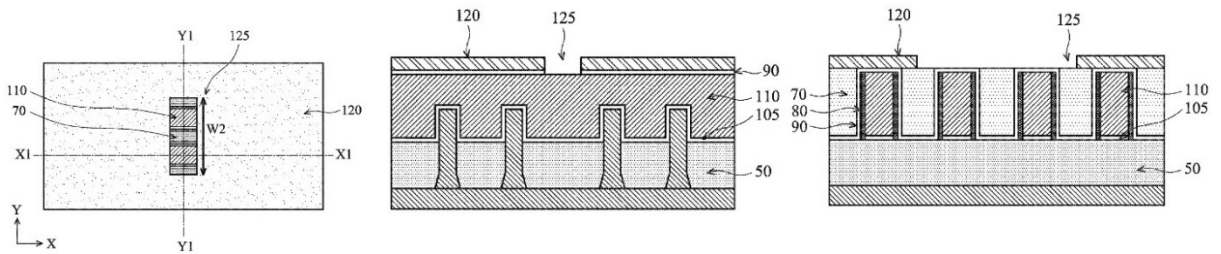
Next, “a gate insulating layer 105 and a poly silicon layer are formed over the isolation insulating layer 50 and the exposed fin structures 20, and then patterning operations are performed so as to obtain a gate layer 110.” (*Id.* ¶[0023].) As shown below, the structure is planarized. (*Id.* ¶[0027].) ILD 70 may be made of “silicon oxide, silicon nitride, silicon oxynitride (SiON), SiOCN,” or another related

material. (*Id.*) “The insulating material for the isolation insulating layer 50 may be the same as or different from that for the ILD 70.” (*Id.* ¶[0026].)



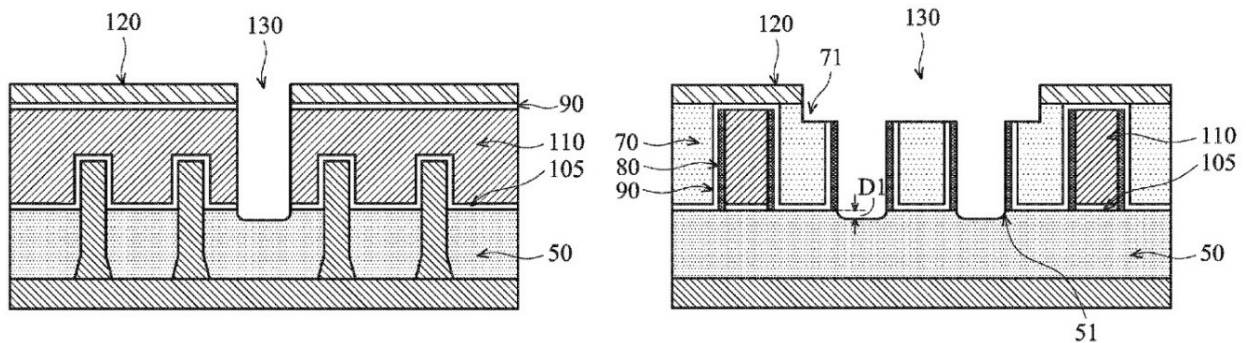
Yu, FIG. 4B Yu, FIG. 4C (X-Z plane) Yu, FIG. 4D (Y-Z plane)

As shown below, a mask pattern 120 with an opening 125 defines regions for a separation plug. (*Id.* ¶[0030].)



Yu, FIG. 5C (X-Y) Yu, FIG. 5A (X-Z) Yu, FIG. 5B (Y-Z)

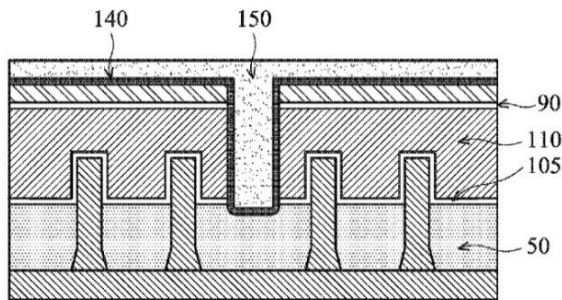
By etching through openings 125, “part of gate layer 110 and the gate insulating layer 105 are removed, so as to obtain a separation opening 130.” (Yu ¶[0031].)



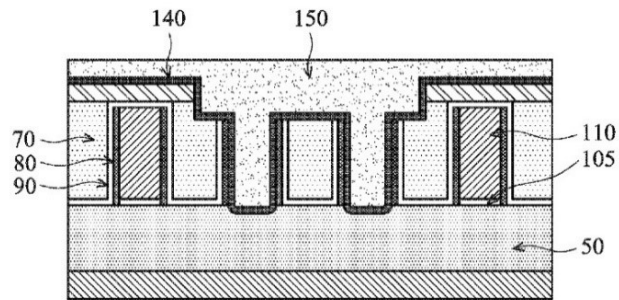
Yu, FIG. 6A (X-Z plane) Yu, FIG. 6B (Y-Z plane)

“[T]he upper portion 71 of the ILD 70 and the surface portion 51 of the isolation insulating layer 50 are also etched, as shown in FIGS. 6A and 6B” above. (*Id.* ¶[0032].) “The depth D1, which is an etched depth of the surface portion 51 of the isolation insulating layer 50 is in a range from about 1 nm to about 10 nm.” (*Id.*)

Openings 130 are filled with an insulator 150 (“silicon oxide or silicon nitride based material[] such as SiN, SiCN, SiON or SiOCN”). (*Id.* ¶¶[0034]-[0037].)

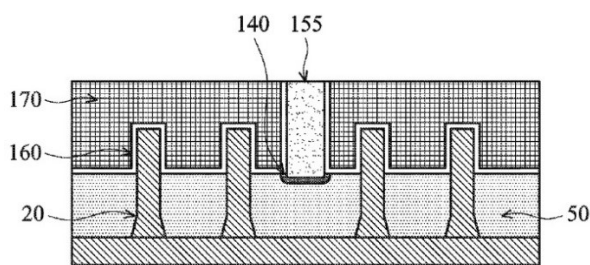


Yu, FIG. 7A (X-Z plane)

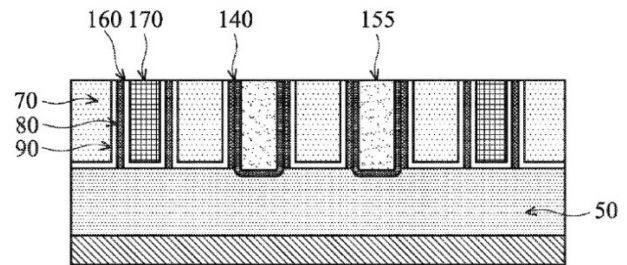


Yu, FIG. 7B (Y-Z plane)

The structure is planarized, and a replacement metal gate process completes the device, as shown below. (*Id.* ¶¶[0037]-[0043], FIGS. 8A-10B.)



Yu, FIG. 10A (X-Z plane)

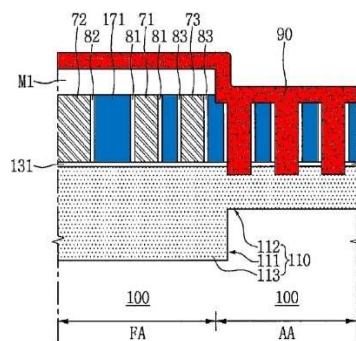


Yu, FIG. 10B (Y-Z plane)

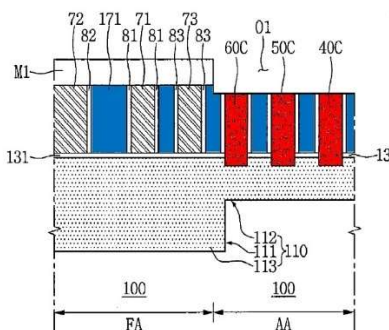
Because Yu is in the same field (FinFETs) and reasonably pertinent to a problem the '880 Patent purports to address (FinFET fabrication), Yu is analogous art. (*See* Ex-1001, 1:9-67; Yu ¶¶[0001]-[0002]; Ex-1003 ¶126.)

1. A POSITA would have found it obvious to make Ha's fin active core using silicon oxide, as Yu discloses

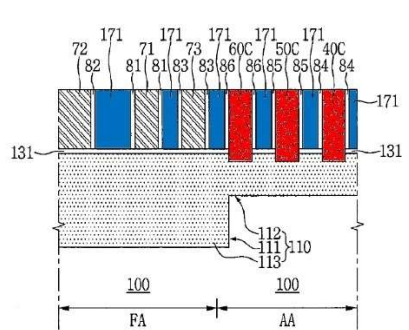
To perform Ha's planarization, illustrated below, a POSITA would have understood core layer 90 (red) and first interlayer insulating layer 171 (blue) are made of different materials, such that core layer 90 may be selectively removed relative to first interlayer insulating layer 171. (Ex-1003 ¶¶326-327.) Ha discloses, for example, "an isotropic etch-back process" that "remov[es] portions of the core layer 90 formed on the first mask pattern M1 or the first interlayer insulating layer 171" and "a planarization process such as a CMP process." (Ha ¶¶[0109]-[0110]; *see id.* ¶¶[0108]-[0111], FIGS. 7A-9C.)



Ha, FIG. 7B



Ha, FIG. 8B

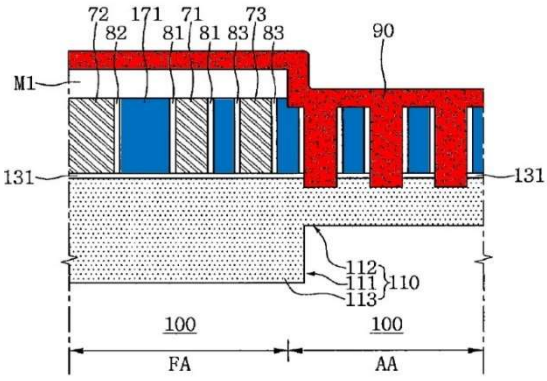
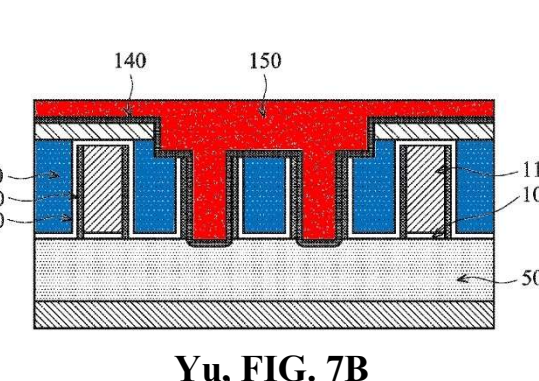
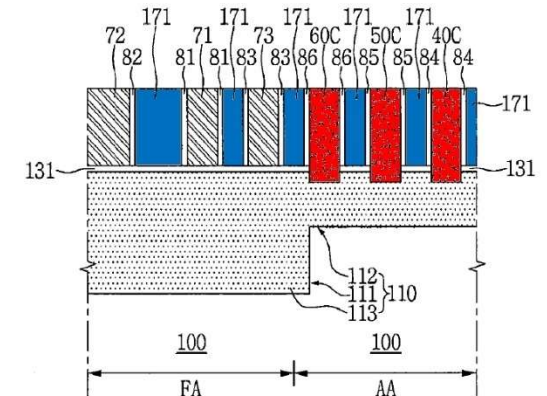
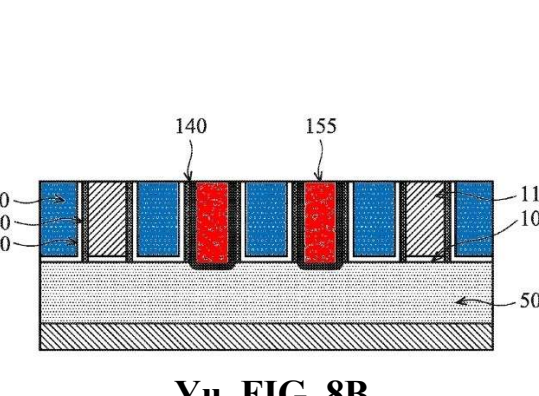


Ha, FIG. 9B

To achieve such selectivity, Ha discloses one embodiment: making core layer 90 using silicon nitride and first interlayer insulating layer 171 using silicon oxide. (Ha ¶[0074], ¶[0107].) Silicon oxide and silicon nitride are textbook examples of insulators that can be removed selectively with respect to one another. (Ex-1003 ¶328; *see* Ex-1011, 38 (Tbl. 10-3).) As Yu demonstrates, a POSITA would have

understood these materials just as easily could be reversed in Ha, i.e., that core layer 90 may comprise silicon oxide, and first interlayer insulating layer 171 may comprise silicon nitride. (Ex-1003 ¶328; *see* Yu ¶[0026], ¶[0036].) This modification would have been obvious. (*Id.*)

As the table below summarizes, Yu and Ha disclose similar structures and process flows. (*Compare* Ha ¶¶[0106]-[0111], FIGS. 7A-9C, *with* Yu ¶¶[0034]-[0038], FIGS. 7A-8B; Ex-1003 ¶329.)

Ha	Yu
 Ha, FIG. 7B	 Yu, FIG. 7B
 Ha, FIG. 9B	 Yu, FIG. 8B

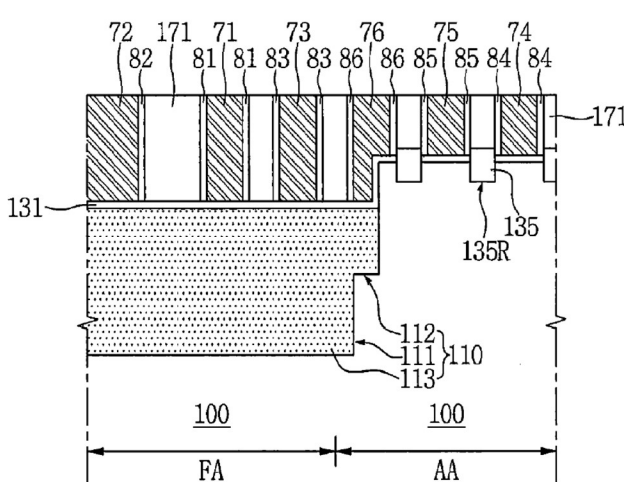
Ha	Yu
“The first interlayer insulating layer 171 may include, for example, silicon oxide.” (Ha ¶[0074].)	“The ILD 70 may include silicon oxide, silicon nitride, silicon oxynitride (SiON), SiOCN, fluorine-doped silicate glass (FSG), or a low-K dielectric material, and may be made of CVD or other suitable process.” (Yu ¶[0026].)
“The core layer 90 may include, for example, silicon nitride.” (Ha ¶[0107].)	“The thick filling insulating layer 150 is made of silicon oxide or silicon nitride based materials such as SiN, SiCN, SiON or SiOCN.” (Yu ¶[0036].)

According to Yu, insulating layer 150 (corresponding to Ha’s core layer 90) and interlayer dielectric layer 70 (corresponding to Ha’s first interlayer insulating layer 171) may comprise either silicon nitride or silicon oxide. (Yu ¶[0026], ¶[0036].) A POSITA thus would have found it obvious that Ha’s core layer 90 may comprise silicon oxide while Ha’s first interlayer insulating layer 171 may comprise silicon nitride. (Ex-1003 ¶330.)

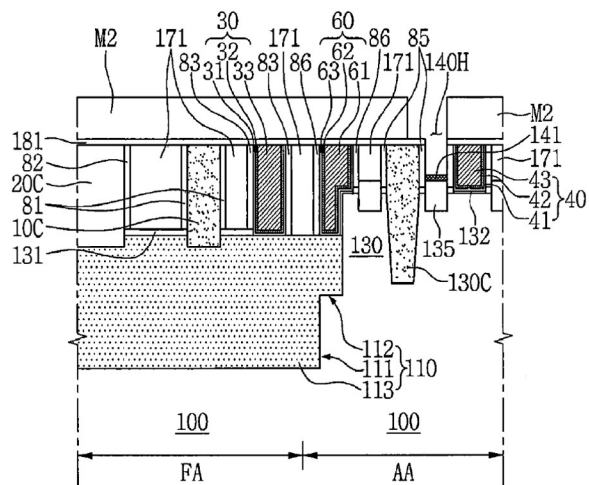
A POSITA would have been motivated to make such a modification since Ha’s process works properly so long as Ha’s core layer 90 is made of an insulating material that can be removed selectively compared to Ha’s insulating first interlayer insulating layer 171. (Ex-1003 ¶331.) Whether core layer 90 is made of silicon nitride and first interlayer insulating layer 171 is made of silicon oxide, or vice versa, is immaterial. Both were known techniques for achieving this same, well-known function. (Ex-1003 ¶¶331-332; *see* Yu ¶[0026], ¶[0036]; Ex-1011, 38 (Tbl. 10-3).)

And “if there’s a known technique to address a known problem using ‘prior art elements according to their established functions,’ then there is a motivation to combine.” (*Intel*, 61 F.4th at 1379-81 (quoting *Intel*, 21 F.4th at 799-800).)

Moreover, success would have been reasonable to expect because such modification would not have been thought to affect any other steps in Ha’s fabrication process or to materially affect the final device. (Ex-1003 ¶333.) For example, a silicon nitride first interlayer insulating layer 171 still would be compatible with source/drain regions 135 (*see* FIG. 4B below). (Ex-1003 ¶333.) And a POSITA would have known how to selectively remove certain portions of a silicon nitride first interlayer insulating layer 171 when contacting source/drain regions 135. (*See* Ha, FIG. 12A; Ex-1011, 38 (Tbl. 10-3); Ex-1003 ¶333.)



Ha, FIG. 4B



Ha, FIG. 12A

Consistent with Yu, a POSITA thus would have found it obvious to reverse the materials for Ha’s core layer 90 and first interlayer insulating layer 171, such

that the former comprises silicon oxide, and the latter comprises silicon nitride. (Ex-1003 ¶334.) Such a modification would have been viewed as an obvious example of (1) substituting one known element for another (silicon oxide for silicon nitride, and vice versa) to obtain predictable results; (2) choosing from among a finite number of identified, predictable solutions (e.g., silicon oxide and nitride, *see* Yu ¶[0026], ¶[0036]), with reasonable expectation of success; and (3) a teaching, suggestion, or motivation in the prior art (*see id.*) that would have led a POSITA to arrive at the claimed invention. (*See KSR*, 550 U.S. at 416-21; Ex-1003 ¶334.)

2. Claim 12

Ha discloses claim 1 under Patent Owner’s apparent view. (*Supra* §VI.C.1.) The combination of Ha and Yu does not materially affect that analysis. (Ex-1003 ¶336.) Additionally, in the combination, Ha’s dielectric layer (core layer 90) comprises silicon oxide. (*Supra* §VI.E.1, Ex-1003 ¶¶335-337.)

VII. TRIAL SHOULD BE INSTITUTED

The Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” sets out a temporary procedure under which Co-Petitioners will have an opportunity to respond to any discretionary denial arguments Patent Owner may raise through a bifurcated briefing process. Co-Petitioners believe discretionary denial is unwarranted and, at the appropriate time, plan to rebut any claims Patent Owner may advance to the contrary.

Meanwhile, Co-Petitioners identify below several non-limiting considerations that weigh against discretionary denial:

- The ITC instituted investigation on March 21, 2025, just 27 days before this Petition was filed. The ITC has not even set a schedule, let alone issued any substantive orders. (*See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 11 (Mar. 20, 2020) (expeditious filing weighs against denial); *SharkNinja v. iRobot Corp.*, IPR2021-00545, Paper 11, at 8 (Sept. 8, 2021) (petitioner's diligence and remaining work at the ITC weighs against denial).)
- No other forum has adjudicated these claims.
- Petitioner TSMC has a 94% institution rate on the merits and a 100% success rate in FWDs. Consistent with that track record, the merits here are strong, presenting one set of grounds that maps onto every claim limitation of the '880 Patent.
- Expert testimony is corroborated by documentary evidence.

- Each of Co-Petitioners (not to mention the other real parties-in-interest) is responsible for substantial and sustained investments and economic activity in the U.S.⁹
- The ITC lacks authority to invalidate the claims, but the companion district court cases, which will be stayed, triggered one-year bar dates for Co-Petitioners and the other real parties-in-interest, thereby limiting their options to invalidate the Challenged Claims. (*See 3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12, at 33-34 (May 26, 2020) (instituting despite parallel ITC case to preserve the “efficiency and integrity of the system”); *Emerson Electric Co., v. Sipco, LLC*, IPR2019-00547, Paper 15, at 9 (Aug. 30, 2019) (IPR proceedings not

⁹ “TSMC Intends to Expand Its Investment in the United States to US **\$165 Billion** to Power the Future of AI,” <https://pr.tsmc.com/english/news/3210> (Mar. 4, 2025); “Apple Will Spend More Than **\$500 billion** in the U.S. Over the Next Four Years,” <https://www.apple.com/newsroom/2025/02/apple-will-spend-more-than-500-billion-usd-in-the-us-over-the-next-four-years/> (Feb. 24, 2025); “Trump and TSMC Announce **\$100 Billion** Plan to Build Five New US Factories,” <https://www.reuters.com/technology/tsmc-ceo-meet-with-trump-tout-investment-plans-2025-03-03/> (Mar. 4, 2025).

duplicative of parallel ITC case).) The ITC may not even reach the issue of invalidity. (*See, e.g., Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).)

VIII. MANDATORY NOTICES

A. Real Parties-in-Interest

Co-Petitioners Taiwan Semiconductor Manufacturing Company Limited and Apple Inc., as well as Broadcom Inc. and Qualcomm Inc., are the real parties-in-interest.

B. Related Matters

First, the '880 Patent has been asserted in *Longitude Licensing Ltd. v. Lenovo Grp. Ltd. et al.*, Case No. 2:25-cv-00171-JRG (E.D. Tex.). In that proceeding, Patent Owner has alleged infringement by the following entities:

- Taiwan Semiconductor Manufacturing Company Ltd.
- Lenovo Group Ltd.
- Motorola Mobile Communication Technology Ltd.
- Motorola (Wuhan) Mobility Technologies Communication Co. Ltd.
- OnePlus Technology (Shenzhen) Co. Ltd.

Second, the '880 Patent has been asserted in *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 1:25-cv-00215-ADA (W.D. Tex.). In that proceeding, Patent Owner has alleged infringement by the following entities:

- Apple Inc.
- Broadcom Inc.
- Qualcomm Inc.

Third, the '880 Patent has been asserted in *Certain Foreign-Fabricated Semiconductor Devices, Products Containing the Same, and Components Thereof*, Inv. No. 337-TA-1443 (U.S.I.T.C.). In that proceeding, Patent Owner has alleged infringement by the following entities:

- Taiwan Semiconductor Manufacturing Company Ltd.
- Apple Inc.
- Broadcom Inc.
- Qualcomm Inc.
- Lenovo Group Ltd.
- Motorola Mobile Communication Technology Ltd.
- Motorola (Wuhan) Mobility Technologies Communication Co. Ltd.
- OnePlus Technology (Shenzhen) Co. Ltd.

Co-Petitioners are not aware of any other proceedings involving the '880 Patent.

C. Lead and Back-Up Counsel

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D. Service Information

Co-Petitioner TSMC consents to service by e-mail at the following addresses:

- jp.long@finnegan.com;
- christian.sanders@finnegan.com;
- TSMC-MSL-IPR@finnegan.com.

Co-Petitioner Apple consents to electronic service by email at IPR50095-0271IP1@fr.com (referencing No. 50095-0271IP1 and cc'ing PTABInbound@fr.com, axf-ptab@fr.com, tar@fr.com, and khan@fr.com).

IX. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 06-0916.

X. GROUNDS FOR STANDING

Co-Petitioners certify the '880 Patent is available for *inter partes* review, and Co-Petitioners are not barred or estopped from requesting review on the grounds presented.

XI. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft 365, this Petition contains 13,644 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, List of Challenged Claims, Mandatory Notices, and Certificate of Service.

XII. CONCLUSION

Trial should be instituted and the challenged claims cancelled.

Dated: April 17, 2025

Respectfully submitted,

/ J. Preston Long /

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Lead Counsel for Co-Petitioners

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Co-Petitioners' Powers of Attorney, and the associated Exhibits 1001-1035** were served via FedEx International delivery on April 17, 2025, on the correspondence address of record below indicated in the U.S. Patent Office's Patent Center for U.S. Patent No. 9,953,880.

Winston Hsu
North America Intellectual Property Corporation
5F., No. 389, Fuhe Rd., Yonghe Dist.
New Taipei City, - 234645
Taiwan

Courtesy copies have been concurrently served by FedEx Priority Overnight delivery on Patent Owner's litigation counsel at:

Michael T. Renaud
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One Financial Center
Boston, MA 02111

Dated: April 17, 2025

By: / William Esper /
William Esper
Legal Assistant and PTAB Coordinator
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