

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
and APPLE INC.
Petitioners,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-00848
U.S. Patent No. 9,953,880 B2

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

TABLE OF CONTENTS

	<u>Page</u>
I. Introduction.....	1
II. Semiconductor Transistor Technology Primer.....	2
A. Basic Transistor Components.....	2
B. Planar vs. Three-Dimensional Transistors	5
C. Processes For Manufacturing Integrated Circuits And Transistors	8
1. The Four Stages Of Fabricating Integrated Circuits.....	8
2. The Wafer Fabrication Stage	9
III. The Challenged '880 Patent	11
A. An Exemplary '880 Patent Method Includes Forming An SDB Trench By Removing Part Of An STI.....	12
B. The Challenged Claims	18
1. A method for fabricating semiconductor device, comprising:.....	18
IV. PTAB Should Deny The Petition Because It Fails To Establish The Required Likelihood Of Success	19
A. The Relevant <i>Ha</i> Disclosures.....	21
B. <i>Ha</i> Does Not Disclose Making An SDB Made In A Trench Made By Removing Part Of An STI.....	25
V. Conclusion	29

TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph McAlexander
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4th ed.)

I. Introduction

Every challenged claim requires a “trench” having at least two characteristics: (1) the trench must be formed by, *inter alia*, removing part of a shallow trench isolation (STI); and (2) a single diffusion break (SDB) structure is formed in that same trench.

But although each ground relies solely on the *Ha* reference as teaching this claimed “trench,” *Ha* does not teach or suggest forming a trench by removing, *inter alia*, part of an STI and then forming an SDB in that resulting trench.

And the Petition does not assert otherwise. Rather, the Petition identifies only one location where part of alleged STI (*Ha*’s isolation region 110) is supposedly removed: “fin gate cut space S3.” (EX1006 at ¶0195; Petition at 62).

But the Petition does not allege that *Ha* teaches or discloses forming an SDB in this “fin gate cut space S3.” Rather, the Petition alleges that *Ha* teaches forming an SDB in a **different** location, in “fin active cut space S4.” And the Petition does not allege that “fin active cut space S4” is made by, *inter alia*, removing a part of the alleged STI. It cannot because *Ha* makes explicit that “fin active cut space S4” is **not** over the alleged STI and is **not** made by removing any part of that alleged STI.

Thus, no grounds identify the claimed trench, which must be both (1) made by removing part of an STI **and** (2) used to form an SDB. Instead, even accepting

the Petition's assertions as true, the Petition identifies one trench that is supposedly made by removing part of an STI and a **different** trench that is allegedly used to form an SDB.

Accordingly, the Petition fails to establish the required reasonable likelihood of success and should be denied.¹

II. Semiconductor Transistor Technology Primer

The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (e.g., fin) transistors; and (3) common process steps for creating transistors. (EX2001, ¶15).

A. Basic Transistor Components

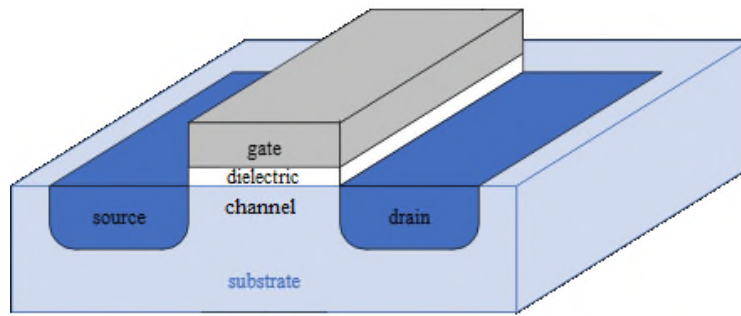
Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (i.e., turning electrical current on and off) and amplification

¹ Because the Petition wholly fails to establish this limitation required in every challenged claim, this Response need not and does not address other failures of the Petition.

(i.e., increasing the amplitude of a signal while retaining its electrical characteristics). (EX2002 at 1-2). Where earlier tube devices used a vacuum to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. (EX2002 at 3; EX2001, ¶6).

One type of transistor typically used in an integrated circuit (or “chip”) is a “field effect transistor,” or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. (EX2002 at 29-34). In a conductor (e.g., a metal), electric current can flow freely. (EX2002 at 29). A dielectric (e.g., silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. (EX2002 at 30). Semiconductors (e.g., silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. (EX2002 at 31-34; EX2001, ¶7).

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. (See, e.g., EX2002 at 510-511). The source, drain, and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.

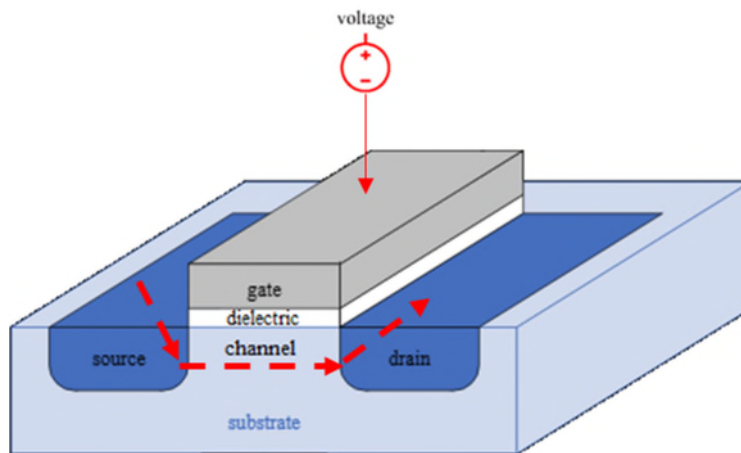


(See, e.g., EX2002 at 510-511; EX2001, ¶8).

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). (EX2002 at 26-28, 427-28). The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). (EX2002 at 510-511; EX2001, ¶9).

The gate is a conductor located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. (EX2002 at 510-511). When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation of a “field effect” in the channel. (EX2002 at 510-511). This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). (EX2002 at 510-511; EX2001, ¶10).

As illustrated below, this field effect allows electrical current to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping the flow of electrical current. (EX2001, ¶11).

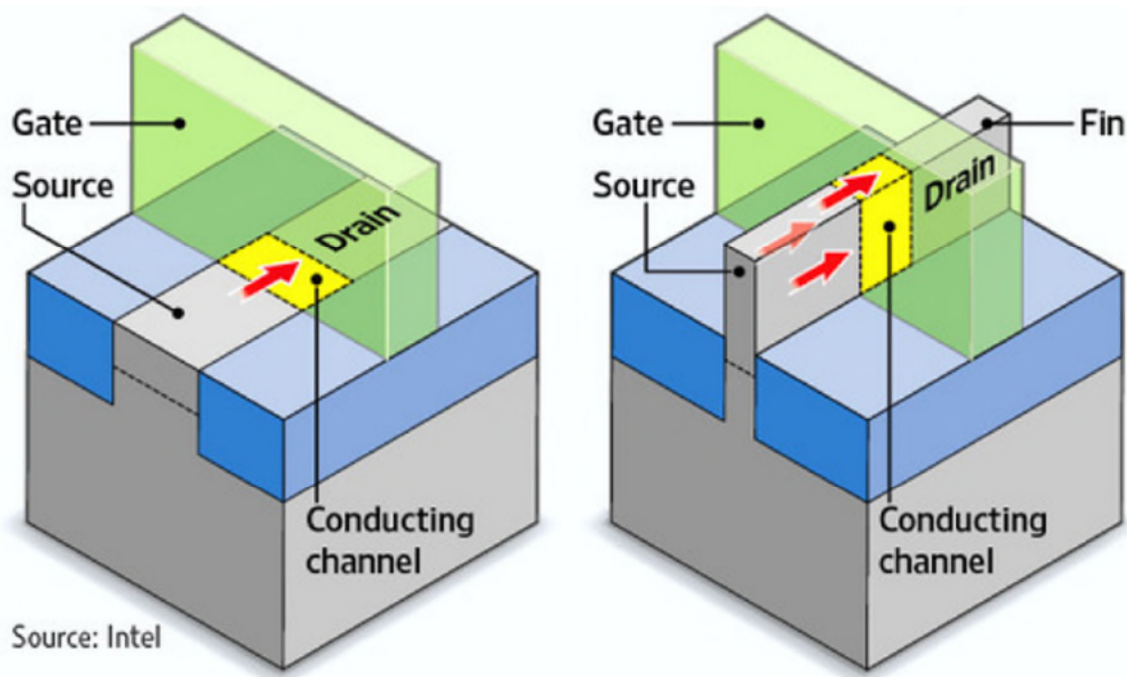


B. Planar vs. Three-Dimensional Transistors

Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more on a chip has been constant and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.” (EX2001, ¶12).

The simplified illustrative FET transistors illustrated in the previous section all feature a gate built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors. (EX2001, ¶13).

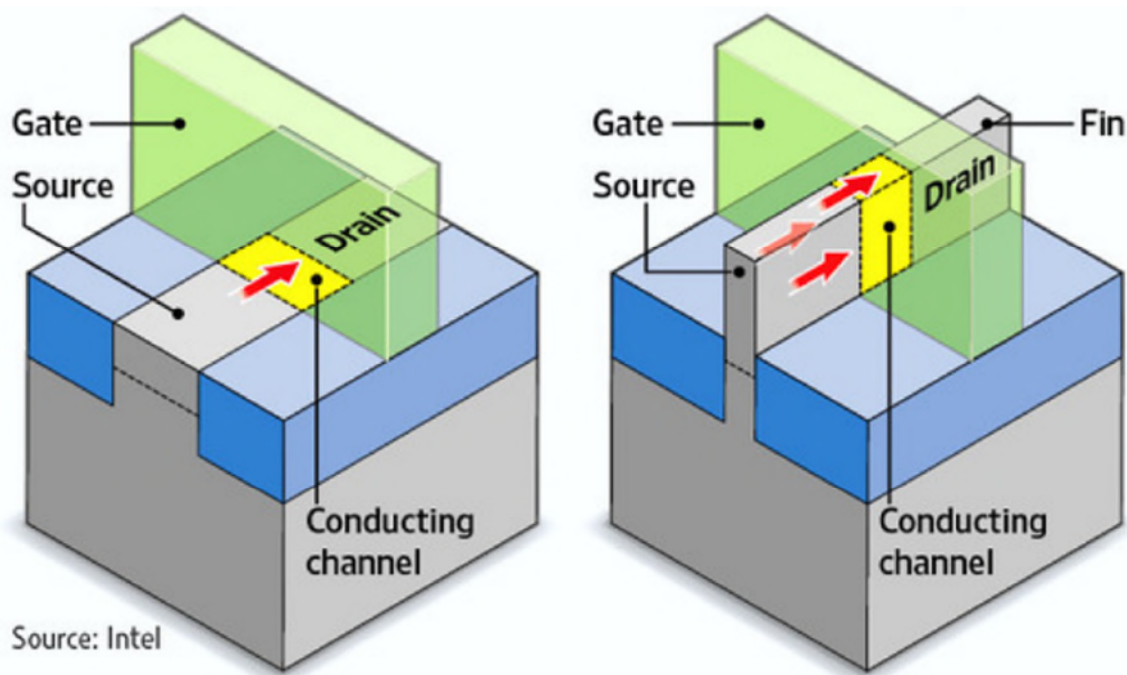
In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



(EX2001, ¶14).

In contrast, as illustrated below in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate

that acts as a channel between the source and drain regions. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.



(EX2001, ¶15).

Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be

more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip. (EX2001, ¶16).

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. (EX2001, ¶17).

In the first stage, the semiconductor material itself is created. (EX2002 at 13). For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. (EX2002 at 13; EX2001, ¶18).

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” (EX2002 at 13-14). A wafer acts as a semiconductor substrate on and in which transistors may be formed. (EX2001, ¶19).

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. (EX2002 at 14). Thousands of integrated circuits can be formed on the substrate of a single wafer. (EX2002 at 14; EX2001, ¶20).

In the packaging stage, the wafer is separated into individual chips. (EX2002 at 14-15; EX2001, ¶21).

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in the wafer's substrate. (EX2002 at 14). These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). (See EX2002 at 29-31, 71). For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. (EX2001, ¶22).

Layering is the operation used to add thin layers to the semiconductor substrate. (EX2002 at 72). The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. (EX2002 at 72; EX2001, ¶23).

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure

shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. (EX2002 at 72; EX2001, ¶24).

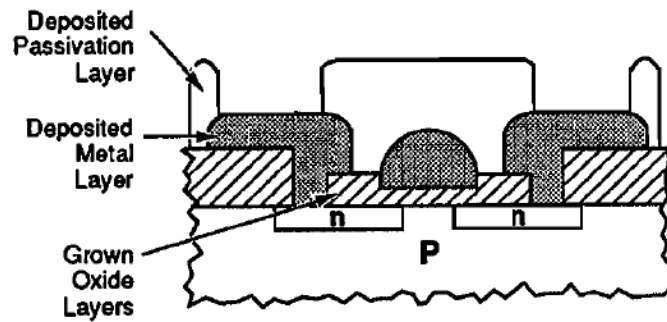


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. (EX2002 at 72-73). This creates a pattern on the wafer surface. (EX2002 at 72-73; EX2001, ¶25).

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. (EX2002 at 72-73; EX2001, ¶26). For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

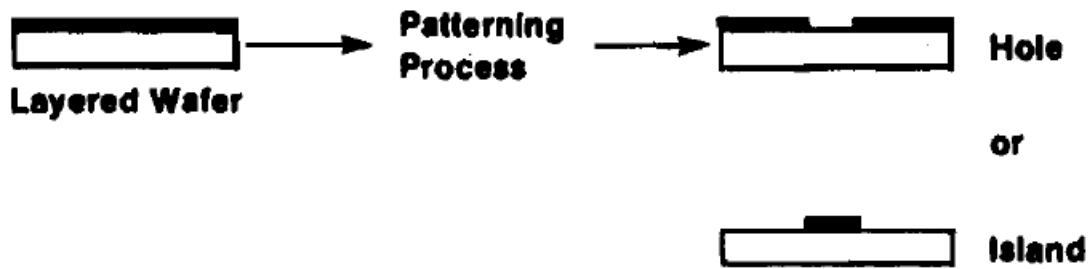


Figure 4.7 Patterning.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

(EX2002 at 73; EX2001, ¶27).

III. The Challenged '880 Patent

The '880 Patent generally discloses improved semiconductor devices and methods, including improved devices and methods for incorporating shallow trench isolation ("STI"), a single diffusion break ("SDB") isolation structure, and an interlayer dielectric ("ILD") for transistors, including FinFET transistors. (*E.g.*,

EX1001 at 1:46-54, 4:59-67, 6:44-56). One improved method includes removing (e.g., “patterning”) parts of a gate layer, a fin-shaped structure, and an STI to form a trench, in which an SDB is then formed. Critically, none of the asserted references or combinations discloses or otherwise includes removing part of an STI to make a trench and then forming an SDB in that same trench. (EX2001, ¶37).

A. An Exemplary '880 Patent Method Includes Forming An SDB Trench By Removing Part Of An STI

The '880 Patent describes an exemplary inventive fabrication method, starting by forming a number of fin-shaped structures on a substrate. Figure 1 illustrates a top view of such fin-shaped structures 14 on a substrate:

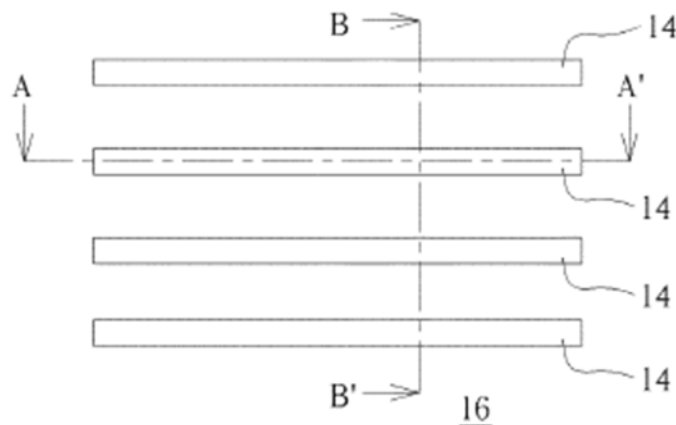
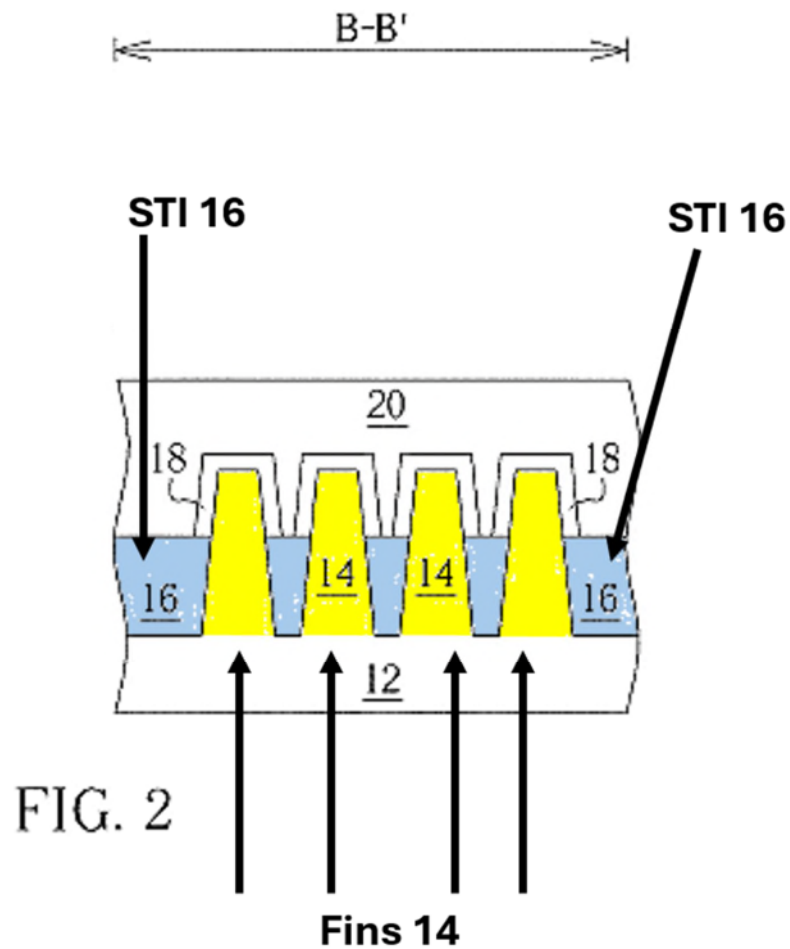


FIG. 1

(EX1001 at Fig. 1, 2:10-21; EX2001, ¶38).

Figure 2 includes two cross-sectional views of Figure 1, with the right view taken along Figure 1's sectional line BB' so that the fins 14 run in and out of the page. (EX1001 at 2:9-17). The right view of Figure 2 (shown and annotated below) illustrates, among other things, a shallow trench isolation (STI) 16 (annotated in blue) formed around the fin-shaped structures 14 (annotated in yellow). (EX1001 at Fig. 2, 2:59-60). An STI is an insulation feature sometimes used in transistor fabrication to prevent electrical current leakage between circuit components. (EX2002 at 440). As the '880 Patent describes, STI 16 is formed by first depositing a layer of dielectric (e.g., silicon oxide) on substrate 12 so that it completely covers fin-shaped structures 14, and then etching away select parts of the dielectric layer (e.g., patterning the layer) so that the remaining parts form STI 16 between fin-shaped structures 14:



(EX1001 at Fig. 2 (partial), 2:60-3:2'²; EX2001, ¶39).

Next, using a series of layering and patterning steps, gate dielectric layer 18 and gate layer 20 are formed over the fin-shaped structures and STI 16. In the

² Unless otherwise indicated, all colors and annotations to the challenged patent's figures are added.

below annotated Figure 2, gate dielectric layer 18 is shown in orange and the gate layer 20 is shown in green:

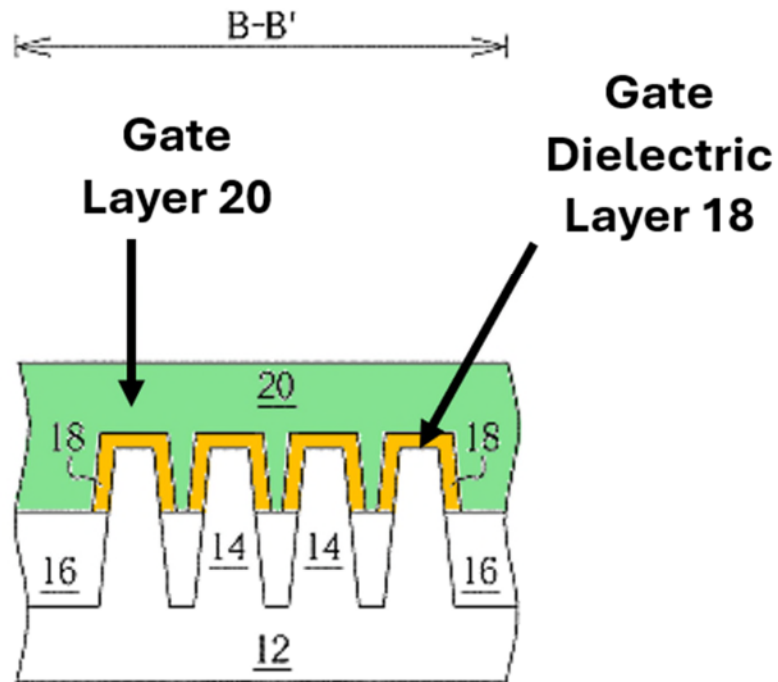
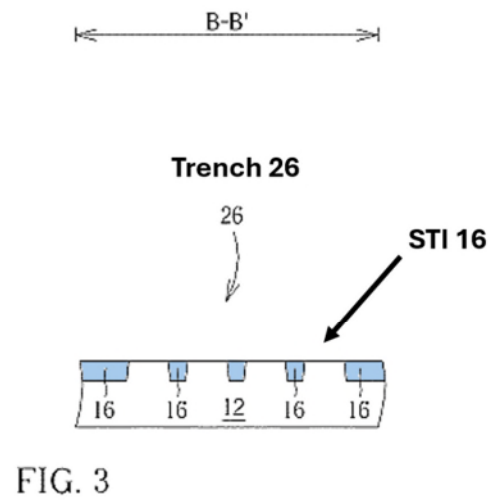
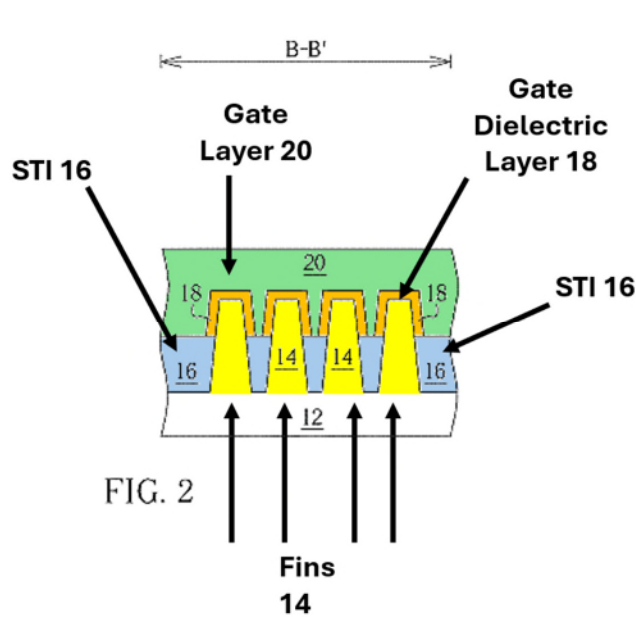


FIG. 2

(EX1001 at Fig. 2 (partial), 2:60-3:2; EX2001, ¶40).

The '880 Patent next describes that patterning is used to form a trench 26. (*E.g.*, EX1001 at Fig 3, 3:17-24). As described and illustrated in Figures 2 and 3 (annotated below), the patterning used to form trench 26 includes removing part of the gate layer 20, part of the fin-shaped structure 14, and part of the STI 16, transforming the structure shown below on the left to the one shown on the right:



(*E.g.*, EX1001 at Figs. 2-3 (partial), 3:17-24; EX2001, ¶41).

A single diffusion break (SDB) structure is then formed in trench 26. (*E.g.*, EX1001 at 3:25-59, Figs. 4-6). An SDB is another type of insulation structure sometimes used in integrated circuits and, as illustrated below in annotated Figure 5, it runs approximately perpendicular to a fin-shaped structure, so that it separates that structure into two sections:

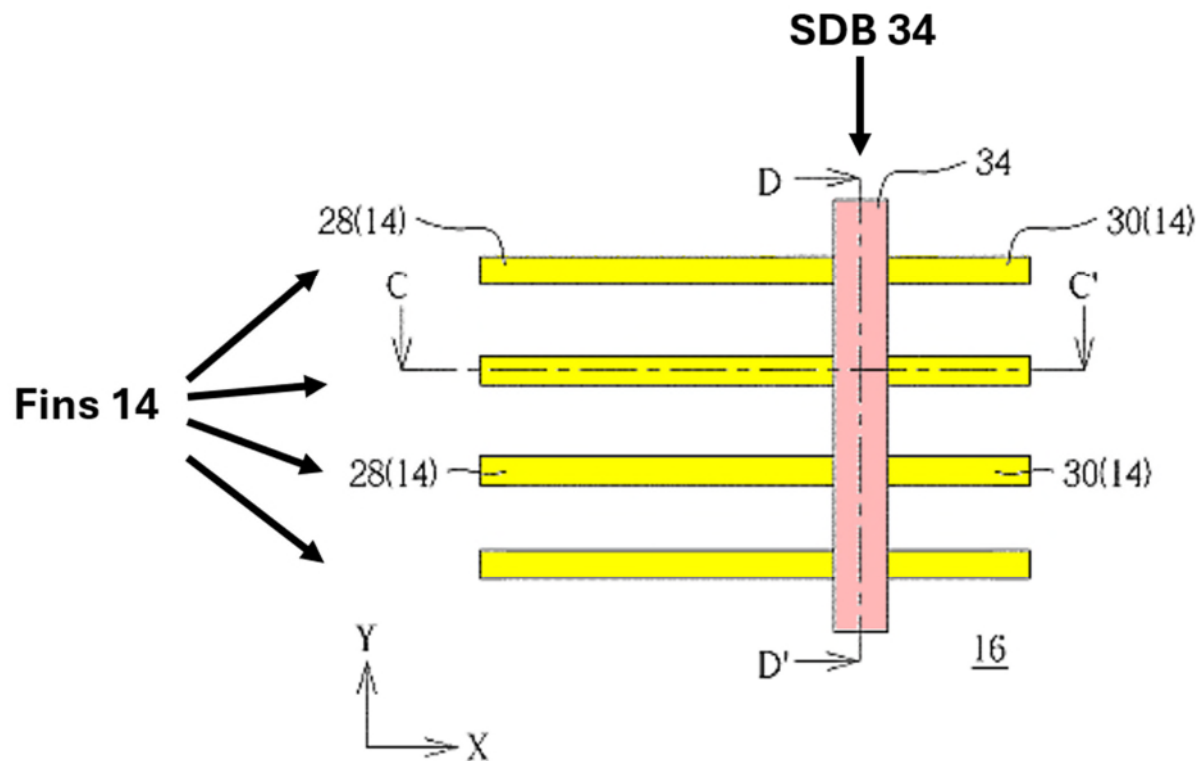


FIG. 5

(EX1001 at Fig. 5, 3:48-59; EX2001, ¶42).

The '880 Patent describes that this SDB 34 is made by forming a dielectric layer 32 in the trench (which, as discussed above, is itself etched into the gate layer 20, part of the fin-shaped structure 14, and part of the STI 16):

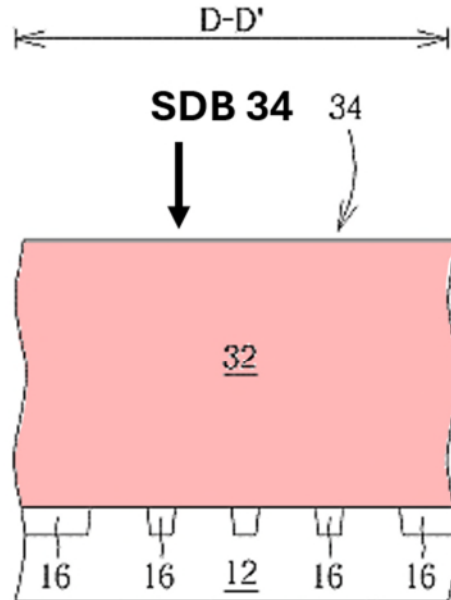


FIG. 6

(EX1001 at Fig. 6 (partial), 3:25-59; EX2001, ¶43).

B. The Challenged Claims

The Petition challenges all of the '880 Patent claims, namely independent claim 1 and its dependent claims 2-12. Consistent with the foregoing illustrative embodiment, each of these challenged claims is directed to a method for fabricating a semiconductor device, including the steps of (1) forming a trench by removing parts of a gate layer, fin-shaped structure, and STI; and (2) forming an SDB in that trench. (EX2001, ¶44).

For example, exemplary independent claim 1 recites:

- 1. A method for fabricating semiconductor device, comprising:**
forming a fin-shaped structure on the substrate;

forming a shallow trench isolation (STI) around the fin-shaped structure;
forming a gate layer on the fin-shaped structure and the STI;
removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench;
forming a dielectric layer into the trench to form a single diffusion break (SDB) structure; and
after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure.

(EX1001 at claim 1³; EX2001, ¶45).

IV. PTAB Should Deny The Petition Because It Fails To Establish The Required Likelihood Of Success

The Petition asserts six different grounds against various selections of claims:

Ground	References	Basis	Challenged Claims
1A	<i>Doris, Ha</i>	§ 103	1-12
1B	<i>Doris, Ha, Colinge</i>	§ 103	1-12
2A/2B	<i>Ha</i>	§ 102 / § 103	1-5, 7-8, 10-11
2C	<i>Ha, Zhao</i>	§ 103	9
2D	<i>Ha, Yu</i>	§ 103	12

(EX2001, ¶46).

The Petition should be denied because, among other reasons, none of these grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teach or make obvious each limitation in any challenged claim. (EX2001, ¶47).

³ Unless otherwise indicated, all emphasis in quotations is added.

For example, each ground fails to identify a reference that teaches the claimed SDB trench made by, among other things, removing part of an STI. Each ground relies solely on the *Ha* reference as teaching this limitation, but *Ha* does not teach or suggest forming a trench by removing, *inter alia*, part of an STI and then forming an SDB in that resulting trench. (EX2001, ¶48).

And the Petition does not assert otherwise. Rather, the Petition identifies only one location where part of the alleged STI (*Ha*'s isolation region 110) is supposedly removed: “fin gate cut space S3.” (EX1006 at ¶0195; Petition at 62; EX2001, ¶49).

But the Petition does not allege that *Ha* teaches or discloses forming an SDB in this “fin gate cut space S3.” Rather, the Petition alleges that *Ha* teaches forming an SDB in a **different** location, in “fin active cut space S4.” And the Petition does not allege that “fin active cut space S4” is made by, *inter alia*, removing a part of the alleged STI. It cannot because *Ha* makes explicit that “fin active cut space S4” is **not** over the alleged STI and is **not** made by removing any part of that alleged STI. (EX2001, ¶50).

Thus, the Petition fails to establish a reasonable likelihood of success because no grounds identify the claimed trench that is both made by removing part of and STI **and** used to form an SDB. Instead, at best, the Petition identifies one

trench that is supposedly made by removing part of an STI and a **different** trench that allegedly used to form an SDB. (EX2001, ¶51).

A. The Relevant *Ha* Disclosures

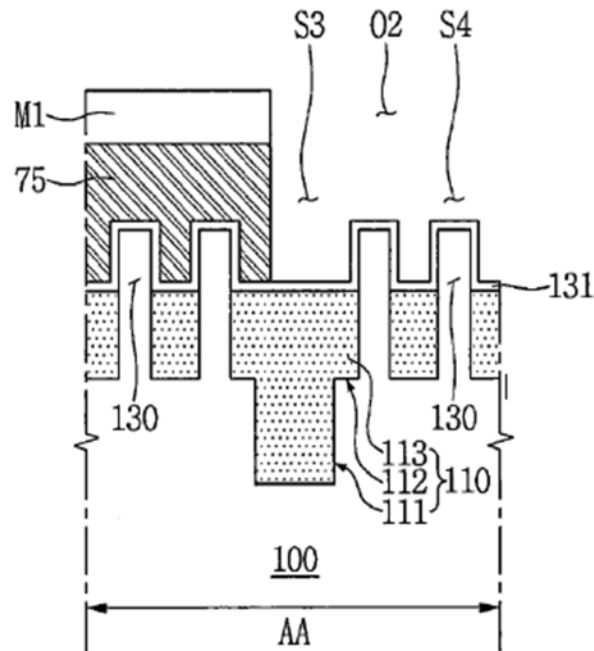
The Petition plays a shell game when trying to address the missing limitations, ambiguously and misleadingly relying on different and distinct aspects of *Ha* in an effort to hide the fact that *Ha* does not teach or suggest forming a trench by removing, *inter alia*, part of a shallow trench isolation (STI) and then forming an SDB in that resulting trench. (*E.g.*, Petition at 62-65). Specifically, the Petition attempts to hide that the alleged *Ha* trench made by removing part of an STI is “fin gate cut space S3,” but the alleged *Ha* trench in which an SDB is supposedly made is the completely different and distinct “fin active cut space S4.” The following demonstrates the attempted sleight of hand. (EX2001, ¶52).

To start, *Ha* identifies creating four different “spaces”:

- Two spaces formed by removing (cutting) parts of a field gate pattern: “field gate cut space S1” and “field gate space 2”;
- One space formed by removing parts of a fin gate pattern: “fin gate cut space S3”; and
- One space formed by removing parts of a fin active region: “fin active cut space S4.”

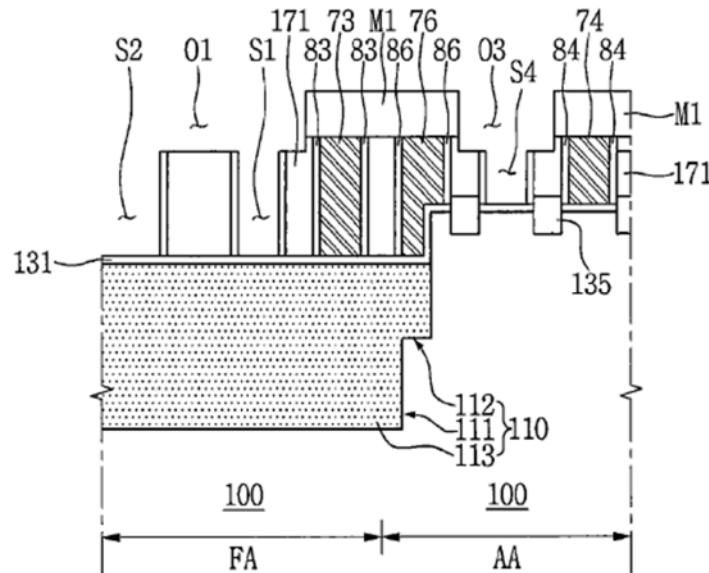
(*E.g.*, EX1006 at ¶099; *see also* ¶¶0091, 0101, 0104, 0105; EX2001, ¶53).

“Fin gate cut space S3” and “fin active cut space S4” are each illustrated in *Ha* Figure 5C. As shown (and as described throughout *Ha*), “fin gate cut space S3” is over the alleged claimed STI (*Ha* isolation region 110), but “fin active cut space S4” is not; instead, it is over (as the name suggests) the fin active region 130:



(EX1006 at Figs. 5A-5C; EX2001, ¶54).

Similarly, *Ha* Figure 5A illustrates “field gate cut space S1,” “field gate space S2,” and “fin active cut space S4.” Once again, as shown (and as described throughout *Ha*), “field gate cut space S1” and “field gate space S2” are over the alleged claimed STI (*Ha* isolation region 110), but “fin active cut space S4” is not:



(EX1006 at Figs. 5A-5C; EX2001, ¶55).

These differences are not disclosed in the Petition but are critical to understanding *Ha* and the Petition's defects. For example, the Petition relies on the following *Ha* passage concerning recessing the isolation region 110 (the alleged STI) as the basis for its assertion that *Ha* discloses removing part of the STI in these spaces. (Petition at 62). But this passage is necessarily limited to the three *Ha* spaces that are over the isolation region 110, and *Ha* pointedly does **not** **identify "fin active cut space S4"** as a space where isolation region 110 may be recessed:

[0105] The isolation region 110 exposed in the first field gate cut space S1, the second field gate cut space S2, and the fin gate cut space S3 may be recessed.

(EX1006 at ¶0105; Petition at 62; EX2001, ¶56).

Instead, *Ha* describes a different method for the “fin active cut space S4.” Namely, because “fin active cut space S4” is over the fin active region 130 instead of the isolation region 110, *Ha* describes a “fin active cutting method” in which fin active region 130—not isolation region 110—may be recessed:

[0104] Referring to FIGS. 6A to 6C, the method may include forming a fin active recess 130R by removing the base insulating layer 131 exposed in the fin active cut space S4 and **recessing the fin active region 130.**

(EX1006 at ¶0104; EX2001, ¶57).

And this is the only method—one that does not include removing any part of the isolation region 110 (the alleged STI)—that *Ha* even arguably discloses for forming an SDB. The sole *Ha* sentence that even mentions an SDB discloses using the **fin active** cutting method that involves an underlying fin active region, not a field gate or fin gate cutting method that involves an underlying isolation region:

[0129] Semiconductor devices and methods of fabricating the same in accordance with some embodiments of the inventive concept, a single diffusion break (SDB) structure can be **implemented using a fin active cutting method.**

(EX1006 at ¶0129; EX2001, ¶58).

B. *Ha* Does Not Disclose Making An SDB Made In A Trench Made By Removing Part Of An STI

Every challenged claim requires that an SDB be formed in a trench that was made, *inter alia*, by removing part of a shallow trench isolation (STI):

removing part of the gate layer, part of the fin-shaped structure, and
part of the STI to form a trench; [and]
forming a dielectric layer into the trench to form a single diffusion
break (SDB) structure.

(EX1001 at claim 1).

The Petition identifies and relies on only a single mention of an SDB in *Ha*:

[0129] Semiconductor devices and methods of fabricating the same in accordance with some embodiments of the inventive concept, **a single diffusion break (SDB) structure can be implemented using a fin active cutting method.**

(Petition at EX1006 at ¶0129). The Petition could identify no other mention of an SDB because there is none. (EX2001, ¶59).

And, tellingly, the Petition does not assert that *Ha* discloses or suggests that the foregoing SDB is formed in a trench made by removing part of an STI, as required by every challenged claim. (Petition at 64-65). Instead, the Petition attempts to skirt the issue by repeatedly asserting that the SDB is formed in the

“fin active cut space S4” (emphasis in Petition) using *Ha*’s **“fin active cutting method”** (emphasis in Petition). (Petition at 64-65; EX2001, ¶60).⁴

But as established, *Ha*’s fin active cut space S4 and fin active cutting method do not involve **any** removal of the alleged STI, *Ha*’s isolation region 110. (Petition at 59-60). They could not because the fin active cut area S4 is explicitly not over isolation region 110; it is over the fin active region 130. Therefore, at most, *Ha*’s fin active cut space S4 and fin active cutting method involve the removal of fin active region, not the alleged STI (isolation region 110) as required:

[0104] Referring to FIGS. 6A to 6C, the method may include forming a fin active recess 130R by removing the base insulating layer 131

⁴ The Petition states or implies that “insulating core layer 90” or “fin active core 130C” as formed in fin active cut space S4 are somehow the SDB mentioned in *Ha*, but *Ha* does not identify either of those structures as an SDB and the Petition provides no analysis or reasoning supporting their assumption that either of these structures is an SDB. (Petition at 64-65). But this additional failure does not matter here, because regardless of whether these structures are SDBs, Petitioners allege that they formed in fin active cut space S4, which is indisputably **not** a trench made by removing part of the alleged STI.

(EX1006 at ¶0104; EX2001, ¶61).

[illegible]

Ha, FIG. 6B
(annotated)

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The closest that the Petition comes to at least (baselessly) implying that the fin active cut space S4 and its fin active cutting method involve the removal the alleged STI (isolation region 110) is the Petition's following ambiguous and incomplete assertion:

Ha further discloses “forming a fin **active** recess 130R ... by recessing the fin **active** region 130” and that, additionally, **“isolation region 110 ... may be recessed.”**

(Petition at 62). But the Petition is conflating two different *Ha* methods and spaces and misleadingly presenting them as one. As established above, the Petition's foregoing quotes concerning the fin **active** region and recess concern a method involving fin active cut space S4 and do not involve recessing isolation region 10:

[0104] Referring to FIGS. 6A to 6C, the method may include forming a fin active recess 130R by removing the base insulating layer 131 exposed in the fin active cut space S4 and **recessing the fin active region 130.**

(EX1006 at ¶0104; EX2001, ¶63).

The remainder of the Petition's quote regarding recessing isolation region 10 does not concern fin active cut space S4; it instead concerns “first field gate cut space S1, the second field gate cut space S2, and the fin gate cut space S3.” This critical distinction is readily apparent from the following bolded language, which Petitioners omitted from their quote:

[0105] The isolation region 110 **exposed in the first field gate cut space S1, the second field gate cut space S2, and the fin gate cut space S3** may be recessed.

(EX1006 at ¶0105; Petition at 62; EX2001, ¶64).

For any and all of the foregoing reasons, the Petition fails to establish a reasonable likelihood of success because no grounds identify the claimed trench that is both made by removing part of an STI **and** used to form an SDB. Instead, the Petition identifies one alleged trench that is supposedly made by removing part of an STI and a **different** alleged trench that is supposedly used to form an SDB. (EX2001, ¶65).

V. Conclusion

For the foregoing reasons, the Board should deny institution of the Petition.

Dated: August 15, 2025

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 4,567. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

Dated: August 15, 2025

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CERTIFICATE OF SERVICE

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