



The conversion of solar energy into electrical power is becoming increasingly important throughout the world as the slow shift away from oil gathers pace. Solar cells are at the heart of this conversion and this book provides a comprehensive source of information on their design, materials, manufacture and performance. Invited contributors of international repute write on specific topics, and the whole book has been carefully edited by two leading researchers in the field.

'Solar Cells' has been abstracted from a larger and more comprehensive volume on photovoltaics: **The Practical Handbook of Photovoltaics**, published in 2003 and edited by Tom Markvart and Luis Castañer.
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Edited by
Markvart
& Castañer

Solar Cells

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and Operation

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Materials, Manufacture
and Operation

Edited by
Tom Markvart and Luis Castañer



Solar Cells: Materials, Manufacture and Operation

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Publisher's Note

In response to a perceived demand for a concise account of solar cell technology, this volume 'Solar Cells: Materials, Manufacture and Operation' has been abstracted virtually without change from the 'Practical Handbook of Photovoltaics: Fundamentals and Applications', also edited by Dr Markvart and Professor Castañer and published in 2003. (ISBN 185617 3909)

A new chapter on 'Low Cost Industrial Manufacture of Crystalline Silicon Solar Cells' by Szułcick et al has been provided as the original chapter was taken from a proceedings volume and was in need of updating.

To save time and costs, the original Section and Chapter numbering has been retained, although a new index has been provided.

1 Introduction

The majority of silicon wafers used for solar cells are Czochralski (CZ) single crystalline and directional solidification, or cast, multicrystalline (mc) material. The split between the two types of wafer is presently about 55% mc-Si and 45% CZ-Si. Until 1995 CZ wafers represented 60% of the substrates used by industry and mc-Si wafers around 25%. The fast scale up of commercially available multicrystalline wafers changed the picture rapidly. The remainder of the silicon substrates used by the industry are non-wafered sheets or ribbons that are of different types and have recently gained significant production figures, following long development phases. Non-wafer silicon accounted for about 4% of the market in 2001, up from 1–2% in the mid-1990s [1, 2].

2 Characteristics of Silicon Wafers for Use in PV Manufacturing

2.1 Geometrical Specifications

Most of the wafer substrates used in production facilities have dimensions relating to the diameters of monocrystalline silicon cylinders for the semiconductor industry (essentially 5 and 6 inch) that, in turn, have influenced standards for wafer carriers, automation, packaging etc. However, in order to maximise the power density of the modules, wafers are square, or pseudo-square in the case of monocrystalline silicon, that is cylinders are shaped as squares with rounded off corners. This reduces the surface area of the wafers by between 2% and 5% compared with a full square of same dimensions.

In the case of mc-Si, ingot sizes are designed to be compatible with multiple numbers of each of the standard wafer dimensions, in order to maximise geometrical yield. Yield considerations limit the possible wafer sizes achievable for any given ingot dimension, as much as expensive wafer cassettes, automation and packaging do later in the process. Table 1 reports the different sizes for commercially available wafers, including typical tolerances.

A SEMI® (Semiconductor Equipment and Materials International) standard, M61000, was developed with the purpose of covering the requirements for silicon wafers for use in solar cell manufacturing [3], including dimensional specifications, defects and electronic properties. Most commercial suppliers sell their wafer products using specifications that are close to those described by

Table 1 Commercially available wafer sizes.

Nominal size	Dimension (mm)	Diagonal (multi) (mm $\pm$ 1)	Diameter (mono) (inch)
103	103 $\pm$ 0.5	146	5
125	125 $\pm$ 0.5	177	6
150	150 $\pm$ 0.5	212	—

M61000. However, smaller wafers are usually 103 mm rather than 100 mm as specified, and there are some notable exceptions to the specifications, e.g. dimensions of wafers produced in-house by some of the early players who have developed their own standard and do not usually buy wafers on the market. Another obvious exception is provided by non-wafer substrates, the dimensions of which are in general determined by the growth equipment and technique. Some manufacturers use rectangular wafers. Other requirements, besides the geometrical definitions of the wafers, are thickness uniformity and reduced levels of cracks and saw marks that could adversely affect later processing.

Typical specifications for commercially available wafers are described in Table 2.

The absolute value of the wafer thickness has dropped by about 100 μ m in the last decade, as a consistent cost reduction measure [4, 5], and is expected to decrease further in the next years [2] as automation and cell processing become more sophisticated and can allow effective handling of thin wafers. Some wafer and cell producers already have less than 300 μ m wafers in their production lines, although in general wafer sizes in such cases are limited to the 100 cm² range in order to maintain mechanical yields in the high 90s. Similarly to the case of the area dimensions, thickness in non-wafer substrates is determined by the process, and is in general less homogeneous, providing one of the major differences between wafer and non-wafer cell technologies. A great deal of effort was put in the last decade in developing automated thickness measurement tools for manufacturing plants, to inspect wafer thickness variations in lots, an extremely difficult task in manually inspected wafer fabrication sequences.

2.2 Physical Specifications

Wafers are generally classified in terms of resistivity, type, and oxygen and carbon content. These data are generally present in all commercial specifications related to single and multicrystalline wafers, and refer to ASTM or equivalent standards. However, the PV community has had to face the unavoidable departure from standard test conditions of all parameters when measuring the properties of the inherently inhomogeneous nature of multicrystalline wafers, which led to agreement on relatively broad ranges for resistivity or upper thresholds for oxygen and carbon contents. Early concerns, for instance, of the influence of grain boundaries on the determination of resistivity using the

Table 2 Other dimensional specifications for typical PV wafers

Parameter	Value
Thickness of a batch	330 $\pm$ 40 μ m
Total Thickness Variation (TTV) of a wafer	50 μ m
Cracks	< 1 mm
Saw marks	< 10 μ m
Bow	< 50 μ m

four-point probe method are now somewhat more relaxed, after significant statistical feedback has provided comfort in the values proposed. Still, in strict terms, standards related to the measurement of resistivity in multicrystalline wafers do not exist, which is true of course for non-wafer silicon technologies as well. This is also true for other kinds of measurements, and the effort to develop meaningful characterisation tools for lower or inhomogeneous quality materials as compared to the semiconductor industry is a clear indication of such a need (see Chapter IIB-4). Furthermore, the increasing volumes of wafers in the growing PV market has forced a second, big departure from semiconductor wafer characterisation standards, imposing fast, non-destructive test methods to optimise costs and yields. In most cases, for instance, resistivity and type are measured at block rather than at wafer level. Table 3 shows the typical values for physical parameters of commercially available wafers for industrial processing. These are either multicrystalline or monocrystalline Czochralski. Float zone wafers for PV may become commercial products, and will be discussed in a later paragraph.

2.3 Physical Specifications

Minority carrier lifetime characterisation of commercial silicon is worth a paragraph on its own. This is by far the most complicated parameter to measure and to effectively relate to subsequent processing quality and yield. It is also most influenced by the inhomogeneity of multicrystalline silicon, as well as by thermal treatments. It became immediately evident to all PV manufacturers at the very beginning of the expansion of the multicrystalline silicon market that the identification of an appropriate tool for analysing and understanding the properties of mc-Si would have been one of the keys for the commercial success of the material. A generous number of attempts were made to adapt the existing lifetime measurements – rigorously valid for high quality polished single crystalline wafers – to provide meaningful values for mc-Si and even CZ-Si for the PV community. Also, as mentioned before, any acceptable test would need to be fast, cost effective, and obviously non-destructive as the number of samples to inspect was bound to be large. This focussed effort led to the development of a number of automated lifetime analysers, which at the end of the development process had relatively low resemblance with the semiconductor industry

Table 3 Physical specifications of commercial silicon wafers

Parameter	Value
Type	P – boron doped
Resistivity	0.5–3 ohm cm
Oxygen (mc-Si)	$< 8 \times 10^{17}$ at/cm ³
Oxygen (CZ-Si)	$< 1 \times 10^{18}$ at/cm ³
Carbon (mc-Si)	$< 1 \times 10^{18}$ at/cm ³
Carbon (CZ-Si)	$< 2 \times 10^{17}$ at/cm ³

counterparts. Probably the most successful commercial methods are the microwave photoconductance decay method (μ -PCD) performed directly on silicon blocks, and the photoconductance decay or quasi-steady state method developed by Ron Sinton which is discussed in Chapter IIB-4.

For the purposes of the present chapter, we will focus on the μ -PCD characterisation of mc-Si blocks. This measurement technique is commercially available and its use is widespread, although strong debates on the validity of the results occurred for many years. The measurement is based on the detection of the amplitude of the microwave field reflected by the sample surface. This amplitude variation depends on the conductivity, and thus also on the number of minority carriers generated by a short laser pulse [6]. The time in which the system recovers the initial state is associated with the quality of the semiconductor material and with the recombination mechanisms in the bulk and at the surface. It is generally rather complicated to separate different contributions, and PV silicon has peculiar characteristics which enhance difficulties, such as relatively high doping, rough surfaces and short diffusion lengths for minority carriers. Furthermore, as mentioned before, the industry requirements are for fast non-destructive techniques which enable prediction of later behaviour of the material in the processing line, in order to minimise the costs of processing low quality material as early as possible. For this reason, the industry has pushed towards the use of fast non-invasive block scanners since the early 1990s, despite the inability of the measurement systems to conform to any of the existing standards. A certain effort has been directed until relatively recently towards developing uniform measurement systems and procedures, which has proven once more the difficulty of the problem [7] and finally led to generally accepted principles subject to bilateral confirmation in the case of commercial relationships between wafer vendors and cell producers.

The main problems with block scanners, besides separation of bulk and surface components, lie in the fact that the measurement is actually performed on a very thin portion of the block. This is due to the absorption of the laser pulse in silicon (usually in the near infrared range) and to the high reflectivity of microwaves which only allow the field to penetrate a skin depth of the sample under examination. Other difficulties lie in the unpredictable behaviour of the material in three dimensions, lateral distribution of carriers, trapping effects, unknown injection levels, and the macroscopic saw damage affecting the control of the distance of the measurement head from the sample. Microwave block-scanners are unable to handle these problems, which are better taken into account by the technique described in Chapter IIB-4. The experience of crystal growers and the feedback from cell processing lines, however, led to the establishment of a method for the analysis of silicon blocks which is able to reject low quality material at block level, and which allows the identification of the correct cropping position for the rejection of tops and tails.

A typical map, performed with a commercially available automated system [8], of a standard block of mc-Si grown by the directional solidification method is shown in Figure 1. The silicon is boron doped to a resistivity of about 1×10^{16} at/cm³, and the measurement is performed with a microwave field in

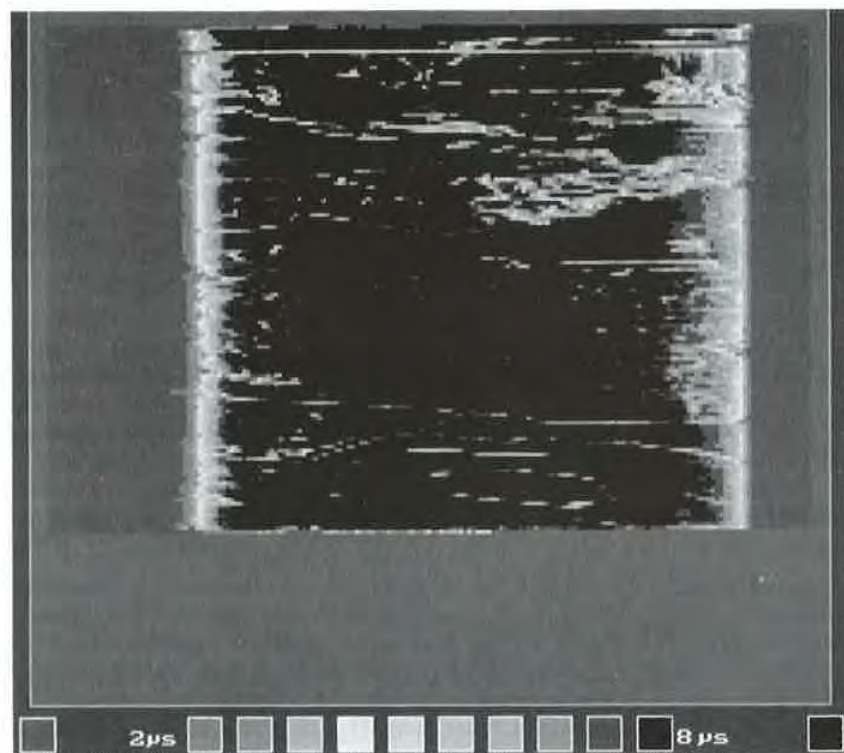


Figure 1 Lifetime map.

the GHz range coupled by an antenna for a sample irradiated by a laser diode pulse at 904 nm.

The absolute value of the minority carrier lifetime is surface limited, as the sample is measured 'as cut'. Normally, in fact, no impractical etching or passivation treatments are applied to the surface which therefore has a high recombination velocity. It is assumed that the surface is always in the same conditions, so any change in the relaxation time is associated with bulk properties. A map such as the one in Figure 1 takes a few minutes to be realised with a modern lifetime scanner such as the one in [8]. Early systems could take several hours to perform measurements with the same resolution. The low lifetime regions (in red) have different physical origins, and this is where the extensive material-to-cell correlation work performed over the years has been essential in comfortably introducing these instruments in the production environment [4, 5, 9]. The red zones at the top, in fact, are determined by the segregation of metals due to the refining process during solidification, and the wafers cannot effectively be used in cell processing, so they are rejected, and possibly remelted. The red zones at the bottom of the block are composed of a highly defected area – the initial crystal growth, highly dislocated and unusable

for solar cells within about 1 cm from the start – and the 2–3 cm region of oxygen rich material which, despite its low initial lifetime, recovers after the thermal treatments used in cell processing and normally produces good quality cells. Care must be taken, therefore, to exactly determine the cut off (by any means possible!) between good and low quality material at the bottom of the block, and this is probably the most difficult part of the quality control procedure at block level.

Figure 2 shows a typical correlation between the lifetime at block level and cell performance, being evidence of a good performance of initially low quality material as detected by the block scanner [9]. The central part of the block is instead relatively uniform and produces good quality cells, in the range 12–15% depending on the particular process used, the higher value provided by silicon nitride-based sequences.

Typical values in the central part of the blocks are around 5–10 μ s, depending on the specific measurement system used. A fundamental assumption of this method is a relative uniformity of the material in any given region of the block (i.e. all central regions behave similarly in same conditions), which is also a result of extensive correlation work [5, 9].

μ -PCD testers are also used to inspect incoming wafers in production lines, and in this case as well, there has been important correlation work to be able to confidently accept material for subsequent processing. This applies to CZ-Si wafers, which are inspected for uniformity as well as for the acceptance threshold value (which varies from case to case).

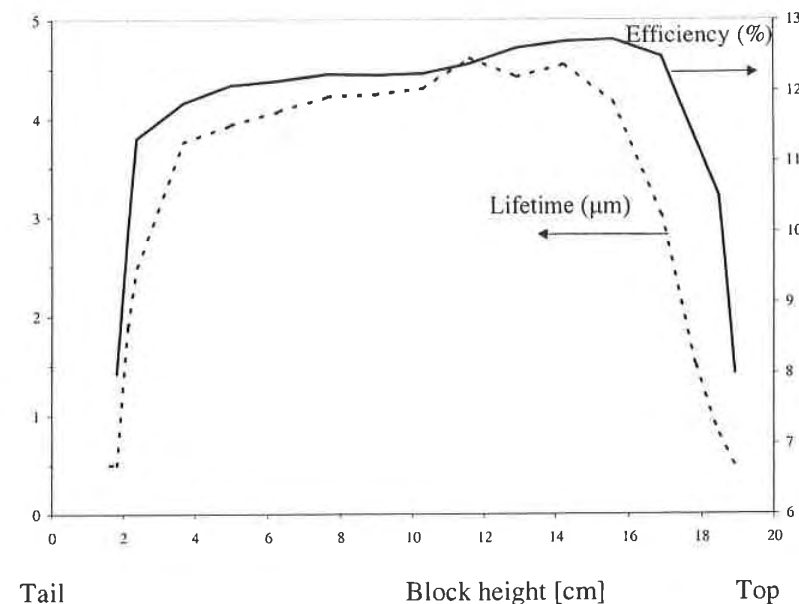


Figure 2 Correlation of lifetime with cell efficiency.

3 Feedstock Silicon

The commercial success of PV is driven critically by its cost. Silicon wafers account for about 50% of the total production cost of a module, a figure which has increased over the years, from the 33% of about 10 years ago, thanks to the constant improvements in technology which has allowed to identify the wafer as the ultimate cost limiting factor [10].

There is no source of silicon feedstock unique to the PV industry, so the issue of a possible feedstock shortage has been largely debated, and is still not concluded. About 10–15% of the silicon used by the microelectronics industry is available in various forms for PV use. This is in the range of 1800–2500 tons per year of higher quality scrap, and an extra 1500–2000 tons of lower quality material (e.g. pot scrap). Based on an effective usage rate of 10–15 tons per MWp produced, the amounts considered cannot feed the fast growing PV market for long. Whilst extensive research programmes have been conducted for many years to upgrade cheap metallurgical silicon to be an independent low cost silicon source for PV, none of the techniques proposed has reached commercial maturity [5]. The scare of a silicon shortage as early as the middle of the present decade has instead favoured several proposals for processes similar to those used for the production of polysilicon, but with looser specifications [11, 12].

From a practical point of view there is, in general, no constraint related to the geometrical specification of the starting material, so for the moment PV can enjoy low cost scrap such as silicon chips from the cutting processes of semiconductor manufacturing, popcorn silicon rods, tops and tails from crystal growth processes, etc. [13].

However, different crystallisation methods require different specifications. In general, monocrystalline and non-wafer technologies require high quality starting material, while the multicrystalline technology can allow a looser specification if some care is taken, due to its purifying characteristics – another point in its favour.

4 Crystal Preparation Methods

A number of techniques are available for the production of silicon wafers for the PV industry: CZ-Si and multicrystalline silicon (which have already been mentioned), magnetically confined multicrystalline silicon, float zone silicon and the non-wafer technologies (also already mentioned). In this paragraph we will briefly introduce the main features of each of them. The reader is encouraged to consult specific references for further details, as we will focus on the most relevant recent developments of the technologies under discussion.

4.1 Czochralski Silicon

The most common method for the growth of single crystalline ingots consists of pulling an oriented seed slowly out of the molten silicon contained in a pure

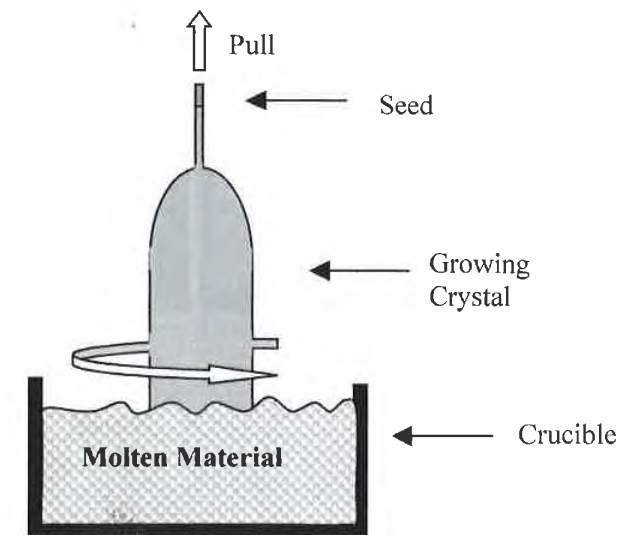


Figure 3 Schematic of CZ growth principle.

quartz crucible. The method is well known and extensively described in literature [10, 14].

What we will mention here is that a number of actions have been taken in the last 10 years to reduce the cost of CZ material, and regain competitiveness against multicrystalline silicon.

For instance, crystal growers now quite commonly use some kind of scrap silicon from the semiconductor industry as well as virgin poly as feedstock. Lower energy consumption, from the standard 100 kWh/kg figure to a promising 40 kWh/kg was recently reported due to improved furnace design, including heaters and gas distribution systems [15]. A crystallisation yield up to 70% from the standard 50% was also reported in the same study.

4.2 Multicrystalline Silicon

The realisation of multicrystalline silicon ingots is a relative simple process, and is based on controlling the extraction of heat from the melt in a quartz crucible in such a way that the interface between the growing solid and the ingot is as flat as possible. In this way, silicon grows in large columns of a few centimetres in section and as tall as 25 cm, and most detrimental impurities are segregated towards the top of the ingot. The critical steps to ensure a high quality and high yield process are in the design of the furnace for appropriate heat control, and in the quality of the quartz crucibles. A schematic of the general method is given in Figure 4.

Modern mc-Si furnaces are designed to minimise inhomogeneity, and maximise productivity [16, 17], and in the last few years a great deal of effort has