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I hereby appoint the practitioners associated with: **23900** as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to the address associated with the above-mentioned Customer Number.

Assignee Name and Address:

Name: United Microelectronics Corp.

Address: No. 3, Li-Hsin Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan,
R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE(S) of Assignee of the entire interest

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature: Chia-Tsung Hung Date: SEP 26 2012

Name: Chia-Tsung Hung

Title: CHAIRMAN

Company: United Microelectronics Corp.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: United Microelectronics Corp.

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

United Microelectronics Corp., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
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- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

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4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

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[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

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STATEMENT UNDER 37 CFR 3.73(c)

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/JIAWEI HUANG/

July 24, 2014

Signature

Date

JIAWEI HUANG

43,330

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The information provided by you in this form will be subject to the following routine uses:

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of and claims the priority benefit of U.S. application Ser. No. 13/370,231 filed on February 9, 2012, now pending. The entirety of the above-mentioned patent application is hereby incorporated by reference herein and made a part of specification.

BACKGROUND OF THE INVENTION

Field of Invention

[0001] This invention relates to a semiconductor process, and particularly relates to a method for fabricating fin-type field-effect transistors (FinFETs), and a semiconductor structure that is fabricated using the method.

Description of Related Art

[0002] MOS is a basic structure widely applied to various semiconductor devices, such as memory devices, image sensors and display devices.

[0003] The traditional MOS transistor is difficult to scale down due to the limitation of the fabricating process, so double-gate transistors with better properties are developed. One example is the FinFET, which has a 3D gate structure to enhance the control on the channel and inhibit the leakage current caused by the punch-through effect, and thus has a higher gate control capability than the conventional MOS transistor.

[0004] However, in the current FinFET process, the density of the fin patterns of the FinFET array is quite high and the thickness of the photoresist layer is quite large, so that the pattern development is difficult and an accurate pattern transfer is impossible.

SUMMARY OF THE INVENTION

[0005] Accordingly, this invention provides a method for fabricating FinFETs that is capable of solving the above problems of the prior art.

[0006] This invention also provides a semiconductor structure that is fabricated using the method of this invention.

[0007] The method for fabricating FinFETs of this invention is described as follows. A semiconductor substrate is patterned to form a plurality of odd fins. A plurality of spacers is formed on the substrate and on the sidewalls of the odd fins, wherein each spacer has a substantially vertical sidewall. A plurality of even fins is then formed on the substrate between the spacers.

[0008] In an embodiment, the substantially vertical-sidewall spacers are formed as follows. A substantially conformal material layer is formed over the substrate. An anisotropic treatment partially changing the etching selectivity of the material layer is performed to the material layer. The material layer is then selectively etched. The anisotropic treatment may include an ion-implantation process or a plasma treatment.

[0009] The semiconductor structure for forming FinFETs of this invention includes a semiconductor substrate, a plurality of odd fins of the FinFETs on the substrate, and a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs. The odd fins of the FinFETs are defined from the substrate. The even fins of the FinFETs are different from the odd fins of the FinFETs in at least one of the width

and the material, and may be further different from the odd fins of the FinFETs in the height.

[0010] The semiconductor structure for forming FinFETs of this invention includes a semiconductor substrate, a plurality of odd fins of the FinFETs on the substrate, and a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs. The even fins of the FinFETs are different from the odd fins of the FinFETs in at least one of the width and the material, and may be further different from the odd fins of the FinFETs in the height.

[0011] The semiconductor structure for forming FinFETs of this invention includes a semiconductor substrate, a plurality of first fins of the FinFETs on the substrate, and a plurality of second fins of the FinFETs on the substrate. Each of the second fins of the FinFETs is located between two first fins of the FinFETs. The second fins of the FinFETs are different from the first fins of the FinFETs in at least one of the width and the material, and may be further different from the first fins of the FinFETs in the height.

[0012] In the method for fabricating FinFETs of this invention, since the odd fins are formed prior to the even fins, the fin pattern density is greatly lowered and the thickness of the photoresist layer can be reduced, so that the development of fin patterns is much easier. Moreover, since the even fins are not formed simultaneously with the odd fins, the width thereof can be controlled by the width of each spacer or the thickness of the substantially conformal layer for forming the spacers, and the height thereof can be controlled by the growth process thereof, the even fins can be different from the odd fins in at least one of the height, the width and the material.

[0013] In order to make the aforementioned and other objects, features and advantages of the present invention comprehensible, a preferred embodiment accompanied with figures is described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIGs. 1-6 illustrate, in a cross-sectional view, a method for fabricating FinFETs patterning process according to an embodiment of this invention, wherein FIG. 6 also illustrates a semiconductor structure according to the embodiment.

DESCRIPTION OF EMBODIMENTS

[0015] It is noted that the following embodiment is intended to further explain this invention but not to limit its scope.

[0016] FIGs. 1-6 illustrate, in a cross-sectional view, a method for fabricating FinFETs patterning process according to an embodiment of this invention, wherein FIG. 6 also illustrates a semiconductor structure according to the embodiment.

[0017] Referring to FIG. 1, a semiconductor substrate 10 is provided, which may be a lightly doped single-crystal silicon substrate. A hard mask layer 12 is then formed on the substrate 10, possibly including silicon nitride (SiN) or SiON. When the hard mask layer 12 includes SiN, pad oxide 14 may be formed on the substrate 10 in advance. A patterned photoresist layer 16 with the patterns of the odd fins of the FinFETs is then formed on the hard mask layer 12. The photoresist layer 16 may include a positive or negative photoresist material.

[0018] Referring to FIG. 2, after the hard mask layer 12 is patterned using the patterned photoresist layer 16 as a mask, the substrate 10 is successively etched and

patterned using the patterned photoresist layer 16 and the patterned hard mask layer 12a as a mask to form a plurality of odd fins 10a. The patterned photoresist layer 16 is usually entirely consumed in the patterning process.

[0019] Referring to FIG. 3, a substantially conformal material layer 18 is formed over the substrate 10. The material layer 18 may be formed by an atomic layer deposition (ALD) process or a furnace deposition process, and the material thereof may be SiN. An anisotropic treatment 20 partially changing the etching selectivity of the material layer 18 is then performed to the material layer 18, forming low-selectivity regions 18a on the substrate 10 and on the sidewalls of the odd fins 10a, and high-selectivity regions 18b over the odd fins 10a and under the recesses regions of the material layer 18. The anisotropic treatment 20 is conducted in a manner such that the interface between any pair of a low-selectivity region 18a and an adjacent high-selectivity region 18b under a recesses region of the material layer 18 is substantially vertical. The anisotropic treatment 20 may include an ion-implantation process or a plasma treatment.

[0020] Referring to FIG. 4, a selective etching process is performed to remove the high-selectivity regions 18b, leaving the low-selectivity regions 18a as a plurality of spacers on the substrate 10 and on the sidewalls of the odd fins 10a, wherein each of the spacers 18a has a substantially vertical sidewall because the interface between any pair of a low-selectivity region 18a and an adjacent high-selectivity region 18b under a recesses region of the material layer 18 is substantially vertical.

[0021] In an embodiment, the material layer 18 includes SiN, the anisotropic treatment 20 includes an ion-implantation process that implants carbon ions in the to-be-removed portions of the material layer 18, and the selective etching for removing the high-selectivity regions 18b of the material layer 18 utilizes phosphoric acid.

[0022] Referring to FIG. 5, a plurality of even fins 20 is then formed on the substrate 10 between the spacers 18a, possibly by an epitaxy process as a selective deposition process based on the exposed surfaces of the semiconductor substrate 10. When the semiconductor substrate 10 includes Si, the product material of the epitaxy process may be Si, SiGe or SiC.

[0023] Since the even fins 20 are not formed simultaneously with the odd fins 10a, the material thereof can be different from that of the odd fins 10a. For example, it is possible that the odd fins 10a include Si and the even fins 20 comprise SiC or SiGe. Nevertheless, the even fins 20 may alternatively be formed from the same material (e.g., Si) of the odd fins 10a, which is namely the material of the substrate 10, by epitaxy.

[0024] In addition, the width of each even fin 20 can be controlled by the width of each spacer 18a (see FIG. 4), which is in turn controlled by the deposition thickness of the substantially conformal material layer 18 for forming the spacers 18a (see FIG. 3). The height of the even fins 20 can be controlled by the growth process of the even fins 20. Accordingly, the even fins 20 may be different from the odd fins 10a in at least one of the height, the width and the material.

[0025] Referring to FIG. 6, the patterned hard mask layer 12a and the spacers 18a are removed, leaving the odd fins 10a and even fins 20 that are arranged alternately.

[0026] FIG. 6 also illustrates a semiconductor structure according to the embodiment of this invention. The semiconductor structure includes odd fins 10a and even fins 20 that are arranged alternately. The odd fins 10a are defined from the semiconductor substrate 10. The even fins 20 may be different from the odd fins 10a in at least one of the width and the material, and may be further different from the odd fins 10a also in height, as mentioned above.

[0027] In the above embodiment of this invention, since the odd fins are formed prior to the even fins, their pattern density is greatly reduced and the thickness of the photoresist layer can be reduced, so that the development of fin patterns is much easier.

[0028] This invention has been disclosed above in the preferred embodiments, but is not limited to those. It is known to persons skilled in the art that some modifications and innovations may be made without departing from the spirit and scope of this invention. Hence, the scope of this invention should be defined by the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate;
a plurality of odd fins of the FinFETs on the substrate, being defined from the substrate; and
a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material.
2. The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.
3. The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material.
4. The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.
5. The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.
6. The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.
7. A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate;
a plurality of odd fins of the FinFETs on the substrate; and
a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material.

8. The semiconductor structure of claim 7, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

9. The semiconductor structure of claim 7, wherein the even fins of the FinFETs comprise an epitaxy material.

10. The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

11. The semiconductor structure of claim 7, wherein the odd fins of the FinFETs comprise Si.

12. The semiconductor structure of claim 7, wherein the even fins of the FinFETs comprise SiC or SiGe.

13. A semiconductor structure for forming FinFET, comprising
a semiconductor substrate;
a plurality of first fins of the FinFETs on the substrate; and
a plurality of second fins of the FinFETs on the substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material.

14. The semiconductor structure of claim 13, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.

15. The semiconductor structure of claim 13, wherein the second fins of the FinFETs comprise an epitaxy material.

16. The semiconductor structure of claim 15, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.

17. The semiconductor structure of claim 13, wherein the first fins of the FinFETs

comprise Si.

18. The semiconductor structure of claim 13, wherein the second fins of the FinFETs comprise SiC or SiGe.

ABSTRACT OF THE DISCLOSURE

A semiconductor structure for forming FinFETs is described. The semiconductor structure includes a semiconductor substrate, a plurality of odd fins of the FinFETs on the substrate, and a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs. The odd fins of the FinFETs are defined from the substrate. The even fins of the FinFETs are different from the odd fins of the FinFETs in at least one of the width and the material, and may be further different from the odd fins of the FinFETs in the height.

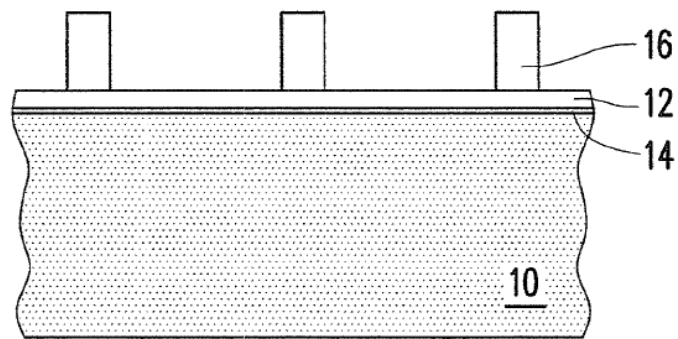


FIG. 1

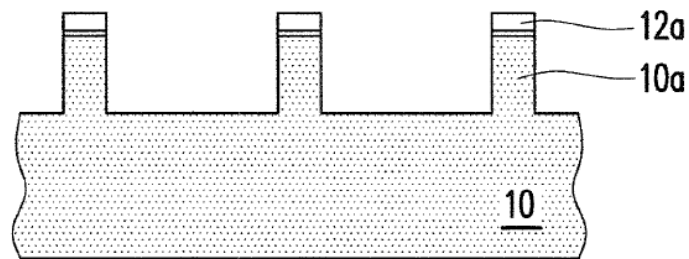


FIG. 2

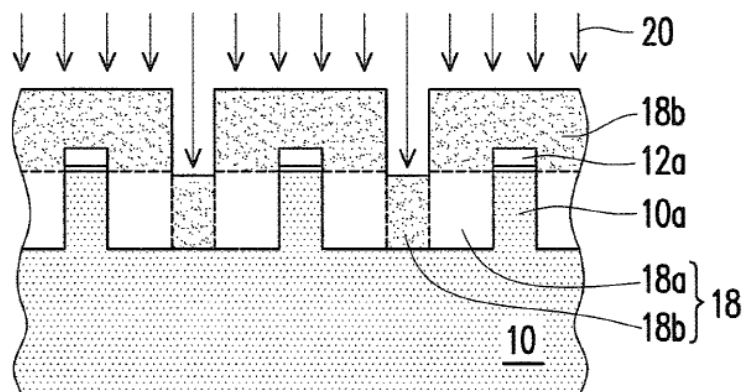


FIG. 3

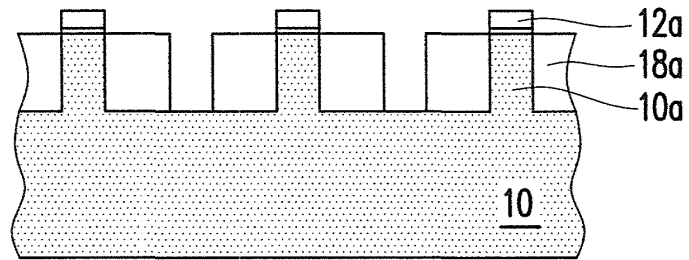


FIG. 4

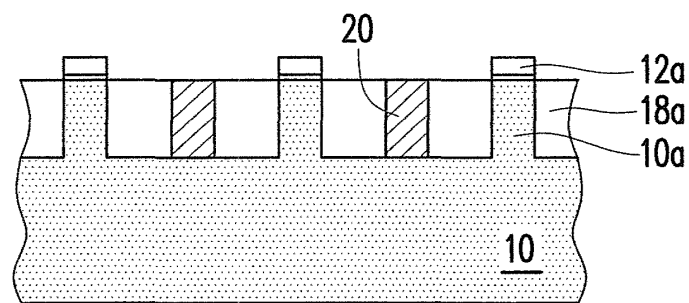


FIG. 5

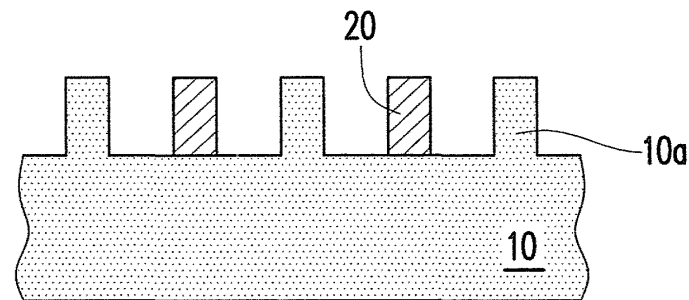


FIG. 6

Doc code: IDS

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	First Named Inventor	Chin-Fu Lin	
	Art Unit		
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	Attorney Docket Number	JCLA40585-D	

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	1	7888192		2011-02-15	Marshall, et al.	
	2	6492216		2002-12-10	Yeo, et al.	
	3	6921963		2005-07-26	Krivokapic, et al.	
	4	7087477		2006-08-08	Fried, et al.	
	5	7247887		2007-07-24	King, et al.	
	6	7250658		2007-07-31	Doris, et al.	
	7	7309626		2007-12-18	leong, et al.	
	8	7470570		2008-12-30	Beintner, et al.	

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	First Named Inventor	Chin-Fu Lin	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	JCLA40585-D	

	9	7531437		2009-05-12	Brask, et al.	
	10	7569857		2009-08-04	Simon, legal representative, et al.	
	11	6043138		2000-03-28	Ibok	
	12	7091551		2006-08-15	Anderson, et al.	
	13	7352034		2008-04-01	Booth, Jr., et al.	
	14	6500725		2002-12-31	Chen , et al.	

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	1	20050051825		2005-03-10	Fujiwara, Makoto; et al.	
	2	20060286729		2006-12-21	Kavalieros; Jack; et al.	
	3	20070108528		2007-05-17	Anderson; Brent A.; et al.	

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	First Named Inventor	Chin-Fu Lin	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	JCLA40585-D	

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	5	20080157208		2008-07-03	Fischer; Kevin J.; et al.	
	6	20090124097		2009-05-14	Cheng; Kangguo	
	7	20090269916		2009-10-29	KANG; Inkuk; et al.	
	8	20100072553		2010-03-25	XU; Jeff J.; et al.	
	9	20100167506		2010-07-01	LIN; Simon Su-Horng; et al.	
	10	20060099830		2006-05-11	Walther; Steven R.; et al.	
	11	20100048027		2010-02-25	Cheng; Kangguo; et al.	
	12	20100144121		2010-06-10	Chang; Cheng-Hung; et al.	
	13	20040195624		2004-10-07	Liu, Chee-Wee; et al.	
	14	20090242964		2009-10-01	Akil; Nader; et al.	

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	First Named Inventor	Chin-Fu Lin	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	JCLA40585-D	

	15	20120043597		2012-02-23	Chen; Howard H. ; et al.	
	16	20120028473		2012-02-02	Lai; Chih-Yu ; et al.	
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	18	20090159936		2009-06-25	Shah; Uday ; et al.	
	19	20070010049		2007-01-11	Anderson; Brent A. ; et al.	
	20	20080020515		2008-01-24	White; Ted R. ; et al.	
	21	20100193770		2010-08-05	Bangsaruntip; Sarunya ; et al.	
	22	20140054650		2014-02-27	Colinge; Jean-Pierre	

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	1	SANCHEZ ET AL., "Low-Temperature Growth of Epitaxial Beta-SiC on Si(100) Using Supersonic Molecular Beams of Methylsilane," J. Phys. Chem. B., July 2002, pp. 8019-8028.	☒
	2	"Archived wikipedia entry of Silicon," Wikipedia, July 2013, pp. 1-9.	☒
	3	"Archived wikipedia entry of Silicon carbide," Wikipedia, July 2013, pp. 1-8.	☒
If you wish to add additional non-patent literature document citation information please click the Add button Add			
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			
<small> ¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached. </small>			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		
	First Named Inventor	Chin-Fu Lin	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	JCLA40585-D	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JIAWEI HUANG/	Date (YYYY-MM-DD)	2014-07-24
Name/Print	JIAWEI HUANG	Registration Number	43330

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		
First Named Inventor/Applicant Name:		CHIN-FU LIN		
Filer:		Jiawei Huang/Michelle Chang		
Attorney Docket Number:		JCLA40585-D		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	19678218
Application Number:	14340267
International Application Number:	
Confirmation Number:	8893
Title of Invention:	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS
First Named Inventor/Applicant Name:	CHIN-FU LIN
Customer Number:	23900
Filer:	Jiawei Huang/Michelle Chang
Filer Authorized By:	Jiawei Huang
Attorney Docket Number:	JCLA40585-D
Receipt Date:	24-JUL-2014
Filing Date:	
Time Stamp:	17:50:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	4373
Deposit Account	500710
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	40585-D_ADS.pdf	1561451	no	8
			677819dea1534b03e7e51912821d5a0a8794e7b2		
Warnings:					
Information:					
2	Oath or Declaration filed	40585-D_Combined_Declaration_Assignment.pdf	234182	no	6
			4d94d50d182c2ad1269f0bf079bf5d5388ce4f7		
Warnings:					
Information:					
3	Power of Attorney	40585-D_POA.pdf	49958	no	1
			ebe508269926c5e4b581bf6c47f764b0935df742		
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73.	40585-D_Statement-373.pdf	134703	no	3
			501904c6c58795ba977146041b0a6af0e4674000		
Warnings:					
Information:					
5	Specification	40585-D_Specification.pdf	493666	no	13
			16fc9858507d8c1fc9cb48d356e5a68814e03b85		
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Form (SB08)	40585-D_IDS.pdf	613896	no	7
			19bc1015888253eebbd270536af49cc5e57771b2		
Warnings:					
Information:					
7	Non Patent Literature	40585-D_IDS_NPL-1.pdf	1923365	no	10
			1617645360c24f20876bf8630fb4a6d4d38a95e6		
Warnings:					
Information:					
8	Non Patent Literature	40585-D_IDS_NPL-2.pdf	875974	no	9
			13b374b1a1f8325fb0f1d2d3e086853c7bfd a589		
Warnings:					
Information:					

9	Non Patent Literature	40585-D_IDS_NPL-3.pdf	895409 2acd01d2a76b918e97ffa8a92b40d5720aaf785a	no	8
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	32968 8541f99fe95bad83aa1e920659e6f338d35a9e39	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			6815572		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA40585-D
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chin-Fu		Lin		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tainan City	Country of Residence i	TW		
Mailing Address of Inventor:					
Address 1		No.16, Ln. 92, Yunong 1st St., East Dist.,			
Address 2					
City	Tainan City	State/Province			
Postal Code	701	Country i	TW		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chin-Cheng		Chien		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tainan City	Country of Residence i	TW		
Mailing Address of Inventor:					
Address 1		No.88, Ln. 35, Guanghua Rd., Shanhua Dist.,			
Address 2					
City	Tainan City	State/Province			
Postal Code	741	Country i	TW		
Inventor 3					Remove
Legal Name					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number		JCLA40585-D	
		Application Number			
Title of Invention		SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS			

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chun-Yuan		Wu	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Yunlin County	Country of Residence i	TW	
Mailing Address of Inventor:				
Address 1		No.3-1, Tiansin, Gukeng Township,		
Address 2				
City	Yunlin County	State/Province		
Postal Code	646	Country i	TW	
Inventor 4				Remove
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Teng-Chun		Tsai	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Tainan City	Country of Residence i	TW	
Mailing Address of Inventor:				
Address 1		No.930, Chongming Rd., East Dist.,		
Address 2				
City	Tainan City	State/Province		
Postal Code	701	Country i	TW	
Inventor 5				Remove
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Chih-Chien		Liu	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Taipei City	Country of Residence i	TW	
Mailing Address of Inventor:				
Address 1		7F., No.59-2, Linsen S. Rd., Jhongjheng District,		
Address 2				
City	Taipei City	State/Province		
Postal Code	100	Country i	TW	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA40585-D
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Customer Number	23900		
Email Address	jcpatents@sbcglobal.net	Add Email	Remove Email
Email Address	jcpi@msn.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		
Attorney Docket Number	JCLA40585-D	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	2	Suggested Figure for Publication (if any)	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
<p>Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.</p>

Representative Information:

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA40585-D
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		
<p>Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.</p>			
<p>Please Select One: ☒ Customer Number ☐ US Patent Practitioner ☐ Limited Recognition (37 CFR 11.9)</p>			
Customer Number	23900		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	13370231	2012-02-09
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA40585-D
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

<p>This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.</p> <p>☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.</p>
--

Authorization to Permit Access:

<p>☐ Authorization to Permit Access to the Instant Application by the Participating Offices</p> <p>If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.</p> <p>In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.</p> <p>In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.</p>

Applicant Information:

<p>Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.</p>
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA40585-D
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		

Applicant 1				Remove
<p>If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.</p>				
Clear				
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117		☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.			☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:				
Name of the Deceased or Legally Incapacitated Inventor : <input type="text"/>				
If the Applicant is an Organization check here. ☒				
Organization Name	United Microelectronics Corp.			
Mailing Address Information:				
Address 1	No. 3, Li-Hsin Rd. II,			
Address 2	Science-Based Industrial Park,			
City	Hsinchu	State/Province		
Country i	TW	Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Applicant Data may be generated within this form by selecting the Add button. Add				

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.	
Assignee 1	
<p>Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.</p>	
Remove	
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	JCLA40585-D
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		State/Province	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/JIAWEI HUANG/		Date (YYYY-MM-DD)	2014-07-24	
First Name	JIAWEI	Last Name	HUANG	Registration Number	43330

Additional Signature may be generated within this form by selecting the Add button.

Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**DECLARATION AND ASSIGNMENT
FOR UTILITY OR DESIGN PATENT APPLICATION**

☒ Declaration Submitted With Initial Filing

OR

☐ Declaration Submitted After Initial Filing (surcharge 37 CFR 1.16(f) required)

(Title of the Invention)

SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

As a below named inventor (hereinafter designated as the undersigned), I hereby
declare that:

This declaration is directed to:

☒ The attached application,

OR

☐ United States Application Number or PCT International application number

_____ Filed on _____

The above-identified application was made or authorized to be made by me.

I believe I am the original inventor or an original joint inventor of a claimed invention in
the application.

**DECLARATION AND ASSIGNMENT
FOR UTILITY OR DESIGN PATENT APPLICATION**

WHEREAS, the undersigned has invented certain new and useful improvements described in the application identified.

WHEREAS 1. United Microelectronics Corp.
of No. 3, Li-Hsin Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan,
R.O.C.

hereinafter referred to as ASSIGNEE, is desirous of acquiring the undersigned's interest in the said invention and application and in any U.S. Letters Patent which may be granted on the same:

NOW, THEREFORE, TO ALL WHOM IT MAY CONCERN: Be it known that, for good and valuable consideration, receipt of which is hereby acknowledged by the undersigned, the undersigned has/have sold, assigned and transferred, and by these presents does/do sell, assign and transfer unto the said Assignee, and Assignee's successors and assigns, all his/her/their rights, title and interest in and to the said invention and application and all future improvements thereon, and in and to any Letters Patent which may hereafter be granted on the same in the United States, the said rights, title and interest to be held and enjoyed by said Assignee as fully and exclusively as it would have been held and enjoyed by said the undersigned had this Assignment and transfer not been made, to the full end and term of any Letters Patent which may be granted thereon, or of any division, renewal, continuation in whole or in part, substitution, conversion, reissue, prolongation or extension thereof.

The undersigned further agrees/agree that he/she/they will, without charge to said Assignee, but at Assignee's expense, cooperate with Assignee in the prosecution of said application and/or applications, execute, verify, acknowledge and deliver all such further papers, including applications for Letters Patent and for the reissue thereof, and instruments of assignment and transfer thereof, and will perform such other acts as Assignee Lawfully may request, to obtain or maintain Letters Patent for said invention and improvement, and to vest title thereto in said Assignee, or Assignee's successors and assigns.

The undersigned hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

**DECLARATION AND ASSIGNMENT
FOR UTILITY OR DESIGN PATENT APPLICATION**

Signature: Chin-Fu Lin Date: JUL 17 2014

Legal Name of Sole or First Inventor: Chin-Fu Lin

Residence: Tainan City, Taiwan

Mailing Address: No.16, Ln. 92, Yunong 1st St., East Dist., Tainan City 701, Taiwan (R.O.C.)

Signature: Chin-cheng Chien Date: JUL 17 2014

Legal Name of Additional Joint Inventor, if any: Chin-Cheng Chien

Residence: Tainan City, Taiwan

Mailing Address: No.88, Ln. 35, Guanghua Rd., Shanhua Dist., Tainan City 741, Taiwan (R.O.C.)

Signature: Chun-Yuan Wu Date: JUL 17 2014

Legal Name of Additional Joint Inventor, if any: Chun-Yuan Wu

Residence: Yunlin County, Taiwan

Mailing Address: No.3-1, Tiansin, Gukeng Township, Yunlin County 646, Taiwan, R.O.C.

Signature: _____ Date: _____

Legal Name of Additional Joint Inventor, if any: Teng-Chun Tsai

Residence: Tainan City, Taiwan

Mailing Address: No.930, Chongming Rd., East Dist., Tainan City 701, Taiwan (R.O.C.)

Signature: Chih-Chien Liu Date: JUL 17 2014

Legal Name of Additional Joint Inventor, if any: Chih-Chien Liu

Residence: Taipei City, Taiwan

Mailing Address: 7F., No.59-2, Linsen S. Rd., Jhongjheng District, Taipei City 100, Taiwan, R.O.C.

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Signature: _____ Date: _____

Legal Name of Additional Joint Inventor, if any: Chin-Cheng Chien

Residence: Tainan City, Taiwan

Mailing Address: No.88, Ln. 35, Guanghua Rd., Shanhuia Dist., Tainan City 741, Taiwan (R.O.C.)

Signature: _____ Date: _____

Legal Name of Additional Joint Inventor, if any: Chun-Yuan Wu

Residence: Yunlin County, Taiwan

Mailing Address: No.3-1, Tiansin, Gukeng Township, Yunlin County 646, Taiwan, R.O.C.

Signature: Teng-Chun Tsai Date: JUL 03 2014

Legal Name of Additional Joint Inventor, if any: Teng-Chun Tsai

Residence: Tainan City, Taiwan

Mailing Address: No.930, Chongming Rd., East Dist., Tainan City 701, Taiwan (R.O.C.)

Signature: _____ Date: _____

Legal Name of Additional Joint Inventor, if any: Chih-Chien Liu

Residence: Taipei City, Taiwan

Mailing Address: 7F., No.59-2, Linsen S. Rd., Jhongjheng District Taipei City 100, Taiwan, R.O.C.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT2953296

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
CHIN-FU LIN	07/17/2014
CHIN-CHENG CHIEN	07/17/2014
CHUN-YUAN WU	07/17/2014
TENG-CHUN TSAI	07/17/2014
CHIH-CHIEN LIU	07/17/2014
RECEIVING PARTY DATA	
Name:	UNITED MICROELECTRONICS CORP.
Street Address:	NO. 3, LI-HSIN RD. II, SCIENCE-BASED INDUSTRIAL PARK
City:	HSINCHU
State/Country:	TAIWAN
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	14340267
CORRESPONDENCE DATA	
Fax Number:	(949)660-0809
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Phone:	9496600761
Email:	jcpatents@sbcglobal.net
Correspondent Name:	J.C. PATENTS
Address Line 1:	4 VENTURE, SUITE 250
Address Line 4:	IRVINE, CALIFORNIA 92618
ATTORNEY DOCKET NUMBER:	JCLA40585-D
NAME OF SUBMITTER:	JIAWEI HUANG
SIGNATURE:	/JIAWEI HUANG/
DATE SIGNED:	07/24/2014
This document serves as an Oath/Declaration (37 CFR 1.63).	
Total Attachments: 6	
source=40585-D_Combined_Declaration_Assignment#page1.tif	
source=40585-D_Combined_Declaration_Assignment#page2.tif	

source=40585-D_Combined_Declaration_Assignment#page3.tif
source=40585-D_Combined_Declaration_Assignment#page4.tif
source=40585-D_Combined_Declaration_Assignment#page5.tif
source=40585-D_Combined_Declaration_Assignment#page6.tif

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Signature: Chin-cheng Chien Date: JUL 17 2014

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Residence: Tainan City, Taiwan

Mailing Address: No.88, Ln. 35, Guanghua Rd., Shanhua Dist., Tainan City 741, Taiwan (R.O.C.)

Signature: Chun-Yuan Wu Date: JUL 17 2014

Legal Name of Additional Joint Inventor, if any: Chun-Yuan Wu

Residence: Yunlin County, Taiwan

Mailing Address: No.3-1, Tiansin, Gukeng Township, Yunlin County 646, Taiwan, R.O.C.

Signature: _____ Date: _____

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Residence: Tainan City, Taiwan

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Signature: Chih-Chien Liu Date: JUL 17 2014

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Residence: Yunlin County, Taiwan

Mailing Address: No.3-1, Tiansin, Gukeng Township, Yunlin County 646, Taiwan, R.O.C.

Signature: Teng-Chun Tsai Date: JUL 03 2014

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Residence: Taipei City, Taiwan

Mailing Address: 7F., No.59-2, Linsen S. Rd., Jhongjheng District Taipei City 100, Taiwan, R.O.C.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/340,267	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE <small>(37 CFR 1.16(a), (b), or (c))</small>	N/A	N/A	N/A			N/A	280
SEARCH FEE <small>(37 CFR 1.16(k), (l), or (m))</small>	N/A	N/A	N/A			N/A	600
EXAMINATION FEE <small>(37 CFR 1.16(o), (p), or (q))</small>	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS <small>(37 CFR 1.16(i))</small>	18	minus 20 = *				x 80 =	0.00
INDEPENDENT CLAIMS <small>(37 CFR 1.16(h))</small>	3	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE <small>(37 CFR 1.16(s))</small>	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT <small>(37 CFR 1.16(j))</small>							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)
	Total <small>(37 CFR 1.16(i))</small>	*	Minus	**	=	x =	x =
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus	***	=	x =	x =
	Application Size Fee <small>(37 CFR 1.16(s))</small>						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						
				TOTAL ADD'L FEE			TOTAL ADD'L FEE
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)
	Total <small>(37 CFR 1.16(i))</small>	*	Minus	**	=	x =	x =
	Independent <small>(37 CFR 1.16(h))</small>	*	Minus	***	=	x =	x =
	Application Size Fee <small>(37 CFR 1.16(s))</small>						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <small>(37 CFR 1.16(j))</small>						
				TOTAL ADD'L FEE			TOTAL ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/340,267	07/24/2014	2812	1600	JCLA40585-D	18	3

CONFIRMATION NO. 8893

23900
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

FILING RECEIPT



OC000000069976946

Date Mailed: 08/05/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Chin-Fu Lin, Tainan City, TAIWAN;
Chin-Cheng Chien, Tainan City, TAIWAN;
Chun-Yuan Wu, Yunlin County, TAIWAN;
Teng-Chun Tsai, Tainan City, TAIWAN;
Chih-Chien Liu, Taipei City, TAIWAN;

Applicant(s)

United Microelectronics Corp., Hsinchu, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 23900

Domestic Priority data as claimed by applicant

This application is a DIV of 13/370,231 02/09/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/01/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/340,267**

Projected Publication Date: 11/13/2014

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/340,267	07/24/2014	Chin-Fu Lin	JCLA40585-D	8893

23900 7590 11/04/2014
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER

REIDA, MOLLY KAY

ART UNIT	PAPER NUMBER
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2816

MAIL DATE	DELIVERY MODE
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11/04/2014

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/340,267	Applicant(s) LIN ET AL.	
	Examiner MOLLY REIDA	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07/24/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-18 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-18 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 07/24/2014 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date <u>07/24/2014</u> . | 4) ☐ Other: ____. |

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Information Disclosure Statement

Acknowledgement is made of Applicant's Information Disclosure Statement (IDS) submitted on 07/24/2014. This IDS has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by White et al. (US Pub. 2008/0020515), or in the alternative, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over White et al. (US Pub. 2008/0020515).

Regarding independent claim 1, White teaches a semiconductor structure (Fig. 9) for forming FinFETs, comprising

a semiconductor substrate (11, para. 0027);

a plurality of odd fins of the FinFETs (in region 97, formed of material 90) on the substrate, being defined from the substrate; and

Art Unit: 2816

a plurality of even fins (in region 98, formed of material 70) of the FinFETs on the substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width (para. 0040) and material (para. 0028, 0033).

The embodiment disclosed by White does not explicitly show a plurality of even fins; however, the pattern disclosed by White was the minimum structure needed to understand the invention and it is standard in the semiconductor art to continue a base pattern (for example continuing the pattern of Fig. 9 to the left and/or right of the pattern disclosed); thus a plurality of even fins is considered to be anticipated, or at the very least obvious to one of ordinary skill in the art over the disclosure of white (refer also to para 0025-0026).

Regarding independent claim 7, White teaches a semiconductor structure (Fig. 9) for forming FinFETs, comprising

a semiconductor substrate (11, para. 0027);

a plurality of odd fins (in region 97, formed of material 90) of the FinFETs on the substrate; and

a plurality of even fins (in region 98, formed of material 70) of the FinFETs on the substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width (para. 0040) and material (para. 0028, 0033).

The embodiment disclosed by White does not explicitly show a plurality of even fins; however, the pattern disclosed by White was the minimum structure needed to understand the invention and it is standard in the semiconductor art to continue a base pattern (for example continuing the pattern of Fig. 9 to the left and/or right of the pattern disclosed); thus a plurality of even fins is considered to be anticipated, or at the very least obvious to one of ordinary skill in the art over the disclosure of white (refer also to para 0025-0026).

Regarding dependent claims 2 and 8, White teaches wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height (para. 0040).

Regarding dependent claims 3 and 9, White teaches wherein the even fins of the FinFETs comprise an epitaxy material (para. 0033).

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Regarding dependent claims 4 and 10, White teaches wherein the odd fins of the FinFETs comprise Si (para. 0028) and the even fins of the FinFETs comprise SiC or SiGe (para. 0033).

Regarding dependent claims 5 and 11, White teaches wherein the odd fins of the FinFETs comprise Si (para. 0028).

Regarding dependent claims 6 and 12, White teaches wherein the even fins of the FinFETs comprise SiC or SiGe (para. 0033).

Regarding independent claim 13, White teaches a semiconductor structure (Fig. 9) for forming FinFET, comprising

a semiconductor substrate (106, para. 0027);

a plurality of first fins (in region 97, formed of material 90) of the FinFETs on the substrate; and

a plurality of second fins (in region 98, formed of material 70) of the FinFETs on the substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width (para. 0040) and material (para. 0028, 0033).

The embodiment disclosed by White does not explicitly show a plurality of second fins; however, the pattern disclosed by White was the minimum structure needed to understand the invention and it is standard in the semiconductor art to continue a base pattern (for example continuing the pattern of Fig. 9 to the left and/or right of the pattern disclosed); thus a plurality of even fins is considered to be anticipated, or at the very least obvious to one of ordinary skill in the art over the disclosure of white (refer also to para 0025-0026).

Regarding dependent claim 14, White teaches wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height (para. 0040).

Regarding dependent claim 15, White teaches wherein the second fins of the FinFETs comprise an epitaxy material (para. 0033).

Regarding dependent claim 16, White teaches wherein the first fins of the FinFETs comprise Si (para. 0028) and the second fins of the FinFETs comprise SiC or SiGe (para. 0033).

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Regarding dependent claim 17, White teaches wherein the first fins of the FinFETs comprise Si (para. 0028).

Regarding dependent claim 18, White teaches wherein the second fins of the FinFETs comprise SiC or SiGe (para. 0033).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOLLY REIDA whose telephone number is (571)272-4237. The examiner can normally be reached on Mon-Fri 8:30-5:00 (approx).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571)272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOLLY REIDA/
Examiner, Art Unit 2816

/CHUONG A LUU/
Primary Examiner, Art Unit 2898

Notice of References Cited	Application/Control No. 14/340,267	Applicant(s)/Patent Under Reexamination LIN ET AL.	
	Examiner MOLLY REIDA	Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0020515	01-2008	White et al.	438/118
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 14340267	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner MOLLY REIDA	Art Unit 2816

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/0886, H01L29/66795, H01L29/785, H01L29/7851, H01L29/7855, H01L29/7856, H01L2029/785 H012029/7858, H01L21/823431, combined with text search,	10/21/2014	mkr

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	288,289,368,401,618,623,E21.618,E21.619,E21.633, combined with text search	10/21/2014	mkr
438	151,154,197,275, combined with text search	10/21/2014	mkr

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Text Search	10/21/2014	mkr
Inventor(s)	10/21/2014	mkr

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L30	4	("20140027860" "20130270559" "20130119482" "20140197456").pn.	US-PGPUB; USPAT	OR	ON	2014/10/21 10:28
L31	0	("2014/0197456").URPN.	USPAT	OR	ON	2014/10/21 10:28
L32	0	("2013/0270559").URPN.	USPAT	OR	ON	2014/10/21 10:29
L33	0	("2014/0027860").URPN.	USPAT	OR	ON	2014/10/21 10:29
L34	4	("2013/0119482").URPN.	USPAT	OR	ON	2014/10/21 10:30
L35	41	(glass near2 glenn).inv.	US-PGPUB; USPAT	OR	ON	2014/10/21 10:32
L36	3	"2013095646"	EPO; DERWENT	OR	ON	2014/10/21 10:43
L37	9	("8053299" "7667271" "20110147842" "20120146101" "20060048697" "20080048269" "7208815" "20060292770" "20060214226").pn.	US-PGPUB; USPAT	OR	ON	2014/10/21 10:52
L38	36	("7888192" "6492216" "6921963" "7087477" "7247887" "7250658" "7309626" "7470570" "7531437" "7569857" "6043138" "7091551" "7352034" "6500725" "20050051825" "20060286729" "20070108528" "20070158756" "20080157208" "20090124097" "20090269916" "20100072553" "20100167506" "20060099830" "20100048027" "20100144121" "20040195624" "20090242964" "20120043597" "20120028473" "20080121970" "20090159936" "20070010049" "20080020515" "20100193770" "20140054650").pn.	US-PGPUB; USPAT	OR	ON	2014/10/21 11:58
L39	12700	438/151,154,275.ccls. 257/401,E21.618,E21.633.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:06
L40	97977	(substrate wafer) with (fin pillar column mast post shaft pilaster connade castellated)	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:06
L41	612346	(substrate wafer) with (trench recess groove open\$3 hole via)	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:06
L42	31245	(trench recess groove open\$3 hole via) with (epi epitax\$5)	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:06
L43	178	L39 and L40 and L41 and L42	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:06
L44	9322	(fin\$1fet\$1) (tri\$1gate\$1) ("3"\$1D\$4fet\$1) ("3"\$1dimentional near2 (fet mosfet)) (three\$1dimentional near2 (fet mosfet))	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:12
L45	708	L40 and L41 and L42 and L44	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:12
L46	599	L45 not L43	US-PGPUB; USPAT;	OR	ON	2014/10/21 12:12

			USOCR			
L47	0	("2013/0302975").URPN.	USPAT	OR	ON	2014/10/21 12:26
L48	12700	438/151,154,275.ccls. 257/401,E21.618,E21.633.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L49	97977	(substrate wafer) with (fin pillar column mast post shaft pilaster connade castellated)	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L50	612346	(substrate wafer) with (trench recess groove open\$3 hole via)	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L51	31245	(trench recess groove open\$3 hole via) with (epi epitax\$5)	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L52	178	L48 and L49 and L50 and L51	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L53	9322	(fin\$1fet\$1) (tri\$1gate\$1) ("3"\$1D\$4fet\$1) ("3"\$1dimentional near2 (fet mosfet)) (three\$1dimentional near2 (fet mosfet))	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L54	708	L49 and L50 and L51 and L53	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L55	599	L54 not L52	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:32
L56	10855	(H01L27/0886 H01L29/66795 H01L29/785 H01L29/7851 H01L29/7855 H01L29/7856 H01L2029/785 H01L2029/7858).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:32
L57	146050	(substrate wafer) with (fin pillar column mast post shaft pilaster connade castellated)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:32
L58	1081490	(substrate wafer) with (trench recess groove open\$3 hole via)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:32
L59	46864	(trench recess groove open\$3 hole via) with (epi epitax\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:32
L60	543	L56 and L57 and L58 and L59	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:32

L61	82	L60 not (L52 L55)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:32
L62	14128	(substrate wafer) with (fin pillar column mast post shaft pilaster connade castellated) with (etch\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:35
L63	2338	(substrate wafer) with (fin pillar column mast post shaft pilaster connade castellated) with (epi epitax\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:35
L64	154720	(fin pillar column mast post shaft pilaster connade castellated) with ((side adj wall) side\$1wall)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:35
L65	388	L62 and L63 and L64	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:35
L66	294	L65 not (L52 L55 L61)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:35
L67	6476	(fin pillar column mast post shaft pilaster connade castellated) with (epi epitax\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:39
L68	766	L62 and L67 and L64	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:39
L69	323	L68 not (L52 L55 L61 L66)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:39
L70	976	(H01L21/823431).cpc.	US-PGPUB;	OR	ON	2014/10/21

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:42
L71	218	L67 and L70	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:42
L72	124	L71 not (L52 L55 L61 L66 L69)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:42
L73	0	("2014/0264616").URPN.	USPAT	OR	ON	2014/10/21 12:43
L74	27392	438/197,275.ccls. 257/288,289,368,401,618,623,E21.618,E21.619,E21.633.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:47
L75	360	L74 and L49 and L50 and L51	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 12:47
L76	78	L75 not (L52 L55 L61 L66 L69 L72)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 12:47
L78	179	(bachner near2 robert)	USPAT	OR	ON	2014/10/21 14:30
L79	104	((Chin-Fu) near2 (Lin)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 14:37
L80	150	((Chin-Cheng) near2 (Chien)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 14:37
L81	65	((Chun-Yuan) near2 (Wu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 14:37
L82	186	((Teng-Chun) near2 (Tsai)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 14:37
L83	144	((Chih-Chien) near2 (Liu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/10/21 14:37
L84	7	((Chin-Fu) near2 (Lin)).INV.	EPO; JPO; DERWENT	OR	ON	2014/10/21 14:37
L85	5	((Chin-Cheng) near2 (Chien)).INV.	EPO; JPO; DERWENT	OR	ON	2014/10/21 14:38
L86	0	((Chun-Yuan) near2 (Wu)).INV.	EPO; JPO;	OR	ON	2014/10/21

			DERWENT			14:38
L87	1	((Teng-Chun) near2 (Tsai)).INV.	EPO; JPO; DERWENT	OR	ON	2014/10/21 14:38
L88	0	((Chih-Chien) near2 (Liu)).INV.	EPO; JPO; DERWENT	OR	ON	2014/10/21 14:38
L89	498	79 80 81 82 83 84 85 86 87 88	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 14:38
L90	35	89 and (fin finfet) and (epi epitax\$6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/10/21 14:40

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Receipt date: 07/24/2014

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

14340267 - GALL:2816

Approved for use through 07/31/2012. OMB 0651-0031

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	Filing Date		
	First Named Inventor	Chin-Fu Lin	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	JCLA40585-D	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7888192		2011-02-15	Marshall, et al.	
	2	6492216		2002-12-10	Yeo, et al.	
	3	6921963		2005-07-26	Krivokapic, et al.	
	4	7087477		2006-08-08	Fried, et al.	
	5	7247887		2007-07-24	King, et al.	
	6	7250658		2007-07-31	Doris, et al.	
	7	7309626		2007-12-18	leong, et al.	
	8	7470570		2008-12-30	Beintner, et al.	

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			First Named Inventor		Chin-Fu Lin	
			Art Unit			
			Examiner Name			
			Attorney Docket Number		JCLA40585-D	

	9	7531437		2009-05-12	Brask, et al.	
	10	7569857		2009-08-04	Simon, legal representative, et al.	
	11	6043138		2000-03-28	Ibok	
	12	7091551		2006-08-15	Anderson, et al.	
	13	7352034		2008-04-01	Booth, Jr., et al.	
	14	6500725		2002-12-31	Chen , et al.	

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	1	20050051825		2005-03-10	Fujiwara, Makoto; et al.	
	2	20060286729		2006-12-21	Kavalieros; Jack; et al.	
	3	20070108528		2007-05-17	Anderson; Brent A.; et al.	

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			Art Unit		
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			Attorney Docket Number	JCLA40585-D	

	4	20070158756		2007-07-12	Dreeskomfeld; Lars; et al.	
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			Art Unit			
			Examiner Name			
			Attorney Docket Number		JCLA40585-D	

	15	20120043597		2012-02-23	Chen; Howard H. ; et al.	
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	1	SANCHEZ ET AL., "Low-Temperature Growth of Epitaxial Beta-SiC on Si(100) Using Supersonic Molecular Beams of Methylsilane," J. Phys. Chem. B., July 2002, pp. 8019-8028.	☒
	2	"Archived wikipedia entry of Silicon," Wikipedia, July 2013, pp. 1-9.	☒
	3	"Archived wikipedia entry of Silicon carbide," Wikipedia, July 2013, pp. 1-8.	☒
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	First Named Inventor	Chin-Fu Lin	
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/JIAWEI HUANG/	Date (YYYY-MM-DD)	2014-07-24
Name/Print	JIAWEI HUANG	Registration Number	43330

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/340,267	07/24/2014	Chin-Fu Lin	JCLA40585-D

CONFIRMATION NO. 8893

PUBLICATION NOTICE

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J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618



OC000000071832642

Title: SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

Publication No. US-2014-0332824-A1

Publication Date: 11/13/2014

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: Reida, Molly Kay

Group Art Unit: 2816

In re PATENT APPLICATION of

Applicants : Lin, Chin-Fu et al.

Serial No. : 14/340,267

Filed : July 24, 2014

For : SEMICONDUCTOR STRUCTURE WITH
DIFFERENT FINS OF FINFETS

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AMENDMENT

It is believed no fee is due. However, the Commissioner is authorized to charge any fees required, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 50-0710 (Order No. JCLA40585-D). Signature: /JIAWEI HUANG/
Jiawei Huang, Reg. No. 43,330

AMENDMENT AND RESPONSE TO OFFICE ACTION

Mail Stop AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Office Action mailed November 4, 2014 has been carefully considered. In response thereto, please consider the following amendment and remarks.

Amendments to the Claims:

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (currently amended) A semiconductor structure for forming FinFETs, comprising

a semiconductor substrate;

a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate; and

a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material.

2. (original) The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

3. (original) The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material.

4. (original) The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

5. (original) The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.

6. (original) The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.

7. (currently amended) A semiconductor structure for forming FinFETs, comprising

a semiconductor substrate;

a plurality of odd fins of the FinFETs on the semiconductor substrate, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and

a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material.

8. (original) The semiconductor structure of claim 7, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

9. (original) The semiconductor structure of claim 7, wherein the even fins of the FinFETs comprise an epitaxy material.

10. (original) The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

11. (original) The semiconductor structure of claim 7, wherein the odd fins of the FinFETs comprise Si.

12. (original) The semiconductor structure of claim 7, wherein the even fins of the FinFETs comprise SiC or SiGe.

13. (currently amended) A semiconductor structure for forming FinFET, comprising

a semiconductor substrate;

a plurality of first fins of the FinFETs on the semiconductor substrate, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and

a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material.

14. (original) The semiconductor structure of claim 13, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.

15. (original) The semiconductor structure of claim 13, wherein the second fins of the FinFETs comprise an epitaxy material.

16. (original) The semiconductor structure of claim 15, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.

17. (original) The semiconductor structure of claim 13, wherein the first fins of the FinFETs comprise Si.

18. (original) The semiconductor structure of claim 13, wherein the second fins of the FinFETs comprise SiC or SiGe.

19. (new) The semiconductor structure of claim 1, wherein the odd fins of the FinFETs are electrically connected to the semiconductor substrate.

20. (new) The semiconductor structure of claim 1, wherein the semiconductor substrate is a single layer structure.

REMARKS

Present Status of the Application

This is a full and timely response to the outstanding non-final Office Action mailed on November 4, 2014. Claims 1-18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by White et al. (US 2008/0020515, hereinafter “White”), or in the alternative, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over White.

In response thereto, Applicants have amended claims 1, 7 and 13, and added new claims 19-20 to more clearly define the claimed invention. The supporting grounds of the amendment are provided at least in paragraphs [0017], [0025]-[0026] of the specification and Figs. 1 and 6. After entry of the foregoing amendments, claims 1-20 remain pending in the present application. It is believed that no new matter is added by way of these amendments made to the claims or otherwise to the application.

Discussion of 35 U.S.C. 102 Rejections and 35 U.S.C. 103 Rejections

Claims 1-18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by White et al. (US 2008/0020515, hereinafter “White”), or in the alternative, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over White.

Every element of the claimed invention must be **literally present, arranged as in the claim**. *Richardson v. Suzuki Motor Co., Ltd.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989).

Claims 1, 7, and 13 are amended to more clearly define the embodiments therein and now respectively read as:

1. A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate;
a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate; and
a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material.

7. A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate;
a plurality of odd fins of the FinFETs on the semiconductor substrate, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and
a plurality of even fins of the FinFETs on the semiconductor

substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material.

13. A semiconductor structure for forming FinFET, comprising a semiconductor substrate;

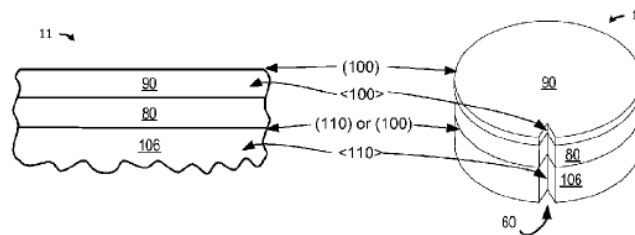
a plurality of first fins of the FinFETs on the semiconductor substrate, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and

a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material.

The Examiner alleged that the structure 11 of White is comparable to the claimed semiconductor substrate, and the FinFET device 20 of White, which is located in the device region 97 and formed of material 90, is comparable to the claimed odd fins or the claimed first fins of the FinFETs. Applicants respectfully disagree with the Examiner's assumption.

First, Applicants respectfully point out that the structure 11 of White is in fact **composed of three different layers**, as shown in Fig. 1. Namely, a substrate 106 located at the bottom, a second semiconductor layer 90 located on top of the substrate 106, and an insulator layer 80 located between the second semiconductor layer 90 and the substrate 106. In addition, the material of the insulator layer 80 is different from the material of the substrate 106 and the second semiconductor layer 90, in which the insulator layer 80 and the second semiconductor layer 90 are formed as SOI (semiconductor-on-insulator) layers as described in paragraphs [0027]-[0028]. That is to say, the Examiner erred in asserting the structure 11 of White, which is constructed as a three layer structure, could be comparable to the claimed substrate.

Fig. 1 of White



From the viewpoint of above, Applicants respectfully submit that the technical feature of “a plurality of odd fins of the FinFETs on the semiconductor substrate, **being defined from the semiconductor substrate**” as described in claim 1, the technical feature of “a plurality of

odd fins of the FinFETs on the semiconductor substrate, wherein the plurality of **odd fins and the semiconductor substrate are in direct contact with each other**” as described in claim 7, and the technical feature of “a plurality of first fins of the FinFETs on the semiconductor substrate, wherein the plurality of **first fins and the semiconductor substrate are in direct contact with each other**” as described in claim 13 are not disclosed by White. In one embodiment of the present invention, as shown in Fig. 6, the odd fins 10a are defined from the semiconductor substrate 10, and the odd fins 10a and the semiconductor substrate 10 are in direct contact with each other. On the other hand, according to Figs. 9-10 and paragraphs [0039]-[0040] of White, White teaches an insulator layer 80 located between the substrate 106 and the FinFET device 20, in which the FinFET device 20 is located in the device region 97 and formed of material 90. In other words, the FinFET device 20 of White is not defined from the substrate 106 and not in direct contact with the substrate 106. For at least the above reasons, White fails to disclose every claimed feature as described in claims 1, 7, and 13 of the present invention.

Fig. 6 of the present invention

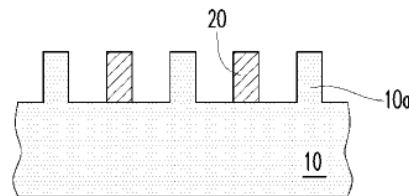


Fig. 9 of White

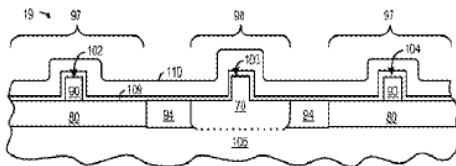
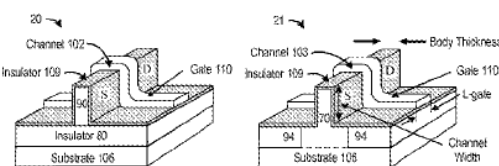


Fig. 10 of White



In view of the above, the technical feature of claim 1 reciting “a plurality of odd fins of the FinFETs on the semiconductor substrate, **being defined from the semiconductor substrate**”, the technical feature of claim 7 reciting “a plurality of odd fins of the FinFETs on the semiconductor substrate, wherein the plurality of **odd fins and the semiconductor substrate are in direct contact with each other**”, and the technical feature of claim 13 reciting “a plurality of first fins of the FinFETs on the semiconductor substrate, wherein the

plurality of **first fins and the semiconductor substrate are in direct contact with each other**” are not disclosed by White, and it would have not been obvious to one of ordinary skill in the art to arrive at the claimed invention by referring to the teachings of White. Therefore, Applicants respectfully submit that claims 1, 7, and 13 are not anticipated by White, stand non-obvious over the cited reference, and are allowable.

Since the independent claims 1, 7, and 13 are allowable, claims 2-6, 8-12, and 14-20 dependent thereon should also be allowed, as a matter of law for it contains all of the limitations of its independent claim. In re *Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Newly Added Claims

Applicants have added dependent claims 19-20, which are dependent from claim 1 to further narrow the scope as provide for within the disclosure. Therefore, it is submitted that claims 19-20 are in condition for allowance for the above reasons.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: January 20, 2015

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Electronic Acknowledgement Receipt	
EFS ID:	21259812
Application Number:	14340267
International Application Number:	
Confirmation Number:	8893
Title of Invention:	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS
First Named Inventor/Applicant Name:	Chin-Fu Lin
Customer Number:	23900
Filer:	Jiawei Huang/Michelle Chang
Filer Authorized By:	Jiawei Huang
Attorney Docket Number:	JCLA40585-D
Receipt Date:	20-JAN-2015
Filing Date:	24-JUL-2014
Time Stamp:	22:20:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	40585-D_1st_Response.pdf	117774 12b48ebfa44e000e149f65cc4c68c1ec4a7b48ca	no	7

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 14/340,267		Filing Date 07/24/2014		☐ To be Mailed	
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)					
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A			N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$	=	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$	=	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL		

APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT	01/20/2015	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(b))	* 3	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=
	Independent (37 CFR 1.16(b))	*	Minus	***	=	X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/340,267	07/24/2014	Chin-Fu Lin	JCLA40585-D	8893

23900 7590 04/24/2015
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER
REIDA, MOLLY KAY

ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
04/24/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 14/340,267	Applicant(s) LIN ET AL.	
	Examiner MOLLY REIDA	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04/08/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-20 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____ | 4) ☐ Other: _____ |

DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by White et al. (US Pub. 2008/0020515), or in the alternative, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over White et al. (US Pub. 2008/0020515).

Regarding independent claim 1, White teaches a semiconductor structure (Fig. 9) for forming FinFETs, comprising

a semiconductor substrate (11, para. 0027);

a plurality of odd fins of the FinFETs (in region 97, formed of material 90) on the semiconductor substrate, being defined from the semiconductor substrate; and

a plurality of even fins (in region 98, formed of material 70) of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width (para. 0040) and material (para. 0028, 0033).

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The embodiment disclosed by White does not explicitly show a plurality of even fins; however, the pattern disclosed by White was the minimum structure needed to understand the invention and it is standard in the semiconductor art to continue a base pattern (for example continuing the pattern of Fig. 9 to the left and/or right of the pattern disclosed); thus a plurality of even fins is considered to be anticipated, or at the very least obvious to one of ordinary skill in the art over the disclosure of white (refer also to para 0025-0026).

Regarding independent claim 7, White teaches a semiconductor structure (Fig. 9) for forming FinFETs, comprising

a semiconductor substrate (11, para. 0027);

a plurality of odd fins (in region 97, formed of material 90) of the FinFETs on the semiconductor substrate, wherein the plurality of odd fins and the semiconductor substrate are in direct in direct contact with each other; and

a plurality of even fins (in region 98, formed of material 70) of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width (para. 0040) and material (para. 0028, 0033).

The embodiment disclosed by White does not explicitly show a plurality of even fins; however, the pattern disclosed by White was the minimum structure needed to understand the invention and it is standard in the semiconductor art to continue a base pattern (for example continuing the pattern of Fig. 9 to the left and/or right of the pattern disclosed); thus a plurality of even fins is considered to be anticipated, or at the very least obvious to one of ordinary skill in the art over the disclosure of white (refer also to para 0025-0026).

Regarding dependent claims 2 and 8, White teaches wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height (para. 0040).

Regarding dependent claims 3 and 9, White teaches wherein the even fins of the FinFETs comprise an epitaxy material (para. 0033).

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Regarding dependent claims 4 and 10, White teaches wherein the odd fins of the FinFETs comprise Si (para. 0028) and the even fins of the FinFETs comprise SiC or SiGe (para. 0033).

Regarding dependent claims 5 and 11, White teaches wherein the odd fins of the FinFETs comprise Si (para. 0028).

Regarding dependent claims 6 and 12, White teaches wherein the even fins of the FinFETs comprise SiC or SiGe (para. 0033).

Regarding independent claim 13, White teaches a semiconductor structure (Fig. 9) for forming FinFET, comprising

a semiconductor substrate (106, para. 0027);

a plurality of first fins (in region 97, formed of material 90) of the FinFETs on the semiconductor substrate, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and

a plurality of second fins (in region 98, formed of material 70) of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width (para. 0040) and material (para. 0028, 0033).

The embodiment disclosed by White does not explicitly show a plurality of second fins; however, the pattern disclosed by White was the minimum structure needed to understand the invention and it is standard in the semiconductor art to continue a base pattern (for example continuing the pattern of Fig. 9 to the left and/or right of the pattern disclosed); thus a plurality of even fins is considered to be anticipated, or at the very least obvious to one of ordinary skill in the art over the disclosure of white (refer also to para 0025-0026).

Regarding dependent claim 14, White teaches wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height (para. 0040).

Regarding dependent claim 15, White teaches wherein the second fins of the FinFETs comprise an epitaxy material (para. 0033).

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Regarding dependent claim 16, White teaches wherein the first fins of the FinFETs comprise Si (para. 0028) and the second fins of the FinFETs comprise SiC or SiGe (para. 0033).

Regarding dependent claim 17, White teaches wherein the first fins of the FinFETs comprise Si (para. 0028).

Regarding dependent claim 18, White teaches wherein the second fins of the FinFETs comprise SiC or SiGe (para. 0033).

Response to Arguments

Applicant's arguments filed Jan 30, 2015 have been fully considered but they are not persuasive.

Applicant argues that the technical features of "a plurality of odd fins of the FinFETs on the semiconductor substrate, **being defined from the semiconductor substrate**", as described in claim 1; "a plurality of odd fins of the FinFETs on the semiconductor substrate, wherein the plurality of **odd fins and the semiconductor substrate are in direct contact with each other**", as described in claim 7; and "a plurality of first fins of the FinFETs on the semiconductor substrate, wherein the plurality of **first fins and the semiconductor substrate are in direct contact with each other**", as described in claim 13 are not disclosed by White.

Applicant's arguments are based upon differences in interpretation of "semiconductor substrate"; the Applicant arguing that because the disclosed substrate of White includes an insulating layer; that is the substrate of White is a SOI (semiconductor-on-insulator) layer, that it cannot read on the claimed "semiconductor substrate".

This argument is unpersuasive because broadly speaking, an SOI substrate may be considered a "semiconductor substrate" in that it both contains semiconductor materials and is used to form semiconductor devices. The claims are interpreted according to the guidelines provided by MPEP 2111; that is, claims are given its broadest reasonable interpretation and while claims are read in light of the specification, limitations from the specification are not imported into the claims. Thus reading an SOI

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substrate as a "semiconductor substrate" is acceptable under the guidelines provided by MPEP 2111 and in the properly made rejection above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOLLY REIDA whose telephone number is (571)272-4237. The examiner can normally be reached on Mon-Fri 8:30-5:00 (approx).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571)272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative

Application/Control Number: 14/340,267

Page 7

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or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOLLY REIDA/
Examiner, Art Unit 2816

/ZANDRA SMITH/
Supervisory Patent Examiner, Art Unit 2816

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L44	2	"13595232"	US-PGPUB; USPAT	OR	ON	2015/04/08 09:56
L45	9	("20060048697" "20060214226" "20060292770" "20080048269" "20110147842" "20120146101" "7208815" "7667271" "8053299").PN. OR ("8963206").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2015/04/08 09:56
L46	2	("2014/0054650").URPN.	USPAT	OR	ON	2015/04/08 09:57
L47	115	((Chin-Fu) near2 (Lin)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/04/08 09:59
L48	162	((Chin-Cheng) near2 (Chien)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/04/08 09:59
L49	73	((Chun-Yuan) near2 (Wu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/04/08 09:59
L50	195	((Teng-Chun) near2 (Tsai)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/04/08 09:59
L51	158	((Chih-Chien) near2 (Liu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/04/08 09:59
L52	7	((Chin-Fu) near2 (Lin)).INV.	EPO; JPO; DERWENT	OR	ON	2015/04/08 09:59
L53	5	((Chin-Cheng) near2 (Chien)).INV.	EPO; JPO; DERWENT	OR	ON	2015/04/08 09:59
L54	0	((Chun-Yuan) near2 (Wu)).INV.	EPO; JPO; DERWENT	OR	ON	2015/04/08 09:59
L55	1	((Teng-Chun) near2 (Tsai)).INV.	EPO; JPO; DERWENT	OR	ON	2015/04/08 09:59
L56	0	((Chih-Chien) near2 (Liu)).INV.	EPO; JPO; DERWENT	OR	ON	2015/04/08 09:59
L57	534	L47 L48 L49 L50 L51 L52 L53 L54 L55 L56	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 09:59
L58	1356	(H01L21/823431).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 10:28

EAST Search History

L61	9454	(fin pillar column mast post shaft pilaster colonnade castellated) with (epi epitax\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 10:34
L62	356	58 and 61	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 10:35
L63	14618	(H01L27/0886 H01L27/0924 H01L29/41791 H01L29/66795 H01L29/6675 H01L29/6681 H01L29/66818 H01L29/785 H01L29/7851 H01L29/7853 H01L29/7854 H01L29/7855).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 11:01
L64	1858	(63 and 61) not 62	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 11:01
L65	14542	(fin\$1fet\$1 finfet) (tri\$1gate\$1 trigate) ("3"\$1D\$4fet\$1) ("3"\$1dimentional near2 (fet mosfet)) (three\$1dimentional near2 (fet mosfet))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 12:38
L66	607	(65 and 61) not (62 64)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/08 12:39

EAST Search History (Interference)

< This search history is empty >

4/ 8/ 2015 3:38:36 PM**C:\Users\mreida\Documents\EAST\Workspaces\14340267.wsp**

Search Notes 	Application/Control No. 14340267	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner MOLLY REIDA	Art Unit 2816

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/0886, H01L29/66795, H01L29/785, H01L29/7851, H01L29/7855, H01L29/7856, H01L2029/785 H012029/7858, H01L21/823431, combined with text search,	10/21/2014	mkr

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	288,289,368,401,618,623,E21.618,E21.619,E21.633, combined with text search	10/21/2014	mkr
438	151,154,197,275, combined with text search	10/21/2014	mkr

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Text Search	10/21/2014	mkr
Inventor(s)	10/21/2014	mkr
Updated EAST Search	04/08/2015	mkr

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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PATENT

Request For Continued Examination (RCE) Transmittal Address to: Commissioner for Patents Box RCE P.O. Box 1450, Alexandria, VA 22313-1450 Fax no.: 571-273-8300	Application No. :	14/340,267
	Filing Date :	July 24, 2014
	First Named Inventor :	CHIN-FU LIN
	Group Art Unit :	2816
	Examiner :	REIDA, MOLLY KAY
	Attorney Docket No. :	JCLA40585-DR

This is a **Request for Continued Examination (RCE)** under 37 C.F.R. 1.114 of the above-identified application.

1. Submission required under 37 CFR § 1.114.

a. ☐ **Previously submitted**

() Consider the amendment(s)/reply under 37 CFR 1.116 previously filed on _____

() Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

b. ☒ **Enclosed**

(X) Amendment and Response under 37 CFR 1.114 in (8) pages.

() Other _____

2. Miscellaneous

a. () Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months.

b. () Associate Power of Attorney.

3. Fees are calculated as follows:

CLAIMS AS FILED							
NUMBER FILED		HIGHEST NO. PREVIOUSLY PAID FOR		PRESENT EXTRA	RATE	ADDITIONAL FEE	
Basic Filing Fee					\$ 1200	\$ 1200	
Total Claims	20	MINUS	20	= 0	x \$ 80	= \$ 0	
Independent Claims	3	MINUS	3	= 0	x \$ 420	= \$ 0	
[] month(s) extension of time is hereby requested.					Time Extension Fee	= \$ 0	
Total:						\$ 1200	

a. [] Check in the amount of \$ ___ enclosed

JCLA40585-DR

PATENT

b. [☒] The Commissioner is hereby authorized to charge the filing fee in the amount of \$ 1200 as calculated above and any additional fee required in connection with filing of this application, or credit any overpayments, to Deposit Account No. 50-0710 (Order No. JCLA40585-DR).

- i. (☒) RCE fee required under 37 CFR 1.17(e)
- ii. (☐) Extension of time fee (37 CFR 1.136 and 1.17).

Date: July 16, 2015

/JIAWEI HUANG/

Jiawei Huang

Registration No. 43,330

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Irvine, CA. 92618

Tel.: (949) 660-0761

Fax: (949)-660-0809

JCLA40585-DR

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: Reida, Molly Kay

Group Art Unit: 2816

In re PATENT APPLICATION of

Applicants : United Microelectronics Corp.

Serial No. : 14/340,267

Filed : July 24, 2014

For : SEMICONDUCTOR STRUCTURE WITH
DIFFERENT FINS OF FINFETS

$$\begin{pmatrix} \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \end{pmatrix}$$

AMENDMENT

AMENDMENT AND RESPONSE UNDER 37 CFR 1.114

Mail Stop AF

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

This Request for Continued Examination under 37 C.F.R. 1.114 and the amendment under 37 CFR 1.114 are filed in reply to the Office Action mailed April 24, 2015. In response thereto, please enter the following amendment and consider the following remarks.

Amendments to the Claims:

Please amend the claims according to the following listing of claims and substitute it for all prior versions and listings of claims in the application.

1. (Currently amended) A semiconductor structure for forming FinFETs, comprising

a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate; and

a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

2. (Original) The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

3. (Original) The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material.

4. (Original) The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

5. (Original) The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.

6. (Original) The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.

7. (Currently amended) A semiconductor structure for forming FinFETs, comprising

a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

a plurality of odd fins of the FinFETs on the semiconductor substrate, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and

a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width

and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

8. (Original) The semiconductor structure of claim 7, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

9. (Original) The semiconductor structure of claim 7, wherein the even fins of the FinFETs comprise an epitaxy material.

10. (Original) The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

11. (Original) The semiconductor structure of claim 7, wherein the odd fins of the FinFETs comprise Si.

12. (Original) The semiconductor structure of claim 7, wherein the even fins of the FinFETs comprise SiC or SiGe.

13. (Currently amended) A semiconductor structure for forming FinFET, comprising

a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

a plurality of first fins of the FinFETs on the semiconductor substrate, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and

a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.

14. (Original) The semiconductor structure of claim 13, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.

15. (Original) The semiconductor structure of claim 13, wherein the second fins of the FinFETs comprise an epitaxy material.

16. (Original) The semiconductor structure of claim 15, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.

17. (Original) The semiconductor structure of claim 13, wherein the first fins of the FinFETs comprise Si.

18. (Original) The semiconductor structure of claim 13, wherein the second fins of the FinFETs comprise SiC or SiGe.

19. (Previously presented) The semiconductor structure of claim 1, wherein the odd fins of the FinFETs are electrically connected to the semiconductor substrate.

20. (Previously presented) The semiconductor structure of claim 1, wherein the semiconductor substrate is a single layer structure.

REMARKS

Present Status of the Application

This is a full and timely response to the outstanding final Office Action mailed on April 24, 2015. Claims 1-18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by White et al. (US 2008/0020515, hereinafter “White”), or in the alternative, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over White.

In response thereto, Applicants have amended claims 1, 7 and 13 to more clearly define the claimed invention. The supporting grounds of the amendment are provided at least in paragraphs [0017], [0022]-[0026] of the specification and Figs. 1, 5-6. After entry of the foregoing amendments, claims 1-20 remain pending in the present application. It is believed that no new matter is added by way of these amendments made to the claims or otherwise to the application.

Discussion of 35 U.S.C. 102 Rejections and 35 U.S.C. 103 Rejections

Claims 1-18 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by White et al. (US 2008/0020515, hereinafter “White”), or in the alternative, are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over White.

Claims 1, 7, and 13 are amended to more clearly define the embodiments therein and now respectively read as:

1. A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate, **wherein a top portion of the semiconductor substrate comprises a semiconductor material;**
a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate; and
a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, **wherein the plurality of even fins are in direct contact with the semiconductor material.**

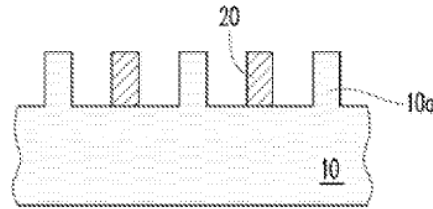
7. A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate, **wherein a top portion of the semiconductor substrate comprises a semiconductor material;**
a plurality of odd fins of the FinFETs on the semiconductor substrate, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and

a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, **wherein the plurality of even fins are in direct contact with the semiconductor material.**

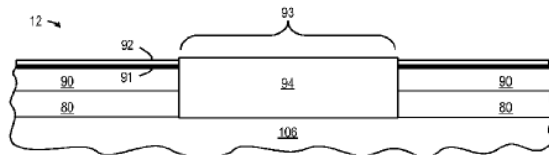
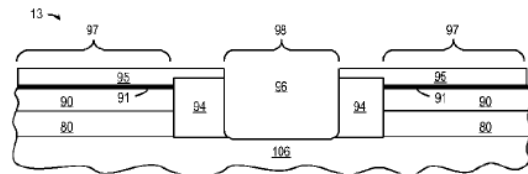
13. A semiconductor structure for forming FinFET, comprising
a semiconductor substrate, **wherein a top portion of the semiconductor substrate comprises a semiconductor material;**
a plurality of first fins of the FinFETs on the semiconductor substrate, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and
a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, **wherein the plurality of second fins are in direct contact with the semiconductor material.**

The Examiner alleged that the structure 11 of White is comparable to the claimed semiconductor substrate; the FinFET device 20 of White, which is located in the device region 97 and formed of material 90, is comparable to the claimed odd fins or the claimed first fins of the FinFETs; and the FinFET device 21 of White, which is located in the device region 98 and formed of material 70, is comparable to the claimed even fins or the claimed second fins of the FinFETs. The Examiner further asserted that the structure 11 comprising insulator layer 80 could be broadly interpreted as a semiconductor substrate. Applicants respectfully disagree with the Examiner's assumption.

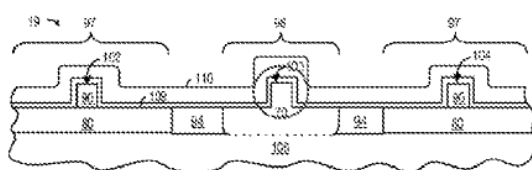
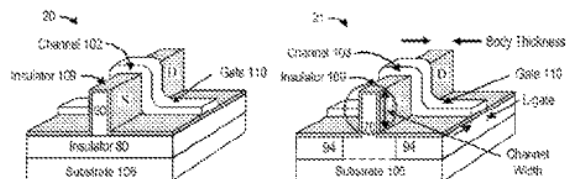
Claims 1, 7, and 13, after amended, claims that “**wherein a top portion of the semiconductor substrate comprises a semiconductor material**”, and “**wherein the plurality of even/second fins are in direct contact with the semiconductor material**”. In one embodiment of the present invention, as shown in Fig. 6, the top portion of the semiconductor substrate 10 contains semiconductor material, the odd fins 10a and the semiconductor material of the semiconductor substrate 10 are in direct contact with each other and the even fins 20 are in direct contact with the semiconductor material of the semiconductor substrate 10.

Fig. 6 of the present invention

White fails to disclose the above technical features. According to Figs. 1-8 of White, the structure 11 is etched to form an opening 93, and an oxide layer 94 is filled in the opening 93. Thereafter, a second etch opening 96 is formed in the oxide layer 94, and a semiconductor layer 70 is formed in the opening 96. Clearly, the semiconductor layer 70 of White is not part of the structure 11.

Fig. 1 of White**Fig. 2 of White**

Further, according to Figs. 9-10 of White, the top portion of the structure 11 is an insulator layer 80 instead of a semiconductor layer (material). In addition, as known in the art, the “fin structure” is defined as a protrusion rises above the top surface of the substrate. In this regard, since the semiconductor layer 70 of White is not part of the structure 11 (with layers 80/90/106, [0027]-[0033]), the protrusion (fin) part of the semiconductor layer 70 of White, as marked in red circle, does not directly contact with the semiconductor material of the substrate 106.

Fig. 9 of White**Fig. 10 of White**

In other words, the technical features of “**wherein a top portion of the semiconductor substrate comprises a semiconductor material**” and “**wherein the plurality of even/second fins are in direct contact with the semiconductor material**” of the present invention are not disclosed by White.

In view of the above, the technical features of claims 1, 7, and 13 reciting “**wherein a top portion of the semiconductor substrate comprises a semiconductor material**” and “**wherein the plurality of even/second fins are in direct contact with the semiconductor material**” are not disclosed by White, and would have not been obvious to one of ordinary skill in the art to arrive at the claimed invention by referring to the teachings of White. Therefore, Applicants respectfully submit that claims 1, 7, and 13 are not anticipated by White, stand non-obvious over the cited reference, and are allowable.

Since the independent claims 1, 7, and 13 are allowable, claims 2-6, 8-12, and 14-20 dependent thereon should also be allowed, as a matter of law for it contains all of the limitations of its independent claim. In re *Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-20 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: July 16, 2015

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Fax: (949)-660-0809

/JIAWEI HUANG/
Jiawei Huang
Registration No. 43,330
Email: jcpi@msn.com

Electronic Patent Application Fee Transmittal				
Application Number:		14340267		
Filing Date:		24-Jul-2014		
Title of Invention:		SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		
First Named Inventor/Applicant Name:		Chin-Fu Lin		
Filer:		Jiawei Huang/Michelle Chang		
Attorney Docket Number:		JCLA40585-D		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	22944097
Application Number:	14340267
International Application Number:	
Confirmation Number:	8893
Title of Invention:	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS
First Named Inventor/Applicant Name:	Chin-Fu Lin
Customer Number:	23900
Filer:	Jiawei Huang/Michelle Chang
Filer Authorized By:	Jiawei Huang
Attorney Docket Number:	JCLA40585-D
Receipt Date:	16-JUL-2015
Filing Date:	24-JUL-2014
Time Stamp:	20:36:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1200
RAM confirmation Number	6443
Deposit Account	500710
Authorized User	HUANG, JIAWEI
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	
Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	40585-DR_RCE_Transmittal_Sheet.pdf	26664	no	2
			dce526957afbc044be3724f239058d34c87bd7c4		
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	40585-DR_RCE_Amend.pdf	230647	no	8
			ec57aaf3e885f3695a6c29da006e1e45fa865070		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30459	no	2
			f9b543d47640080eb31e2c22db547613024702eb		
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<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 14/340,267		Filing Date 07/24/2014		☐ To be Mailed	
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)					
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A			N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$	=	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$	=	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL			

APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			

AMENDMENT	07/16/2015	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$80 =	0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$420 =	0	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
						TOTAL ADD'L FEE		0

(Column 1)		(Column 2)		(Column 3)			
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AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
						TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ZURIASHWORK ZENEBE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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NOTICE OF ALLOWANCE AND FEE(S) DUE

23900 7590 09/11/2015
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER

REIDA, MOLLY KAY

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 09/11/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/340,267	07/24/2014	Chin-Fu Lin	JCLA40585-D	8893

TITLE OF INVENTION: SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/11/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23900 7590 09/11/2015
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4 VENTURE, SUITE 250
IRVINE, CA 92618

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/340,267	07/24/2014	Chin-Fu Lin	JCLA40585-D	8893

TITLE OF INVENTION: SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/11/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDA, MOLLY KAY	2816	257-077000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/340,267	07/24/2014	Chin-Fu Lin	JCLA40585-D	8893

23900 7590 09/11/2015
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER

REIDA, MOLLY KAY

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 09/11/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/340,267	Applicant(s) LIN ET AL.	
	Examiner MOLLY REIDA	Art Unit 2816	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to communications filed 07/16/2015 and interview of 08/28/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☒ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date <u>08/28/2015</u> .	

/MOLLY REIDA/ Examiner, Art Unit 2816	
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DETAILED ACTION

The present application is being examined under the pre-AIA first to invent provisions.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Jiawei Huang (Reg. 43,330) on 08/28/2015.

Claim 1 has been amended as follows:

A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;
a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material; and
a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

Claim 7 has been amended as follows:

A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;
a plurality of odd fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and

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a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

Claim 13 has been amended as follows:

A semiconductor structure for forming FinFET, comprising

a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material:

a plurality of first fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and

a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.

Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claims 1-6, 19 and 20, there is no teaching, suggestion, or motivation for combination from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of "wherein a top portion of the semiconductor substrate comprises a semiconductor material; a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material; and a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material", in combination with the other limitations.

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With respect to claims 7-12, there is no teaching, suggestion, or motivation for combination from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of “wherein a top portion of the semiconductor substrate comprises a semiconductor material; a plurality of odd fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material”, in combination with the other limitations.

With respect to claims 13-18, there is no teaching, suggestion, or motivation for combination from the prior art of record, nor does the prior art of record otherwise make obvious the limitations of “wherein a top portion of the semiconductor substrate comprises a semiconductor material; a plurality of first fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material”, in combination with other limitations.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MOLLY REIDA whose telephone number is (571)272-4237. The examiner can normally be reached on Mon-Fri 8:30-5:00 (approx).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571)272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MOLLY REIDA/
Examiner, Art Unit 2816

/ZANDRA SMITH/
Supervisory Patent Examiner, Art Unit 2816

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	123	((Chin-Fu) near2 (Lin)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/31 08:51
L2	167	((Chin-Cheng) near2 (Chien)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/31 08:51
L3	77	((Chun-Yuan) near2 (Wu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/31 08:51
L4	204	((Teng-Chun) near2 (Tsai)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/31 08:51
L5	165	((Chih-Chien) near2 (Liu)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2015/08/31 08:51
L6	7	((Chin-Fu) near2 (Lin)).INV.	EPO; JPO; DERWENT	OR	ON	2015/08/31 08:51
L7	5	((Chin-Cheng) near2 (Chien)).INV.	EPO; JPO; DERWENT	OR	ON	2015/08/31 08:51
L8	0	((Chun-Yuan) near2 (Wu)).INV.	EPO; JPO; DERWENT	OR	ON	2015/08/31 08:51
L9	1	((Teng-Chun) near2 (Tsai)).INV.	EPO; JPO; DERWENT	OR	ON	2015/08/31 08:51
L10	0	((Chih-Chien) near2 (Liu)).INV.	EPO; JPO; DERWENT	OR	ON	2015/08/31 08:51
L11	561	L1 L2 L3 L4 L5 L6 L7 L8 L9 L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 08:51
L17	1979	(H01L21/823431).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 09:09
L18	10372	(fin pillar column mast post shaft pilaster colonnade castellated) with (epi epitax\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 09:09
L19	565	L17 and L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2015/08/31 09:09

			IBM_TDB			
L20	16954	(H01L27/0886 H01L27/0924 H01L29/41791 H01L29/66795 H01L29/6675 H01L29/6681 H01L29/66818 H01L29/785 H01L29/7851 H01L29/7853 H01L29/7854 H01L29/7855) .cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 09:57
L21	2254	(L20 and L18) not L19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 09:57
L22	16333	(fin\$1fet\$1 finfet) (tri\$1gate\$1 trigate) ("3"\$1D\$4fet\$1) ("3"\$1dimentional near2 (fet mosfet)) (three\$1dimentional near2 (fet mosfet))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 09:59
L23	646	(L22 and L18) not (L19 L21)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/08/31 09:59

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	0	((Chin-Fu) near2 (Lin)).INV.	UPAD	OR	ON	2015/08/31 09:07
L13	0	((Chin-Cheng) near2 (Chien)).INV.	UPAD	OR	ON	2015/08/31 09:07
L14	0	((Chun-Yuan) near2 (Wu)).INV.	UPAD	OR	ON	2015/08/31 09:08
L15	1	((Teng-Chun) near2 (Tsai)).INV.	UPAD	OR	ON	2015/08/31 09:08
L16	0	((Chih-Chien) near2 (Liu)).INV.	UPAD	OR	ON	2015/08/31 09:08
L24	5	(fin pillar column mast post shaft pilaster colonnade castellated) with (epi epitax\$5)	UPAD	OR	ON	2015/08/31 11:41
L25	5	(fin\$1fet\$1 finfet) (tri\$1gate\$1 trigate) ("3"\$1D\$4fet\$1) ("3"\$1dimentional near2 (fet mosfet)) (three\$1dimentional near2 (fet mosfet))	UPAD	OR	ON	2015/08/31 11:41
L26	9	24 25	UPAD	OR	ON	2015/08/31 11:41

8/ 31/ 2015 11:44:08 AM

C:\Users\mreida\Documents\EAST\Workspaces\14340267.wsp

Issue Classification 	Application/Control No. 14340267	Applicant(s)/Patent Under Reexamination LIN ET AL.	
	Examiner MOLLY REIDA	Art Unit 2816	

CPC					
Symbol				Type	Version
H01L		29	785	F	2013-01-01
H01L		21	823437	I	2013-01-01
H01L		27	10879	I	2013-01-01
H01L		29	66795	I	2013-01-01
H01L		21	764	I	2013-01-01
H01L		29	165	I	2013-01-01
H01L		21	823431	I	2013-01-01
H01L		21	31111	I	2013-01-01
H01L		21	02381	A	2013-01-01
H01L		21	02532	A	2013-01-01
H01L		21	02636	A	2013-01-01
H01L		21	31116	A	2013-01-01
H01L		21	3115	A	2013-01-01
H01L		21	3141	A	2013-01-01
H01L		21	3185	A	2013-01-01
H01L		27	0886	I	2013-01-01
H01L		29	1095	I	2013-01-01
H01L		29	1608	I	2013-01-01
H01L		29	161	I	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

/MOLLY REIDA/ Examiner.Art Unit 2816 (Assistant Examiner)	08/31/2015 (Date)	Total Claims Allowed: 20	
/ZANDRA SMITH/ Supervisory Patent Examiner.Art Unit 2816 (Primary Examiner)	09/04/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

Issue Classification 	Application/Control No. 14340267	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner MOLLY REIDA	Art Unit 2816

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION										
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED					
						H	0	1	L	29 / 04 (2006.01.01)						
CROSS REFERENCE(S)						H	0	1	L	29 / 76 (2006.0)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															

/MOLLY REIDA/ Examiner.Art Unit 2816 (Assistant Examiner)	08/31/2015 (Date)	Total Claims Allowed: 20	
/ZANDRA SMITH/ Supervisory Patent Examiner.Art Unit 2816 (Primary Examiner)	09/04/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

Issue Classification 	Application/Control No. 14340267	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner MOLLY REIDA	Art Unit 2816

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	15												
2	2	18	16												
3	3	19	17												
4	4	20	18												
5	5														
6	6														
7	18														
8	20														
9	7														
10	8														
11	9														
12	10														
13	11														
14	12														
15	13														
16	14														

/MOLLY REIDA/ Examiner.Art Unit 2816 (Assistant Examiner)	08/31/2015 (Date)	Total Claims Allowed: 20	
/ZANDRA SMITH/ Supervisory Patent Examiner.Art Unit 2816 (Primary Examiner)	09/04/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

Search Notes 	Application/Control No. 14340267	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner MOLLY REIDA	Art Unit 2816

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/0886, H01L29/66795, H01L29/785, H01L29/7851, H01L29/7855, H01L29/7856, H01L2029/785 H012029/7858, H01L21/823431, combined with text search,	10/21/2014	mkr

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	288,289,368,401,618,623,E21.618,E21.619,E21.633, combined with text search	10/21/2014	mkr
438	151,154,197,275, combined with text search	10/21/2014	mkr

SEARCH NOTES		
Search Notes	Date	Examiner
EAST Text Search	10/21/2014	mkr
Inventor(s)	10/21/2014	mkr
Updated EAST Search	04/08/2015	mkr
Updated EAST Search	08/31/2015	mkr

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	Inventor(s)	08/31/2015	mkr
	UPAD Text Search	08/31/2015	mkr

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BIB DATA SHEET

CONFIRMATION NO. 8893

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/340,267	07/24/2014	257	2816	JCLA40585-D		
RULE						
APPLICANTS United Microelectronics Corp., Hsinchu, TAIWAN; INVENTORS Chin-Fu Lin, Tainan City, TAIWAN; Chin-Cheng Chien, Tainan City, TAIWAN; Chun-Yuan Wu, Yunlin County, TAIWAN; Teng-Chun Tsai, Tainan City, TAIWAN; Chih-Chien Liu, Taipei City, TAIWAN; ** CONTINUING DATA ***** This application is a DIV of 13/370,231 02/09/2012 PAT 8822284 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/01/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/MOLLY KAY REIDA/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
			TAIWAN	2	18	3
ADDRESS						
J C PATENTS 4 VENTURE, SUITE 250 IRVINE, CA 92618 UNITED STATES						
TITLE						
SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS						
FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		
1600						

<i>Index of Claims</i> 	Application/Control No. 14340267	Applicant(s)/Patent Under Reexamination LIN ET AL.
	Examiner MOLLY REIDA	Art Unit 2816

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant										☐ CPA										☐ T.D.										☐ R.1.47									
CLAIM			DATE																																				
Final	Original		08/31/2015																																				
1	1	=																																					
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8	20	=																																					

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23900 7590 09/11/2015
J C PATENTS
4 VENTURE, SUITE 250
IRVINE, CA 92618

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

JIAWEI HUANG	(Depositor's name)
/JIAWEI HUANG/	(Signature)
OCTOBER 08, 2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/340,267	07/24/2014	Chin-Fu Lin	JCLA40585-D	8893

TITLE OF INVENTION: SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/11/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDA, MOLLY KAY	2816	257-077000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 **J.C. PATENTS**
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

United Microelectronics Corp.

Hsinchu, Taiwan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number **50-0710** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /JIAWEI HUANG/ Date 10/08/2015
Typed or printed name JIAWEI HUANG Registration No. 43,330

Electronic Patent Application Fee Transmittal				
Application Number:		14340267		
Filing Date:		24-Jul-2014		
Title of Invention:		SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS		
First Named Inventor/Applicant Name:		Chin-Fu Lin		
Filer:		Jiawei Huang/Michelle Chang		
Attorney Docket Number:		JCLA40585-D		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	23734468
Application Number:	14340267
International Application Number:	
Confirmation Number:	8893
Title of Invention:	SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS
First Named Inventor/Applicant Name:	Chin-Fu Lin
Customer Number:	23900
Filer:	Jiawei Huang/Michelle Chang
Filer Authorized By:	Jiawei Huang
Attorney Docket Number:	JCLA40585-D
Receipt Date:	08-OCT-2015
Filing Date:	24-JUL-2014
Time Stamp:	16:32:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	3328
Deposit Account	500710
Authorized User	HUANG, JIAWEI
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	40585-DR_Issue_Fee.pdf	92414	no	1
			0b079a0084e3a5b7cd11fc658e126abfc0fd88a7		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30438	no	2
			17c1d1b422d67989b9b0725540517829269080e7		

Warnings:

Information:

Total Files Size (in bytes):	122852
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/340,267	11/10/2015	9184292	JCLA40585-D	8893
23900	7590	10/21/2015		
J C PATENTS 4 VENTURE, SUITE 250 IRVINE, CA 92618				

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Chin-Fu Lin, Tainan City, TAIWAN;
United Microelectronics Corp., Hsinchu, TAIWAN;
Chin-Cheng Chien, Tainan City, TAIWAN;
Chun-Yuan Wu, Yunlin County, TAIWAN;
Teng-Chun Tsai, Tainan City, TAIWAN;
Chih-Chien Liu, Taipei City, TAIWAN;

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