

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

LONGITUDE LICENSING LTD., and
MARLIN SEMICONDUCTOR LIMITED

Plaintiffs,

V.

LENOVO GROUP LIMITED, MOTOROLA
(WUHAN) MOBILITY TECHNOLOGIES
COMMUNICATION COMPANY LIMITED,
MOTOROLA MOBILE COMMUNICATION
TECHNOLOGY LTD., ONEPLUS
TECHNOLOGY (SHENZHEN) CO., LTD., and
TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY LIMITED

Defendants.

C.A. No. 2:25-cv-171

JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiffs Longitude Licensing Ltd. and Marlin Semiconductor Limited (collectively, “Plaintiffs”) bring this Complaint for patent infringement (“Complaint”) against Defendants Lenovo Group Limited (“Lenovo Group”), Motorola (Wuhan) Mobility Technologies Communication Company Limited (“Motorola (Wuhan)”), Motorola Mobile Communication Technology LTD. (“Motorola Mobile”) (Lenovo Group, Motorola (Wuhan), and Motorola Mobile, together “Lenovo Defendants”), OnePlus Technology (Shenzhen) Co., Ltd. (“OnePlus”), and Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) (Lenovo, Motorola, OnePlus, and TSMC together, “Defendants”). Plaintiffs allege as follows:

THE PARTIES

1. Plaintiff Longitude Licensing Ltd. (“Longitude”) is an Irish limited liability company and has a principal place of business at Blanchardstown Corporate Park 2, Plaza 255, Suite 2A, Dublin D15 YH6H, Ireland.

2. Plaintiff Marlin Semiconductor Limited (“Marlin Semiconductor”) is an Irish limited liability company and has a principal place of business at Blanchardstown Corporate Park 2, Plaza 255, Suite 2A, Dublin D15 YH6H, Ireland.

3. Marlin Semiconductor is the owner by way of assignment of U.S. Patent No. 7,745,847 (“the ’847 Patent”), attached as Exhibit A, U.S. Patent No. 9,093,473 (“the ’473 Patent”), attached as Exhibit B, U.S. Patent No. 9,147,747 (“the ’747 Patent”), attached as Exhibit C, U.S. Patent No. 9,184,292 (“the ’292 Patent”), attached as Exhibit D, and U.S. Patent No. 9,953,880 (“the ’880 Patent”), attached as Exhibit E. All aforementioned patents are collectively the “Asserted Patents.”

Lenovo

4. Upon information and belief, Lenovo Group Limited (“Lenovo Group”) is a corporation organized and existing under the laws of China, with a principal place of business at 23rd Floor, Lincoln House, Taikoo Place, 979 King's Road, Quarry Bay, Hong Kong S.A.R. of China.

5. On information and belief, Lenovo Group’s subsidiaries include Defendants Motorola Mobile Communication Technology Ltd. and Motorola (Wuhan) Mobility Technologies Communication Company Limited.

6. Upon information and belief, Motorola Mobile Communication Technology Ltd. (“Motorola Mobile”) is a corporation organized and existing under the laws of China, with a principal place of business at Room 203A, Area A, No. 178 Xinfeng Road, Huizhi Space, Torch High-tech Zone, Xiamen, 361006, China. Additionally, Motorola Mobile is a wholly owned subsidiary of Lenovo Group organized and existing under the laws of China.

7. Upon information and belief, Motorola (Wuhan) Mobility Technologies Communication Company Limited (“Motorola (Wuhan)”) is a corporation organized and existing

under the laws of China, with a principal place of business at No. 19, Gaoxin 4th Road, Donghu New Technology Development Zone Wuhan, Hubei, 430205 China. Additionally, Motorola (Wuhan) is a wholly owned subsidiary of Lenovo Group organized and existing under the laws of China.

8. Lenovo Group Limited, Motorola Mobile, and Motorola (Wuhan) (together, “Lenovo Defendants”) engage in business in Texas. Pursuant to § 17.044 of the Texas Civil Practice & Remedies Code, Lenovo Group has designated the Secretary of State as its agent for service of process and may be served with process through the Secretary of State. The Secretary of State may forward service to Lenovo Group at its home office address located at 23rd Floor, Lincoln House, Taikoo Place, 979 King's Road, Quarry Bay, Hong Kong S.A.R. of China. Alternatively, Lenovo Group may be served with process by serving the Registered Agent of its wholly owned subsidiary Lenovo (United States) Inc., at 8001 Development Dr., ATT: Karen Jones, Morrisville, NC 27560-7416.

OnePlus

9. Upon information and belief, Defendant OnePlus Technology (Shenzhen) Co., Ltd. (“OnePlus”) is a corporation organized and existing under the laws of China, with a principal place of business at Tairan 8th Road, Shenzhen, Guangdong 518000, China.

10. OnePlus engages in business in Texas. Pursuant to § 17.044 of the Texas Civil Practice & Remedies Code, TSMC has designated the Secretary of State as its agent for service of process and may be served with process through the Secretary of State. The Secretary of State may forward service to OnePlus at its home office address located at Tairan 8th Road, Shenzhen, Guangdong 518000, China. Alternatively, OnePlus may be served with process by serving the Registered Agent of its wholly owned subsidiary OnePlus USA Corp., Registered Agents Inc., at 5900 Balcones Drive, Suite 100, Austin, TX 78731.

TSMC

11. Upon information and belief, Defendant Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) is a Taiwanese company with a principal place of business at 8, Li Hsin Road 6, Hsinchu Science Park, Hsinchu City 30078, Taiwan, R.O.C.

12. TSMC engages in business in Texas. Pursuant to § 17.044 of the Texas Civil Practice & Remedies Code, TSMC has designated the Secretary of State as its agent for service of process and may be served with process through the Secretary of State. The Secretary of State may forward service to TSMC at its home office address located at 8, Li-Hsin Rd. 6, Hsinchu Science Park, Hsinchu 300-78, Taiwan, R.O.C. Alternatively, TSMC may be served with process by serving the Registered Agent of its wholly owned subsidiary TSMC North America, Steven A. Schulman, at 2851 Junction Avenue, San Jose, CA 95134.

JURISDICTION AND VENUE

13. This is an action for patent infringement under the patent laws of the United States, Title 35 of the United States Code. Accordingly, this Court has subject matter jurisdiction over this action under 28 U.S.C. §§ 1331 and 1338(a).

14. This Court has specific personal jurisdiction over Defendants, at least in part, because Defendants conduct business in this judicial District, including the manufacture, use, sale, offer for sale, and/or importation of products that infringe, or that are made using processes that infringe, the Asserted Patents, and other activities related the design, manufacture, distribution, and/or support of those products and processes.

15. Plaintiffs’ causes of action arise, at least in part, from Defendants’ contacts with and activities in the State of Texas and this judicial District. Upon information and belief, each Defendant has committed acts of infringement within the State of Texas and this judicial District

by, *inter alia*, directly and/or indirectly making, having made, using, selling, offering to sell, and/or importing products that infringe, or that are manufactured using processes that infringe, one or more claims of the Asserted Patents.

16. Defendants have committed acts within this judicial District giving rise to this action, and have established sufficient minimum contacts with the State of Texas such that the exercise of jurisdiction would not offend traditional notions of fair play and substantial justice.

17. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391 and 1400.

Lenovo Defendants

18. Venue in this district is proper under 28 U.S.C. § 1391(c)(3) with respect to Lenovo Group. The subsidiary Lenovo Defendants are not residents in the United States and may be sued in this district, because suits against foreign entities are proper in any judicial District where they are subject to personal jurisdiction. The Lenovo Defendants have committed acts of infringement in this district.

19. This Court has personal jurisdiction over the Lenovo Defendants. The Lenovo Defendants are subject to this Court's specific personal jurisdiction pursuant to due process and/or the Texas Long Arm Statute. Plaintiffs' cause of action arises, at least in part, from the Lenovo Defendants' contacts with and activities in the State of Texas and in this district. Upon information and belief, the Lenovo Defendants have committed act of infringement within the State of Texas and this district by, *inter alia*, making, having made, using, selling, offering to sell, and/or importing products that infringe (or products manufactured using infringing processes) one or more claims of the Asserted Patents, and also by inducing and contributing to such infringement by its subsidiaries, affiliates, retail partners, and customers, including, but not limited to, Best Buy, and end-users of devices sold by its customers, in violation of at least 35 U.S.C. §§ 271(a)-(c) and (g).

20. The Lenovo Defendants have conducted and do conduct business within the State of Texas. The Lenovo Defendants, directly or through corporate relatives, subsidiaries, or intermediaries (including distributors, retailers, and others), ship, distribute, make, have made, use, sell, offer for sale, import, and/or advertise (including by providing interactive web pages) their infringing products (or products manufactured using infringing processes) and/or services in the United States and the Eastern District of Texas and/or contribute to or actively induce their subsidiaries, affiliates, retail partners, and customers to ship, distribute, make, have made, use, offer to sell, sell, import, and/or advertise (including by providing interactive websites) infringing products (or products manufactured using infringing processes) and/or services in the United States and the Eastern District of Texas.

21. The Lenovo Defendants, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), have purposefully and voluntarily placed one or more of their infringing products (or products manufactured using infringing processes) and/or services, as described below, into the stream of commerce with the expectation that those products will be purchased and used by customers and/or consumers in the Eastern District of Texas. These infringing products (or products manufactured using infringing processes) and/or services have been and continue to be made, used, sold, offered for sale, purchased, and/or imported by customers and/or consumers in the Eastern District of Texas. These infringing products, including those incorporated into the Lenovo Yoga Slim 7X laptops, are available at least at Best Buy locations throughout this district, including but not limited to: 422 W Loop 281 STE 100, Longview, TX 75605.

22. On information and belief, the Lenovo Defendants manufacture, have manufactured, sell, offer for sale, and/or import products throughout the State of Texas, including

within this judicial District, and introduce infringing products into the stream of commerce knowing that they would be sold in the State of Texas and this judicial District.

23. On information and belief, the Lenovo Defendants, either themselves and/or through the activities of their subsidiaries, make, have made, use, sell, offer for sale, and/or import throughout the United States, including within this judicial District, products, such as laptops, smartphones, tablets, desktop computers, and personal computers, that infringe (or that are manufactured by processes that infringe) the Asserted Patents. *See* Lenovo Products, available at <https://www.lenovo.com/us/en/pc/> (accessed February 10, 2025); Motorola Phones, available at <https://www.motorola.com/us/en/smartphones/index.html> (accessed February 10, 2025).

24. For example, on information and belief, the Lenovo Defendants make, have made, use, sell, offer for sale, and/or import the Lenovo Yoga Slim 7X laptop, incorporating the Qualcomm Snapdragon X Elite manufactured using TSMC's infringing 4 nm process node; and the Moto G Play smartphone, incorporating the Qualcomm Snapdragon 680 4G manufactured using TSMC's infringing 6 nm process node.

25. The Lenovo Defendants, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), have purposefully and voluntarily placed one or more infringing products (or products manufactured using infringing processes) and/or services, as described below, into the stream of commerce with the expectation that those products will be purchased and used by customers and/or consumers in the Eastern District of Texas. These infringing products (or products manufactured using infringing processes) and/or services have been and continue to be made, used, sold, offered for sale, purchased, and/or imported by customers and/or consumers in the Eastern District of Texas. For example, the Lenovo Defendants sell and offers to sell infringing products through their websites [Lenovo.com](https://www.lenovo.com) and [Motorola.com](https://www.motorola.com)

which are accessible to customers and/or consumers in the Eastern District of Texas and throughout the United States. Further, infringing products, including but not limited to the infringing Lenovo Yoga Slim 7X laptop, incorporating the Qualcomm Snapdragon X Elite processor which is manufactured by TSMC, and Moto G Play smartphone, incorporating the Qualcomm Snapdragon 680 4G processor which is manufactured by TSMC, and are available at least at Best Buy locations throughout this district, including but not limited to: 422 W Loop 281 STE 100, Longview, TX 75605.

26. The Lenovo Defendants are thus subject to personal jurisdiction in this District. *See, e.g., World-Wide Volkswagen Corp. v. Woodson*, 444 U.S. 286, 297–98 (1980) (holding that under the stream of commerce theory, a corporation subjects itself to personal jurisdiction in a forum when it “delivers its products into the stream of commerce with the expectation that they will be purchased by consumers in the forum.”); *Commonwealth Sci. & Indus. Rsch. Org. v. Mediatek Inc.*, No. 6:12-CV-578, 2013 WL 12152471, at *2 (E.D. Tex. Sept. 12, 2013) (finding personal jurisdiction over Taiwanese chipmaker Realtek, which sold semiconductor chips “to foreign distributors outside the United States, which then s[old] the Realtek chips exclusively to foreign module makers and foreign original equipment manufacturers, which then integrate[d] Realtek’s IC chips into products eventually sold worldwide, including in the Eastern District,” including because allegedly “Realtek s[old] the accused products into distribution channels knowing that those products will be sold in the Eastern District of Texas.”); *Largan Precision Co. v. Ability Opto-Elects. Tech. Co.*, No. 4:19-CV-696, 2020 WL 569815, at *7 (E.D. Tex. Feb. 5, 2020) (finding personal jurisdiction over Taiwanese manufacturer of optical lenses then sold to “third-party module integrators,” who sold to “system integrators,” who sold to “original equipment manufacturer[s]....such as HP, who then turn[ed] around and s[old]...to an end customer”

because. . . “the Court has no problem concluding that AOET could have expected that those products [the final products containing its lenses] would be sold in Texas.”); *Viavi Sols. Inc. v. Zhejiang Crystal-Optech Co.*, No. 2:21-CV-00378-JRG, 2022 WL 16856099, at *3 (E.D. Tex. Nov. 10, 2022); *Atlas Glob. Techs. LLC v. TP-Link Techs. Co.*, No. 2:21-CV-430-JRG-RSP, 2022 WL 18584501 (E.D. Tex. Dec. 28, 2022), report and recommendation adopted, No. 221CV00430JRGRSP, 2023 WL 1478451 (E.D. Tex. Feb. 2, 2023); *ICON Health & Fitness, Inc. v. Horizon Fitness, Inc.*, 2009 WL 1025467, *14 (E.D. Tex. Mar. 26, 2009).

27. The Lenovo Defendants have established sufficient minimum contacts with the State of Texas such that the exercise of jurisdiction would not offend traditional notions of fair play and substantial justice.

OnePlus

28. Venue in this district is proper under 28 U.S.C § 1391(c)(3) with respect to OnePlus. OnePlus is not a resident in the United States and may be sued in this District, because suits against foreign entities are proper in any judicial District where they are subject to personal jurisdiction. OnePlus has committed acts of infringement in this District.

29. This Court has personal jurisdiction over OnePlus. OnePlus is subject to this Court’s specific personal jurisdiction pursuant to due process and/or the Texas Long Arm Statute. Plaintiffs’ cause of action arises, at least in part, from OnePlus’s contacts with and activities in the State of Texas and in this district. Upon information and belief, OnePlus has committed act of infringement within the State of Texas and this district by, *inter alia*, making, having made, using, selling, offering to sell, and/or importing products that infringe (or products manufactured using infringing processes) one or more claims of the Asserted Patents, and also by inducing and contributing to such infringement by its subsidiaries, affiliates, retail partners, and customers, including but not limited to Best Buy, and end-users of devices sold by its customers, in violation

of at least 35 U.S.C. §§ 271(a)-(c) and (g).

30. OnePlus has conducted and does conduct business within the State of Texas. OnePlus, directly or through corporate relatives, subsidiaries, or intermediaries (including distributors, retailers, and others), ships, distributes, makes, has made, uses, sells, offers for sale, imports, and/or advertises (including by providing interactive web pages) its infringing products (or products manufactured using infringing processes) and/or services in the United States and the Eastern District of Texas and/or contributes to or actively induces its subsidiaries, affiliates, retail partners, and its customers to ship, distribute, make, have made, use, offer to sell, sell, import, and/or advertise (including by providing interactive websites) infringing products (or products manufactured using infringing processes) and/or services in the United States and the Eastern District of Texas.

31. OnePlus, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has purposefully and voluntarily placed one or more of its infringing products (or products manufactured using infringing processes) and/or services, as described below, into the stream of commerce with the expectation that those products will be purchased and used by customers and/or consumers in the Eastern District of Texas. These infringing products (or products manufactured using infringing processes) and/or services have been and continue to be made, used, sold, offered for sale, purchased, and/or imported by customers and/or consumers in the Eastern District of Texas. These infringing products, including those incorporated into the OnePlus 13, OnePlus 13R, and OnePlus Nord N30 5G smartphones, are available at least at Best Buy locations throughout this district, including but not limited to: 422 W Loop 281 STE 100, Longview, TX 75605.

32. On information and belief, OnePlus manufactures, has manufactured, sells, offers

for sale, and/or imports products throughout the State of Texas, including within this judicial District, and introduces infringing products into the stream of commerce knowing that they would be sold in the State of Texas and this judicial District.

33. On information and belief, OnePlus, either itself and/or through the activities of its subsidiaries, makes, has made, uses, sells, offers for sale, and/or imports throughout the United States, including within this judicial District, products, such as smartphones, tablets, and wearables, that infringe (or that are manufactured by processes that infringe) the Asserted Patents. *See* OnePlus Store, available at <https://www.oneplus.com/us/store> (accessed February 10, 2025).

34. For example, on information and belief, OnePlus makes, has made, uses, sells, offers for sale, and/or imports the OnePlus 13, incorporating the Qualcomm Snapdragon 8 Elite manufactured using TSMC's infringing 3nm process node. On information and belief, OnePlus also makes, has made, uses, sells, offers for sale, and/or imports the OnePlus 13R, incorporating the Qualcomm Snapdragon 8 Gen 3 manufactured using TSMC's infringing 4nm process node. In addition, on information and belief, OnePlus makes, has made, uses, sells, offers for sale, and/or imports the OnePlus Nord N30 5G, incorporating the Qualcomm Snapdragon 695 5G manufactured using TSMC's infringing 6nm process node.

35. OnePlus, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has purposefully and voluntarily placed one or more of its infringing products (or products manufactured using infringing processes) and/or services, as described below, into the stream of commerce with the expectation that those products will be purchased and used by customers and/or consumers in the Eastern District of Texas. These infringing products (or products manufactured using infringing processes) and/or services have been and continue to be made, used, sold, offered for sale, purchased, and/or imported by

customers and/or consumers in the Eastern District of Texas. For example, OnePlus sells and offers to sell infringing products through its website OnePlus.com which is accessible to customers and/or consumers in the Eastern District of Texas and throughout the United States. Further, infringing products, including but not limited to the infringing OnePlus 13, OnePlus 13R, and Nord N30 5G smartphones, incorporating the Qualcomm Snapdragon 8 Elite, Snapdragon 8 Gen 3, and Snapdragon 695 5G processors which are manufactured by TSMC, and is available at least at Best Buy locations throughout this district, including but not limited to: 422 W Loop 281 STE 100, Longview, TX 75605.

36. OnePlus is thus subject to personal jurisdiction in this district. *See, e.g., World-Wide Volkswagen Corp. v. Woodson*, 444 U.S. 286, 297–98 (1980) (holding that under the stream of commerce theory, a corporation subjects itself to personal jurisdiction in a forum when it “delivers its products into the stream of commerce with the expectation that they will be purchased by consumers in the forum.”); *Commonwealth Sci. & Indus. Rsch. Org. v. Mediatek Inc.*, No. 6:12-CV-578, 2013 WL 12152471, at *2 (E.D. Tex. Sept. 12, 2013) (finding personal jurisdiction over Taiwanese chipmaker Realtek, which sold semiconductor chips “to foreign distributors outside the United States, which then s[old] the Realtek chips exclusively to foreign module makers and foreign original equipment manufacturers, which then integrate[d] Realtek’s IC chips into products eventually sold worldwide, including in the Eastern District,” including because allegedly “Realtek s[old] the accused products into distribution channels knowing that those products will be sold in the Eastern District of Texas.”); *Largan Precision Co. v. Ability Opto-Elecs. Tech. Co.*, No. 4:19-CV-696, 2020 WL 569815, at *7 (E.D. Tex. Feb. 5, 2020) (finding personal jurisdiction over Taiwanese manufacturer of optical lenses then sold to “third-party module integrators,” who sold to “system integrators,” who sold to “original equipment manufacturer[s]...such as HP, who then

turn[ed] around and s[old]...to an end customer” because. . .“the Court has no problem concluding that AOET could have expected that those products [the final products containing its lenses] would be sold in Texas.”); *Viavi Sols. Inc. v. Zhejiang Crystal-Optech Co.*, No. 2:21-CV-00378-JRG, 2022 WL 16856099, at *3 (E.D. Tex. Nov. 10, 2022); *Atlas Glob. Techs. LLC v. TP-Link Techs. Co.*, No. 2:21-CV-430-JRG-RSP, 2022 WL 18584501 (E.D. Tex. Dec. 28, 2022), report and recommendation adopted, No. 221CV00430JRGRSP, 2023 WL 1478451 (E.D. Tex. Feb. 2, 2023); *ICON Health & Fitness, Inc. v. Horizon Fitness, Inc.*, 2009 WL 1025467, *14 (E.D. Tex. Mar. 26, 2009).

37. OnePlus has established sufficient minimum contacts with the State of Texas such that the exercise of jurisdiction would not offend traditional notions of fair play and substantial justice.

TSMC

38. Venue in this district is proper under 28 U.S.C § 1391(c)(3) with respect to TSMC. TSMC is not a resident in the United States and may be sued in this District, because suits against foreign entities are proper in any judicial District where they are subject to personal jurisdiction. TSMC has committed acts of infringement in this District.

39. This Court has personal jurisdiction over TSMC. TSMC is subject to this Court’s specific personal jurisdiction pursuant to due process and/or the Texas Long Arm Statute. Plaintiffs’ cause of action arises, at least in part, from TSMC’s contacts with and activities in the State of Texas and in this district. Upon information and belief, TSMC has committed act of infringement within the State of Texas and this district by, *inter alia*, making, having made, using, selling, offering to sell, and/or importing products that infringe (or products manufactured using infringing processes) one or more claims of the Asserted Patents, and also by inducing and contributing to such infringement by its subsidiaries, affiliates, and direct or indirect customers, including, but not

limited to, Qualcomm, Lenovo, OnePlus, and end-users of devices sold by them, in violation of at least 35 U.S.C. §§ 271(a)-(c) and (g). TSMC, for example, partners with electronic design automation (EDA) partners throughout the United States, including within this district, to “win business and stay competitive” using its “Open Innovation Platform.” <https://www.tsmc.com/english/dedicatedFoundry/grandAlliance> (accessed Feb. 13, 2025). Specifically, TSMC’s “EDA Alliance, a key component of TSMC Open Innovation Platform (OIP), reduces design barriers for customer's adoption of TSMC process technologies.” https://www.tsmc.com/english/dedicatedFoundry/oip/eda_alliance (accessed Feb. 13, 2025). “By combining TSMC and EDA Alliance members R&D capability and resource, new generations of EDA solutions are enabled to be compliant to TSMC technology requirements.” *Id.* “Selected EDA Alliance partners work closely with TSMC's design technology teams to address customer design needs through the enablement of new EDA tool features that align with TSMC advanced process development roadmap, as well as the implementation of TSMC's design methodology in Reference Flows.” *Id.* Upon information and belief, TSMC’s induces and contributes to the infringement of its customers by partnering with EDA alliance members on the development and certification of instructions, manuals, and design software, which are provided to TSMC’s customers for the purpose of designing, using, selling, offering for sale, and importing products that use TSMC’s infringing semiconductor manufacturing structures and processes. Among TSMC’s EDA alliance partners is Siemens EDA, which TSMC recognized in 2021 as one of four “OIP Partner[s] of the Year,” along with ANSYS, Cadence Design Systems, and Synopsis, for its work with TSMC on “Joint Development of 4nm Design Infrastructure.” <https://pr.tsmc.com/english/news/2875> (accessed Feb. 13, 2025). Upon information and belief, Siemens EDA is a division of Siemens Industry Software, which has its global corporate office in

this district, located at 5800 Granite Parkway, Suite 600, Plano, TX 75024.

40. TSMC has conducted and does conduct business within the State of Texas. TSMC, directly or through corporate relatives, subsidiaries, or intermediaries (including distributors, retailers, alliance partners, and others), ships, distributes, makes, has made, uses, sells, offers for sale, imports, and/or advertises (including by providing interactive web pages) its infringing products (or products manufactured using infringing processes) and/or services in the United States and the Eastern District of Texas and/or contributes to or actively induces its customers, subsidiaries, partners, affiliates, and/or other third parties to ship, distribute, make, have made, use, offer to sell, sell, import, and/or advertise (including by providing interactive websites and EDA tools, instructions, and manuals) infringing products (or products manufactured using infringing processes) and/or services in the United States and the Eastern District of Texas.

41. TSMC, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has purposefully and voluntarily placed one or more of its infringing products (or products manufactured using infringing processes) and/or services, as described below, into the stream of commerce with the expectation that those products will be purchased and used by customers and/or consumers in the Eastern District of Texas. These infringing products (or products manufactured using infringing processes) and/or services have been and continue to be made, used, sold, offered for sale, purchased, and/or imported by customers and/or consumers in the Eastern District of Texas. These infringing products, including but not limited to the infringing TSMC semiconductor dies incorporated into Lenovo's Moto G Play smartphone (incorporating a TSMC 6nm semiconductor die in the Qualcomm Snapdragon 680 4G), Lenovo's Yoga Slim 7X laptop (incorporating a TSMC 4nm semiconductor die in the Qualcomm Snapdragon X Elite integrated circuit), OnePlus's OnePlus 13 smartphone

(incorporating a TSMC 3nm semiconductor die in the Qualcomm Snapdragon 8 Elite), OnePlus 13R smartphone (incorporating a TSMC 4nm semiconductor die in the Qualcomm Snapdragon 8 Gen 3), and Nord 30 5G smartphone (incorporating a TSMC 6nm semiconductor die in the Qualcomm Snapdragon 695 5G) are available at least at Best Buy locations throughout this district, including but not limited to: 422 W Loop 281 STE 100, Longview, TX 75605.

42. On information and belief, TSMC manufactures, has manufactured, sells, offers for sale, and/or imports products throughout the State of Texas, including within this judicial District, and introduces infringing products into the stream of commerce knowing that they would be sold in the State of Texas and this judicial District.

43. On information and belief, TSMC, either itself and/or through the activities of its subsidiaries, makes, has made, uses, sells, offers for sale, and/or imports throughout the United States, including within this judicial District, products, such as semiconductor devices and integrated circuits, that infringe (or that are manufactured by processes that infringe) the Asserted Patents. TSMC's customers, and other downstream entities, such as the Lenovo Defendants', and OnePlus's suppliers, including but not limited to, Qualcomm, use TSMC's EDA software, manuals, and instructions to design, have manufactured, and incorporate these products into downstream products that are made, used, sold, offered for sale, and/or imported throughout the United States, including the State of Texas and within this judicial District. These downstream products may include, but are not limited to, integrated circuits, computers, smartphones, tablets, smartwatches, televisions, internet of things (IoT) devices, automobiles, and network units, that include semiconductor devices and integrated circuits.

44. As one example, on information and belief, TSMC uses its infringing 4 nm process node to fabricate the Qualcomm Snapdragon X Elite integrated circuit incorporated in Defendant

Lenovo's Yoga Slim 7X laptop and Qualcomm Snapdragon 8 Gen 3 integrated circuit incorporated into Defendant OnePlus's OnePlus 13R smartphone, its infringing 6 nm process node to fabricate the Qualcomm Snapdragon 680 4G in Defendant Lenovo's Moto G Play smartphone and the Qualcomm 695 5G integrated circuit incorporated in Defendant OnePlus's Nord N30 5G smartphone, and its infringing 3nm process node to fabricate the Qualcomm Snapdragon 8 Elite integrated circuit incorporated in Defendant OnePlus's OnePlus 13 smartphone.

45. TSMC, directly and/or through subsidiaries or intermediaries (including distributors, retailers, and others), has purposefully and voluntarily placed one or more of its infringing products (or products manufactured using infringing processes) and/or services, as described below, into the stream of commerce with the expectation that those products will be purchased and used by customers and/or consumers in the Eastern District of Texas. These infringing products (or products manufactured using infringing processes) and/or services have been and continue to be made, used, sold, offered for sale, purchased, and/or imported by customers and/or consumers in the Eastern District of Texas. These infringing products, including but not limited to the infringing Lenovo Yoga Slim 7X laptop (incorporating a TSMC 4nm semiconductor die in the Qualcomm Snapdragon X Elite integrated circuit) and Moto G Play smartphone (incorporating a TSMC 4nm semiconductor die in the Qualcomm Snapdragon 680 4G), OnePlus's infringing OnePlus 13R smartphone (incorporating a TSMC 4nm semiconductor die in the Qualcomm Snapdragon 8 Gen 3 integrated circuit), and OnePlus's infringing Nord N30 5G smartphone (incorporating a TSMC 6nm semiconductor die in the Qualcomm 695 5G integrated circuit) and OnePlus 13 smartphone (incorporating a TSMC 3nm semiconductor die in the Qualcomm Snapdragon 8 Elite) which are available at least at Best Buy locations throughout this district, including but not limited to: 422 W Loop 281 STE 100, Longview, TX 75605.

46. On information and belief, TSMC has also placed integrated circuits using TSMC's process node technology and products containing these integrated circuits that infringe (or products manufactured using infringing processes) into the stream of commerce by shipping infringing products (or products manufactured using infringing processes) into Texas, shipping those products knowing that they would be shipped into Texas, and/or shipping them knowing that they would be incorporated into other infringing products that would be shipped into Texas.

47. According to TSMC's annual report, in 2023, 65.2% of TSMC's net revenue came from sales contracts with customers in the "United States," and 37.7% of TSMC's net revenue came from its "Smartphone" platform. *See* 2023 TSMC Annual Report, available at: https://investor.tsmc.com/sites/ir/annual-report/2023/2023_Annual_Report_E.pdf (accessed Feb. 13, 2025). As to TSMC's revenue, Texas is the second most populous state in the United States. TSMC therefore knows, expects, intends, and desires that the integrated circuits it manufactures, and products containing its integrated circuits, will be sold in Texas, including in this District, which includes some of the largest cities in Texas by population.

48. TSMC is thus subject to personal jurisdiction in this District. *See, e.g., World-Wide Volkswagen Corp. v. Woodson*, 444 U.S. 286, 297–98 (1980) (holding that under the stream of commerce theory, a corporation subjects itself to personal jurisdiction in a forum when it "delivers its products into the stream of commerce with the expectation that they will be purchased by consumers in the forum."); *Commonwealth Sci. & Indus. Rsch. Org. v. Mediatek Inc.*, No. 6:12-CV-578, 2013 WL 12152471, at *2 (E.D. Tex. Sept. 12, 2013) (finding personal jurisdiction over Taiwanese chipmaker Realtek, which sold semiconductor chips "to foreign distributors outside the United States, which then s[old] the Realtek chips exclusively to foreign module makers and foreign original equipment manufacturers, which then integrate[d] Realtek's IC chips into products

eventually sold worldwide, including in the Eastern District,” including because allegedly “Realtek s[old] the accused products into distribution channels knowing that those products will be sold in the Eastern District of Texas.”); *Largan Precision Co. v. Ability Opto-Elects. Tech. Co.*, No. 4:19-CV-696, 2020 WL 569815, at *7 (E.D. Tex. Feb. 5, 2020) (finding personal jurisdiction over Taiwanese manufacturer of optical lenses then sold to “third-party module integrators,” who sold to “system integrators,” who sold to “original equipment manufacturer[s]....such as HP, who then turn[ed] around and s[old]...to an end customer” because. . . “the Court has no problem concluding that AOET could have expected that those products [the final products containing its lenses] would be sold in Texas.”); *Viavi Sols. Inc. v. Zhejiang Crystal-Optech Co.*, No. 2:21-CV-00378-JRG, 2022 WL 16856099, at *3 (E.D. Tex. Nov. 10, 2022); *Atlas Glob. Techs. LLC v. TP-Link Techs. Co.*, No. 2:21-CV-430-JRG-RSP, 2022 WL 18584501 (E.D. Tex. Dec. 28, 2022), report and recommendation adopted, No. 221CV00430JRGRSP, 2023 WL 1478451 (E.D. Tex. Feb. 2, 2023); *ICON Health & Fitness, Inc. v. Horizon Fitness, Inc.*, 2009 WL 1025467, *14 (E.D. Tex. Mar. 26, 2009).

49. TSMC has established sufficient minimum contacts with the State of Texas such that the exercise of jurisdiction would not offend traditional notions of fair play and substantial justice.

JOINDER

50. Joinder of Defendants is proper under 35 U.S.C. § 299. The allegations of patent infringement contained herein arise out of the same series of transactions or occurrences relating to the making (or having made), using (or inducing the use of), selling, or offering for sale within the United States, or importing (or having imported) into the United States, several of the same infringing products, including, e.g., the Lenovo Defendants’ and OnePlus’s products incorporating the semiconductor devices fabricated by TSMC.

51. Examples of such products include, but are not limited to, Lenovo's Yoga Slim 7X laptop (which is, on information and belief, a laptop containing a Qualcomm Snapdragon X Elite integrated circuit fabricated by TSMC's 4 nm process node) and Moto G Play smartphone (which is, on information and belief, a smartphone containing a Qualcomm Snapdragon 680 4G integrated circuit fabricated by TSMC's 6 nm process node), and OnePlus's Nord N30 5G smartphone (which is, on information and belief, is a smartphone containing a Qualcomm Snapdragon 695 5G integrated circuit fabricated by TSMC at TSMC's 6 nm process node) and OnePlus 13 smartphone (which is, on information and belief, is a smartphone containing a Qualcomm Snapdragon 8 Elite integrated circuit fabricated by TSMC at TSMC's 3nm process node). Therefore, the Lenovo Defendants' and OnePlus's products, on information and belief, contain and/or consist of chips fabricated by TSMC, and are designed, made, used, sold, offered for sale, and/or imported in this judicial District. *See, e.g.,* <https://www.lenovo.com/us/en/pc/> (accessed Feb. 13, 2025); <https://www.motorola.com/us/en/smartphones/index.html> (accessed Feb. 13, 2025); <https://www.oneplus.com/us/store> (accessed Feb. 13, 2025).

ALLEGATIONS OF PATENT INFRINGEMENT

52. Plaintiffs incorporate the allegations of all of the foregoing paragraphs as if fully restated herein.

53. As set forth below, the infringing products consist of and/or incorporate, without any license from Plaintiffs, semiconductor devices protected by patents owned by Plaintiffs. Plaintiffs respectfully seek relief from this Court for Defendants' infringement.

54. Plaintiffs are the sole and exclusive owner of all right, title, and interest in and to the Asserted Patents, and hold the exclusive right to take all actions necessary to enforce their rights to the Asserted Patents, including the filing of this action. Plaintiffs also have the right to recover all damages for past, present, and future infringement of the Asserted Patents.

55. Plaintiffs, the present owner of the Asserted Patents, and the prior owner of the Asserted Patents, have complied with 35 U.S.C. §§ 286 and 287(a), and are therefore are entitled to past damages for Defendants' infringement beginning six years prior to the filing date of the present Complaint. Plaintiffs are also entitled to damages for Defendants' continuing infringement until the expiration of the last to expire of the Asserted Patents.

The Lenovo Defendants

56. The Lenovo Defendants, either themselves and/or through the activities of their subsidiaries or intermediaries (including distributors, retailers, and others), manufacture, have manufactured, make, have made, use, sell, offer for sale, import, have imported, test, design, and/or market in the United States semiconductor devices, integrated circuits, and products containing the same that infringe (or that are manufactured by processes that infringe) the Asserted Patents.

57. The Lenovo Defendants have directly infringed, and continue to directly infringe, the Asserted Patents under 35 U.S.C. § 271(a) and (g) by making, having made, using, selling and/or offering for sale, in this district and elsewhere in the United States, and/or importing into this district and elsewhere in the United States, certain semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents, as described in further described in Counts I-III *infra*.

58. The Lenovo Defendants have been placed on actual notice of the Asserted Patents at least as early as the filing of this Complaint, which constitutes notice of the Asserted Patents in accordance with 35 U.S.C. § 287.

59. The Lenovo Defendants have also indirectly infringed, and continue to indirectly infringe the Asserted Patents under 35 U.S.C. § 271(b) and (c). The Lenovo Defendants have knew and intended to induce the infringement of the Asserted Patents by their subsidiaries, affiliates, retail partners, customers, and/or other third parties. The infringing products (or products

manufactured by infringing processes) have no substantially non-infringing use. After receiving actual notice of the Asserted Patents, the Lenovo Defendants proceeded to actively induce infringement of the Asserted Patents by inducing their subsidiaries, affiliates, retail partners, customers, and/or other third parties to make, use, sell, offer for sale, market, advertise, and/or import semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents, as described in detail in Counts I-III *infra*.

60. Additionally, the Lenovo Defendants have indirectly infringed, and continue to indirectly infringe, the Asserted Patents under 35 U.S.C. § 271(c) by materially contributing to infringement of the Asserted Patents by making, using, selling, offering for sale, advertising, marketing, and/or importing semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents, as described in detail in Counts I-III *infra*.

61. The scope of infringing products includes, but is not limited to, all of the Lenovo Defendants' laptops, smartphones, tablets, desktop computers, and personal computers, and other products, or products incorporating products, manufactured by TSMC using any of TSMC's 16nm and smaller process nodes (e.g., 16nm, 12nm, 7nm, 6nm, 5nm, 4nm and 3 nm), including, to the extent TSMC does not manufacture the entire final integrated circuit, the substantial portion of those integrated circuits that TSMC does manufacture. *See, e.g.,* https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_16_12nm (accessed Feb. 13, 2025). Plaintiffs reserve the right to accuse any of Lenovo Defendants' forthcoming technology or products not yet commercially available, and any products about which it learns additional relevant information.

62. On information and belief, using an infringing 7nm/6nm process node, TSMC fabricates the Qualcomm Snapdragon 680 4G die, incorporated into Lenovo's Moto G Play

smartphone, sold throughout the United States. The Qualcomm Snapdragon 680 4G die, on information and belief, is manufactured by TSMC using the 6nm variation of the TSMC 7nm/6nm process node. On information and belief, TSMC also manufactures other devices incorporated into Lenovo Defendants' products using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

63. On information and belief, using an infringing 5nm/4nm process node, TSMC fabricates the Qualcomm Snapdragon X Elite integrated circuit, incorporated into the Lenovo Yoga Slim 7X laptop, sold throughout the United States. The Qualcomm Snapdragon X Elite integrated circuit, on information and belief, is manufactured by TSMC using the 4nm variation of the TSMC 5nm/4nm process node. TSMC also manufactures other devices incorporated into Lenovo Defendants' products using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

64. In particular, on information and belief, all devices manufactured by TSMC at a given "process node" are the same or essentially the same, and are created in the same or essentially the same way, with respect to aspects relevant to the claims of the Asserted Patents. If one product using a TSMC-based integrated circuit or other product manufactured by TSMC at a given process node infringes one of the Asserted Patents, as described in detail in Counts I-III *infra*, all other devices manufactured by TSMC at that process node infringe that Asserted Patent. Plaintiffs reserve the right to identify additional products that are produced at accused nodes, and to add nodes, as it learns more information.

65. The Lenovo Defendants' acts of infringement have caused damage to Plaintiffs. Plaintiffs are entitled to recover from the Lenovo Defendants the damages incurred by Plaintiffs as a result of the Lenovo Defendants' wrongful acts.

66. The Lenovo Defendants' acts of direct and indirect infringement are willful and have caused, and will continue to cause, substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law. The Lenovo Defendants performed and continue to perform the acts that constitute direct and/or indirect infringement, with knowledge or willful blindness that the acts would constitute direct and/or indirect infringement of the Asserted Patents. Notwithstanding the Lenovo Defendants' knowledge of the Asserted Patents since at least as early as the filing of the present Complaint, the Lenovo Defendants have and continue to willfully infringe the Asserted Patents.

OnePlus

67. OnePlus, either itself and/or through the activities of its subsidiaries or intermediaries (including distributors, retailers, and others), manufactures, has manufactured, makes, has made, uses, sells, offers for sale, imports, has imported, tests, designs, and/or markets in the United States semiconductor devices, integrated circuits, and products containing the same that infringe (or that are manufactured by processes that infringe) the Asserted Patents.

68. OnePlus has directly infringed, and continues to directly infringe, the Asserted Patents under 35 U.S.C. § 271(a) and (g) by making, having made, using, selling and/or offering for sale, in this district and elsewhere in the United States, and/or importing into this district and elsewhere in the United States, certain semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents, as described in further described in Counts I-V *infra*.

69. OnePlus has been placed on actual notice of the Asserted Patents at least as early as the filing of this Complaint, which constitutes notice of the Asserted Patents in accordance with 35 U.S.C. § 287.

70. OnePlus has also indirectly infringed, and continues to indirectly infringe the

Asserted Patents under 35 U.S.C. § 271(b) and (c). OnePlus knew and intended to induce the infringement of the Asserted Patents by its subsidiaries, affiliates, retail partners, customers, and/or other third parties. The infringing products (or products manufactured by infringing processes) have no substantially non-infringing use. After receiving actual notice of the Asserted Patents, OnePlus proceeded to actively induce infringement of the Asserted Patents by inducing its subsidiaries, affiliates, retail partners, customers, and/or other third parties to make, use, sell, offer for sale, market, advertise, and/or import semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents, as described in detail in Counts I-V *infra*.

71. Additionally, OnePlus has indirectly infringed, and continues to indirectly infringe, the Asserted Patents under 35 U.S.C. § 271(c) by materially contributing to infringement of the Asserted Patents by making, using, selling, offering for sale, advertising, marketing, and/or importing semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents, as described in detail in Counts I-V *infra*.

72. The scope of infringing products includes, but is not limited to, all OnePlus smartphones, tablets, and wearables other products, or products incorporating products, manufactured by TSMC using of TSMC's 16nm and smaller process nodes (e.g., 16nm, 12nm, 7nm, 6nm, 5nm, 4nm and 3 nm), including, to the extent TSMC does not manufacture the entire final integrated circuit, the substantial portion of those integrated circuits that TSMC does manufacture.

See, e.g.,

https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_16_12nm (accessed Feb. 13, 2025). Further patent-specific assertions are below. Plaintiffs reserve the right to accuse any forthcoming TSMC technology or products not yet commercially available, and any products

about which it learns additional relevant information.

73. On information and belief, using an infringing 7nm/6nm process node, TSMC fabricates the Qualcomm Snapdragon 695 5G semiconductor die, incorporated into OnePlus's Nord N30 5G smartphone, sold throughout the United States. The Qualcomm Snapdragon 695 5G integrated circuit, on information and belief, is manufactured by TSMC using the 6nm variation of the TSMC 7nm/6nm process node. On information and belief, TSMC also manufactures other devices incorporated into OnePlus products using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

74. On information and belief, using an infringing 5nm/4nm process node, TSMC fabricates the Qualcomm Snapdragon 8 Gen 3 semiconductor die, incorporated into OnePlus's OnePlus 13R smartphone, sold throughout the United States. The Qualcomm Snapdragon 8 Gen 3 integrated circuit, on information and belief, is manufactured by TSMC using the 4nm variation of the TSMC 5nm/4nm process node. On information and belief, TSMC also manufactures other devices incorporated into OnePlus products using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

75. On information and belief, using an infringing 3nm process node, TSMC fabricates the Qualcomm Snapdragon 8 Elite die, incorporated into the OnePlus 13 smartphone, sold throughout the United States. On information and belief, TSMC also manufactures other devices incorporated into OnePlus products using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

76. In particular, on information and belief, all devices manufactured by TSMC at a given "process node" are the same or essentially the same, and are created in the same or essentially the same way, with respect to aspects relevant to the claims of the Asserted Patents. If one product

using a TSMC-based integrated circuit or other product manufactured by TSMC at a given process node infringes one of the Asserted Patents, as described in detail in Counts I-V *infra*, all other devices manufactured by TSMC at that process node infringe that Asserted Patent. Plaintiffs reserve the right to identify additional products that are produced at accused nodes, and to add nodes, as it learns more information.

77. OnePlus's acts of infringement have caused damage to Plaintiffs. Plaintiffs are entitled to recover from OnePlus the damages incurred by Plaintiffs as a result of OnePlus's wrongful acts.

78. OnePlus's acts of direct and indirect infringement are willful and have caused, and will continue to cause, substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law. OnePlus performed and continues to perform the acts that constitute direct and/or indirect infringement, with knowledge or willful blindness that the acts would constitute direct and/or indirect infringement of the Asserted Patents. Notwithstanding OnePlus's knowledge of the Asserted Patents since at least as early as the filing of the present Complaint, OnePlus has and continues to willfully infringe the Asserted Patents.

TSMC

79. TSMC, either itself and/or through the activities of its subsidiaries or intermediaries (including distributors, retailers, EDA alliance partners, and others), manufacturers, has manufactured, makes, has made, uses, sells, offers to sell, imports, has imported, tests, designs, and/or markets in the United States semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents.

80. TSMC has directly infringed, and continues to directly infringe, the Asserted Patents under 35 U.S.C. § 271(a) and (g) by making, using, selling and/or offering for sell, in this district and elsewhere in the United States, and/or importing into this district and elsewhere in the

United States, certain semiconductor devices that infringe the Asserted Patents (or that are manufactured by processes that infringe), as described in further described in Counts I-V *infra*.

81. With notice of the Asserted Patents, TSMC has proceeded to directly infringe by making, having made, using, testing, designing, selling, offering for sale, and/or importing in this district and elsewhere in the United States, semiconductor devices, integrated circuits, products containing the same, and components thereof that infringe the Asserted Patents.

82. Prior to initiating litigation, since March 8, 2023, Plaintiffs sought to negotiate a license with TSMC and its customers. Subsequent to the first notice letter on March 8, 2023, Plaintiffs conducted extensive discussions with TSMC, and its customers, to reach an amicable license. These discussions included at least seven virtual meetings, numerous email exchanges, and two in-person meetings in Hsinchu with TSMC. Neither TSMC nor its customers have ever made an offer to purchase a license to the MSL patents.

83. Specifically, on March 8, 2023, Plaintiffs sent a notice letter to TSMC's customer that its products infringe twelve of Marlin's patents, including the '847 patent and the '473 patent, based on its incorporation of infringing TSMC products. In a second notice letter dated December 7, 2023, Plaintiffs informed TSMC's customer that its various products infringed an additional twelve Marlin patents, including the '292 Patent. Of the twenty-four patents identified in Plaintiffs' two notice letters to TSMC's customer, twenty-two are directed to semiconductor structures and fabrication, while the other two patents are directed to circuit structures and operation. On information and belief, TSMC was aware that the infringing instrumentalities identified by the notice letters in its customer's products were fabricated and/or included components fabricated by TSMC.

84. TSMC was on actual notice of at least the '847 Patent and '473 Patent at least as

early as October 2023, when, upon information and belief, TSMC's customer forwarded Marlin's notice letters to TSMC. On October 31, 2023, Plaintiffs conducted a virtual meeting (over zoom) with TSMC's customer, during which Plaintiffs mentioned that its representative would be in Hsinchu, Taiwan in November 2023, and offered to meet with TSMC to discuss a possible license at that time. TSMC emailed Plaintiffs on October 31, 2023, and declined the meeting with Plaintiffs' representative. On December 22, 2023, TSMC's customer transmitted a letter to Plaintiffs, indicating that it is coordinating with TSMC on its response to Plaintiffs' notice letters.

85. After subsequent email exchanges, Plaintiffs representatives traveled to Hsinchu, Taiwan on May 21-22, 2024 to meet with TSMC. In those meetings, TSMC referred expressly to the twenty-two patents, including '847 Patent, '473 Patent, and '292 Patent, regarding semiconductor structures and fabrication which were asserted by Plaintiffs against TSMC's customers. At the meeting, TSMC claimed to have prepared *inter partes review* petitions against all 22 patents that Plaintiffs identified to TSMC's customer, and presented to Plaintiffs portions of the purported draft petitions for several of the patents, including at least the '473 Patent. Thus, TSMC was placed on actual notice of at least the '847 Patent, '473 Patent, and '292 Patent at least as early as May 21, 2024, by way of the meeting between Plaintiffs and TSMC in Hsinchu, Taiwan.

86. Additionally, filing of this Complaint also constitutes notice of the Asserted Patents in accordance with 35 U.S.C. § 287.

87. On information and belief, within the United States including in this district, TSMC conducts sales activities, negotiations, design and development work, and other activities related to its semiconductor devices and sales thereof.

88. On information and belief, TSMC at least imports its semiconductor devices to the United States to its customers and its subsidiaries. Moreover, TSMC sells to U.S. companies, such

as Qualcomm, Broadcom, and Apple, and 65.2% of its revenue comes from sales to the U.S., as explained above. *See TSMC 2023 Annual Report, Consolidated Financial Statements* at 52 available at: [https://investor.tsmc.com/sites/ir/annual-report/2023/2023 Annual Report E.pdf](https://investor.tsmc.com/sites/ir/annual-report/2023/2023%20Annual%20Report%20E.pdf) (accessed Feb. 13, 2025). Also, TSMC “provides customer support, account management, and engineering services through offices in North America[.]” *Id.* at 16.

89. Further, according to TSMC’s annual report, TSMC operates subsidiaries in the United States, such as TSMC North America, whose business activities include “[s]ales and marketing of integrated circuits and other semiconductor devices.” *Id.* at 181. Thus, TSMC’s sales and offers for sale, even if they include some foreign activity, are “in the United States.” *See, e.g., Carnegie Mellon Univ. v. Marvell Tech. Grp., Ltd.*, 807 F.3d 1283, 1308-1309 (Fed. Cir. 2015) (finding that a reasonable jury could conclude that sales of chips manufactured outside the United States were “in the United States” under § 271(a) where fabless chip designer Marvell’s design activities were in the U.S., and there was “sales activity by Marvell within the United States, even for chips manufactured, delivered, and used entirely abroad”); *Godo Kaisha IP Bridge 1 v. Broadcom Ltd.*, No. 2:16-CV-00134-JRG, 2017 WL 2869332, at *3 (E.D. Tex. May 18, 2017); *Lake Cherokee Hard Drive Techs., L.L.C. v. Marvell Semiconductor, Inc.*, 964 F. Supp. 2d 653, 658 (E.D. Tex. 2013).

90. On information and belief, TSMC imports its infringing semiconductor devices directly into the United States in connection with its CyberShuttle and/or Multi-Project Wafer (“MPW”) program. *See* <https://www.tsmc.com/english/dedicatedFoundry/services/cyberShuttle> (accessed Feb. 13, 2025). TSMC’s CyberShuttle program provides a “prototyping service [that] significantly reduces NRE costs by covering the widest technology range (from 0.5um to 7nm) and the most frequent launch schedule (up to 10 shuttles per month).” *Id.* Further, TSMC has a

university program (“TSMC University FinFET Program”) which “offers the industry’s most successful fin field-effect transistor (FinFET) technologies with multi-project wafer (MPW) services and design collateral, for TSMC’s 16-nanometer (16nm) and 7-nanometer (7nm) processes, covering both logic designs and radio frequency (RF) designs.” https://www.tsmc.com/english/dedicatedFoundry/services/university_program (accessed Feb. 13, 2025). In addition, TSMC collaborates closely with Stanford, MIT, Princeton, and UCSD on the “TSMC University Collaboration Program,” and offers the “TSMC University Shuttle Program” which provides “access to TSMC silicon process technologies for digital and analog/mixed signal circuits, RF designs, non-volatile memory design and ultra-low power designs.” (TSMC 2023 Annual Report) at 104.

91. In addition to whatever volumes of infringing products TSMC imports into the United States through the CyberShuttle and MPW programs, on information and belief, those shipments further result in TSMC securing a “design win” to mass-produce the design incorporated in the CyberShuttle prototype. Thus significant sales that are “within the United States” even if certain aspects of the sale or performance thereof take place in other countries.

92. TSMC has also indirectly infringed, and continues to indirectly infringe the Asserted Patents under 35 U.S.C. § 2871(b) and (c). TSMC knew and intended to induce the infringement of the Asserted Patents by its direct or indirect customers, subsidiaries, partners, affiliates, and/or other third parties. The infringing products (or are manufactured by processes that infringe) have no substantially non-infringing use. After receiving actual notice of the Asserted Patents, TSMC proceeded to actively induce infringement of the Asserted Patents by inducing its customers, subsidiaries, partners, affiliates, and/or other third parties to make, use, sell, offer for sale, market, advertise, and/or import semiconductor devices, integrated circuits, and/or products

containing the same that infringe (or are manufactured by processes that infringe) the Asserted Patents, as described in detail in Counts I-V *infra*.

93. Additionally, TSMC has indirectly infringed, and continues to indirectly infringe, the Asserted Patents under 35 U.S.C. § 271(c) by materially contributing to infringement of the Asserted Patents by making, using, selling, offering for sale, advertising, marketing, and/or importing semiconductor devices that infringe (or that are manufactured by processes that infringe) the Asserted Patents, as described in detail in Counts I-V *infra*.

94. The scope of infringing products includes, but is not limited to, all TSMC semiconductor devices, integrated circuits, and other products manufactured by TSMC using any of TSMC's 16nm and smaller process nodes (e.g., 16nm, 12nm, 7nm, 6nm, 5nm, 4nm and 3 nm), including, for example, the semiconductor devices and integrated circuits incorporated into Lenovo and OnePlus products, and to the extent TSMC does not manufacture the entire final integrated circuit, the substantial portion of those integrated circuits that TSMC does manufacture. See, e.g., https://www.tsmc.com/english/dedicatedFoundry/technology/logic/1_16_12nm (accessed Feb. 13, 2025). The scope of infringing products also includes downstream products that incorporate those TSMC's products, such as computers, smartphones, tablets, smart watches, network units, and other electronic devices. Further patent-specific assertions are below. Plaintiffs reserve the right to accuse any forthcoming TSMC technology or products not yet commercially available, and any products about which it learns additional relevant information.

95. On information and belief, using an infringing 7nm/6nm process node, TSMC fabricates the, semiconductor die incorporated into, at least, the Qualcomm Snapdragon 680 4G in the Lenovo Moto G Play smartphone and Qualcomm Snapdragon 695 5G in the OnePlus Nord N30 5G smartphone, sold throughout the United States. On information and belief, TSMC

manufactures the Qualcomm Snapdragon 680 4G and Qualcomm Snapdragon 695 5G semiconductor dies using the 6nm variation of the its 7nm/6nm process node. TSMC also manufactures other TSMC devices using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

96. On information and belief, using an infringing 5nm/4nm process node, TSMC fabricates the semiconductor die incorporated into, at least, the Qualcomm Snapdragon X Elite processor in the Lenovo Yoga Slim 7X laptop and Qualcomm Snapdragon 8 Gen 3 processor in the OnePlus 13R smartphone, sold throughout the United States. On information and belief, TSMC manufactures the Qualcomm Snapdragon X Elite and Qualcomm Snapdragon 8 Gen 3 semiconductor dies using the 4nm variation of the its 5nm/4nm process node. TSMC also manufactures other TSMC devices using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

97. On information and belief, using an infringing 3nm process node, TSMC also fabricates the semiconductor die, incorporated into, at least, the Qualcomm Snapdragon 8 Elite integrated circuit in the OnePlus 13 smartphone, sold throughout the United States. TSMC also manufactures other devices using this process node, which thus infringe and are incorporated into other electronic devices sold to end user customers in the United States.

98. In particular, on information and belief, all devices manufactured by TSMC at a given “process node” are the same or essentially the same, and are created in the same or essentially the same way, with respect to aspects relevant to the claims of the Asserted Patents. If one product using a TSMC-based integrated circuit or other product manufactured by TSMC at a given process node infringes one of the Asserted Patents, as described in detail in Counts I-V *infra*, all other devices manufactured by TSMC at that process node infringe that Asserted Patent. Plaintiffs

reserve the right to identify additional products that are produced at accused nodes, and to add nodes, as it learns more information.

99. TSMC specifically intends that third parties, such as its direct and indirect customers (such as Qualcomm, Lenovo, and OnePlus) and intermediaries thereof, resellers, retailers, and end users infringe the Asserted Patents, and knows that these others perform acts that constitute direct infringement. For example, TSMC designed and/or manufactured the products such that they would each infringe the Asserted Patents if used, sold, offered for sale, or imported in the United States, and specifically intended that they be used, sold, offered for sale, and imported into the United States. TSMC provided, directly or indirectly, infringing products to others, such as, direct and indirect customers and intermediaries thereof, resellers, retailers, and end users knowing and intending that those others would use, sell, offer for sale, and/or import in and into the United States, downstream products that incorporate TSMC's infringing semiconductor products, thereby directly infringing one or more claims of the Asserted Patents.

100. Upon information and belief, TSMC knowingly and actively aided and abetted the direct infringement of the Asserted Patents by directly and indirectly instructing and encouraging its direct and indirect customers and other downstream manufacturers and implementers, purchasers, users, and developers to use and/or adopt the Asserted Patent's technology in the form of TSMC's products. These instructions and encouragement include, but are not limited to, manufacturing infringing products for its customers' and other downstream entities' infringing use, sale, offer for sale, and importing of, advertising of, and promoting the use of the infringing products, and directly and indirectly providing instructions, support, and technical information regarding infringing products to direct infringers described above.

101. In addition, TSMC partners with EDA partners throughout the United States,

including within this district, to “win business and stay competitive” using its “Open Innovation Platform.” <https://www.tsmc.com/english/dedicatedFoundry/grandAlliance> (accessed Feb. 13, 2025). Specifically, TSMC’s “EDA Alliance, a key component of TSMC Open Innovation Platform (OIP), reduces design barriers for customer's adoption of TSMC process technologies.” https://www.tsmc.com/english/dedicatedFoundry/oip/eda_alliance (accessed Feb. 13, 2025). “By combining TSMC and EDA Alliance members R&D capability and resource, new generations of EDA solutions are enabled to be compliant to TSMC technology requirements.” *Id.* “Selected EDA Alliance partners work closely with TSMC's design technology teams to address customer design needs through the enablement of new EDA tool features that align with TSMC advanced process development roadmap, as well as the implementation of TSMC's design methodology in Reference Flows.” *Id.* Upon information and belief, TSMC’s induces and contributes to the infringement of its customers , subsidiaries, partners, affiliates, and/or other third parties, by partnering with EDA alliance members on the development and certification of instructions, manuals, and design software, which are provided to TSMC’s customers for the purpose of designing, using, selling, offering for sale, and importing products that use TSMC’s infringing semiconductor manufacturing structures and processes. Among TSMC’s EDA alliance partners is Siemens EDA, which TSMC recognized in 2021 as one of four “OIP Partner[s] of the Year,” along with ANSYS, Cadence Design Systems, and Synopsis, for its work with TSMC on “Joint Development of 4nm Design Infrastructure.” <https://pr.tsmc.com/english/news/2875> (accessed Feb. 13, 2025).

102. TSMC’s acts of infringement have caused damage to Plaintiffs. Plaintiffs are entitled to recover from TSMC the damages incurred by Plaintiffs as a result of TSMC’s wrongful acts.

103. TSMC's acts of direct and indirect infringement are willful, and have caused and will continue to cause substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law. TSMC performed and continues to perform the acts that constitute direct and/or indirect infringement, with knowledge or willful blindness that the acts would constitute direct and/or indirect infringement of the Asserted Patents. Notwithstanding TSMC's knowledge of the Asserted Patents and TSMC's infringement thereof since before, and no later than the filing of, the present Complaint, TSMC has and continues to willfully infringe the Asserted Patents.

COUNT I

Infringement of the '847 Patent

104. Plaintiffs incorporate the allegations of all of the foregoing paragraphs as if fully restated herein.

105. Plaintiff Marlin Semiconductor is the assignee and lawful owner of all rights, title, and interest in and to the '847 Patent. The '847 Patent is valid and enforceable.

106. The '847 Patent is entitled "Metal Oxide Semiconductor Transistor," and issued on June 29, 2010 to inventors Chu-Yin Tseng, Shih-Chieh Hsu, Chih-Chiang Wu, Shyh-Fann Ting, Po-Lun Cheng, and Hsuan-Hsu Chen. The '847 Patent issued from U.S. Patent Application No. 11/836,772, which was filed on Aug. 9, 2007.

107. Defendants have directly and indirectly infringed, and continue to directly and indirectly infringe, the '847 Patent by making, having made, using, selling, offering for sale, and/or importing into the United States products that infringe (or that are manufactured using processes that infringe) the '847 Patent including, but not limited to semiconductor devices manufactured using TSMC's 16nm, 12nm, 7nm, 6nm, 5nm, 4nm, and 3nm process nodes. The products that infringe one or more claims of the '847 Patent include, but are not limited to, at least the products identified herein. Further discovery may reveal additional infringing products and/or models.

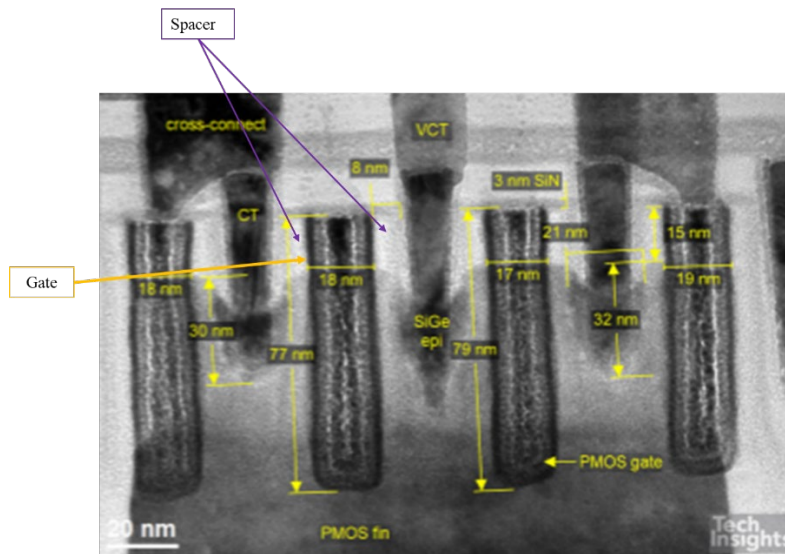
108. For example, and without limitation, the infringing products infringe one or more claims of the '847 Patent, including but not limited to claim 1. The infringing products fall within the scope of and include, either literally or under the doctrine of equivalents, all of the elements of at least claim 1 of the '847 Patent.

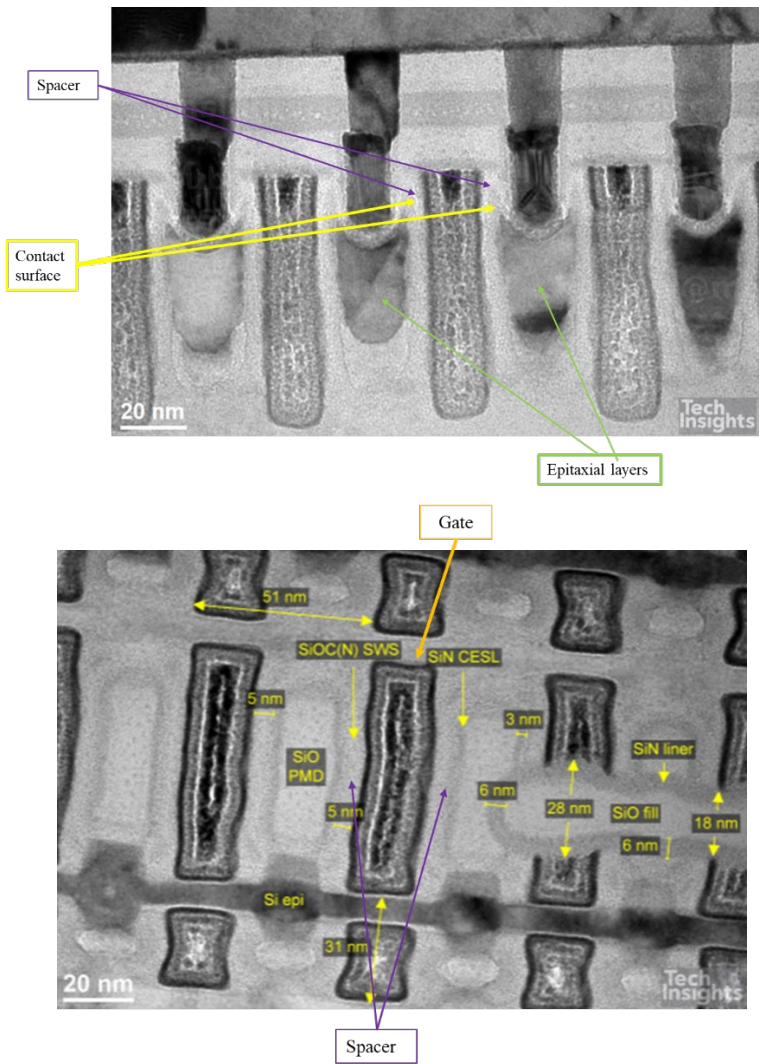
109. The infringing products include all the limitations of at least claim 1 of the '847 Patent. Specifically, the '847 Patent claims, e.g., A MOS transistor structure, comprising: a gate formed on a semiconductor substrate; two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate; a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

110. With respect to exemplary devices, the semiconductor die incorporated in the Qualcomm Snapdragon X Elite integrated circuit, which is incorporated in the Lenovo Yoga Slim 7X laptop, is manufactured by TSMC using its 4nm process node. *See Tomshardware.com, Snapdragon X Elite Outperforms Intel, AMD, Apple CPUs (In Vendor Benchmarks)*, at <https://www.tomshardware.com/news/snapdragon-x-elite-outperforms-intel-amd-apple-cpus-in-vendor-benchmarks> (accessed Feb. 13, 2025). The semiconductor die incorporated in the Qualcomm Snapdragon 8 Gen 3 integrated circuit, which is incorporated in OnePlus 13R smartphone, is manufactured by TSMC using its 4nm process node. *See* <https://nanoreview.net/en/soc/qualcomm-snapdragon-8-gen-3> (accessed Feb. 13, 2025).

111. The other products produced by TSMC at the same node size also infringe for the same reasons as above, as explained in ¶ 96.

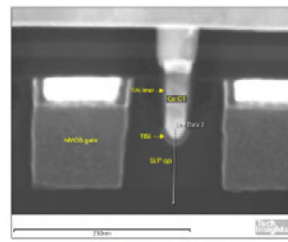
112. These exemplary devices directly infringe at least claim 1 of the '847 Patent. Specifically, the TSMC 4nm semiconductor dies incorporated in the Lenovo Yoga Slim 7X laptop and OnePlus 13R smartphone comprise all elements of claim 1 of the '847 Patent. Upon information and belief, these exemplary devices are substantially similar in materials, structures, and features as semiconductor dies that TSMC manufactures using its 5nm process node, which is representative of the exemplary devices and other semiconductor devices manufactured using TSMC's 16nm, 12nm, 7nm, 6nm, 5nm, 4nm, and 3nm process nodes. Furthermore, as shown in the images below of an example semiconductor die made using TSMC's 5 nm process node (a TSMC 5 nm semiconductor die incorporated in an Apple A15 Bionic APLW07 integrated circuit), the example semiconductor die comprises all elements of claim 1 of the '847 Patent.



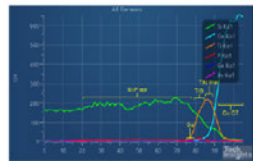
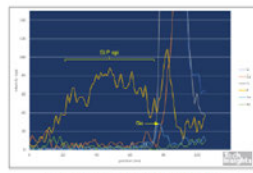


NMOS S/D Epi and Contact Composition

- The NMOS S/D epi is doped with phosphorus, with Ge detected at the top of the epi, near the silicide.
- A Ti silicide is used at the epi-contact interface.
- The S/D CT contact has a TiN liner and is filled with Co.



Linescan Across S/D in IO Region – HAADF STEM Cross Section Across Gates



EDS Linescan (Top) and Zoom on Selected Elements (Bottom)

Tech Insights

113. As a result of Defendants' infringement of the '847 Patent, Plaintiffs are entitled to monetary damages in an amount adequate to compensate for Defendants' infringement, but in no event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

114. Defendants' acts of direct and indirect infringement of the '847 Patent are willful, and have caused and will continue to cause substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law.

COUNT II

Infringement of the '473 Patent

115. Plaintiffs incorporate the allegations of all of the foregoing paragraphs as if fully restated herein.

116. Plaintiff Marlin Semiconductor is the assignee and lawful owner of all rights, title, and interest in and to the '473 Patent. The '473 Patent is valid and enforceable.

117. The '473 Patent is entitled "Method for Fabricating Metal-Oxide Semiconductor Transistor," and issued on July 28, 2015 to inventors Ming-Te Wei, Wen-Chen Wu, Lung-En Kuo, and Po-Chao Tsao. The '473 Patent issued from U.S. Patent Application No. 14/331,229, which was filed on July 15, 2014, and is a division of U.S. Patent Application No. 12/837,475, which was filed on July 15, 2010, now U.S. Patent No. 8,816,409.

118. Defendants have directly and indirectly infringed, and continue to directly and indirectly infringe, the '473 Patent by making, having made, using, selling, offering for sale, and/or importing into the United States products that infringe the '473 Patent including, but not limited to semiconductor devices manufactured using TSMC's 16nm, 12nm, 7nm, 6nm, 5nm, 4nm, and 3nm process nodes. The products that infringe one or more claims of the '473 Patent include, but are not limited to, at least the products identified herein. Further discovery may reveal additional

infringing products and/or models.

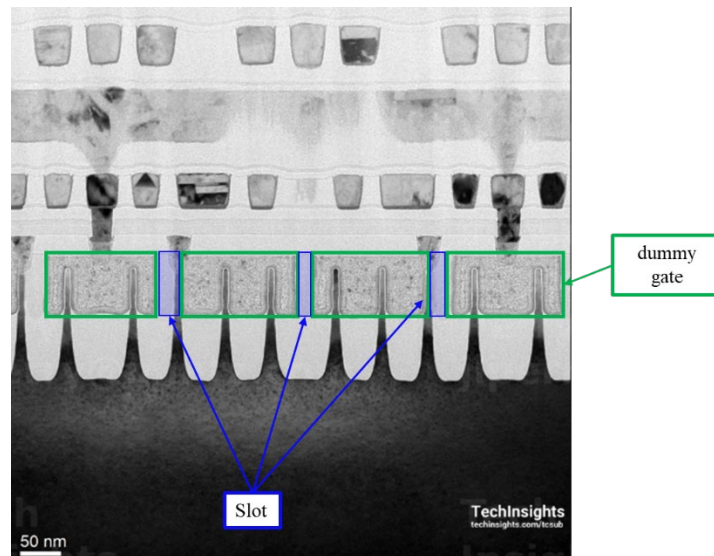
119. For example, and without limitation, the infringing products infringe one or more claims of the '473 Patent, including but not limited to claim 1. The infringing products fall within the scope of and include, either literally under the doctrine of equivalents, all of the elements of at least claim 1 of the '473 Patent.

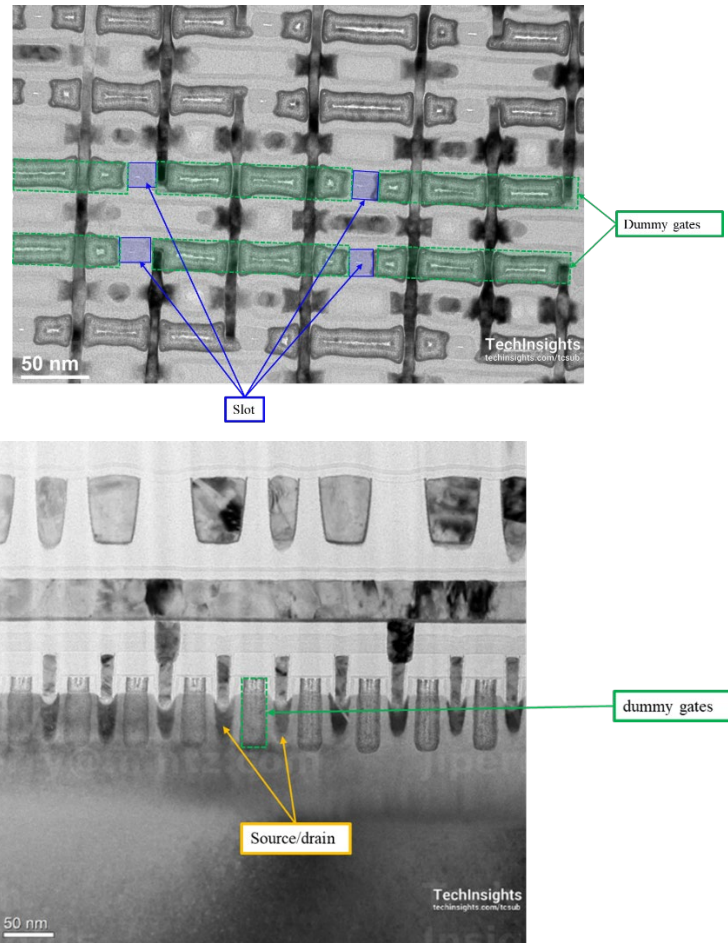
120. The infringing products include all the limitations of at least claim 1 of the '473 Patent. Specifically, the '473 Patent claims, e.g., a method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising: providing a semiconductor substrate; forming a silicon layer on the semiconductor substrate; performing a first photo-etching process on the silicon layer for forming a gate pattern; forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

121. With respect to exemplary devices, the semiconductor die incorporated in the Qualcomm Snapdragon 680 4G, which is incorporated in the Lenovo Yoga Slim 7X laptop, is manufactured by TSMC using its 6nm process node. *See GMS Arena, Motorola Moto G Play*, at [https://www.gsmarena.com/motorola_moto_g_play_\(2024\)-12798.php](https://www.gsmarena.com/motorola_moto_g_play_(2024)-12798.php) (accessed Feb. 13, 2025); Gizmochina.com, *New Qualcomm mid-range chips on the way, will support 144Hz refresh rate*, at <https://www.gizmochina.com/2021/09/11/new-qualcomm-mid-range-chips-on-the-way-will-support-144hz-refresh-rate/> (accessed on Feb. 13, 2025). The semiconductor die incorporated in the Qualcomm Snapdragon 695 5G, which is incorporated in the OnePlus Nord N30 5G smartphone, is manufactured by TSMC using its 6nm process node. *See https://nanoreview.net/en/soc/qualcomm-snapdragon-695* (accessed Feb. 13, 2025).

122. The other products produced by TSMC at the same node size also infringe for the same reasons as above, as explained in ¶ 96.

123. The exemplary devices infringe at least claim 1 of the '473 Patent. Specifically, the TSMC 6nm semiconductor dies incorporated into the Lenovo Yoga Slim 7X laptop and OnePlus 13R smartphone comprise all elements of claim 1 of the '473 Patent. Upon information and belief, these exemplary devices are substantially similar in materials, structures, and features as semiconductor dies that TSMC manufactures using its 7nm process node, which is representative of the exemplary devices and other semiconductor devices manufactured using TSMC's 16nm, 12nm, 7nm, 6nm, 5nm, 4nm, and 3nm process nodes. Furthermore, as shown in the images below of an example semiconductor die made using TSMC's 7nm process node (a TSMC 7nm semiconductor die incorporated in an Apple A13 Bionic APLW85 integrated circuit), the example semiconductor die comprises all elements of claim 1 of the '743 Patent.





124. As a result of Defendants' infringement of the '473 Patent, Plaintiffs are entitled to monetary damages in an amount adequate to compensate for Defendants' infringement, but in no event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

125. Defendants' acts of direct infringement of the '473 Patent are willful, and have caused and will continue to cause substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law.

COUNT III

Infringement of the '292 Patent

126. Plaintiffs incorporate the allegations of all of the foregoing paragraphs as if fully

restated herein.

127. Plaintiff Marlin Semiconductor is the assignee and lawful owner of all rights, title, and interest in and to the '292 Patent. The '292 Patent is valid and enforceable.

128. The '292 Patent is entitled "Semiconductor Structure with Different Fins of FinFETs," and issued on Nov. 10, 2015 to inventors Chin-Fu Lin, Chin-Cheng Chien, Chun-Yuan Wu, Teng-Chun Tsai, and Chih-Chien Liu. The '292 Patent issued from U.S. Patent Application No. 14/340,267, which was filed on July 24, 2014, and is a division of U.S. Patent Application No. 13/370,231, which was filed on Feb. 9, 2012, now U.S. Patent No. 8,822,284.

129. Defendants have directly and indirectly infringed, and continue to directly and indirectly infringe, the '292 Patent by making, having made, using, selling, offering for sale, and/or importing into the United States products that infringe the '292 Patent including but not limited to semiconductor devices manufactured using TSMC's 16nm, 12nm, 7nm, 6nm, 5nm, 4nm, and 3nm process nodes. The products that infringe one or more claims of the '292 Patent include, but are not limited to, at least the products identified herein. Further discovery may reveal additional infringing products and/or models.

130. For example, and without limitation, the infringing products infringe one or more claims of the '292 Patent, including but not limited to claim 1. The infringing products fall within the scope of and include, either literally under the doctrine of equivalents, all of the elements of at least claim 1 of the '292 Patent.

131. The infringing products include all the limitations of at least claim 1 of the '292 Patent. Specifically, the '292 Patent claims, e.g., A semiconductor structure for forming FinFETs, comprising: a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material; a plurality of odd fins of the FinFETs on the semiconductor

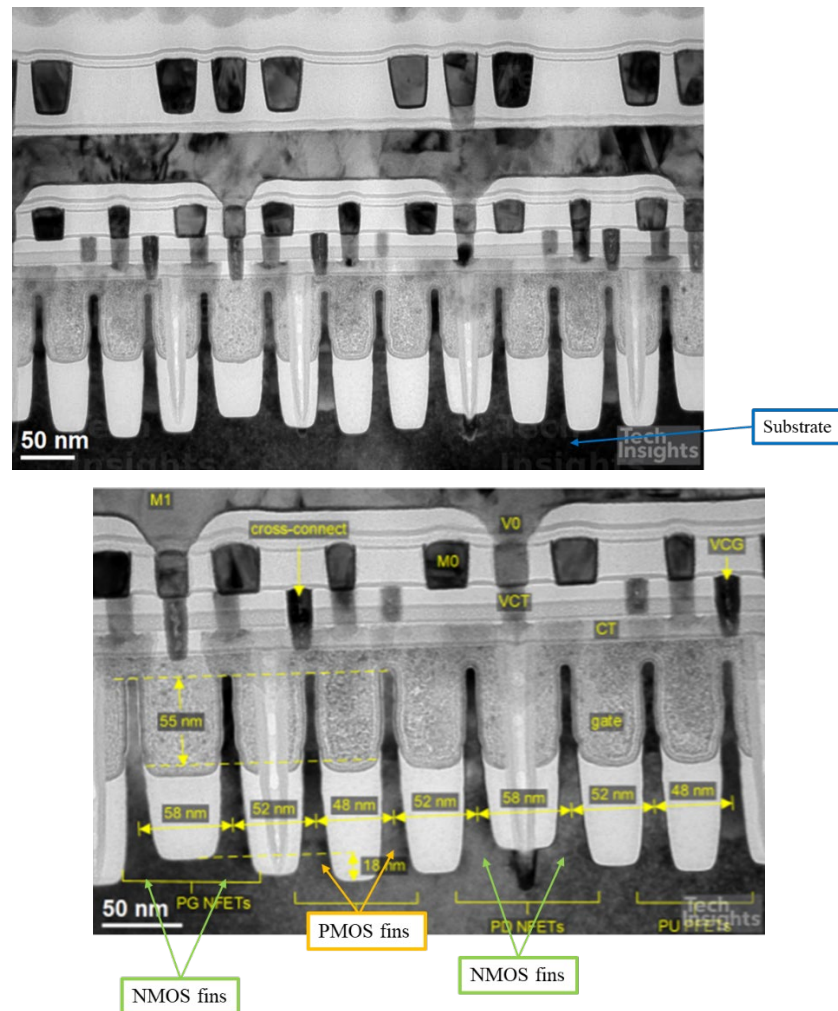
substrate, being defined from the semiconductor substrate and being formed of the semiconductor material; and a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

132. With respect to exemplary devices, the semiconductor die incorporated in the Qualcomm Snapdragon X Elite is manufactured by TSMC using its 4nm process node. *See* Tomshardware.com, *Snapdragon X Elite Outperforms Intel, AMD, Apple CPUs (In Vendor Benchmarks)*, at <https://www.tomshardware.com/news/snapdragon-x-elite-outperforms-intel-amd-apple-cpus-in-vendor-benchmarks>(accessed Feb. 13, 2025). The semiconductor die incorporated in the Qualcomm Snapdragon 8 Gen 3 integrated circuit, which is incorporated in OnePlus 13R smartphone, is manufactured by TSMC using its 4nm process node. *See* <https://nanoreview.net/en/soc/qualcomm-snapdragon-8-gen-3> (accessed Feb. 13, 2025).

133. The other products produced by TSMC at the same node size also infringe for the same reasons as above, as explained in ¶ 96.

134. These exemplary devices directly infringe at least claim 1 of the '292 Patent. Specifically, the TSMC 4nm semiconductor dies incorporated in the Lenovo Yoga Slim 7X laptop and OnePlus 13R smartphone comprise all elements of claim 1 of the '292 Patent. Upon information and belief, these exemplary devices are substantially similar in materials, structures, and features as semiconductor dies that TSMC manufactures using its 5nm process node, which is representative of the exemplary devices and other semiconductor devices manufactured using TSMC's 16nm, 12nm, 7nm, 6nm, 5nm, 4nm, and 3nm process nodes. Furthermore, as shown in the images below of an example semiconductor die made using TSMC's 5 nm process node (a

TSMC 5 nm semiconductor die incorporated in an Apple A15 Bionic APLW07 integrated circuit), the example semiconductor die comprises all elements of claim 1 of the '292 Patent.



135. As a result of Defendants' infringement of the '292 Patent, Plaintiffs are entitled to monetary damages in an amount adequate to compensate for Defendants' infringement, but in no event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

136. Defendants' acts of direct infringement of the '292 Patent are willful, and have caused and will continue to cause substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law.

COUNT IV

Infringement of the '747 Patent

137. Plaintiffs incorporate the allegations of all of the foregoing paragraphs as if fully restated herein.

138. Plaintiff Marlin Semiconductor is the assignee and lawful owner of all rights, title, and interest in and to the '747 Patent. The '747 Patent is valid and enforceable.

139. The '747 Patent is entitled "Semiconductor Structure with Hard Mask Disposed on the Gate Structure," and issued on Sept. 29, 2015 to inventors Ching-wen Hung and Chih-sen Huang. The '747 Patent issued from U.S. Patent Application No. 13/875,293, which was filed on May 2, 2013.

140. Defendants have directly and indirectly infringed, and continue to directly and indirectly infringe, the '747 Patent by making, having made, using, selling, offering for sale, and/or importing into the United States products that infringe the '747 Patent including, but not limited to semiconductor devices manufactured using TSMC's 3nm process node. The products that infringe one or more claims of the '747 Patent include, but are not limited to, at least the products identified herein. Further discovery may reveal additional infringing products and/or models.

141. For example, and without limitation, the infringing products infringe one or more claims of the '747 Patent, including but not limited to claim 1. The infringing products fall within the scope of and include, either literally under the doctrine of equivalents, all of the elements of at least claim 1 of the '747 Patent.

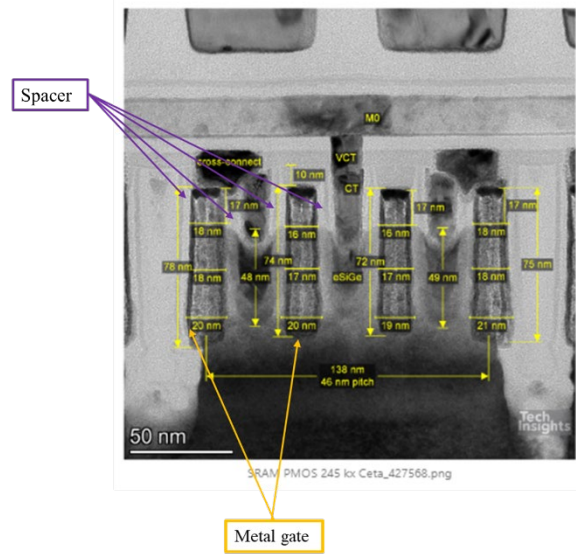
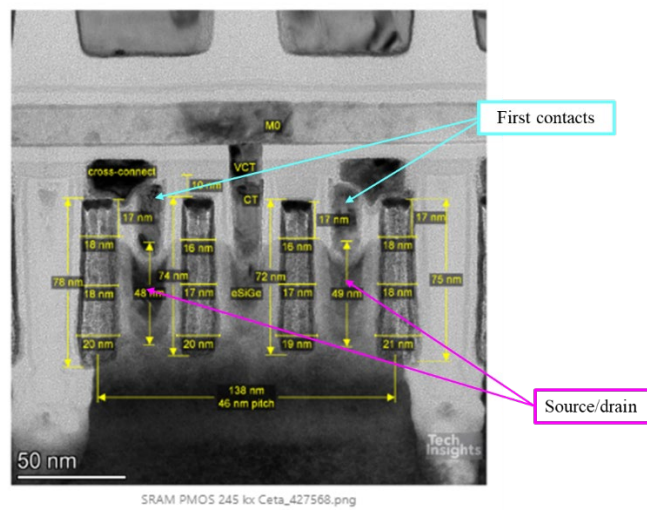
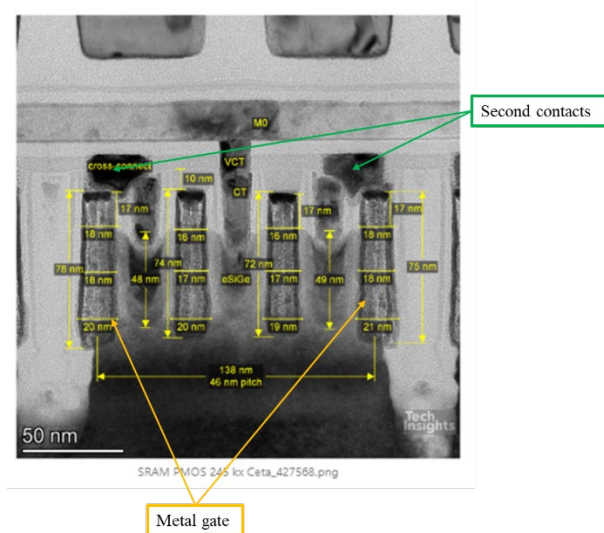
142. The infringing products include all the limitations of at least claim 1 of the '747 Patent. Specifically, the '747 Patent claims, e.g., a semiconductor structure, comprising: a substrate; a first dielectric layer disposed on the substrate; at least two metal gates disposed in the first dielectric layer; a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated

top surface; a source/drain region (S/D region) disposed between two metal gates; a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region; a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts; and a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

143. With respect to exemplary devices, the semiconductor die incorporated in the Qualcomm Snapdragon 8 Elite integrated circuit, which is incorporated in the OnePlus 13, is manufactured by TSMC using its 3nm process node. *See* NSane Forums, *Qualcomm announces Snapdragon 8 Elite flagship smartphone SoC with major improvements*, at <https://nsaneforums.com/news/mobile-news/qualcomm-announces-snapdragon-8-elite-flagship-smartphone-soc-with-major-improvements-r26125/> (accessed Feb. 13, 2025).

144. The other products produced by TSMC at the same node size also infringe for the same reasons as above, as explained in ¶ 96.

145. These exemplary devices directly infringe at least claim 1 of the '747 Patent. Specifically, the TSMC 3nm semiconductor die incorporated in the OnePlus 13 smartphone comprises all elements of claim 1 of the '747 Patent. Upon information and belief, these exemplary devices are substantially similar in materials, structures, and features as semiconductor dies that TSMC manufactures using its 3nm process node, which is representative of the exemplary devices and other semiconductor devices manufactured using TSMC's 3nm process node. Furthermore, as shown in the images below of an example semiconductor die made using TSMC's 3nm process node (a TSMC 3nm semiconductor die incorporated in the Apple A17 Pro APL1V02 integrated circuit), the example semiconductor die comprises all elements of claim 1 of the '747 Patent.



146. As a result of Defendants' infringement of the '747 Patent, Plaintiffs are entitled to

monetary damages in an amount adequate to compensate for Defendants' infringement, but in no event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

147. Defendants' acts of direct infringement of the '747 Patent are willful, and have caused and will continue to cause substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law.

COUNT V

Infringement of the '880 Patent

148. Plaintiffs incorporate the allegations of all of the foregoing paragraphs as if fully restated herein.

149. Plaintiff Marlin Semiconductor is the assignee and lawful owner of all rights, title, and interest in and to the '880 Patent. The '880 Patent is valid and enforceable.

150. The '880 Patent is entitled "Semiconductor Device and Method for Fabricating the Same," and issued on Apr. 24, 2018 to inventors Chun-Hao Lin, Hsin-Yu Chen, and Shou-Wei Hsieh. The '880 Patent issued from U.S. Patent Application No. 15/660,991, which was filed on July 27, 2017.

151. Defendants have directly and indirectly infringed, and continue to directly and indirectly infringe, the '880 Patent by making, having made, using, selling, offering for sale, and/or importing into the United States products that infringe the '880 Patent including, but not limited to semiconductor devices manufactured using TSMC's 3nm process node. The products that infringe one or more claims of the '880 Patent include, but are not limited to, at least the products identified herein. Further discovery may reveal additional infringing products and/or models.

152. For example, and without limitation, the infringing products infringe one or more claims of the '880 Patent, including but not limited to claim 1. The infringing products fall within

the scope of and include, either literally under the doctrine of equivalents, all of the elements of at least claim 1 of the '880 Patent.

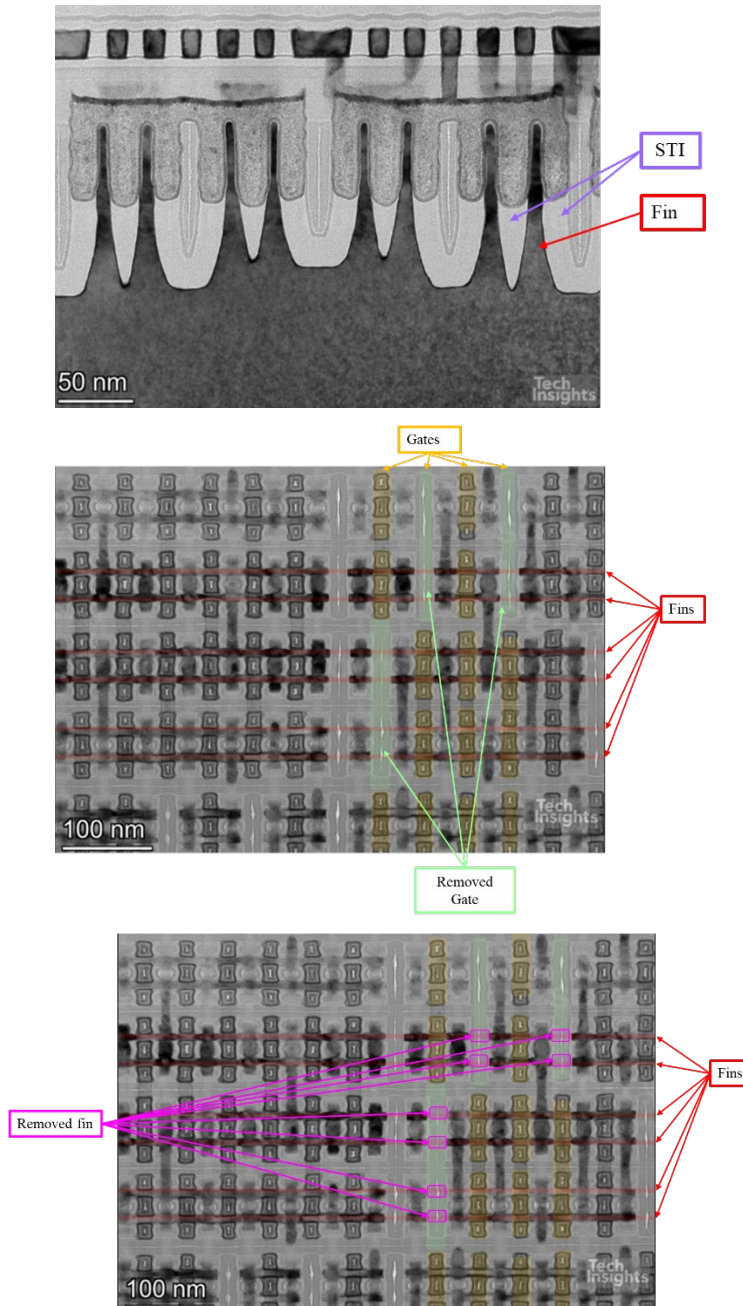
153. The infringing products include all the limitations of at least claim 1 of the '880 Patent. Specifically, the '880 Patent claims, *e.g.*, a method for fabricating semiconductor device, comprising: forming a fin-shaped structure on a substrate; forming a shallow trench isolation (STI) around the fin-shaped structure; forming a gate layer on the fin-shaped structure and the STI; removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench; forming a dielectric layer into the trench to form a single diffusion break (SDB) structure; and after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure.

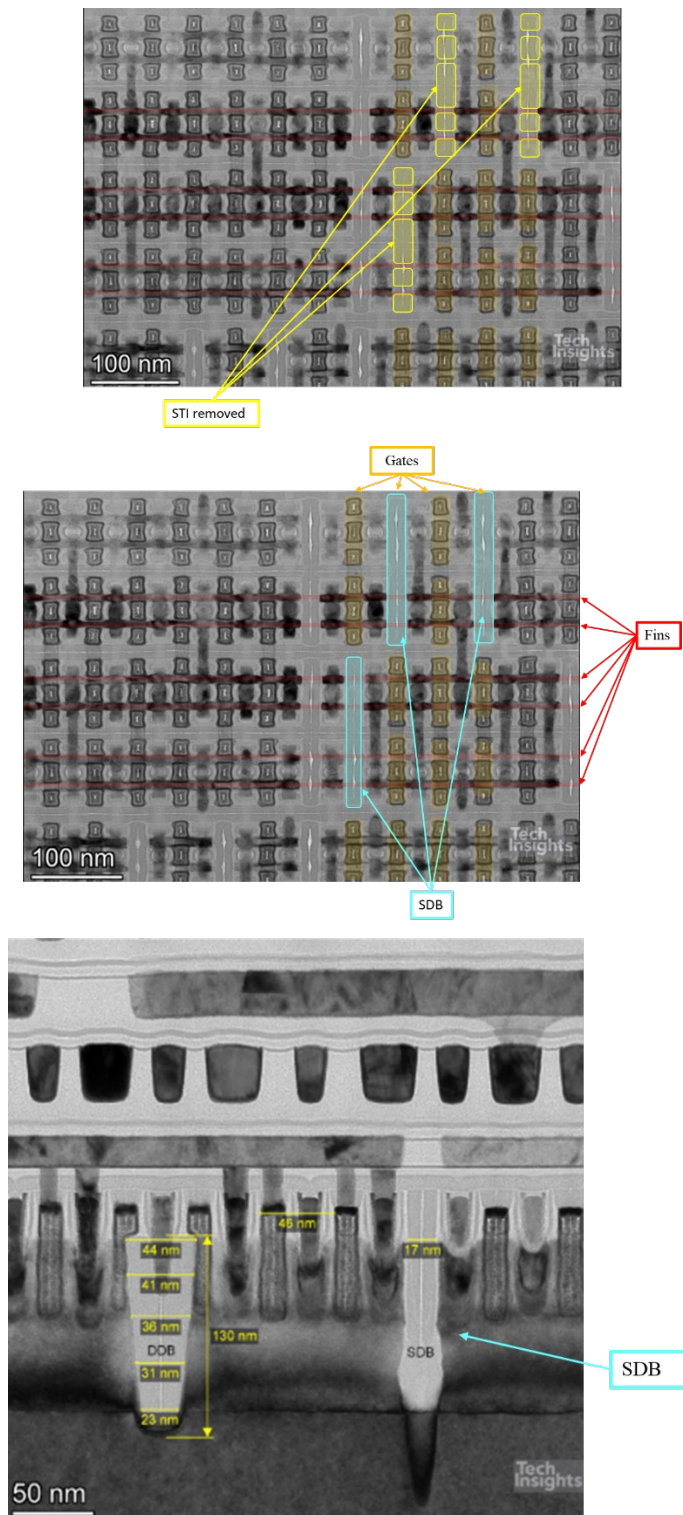
154. With respect to exemplary devices, the semiconductor die incorporated in the Qualcomm Snapdragon 8 Elite integrated circuit, which is incorporated in the OnePlus 13, is manufactured by TSMC using its 3nm process node. *See* NSane Forums, *Qualcomm announces Snapdragon 8 Elite flagship smartphone SoC with major improvements*, at <https://nsaneforums.com/news/mobile-news/qualcomm-announces-snapdragon-8-elite-flagship-smartphone-soc-with-major-improvements-r26125/> (accessed Feb. 13, 2025).

155. The other products produced by TSMC at the same node size also infringe for the same reasons as above, as explained in ¶ 96.

156. These exemplary devices directly infringe at least claim 1 of the '880 Patent. Specifically, the TSMC 3nm semiconductor die incorporated in the OnePlus 13 smartphone comprises all elements of claim 1 of the '880 Patent. Upon information and belief, these exemplary devices are substantially similar in materials, structures, and features as semiconductor dies that TSMC manufactures using its 3nm process node, which is representative of the exemplary devices and other semiconductor devices manufactured using TSMC's 3nm process node. Furthermore, as

shown in the images below of an example semiconductor die made using TSMC's 3nm process node (a TSMC 3nm semiconductor die incorporated in the Apple A17 Pro APL1V02 integrated circuit), the example semiconductor die comprises all elements of claim 1 of the '880 Patent.





157. As a result of Defendants' infringement of the '880 Patent, Plaintiffs are entitled to monetary damages in an amount adequate to compensate for Defendants' infringement, but in no

event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

158. Defendants' acts of direct infringement of the '880 Patent are willful, and have caused and will continue to cause substantial damage and irreparable harm to Plaintiffs, and Plaintiffs have no adequate remedy at law.

PRAYER FOR RELIEF

WHEREFORE, Plaintiffs request the Court grant the relief set forth below:

- a. Enter a judgment that the Defendants have directly or indirectly infringed, and continue to directly or indirectly infringe one or more claims of each of the Asserted Patents;
- b. Enter a judgment that Defendants' acts of patent infringement are willful;
- c. Order Defendants to account for and pay damages caused to Plaintiffs by Defendants' unlawful acts of patent infringement;
- d. Award Plaintiffs increased damages and attorney fees pursuant to 35 U.S.C. §§ 284 and 285;
- e. Award Plaintiffs the interest and costs incurred in action; and
- f. Grant Plaintiffs other and further relief, including equitable relief, as the Court finds just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Fed. R. Civ. P. 38, Plaintiffs hereby demand a jury trial for all claims and issues deemed to be triable by a jury.

Dated: February 13, 2025

Respectfully submitted,

/s/ Adam Rizk by permission Andrea L. Fair
Michael T. Renaud (629783MA)
Adam Rizk (688305MA)

Matthew Karambelas (*Pro hac vice*
forthcoming)
Jessica L. Perry (*Pro hac vice* forthcoming)
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Exhibit A



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Tseng et al.

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(45) **Date of Patent:** **Jun. 29, 2010**

(54) **METAL OXIDE SEMICONDUCTOR TRANSISTOR**

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(22) Filed: **Aug. 9, 2007**

(57) **ABSTRACT**

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H01L 31/109 (2006.01)

H01L 31/0328 (2006.01)

H01L 31/0336 (2006.01)

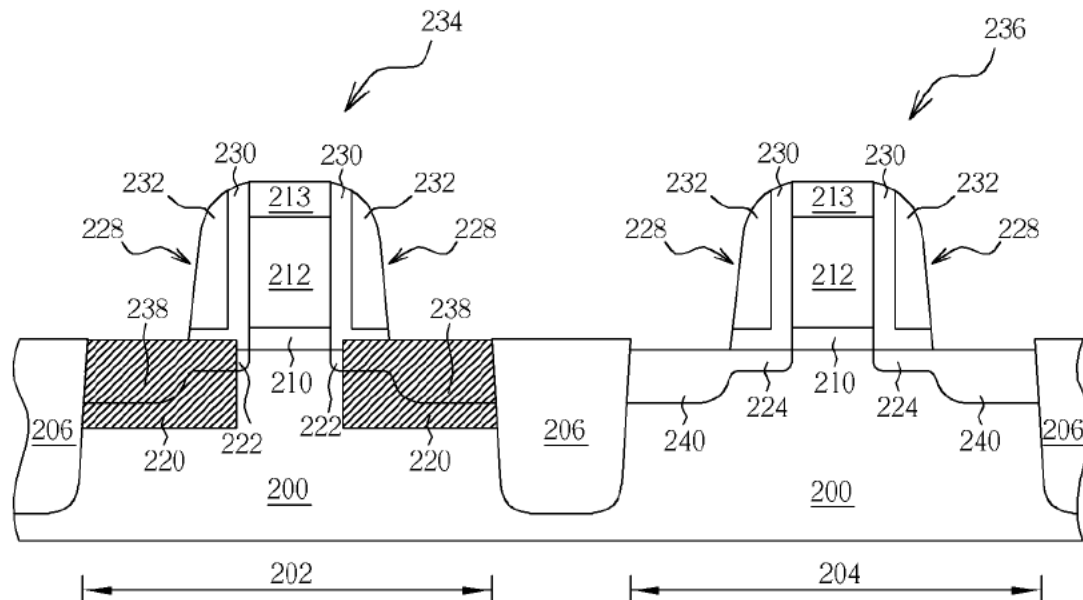
(52) **U.S. Cl.** **257/190**; 438/218; 438/285

(58) **Field of Classification Search** 257/19, 257/190, 192, 197; 438/218, 285

See application file for complete search history.

The present invention provides a method for fabricating a metal oxide semiconductor transistor. First, a semiconductor substrate is provided and at least a gate is formed on the semiconductor substrate. A protective layer is then formed on the semiconductor substrate and the gate. Subsequently, at least a recess is formed in the semiconductor substrate adjacent to the gate, and then an epitaxial layer is formed in the recess. A lightly doped region is formed in the semiconductor substrate adjacent to the gate. Finally, a spacer is formed on the sidewall of the gate.

11 Claims, 14 Drawing Sheets



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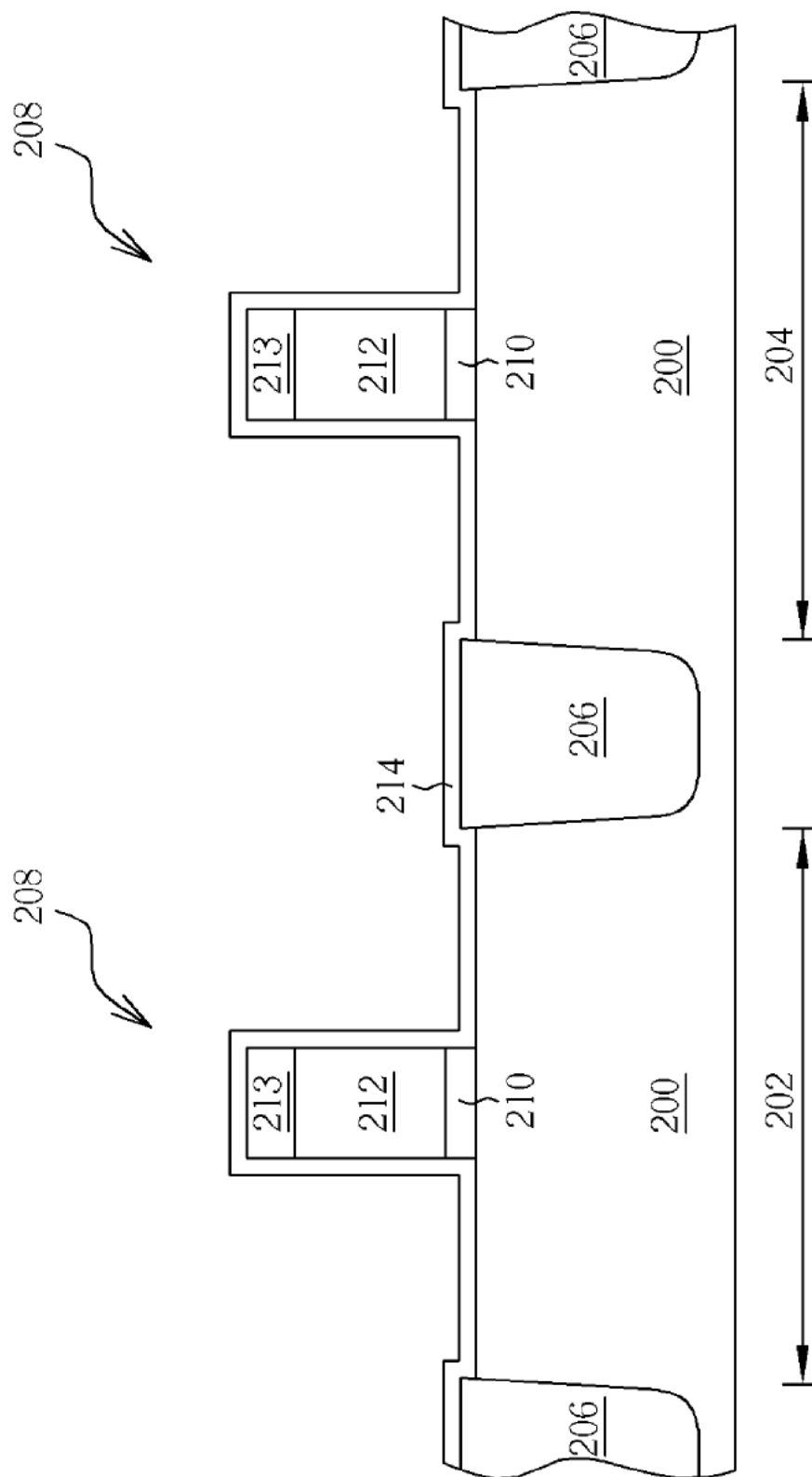


Fig. 1

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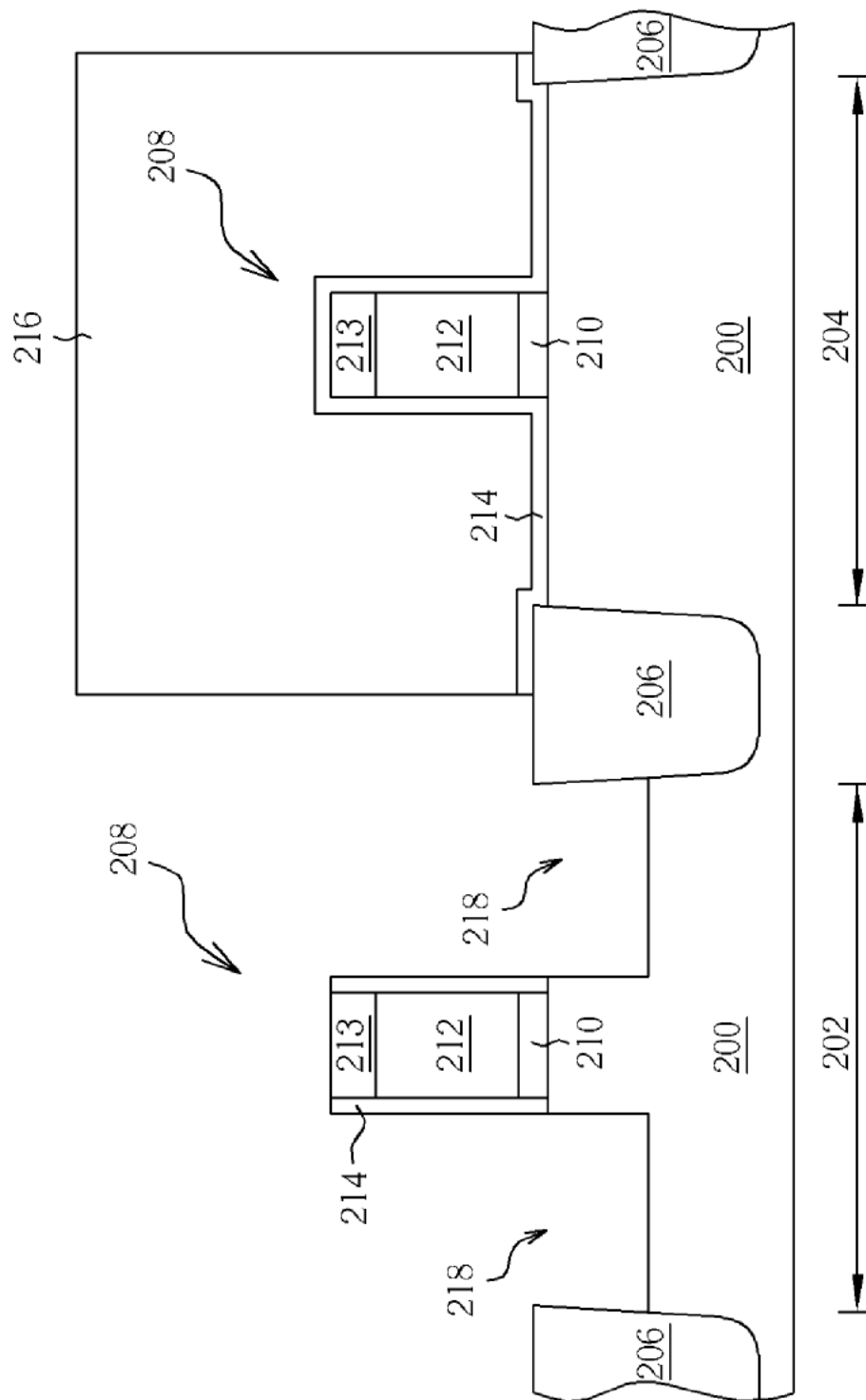


Fig. 2

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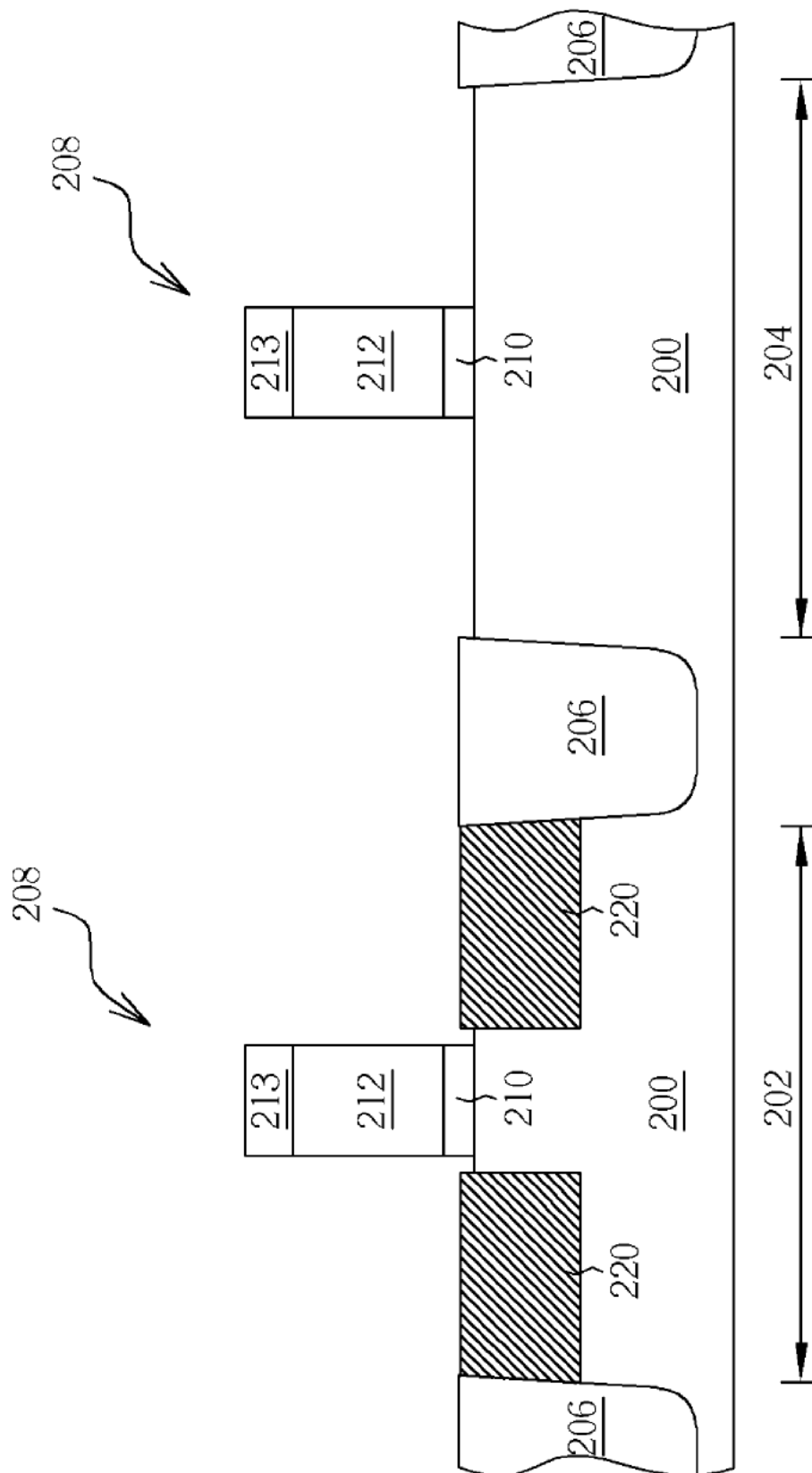


Fig. 3

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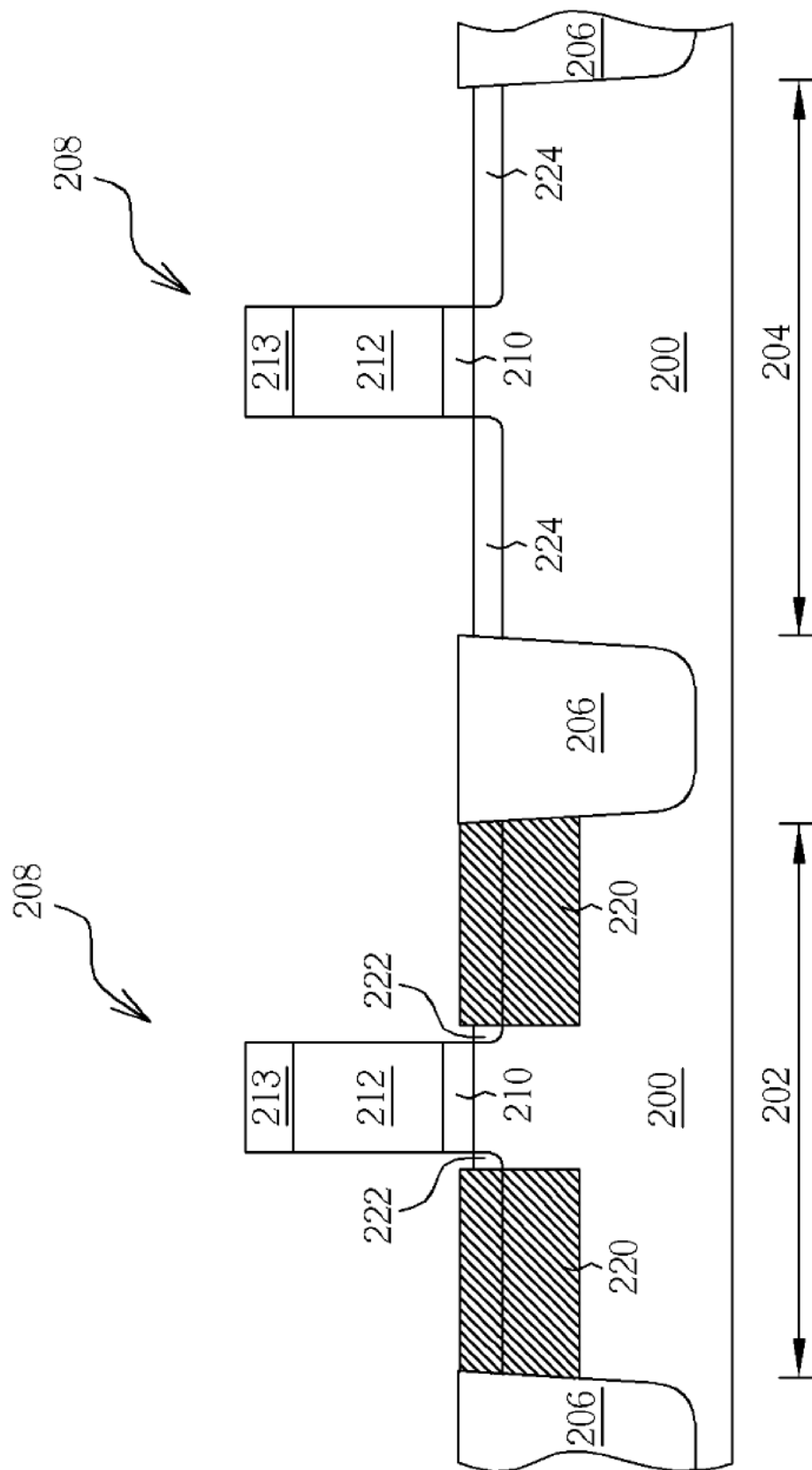


Fig. 4

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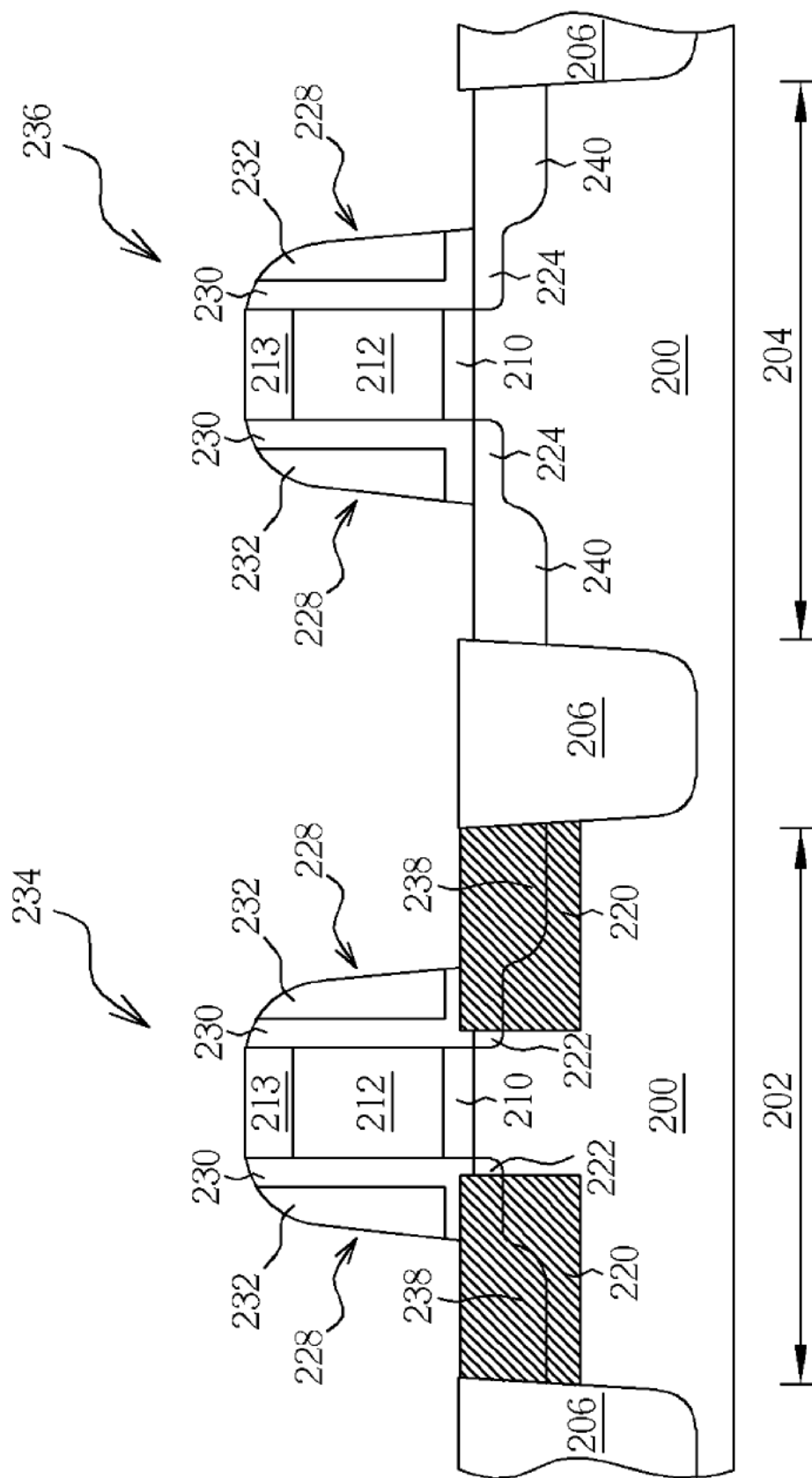


Fig. 5

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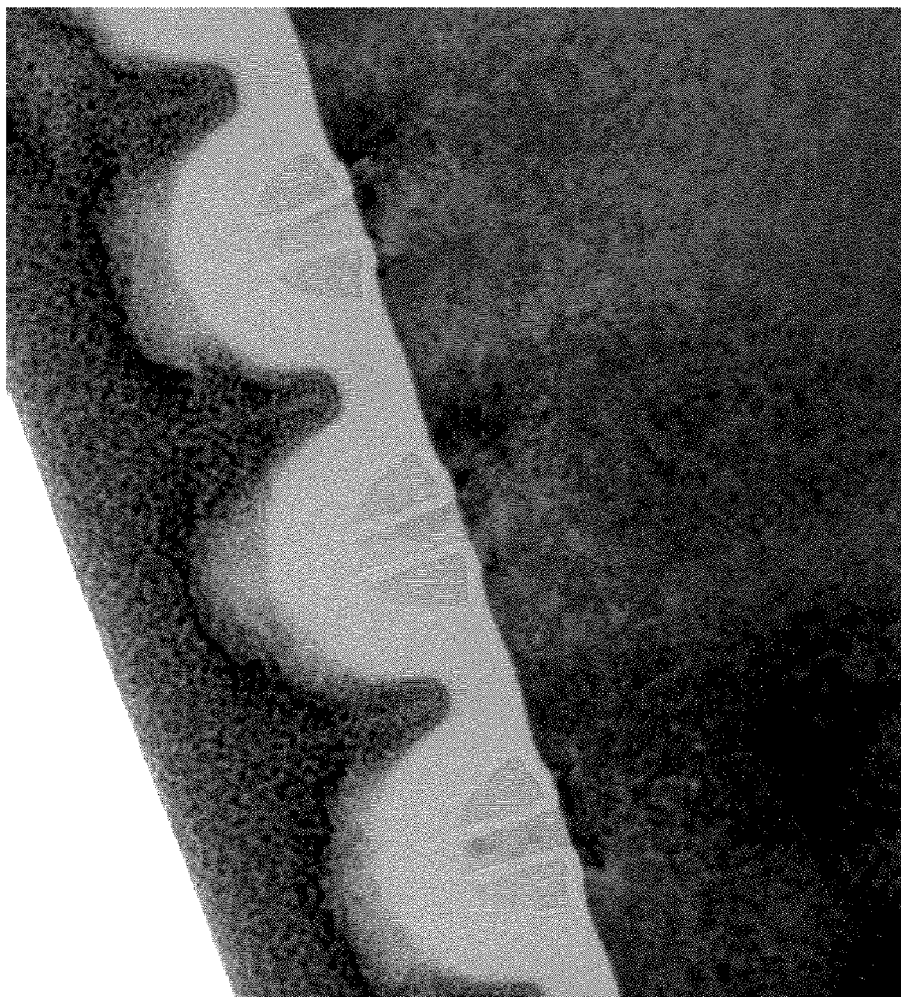


Fig. 6

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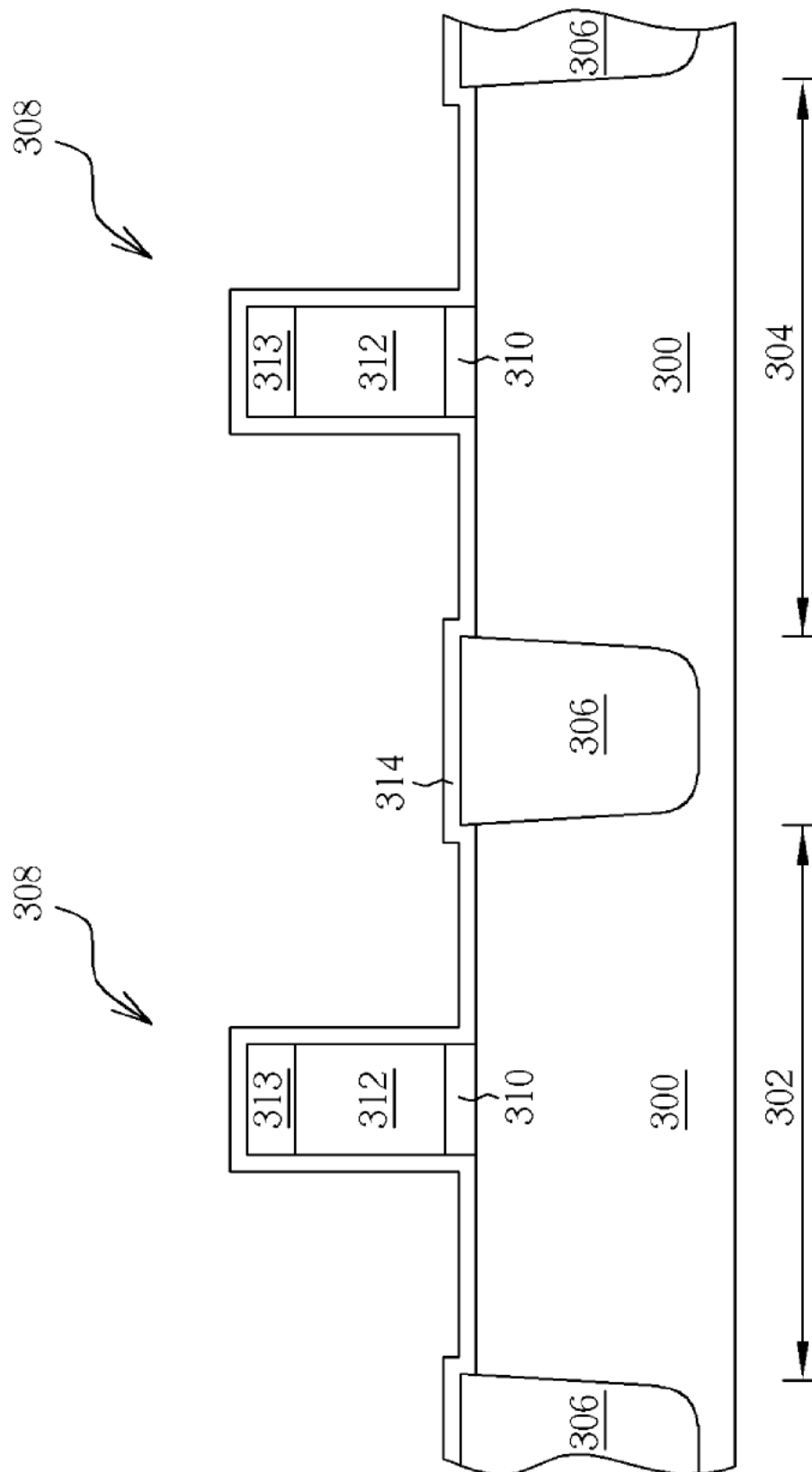


Fig. 7

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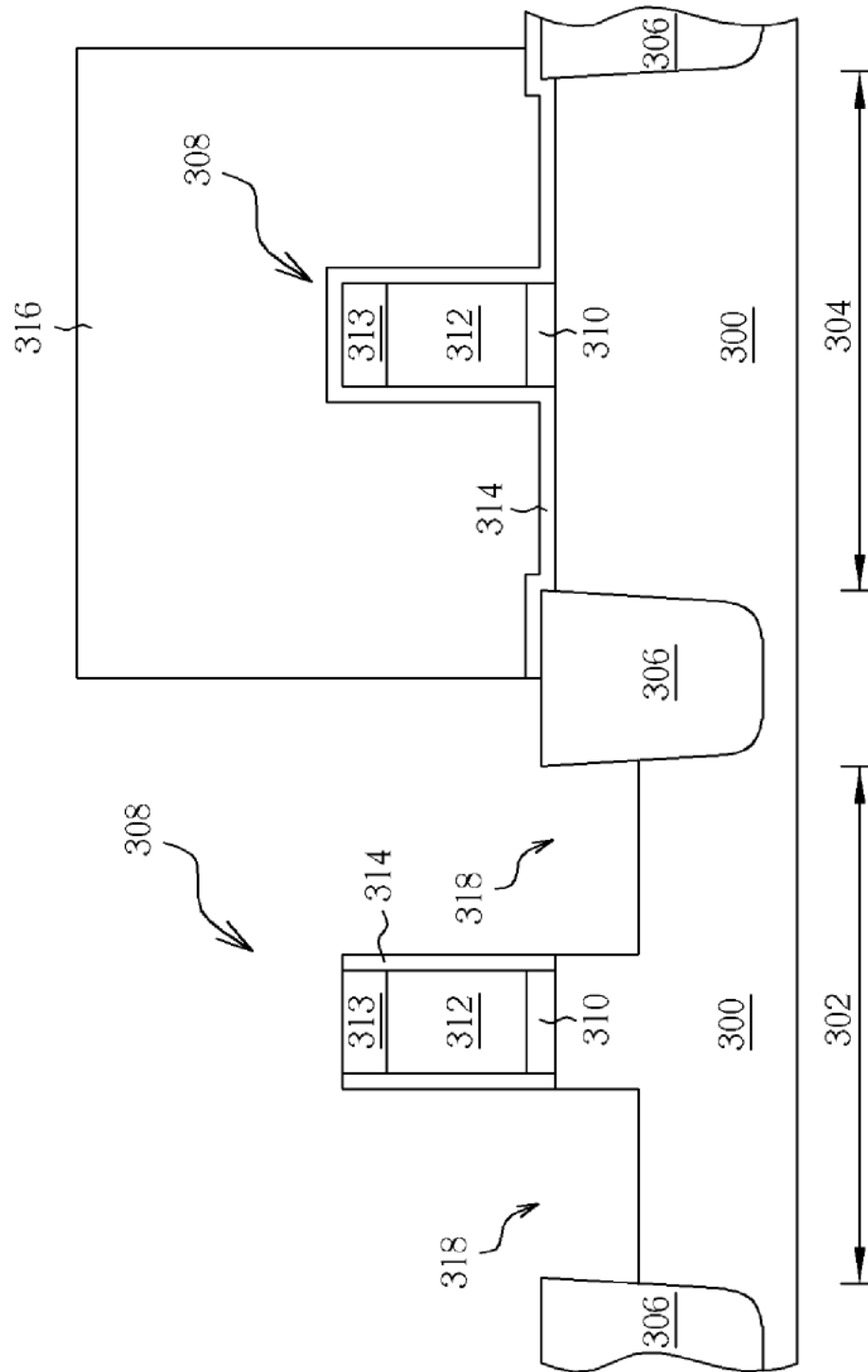


Fig. 8

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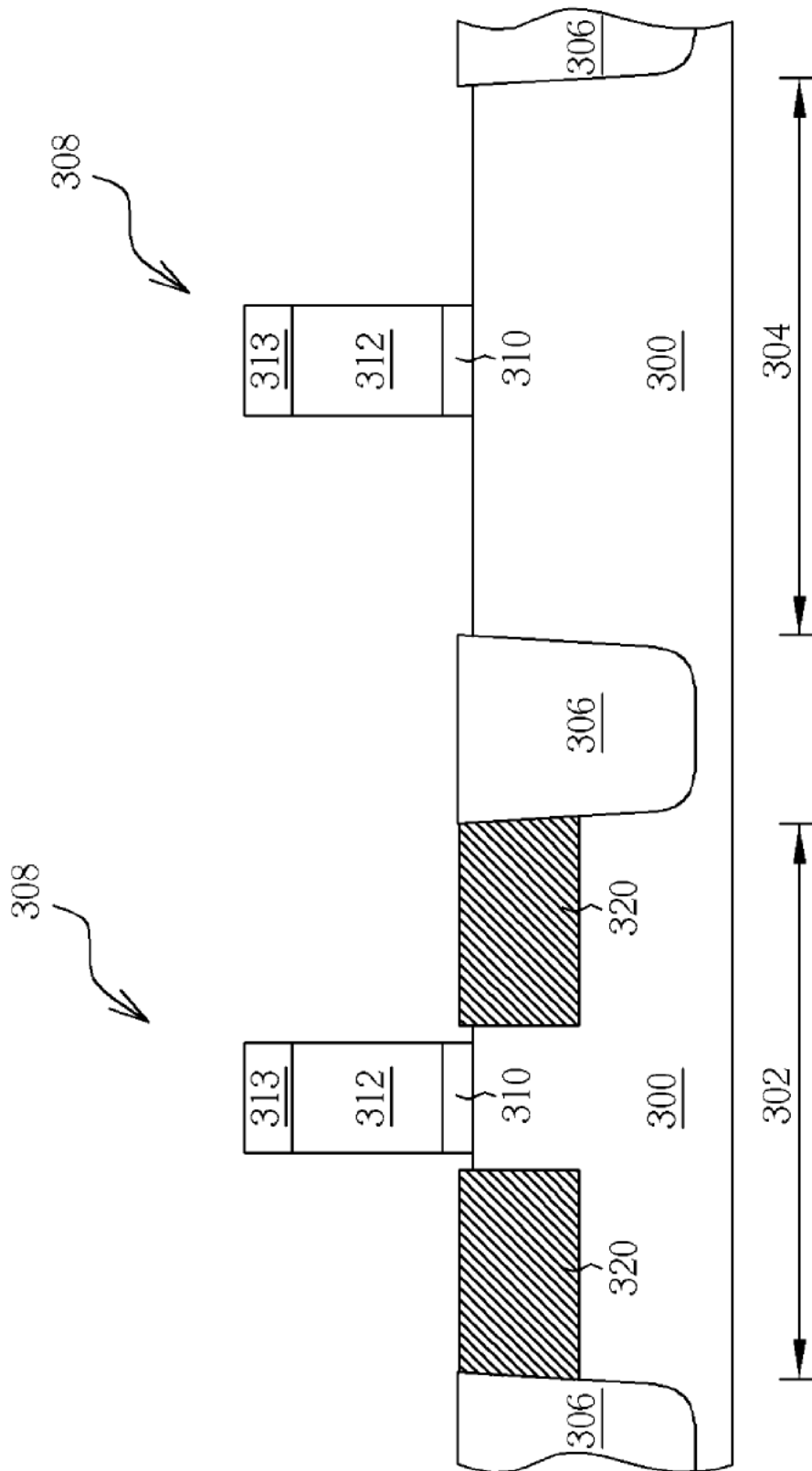


Fig. 9

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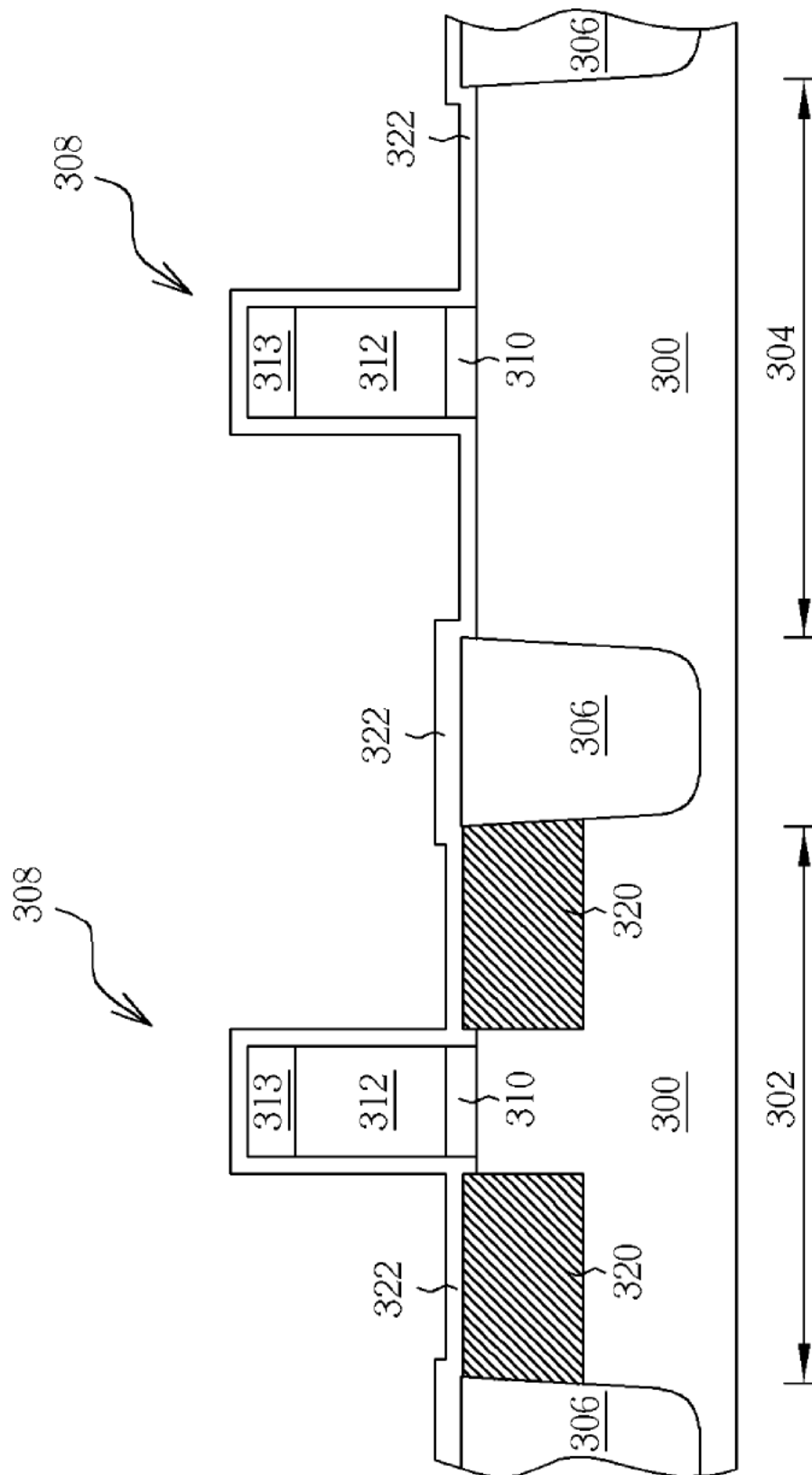


Fig. 10

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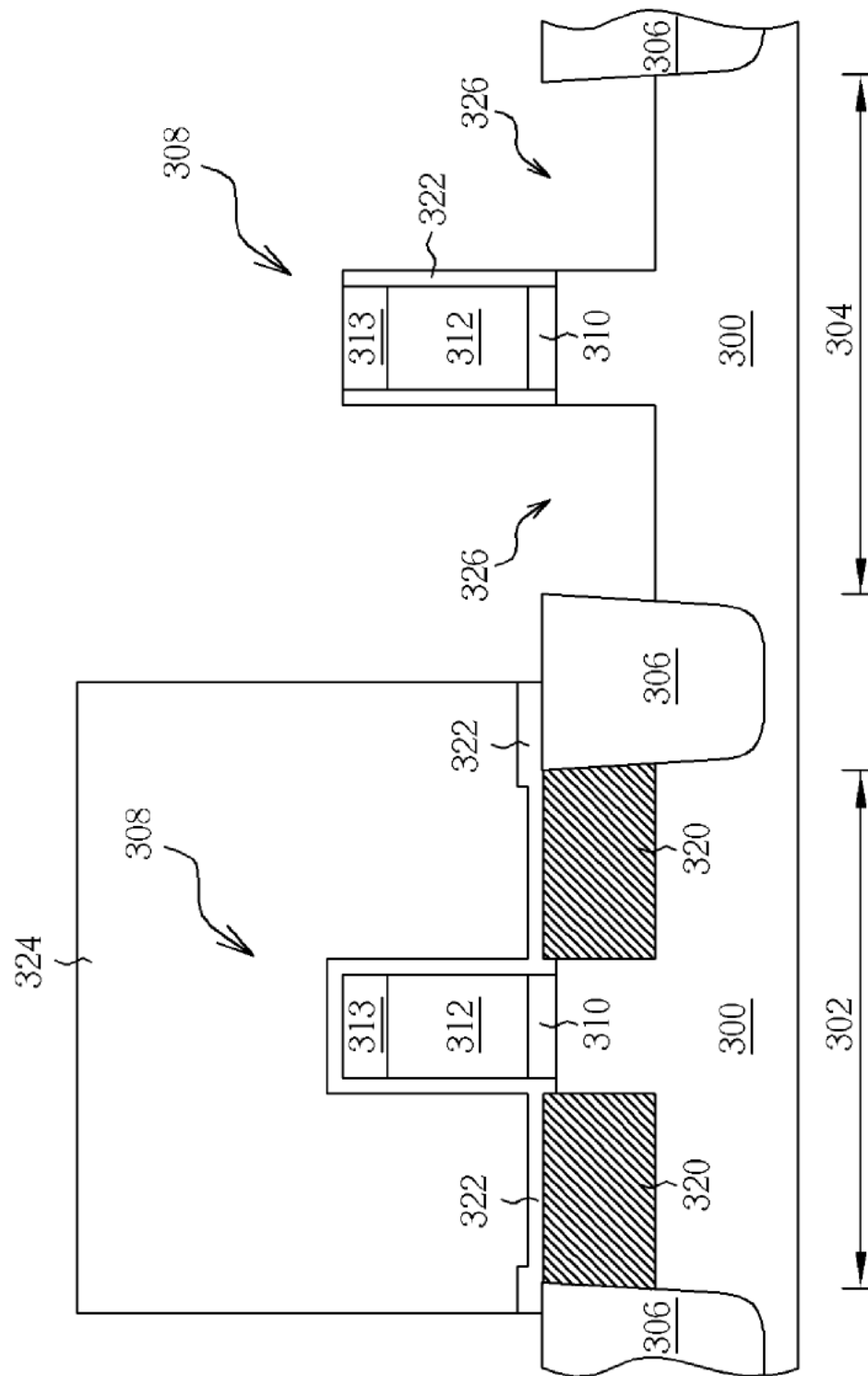


Fig. 11

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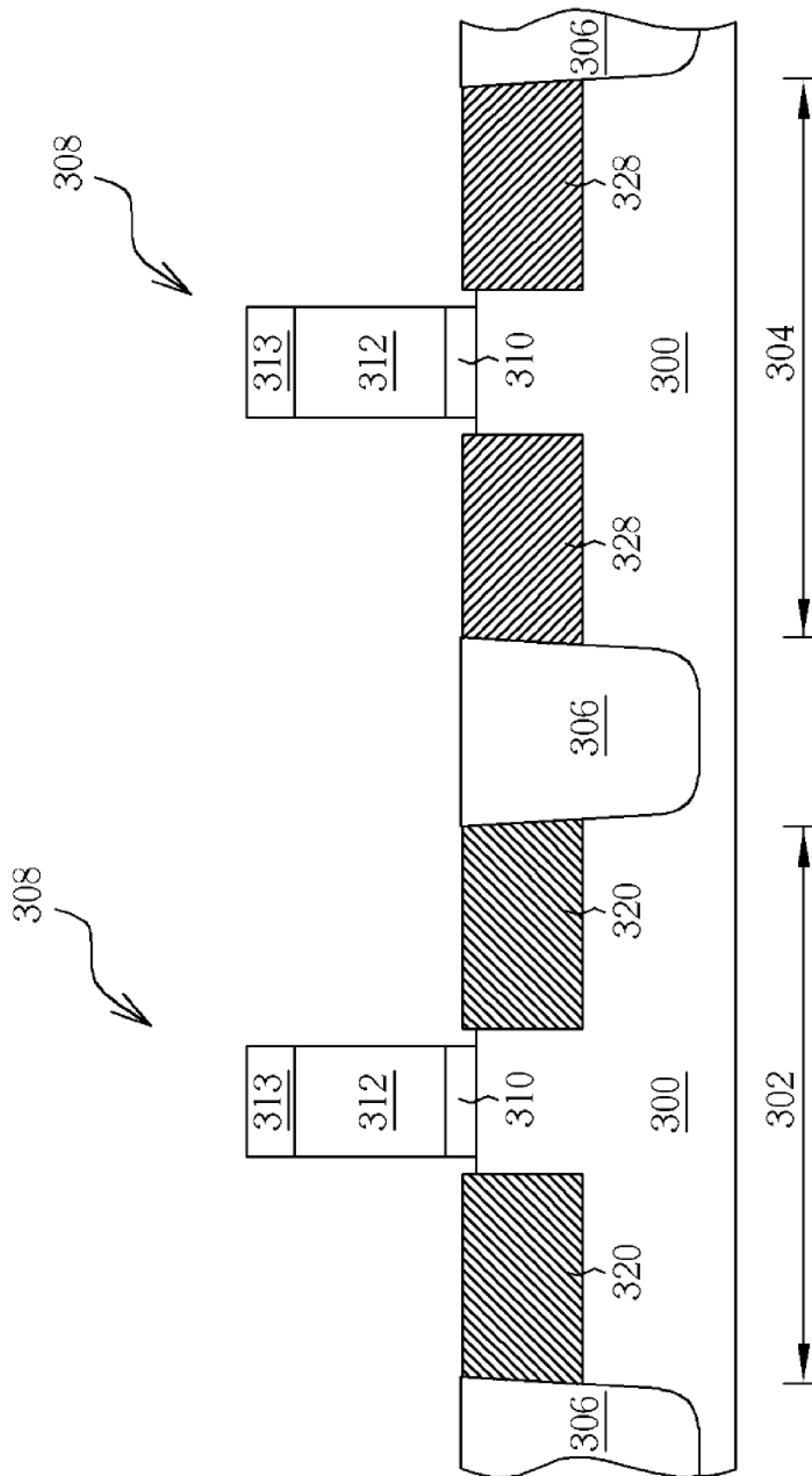


Fig. 12

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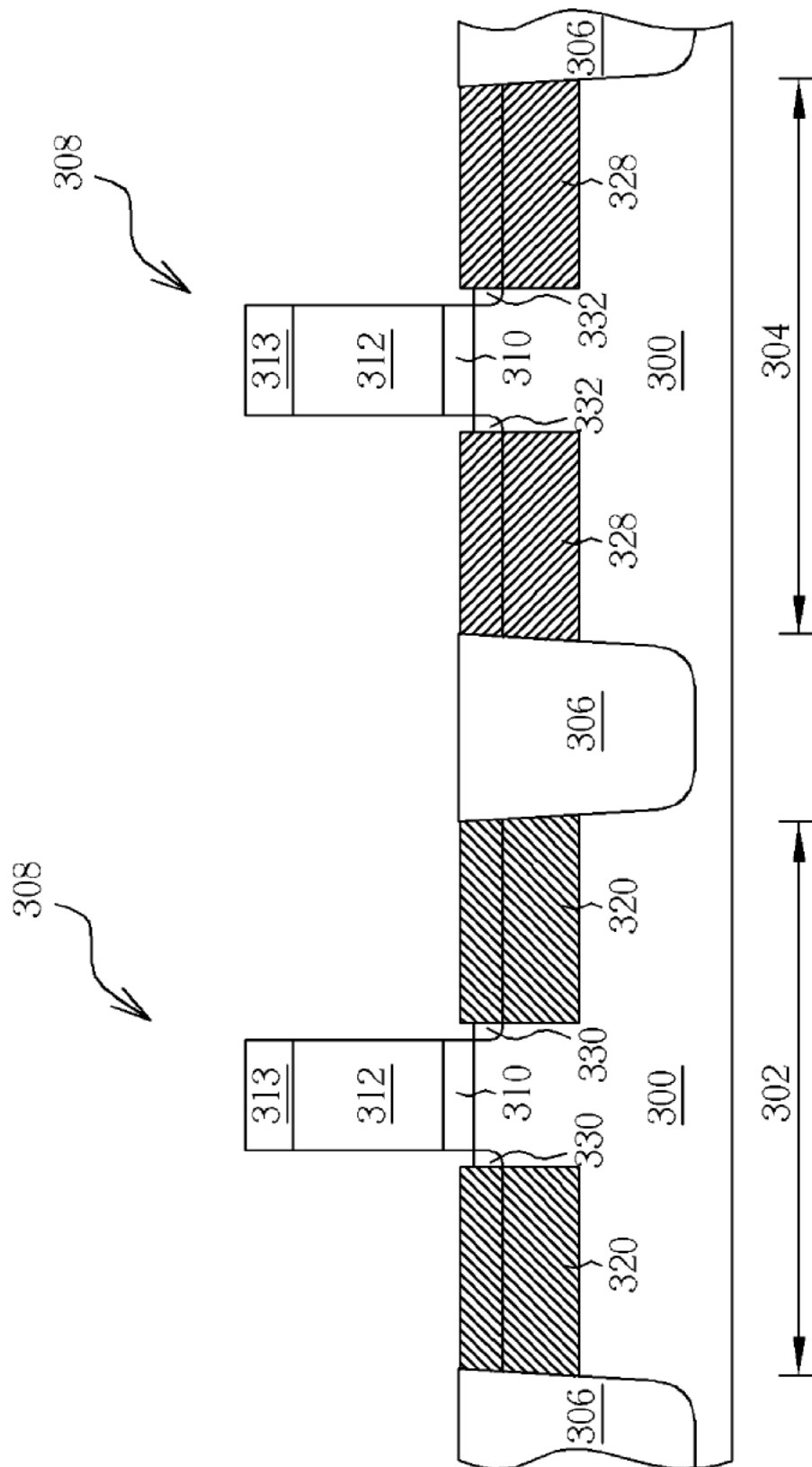


Fig. 13

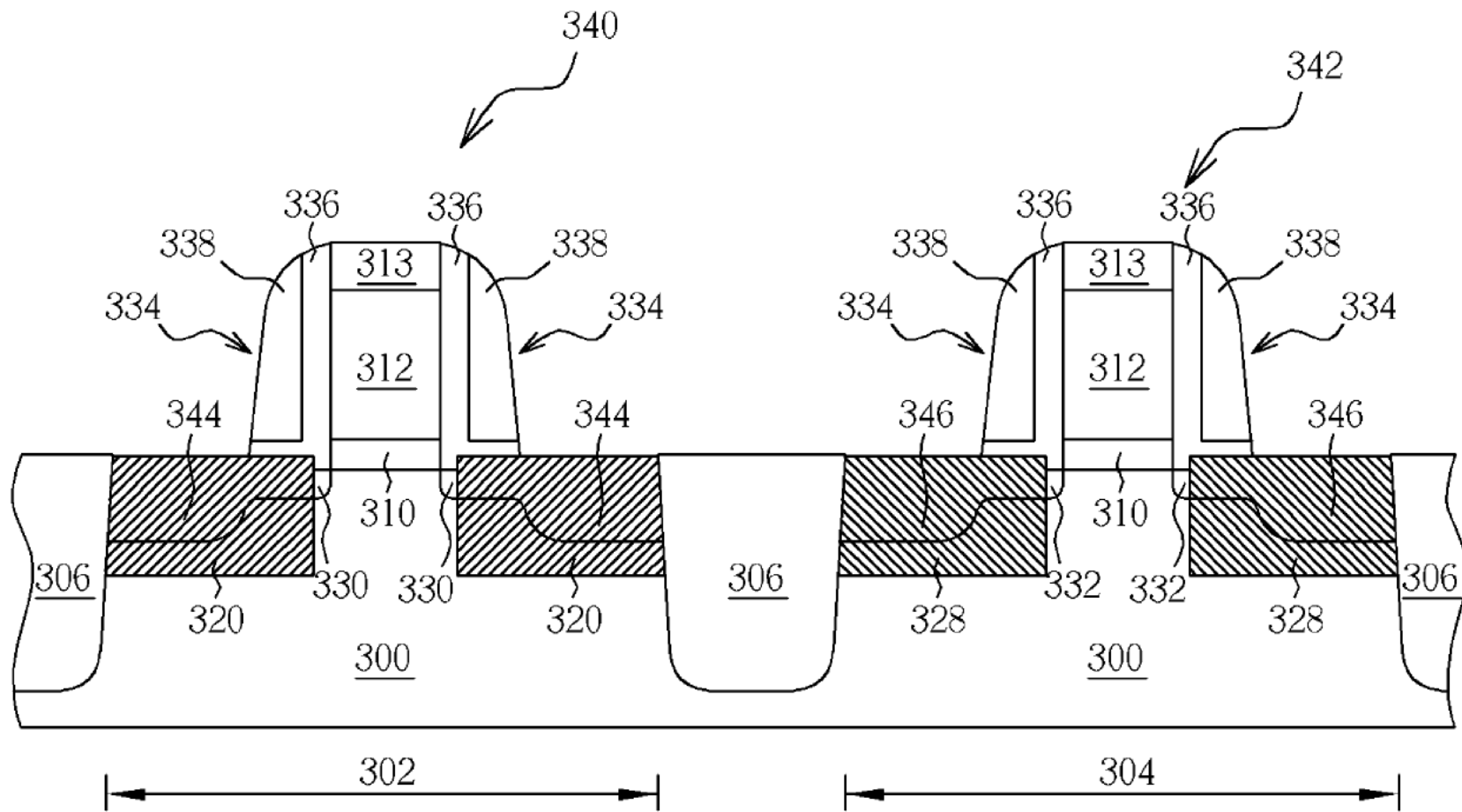


Fig. 14

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METAL OXIDE SEMICONDUCTOR TRANSISTOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for fabricating a metal oxide semiconductor (MOS) transistor, and more particularly, to a method for fabricating a strained silicon channel MOS transistor.

2. Description of the Prior Art

A conventional MOS transistor generally includes a semiconductor substrate, such as silicon, a source region, a drain region, a channel positioned between the source region and the drain region, and a gate located above the channel. The gate composed of a gate dielectric layer, a gate conductive layer positioned on the gate dielectric layer, and spacers positioned on the sidewalls of the gate conductive layer. Generally, for a given electric field across the channel of a MOS transistor, the amount of current that flows through the channel is directly proportional to a mobility of the carriers in the channel. Therefore, how to improve the carrier mobility so as to increase the speed performance of MOS transistors has become a major topic for study in the semiconductor field.

One way to increase the mobility of the carriers in the channel of an MOS transistor is to produce a mechanical stress in the channel. A compressive strained channel, such as a silicon germanium (SiGe) channel layer grown on silicon, has significant hole mobility enhancement. A tensile strained channel, such as a thin silicon channel layer grown on silicon germanium, achieves significant electron mobility enhancement. Another prior art method of obtaining a strained channel is to epitaxially grow a SiGe layer adjacent to the spacers within the semiconductor substrate after forming the spacer.

In this type of MOS transistor, a biaxial tensile strain occurs in the epitaxial silicon layer due to the silicon germanium, which has a larger lattice constant than silicon, and, as a result, the band structure alters, and the carrier mobility increases. This enhances the speed performance of the MOS transistor.

The performance of MOS transistors has increased year after year with the diminution of critical dimensions and the advance of very large scale integrated circuits (VLSI); therefore, the demand for the speed performance of the MOS transistor has also greatly increased. However, the compressive or tensile stress obtained according to the conventional method has been hardly achieved the required extent.

Accordingly, the applicants provide a method of fabricating strained silicon channel MOS transistors to improve the shortages from the prior art, and then increase the carrier mobility of MOS transistors.

SUMMARY OF THE INVENTION

The present invention relates to a method of fabricating a MOS transistor, and more particularly, to a method of fabricating a strained silicon channel MOS transistor to improve the disadvantages of the prior art.

According to the claims, the present invention provides a method of fabricating a MOS transistor, the method comprising providing a semiconductor substrate; forming at least a gate on the semiconductor substrate; forming a protective layer on the semiconductor substrate, and the protective layer covering the surface of the gate; forming at least a recess within the semiconductor substrate adjacent to the gate; forming an epitaxial layer in the recess; forming a lightly doped

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region within the semiconductor substrate adjacent to the gate; and forming a spacer on the sidewall of the gate.

According to the claims, the present invention provides another method for fabricating a CMOS transistor, the method comprising providing a semiconductor substrate having at least a first conductive transistor area for fabricating first conductive transistors and at least a second conductive transistor area for fabricating second conductive transistors, and an isolation structure between the first conductive transistor area and the second conductive transistor area; forming a gate on the first conductive transistor area and on the second conductive transistor area respectively; forming a first protective layer on the semiconductor substrate, and the first protective layer covering the surface of each gate; forming at least a first recess within the semiconductor substrate adjacent to the gate in the first conductive transistor area; forming a first epitaxial layer in the recess; forming a first ion lightly doped region within the semiconductor substrate adjacent to the gate in the first conductive transistor area; and forming a spacer on the sidewall of each gate.

According to the claims, the present invention further provides a MOS transistor structure, the structure comprising a gate formed on a semiconductor substrate; two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate; a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layer; and two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 to FIG. 5 are cross-sectional diagrams, illustrating a fabricating method of MOS transistors in accordance with the first preferred embodiment of the present invention.

FIG. 6 shows a transmission electron microscopy picture of MOS transistors in accordance with the first preferred embodiment of the present invention.

FIG. 7 to FIG. 14 are cross-sectional diagrams, illustrating a fabricating method of MOS transistors in accordance with the second preferred embodiment of the present invention.

DETAILED DESCRIPTION

Please refer to FIG. 1 to FIG. 5, which are cross-sectional diagrams illustrating a method for fabricating a MOS transistor in accordance with the first preferred embodiment of the present invention. For highlighting the characteristic of the present invention and for clarity of illustration, FIG. 1 to FIG. 5 merely show a first conductive transistor area and a second conductive transistor area. As shown in FIG. 1, a semiconductor substrate **200** is provided such as a silicon substrate or a silicon-on-insulator (SOI) substrate, but not limited thereto. The semiconductor substrate **200** comprises a plurality of first conductive transistor areas **202** and a plurality of second conductive transistor areas **204**, and the first conductive transistor areas **202** and the second conductive transistor areas **204** are isolated by isolation structures such as shallow trench isolations (STI) **206**. Generally speaking, the STI **206** is formed by etching a trench in the semiconductor substrate **200** and then filling the trench with insulating materials such as silicon oxide. Besides, the semiconductor substrate **200**

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further comprises a plurality of gates **208**, positioned respectively on each first conductive transistor area **202** and each second conductive transistor area **204**. Each gate **208** comprises a dielectric layer **210**, a conductive layer **212** positioned on the dielectric layer **210** and a cap layer **213** positioned on the conductive layer **212**. In general, the dielectric layer **210** comprises isolating materials such as silicon oxide components or silicon nitride components, etc; the conductive layer **212** comprises conductive materials such as polysilicon or metal silicide; and the cap layer **213** comprises dielectric materials such as silicon nitride.

Subsequently, a protective layer **214** is formed on the semiconductor substrate **200**, and the protective layer **214** covers the surface of each gate **208**. According to the first preferred embodiment of the present invention, the protective layer **214** may comprise any materials with an appropriate etching selectivity to the semiconductor substrate **200** and the conductive layer **212**: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The protective layer **214** has a thickness of about 150 to 250 Å, and is preferably about 200 Å.

As shown in FIG. 2, a patterned mask **216** is coated on the second conductive transistor area **204** and a portion of the STI **206**. An etching process such as an anisotropic dry etching is then carried out to etch recesses **218** in the first conductive transistor area **202**. Thereafter, the patterned mask **216** is removed.

As shown in FIG. 3, after a pre-cleaning step is performed to clean the semiconductor substrate **200** of the first conductive transistor area **202**, such as using DHF solution or SPM solution to remove impurities upon the surface of the recesses **218**, an epitaxial growth process is carried out to form epitaxial layers **220** in the recesses **218**. Then, the protective layer **214** is removed. The epitaxial layer **220** is grown in the recess **218** and it may be grown higher than the surface of the semiconductor substrate **200**, so as to form a raised epitaxial layer **220**. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the first preferred embodiment of the present invention, when the first conductive transistor area **202** is a PMOS transistor area, the epitaxial layer **220** is composed of SiGe. And when the first conductive transistor area **202** is an NMOS transistor, the epitaxial layer **220** is composed of SiC.

As shown in FIG. 4, a patterned mask (not shown) is coated on the second conductive transistor area **204**. A first ion lightly doped process is carried out to form a first ion lightly doped region **222** in the first conductive transistor area **202**. Then the patterned mask is removed. Thereafter, another patterned mask (not shown) is coated on the first conductive transistor area **202**. A second ion lightly doped process is then carried out to form a second ion lightly doped region **224** in the second conductive transistor area **204**. Then the patterned mask is removed.

As shown in FIG. 5, spacers **228** are formed on the sidewalls of each gate **280**. According to the first preferred embodiment of the present invention, each spacer **228** comprises an oxide liner **230** and a nitride spacer **232**. The spacers **228** cover the sidewalls of each gate **208** and also extend laterally onto the first ion lightly doped region **222** and the second ion lightly doped region **224**. Each spacer **228** may also comprise an offset spacer (not shown) positioned between the gate **208** and the oxide liner **230**. Because each spacer **228** in the first conductive transistor area **202** lies over the raised epitaxial layer **220**, thus each spacer **228** in the first conductive transistor area **202** is tilted upward. Please refer to FIG. 10, which is a transmission electron microscopy (TEM)

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picture of the MOS transistors in accordance with the first preferred embodiment of the present invention.

Finally, a patterned mask (not shown) is coated on the second conductive transistor area **204**. A first ion source/drain implantation process is then carried out to form a first ion source/drain region **238** in the first conductive transistor area **202**; thereby a first conductive transistor **234** such as a PMOS transistor is formed in the first conductive transistor area **202**. Thereafter, the patterned mask is removed. Subsequently, another patterned mask (not shown) is coated on the first conductive transistor area **202**. A second ion source/drain implantation process is carried out to form a second ion source/drain region **240** in the second conductive transistor area **204**; thereby a second conductive transistor **236** such as an NMOS transistor is formed in the second conductive transistor area **204**. Thereafter, the patterned mask is removed.

It should be noticed that the process of forming the source/drain regions **238** as shown in FIG. 5 is an optional step depending on the method used in the epitaxial growth process. Because the epitaxial growth process as shown in FIG. 3 may be an in-situ doped epitaxial growth process, therefore, while the epitaxial layer **200** is formed, the demanded doped ions can also be implanted into the semiconductor substrate **200** or the grown epitaxial layer **200**, as a result, the corresponding source/drain regions are formed. Thus, the source/drain implantation process as shown in FIG. 5 can be skipped. According to the first preferred embodiment of the present invention, when the first conductive transistor area **202** is a PMOS transistor area, the epitaxial growth process, which is carried out to form the epitaxial layer **220** composed of silicon germanium, may be an in-situ doped boron epitaxial growth process. Accordingly, the corresponding source/drain regions are formed by implanting the demanded boron ions within the semiconductor substrate **200** while the epitaxial layer **220** is formed.

Please refer to FIG. 7 to FIG. 14, which are cross-sectional diagrams illustrating a method for fabricating a MOS transistor in accordance with the second preferred embodiment of the present invention. For highlighting the characteristic of the present invention and for clarity of illustration, FIG. 7 to FIG. 14 merely show a first conductive transistor area and a second conductive transistor area. As shown in FIG. 7, a semiconductor substrate **300** is provided such as a silicon substrate or a silicon-on-insulator (SOI) substrate, but not limited thereto. The semiconductor substrate **300** comprises a plurality of first conductive transistor areas **302** and a plurality of second conductive transistor areas **304**, and the first conductive transistor areas **302** and the second conductive transistor areas **304** are isolated by isolation structures such as shallow trench isolations (STI) **306**. Generally speaking, STI **306** is formed by etching a trench in the semiconductor substrate **300** and then filling the trench with insulating materials such as silicon oxide. Besides, the semiconductor substrate **300** further comprises a plurality of gates **308**, positioned respectively on each first conductive transistor area **302** and each second conductive transistor area **304**. Each gate **308** comprises a dielectric layer **310**, a conductive layer **312** positioned on the dielectric layer **310** and a cap layer **313** positioned on the conductive layer **312**. In general, the dielectric layer **310** comprises isolating materials such as silicon oxide components or silicon nitride components, etc; the conductive layer **312** comprises conductive materials such as polysilicon or metal silicide; and the cap layer **313** comprises dielectric materials such as silicon nitride.

Subsequently, a first protective layer **314** is formed on the semiconductor substrate **300**, and the first protective layer **314** covers the surface of each gate **308**. According to the

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second preferred embodiment of the present invention, the first protective layer 314 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 300 and the conductive layer 312: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The first protective layer 314 has a thickness of about 150 to 250 Å, and is preferably about 200 Å.

As shown in FIG. 8, a first patterned mask 316 is coated on the second conductive transistor area 304 and a portion of the STI 306. An etching process such as an anisotropic dry etching is carried out to form first recesses 318 in the first conductive transistor area 302. Thereafter, the first patterned mask 316 is removed.

As shown in FIG. 9, after a pre-cleaning step is performed to clean the semiconductor substrate 300 of the first conductive transistor area 302, such as using DHF solution or SPM solution to remove impurities upon the surface of the first recesses 318, an epitaxial growth process is carried out to form first epitaxial layers 320 in the first recesses 318. Then, the first protective layer 314 is removed. The first epitaxial layer 320 is grown in the first recess 318 and it may be grown higher than the surface of the semiconductor substrate 300, so as to form a raised epitaxial layer. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the second preferred embodiment of the present invention, when the first conductive transistor area 302 is a PMOS transistor area, the first epitaxial layer 320 is composed of SiGe.

As shown in FIG. 10, a second protective layer 322 is formed on the semiconductor substrate 300 and the second protective layer 322 covers the surface of each gate 308. According to the second preferred embodiment of the present invention, the second protective layer 322 may comprise any materials with an appropriate etching selectivity to the semiconductor substrate 300 and the conductive layer 312: silicon nitride component, for instance, but not limited thereto. Silicon oxide component may also be used, but the effect of using silicon nitride is better. The second protective layer 322 has a thickness of about 150 to 250 Å, and is preferably about 200 Å.

As shown in FIG. 11, a second patterned mask 324 is coated on the first conductive transistor area 302 and a portion of the STI 306. An etching process such as an anisotropic dry etching is carried out to form second recesses 326 in the second conductive transistor area 304. Thereafter, the second patterned mask 324 is removed.

It should be noticed that the steps of forming the second recess 326 shown in FIG. 10 to FIG. 11 might be performed without using the second protective layer 322. Namely, after forming the first epitaxial layer 320 as shown in FIG. 9, the first protective layer 314 is not removed and then the second patterned mask 324 is coated directly on the first conductive transistor area 302 and a portion of the STI 306. Subsequently, an etching process such as that shown in FIG. 11 is carried out to form the second recesses 326 in the second conductive transistor area 304. Thereafter, the second patterned mask 324 and the first protective layer 314 are removed. Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention.

As shown in FIG. 12, after a pre-cleaning step is performed to clean the semiconductor substrate 300 of the second conductive transistor area 304, such as using DHF solution or SPM solution to remove impurities upon the surface of the second recesses 326, an epitaxial growth process is carried out to form second epitaxial layers 328 in the second recesses

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326. Then, the second protective layer 322 is removed. The second epitaxial layer 328 is grown in the second recess 326 and it may be grown higher than the surface of the semiconductor substrate 300, so as to form a raised epitaxial layer. Besides, the epitaxial growth process may be an in-situ doped ion epitaxial growth process. According to the second preferred embodiment of the present invention, when the second conductive transistor area 304 is an NMOS transistor area, the second epitaxial layer 328 is composed of SiC. It should be noticed that the process of forming the first epitaxial layer 320 as shown in FIG. 7 to FIG. 9 might be performed after the process of forming the second epitaxial layer 328 as shown in FIG. 10 to FIG. 12. Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention.

As shown in FIG. 13, a patterned mask (not shown) is coated on the second conductive transistor area 304. A first ion lightly doped process is carried out to form a first ion lightly doped region 330 in the first conductive transistor area 302. Then the patterned mask is removed. Thereafter, another patterned mask (not shown) is coated on the first conductive transistor area 302. A second ion lightly doped process is then carried out to form a second ion lightly doped region 332 in the second conductive transistor area 304. Then the patterned mask is removed.

As shown in FIG. 14, spacers 334 are formed on the sidewalls of each gate 308. According to the second preferred embodiment of the present invention, each spacer 334 comprises an oxide liner 336 and a nitride spacer 338. The spacers 334 cover the sidewalls of each gate 308 and extend laterally onto the first ion lightly doped region 330 and the second ion lightly doped region 332. The spacers 334 also cover a portion of the first epitaxial layer 320 and a portion of the second epitaxial layer 328. Additionally, each spacer 334 may further comprise an offset spacer (not shown) positioned between the gate 308 and the oxide liner 336.

Finally, a patterned mask (not shown) is coated on the second conductive transistor area 304. A first ion source/drain implantation process is then carried out to form a first ion source/drain region 344 in the first conductive transistor area 302; thereby a first conductive transistor 340 such as a PMOS transistor is formed in the first conductive transistor area 302. Thereafter, the patterned mask is removed. Subsequently, another patterned mask (not shown) is coated on the first conductive transistor area 302. A second ion source/drain implantation process is carried out to form a second ion source/drain region 346 in the second conductive transistor area 304; thereby a second conductive transistor 342 such as an NMOS transistor is formed in the second conductive transistor area 304. Thereafter, the patterned mask is removed.

It should be noticed that the processes of forming the first source/drain regions 344 and the second source/drain regions 346 as shown in FIG. 14 is an optional step depending on the method used in the epitaxial growth process. Because the epitaxial growth process as shown in FIG. 9 may be an in-situ doped epitaxial growth process, therefore, while the first epitaxial layer 320 or the second epitaxial layer 328 is formed, the demanded doped ions can also be implanted into the semiconductor substrate 300 or the grown epitaxial layers 320, 328, as a result, the corresponding source/drain regions are formed. Accordingly, source/drain implantation as shown in FIG. 14 can be skipped.

Since the characteristic of the present invention is to form the epitaxial layer before forming the spacer, thus the distance between the gate and the epitaxial layer is no longer limited by the width of the spacer. Besides, the process of etching the

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recess is carried out before forming the spacer. At this moment, the pattern density on the semiconductor substrate is lower than the time when the spacer is formed, thus the micro-loading effect caused by the pattern density can be reduced, and then the uniformity in etching the recess is increased. Additionally, the lightly doped regions and the source/drain regions are doped after forming the epitaxial layer, thus the doped ions will not be affected by the high temperature epitaxial growth process, which leads the doped ions to diffuse. Finally, since the present invention provides a protective layer to cover the semiconductor substrate and the shallow trench isolation (STI), the problem of the STI thickness loss will be reduced.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention.

What is claimed is:

1. A MOS transistor structure, comprising:

a gate formed on a semiconductor substrate;

two raised epitaxial layers positioned respectively in the semiconductor substrate next to the relative sides of the gate and above the surface of the semiconductor substrate;

a spacer formed on the sidewall of the gate and extending laterally upon a portion of the raised epitaxial layers, and a contact surface of the raised epitaxial layers and a bottom of the spacer is above the surface of the semiconductor substrate; and

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two doped region formed respectively in the semiconductor substrate next to the relative sides of the gate.

2. The structure of claim 1, wherein the gate further comprises:

a dielectric layer;

a conductive layer, positioned on the dielectric layer; and a cap layer, positioned on the conductive layer.

3. The structure of claim 1, wherein the MOS transistor comprises a PMOS transistor.

4. The structure of claim 3, wherein the epitaxial layer comprises SiGe.

5. The structure of claim 1, wherein the MOS transistor comprises an NMOS transistor.

6. The structure of claim 5, wherein the epitaxial layer comprises SiC.

7. The structure of claim 1, wherein the spacer further comprises an offset spacer, positioned between the gate and the spacer.

8. The structure of claim 1, wherein the spacer further comprises an oxide liner and a nitride spacer.

9. The structure of claim 1, wherein the edge of the raised epitaxial layers is not aligned with the edge of the spacer.

10. The structure of claim 1, wherein the spacer further comprises a L-shaped spacer.

11. The structure of claim 1, further comprising a lightly doped drain disposed in the semiconductor substrate and outside the raised epitaxial layers.

* * * * *

Exhibit B



US009093473B2

(12) **United States Patent**
Wei et al.

(10) **Patent No.:** **US 9,093,473 B2**
(45) **Date of Patent:** **Jul. 28, 2015**

(54) **METHOD FOR FABRICATING
METAL-OXIDE SEMICONDUCTOR
TRANSISTOR**

(2013.01); **H01L 29/7816** (2013.01); **H01L 29/7834** (2013.01); **H01L 29/7848** (2013.01); **H01L 29/66575** (2013.01)

(71) Applicant: **UNITED MICROELECTRONICS
CORP.**, Hsin-Chu (TW)

(58) **Field of Classification Search**

CPC H01L 29/66689; H01L 29/7816;
H01L 29/6656; H01L 29/66636; H01L
29/7834; H01L 29/165; H01L 21/823828;
H01L 21/823864; H01L 21/823807; H01L
29/7848; H01L 29/66575

See application file for complete search history.

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H01L 29/66 (2006.01)
H01L 21/8238 (2006.01)
H01L 29/165 (2006.01)
H01L 29/78 (2006.01)

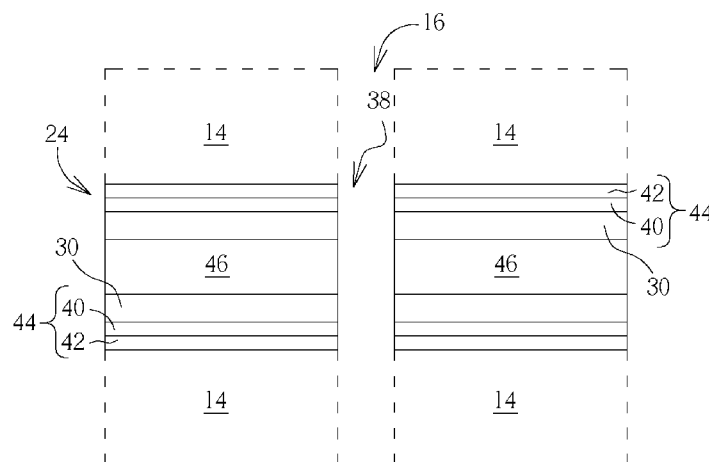
(52) **U.S. Cl.**

CPC .. **H01L 29/66689** (2013.01); **H01L 21/823807**
(2013.01); **H01L 21/823828** (2013.01); **H01L 21/823864** (2013.01); **H01L 29/165** (2013.01);
H01L 29/6656 (2013.01); **H01L 29/66636**

ABSTRACT

A method for fabricating a metal-oxide semiconductor (MOS) transistor is disclosed. The method includes the steps of: providing a semiconductor substrate; forming a silicon layer on the semiconductor substrate; performing a first photo-etching process on the silicon layer for forming a gate pattern; forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

10 Claims, 3 Drawing Sheets



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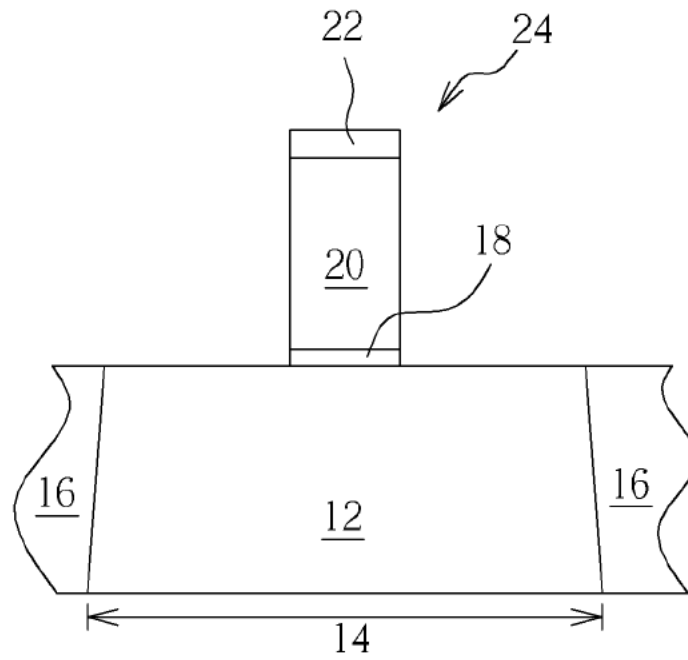


FIG. 1



FIG. 2

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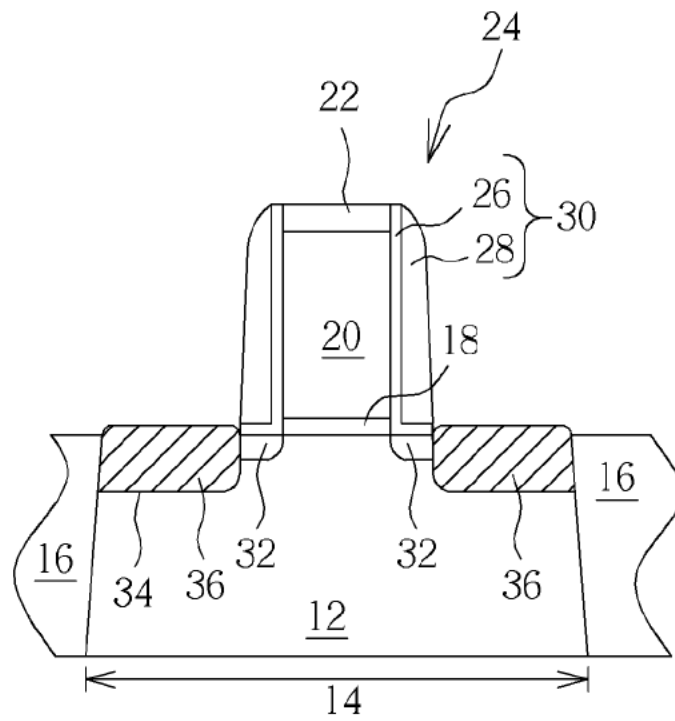


FIG. 3

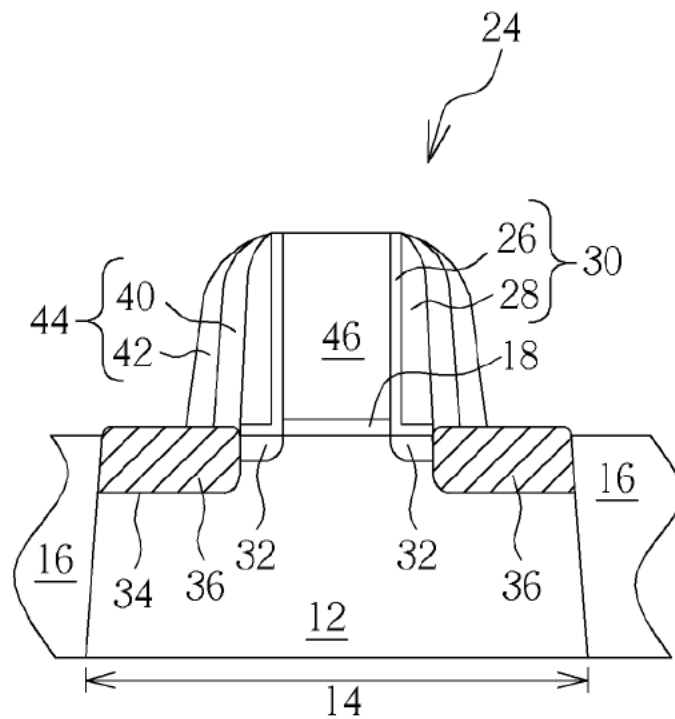


FIG. 4

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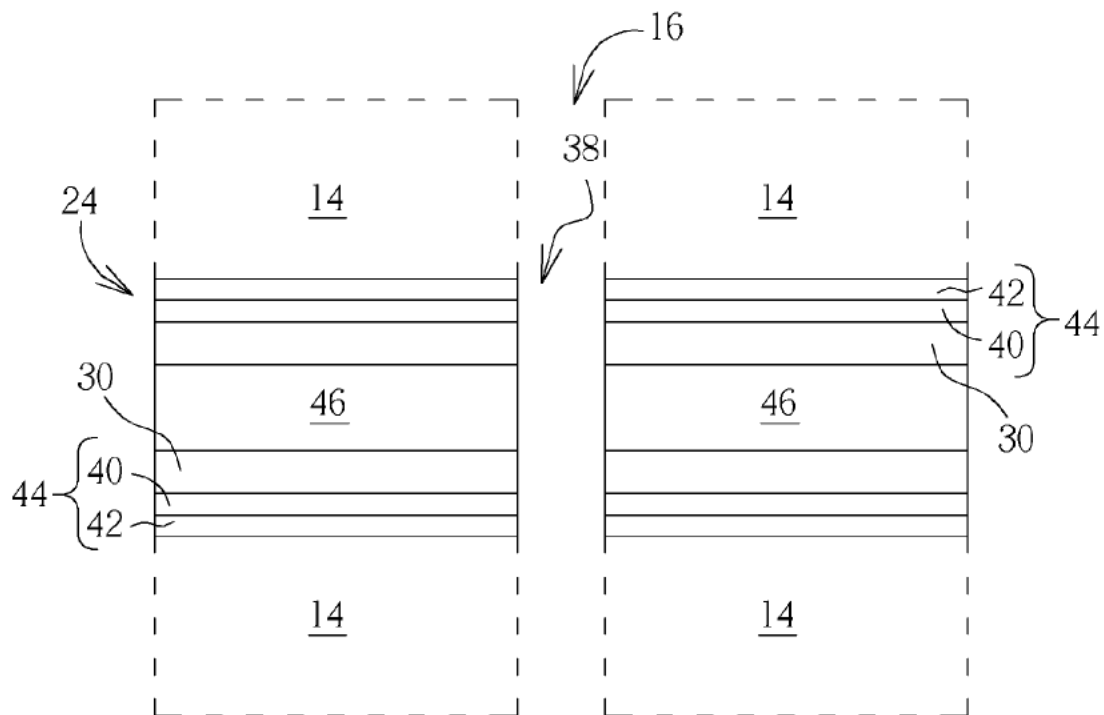


FIG. 5

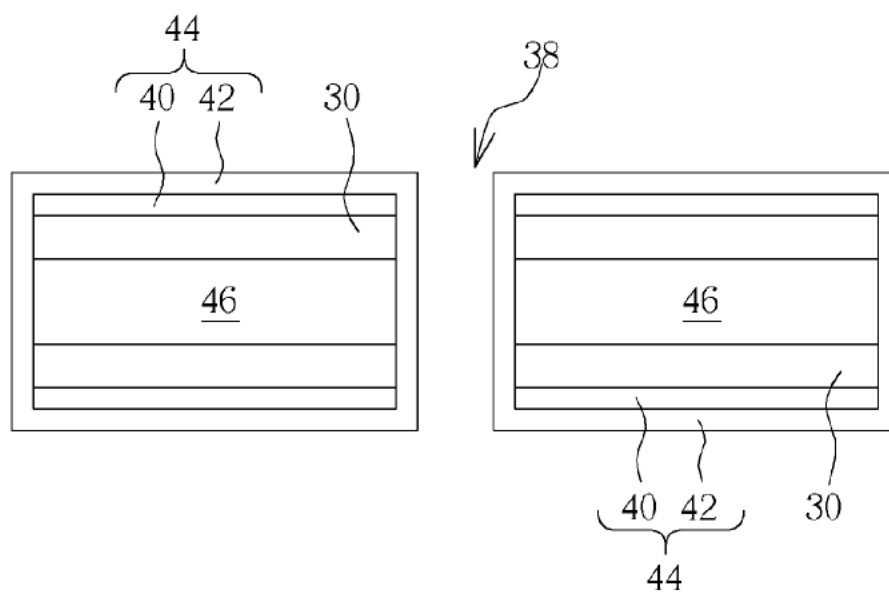


FIG. 6

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METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 12/837,475 filed Jul. 15, 2010, and incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a method for fabricating MOS transistor, and more particularly, to a method of defining polysilicon slot before formation of epitaxial layer.

2. Description of the Prior Art

In the field of semiconductor fabrication, the use of polysilicon material is diverse. Having a strong resistance for heat, polysilicon materials are commonly used to fabricate gate electrodes for metal-oxide semiconductor transistors. The gate pattern fabricated by polysilicon materials is also used to form self-aligned source/drain regions as polysilicon readily blocks ions from entering the channel region.

As the dimension of semiconductor devices decreases, the fabrication of transistors also improves substantially for fabricating small size and high quality transistors. Conventional approach of fabricating the gate of metal-oxide semiconductor (MOS) transistors typically forms a polysilicon layer on a semiconductor substrate and a hard mask on the polysilicon layer before using two photo-etching processes (PEP) to pattern the polysilicon layer and the hard mask into a gate of the transistor. Preferably, the first photo-etching process is conducted to pattern the hard mask and the polysilicon layer into a plurality of rectangular polysilicon gate pattern as the second photo-etching process forms a polysilicon slot in each of the rectangular gate pattern for separating each gate pattern into two gates. Thereafter, elements including spacers are formed on the sidewall of the gate and lightly doped drains and epitaxial layer are formed in the semiconductor substrate adjacent to two sides of the spacer.

However, as the polysilicon slot is preferably formed before the formation of epitaxial layer, the etching ratio involved during the formation of the polysilicon slot typically affects the process thereafter. For instance, if the etching ratio of the second photo-etching process is low, the gate pattern would not be etched through completely to form the polysilicon slot and phenomenon such as polysilicon residue and line end bridge would result, whereas if the etching ratio of the second photo-etching process is high, the hard mask disposed on top of the polysilicon gate pattern would be consumed, which would further induce consumption of the spacer formed on the sidewall of the gate thereafter. As some of the spacer on the sidewall is consumed away, a portion of the gate is exposed and un-wanted epitaxial layer would be formed on the exposed portion of the gate.

SUMMARY OF THE INVENTION

It is an objective of the present invention to provide a method for fabricating a MOS transistor for resolving the aforementioned issue caused by conventional approach.

According to a preferred embodiment of the present invention, a method for fabricating a metal-oxide semiconductor (MOS) transistor is disclosed. The method includes the steps of: providing a semiconductor substrate; forming a silicon

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layer on the semiconductor substrate; performing a first photo-etching process on the silicon layer for forming a gate pattern; forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

According to another aspect of the present invention, a metal-oxide semiconductor (MOS) transistor is disclosed. The MOS transistor includes: a semiconductor substrate; a gate disposed on the semiconductor substrate, wherein the gate comprises four sidewalls, and two of the four sidewalls opposite to each other comprise a spacer thereon while the other two sidewalls opposite to each other comprise no spacer; and an epitaxial layer disposed in the semiconductor substrate adjacent to two sides of the spacer.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-6 illustrate a method for fabricating a MOS transistor according to a preferred embodiment of the present invention.

DETAILED DESCRIPTION

Referring to FIGS. 1-6, FIGS. 1-6 illustrate a method for fabricating a MOS transistor according to a preferred embodiment of the present invention. As shown in FIG. 1, a semiconductor substrate 12, such as a silicon substrate or a silicon-on-insulator (SOI) substrate is provided. At least an active region 14 is defined on the semiconductor substrate 12 and a plurality of shallow trench isolations (STI) 16 are formed for separating the active region 14 from adjacent regions or devices.

A gate insulating layer (not shown) composed of dielectric material such as oxides or nitrides is deposited on surface of the semiconductor substrate 12, and a polysilicon layer preferably with a depth of approximately 1000 Angstroms and a hard mask are formed sequentially on the gate insulating layer thereafter. In this embodiment, the hard mask could be selected from a material consisting of SiO₂, silicon nitride, and SiON, and the polysilicon layer could be composed of undoped polysilicon material or polysilicon with N⁺ dopants, which are all within the scope of the present invention.

Next, a photo-etching process is performed on the hard mask and the polysilicon layer by first forming a patterned photoresist (not shown) on the hard mask and then using the photoresist as mask to carryout a patterning process. The patterning process preferably removes a portion of the hard mask, the polysilicon layer and the gate insulating layer through a single or multiple etching to form a gate pattern 24 composed of patterned gate insulating layer 18, patterned polysilicon layer 20, and patterned hard mask 22 in the active region 14. The patterned photoresist is removed subsequent to the patterning process.

Next, as shown in FIG. 2, FIG. 2 illustrates a top view of the gate formed after the first photo-etching process. As shown in the figure, a plurality of rectangular gate patterns 24 are formed on the semiconductor substrate 12 after the aforementioned first photo-etching process, in which each gate pattern

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24 is composed of a patterned gate insulating layer 18, a patterned gate polysilicon layer 20, and a patterned hard mask 22.

As shown in FIG. 3, a first stage spacer formation is conducted by first depositing a silicon oxide layer (not shown) and a silicon nitride layer (not shown) on the semiconductor substrate 12. An etching back is carried thereafter to remove a portion of the silicon oxide layer and silicon nitride layer to form a first spacer 30 composed of silicon oxide layer 26 and silicon nitride layer 28 on the sidewall of the gate pattern 24.

Next, a selective epitaxial growth (SEG) process is performed to form a strained silicon in the semiconductor substrate 12. For instance, a patterned photoresist (not shown) could be formed on the semiconductor substrate, and an etching process is conducted to form two recesses 34 in the semiconductor substrate 12 adjacent to two sides of the gate pattern 24. A surface clean is carried out thereafter to completely remove native oxides or other impurities from the surface of the recesses 34. Next, a selective epitaxial growth process is performed to substantially fill the two recesses 34 for forming an epitaxial layer 36. Preferably, a light ion implantation could be conducted before the formation of the first spacer 30 and the epitaxial layer 36 to implant n-type or p-type dopants into the semiconductor substrate 12 adjacent to two sides of the gate pattern 24 for forming a lightly doped drain 32, and the material of the epitaxial layer 36 could be selected according to the type of the transistor or demand of the product.

For instance, if the transistor fabricated were to be a PMOS transistor, an epitaxial layer 36 composed of silicon germanium is preferably formed in the recesses 34 to provide a compressive strain to the channel region of the PMOS transistor thereby increasing the hole mobility of the transistor. Conversely, if the transistor fabricated were to be a NMOS transistor, an epitaxial layer composed of silicon carbide (SiC) is preferably formed in the recesses 34 to provide a tensile strain to the channel region of the NMOS transistor for increasing the electron mobility of the transistor.

Referring now to FIGS. 4 and 5, FIG. 4 illustrates a cross-sectional view of the gate pattern after FIG. 3 and FIG. 5 illustrates a top view of the gate according to this embodiment. As shown in the figures, the hard mask 22 disposed on top of the polysilicon layer 20 is removed, and a spacer material layer, such as a silicon oxide layer (not shown) and a silicon nitride layer (not shown) are deposited sequentially on the semiconductor substrate 12. A photo-etching process is then carried out by first forming a patterned photoresist (not shown) on the polysilicon layer 20 and performing an etching process by using the patterned photoresist as mask to remove the polysilicon layer 20 on top of the shallow trench isolation 16, such as a part of the two ends and central portion of the polysilicon layer 20 for forming at least a polysilicon slot 38 in the rectangular gate pattern 24. The polysilicon slot 38 preferably separates the gate pattern 24 into two independent gates 46. After stripping the patterned photoresist and cleaning off remaining particles from the surface of the semiconductor substrate 12, an etching back is conducted on the deposited silicon oxide layer (not shown) and silicon nitride layer (not shown) for forming a second spacer 44 composed of silicon oxide layer 40 and silicon nitride layer 42 on the sidewall of the gate 46.

For simplification purpose, only one gate pattern 24 is revealed in FIG. 5 and other doping regions including lightly doped drain and epitaxial layers are also omitted. As shown in the figure, the polysilicon slot 38 preferably divides the gate pattern 24 into two independent portions, and as part of the silicon oxide layer 40 and silicon nitride layer 42 is removed

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for forming the polysilicon slot 38 and separating the gate pattern 24, no spacer is formed on at least two opposite sidewalls of the gate 46 after the separation. In other words, a second spacer 44 composed of silicon oxide layer 40 and silicon nitride layer 42 is formed on two opposite sidewalls of the polysilicon gate 46, whereas the other two remaining opposite sidewall contain no spacer.

Preferably, the polysilicon slot 38 is formed after the removal of the hard mask to facilitate a rework process conducted afterwards. For instance, a rework is typically carried out during a lithography for forming the polysilicon slot 38, and as the hard mask 22 is removed from the active region 14 of the semiconductor substrate 12 before rework is carried out, the exposed silicon substrate surface becomes unprotected. Unfortunately, reacting gas such as oxygen used to remove photoresist material during rework typically accumulates native oxides on the surface of the substrate or forms recesses on the substrate. Hence, the present embodiment preferably removes the hard mask 22 from the polysilicon layer 20 and then deposits the aforementioned silicon oxide and silicon nitride layer on the substrate 12. These deposited silicon oxide and silicon nitride layer could not only be used as material layers for forming the second spacer, but also be used as etching mask for forming the polysilicon slot and protecting the active region.

In addition to forming the polysilicon slot after removing the hard mask, as addressed in the above embodiment, the polysilicon slot 38 could also be formed at any point after the epitaxial layer 36 is formed, which is within the scope of the present invention.

Moreover, the above embodiment of forming the second spacer preferably forms a silicon oxide layer and a silicon nitride layer before the etching back process, and then using one single etching back to simultaneously remove a portion of the silicon oxide layer and silicon nitride layer for forming the second spacer. However, the present invention could also deposit a single silicon oxide layer before the polysilicon slot is formed, and then deposit a silicon nitride layer after the formation of the polysilicon slot to form different MOS transistor structures.

For instance, a silicon oxide layer 40 could be deposited on the semiconductor substrate 12 after removing the hard mask, and after following the aforementioned step for forming the polysilicon slot 38, a silicon nitride layer 42 is deposited on the substrate 12, and a portion of the silicon oxide layer 40 and silicon nitride layer 42 are removed through etching back process to form the second spacer 44. As shown in FIG. 6, as part of the silicon oxide layer 40 is removed during the formation of the polysilicon slot 38, the silicon oxide layer 40 of the second spacer 44 would only be disposed on two opposite sidewall of the gate, and as the silicon nitride layer 42 of the second spacer 44 is deposited after the formation of the polysilicon slot 38, the silicon nitride layer 42 is preferably formed on four sidewalls of the gate 46.

According to another embodiment of the present invention, a silicon oxide layer 40 could be deposited on the semiconductor substrate 12 after removing the hard mask, and after following the aforementioned approach for forming the polysilicon slot 38, an etching back is carried out to remove a portion of the silicon oxide layer 40 for forming a second spacer, and then depositing a silicon nitride layer 42 on the substrate 12, and then performing another etching back to remove part of the silicon nitride layer 42 for forming a third spacer. Despite the fabrication sequence of this embodiment is slightly different from the above approach, the same transistor structure as disclosed in FIG. 6 could be fabricated.

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In contrast to the conventional approach of forming polysilicon slot before the epitaxial layer, the present invention uses a first photo-etching process to define a rectangular polysilicon gate pattern, forms an epitaxial layer adjacent to two sides of the gate pattern, and then uses a second photo-etching process to define the polysilicon slot while separating the gate pattern into two gates. As the definition of the polysilicon slot is carried after the formation of the epitaxial layer, issues such as line end bridge of epitaxial layer and growth of epitaxial layer on sidewall of the gate could be prevented substantially.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:

providing a semiconductor substrate;
forming a silicon layer on the semiconductor substrate;
performing a first photo-etching process on the silicon layer for forming a gate pattern;
forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and
after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

2. The method of claim 1, wherein after forming the silicon layer comprises:

forming a hard mask on the silicon layer;
performing the first photo-etching process on the hard mask and the silicon layer for forming the gate pattern;
forming a first spacer around the gate pattern;
forming a lightly doped drain in the semiconductor substrate adjacent to two sides of the gate pattern;
forming at least a recess in the semiconductor substrate adjacent to two sides of the first spacer;
forming the epitaxial layer in the recess;
removing the hard mask disposed on the silicon layer;

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forming a first dielectric layer on the semiconductor substrate while covering the gate pattern;
performing the second photo-etching process on the gate pattern, the first spacer, and the first dielectric layer to form the slot in the gate pattern; and
removing a portion of the first dielectric layer for forming a second spacer.

3. The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.

4. The method of claim 1, wherein the hard mask comprises silicon nitride.

5. The method of claim 2, wherein the step of forming the first spacer comprises:

forming a silicon oxide layer and a silicon nitride layer on the semiconductor substrate; and
etching back the silicon oxide layer and the silicon nitride layer for forming the first spacer.

6. The method of claim 2, wherein the first dielectric layer comprises a silicon oxide layer and a silicon nitride layer.

7. The method of claim 2, wherein after performing the second photo-etching process comprises:

forming a second dielectric layer on the semiconductor substrate; and
removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.

8. The method of claim 7, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

9. The method of claim 2, wherein after forming the second spacer comprises:

forming a second dielectric layer on the semiconductor substrate; and
removing a portion of the second dielectric layer for forming a third spacer.

10. The method of claim 9, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

* * * * *

Exhibit C



US009147747B2

(12) **United States Patent**
Hung et al.

(10) **Patent No.:** **US 9,147,747 B2**
(45) **Date of Patent:** **Sep. 29, 2015**

(54) **SEMICONDUCTOR STRUCTURE WITH
HARD MASK DISPOSED ON THE GATE
STRUCTURE**

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(73) Assignee: **UNITED MICROELECTRONICS
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U.S.C. 154(b) by 35 days.

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H01L 29/66 (2006.01)
H01L 29/78 (2006.01)
H01L 29/417 (2006.01)

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(2013.01); **H01L 29/665** (2013.01); **H01L**
29/66795 (2013.01); **H01L 29/785** (2013.01);
H01L 29/7839 (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/665; H01L 21/823814;
H01L 2924/0002; H01L 21/28518; H01L
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USPC 257/365, 369, E21.421, E27.062,
257/E29.264

See application file for complete search history.

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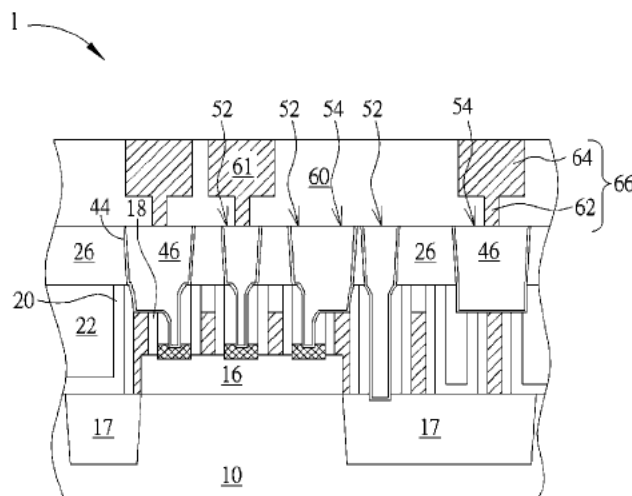
Primary Examiner — Andy Huynh

(74) *Attorney, Agent, or Firm* — Winston Hsu; Scott Margo

(57) **ABSTRACT**

The present invention provides a manufacturing method of a semiconductor structure, comprising the following steps. First, a substrate is provided, a first dielectric layer is formed on the substrate, a metal gate is disposed in the first dielectric layer and at least one source/drain region (S/D region) is disposed on two sides of the metal gate, a second dielectric layer is then formed on the first dielectric layer, a first etching process is then performed to form a plurality of first trenches in the first dielectric layer and the second dielectric layer, wherein the first trenches expose each S/D region. Afterwards, a salicide process is performed to form a salicide layer in each first trench, a second etching process is then performed to form a plurality of second trenches in the first dielectric layer and the second dielectric layer, and the second trenches expose the metal gate.

9 Claims, 5 Drawing Sheets



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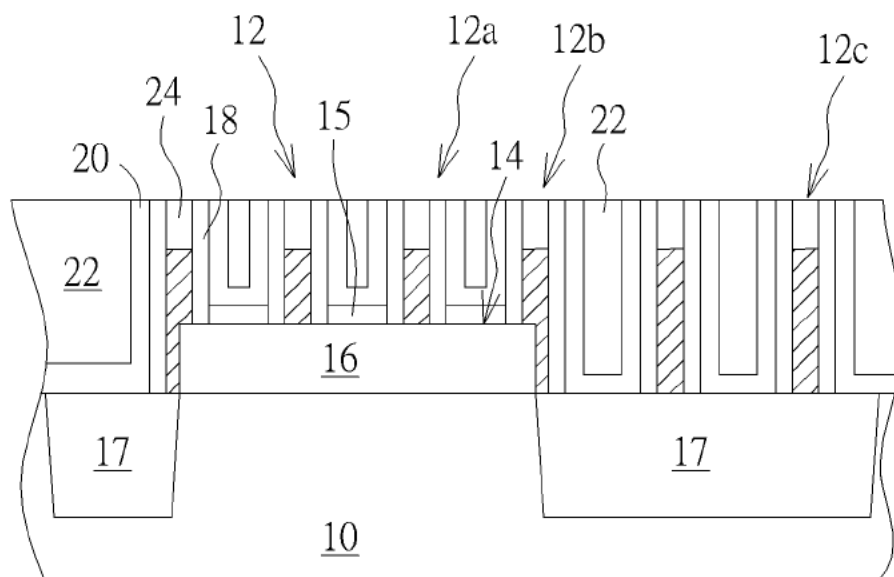


FIG. 1

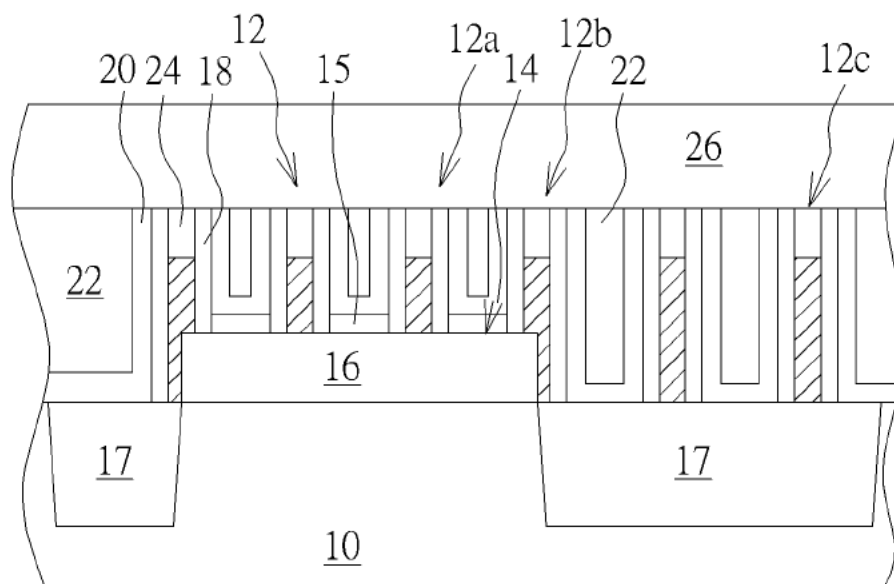


FIG. 2

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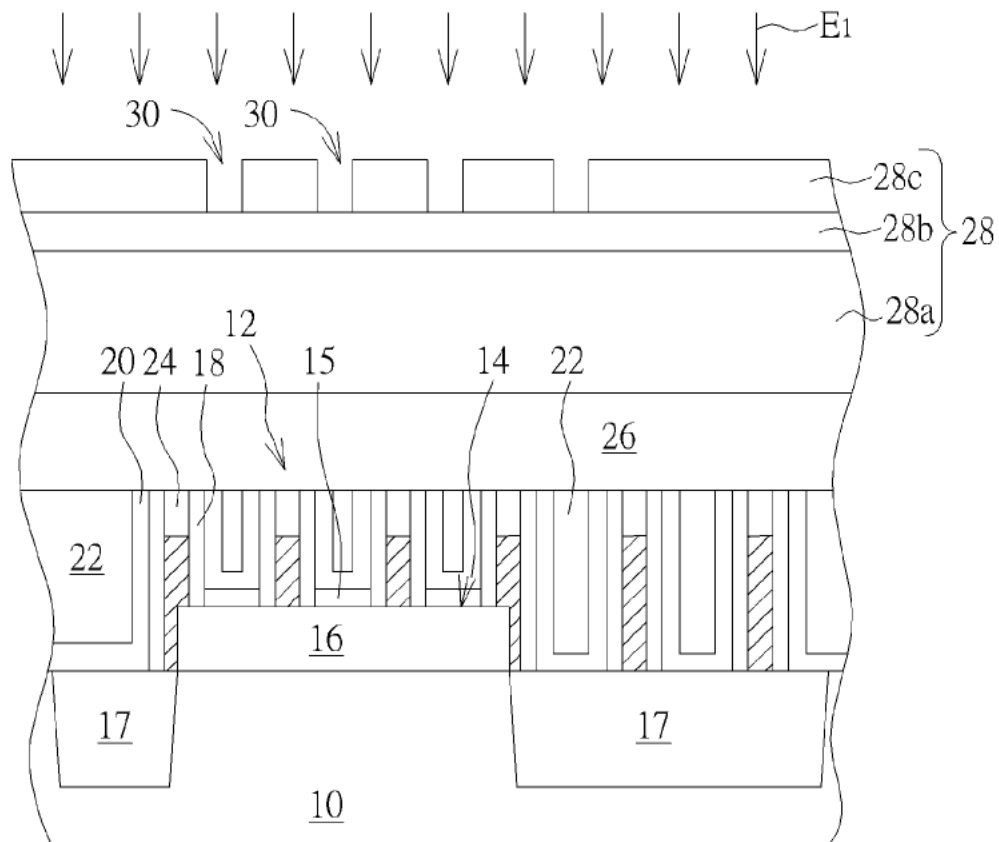


FIG. 3

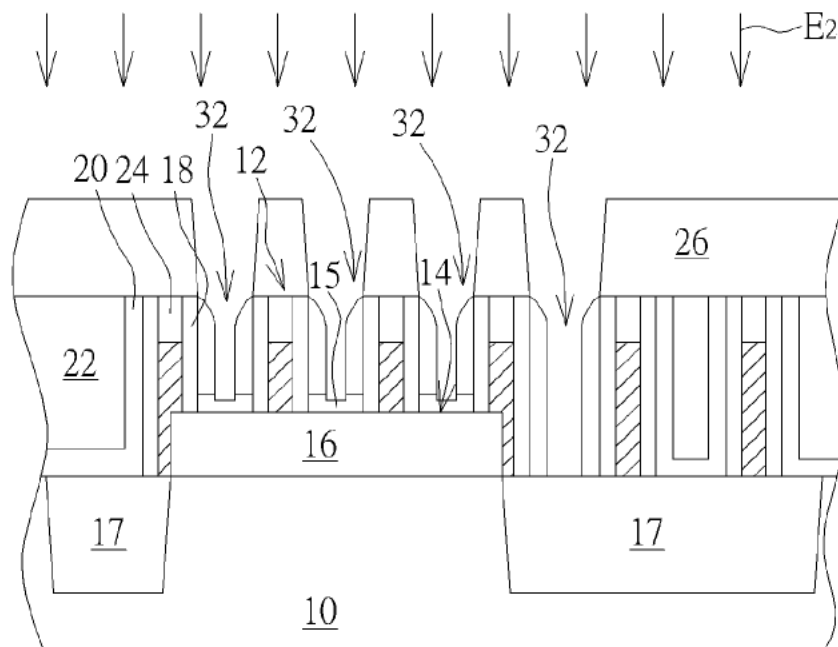


FIG. 4

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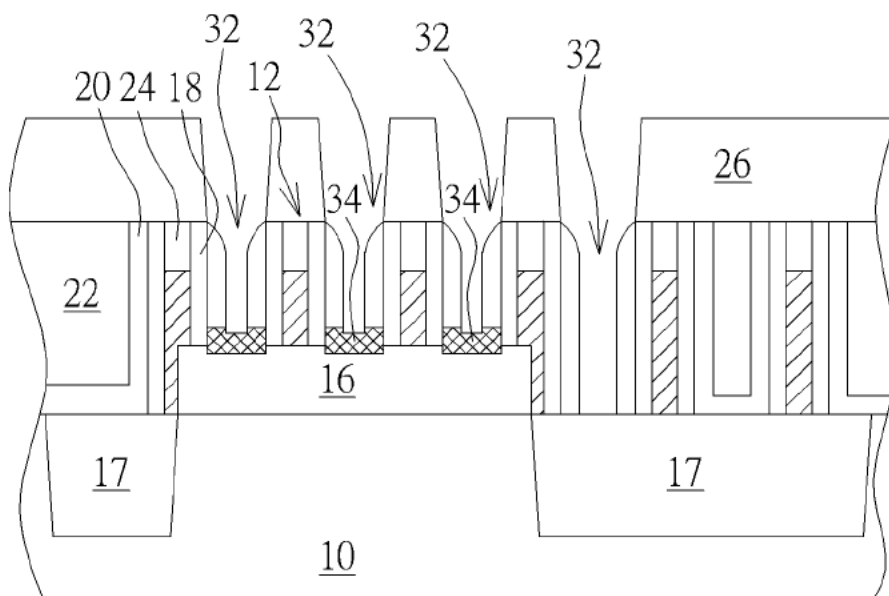


FIG. 5

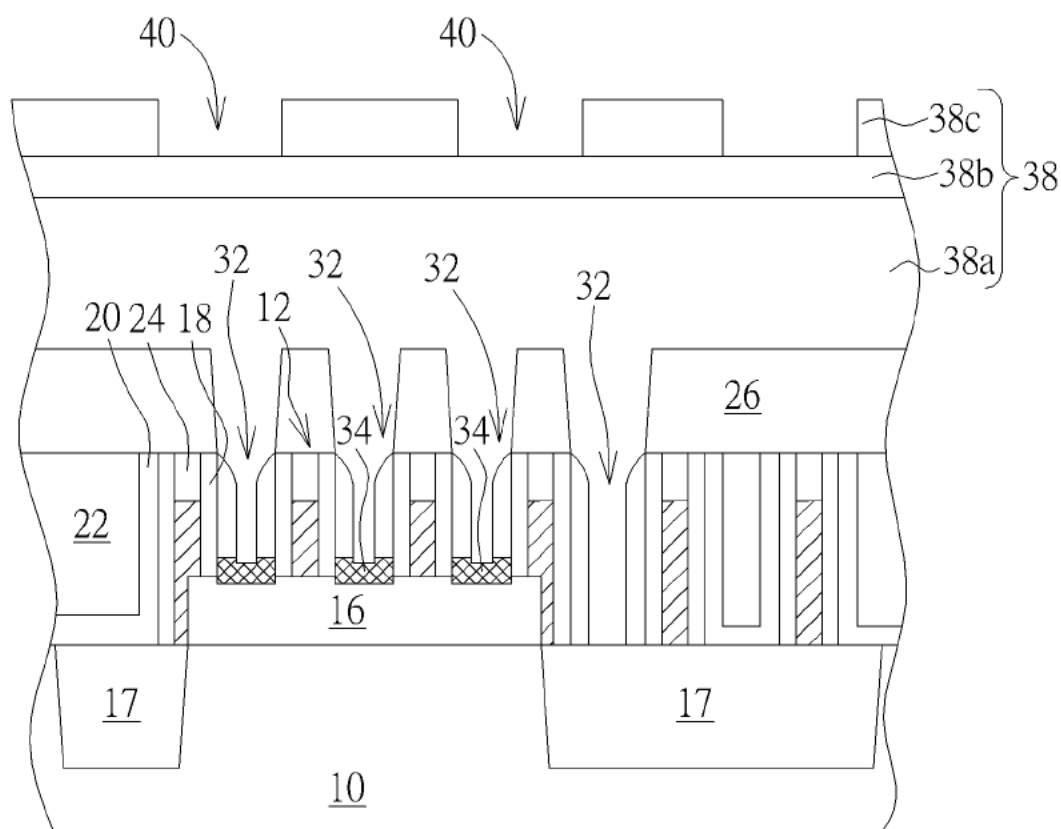


FIG. 6

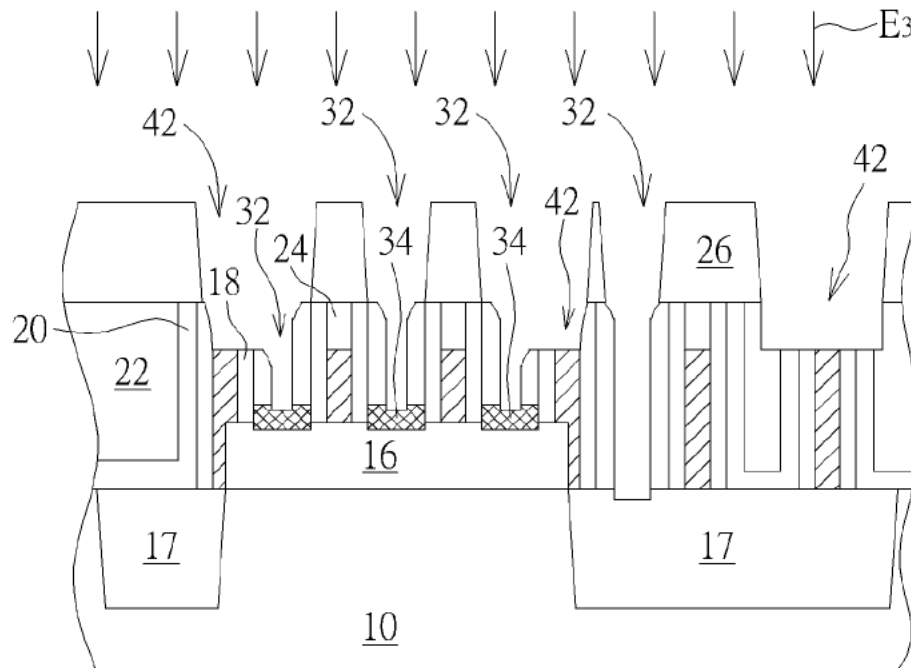


FIG. 7

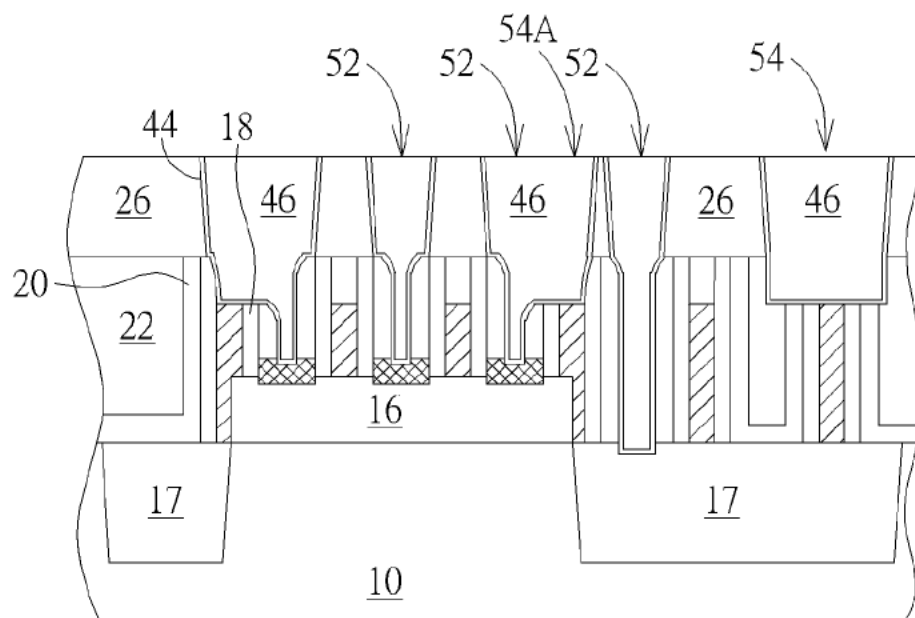


FIG. 8

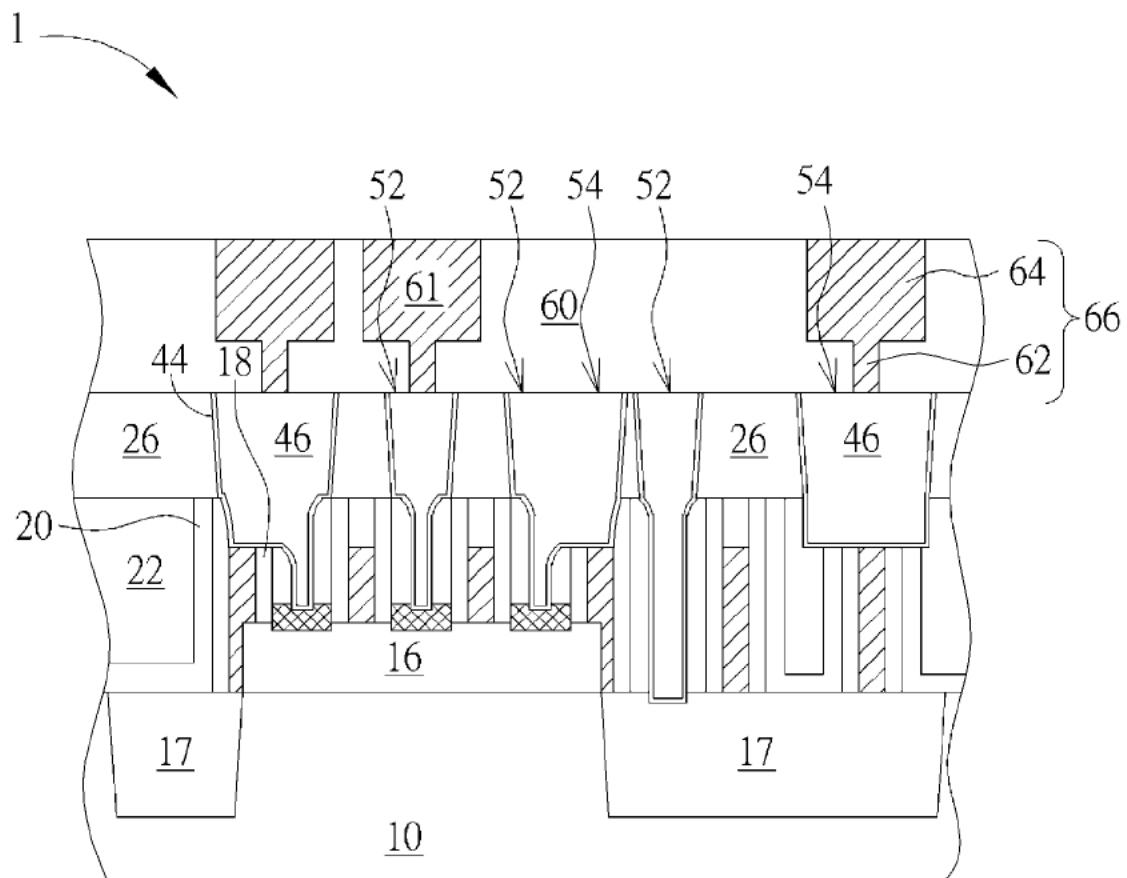


FIG. 9

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SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to semiconductor manufacturing process, and more specifically, to a method using a hard mask on the metal gate to form contacts structure simultaneously during a plurality of etching processes.

2. Description of the Prior Art

Along with the continuous miniaturization of the Integrated Circuits (IC), the line width of interconnections and the feature size of semiconductor devices have continuously shrunk. In general, discrete devices in integrated circuits are connected to each other through contact plugs (or contact slots) and interconnection structures, and their related fabrication methods have become an important matter in the next-generation semiconductor devices.

In current fabricating processes, due to the limitations of the back end of the line (BEOL) process capacity, the yield of contact plugs with high aspect ratio (HAR) is relatively low and cannot reach the new requirements. In order to overcome this drawback, a double patterning technique, generally including two photolithographic and two etching processes (2P2E) has been invented in order to fabricate required device patterns. Generally, a contact is divided into two parts, a lower contact structure and an upper contact structure (i.e. the metal level zero, M0). After the lower contact structure is formed completely, the M0 is continuously formed. The M0 can be a pole structure or a slot structure. However, since the upper contact structure (M0) and the lower contact structure are formed in different steps, a barrier layer will exist between the upper contact structure (M0) and the lower contact structure, thereby affecting the conductivity of the contact. Besides, the manufacturing process is too complex.

Accordingly, in order to overcome the above-mentioned drawbacks, there is a need to provide a modified method for fabricating interconnection structures with better yields.

SUMMARY OF THE INVENTION

To solve the issues mentioned above, the present invention provides a semiconductor device comprising a substrate, a first dielectric layer disposed on the substrate, a metal gate disposed in the first dielectric layer, a source/drain region (S/D region) disposed on two sides of the metal gate, and a hard mask disposed on the metal gate, wherein the top surface of the hard mask and the top of the first dielectric layer are on the same level.

The present invention further comprises a manufacturing method for forming the semiconductor device at least comprising the following steps: first, a substrate is provided, a first dielectric layer is formed on the substrate, a metal gate is disposed in the first dielectric layer and at least one source/drain region (S/D region) is disposed on two sides of the metal gate; a second dielectric layer is then formed on the first dielectric layer, a first etching process is then performed, to form a plurality of first trenches in the first dielectric layer and the second dielectric layer, wherein the first trenches expose each S/D region. Afterwards, a salicide process is performed to form a salicide layer in each first trench; a second etching process is then performed to form a plurality of second trenches in the first dielectric layer and the second dielectric layer, and the second trenches expose the metal gate.

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The present invention further comprises a hard mask on the metal gate, and uses etching gases with different etching rates to selectively etch the hard mask and the dielectric layer disposed above. In this way, the contacts disposed correspondingly to the metal gate and the contacts disposed correspondingly to the S/D region can be formed simultaneously, and replace the 0th metal layer (M0) and the lower contact structure in a conventional process, thereby reducing the manufacturing steps.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-9 are schematic diagrams illustrating a manufacturing method of the FinFET semiconductor device according to a first preferred embodiment of the present invention.

DETAILED DESCRIPTION

To provide a better understanding of the present invention to users skilled in the technology of the present invention, preferred embodiments are detailed as follows. The preferred embodiments of the present invention are illustrated in the accompanying drawings with numbered elements to clarify the contents and effects to be achieved.

Please note that the figures are only for illustration and the figures may not be to scale. The scale may be further modified according to different design considerations. When referring to the words "up" or "down" that describe the relationship between components in the text, it is well known in the art and should be clearly understood that these words refer to relative positions that can be inverted to obtain a similar structure, and these structures should therefore not be precluded from the scope of the claims in the present invention.

Please refer to FIGS. 1-9 are schematic diagrams illustrating a manufacturing method of the FinFET semiconductor device according to a first preferred embodiment of the present invention. As shown in FIG. 1, a substrate 10 is first provided, wherein the substrate 10 comprises at least one metal gate 12 disposed on the substrate 10 and at least one source/drain region (S/D region) 14 disposed on two sides of the metal gate 12. Besides, the substrate 10 selectively comprises at least one fin structure 16. In this embodiment, the metal gate 12 comprises metal materials, the S/D region 14 can be formed on two sides of the metal gate 12 of the substrate 10 through an ion implantation process, or formed on the fin structure 16 disposed on two sides of the metal gate 12. The method of the present invention further comprises forming at least one shallow trench isolation (STI) 17 in the substrate 10 surrounding the metal gate 12, to isolate the metal gate 12 from the fin structures 16 and others electric elements on the substrate 10. In this embodiment, the metal gate may cross the fin structure disposed on the substrate 10 (such as the metal gate 12a shown in FIG. 1), or be disposed on the STI 17 (such as the metal gate 12c shown in FIG. 1) and be used as a dummy gate, or may disposed on the edge of the fin structure 16 to protect the fin structure 16 (such as the metal gate 12b shown in FIG. 1).

In addition, the method of the present invention further comprises selectively forming an epoxy layer 15 on the S/D region 14. Afterwards, a spacer 18 and a contact etching stop layer (CESL) 20 may be formed on two sides of the metal gate 12. A first dielectric layer 22 is then formed on the substrate

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10, and a planarization process is then performed, such as a chemical mechanical polishing (CMP), to have the top surface of the metal gate 12 and the top surface of the first dielectric layer 22 on the same level. It is worth noting that in this embodiment, an etching process is performed after the metal gate 12 is completed, to remove parts of the metal gate 12, and a hard mask 24 is then formed to replace the upper portion of the metal gate 12. Another planarization process is then performed to remove the extra hard mask 24. In other words, in the present embodiment, a hard mask 24 is disposed on the top of the metal gate 12, and the top surface of the hard mask 24 and the top surface of the first dielectric layer 22 are on the same level. Besides, since the hard mask 24 replaces some top portion of the metal gate 12, the hard mask 24 is therefore disposed only on the metal gate 12, and disposed between the spacers 18. In addition, since parts of the spacer 18 and parts of the CESL 20 are removed during another planarization process, so the spacer 18 and the CESL 20 have a truncated top surface. In the present embodiment, the spacer 18, the CESL 20 and the hard mask 24 mainly comprise silicon nitride, and the first dielectric layer 22 mainly comprises silicon oxide, but not limited thereto. These elements and the manufacturing methods thereof are well known to persons of ordinary skills in the art and the details will not be described here.

As shown in FIG. 2, a second dielectric layer 26 is then formed on the first dielectric layer 22. According to the preferred embodiment, the photoresist layer 28 sequentially includes an organic dielectric layer (ODL) 28a, a silicon-containing hard mask bottom anti-reflecting coating (SHB) 28b and a photoresist (PR) layer 28c. In short, the photoresist layer 28 is a tri-layer structure consisting of an ODL/SHB/PR structure, but not limited thereto. Afterwards, in order to form the metal plug that is electrically connected to the S/D region 14 (wherein the metal plug can replace the M0 and the lower contacts structure electrically connected to the S/D region in conventional process, denoted here as the 0th metal contact, M0CT), a photo-etching process is performed to pattern the photoresist layer 28c and to form a plurality of openings 30, wherein each opening 30 is at least disposed correspondingly to the S/D region 14 disposed below, but not limited thereto. Parts of the openings 30 may be disposed correspondingly to the STI 17 surrounding the metal gate 12 to reduce the pattern density difference between the region including the transistor (mainly comprising the metal gate 12, the S/D region 14 and the fin structure 16) and the periphery region.

Afterwards, as shown in FIGS. 3~4, at least one etching process E1 is performed to transfer the pattern to others layer disposed below, wherein the etching process E1 comprises: from top to bottom, etching the SHB 28b, the ODL 28a, the second dielectric layer 26 and the first dielectric layer 22 in sequence, until exposing the CESL 20. As shown in FIG. 4, another etching process E2 is then performed, parts of the CESL 20 are removed to expose the epoxy layer 15 disposed below and to form a plurality of first trenches 32, wherein each first trench 32 exposes the epoxy layer 15. It is worth noting that since the epoxy layer is selectively formed, each first trench 32 may therefore directly expose the S/D region 14. Besides, according to different embodiments, parts of the first trenches 32 may be disposed on STI 17.

The etching process of the present invention uses etching gases, which may comprise per fluorocarbon gases, such as tetrafluoromethane (CF₄), fluoroform (CHF₃), hexafluoride-1,3+butadiene (C₄F₆), and further comprises oxygen and argon, but not limited thereto. It is worth noting that the higher the ratio of per fluorocarbon gases to oxygen in the etching gas is, the higher the selectivity of the silicon nitride to silicon

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oxide will be. In other words, the more per fluorocarbon gases are present in the etching gas, the faster the etching rate will be for etching the silicon nitride, compared with the etching rate for etching the silicon oxide. In this embodiment, the main material of the first dielectric layer 22 and the second dielectric layer 26 is silicon oxide, the main material of the CESL 20 is silicon nitride, and the etching gas in etching process E1 is a high selectivity gas (to silicon nitride and silicon oxide), and the selectivity is preferably larger than 5, so the etching rate for etching the second dielectric layer 26 and etching the first dielectric layer 22 will be relatively fast, but the etching rate for etching the CESL 20 is relatively slow when the etching process E1 is performed. The etching rate for etching the second dielectric layer 26 and etching the first dielectric layer 22 is at least five times higher than the etching rate for etching the CESL 20, so the CESL 20 is not easily etched trough during the etching process E1, and the etching will stop on the surface of the CESL 20. Afterwards, the etching gas is adjusted for the etching process E2, and the CESL 20 disposed on the bottom of the first trenches 32 will be removed during the etching process E2.

As shown in FIG. 5, a salicide (self-aligned silicide) process is performed to the epoxy layer 15 to form a salicide layer 34 on the bottom of the first trenches 32. The salicide process mainly comprises filling a metal layer (not shown) in each first trench 32, and a thermal process is then performed to form a salicide layer 34 on the interface between the metal layer and the silicon-containing surface. Afterwards, the metal layer disposed in the first trenches 32 is removed. It is worth noting that since the salicide layer 34 is only formed on the silicon-containing surface, it may therefore be formed on the fin structure 16, on the epoxy layer 15 or on the substrate 10, but will not be formed on the STI 17.

As shown in FIG. 6, a photoresist layer 38 is then formed, wherein the material of the photoresist layer 38 may be the same as the material of the photoresist layer 28, comprising an organic dielectric layer (ODL) 38a, a silicon-containing hard mask bottom anti-reflecting coating (SHB) 38b and a photoresist layer 38c. Afterwards, in order to form the metal plug that is electrically connected to the metal gate 12 (wherein the metal plug can replace the M0 and the lower contacts structure electrically connected to the metal gate in conventional process, denoted here as the 0th metal gate contact, M0PY), a photo-etching process is performed to pattern the photoresist layer 38c and to form a plurality of openings 40, wherein each opening 40 is at least disposed correspondingly to the metal gate 12, but not limited thereto. Parts of the opening 40 may be disposed correspondingly to the STI 17.

As shown in FIG. 7, an etching process E3 is then performed to transfer the pattern to other layers disposed below, wherein the etching process E3 comprises etching in sequence from top to bottom: the SHB 38b, the ODL 38a, the second dielectric layer 26 and the hard mask 24. It is worth noting that in the etching process E3, the volume ratio of the per fluorocarbon gases to oxygen is adjusted to have an etching rate for etching the silicon nitride similar to the etching rate for etching the silicon oxide. In other words, the etching gas used in the etching process E3 has a low-selectivity for the silicon nitride and silicon oxide (the selectivity is preferably smaller than 5), so the etching gas can therefore remove the silicon nitride and remove the silicon oxide simultaneously. After the etching process E3 is performed, the top of the metal gate 12 can be exposed, besides, a plurality of second trenches 42 can be formed. Afterwards, the remaining photoresist layer and the ODL 38a disposed in the first trenches 32 or in the second trenches 42 can be removed through an ash process or other suitable processes.

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As shown in FIG. 8, a barrier layer 44 and a metal layer 46 are filled in each first trench 32 and each second trench 42 simultaneously, wherein the barrier layer 44 may comprise titanium nitride (TiN), tantalum nitride (TaN) or Ti/TiN multiple barrier layers to improve the adhesivity between the inner surface of each trench and the metal layer formed in the following steps. The metal layer 46 preferably comprises tungsten (W) that has better gap fill performances. A planarization process is then performed to remove the extra barrier layer and the metal layer disposed on the top surface of the second dielectric layer 26 to simultaneously form a plurality of first contacts 52 and a plurality of second contacts 54 in the first dielectric layer 22 and in the second dielectric layer 26, wherein each first contact 52 at least is electrically connected to parts of the S/D region 14 (in other words, the first contacts 52 of the present embodiment are the M0CT mentioned above), each second contact 54 is at least electrically connected to parts of the metal gate 12 (in other words the second contacts 54 of the present embodiment are the MOPY mentioned above). In addition, since the first contacts 52 and the second contacts 54 are filled by the metal layer 46 and completed simultaneously, each first contact 52 and each second contact 54 is a monolithically formed structure. It is worth noting that in the present invention, parts of the second trenches 42 and parts of the first trenches 32 are partially overlapped, so parts of the first contact 52 will be connected to parts of the second contacts 54 (such as the second contact 54A shown in FIG. 8). These connection portions of the first contacts 52 and the second contacts 54 may be used as share contacts of a semiconductor device, but not limited thereto.

As shown in FIG. 9, a metal interconnect process is performed, comprising forming a third dielectric layer 60 on the top of the second dielectric layer 26, wherein the third dielectric layer 60 is like the inter metal dielectric (IMD) in conventional technology, and forming a plurality of via holes (not shown) and a plurality of trace patterns (not shown) through an etching process or other methods. Finally, a metal layer 61 is simultaneously filled in each via hole and each trace pattern, and a planarization process is performed to remove the extra metal layer on the surface of the third dielectric layer 60 to complete a plurality of via hole structures 62 and a plurality of trace structures 64 simultaneously. In this embodiment, the via hole structures 62 and the corresponding trace structures 64 can be regarded as third contacts 66, wherein each third contact 66 is a monolithically formed structure. Each via hole structure 62 directly contacts the first contacts 52 or the second contacts 54 disposed below along a vertical direction. The trace structures 64 are on a same level, and electrically connected to others elements along a horizontal direction. The via hole structures 62 may have rectangular, circular or other block shapes, and the trace structures 64 may be lines or have striped shapes when viewed from top views, but not limited thereto.

It is worth noting that in the manufacturing process mentioned above, the first trenches 32 are formed before the second trenches 42 are formed, however, the present invention is not limited thereto. In another embodiment of the present invention, a low-selectivity etching gas may be used to form the second trenches 42, and a high-selectivity etching gas is then used to form the first trenches 32. A barrier layer 44 and a metal layer 46 are then filled into the first trenches 32 and the second trenches 42. A planarization process is then performed to complete a plurality of first contacts 52 and a plurality of second contacts 54. This manufacturing sequence should be comprised in the scope of the present invention.

A semiconductor device 1 of the present invention can be formed through the manufacturing process mentioned above,

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wherein the final structure is shown in FIG. 9. Please refer to FIGS. 1-9. The semiconductor device 1 at least comprises a substrate 10, a first dielectric layer 22 disposed on the substrate 10, a metal gate 12 disposed in the first dielectric layer 22, a S/D region 14 disposed on two sides of the metal gate 12, and a hard mask 24 disposed on the metal gate 12, wherein the top surface of the hard mask 24 and the top of the first dielectric layer 22 are on the same level, a second dielectric layer 26 disposed on the first dielectric layer 22. The present invention further comprises a plurality of first contacts 52 disposed in the first dielectric layer 22 and in the second dielectric layer 26 electrically connected to parts of the S/D region 14, wherein each first contact 52 is a monolithically formed structure, and a plurality of second contacts 54 disposed in the first dielectric layer 22 and in the second dielectric layer 26 electrically connected to parts of the metal gate 12, wherein each second contact 54 is a monolithically formed structure. In addition, the semiconductor device 1 selectively comprises the following components: an epoxy layer 15 disposed on the S/D region 14, a STI 17 disposed in the substrate 10 surrounding the metal gate 12, at least a spacer 18 and at least a CESL 20 disposed on two sides of the metal gate 12, wherein both of the two elements have a truncated top surface, a fin structure 16 disposed on the substrate 10, a salicide layer 34 disposed between each S/D region 14 and each first contact 52, a third dielectric layer 60 disposed on the second dielectric layer 26, and a plurality of third contacts 66 disposed on parts of the first contacts 52 or on parts of the second contacts 54, wherein each third contact 66 is a monolithically formed structure, and each third contact 66 comprises a via hole structure 62 and a trace structure 64, wherein each via hole structure 62 and each trace structure 64 comprise the same material, and contact each other. The other components, material properties, and manufacturing methods of the semiconductor device 1 are similar to those of the first preferred embodiment detailed above and will not be redundantly described.

In summary, the present invention comprises a hard mask on a metal gate, and uses etching gases with different etching rates to selectively etch the hard mask and the dielectric layer disposed above. Therefore, contacts disposed correspondingly to the metal gate and contacts disposed correspondingly to the S/D region can be formed simultaneously, and replace the 0th metal layer (M0) and the lower contact structures of conventional process, thereby reducing the manufacturing steps.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A semiconductor structure, comprising:

- a substrate;
- a first dielectric layer disposed on the substrate;
- at least two metal gates disposed in the first dielectric layer;
- a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;
- a source/drain region (S/D region) disposed between two metal gates;
- a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;
- a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts; and

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a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

2. The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer. 5

3. The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

4. The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure. 10

5. The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure. 15

6. The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

7. The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact. 20

8. The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure. 25

9. The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly. 30

* * * * *

Exhibit D



US009184292B2

(12) **United States Patent**
Lin et al.

(10) **Patent No.:** **US 9,184,292 B2**

(45) **Date of Patent:** **Nov. 10, 2015**

(54) **SEMICONDUCTOR STRUCTURE WITH DIFFERENT FINS OF FINFETS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Jul. 24, 2014**

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Related U.S. Application Data

(62) Division of application No. 13/370,231, filed on Feb. 9, 2012, now Pat. No. 8,822,284.

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H01L 29/76 (2006.01)
H01L 29/78 (2006.01)
H01L 21/8234 (2006.01)
H01L 27/108 (2006.01)
H01L 29/66 (2006.01)
H01L 21/764 (2006.01)
H01L 29/165 (2006.01)

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(52) **U.S. Cl.**
CPC **H01L 29/785** (2013.01); **H01L 21/31111** (2013.01); **H01L 21/764** (2013.01); **H01L**

21/823431 (2013.01); **H01L 21/823437** (2013.01); **H01L 27/10879** (2013.01); **H01L 29/1095** (2013.01); **H01L 29/161** (2013.01); **H01L 29/165** (2013.01); **H01L 29/1608** (2013.01); **H01L 29/66795** (2013.01); **H01L 21/02381** (2013.01); **H01L 21/02532** (2013.01); **H01L 21/02636** (2013.01); **H01L 21/3115** (2013.01); **H01L 21/3141** (2013.01); **H01L 21/3185** (2013.01); **H01L 21/31116** (2013.01); **H01L 27/0886** (2013.01)

(58) **Field of Classification Search**

None

See application file for complete search history.

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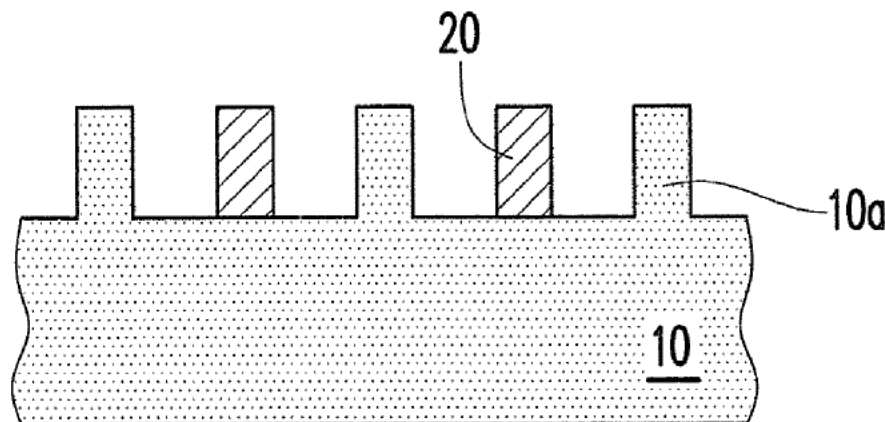
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(57) **ABSTRACT**

A semiconductor structure for forming FinFETs is described. The semiconductor structure includes a semiconductor substrate, a plurality of odd fins of the FinFETs on the substrate, and a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs. The odd fins of the FinFETs are defined from the substrate. The even fins of the FinFETs are different from the odd fins of the FinFETs in at least one of the width and the material, and may be further different from the odd fins of the FinFETs in the height.

20 Claims, 2 Drawing Sheets



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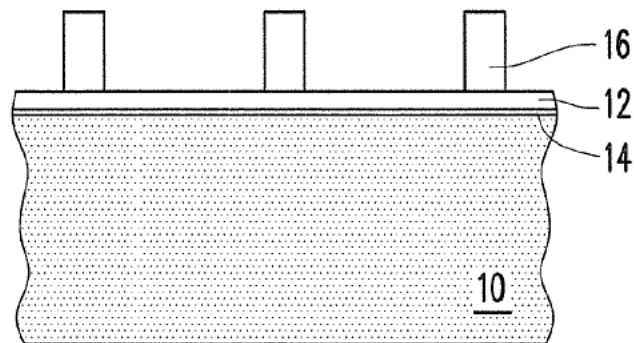


FIG. 1

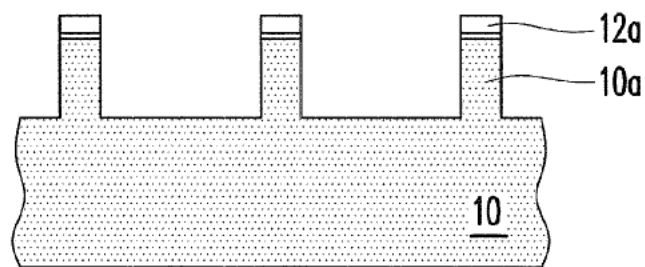


FIG. 2

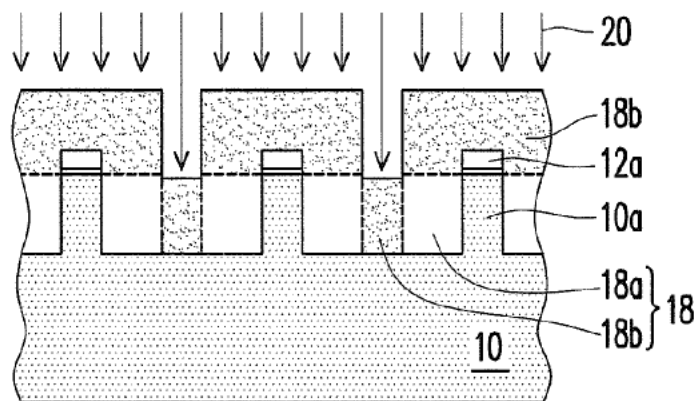


FIG. 3

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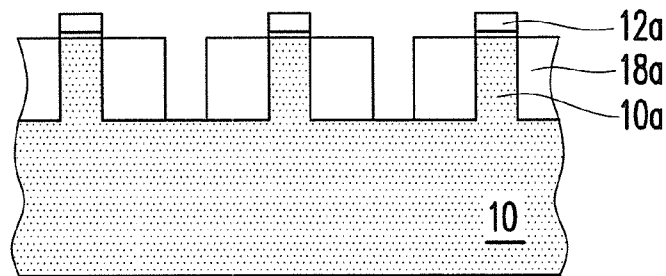


FIG. 4

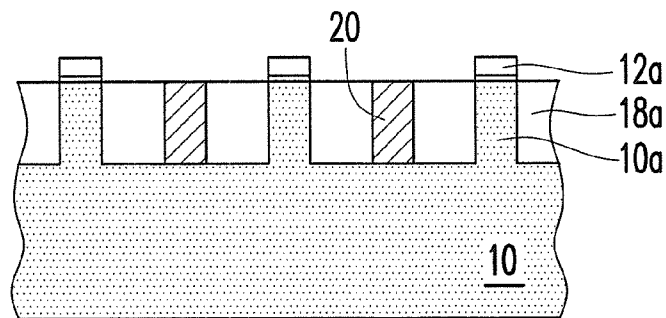


FIG. 5

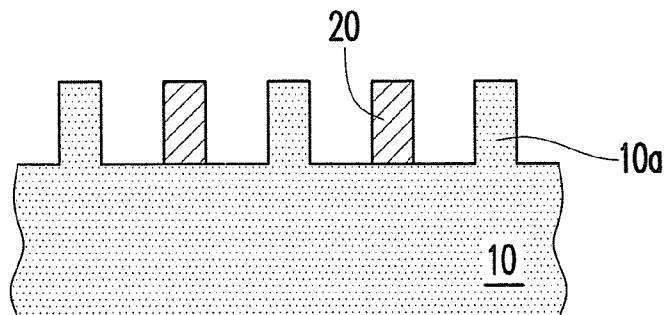


FIG. 6

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**SEMICONDUCTOR STRUCTURE WITH
DIFFERENT FINS OF FINFETS****CROSS-REFERENCE TO RELATED
APPLICATION**

This application is a divisional of and claims the priority benefit of U.S. application Ser. No. 13/370,231 filed on Feb. 9, 2012, now pending. The entirety of the above-mentioned patent application is hereby incorporated by reference herein and made a part of specification.

BACKGROUND OF THE INVENTION**1. Field of Invention**

This invention relates to a semiconductor process, and particularly relates to a method for fabricating fin-type field-effect transistors (FinFETs), and a semiconductor structure that is fabricated using the method.

2. Description of Related Art

MOS is a basic structure widely applied to various semiconductor devices, such as memory devices, image sensors and display devices.

The traditional MOS transistor is difficult to scale down due to the limitation of the fabricating process, so double-gate transistors with better properties are developed. One example is the FinFET, which has a 3D gate structure to enhance the control on the channel and inhibit the leakage current caused by the punch-through effect, and thus has a higher gate control capability than the conventional MOS transistor.

However, in the current FinFET process, the density of the fin patterns of the FinFET array is quite high and the thickness of the photoresist layer is quite large, so that the pattern development is difficult and an accurate pattern transfer is impossible.

SUMMARY OF THE INVENTION

Accordingly, this invention provides a method for fabricating FinFETs that is capable of solving the above problems of the prior art.

This invention also provides a semiconductor structure that is fabricated using the method of this invention.

The method for fabricating FinFETs of this invention is described as follows. A semiconductor substrate is patterned to form a plurality of odd fins. A plurality of spacers is formed on the substrate and on the sidewalls of the odd fins, wherein each spacer has a substantially vertical sidewall. A plurality of even fins is then formed on the substrate between the spacers.

In an embodiment, the substantially vertical-sidewall spacers are formed as follows. A substantially conformal material layer is formed over the substrate. An anisotropic treatment partially changing the etching selectivity of the material layer is performed to the material layer. The material layer is then selectively etched. The anisotropic treatment may include an ion-implantation process or a plasma treatment.

The semiconductor structure for forming FinFETs of this invention includes a semiconductor substrate, a plurality of odd fins of the FinFETs on the substrate, and a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs. The odd fins of the FinFETs are defined from the substrate. The even fins of the FinFETs are different from the odd fins of the FinFETs in at least one of the width and the material, and may be further different from the odd fins of the FinFETs in the height.

The semiconductor structure for forming FinFETs of this invention includes a semiconductor substrate, a plurality of

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odd fins of the FinFETs on the substrate, and a plurality of even fins of the FinFETs on the substrate between the odd fins of the FinFETs. The even fins of the FinFETs are different from the odd fins of the FinFETs in at least one of the width and the material, and may be further different from the odd fins of the FinFETs in the height.

The semiconductor structure for forming FinFETs of this invention includes a semiconductor substrate, a plurality of first fins of the FinFETs on the substrate, and a plurality of second fins of the FinFETs on the substrate. Each of the second fins of the FinFETs is located between two first fins of the FinFETs. The second fins of the FinFETs are different from the first fins of the FinFETs in at least one of the width and the material, and may be further different from the first fins of the FinFETs in the height.

In the method for fabricating FinFETs of this invention, since the odd fins are formed prior to the even fins, the fin pattern density is greatly lowered and the thickness of the photoresist layer can be reduced, so that the development of fin patterns is much easier. Moreover, since the even fins are not formed simultaneously with the odd fins, the width thereof can be controlled by the width of each spacer or the thickness of the substantially conformal layer for forming the spacers, and the height thereof can be controlled by the growth process thereof, the even fins can be different from the odd fins in at least one of the height, the width and the material.

In order to make the aforementioned and other objects, features and advantages of the present invention comprehensible, a preferred embodiment accompanied with figures is described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-6 illustrate, in a cross-sectional view, a method for fabricating FinFETs patterning process according to an embodiment of this invention, wherein FIG. 6 also illustrates a semiconductor structure according to the embodiment.

DESCRIPTION OF EMBODIMENTS

It is noted that the following embodiment is intended to further explain this invention but not to limit its scope.

FIGS. 1-6 illustrate, in a cross-sectional view, a method for fabricating FinFETs patterning process according to an embodiment of this invention, wherein FIG. 6 also illustrates a semiconductor structure according to the embodiment.

Referring to FIG. 1, a semiconductor substrate 10 is provided, which may be a lightly doped single-crystal silicon substrate. A hard mask layer 12 is then formed on the substrate 10, possibly including silicon nitride (SiN) or SiON. When the hard mask layer 12 includes SiN, pad oxide 14 may be formed on the substrate 10 in advance. A patterned photoresist layer 16 with the patterns of the odd fins of the FinFETs is then formed on the hard mask layer 12. The photoresist layer 16 may include a positive or negative photoresist material.

Referring to FIG. 2, after the hard mask layer 12 is patterned using the patterned photoresist layer 16 as a mask, the substrate 10 is successively etched and patterned using the patterned photoresist layer 16 and the patterned hard mask layer 12a as a mask to form a plurality of odd fins 10a. The patterned photoresist layer 16 is usually entirely consumed in the patterning process.

Referring to FIG. 3, a substantially conformal material layer 18 is formed over the substrate 10. The material layer 18 may be formed by an atomic layer deposition (ALD) process

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or a furnace deposition process, and the material thereof may be SiN. An anisotropic treatment **20** partially changing the etching selectivity of the material layer **18** is then performed to the material layer **18**, forming low-selectivity regions **18a** on the substrate **10** and on the sidewalls of the odd fins **10a**, and high-selectivity regions **18b** over the odd fins **10a** and under the recesses regions of the material layer **18**. The anisotropic treatment **20** is conducted in a manner such that the interface between any pair of a low-selectivity region **18a** and an adjacent high-selectivity region **18b** under a recesses region of the material layer **18** is substantially vertical. The anisotropic treatment **20** may include an ion-implantation process or a plasma treatment.

Referring to FIG. 4, a selective etching process is performed to remove the high-selectivity regions **18b**, leaving the low-selectivity regions **18a** as a plurality of spacers on the substrate **10** and on the sidewalls of the odd fins **10a**, wherein each of the spacers **18a** has a substantially vertical sidewall because the interface between any pair of a low-selectivity region **18a** and an adjacent high-selectivity region **18b** under a recesses region of the material layer **18** is substantially vertical.

In an embodiment, the material layer **18** includes SiN, the anisotropic treatment **20** includes an ion-implantation process that implants carbon ions in the to-be-removed portions of the material layer **18**, and the selective etching for removing the high-selectivity regions **18b** of the material layer **18** utilizes phosphoric acid.

Referring to FIG. 5, a plurality of even fins **20** is then formed on the substrate **10** between the spacers **18a**, possibly by an epitaxy process as a selective deposition process based on the exposed surfaces of the semiconductor substrate **10**. When the semiconductor substrate **10** includes Si, the product material of the epitaxy process may be Si, SiGe or SiC.

Since the even fins **20** are not formed simultaneously with the odd fins **10a**, the material thereof can be different from that of the odd fins **10a**. For example, it is possible that the odd fins **10a** include Si and the even fins **20** comprise SiC or SiGe. Nevertheless, the even fins **20** may alternatively be formed from the same material (e.g., Si) of the odd fins **10a**, which is namely the material of the substrate **10**, by epitaxy.

In addition, the width of each even fin **20** can be controlled by the width of each spacer **18a** (see FIG. 4), which is in turn controlled by the deposition thickness of the substantially conformal material layer **18** for forming the spacers **18a** (see FIG. 3). The height of the even fins **20** can be controlled by the growth process of the even fins **20**. Accordingly, the even fins **20** may be different from the odd fins **10a** in at least one of the height, the width and the material.

Referring to FIG. 6, the patterned hard mask layer **12a** and the spacers **18a** are removed, leaving the odd fins **10a** and even fins **20** that are arranged alternately.

FIG. 6 also illustrates a semiconductor structure according to the embodiment of this invention. The semiconductor structure includes odd fins **10a** and even fins **20** that are arranged alternately. The odd fins **10a** are defined from the semiconductor substrate **10**. The even fins **20** may be different from the odd fins **10a** in at least one of the width and the material, and may be further different from the odd fins **10a** also in height, as mentioned above.

In the above embodiment of this invention, since the odd fins are formed prior to the even fins, their pattern density is greatly reduced and the thickness of the photoresist layer can be reduced, so that the development of fin patterns is much easier.

This invention has been disclosed above in the preferred embodiments, but is not limited to those. It is known to

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persons skilled in the art that some modifications and innovations may be made without departing from the spirit and scope of this invention. Hence, the scope of this invention should be defined by the following claims.

What is claimed is:

1. A semiconductor structure for forming FinFETs, comprising

a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material; and

a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

2. The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

3. The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material.

4. The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

5. The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.

6. The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.

7. The semiconductor structure of claim 1, wherein the odd fins of the FinFETs are electrically connected to the semiconductor substrate.

8. The semiconductor structure of claim 1, wherein the semiconductor substrate is a single layer structure.

9. A semiconductor structure for forming FinFETs, comprising

a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

a plurality of odd fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and

a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

10. The semiconductor structure of claim 9, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

11. The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise an epitaxy material.

12. The semiconductor structure of claim 11, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

13. The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si.

14. The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise SiC or SiGe.

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15. A semiconductor structure for forming FinFET, comprising

a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material:

a plurality of first fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and

a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.

16. The semiconductor structure of claim **15**, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.

17. The semiconductor structure of claim **15**, wherein the second fins of the FinFETs comprise an epitaxy material.

18. The semiconductor structure of claim **17**, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.

19. The semiconductor structure of claim **15**, wherein the first fins of the FinFETs comprise Si.

20. The semiconductor structure of claim **15**, wherein the second fins of the FinFETs comprise SiC or SiGe.

* * * * *

Exhibit E

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(45) **Date of Patent:** Apr. 24, 2018

(58) **Field of Classification Search**

CPC H01L 21/823431; H01L 21/823437; H01L
21/823481; H01L 21/308; H01
21/31051; H01L 21/31144; H01L
29/66545; H01L 21/76224; H01L
21/823475; H01L 29/66795; H01L
27/11807; H01L 29/0642
USPC 257/288, 368, 369; 438/151, 197, 199
See application file for complete search history.

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 15/660,991

(22) Filed: **Jul. 27, 2017**

(30) **Foreign Application Priority Data**

Jun. 29, 2017 (CN) 2017 1 0516576

(51) **Int. Cl.**

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<i>H01L 21/8234</i>	(2006.01)
<i>H01L 21/762</i>	(2006.01)
<i>H01L 29/66</i>	(2006.01)
<i>H01L 21/311</i>	(2006.01)

(52) U.S. Cl.

CPC *H01L 21/823481* (2013.01); *H01L 21/31144* (2013.01); *H01L 21/76224* (2013.01); *H01L 21/823475* (2013.01); *H01L 29/66545* (2013.01); *H01L 29/66795* (2013.01)

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Primary Examiner — Shahed Ahmed

(74) *Attorney, Agent, or Firm* — Winston Hsu

(57) **ABSTRACT**

A method for fabricating semiconductor device includes the steps of: forming a fin-shaped structure on a substrate; forming a shallow trench isolation (STI) around the fin-shaped structure; forming a gate layer on the fin-shaped structure and the STI; removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench; and forming a dielectric layer into the trench to form a single diffusion break (SDB) structure.

12 Claims, 5 Drawing Sheets

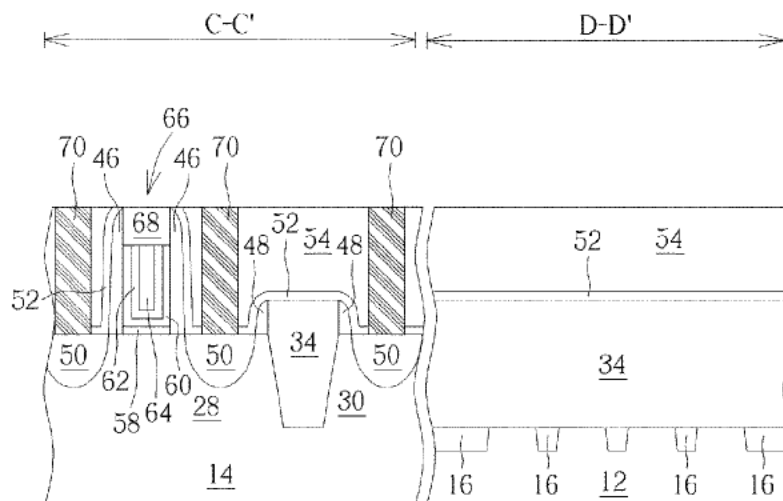


FIG. 10

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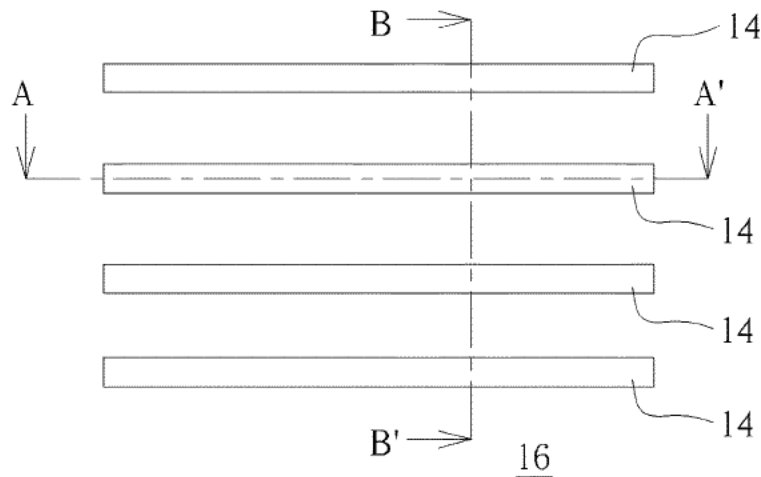


FIG. 1

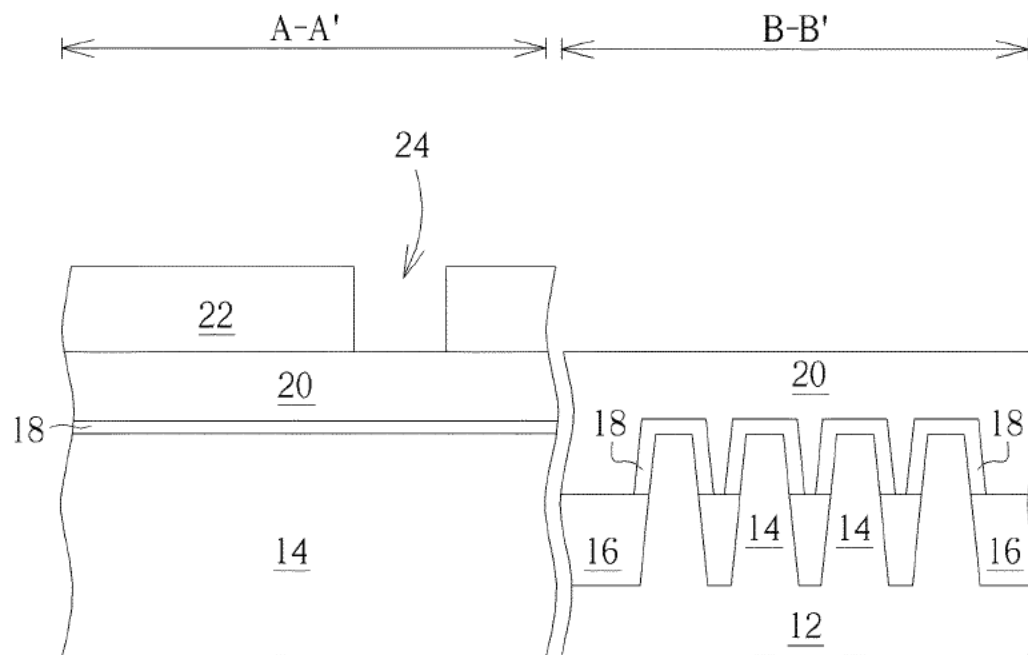


FIG. 2

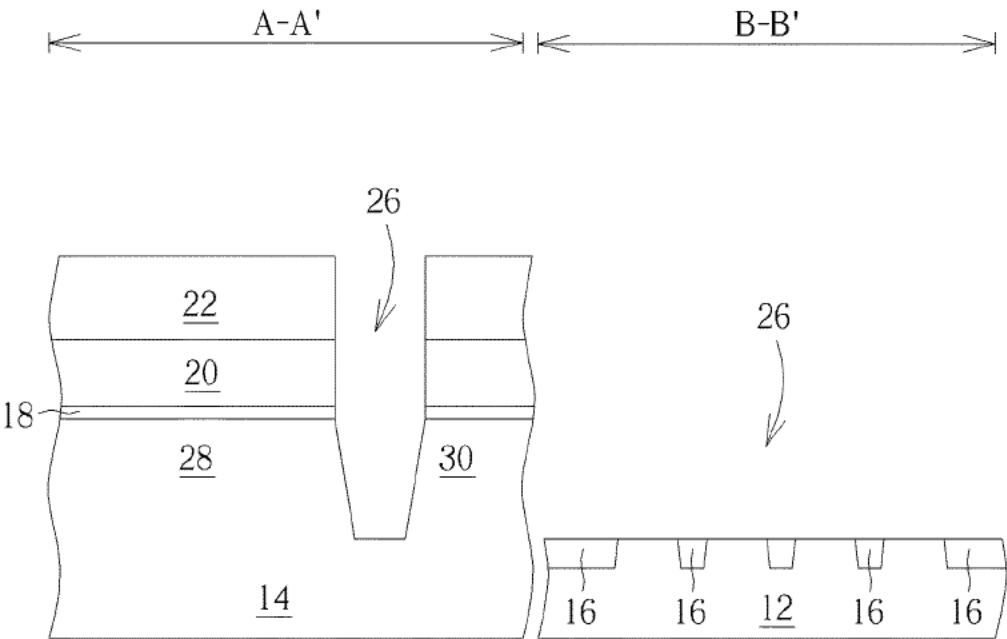


FIG. 3

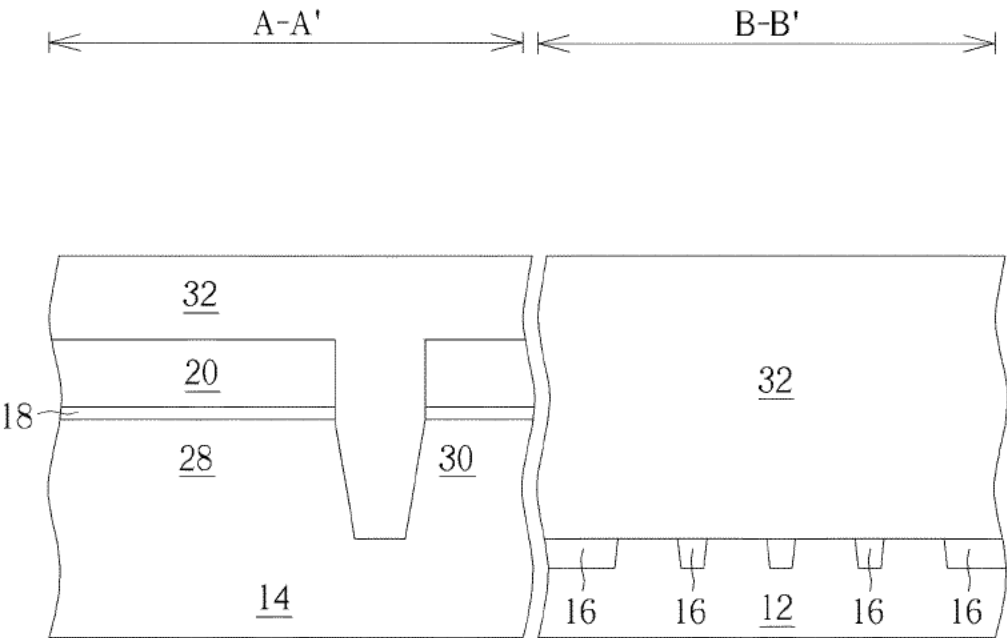


FIG. 4

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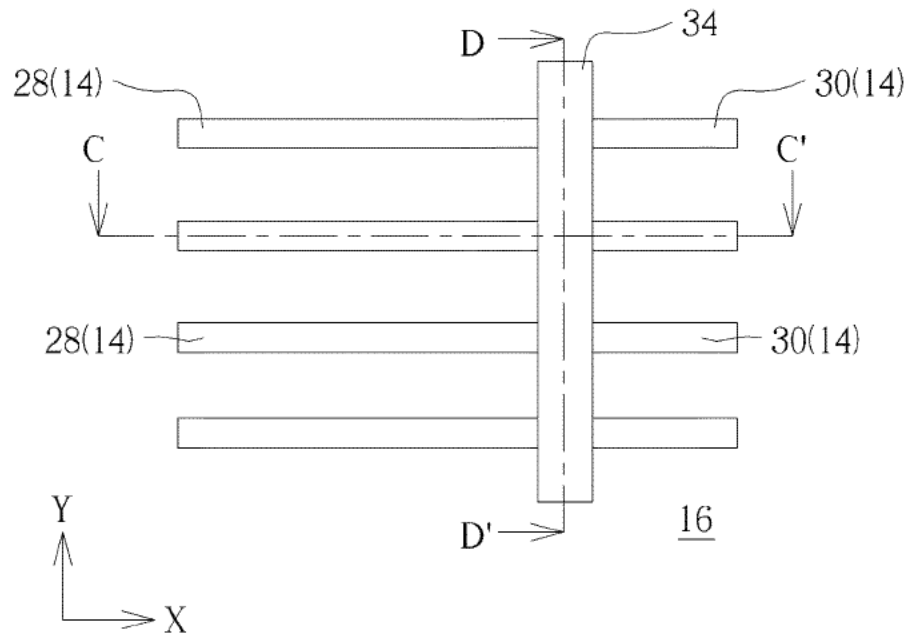


FIG. 5

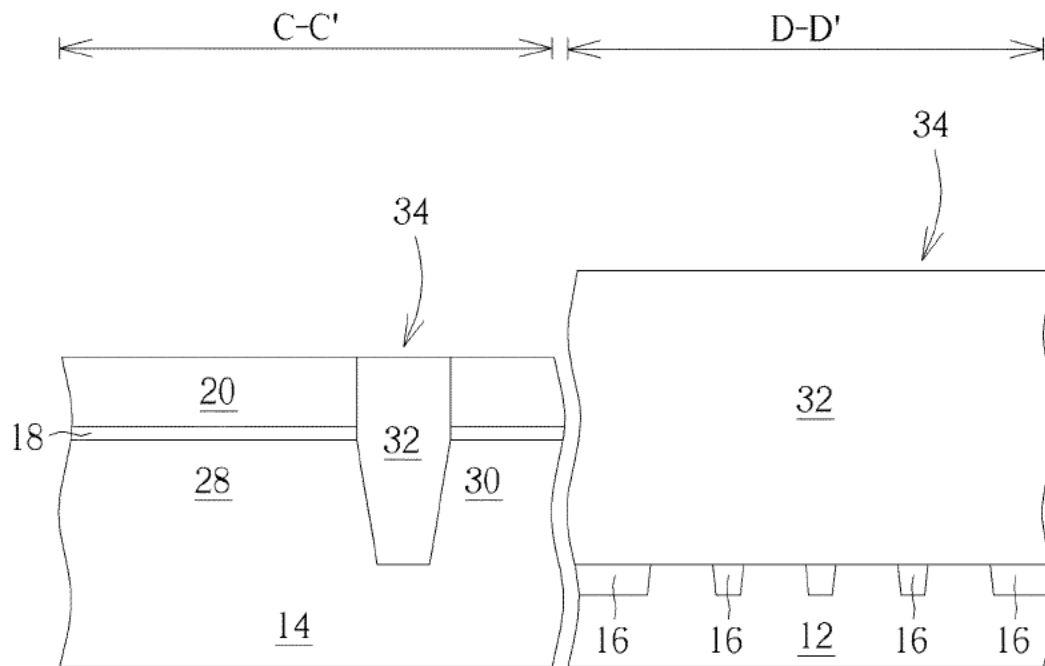


FIG. 6

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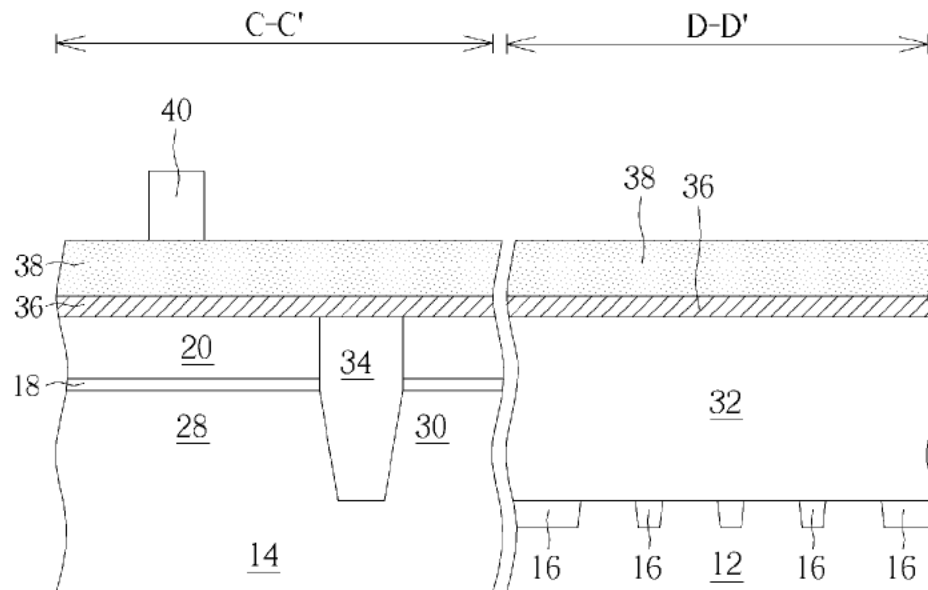


FIG. 7

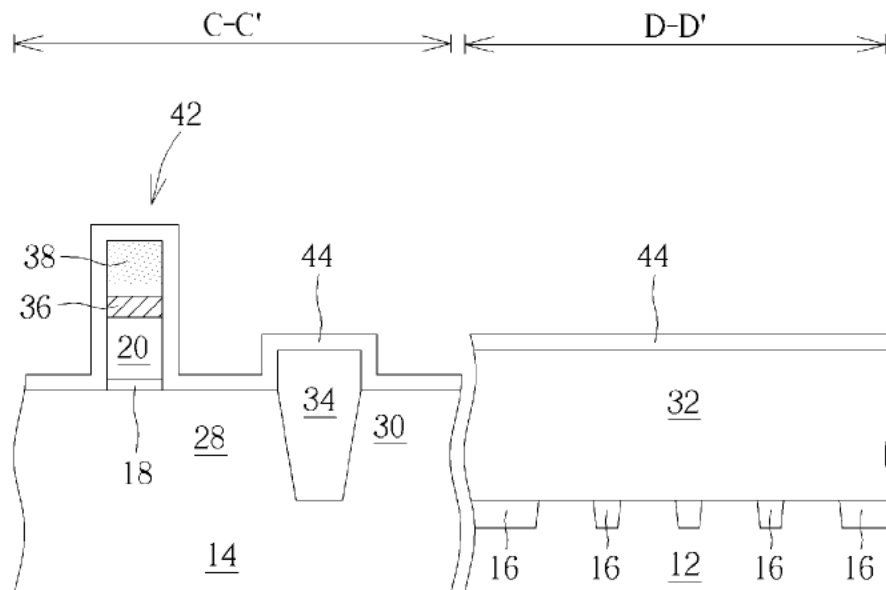


FIG. 8

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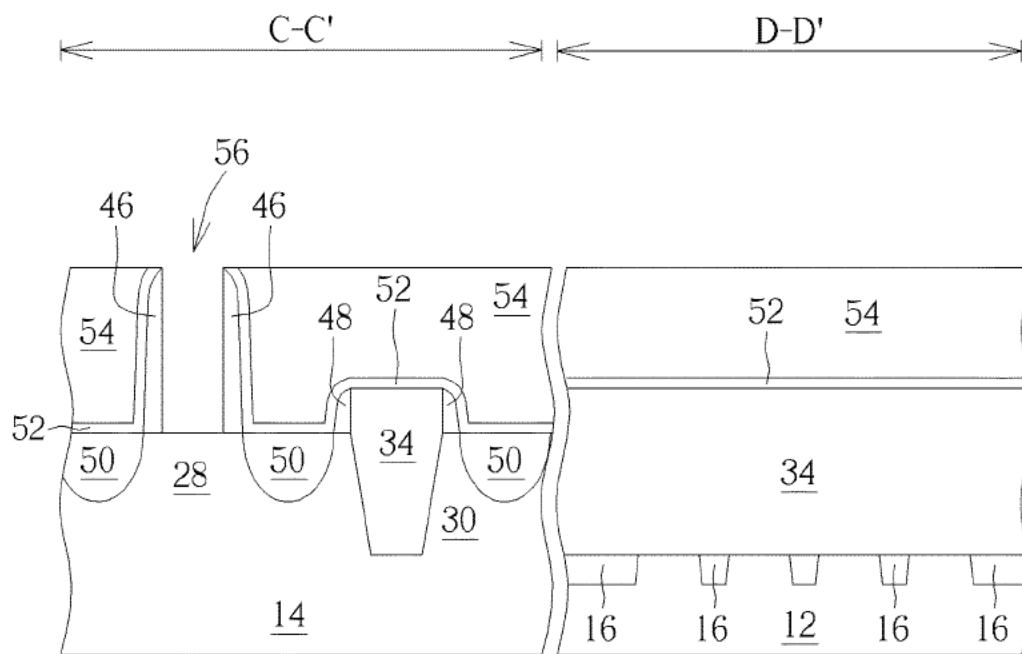


FIG. 9

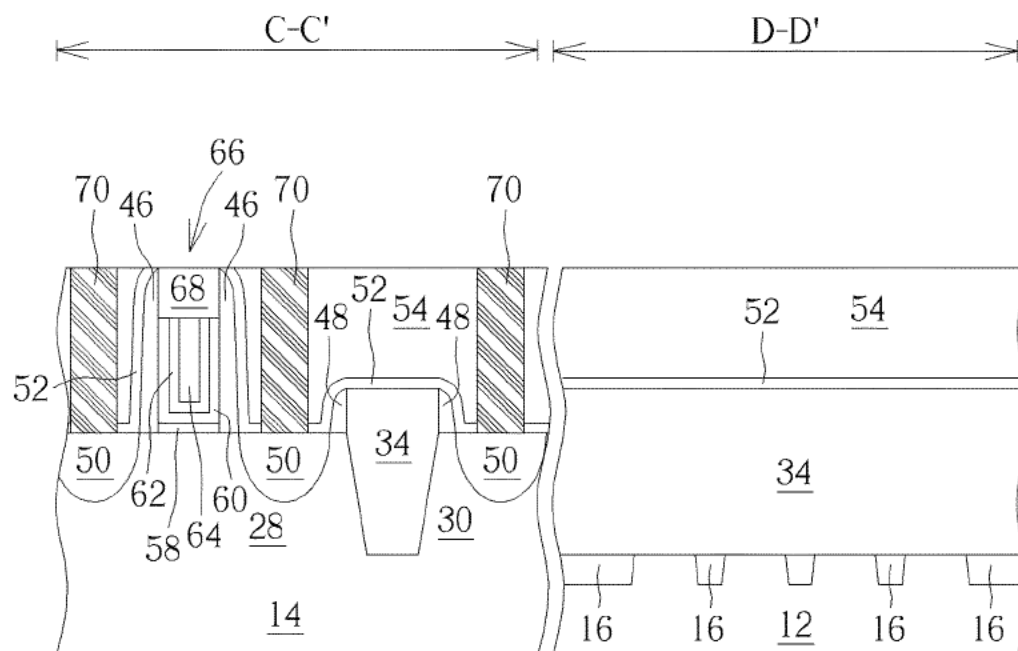


FIG. 10

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**SEMICONDUCTOR DEVICE AND METHOD
FOR FABRICATING THE SAME****BACKGROUND OF THE INVENTION**

1. Field of the Invention

The invention relates to a method for fabricating semiconductor device, and more particularly to a method for dividing fin-shaped structure to form single diffusion break (SDB) structure.

2. Description of the Prior Art

With the trend in the industry being towards scaling down the size of the metal oxide semiconductor transistors (MOS), three-dimensional or non-planar transistor technology, such as fin field effect transistor technology (FinFET) has been developed to replace planar MOS transistors. Since the three-dimensional structure of a FinFET increases the overlapping area between the gate and the fin-shaped structure of the silicon substrate, the channel region can therefore be more effectively controlled. This way, the drain-induced barrier lowering (DIBL) effect and the short channel effect are reduced. The channel region is also longer for an equivalent gate length, thus the current between the source and the drain is increased. In addition, the threshold voltage of the fin FET can be controlled by adjusting the work function of the gate.

In current FinFET fabrication, after shallow trench isolation (STI) is formed around the fin-shaped structure part of the fin-shaped structure and part of the STI could be removed to form a trench, and insulating material is deposited into the trench to form single diffusion break (SDB) structure or isolation structure. However, the integration of the SDB structure and metal gate fabrication still remains numerous problems. Hence how to improve the current FinFET fabrication and structure has become an important task in this field.

SUMMARY OF THE INVENTION

According to an embodiment of the present invention, a method for fabricating semiconductor device includes the steps of: forming a fin-shaped structure on a substrate; forming a shallow trench isolation (STI) around the fin-shaped structure; forming a gate layer on the fin-shaped structure and the STI; removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench; and forming a dielectric layer into the trench to form a single diffusion break (SDB) structure.

According to another aspect of the present invention, a semiconductor device includes: a fin-shaped structure on a substrate; a single diffusion break (SDB) structure in the fin-shaped structure to divide the fin-shaped structure into a first portion and a second portion; a gate structure on the first portion; and a contact etch stop layer (CESL) adjacent to the gate structure and extending to cover the SDB structure.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-10 illustrate a method for fabricating a semiconductor device according to an embodiment of the present invention.

DETAILED DESCRIPTION

Referring to FIGS. 1-2, in which FIG. 1 is a top view illustrating a method for fabricating a semiconductor device according to an embodiment of the present invention, the left portion of FIG. 2 illustrates a cross-sectional view of FIG. 1 for fabricating the semiconductor device along the sectional line AA', and the right portion of FIG. 2 illustrates a cross-sectional view of FIG. 1 for fabricating the semiconductor device along the sectional line BB'. As shown in FIGS. 1-2, a substrate 12, such as a silicon substrate or silicon-on-insulator (SOI) substrate is first provided, and a plurality of fin-shaped structures 14 are formed on the substrate 12. It should be noted that even though four fin-shaped structures 14 are disposed on the substrate 12 in this embodiment, it would also be desirable to adjust the number of fin-shaped structures 14 depending on the demand of the product, which is also within the scope of the present invention.

Preferably, the fin-shaped structures 14 of this embodiment could be obtained by a sidewall image transfer (SIT) process. For instance, a layout pattern is first input into a computer system and is modified through suitable calculation. The modified layout is then defined in a mask and further transferred to a layer of sacrificial layer on a substrate through a photolithographic and an etching process. In this way, several sacrificial layers distributed with a same spacing and of a same width are formed on a substrate. Each of the sacrificial layers may be stripe-shaped. Subsequently, a deposition process and an etching process are carried out such that spacers are formed on the sidewalls of the patterned sacrificial layers. In a next step, sacrificial layers can be removed completely by performing an etching process. Through the etching process, the pattern defined by the spacers can be transferred into the substrate underneath, and through additional fin cut processes, desirable pattern structures, such as stripe patterned fin-shaped structures could be obtained.

Alternatively, the fin-shaped structures 14 could also be obtained by first forming a patterned mask (not shown) on the substrate 12, and through an etching process, the pattern of the patterned mask is transferred to the substrate 12 to form the fin-shaped structures 14. Moreover, the formation of the fin-shaped structures 14 could also be accomplished by first forming a patterned hard mask (not shown) on the substrate 12, and a semiconductor layer composed of silicon germanium is grown from the substrate 12 through exposed patterned hard mask via selective epitaxial growth process to form the corresponding fin-shaped structures 14. These approaches for forming fin-shaped structure are all within the scope of the present invention.

Next, a shallow trench isolation (STI) 16 is formed around the fin-shaped structures 14. In this embodiment, the formation of the STI 16 could be accomplished by conducting a flowable chemical vapor deposition (FCVD) process to form a silicon oxide layer on the substrate 12 and covering the fin-shaped structures 14 entirely. Next, a chemical mechanical polishing (CMP) process along with an etching process are conducted to remove part of the silicon oxide layer so that the top surface of the remaining silicon oxide

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is even with or slightly lower than the top surface of the fin-shaped structures **14** for forming the STI **16**.

Next, a gate dielectric layer **18** and a gate layer **20** are formed to cover the fin-shaped structures **14** and the STI **16** entirely, and a patterned mask **22** is formed on the gate layer **20**, in which the patterned mask **22** includes an opening **24** to expose part of the gate layer **20** surface. In this embodiment, the gate dielectric layer **18** preferably includes silicon oxide and the gate layer **20** is selected from the group consisting of amorphous silicon and polysilicon. The patterned mask **22** could additionally include an organic dielectric layer (ODL), a silicon-containing hard mask bottom anti-reflective coating (SHB), and a patterned resist and the step of forming the opening **24** in the patterned mask **22** could be accomplished by using the patterned resist as mask to remove part of the SHB and part of the ODL.

Next, as shown in FIG. 3, an etching process is conducted by using the patterned mask **22** as mask to remove part of the gate layer **20**, part of the gate dielectric layer **18**, and part of the fin-shaped structures **14** to form a trench **26**. The trench **26** preferably divides the fin-shaped structures **14** into two portions including a first portion **28** on the left side of the trench **26** and a second portion **30** on the right side of the trench **26**.

Next, as shown in FIG. 4, a planar dielectric layer **32** is formed into the trench **26** and on the gate layer **20**, in which the dielectric layer **32** preferably fills the trench **26** entirely so that the top surface of the dielectric layer **32** is slightly higher than the top surface of the gate layer **20**. In this embodiment, the dielectric layer **32** and the STI **16** are preferably made of different material, in which the dielectric layer **32** filled into the trench **26** preferably includes silicon nitride while the STI **16** preferably includes silicon oxide, but not limited thereto. Nevertheless, according to an embodiment of the present invention, the dielectric layer **32** and the STI **16** could also include same material such as silicon oxide, which is also within the scope of the present invention.

Referring to FIGS. 5-6, in which FIG. 5 is a top view illustrating the fabrication of the semiconductor device following FIG. 4, the left portion of FIG. 6 illustrates a cross-sectional view of FIG. 5 along the sectional line CC' and the right portion of FIG. 6 illustrates a cross-sectional view of FIG. 5 along the sectional line DD'. As shown in FIGS. 5-6, a planarizing process such as CMP is conducted to remove part of the dielectric layer **32** so that the top surface of the remaining dielectric layer **32** is even with the top surface of the gate layer **20**. This forms a single diffusion break (SDB) structure **34** protruding above the fin-shaped structures **14**, in which the top surfaces of the SDB structure **32** and the gate layer **20** are coplanar. As shown in FIG. 5, the fin-shaped structures **14** are disposed extending along a first direction (such as X-direction) and the SDB structure **34** is disposed extending along a second direction (such as Y-direction), in which the SDB structure **34** preferably separates each of the fin-shaped structures into two portions, including a first portion **28** on the left side of the SDB structure **34** and a second portion **30** on the right side of the SDB structure **34**.

Next, as shown in FIG. 7, a pattern transfer process is conducted by first forming a first hard mask **36**, a second hard mask **38**, and a patterned mask **40** on the gate layer **20** while the patterned mask **40** not covering the SDB structure **34**. In this embodiment, the first hard mask **36** and the second hard mask **38** are composed of different material, in which the first hard mask **36** preferably includes silicon nitride and the second hard mask **38** preferably includes

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silicon oxide, but not limited thereto. The patterned hard mask **40** could be a single patterned resist or could be made of same material as the patterned mask **22** from FIG. 2, and in such instance, the patterned mask **40** could include a tri-layered structure such as an organic dielectric layer (ODL), a silicon-containing hard mask bottom anti-reflective coating (SHB), and a patterned resist.

Next, as shown in FIG. 8, one or multiple etching processes are conducted by using the patterned mask **40** as mask to remove part of the second hard mask **38**, part of the first hard mask **36**, part of the gate layer **20**, and part of the gate dielectric layer **18** to form a gate structure **42** adjacent to the SDB structure **34**. It should be noted that no additional gate structure is formed directly on top of the SDB structure **34** during the formation of gate structure **42**, however, dummy gate (not shown) could be disposed on an edge of the fin-shaped structures **14** to stand on top of both the fin-shaped structures **14** and the STI **16** at the same time, in which the top surface of the dummy gate is even with the top surface of the gate structure **42**. Preferably, the top surface of the STI **16** is slightly lower than the top surface of the fin-shaped structure **14** while the top surface of the SDB structure **34** is higher than both the top surface of the fin-shaped structures **14** and the STI **16**. Moreover, the height of the SDB **34** protruding above the fin-shaped structures **14** is reduced slightly during the etching process so that the top surface of the SDB **34** would become slightly lower than the top surface of the gate layer **20**. Next, a cap layer **44** is formed on the fin-shaped structures **14** to cover the gate structure **42** and the SDB structure **34** at the same time. In this embodiment, the cap layer **44** could include material such as SiN, SiO₂, SiON, SiCN, or combination thereof.

Next, as shown in FIG. 9, an etching process is conducted to remove part of the cap layer **44** for forming a first spacer **46** adjacent to the sidewalls of the gate structure **42** and at the same time forming a second spacer **48** on the sidewalls of the SDB structure **34**. Next, source/drain regions **50** and/or epitaxial layers (not shown) are formed in the fin-shaped structures **14** adjacent to two sides of the first spacer **46** and second spacer **48**, and silicides (not shown) could be selectively formed on the surface of the source/drain regions **50** and/or epitaxial layers afterwards. In this embodiment, each of the first spacer **46** and second spacer **48** could be a single spacer or a composite spacer, such as a spacer including but not limited to for example an offset spacer and a main spacer. Preferably, the offset spacer and the main spacer could include same material or different material while both the offset spacer and the main spacer could be made of material including but not limited to for example SiO₂, SiN, SiON, SiCN, or combination thereof. The source/drain regions **50** could include dopants and epitaxial material of different conductive type depending on the type of device being fabricated. For example, the source/drain regions **50** on an NMOS region could include SiC or SiP while the source/drain regions **50** on a PMOS region could include SiGe, but not limited thereto.

Next, a contact etch stop layer (CESL) **52** is formed on the surface of the fin-shaped structures **14** and covering the gate structure **42** and the SDB structure **34**, and an interlayer dielectric (ILD) layer **54** is formed on the CESL **52**. Next, a planarizing process such as CMP is conducted to remove part of the ILD layer **54** and part of the CESL **52** for exposing the gate layer **20** made of polysilicon, in which the top surface of the gate layer **20** is even with the top surface of the ILD layer **52**.

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Next, a replacement metal gate (RMG) process is conducted to transform the gate structure **42** into a metal gate. For instance, the RMG process could be accomplished by first performing a selective dry etching or wet etching process using etchants including but not limited to for example ammonium hydroxide (NH₄OH) or tetramethylammonium hydroxide (TMAH) to remove the second hard mask **38**, first hard mask **36**, gate layer **20**, and even gate dielectric layer **18** from gate structure **42** for forming a recess **56** in the ILD layer **54**.

Next, as shown in FIG. **10**, a selective interfacial layer **58** or gate dielectric layer (not shown), a high-k dielectric layer **60**, a work function metal layer **62**, and a low resistance metal layer **64** are formed in the recess **56**, and a planarizing process such as CMP is conducted to remove part of low resistance metal layer **64**, part of work function metal layer **62**, and part of high-k dielectric layer **60** to form metal gate **66**. Next, part of the low resistance metal layer **64**, part of the work function metal layer **62**, and part of the high-k dielectric layer **60** are removed to form another recess (not shown), and a hard mask **68** made of dielectric material including but not limited to for example silicon nitride is deposited into the recess so that the top surfaces of the hard mask **68** and ILD layer **54** are coplanar. In this embodiment, the gate structure or metal gate **66** fabricated through high-k last process of a gate last process preferably includes an interfacial layer **58** or gate dielectric layer (not shown), a U-shaped high-k dielectric layer **60**, a U-shaped work function metal layer **62**, and a low resistance metal layer **64**.

In this embodiment, the high-k dielectric layer **60** is preferably selected from dielectric materials having dielectric constant (k value) larger than **4**. For instance, the high-k dielectric layer **60** may be selected from hafnium oxide (HfO₂), hafnium silicon oxide (HfSiO₄), hafnium silicon oxynitride (HfSiON), aluminum oxide (Al₂O₃), lanthanum oxide (La₂O₃), tantalum oxide (Ta₂O₅), yttrium oxide (Y₂O₃), zirconium oxide (ZrO₂), strontium titanate oxide (SrTiO₃), zirconium silicon oxide (ZrSiO₄), hafnium zirconium oxide (HfZrO₄), strontium bismuth tantalate (SrBi₂Ta₂O₉, SBT), lead zirconate titanate (PbZr_xTi_{1-x}O₃, PZT), barium strontium titanate (Ba_xSr_{1-x}TiO₃, BST) or a combination thereof.

In this embodiment, the work function metal layer **62** is formed for tuning the work function of the metal gate in accordance with the conductivity of the device. For an NMOS transistor, the work function metal layer **62** having a work function ranging between 3.9 eV and 4.3 eV may include titanium aluminide (TiAl), zirconium aluminide (ZrAl), tungsten aluminide (WAl), tantalum aluminide (TaAl), hafnium aluminide (HfAl), or titanium aluminum carbide (TiAlC), but it is not limited thereto. For a PMOS transistor, the work function metal layer **62** having a work function ranging between 4.8 eV and 5.2 eV may include titanium nitride (TiN), tantalum nitride (TaN), tantalum carbide (TaC), but it is not limited thereto. An optional barrier layer (not shown) could be formed between the work function metal layer **62** and the low resistance metal layer **64**, in which the material of the barrier layer may include titanium (Ti), titanium nitride (TiN), tantalum (Ta) or tantalum nitride (TaN). Furthermore, the material of the low-resistance metal layer **64** may include copper (Cu), aluminum (Al), titanium aluminum (TiAl), cobalt tungsten phosphide (CoWP) or any combination thereof.

Next, a pattern transfer process is conducted by using a patterned mask (not shown) as mask to remove part of the ILD layer **54** adjacent to the metal gate **66** and SDB structure **34** for forming contact holes (not shown) exposing the

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source/drain regions **50** underneath. Next, metals including a barrier layer selected from the group consisting of Ti, TiN, Ta, and TaN and a low resistance metal layer selected from the group consisting of W, Cu, Al, TiAl, and CoWP are deposited into the contact holes, and a planarizing process such as CMP is conducted to remove part of aforementioned barrier layer and low resistance metal layer for forming contact plugs **70** electrically connecting the source/drain regions **50**. This completes the fabrication of a semiconductor device according to a preferred embodiment of the present invention.

Referring again to FIG. **10**, which further illustrates a structural view of a semiconductor device according to an embodiment of the present invention. As shown in FIG. **10**, the semiconductor device preferably includes a fin-shaped structure **14** disposed on the substrate **12**, a SDB structure **34** disposed within the fin-shaped structure **14** while protruding above the fin-shaped structure **14** and dividing the fin-shaped structure **14** into a first portion **28** and a second portion **30**, and a gate structure or metal gate **66** disposed on the first portion **28**. Preferably, the top surface of the metal gate **66** is even with or slightly higher than the top surface of the SDB structure **34**, the fin-shaped structure **14** is disposed extending along a first direction while the SDB structure **34** is disposed extending along a second direction, in which the first direction is orthogonal to the second direction as shown in FIG. **5**.

The semiconductor device also includes a first spacer **46** on the sidewalls of the metal gate **66**, a second spacer **48** on the sidewalls of the SDB structure **34**, a CESL **52** disposed adjacent to the first spacer **46** and extending to cover the second spacer **48** and SDB structure **34** while contacting the SDB structure **34** directly, and source/drain regions **50** disposed in the fin-shaped structure **14** adjacent to two sides of the first spacer **46** and second spacer **48**.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A method for fabricating semiconductor device, comprising:
 - forming a fin-shaped structure on a substrate;
 - forming a shallow trench isolation (STI) around the fin-shaped structure;
 - forming a gate layer on the fin-shaped structure and the STI;
 - removing part of the gate layer, part of the fin-shaped structure, and part of the STI to form a trench;
 - forming a dielectric layer into the trench to form a single diffusion break (SDB) structure; and
 - after forming the SDB structure forming an interlayer dielectric (ILD) layer on the SDB structure.
2. The method of claim 1, further comprising forming a gate dielectric layer on the fin-shaped structure before forming the gate layer.
3. The method of claim 2, further comprising:
 - forming a patterned mask on the gate layer; and
 - using the patterned mask as mask to remove part of the gate layer, part of the gate dielectric layer, and part of the fin-shaped structure to form the trench.
4. The method of claim 1, further comprising:
 - forming the dielectric layer into the trench and on the gate layer; and

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planarizing the dielectric layer so that the top surfaces of the dielectric layer and the gate layer are coplanar.

5. The method of claim 1, further comprising removing part of the gate layer after forming the SDB structure to form a gate structure adjacent to the SDB structure. 5

6. The method of claim 5, further comprising: forming a cap layer on the gate structure and the SDB structure; and

removing part of the cap layer to form a first spacer adjacent to the gate structure and a second spacer 10 adjacent to the SDB structure.

7. The method of claim 1, wherein the fin-shaped structure is disposed extending along a first direction and the SDB structure is disposed extending along a second direction.

8. The method of claim 7, wherein the first direction is 15 orthogonal to the second direction.

9. The method of claim 1, wherein the gate layer comprises amorphous silicon.

10. The method of claim 1, wherein the gate layer comprises polysilicon. 20

11. The method of claim 1, wherein the dielectric layer comprises silicon nitride.

12. The method of claim 1, wherein the dielectric layer comprises silicon oxide.

* * * * *

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CIVIL COVER SHEET

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I. (a) PLAINTIFFS

Longitude Licensing Ltd. and Marlin Semiconductor
I limited

(b) County of Residence of First Listed Plaintiff _____
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorneys (Firm Name, Address, and Telephone Number)

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Pkwy., Longview, TX 75604; 903-757-6400

DEFENDANTS

Lenovo Group Limited, et al.

County of Residence of First Listed Defendant _____
(IN U.S. PLAINTIFF CASES ONLY)

NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF
THE TRACT OF LAND INVOLVED.

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1 U.S. Government Plaintiff ☒ 3 Federal Question
(U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant ☐ 4 Diversity
(Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant)

- | | PTF | DEF | | PTF | DEF |
|---|----------------------------|----------------------------|---|----------------------------|----------------------------|
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| Citizen of Another State | ☐ 2 | ☐ 2 | Incorporated and Principal Place of Business In Another State | ☐ 5 | ☐ 5 |
| Citizen or Subject of a Foreign Country | ☐ 3 | ☐ 3 | Foreign Nation | ☐ 6 | ☐ 6 |

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CONTRACT	TORTS	FORFEITURE/PENALTY	BANKRUPTCY	OTHER STATUTES
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REAL PROPERTY ☐ 210 Land Condemnation ☐ 220 Foreclosure ☐ 230 Rent Lease & Ejectment ☐ 240 Torts to Land ☐ 245 Tort Product Liability ☐ 290 All Other Real Property	CIVIL RIGHTS ☐ 440 Other Civil Rights ☐ 441 Voting ☐ 442 Employment ☐ 443 Housing/Accommodations ☐ 445 Amer. w/Disabilities - Employment ☐ 446 Amer. w/Disabilities - Other ☐ 448 Education PRISONER PETITIONS Habeas Corpus: ☐ 463 Alien Detainee ☐ 510 Motions to Vacate Sentence ☐ 530 General ☐ 535 Death Penalty Other: ☐ 540 Mandamus & Other ☐ 550 Civil Rights ☐ 555 Prison Condition ☐ 560 Civil Detainee - Conditions of Confinement			

V. ORIGIN (Place an "X" in One Box Only)

- ☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from Another District (specify) ☐ 6 Multidistrict Litigation - Transfer ☐ 8 Multidistrict Litigation - Direct File

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing (Do not cite jurisdictional statutes unless diversity):

35 U.S.C. § 271

Brief description of cause:
Patent Infringement

VII. REQUESTED IN COMPLAINT:

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CHECK YES only if demanded in complaint:

JURY DEMAND: ☒ Yes ☐ No

VIII. RELATED CASE(S) IF ANY

(See instructions):

JUDGE

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DATE

02/13/2025

SIGNATURE OF ATTORNEY OF RECORD

/s/ Andrea L. Fair

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