Improvements of NBTI Reliability in SiGe p-FETs

J. Franco[1], B. Kaczer, M. Cho, G. Eneman[1,2], G. Groeseneken[1]
IMEC
Kapeldreef 75, B-3000 Leuven, Belgium
Phone: +32 16 28 10 85; fax: +32 16 28 17 06; e-mail: Jacopo.Franco@imec.be
[1]also at ESAT Dept., K.U. Leuven, Belgium
[2] also FWO-Vlaanderen, Belgium

T. Grasser
Christian Doppler Laboratory for TCAD
Institute for Microelectronics, TU Wien
Gusshausstrasse 27-29, 1040 Wien, Austria

***Abstract*—NBTI reliability of buried SiGe channel p-FETs is investigated as a function of Ge concentration, SiGe layer thickness and Si cap thickness. Measurements show that NBTI reliability can be dramatically improved by varying these three parameters, i.e., increasing the Ge fraction, increasing the thickness of the SiGe layer, and reducing the Si cap thickness. Consequently, it is demonstrated that SiGe devices are a promising option for improving NBTI in highly-scaled sub-1nm EOT pFETs.**

Keywords: NBTI, SiGe, Ge, Reliability, pFETs, thin EOT, high-mobility substrates

I. INTRODUCTION

The negative bias temperature instability (NBTI) is a major reliability problem for the semiconductor industry [1]. Reduction of effective oxide thickness (EOT), which is one of the most efficient ways to improve MOSFET performance, enhances NBTI due to increased oxide electric field (E_{ox}). As a consequence, 10 year lifetime can be guaranteed for sub-1nm EOT Si pFETs only at gate overdrive voltages far below the expected operating voltages (Fig. 1).

Another way to improve FET performance is the use of a strained SiGe channel [2-6]. In this paper the NBTI reliability of such SiGe devices is investigated. All SiGe pFETs under test showed better NBTI reliability with respect to their Si channel counterparts. As can be seen from Fig. 1, an *ad hoc* optimization of SiGe device gate-stacks at the moment seems to be the only solution to the NBTI issue for sub-1nm EOT devices, as it allows to significantly increase the operating gate overdrive (V_{op}) while still guaranteeing 10 year device lifetime.

II. EXPERIMENTAL

The buried SiGe channel p-FETs used in this work were fabricated at IMEC on 300 mm (100) Si wafers. A cross-sectional sketch of the final device and a band diagram of this type of stack in inversion are depicted in Fig. 2.

After a pre-epi clean, an HCl etchback of Si was performed to level the surface of the final grown structure to the shallow trench isolation (STI). A 2nm-thick Si buffer was grown at 500°C from SiH_4 precursor to guarantee a high quality starting Si surface for the following growth of a compressively strained thin $Si_{1-x}Ge_x$ layer with thickness varying between 3nm and 7nm. Ge fractions were x=0.45 or x=0.55. Epitaxial growth was performed from SiH_4 and GeH_4 precursors at 500°C for x=0.45 and at 450°C for x=0.55. On top of the $Si_{1-x}Ge_x$ layer, a thin undoped Si cap was grown from SiH_4 at 500°C for x=0.45 and at 475°C for x=0.55. The physical thicknesses of this thin Si cap varied between 0.65nm and 2nm (as estimated from C-V curves and TEM pictures of the final device). A detailed description of the epi-process can be found elsewhere [7-8].

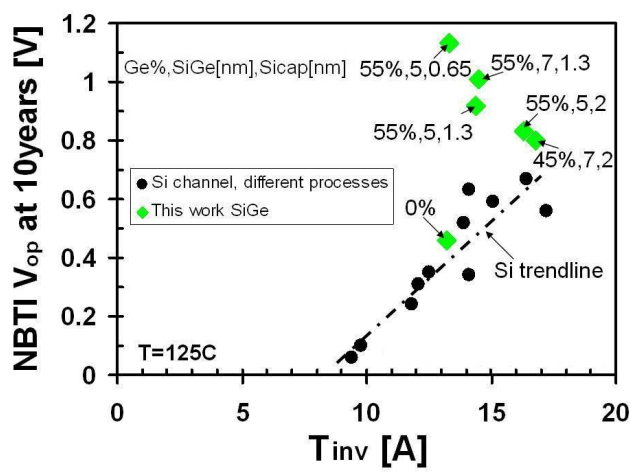

Figure 1. Plot of the operating overdrive voltage (V_{op}) for 10 year lifetime assuming a 30mV threshold voltage shift criterion under NBTI stress condition (T=125°C) vs. the capacitance equivalent thickness evaluated in inversion (T_{inv}), for Si channel devices with different processing used as a reference and for SiGe pFETs used in this work. For low T_{inv}, Si devices V_{op} is below the expected operating voltage. In contrast to that, optimized SiGe devices presented in this study show improved lifetime, and therefore provide a potential solution for the NBTI issue toward sub-1nm EOT devices.

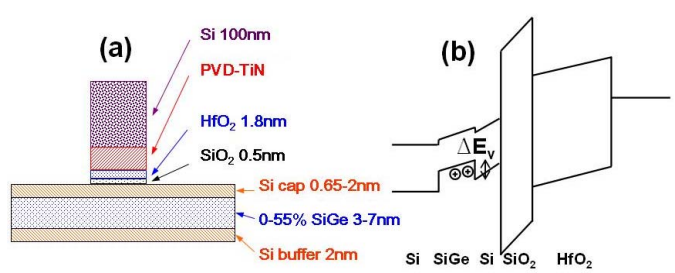

Figure 2. (a) Gate-stack sketch of the SiGe devices under test; (b) Band diagram in inversion. Si cap acts as a barrier (ΔE_v) for holes.

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Gate stack fabrication started with a very thin (0.8nm) wet chemical oxidation of the Si cap. On top of this SiO_2 interfacial layer (IL), ~1.8nm of HfO_2 were deposited using atomic layer deposition (ALD). Finally, a TiN metal gate was deposited. Channel width and length of the devices used in this work were 10 µm and 1 µm respectively. Effective mobility enhancement factor of our SiGe devices with respect to Si control ranged between 1.5x and 2.2x, depending on the process parameters.

NBTI stress experiments were performed using the extended measure-stress-measure technique [9]. Devices were stressed at $T = 125^{o}C$ with several gate overdrive conditions and up to 2000s of stress time. To monitor the degradation, stress was interrupted several times for sensing source current at $V_G \sim V_{th}$. Measured source current was converted to threshold voltage shift using the IsVg curve of the fresh device as a conversion table. Relaxation traces were recorded for ~12s. However for lifetime prediction ΔV_{th} was evaluated at t_{relax}=2ms, i.e., the minimum delay to get a reliable measurement with the used setup (2x Keithley 2602 Source Meter). Such delay was fixed in all the experiments to allow cross-comparison. For each gate voltage the stress time needed to reach a failure criterion, assumed as 30mV threshold voltage shift, is extracted. The 10 year lifetime operating overdrive (V_{op}) is then extrapolated fitting a power law to the lifetime vs. gate overdrive dataset (Fig. 3-5).

The three major process parameters of our SiGe pMOSFETs, i.e. the Ge concentration, the SiGe layer thickness and the Si cap thickness, were varied separately in order to assess their impact on NBTI reliability.

III. Results and Discussion

We now report the main experimental observations followed by a discussion of possible explanations for the observed NBTI improvement.

A. Experimental Observations

Because of the valence band offset between the SiGe and the Si cap (see Fig. 2b) inversion channel holes are confined in the SiGe layer, which therefore acts as a quantum well (QW) for holes. This causes the Si cap thickness to lower the inversion capacitance as compared to the accumulation capacitance. For these devices it is therefore necessary to report the capacitance-equivalent thickness in inversion (T_{inv}, evaluated at $V_G=V_{th}$-0.6V) which will be affected by the thickness of the Si cap.

A large set of stress experiments was performed on SiGe p-FETs changing only one of the gate-stack parameters under investigation at the time, while fixing the other two. For comparison purposes, a second set of standard Si channel devices with identical dimensions and gate stack were considered. It is worth noting that, although having the same gate stack, Si channel devices show a lower T_{inv} as compared to the SiGe channel devices due to the absence of any additional displacement for holes (i.e. the Si cap acting as a barrier in SiGe devices). The T_{inv} for the Si channel reference devices was estimated as 1.32nm.

From NBTI stress experiments the following observations were made:

1) Ge content: As is shown in Fig. 3, the introduction of Ge in the channel dramatically improved the NBTI reliability. The extrapolated operating overdrive voltage for a 10 year lifetime (V_{op}), assuming a 30mV threshold voltage shift criterion, increased from 0.46V for the pure Si reference up to 0.8V for 45% Ge content device with a SiGe layer thickness of 7nm and a Si cap thickness of 2nm. Increasing the Ge concentration up to 55%, while keeping constant the other parameters, boosted the operating overdrive voltage even more, reaching 0.9V.

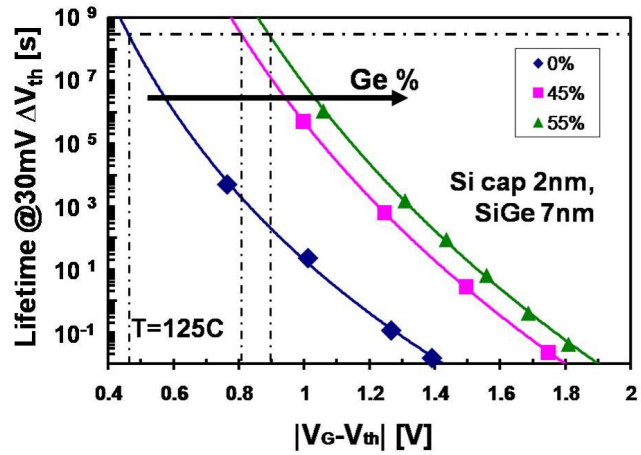

Figure 3. Higher Ge content improves extrapolated operating overdrive voltage for 10 year lifetime. (triangles: rescaled from 5nm SiGe layer).

2) SiGe QW thickness: Increasing the thickness of the SiGe QW had also a positive impact on the NBTI reliability (Fig. 4): V_{op} increased from 0.85V up to 1.01V when moving from a 3nm-thick SiGe layer to a 7nm one. This observation was made while fixing the Si cap thickness to 2nm on 55% Ge channel concentration devices.

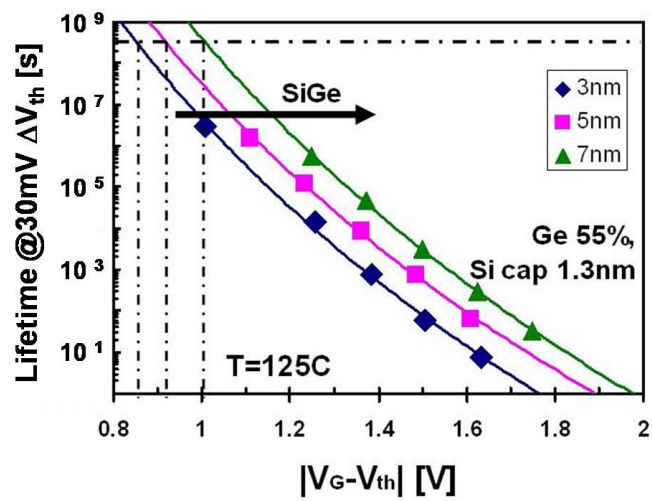

Figure 4. A thicker SiGe channel, i.e. a thicker QW for holes, improves the NBTI reliability.

3) Si cap thickness: The Si cap had also a significant impact on the NBTI reliability (Fig. 5). A thicker Si cap clearly degraded the NBTI performance. V_{op} increased from 0.82V to

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1.14V while the Si cap thickness decreased from 2nm to 0.65nm. The thickness of the Si cap impacts, as already mentioned, the C_{ox} value in inversion and therefore the T_{inv}; hence a fixed overdrive stress voltage leads to different electric fields (E_{ox}) for devices with different Si cap. Since this may affect the interpretation of NBTI data, in order to have a more fair comparison, the effective degradation ($\Delta N_{eff}=\Delta V_{th}*C_{ox}/q$) is plotted as function of E_{ox} and compared for different Si cap thickness (Fig. 6). E_{ox} extraction is not trivial for such complex structures. Here we used the following method: a Q-V curve was obtained by integrating the measured C-V trace; a line was fitted to the almost linear part of the Q-V curve; the slope of the line represented the estimated C_{ox}; the capacitance equivalent thickness (CET) was calculated from C_{ox}; finally E_{ox} was calculated as $|V_G-V_{th}|$/CET. As one can see from Fig. 6, the impact of the Si cap thickness on NBTI degradation is still clear when correcting for the differences in E_{ox}.

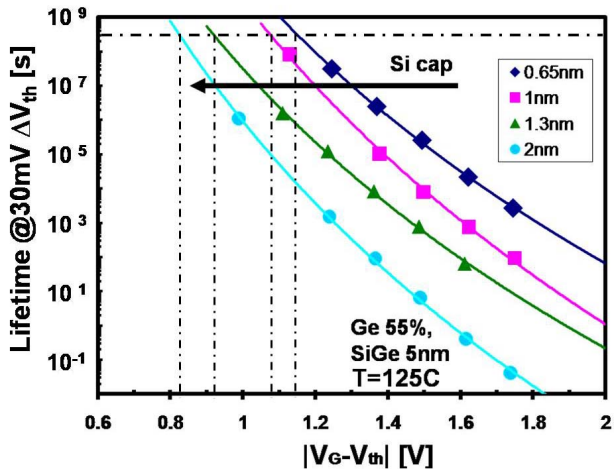

Figure 5. A thicker Si cap reduces NBTI reliability. On the contrary, the use of a thin Si cap improves NBTI reliability while enabling T_{inv} reduction.

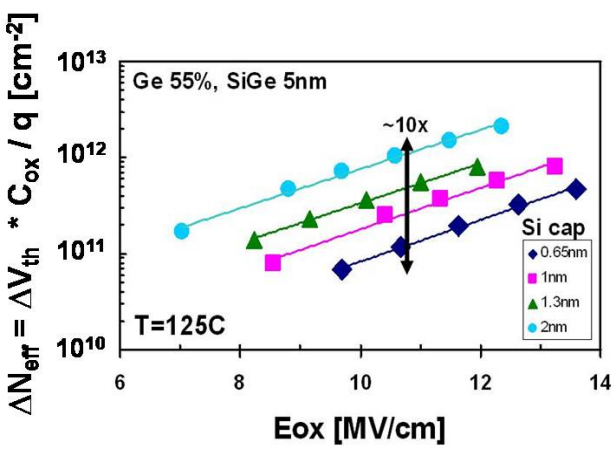

Figure 6. Comparison of degradation as a function of E_{ox} confirms NBTI dependence on Si cap thickness is not an artifact due to different T_{inv}.

B. Discussion

Previous work attributed improvement of NBTI to induced strain at the interface [10]. This explanation does not apply to our devices. The SiGe layer thicknesses considered here were well below the reported critical relaxation thickness for the used epitaxial process, causing the channel to be compressively strained [7]. Avoiding relaxation of the SiGe results in a Si cap that is lattice-matched to the underlying Si substrate. Therefore we conclude that strain effects at the Si/SiO_2 interface were not involved here.

As shown in the band diagram of Fig. 2b, channel holes are confined in the SiGe QW due to the valence band offset (ΔE_v) between SiGe and Si. Fig. 7 shows ΔE_v as a function of the Ge concentration as calculated using MEDICI [11]. The higher offset caused by a higher Ge fraction in the channel reduces the hole tunneling probability through the Si cap layer acting as a potential barrier for holes. This can explain the observed NBTI reduction when increasing the Ge content (Fig. 3).

A similar explanation can justify also the observed NBTI trend when changing the SiGe layer thickness (Fig. 4): for a very thin QW, i.e. 3nm, quantum mechanical effects increase the hole energy, and therefore artificially reduce the ΔE_v [12]. This can lead to degraded NBTI performance due to an enhanced hole tunneling probability.

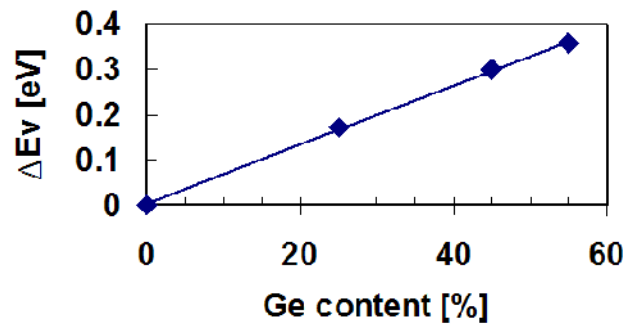

Figure 7. While increasing the Ge content, the SiGe bandgap is reduced and therefore the valence band offset between SiGe and Si increases.

This explanation, however, does not apply to our third experimental observation: a thicker Si cap, i.e. a thicker barrier for holes (Fig. 2), is expected to reduce the tunneling probability [13]. In contrast to this, a thicker Si cap degrades the NBTI reliability, which, on the other hand, is strongly improved when using a thin Si cap (Fig. 5).

Interestingly, the use of a thin Si cap for the passivation of similar structures has been reported to be detrimental for the initial interface quality as compared with thicker Si cap [14]. Charge pumping measurements on our SiGe pFETs confirmed that the Si cap thickness has a considerable impact on the initial interface quality: the use of a 0.65nm Si cap increases the initial N_{it} values by almost two orders of magnitude (Fig. 8) as compared to the 2nm thick Si cap. Therefore NBTI experimental data suggest an anti-correlation between initial N_{it} and NBTI reliability for SiGe devices: a better initial interface quality (i.e., thicker Si cap) leads to degraded NBTI performance. A possible explanation for this trend is that a higher initial N_{it} value, i.e. an already partially degraded interface, could slow down the extra defect creation during NBTI stress [15]. This could explain why devices with thinner Si cap, showing a bad initial interface quality, suffer less NBTI.

The impact of the Si cap thickness on the NBTI reliability is of particular interest because it provides an additional benefit to the advantages of T_{inv} scaling. As one can notice in Fig. 1, a thinner Si cap improves NBTI reliability while reducing T_{inv} due to reduced hole displacement.

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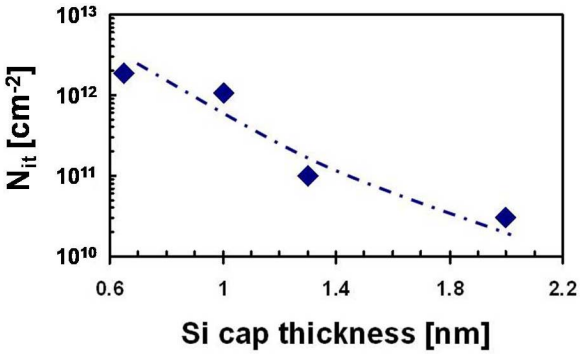

Figure 8. Charge pumping measurements show degraded interface quality for thinner Si cap.

IV. Conclusions

The NBTI reliability of buried SiGe channel p-FETs was investigated as a function of Ge concentration, SiGe layer thickness and Si cap thickness. Measurements showed that the NBTI reliability can be dramatically improved by increasing the Ge content, increasing the SiGe QW thickness and decreasing the Si cap thickness. By means of optimizing the three gate-stack parameters under investigation, SiGe devices can yield excellent NBTI reliability with respect to their Si counterparts. Buried channel SiGe devices therefore are extremely promising for helping to solve the NBTI issue in sub-1nm EOT pFETs.

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