

Mechanisms Limiting EOT Scaling and Gate Leakage Currents of High-k/Metal Gate Stacks Directly on SiGe and a Method to Enable sub-1nm EOT

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Abstract

For the first time, we provide mechanistic understanding of high gate leakage current on surface channel SiGe pFET with high-k/metal gate to enable sub 1nm EOT. The primary mechanism limiting EOT scaling is Ge enhanced Si oxidation resulting in a thick (1.4nm) SiO_x interface layer. A secondary mechanism, Ge doping (≥4%) in high-k, possibly by up diffusion, also results in higher leakage. With this understanding, we optimized high-k nitridation reducing O and Ge diffusion to achieve EOT=0.91nm directly on SiGe with leakage equivalent to bulk Si. High I_{on} (1.5× Si), and low subthreshold slope (73mV/dec) are also achieved. This mechanism enables high mobility channel gate dielectric development directly on SiGe without the need for Si cap, simplifying processing and device design.

Introduction

Selective, epitaxial strained SiGe (<40% Ge) is an attractive channel material beyond Si due to its high carrier mobility (~2× Si) and compatibility to the conventional CMOS processes [1]. Besides high mobility, the SiGe valence band offset to Si simplifies achievement of a low pFET threshold voltage (V_t) with high-k/metal gate [2]. However, the SiGe/dielectric interface has several issues: 1) Ge up-diffusion resulting in degradation of device performance [3], 2) interface states [3], 3) Ge condensation [4] and 4) excessive interface oxidation [5]. Consequently, many researchers fabricated SiGe devices with Si cap and low temperature process [6,7]. However, no reports clarify the material and device mechanisms associated with the SiGe/high-k interface for a true surface channel pFET. A known issue with SiGe channel is high gate leakage current (J_g) [2] that makes HfSiON physical thickness scaling unlikely to achieve sub 1 nm EOT. In this work, we explore metal/HfSiON gate stacks on SiGe channel with and without a Si cap including 950°C S/D anneal. Nitrogen dose and placement in HfSiON is proposed to solve the J_g issues. Particular attention is paid to leakage mechanisms such as 1) Ge up-diffusion and 2) accelerated low-k SiO_x bottom interfacial layer (BIL) growth. Sub 1nm EOT surface channel SiGe pFET performance is evaluated and compared to surface channel Si pFETs.

Experiment

After surface clean, selective, epitaxial SiGe was grown. The gate dielectric was grown with atomic layer deposition and nitrided with thermal or plasma nitridation (N*) to form the following stacks: Top nitrided (TN) HfSiON, intensive top nitrided (TN*) HfSiON and Cyclic nitrided (Cyc-N*) HfSiON. Cyc-N* HfSiON consists of multiple HfSiO depositions followed by nitridation. Subsequent processing included a conventional gate first metal gate (MG) process with a 950°C source/drain anneal.

Results

For SiGe pFET gate stacks, EOT does not scale with increasing J_g for physically thin (~2nm) HfSiON [Fig.1(a)]. Compared with MG/TN-HfSiON/Si stacks, MG/TN-HfSiON/SiGe stacks have higher J_g (>10x) [Fig.1(b)]. Consequently, high-k physical thickness scaling is unlikely to scale HfSiON EOT on SiGe. Increasing the Si cap thickness causes the Si/SiGe to mimic the bulk Si channel and hence

improves the J_g-EOT trend, indicating that interfacial Ge is critical [Fig.1(c)].

HfGeO was intentionally deposited on Si with PVD to simulate Ge up diffusion into the high-k as a possible leakage mechanism. HfGeO (4-15% Ge) increases both J_g and EOT suggesting Hf germanate is undesirable (Fig.2). However, the band gap of Hf germanate is similar to that of HfO₂, suggesting that band gap (barrier height) reduction is unlikely the cause of poor dielectric performance (Fig.3). To understand Hf germanate formation, XPS was done [Fig. 4(a),(b)]. Shifts in Hf4f and O1s chemical states correlate with Hf germanate formation and a similar shift is observed for the HfO₂/SiGe stack, suggesting interfacial germanate does form in the absence of Si cap. Most important, nitridation suppresses these germanate features [Fig.4(c),(d)] suggesting that Ge up diffusion is one key mechanism.

A second key mechanism is Ge catalyzed BIL growth. TEM proves that Ge enhances BIL growth but nitridation reduces BIL thickness (Fig.5). EOT reduction and thin BIL was achieved with plasma N* forming HfSiON (Fig.6). Large EOT reduction (0.4nm) with small J_g increase (<10x) suggests that reduction of low-k BIL is the main factor for EOT scaling (Fig.6). EELS suggests that the BIL is SiO_x but just a small amount of Ge (~3%) up diffuses [Fig.7(a)]. Therefore N content and location is key to achieve thin BIL [Fig.7(b)]. If nitridation is insufficient, O may diffuse down to the SiGe to form SiO_x and Ge segregates below the BIL - the well-known Ge condensation phenomena [4]. Plasma nitridation (TN* and cyc-N*) slows O diffusion and can also locate N close to both SiGe and MG [8]. The Ge up-diffusion and BIL growth was efficiently suppressed and hence can realize EOT=0.91nm and low J_g (Fig.6,8).

Minimal C-V hysteresis (<10mV) and frequency dispersion was observed on HfSiON/SiGe stacks. However, SiGe Nit (charge pumping) is 10x greater than Si channel (6×10¹¹ cm⁻² vs. 5×10¹⁰ cm⁻²) [Fig.9]. Additionally, the Nit of SiGe devices may be under-estimated because the quantum well of SiGe/Si could confine carriers. This high Nit can degrade the mobility. Fortunately, the intrinsic hole mobility of SiGe is high enough to compensate mobility degradation (Fig.10). However, the quantum well of Si/SiGe will increase T_{inv} suggesting formation of a buried channel (Fig.11). Although performance of SiGe pFETs is not as good as Si/SiGe (buried channel) pFETs, SiGe pFETs do not have the issues of high off-state current. Surface channel SiGe pFETs with 0.91nm EOT (TN* HfSiON) can have 1.5x I_{on} improvement vs. surface channel Si pFETs [Fig.12(a)]. The sub-threshold swing (73mV/dec) is small and hence results in low off-state leakage current [Fig.12(b)]. |V_t| is reduced 0.3V making low V_t pFETs more straightforward (Fig.12b) [2].

Conclusion

The mechanisms of high gate leakage current in MG/HfSiON/SiGe stacks are 1) Ge enhanced Si oxidation and 2) Ge up-diffusion, the first being the primary mechanism. Optimized plasma nitridation of HfSiON/SiGe stacks addresses O and Ge diffusion issues enabling EOT=0.91nm. Dielectric deposition directly on SiGe reduces process and device design complexity associated with the common Si cap approach. This scaling and performance demonstration paves the way for surface channel SiGe pFETs at sub 32nm nodes.

References

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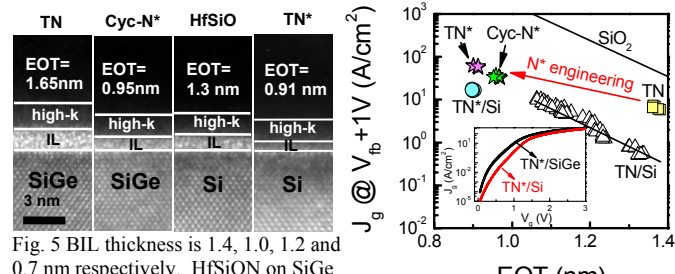
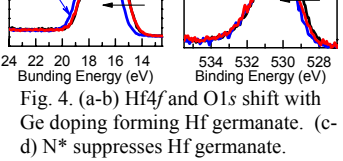
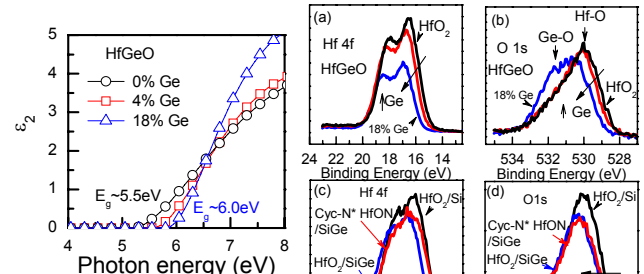
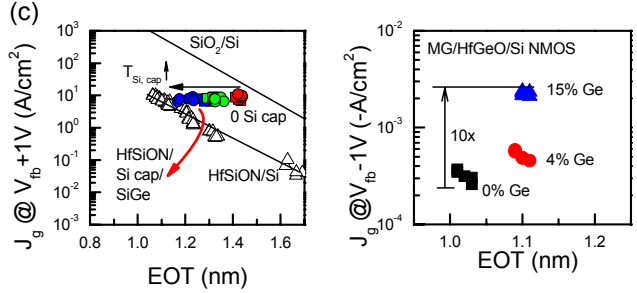
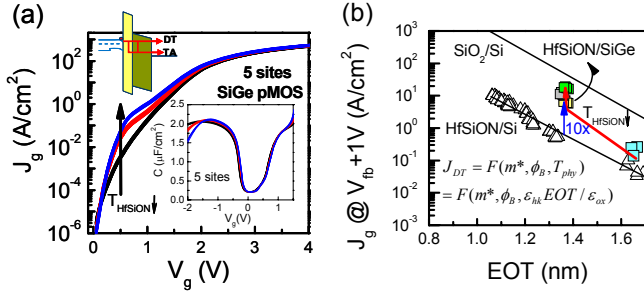


Fig. 6 Large EOT reduction (0.4nm) with small J_g increase (< 10x) suggests that low k material (BIL) is the main factor of EOT scaling instead of Hf germanate (Ge up diffusion).

