

Additive Mobility Enhancement and Off-State Current Reduction in SiGe Channel pMOSFETs with Optimized Si Cap and High-k Metal Gate Stacks

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Abstract

We have demonstrated high mobility pMOSFETs on high quality epitaxial SiGe films selectively grown on Si (100) substrates. With a Si cap processed on SiGe channels, HfSiO₂ high-k gate dielectrics exhibited low C-V hysteresis (<10 mV), interface trap density (7.5×10^{10}), and gate leakage current ($\sim 10^{-2}$ A/cm² at an EOT of 13.4 Å), which are comparable to gate stack on Si channels. The mobility enhancement afforded intrinsically by the SiGe channel (60%) is further increased by a Si cap (40%) process, resulting in a combined ~100% enhancement over Si channels. The Si cap process also mitigates the low potential barrier issues of SiGe channels, which are major causes of the high off-state current of small bandgap energy SiGe pMOSFETs, by improving gate control over the channel.

Device Fabrication

Epitaxial SiGe (Ge=25%) channels and Si caps were selectively grown on shallow trench isolation formed Si (100) substrates. The Si cap thicknesses were varied (0~7nm). HfSiO₂ gate dielectrics were deposited by atomic layer deposition on SiGe channels after surface passivation, followed by sputtering of the metal gates.

Results and Discussion

Fig.1(a) shows TEMs of a 3nm Si cap deposited on a SiGe channel with a high-k HfSiO₂ dielectric/metal gate stack. After a high temperature spike anneal on the S/D, a Si cap layer on the SiGe channel is hardly distinguishable in Fig.1(b). EELS analysis in Fig.2, however, clearly detected the Si-rich layer at the interface. Subsequent electrical data also confirmed a Si cap layer and its impact on SiGe pMOSFETs. Fig.3 compares C-V curves of varying Si cap thicknesses (0~7nm). The C-V hysteresis at 100KHz was minimal (measured to be <10 mV). With a HfSiO₂ physical thickness of 40 Å, the EOT was reduced from 14.1 Å to 13.4~13.5 Å after Si cap processing (Fig.4). EOT is further scaled down by thinning the HfSiO₂ gate dielectrics. Diffusion of Ge from the SiGe channel into the high-k dielectric was effectively suppressed by the Si cap, which lessened the formation of low-k interfacial oxide. A slightly lower EOT was obtained on thinner Si caps. Interface trap density (D_{it}) was measured using the charge pumping technique on SiGe pMOSFETs (Fig.5). Si cap processing significantly reduced the D_{it} from 1.1×10^{12} to 7.5×10^{10} , which is comparable to 5.5×10^{10} for a Si channel. Fig.6 shows threshold voltage (V_{th}) dependency on Si cap for the SiGe channel. A 3nm Si cap shows a lower V_{th} than 5 or 7nm Si caps, when compared with the V_{th} of the Si channel. The SiGe

channel without a Si cap shows the lowest V_{th} . Low V_{th} is attributed to the small bandgap energy of the SiGe channel (or valence band offset relative to the Si cap), which requires small surface potential for channel inversion. This behavior is in good agreement with the positive V_{th} reported on other Ge pMOSFETs [1-2]. C-V curves of SiGe MOSFETs in Fig.7 support varying V_{th} as a function of Ge content. Note flatband voltages are, however, relatively independent of Ge content. The high C-V stretch-out observed without the Si cap is due to high interface charge density. The slightly high EOT of the Si cap on SiGe channel (compared to Si channel) might be due to carrier confinement in the SiGe channel with the Si cap acting as an insulator. However, multi- V_{th} s, which are typically observed with Si cap on SiGe channel at a high surface field, are not observed in the C-V curves. Fig.8 compares the I_d - V_g curves of SiGe and Si channel pMOSFETs. High drain current is obtained in optimized Si caps on the SiGe channel when carriers transport on the SiGe channel and the Si cap serves as a passivation layer. Drain current is compromised when the Si cap becomes too thick for carriers to be transported through it. The off-state current of the SiGe channel is intrinsically higher than the Si channel because of a high subthreshold and substrate current, which are degraded by the low built-in potential of source-to-channel and S/D junctions (Fig.9). Si cap processing mitigates off-state current and short channel effects by improving the gate dielectric-channel interface quality and, therefore, providing better gate control over the channel. Fig.10 shows I_d - V_g for SiGe short channels. Fig.11 shows ~100% enhanced drive current for SiGe pMOSFETs with an optimized Si cap. Mobility enhancement was confirmed in the transconductance and mobility results in Fig.12. SiGe channels without a Si cap exhibited ~60% mobility enhancement over the Si channels. After applying the Si cap process, SiGe channel mobility was further enhanced by ~40%. Therefore, a ~100% mobility enhancement was achieved by the combined SiGe channel and Si cap processing.

Conclusions

Optimized Si caps reduced interface trap density from 1.1×10^{12} to 7.5×10^{10} and showed minimal C-V hysteresis (< 10 mV). Si cap processing effectively suppressed the off-state current of SiGe pMOSFETs by providing better gate control over the channel, while enhancing hole mobility by 40% in the SiGe channel, which resulted in a ~100% mobility enhancement over Si channels after combining the SiGe channel and Si cap processing. Results obtained in this study advance the optimization of high mobility SiGe as an alternative channel material for future technology nodes.

References

- [1] P.Zimmerman et al., IEDM, p.655, 2006.
- [2] O.Weber et al., IEDM, p.143, 2005.

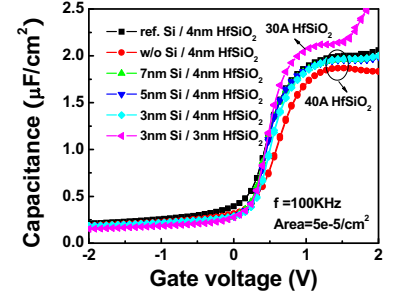
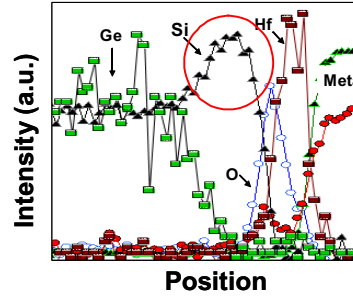
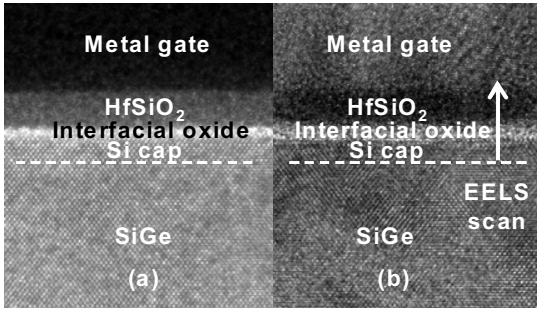


Fig.1 HR-XTEM of gate stack with Si cap, high-k HfSiO₂, and metal gates on epitaxial SiGe (Ge=25%) layers selectively grown on Si (100) substrates. (a) Before and (b) after high temperature spike anneal for source/drain activation.

Fig.2 EELS analysis on the gate stack in direction shown in Fig.1(b) shows the Si-rich layer at the interface.

Fig.3 C-V of SiGe MOS capacitors showing scalable low EOT and minimal hysteresis (<10 mV) of 40Å HfSiO₂ on SiGe channels.

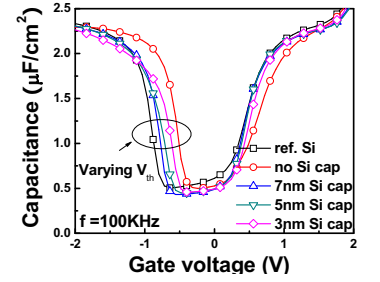
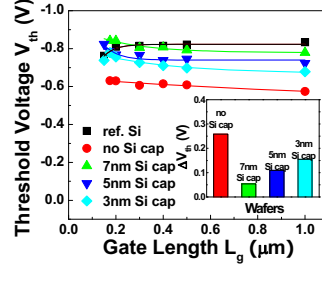
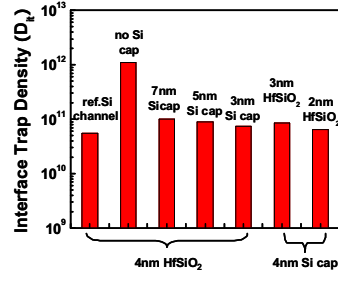
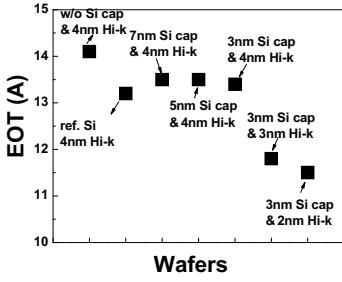


Fig.4 Scalable EOT on SiGe channels with varying Si cap and high-k dielectrics. EOT for Si cap is lower than without Si cap.

Fig. 5 Significant reduction in D_{it} from 1.1×10^{12} to 7.5×10^{10} after Si cap processing, providing better gate control over the SiGe channels.

Fig.6 V_{th} dependency on Si cap for the SiGe channel. Low V_{th} is attributed to the small bandgap energy of the SiGe channel.

Fig. 7 Varying V_{th} and relatively independent V_{th} of Ge content. Slight C-V stretch-out without the Si cap due to high interface charge density.

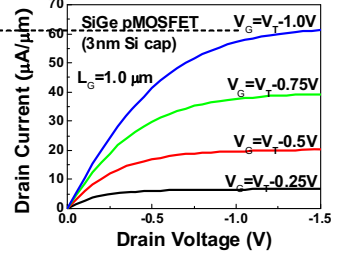
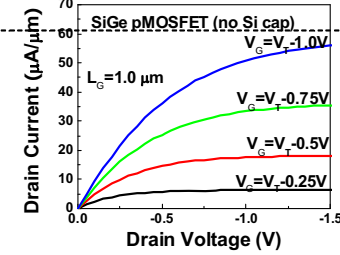
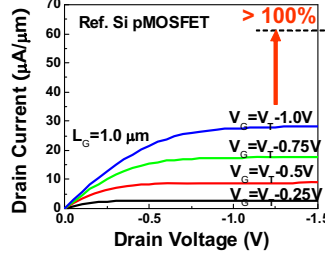
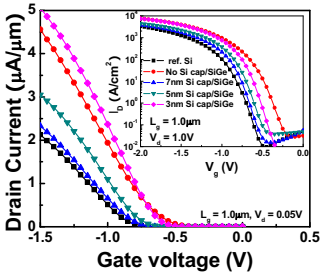


Fig.8 I_d-V_g of SiGe and Si channels. High drain current occurs in optimized Si caps when holes transport on SiGe channel and Si cap serves as a passivation layer.

Fig.11 Drive current enhancement afforded intrinsically by the SiGe channel is further increased by an optimized Si cap, resulting in a combined >100% enhancement over Si channels compared to reference Si channel at normalized gate voltages.

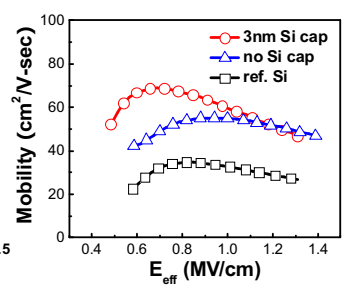
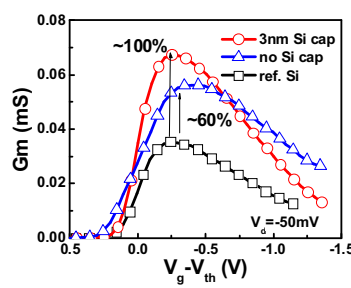
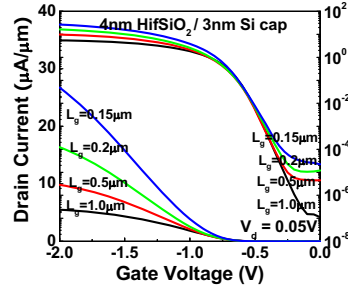
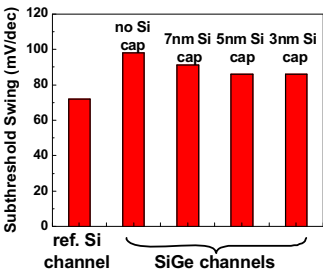


Fig.9 Intrinsically higher S.S. for SiGe than Si channels because of low built-in potential of source-to-channel and S/D junctions.

Fig.10 Si cap processing lessens short channel effects by improving interface quality and, therefore, providing better gate control over the channel.

Fig.12 SiGe channels without a Si cap exhibited ~60% mobility enhancement over the Si channels. After applying the Si cap process, SiGe channel mobility is further enhanced by ~40%. Therefore, a ~100% mobility enhancement was achieved by the combined SiGe channel and Si cap processing.