

Opportunities and Challenges for Germanium and Silicon-Germanium Channel p-FETs.

To cite this article: Stephen W. Bedell *et al* 2009 *Meet. Abstr.* **MA2009-01** 714

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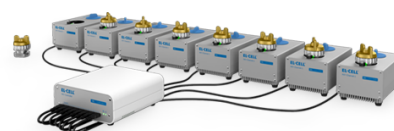
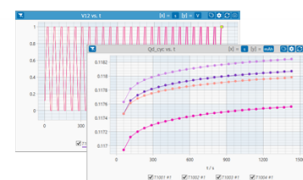
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Opportunities and Challenges for Germanium and Silicon-Germanium Channel p-FETs

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In an attempt to extend FET performance through mobility scaling, high content SiGe and pure Ge channels have been proposed [1,2] as viable alternatives to Si. Most of the work in this area has focused on carrier transport in large devices with non-scaled gate stacks. In this work, we summarize the results of Ge and high-Ge content SiGe channel p-FETs fabricated on lattice-engineered SGOI substrates with scaled high- κ gate dielectrics and metal gate electrodes. This work will present the advantages of SiGe and Ge channels, such as better dielectric thickness scaling, carrier transport and threshold voltage V_T control, as well as some of the disadvantages such as higher off-state leakage I_{OFF} .

Figure 1 shows the drain current I_D versus gate voltage V_G for a Si channel (SOI), a $\text{Si}_{0.5}\text{Ge}_{0.5}$ channel grown on SiGe-on-insulator (SGOI), and a strained Ge channel grown on SGOI. The gate dielectric material was HfO_2 for all devices and the gate metal was TaN for the Si and SiGe channel devices and TiN for the Ge channel device. The linear V_T of these devices range from -780 mV for the SOI device to +420 mV for the strained Ge device. This ability to control the threshold voltage V_T of the devices by engineering the Ge composition and strain is one of the promising opportunities enabled by channel engineering. Also, mobility and drive current increase with increasing Ge content; with pure Ge being the highest even at deep submicron channel lengths [3,4]. The biggest challenge which limits the usefulness of high Ge content channel layers is the exponential increase in off-state leakage. In Fig. 1 I_{OFF} is seen to increase by more than 4 orders of magnitude from Si to pure Ge.

Figure 2 shows the gate capacitance C_G versus V_G for the three devices shown in Fig. 1. The higher gate capacitance observed for the SiGe channel device compared to the Si device is due to the overall lower thermal budget required to activate dopants in the SiGe/SGOI structure. This illustrates another subtle advantage afforded by using SiGe-based devices over the Si devices. Namely, there is more flexibility in controlling unwanted regrowth at the channel/high- κ interface. Therefore, SiGe-based devices may help gate dielectric thickness scaling by reducing the overall process temperature.

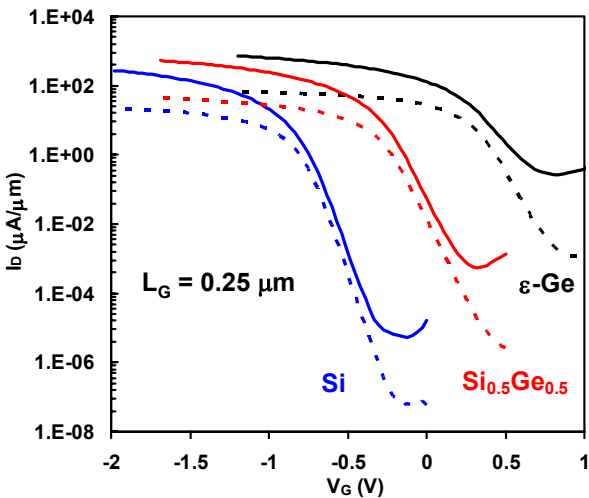


Figure 1. Drain current I_D vs. gate voltage V_G for Si, $\text{Si}_{0.5}\text{Ge}_{0.5}$, and pure Ge channel devices with HfO_2 gate dielectric. The Si data is from a SOI substrate, whereas the Ge-containing channels were grown on SGOI substrates.

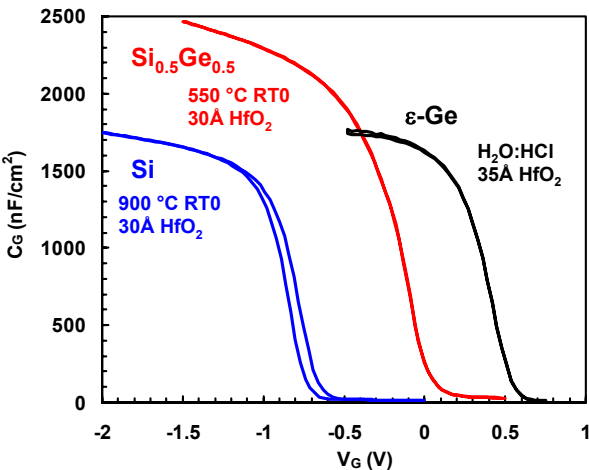


Figure 2. Gate capacitance C_G vs. gate voltage V_G for the same devices shown in Fig. 1. All data shown is taken at 100 kHz with forward and reverse V_G sweep.

References:

- [1] M. L. Lee *et al.*, *J. Appl. Phys.*, **97** (2005) 011101.
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