

High-Mobility 0.85nm-EOT Si_{0.45}Ge_{0.55}-pFETs: Delivering high performance at scaled VDD.

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Abstract

This work demonstrates the successful integration of 0.85nm-EOT Si_{0.45}Ge_{0.55}-pFETs using a gate first approach. An in-depth analysis, ranging from capacitor-level up to circuit-level is carried out, with systematic benchmarking to a conventional Si-channel reference. Outperforming the state-of-the-art Si_{0.55}Ge_{0.45}-pFETs, an I_{ON} of 630μA/μm at L_{G,POLY} = 35nm with I_{OFF} = 100nA/μm and V_{DD} = -1V has been achieved without any epi-S/D boosters. Significant improvements at lower V_{DD} have also been confirmed through complex circuit simulations and validated by experimental results.

Introduction

High-mobility (Si)Ge-pFETs have been demonstrated to be viable candidates for future high-speed applications due to its excellent drive current performance, low threshold voltage values achieved, and integration-friendliness to the silicon substrate [1,2,12]. In [2], Si_{0.55}Ge_{0.45} with a high thermal budget has been demonstrated to provide high-performing SiGe-pFETs at aggressive Equivalent Oxide Thickness (EOT~5Å). However, channel relaxation has recently become a key concern for Ge contents, typically above 45% [3,4]. In this work, the integration of 0.85nm-EOT gate-first SiGe-pFETs up to Ge-55% is demonstrated with improved performance. The applicability of these devices to low operating voltage (V_{DD}), including an in-depth benchmarking to Si from capacitor up to the circuit level, has also been carried out.

Optimization Strategy and First-Level electrical results

Key fabrication steps are summarized in figure 1. To minimize process complexity, one can notice that *only one step* was added to the 300mm-Si baseline flow: the in-situ Si/SiGe growth. A high resolution TEM picture of the Si_{0.45}Ge_{0.55}-pFET can be seen in figure 2, showing smooth channel interface and defect-free Silicon-Germanium layer after full processing. Important optimizations were carried out with respect to the thicknesses of the dual Si-SiGe layers.

Figure 3 highlights the need of a thin silicon layer to better passivate the high-mobility channel and the importance of the SiGe layer thickness control with respect to the junction leakage reduction. The optimization of these two physical parameters is crucial to obtain high-performing Si_{0.45}Ge_{0.55}-pFETs. Despite the introduction of the Si cap layer, low EOT values, down to 0.85nm, are successfully demonstrated (figure 4), while the interfacial defect state density (D_{IT}) is maintained at a reasonably low level (only ~2X of the Si reference). Regarding the transport, 50%-higher low-field mobility is demonstrated in figure 5 (below) for Si_{0.45}Ge_{0.55}-pFETs over the Si control.

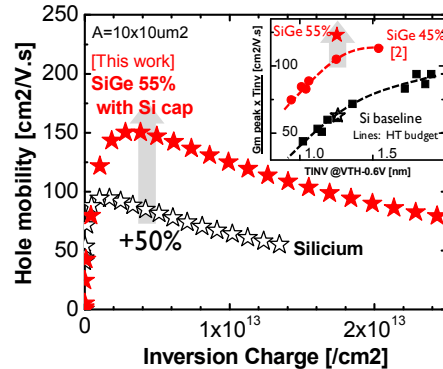


Fig. 5: Split-CV mobility curves showing a 50% mobility boost at EOT~0.85nm. In inset, benchmarking data [peak Gm mobility]. SiGe-55% pFETs outperform other Si-(Ge)-based transistors (with no epi-S/D boosters).

Low-temperature split-CV mobility shown in Fig. 6 confirms the aforementioned gain at both low and high vertical field. The beneficial impact from the silicon cap layer is in better screening of the oxide defects from the channel and reducing the effective surface roughness. Finally, high-field transport is addressed. Conventional DC I_{DRAIN}-V_{DRAIN} and I_{DRAIN}-V_{GATE} characteristics with excellent performance are reported in figures 7 and 8. I_{ON}/I_{OFF} characteristic for Si_{0.45}Ge_{0.55}-pFETs depicts a drive current of ~630μA/μm at I_{OFF,HP_TARGET} = 100nA/μm and V_{DD} = -1V, significantly outperforming the Si reference at same EOT, and other Si counterparts with no e-S/D boosters (Fig. 9). Compared to the state-of-the-art Si_{0.55}Ge_{0.45} recently

published [2], a higher performance (+ ~5%) is obtained, at reduced gate leakage (x1/3) [EOT effect mainly]. Other information about electrical parameters can be also found in the summary table (figure 10).

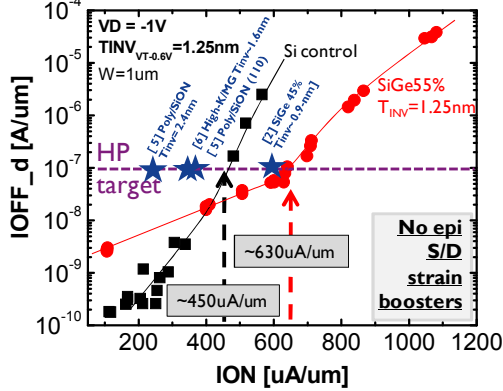


Fig. 9: I_{ON}/I_{OFF} plot at $V_{DD} = -1V$. Performance benchmarking with unstrained Si-pFETs (no SiGe-S/D) is done. Higher performance is reported compared to our previous SiGe-45% work.

Si_{0.45}Ge_{0.55}-pFETs for low-power logic applications

The impact of reduced drain voltage is also investigated on Si_{0.45}Ge_{0.55}-pFET performance with respect to regular Si devices. A relevant methodology is introduced in figure 11, aiming at the compensation of the threshold voltage difference between Si and Si_{0.45}Ge_{0.55} samples. By adjusting only the work function of each system and by comparing two relevant devices (with similar electrostatic control i.e. DIBL), an 80% drive current gain is demonstrated at very low drain voltage (-20mV in Fig. 12) compared to ~40% at $V_D = -1V$ (Fig. 10). Following the same methodology, the drive current gain at intermediate values is extracted to show a quasi linear dependency with respect to drain voltage (Fig. 13). Further improvements are demonstrated when V_D and V_{DD} are reduced together. This performance boost can be mainly explained by a gain in source velocity (Fig. 14) as predicted theoretically [7]. Finally, lowering the V_D is not only beneficial in drive current gain but also in the off-state regime by significantly reducing the junction leakage component (Fig. 15). This behavior could enable a low power option also for Si_{0.45}Ge_{0.55} - pFETs.

Boosting circuit performance with SiGe-based technology

A SiGe-based system-level performance assessment is carried out using the methodology described in figure 16. Based on a significant electrical data collection, three different circuit components are subsequently emulated with the new Si_{0.45}Ge_{0.55} technology as compared to the Si control:

(Circuit 1) Transistor stacking is known as an efficient technique to reduce power consumption at the cost of a small speed reduction [8,9]. In figure 17, an increase in the I_{ON} ratio between Si_{0.45}Ge_{0.55} and Si is observed for the

stacked devices and for reduced V_{DD} . Hence, SiGe-based circuits in a stacking mode appear less penalized with respect to Si-only circuits in the field of dynamic voltage scaling (V_{DD} lowering).

(Circuit 2) CMOS inverter delay is experimentally evaluated using the effective current methodology [10,11]. An I_{EFF} gain up to 60% is observed using Si_{0.45}Ge_{0.55}-pFETs over that of Si reference (Fig. 18). Note that the I_{EFF} approximation is validated by circuit simulation (Fig. 19).

(Circuit 3) 8-bit multiplier circuit is finally assessed by using 32nm-design rules and digital standard cell library. Figure 20 shows the simulation result and demonstrates a large performance gain at commercial V_{DD} when employing the Si_{0.45}Ge_{0.55} technology. Finally, Si and SiGe-based simulation results match at both $V_{DD} = -1.1V$ and $-0.6V$. This implies a significant dynamic power reduction of ~70% can be achieved without any loss of performance.

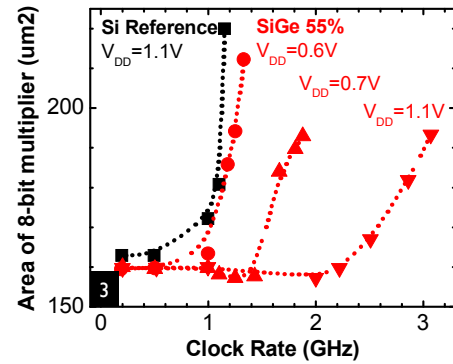


Fig. 20: Area of 8-bit multiplier versus target clock rate for bulk silicon standard cell library with a V_{DD} of 1.1V and SiGe cell libraries characterized with V_{DD} 's of 1.1V, 0.7V and 0.6V.

At a V_{DD} of 0.6V, the clock rate versus area trade-off of the SiGe implementation of the multiplier is the similar to the bulk-silicon implementation at a V_{DD} of 1.1V. This reduction in supply voltage corresponds to a reduction in dynamic power of 70% with no loss of performance.

Conclusions

A 0.85nm-EOT high-mobility Si_{0.45}Ge_{0.55}-pFET has been successfully fabricated on a 300mm-Si platform. A 630 μ A/ μ m I_{ON} at $I_{OFF} = 100$ nA/ μ m and $V_{DD} = -1V$ has been achieved without any epi-S/D boosters. Further improvements at lower operating voltage have been demonstrated through circuit simulations and validated with experimental results. The significant dynamic V_{DD} reduction shown in this work makes high-Ge content pFETs very attractive for power consumption restricted platforms.

Acknowledgements

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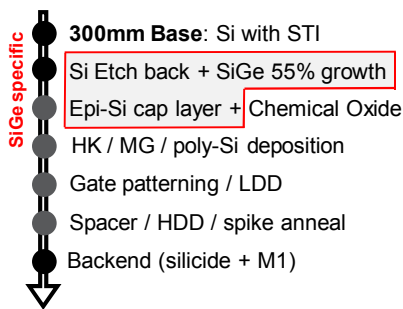


Fig. 1: Process flow schematic. Only one process step has been changed compared to regular Si devices.

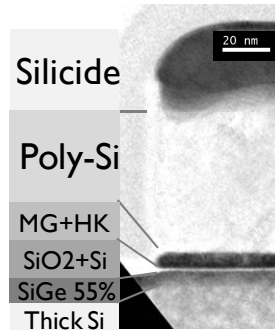


Fig. 2: Process flow schematic. Only one process step has been changed compared to regular Si devices.

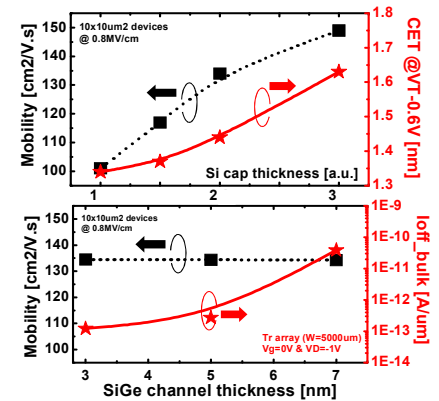


Fig. 3: One example of thickness optimization applied to the SiGe-55% pFETs in order to maximize the performance (Si: mobility / T_{INV} trade-off and SiGe: junction leakage – I_{OFF} reduction)

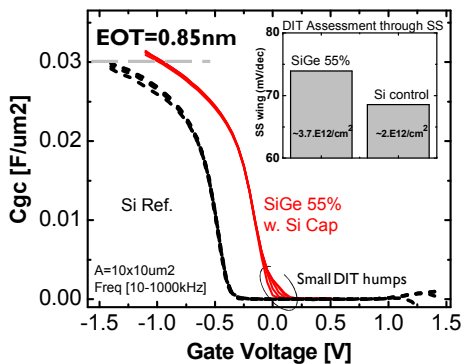


Fig. 4: Inversion capacitance as a function of gate voltage. Sub-nm EOT SiGe-pFETs with relatively low DIT values compared to the Si-control are demonstrated.

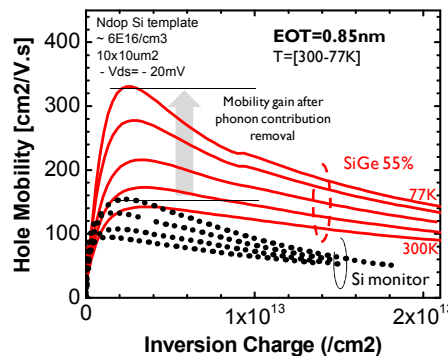


Fig. 6: Split-CV mobility as a function of temperature. After phonon contribution reduction, the SiGe-55% mobility is higher than Si, likely due the beneficial role of the Si cap (screening layer).

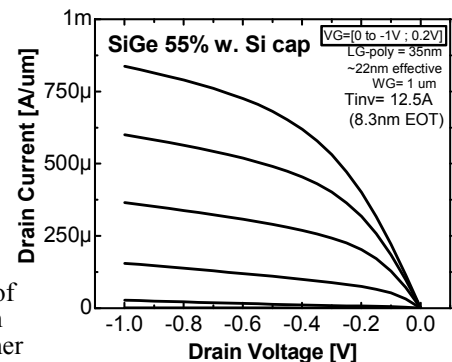


Fig. 7: Transfer characteristics of a SiGe-55% pFET with 0.85nm EOT and $L_G \sim 35$ nm.

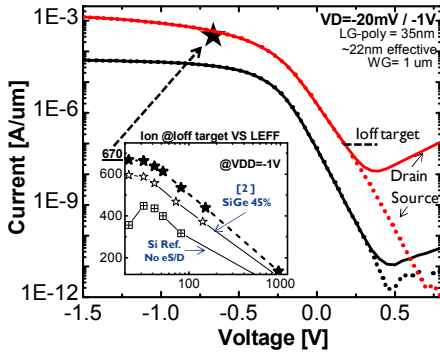


Fig. 8: I_d - V_g curves at two V_D 's for a short channel SiGe-55% pFET. The inset demonstrates higher drive current @ a fixed I_{OFF} HP target.

Fig. 10: Summary table with the main electrical parameters. Comparison with Si at matched T_{INV} and previous work (SiGe-45% [2]).

	Match Si w/AIO cap	SiGe 45% VLSI'10- [2]	Match Si no cap	SiGe 55% [this work]
$T_{inv}[A]$ @VTH-0.6V /EOT[A]	10/6	8.5-9/5.5	12.5/8.9	12.5/8.5
"Gm x T_{inv} " Mobility 1x1 [cm ² /V.s]	43	80	63	123
VT,LIN 1x1 [mV]	-440	-360	-600	-200
Log JG @ -1V 1x1 [A/cm ²]	-1.13	-0.23	-1.7	-0.75
SS 1x1 [mV/dec]	72	73.5	68	73.5
I_{dsat} @VTH,LIN -0.6V [uA/um] @Ioff HP Tgt	590	599	480	667 (+40%)
I_{dsat} @VG=-1V [uA/um] @Ioff HP Tgt	570	604	450	630

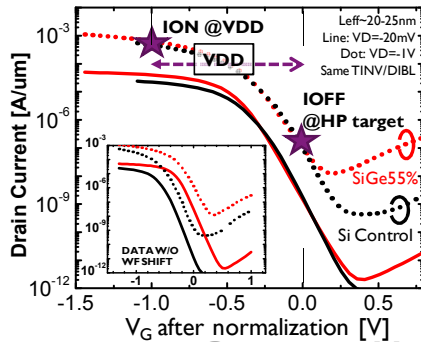


Fig. 11: I_D - V_G curves before (inset) and after Work Function normalization to illustrate the methodology used in the performance benchmarking part.

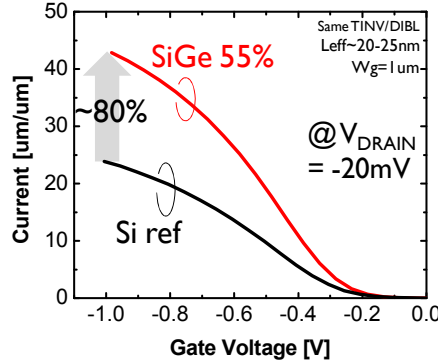


Fig. 12: Illustration, after normalization, of the drive current gain obtained at low V_D .

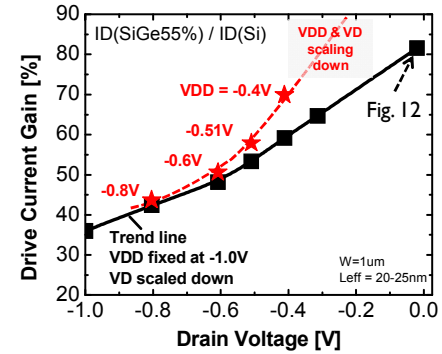


Fig. 13: Drive current gain as a function of V_D . Large gain at lower V_D is confirmed. Further performance improvement can be obtained by scaling down V_D and V_{DD} together.

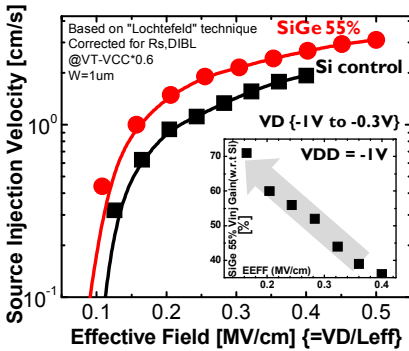


Fig. 14: Source injection velocity (V_{inj}) vs. the lateral field calculated from V_D .

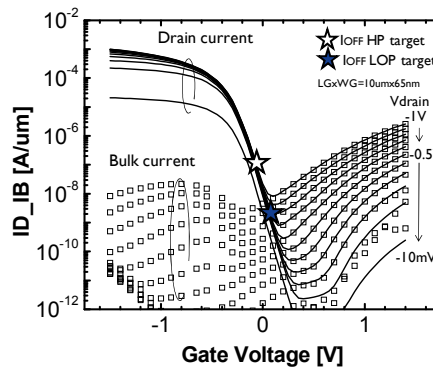


Fig. 15: Drain and Bulk currents VS V_G for Si_{0.45}Ge_{0.55}-pFETs (different V_D). $I_{OFF-LOP}$ target can be reached by lowering V_D (below -0.7V). $I_{eff} = (I_{high} + I_{low})/2$

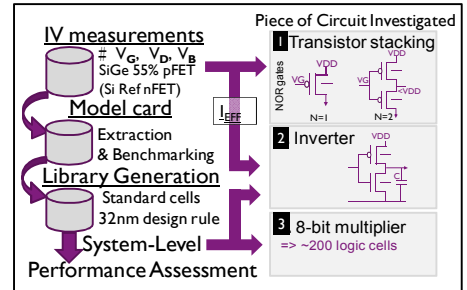


Fig. 16: Block diagram related to our System-Level Performance Assessment. Three different piece of circuit will be compared targeting low V_D applications.

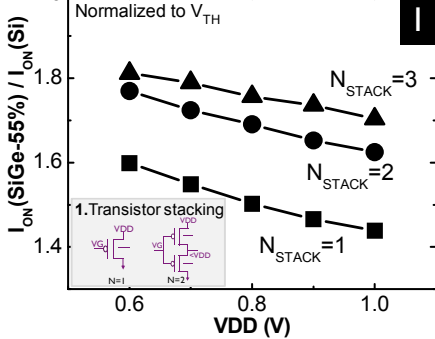


Fig. 17: **Circuit1-** Series of NOR gates applied in leakage current reduction technique [8,9]. By reducing V_{DD} and/or by increasing the number of stacked transistors, the I_{ON} gain is improved.

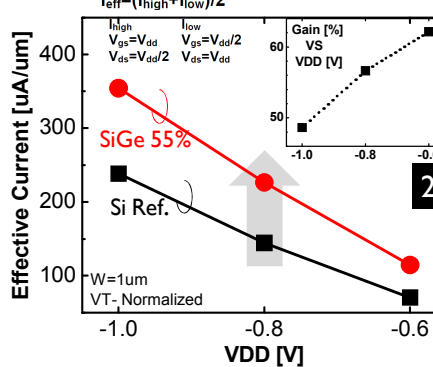


Fig. 18: **Circuit2-** I_{EFF} extraction vs V_{DD} [10]. Higher I_{EFF} (lower Delay) is shown for SiGe-55%. In inset, further boost at low operating voltage is demonstrated.

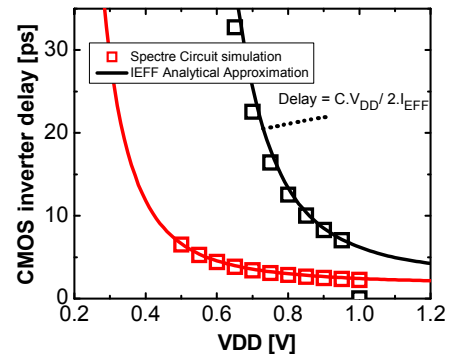


Fig. 19: **Circuit2-** SiGe vs Si CMOS inverters delay based on circuit simulation using the extracted Verilog-A model cards and the analytical approximation $CV_{DD}/2.I_{eff}$.