



Improving bulk FinFET DC performance in comparison to SOI FinFET

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ABSTRACT

The implementation of FinFET structure in bulk silicon wafers is very attractive due to low-cost technology and compatibility with standard bulk CMOS in comparison with silicon-on-insulator (SOI) FinFET. SOI and bulk FinFET were analyzed by a three-dimensional numerical device simulator. We have shown that bulk FinFET with source/drain-to-body (S/D) junctions shallower than gate-bottom has equal or better subthreshold performance than SOI FinFET. By reducing S/D junction depth, fin width scaling for suppression of short-channel-effects (SCEs) can be relaxed. On-state performance has also been examined and drain current difference between the SOI and bulk FinFET at higher body doping levels has been explained by investigating enhanced conduction in silicon-oxide interface corners. By keeping the body doping low and junctions shallower than the gate-bottom, bulk FinFET characteristics can be improved with no increase in process complexity and cost.

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1. Introduction

Semiconductor industry faces rising challenges as CMOS scales down to the 45 nm technology node and beyond. Among the most important challenges are short-channel-effects (SCEs) which are caused by the decreased gate control of the channel. These problems can be overcome by either introducing new materials (e.g. in the gate stack) or by introducing new device architectures. Double-gate MOSFETs have shown excellent down-scaling characteristics and high-performance when compared to the conventional single-gate device structures, due to better gate controllability of the channel. FinFET, a self-aligned double-gate transistor, is the most viable implementation of double-gate MOSFET structure because of its simplicity and compatibility with conventional planar CMOS technology [1]. FinFET is an attractive candidate to either succeed bulk CMOS technology at the end-of-scaling or to be integrated with bulk CMOS in various applications, e.g. NAND flash memories [2]. Although mainly fabricated on silicon-on-insulator (SOI) substrates where they have demonstrated excellent subthreshold characteristics [3,4], bulk or body-tied FinFET has also gained attention mainly due to its ability to be integrated with standard bulk CMOS technology [5,6]. SOI FinFETs have some disadvantages over bulk FinFETs such as high wafer cost, high defect

density, heat transfer problems and may suffer from floating body problem. Also, bulk FinFET shows better immunity to negative-bias-temperature (NBT) stress [7]. Clearly, it is useful and cost-effective to implement FinFET technology on bulk silicon wafer if its characteristics can match those of SOI FinFET devices.

In this paper, the characteristics of bulk FinFET are analyzed by 3D device simulation and compared with SOI FinFET. The goal of such comparison is to find the bulk FinFET structure for a 45 nm technology node with comparable or better characteristics than the SOI counterpart (with identical geometrical dimensions) which would not demand additional complex process steps. Furthermore, the effects specific to bulk FinFET structure and its electrostatic behavior are examined, especially investigating the subthreshold region which is crucial for low standby power (LSP) applications, and the saturation region which is crucial for high-performance (HP) applications [8–10]. The influence of different fin widths, source/drain-to-body (S/D) junction depths, body doping and bias on transistor characteristics is analyzed.

2. Device structure and numerical simulations

Bulk FinFET and SOI FinFET structures are analyzed and compared by using 3D numerical device simulator [11]. Fig. 1a and b show 3D illustrations of both structures, while cross-sectional views are shown in Fig. 1c. We assumed *p*-type body with variable doping, source and drain regions doped with 10^{20} cm^{-3} , abrupt source and drain junctions (with variable junction depths in the case of bulk FinFET), n^+ polysilicon gates doped with 10^{20} cm^{-3} , gate oxide thickness (t_{gox}) of 2 nm and top-gate oxide thickness

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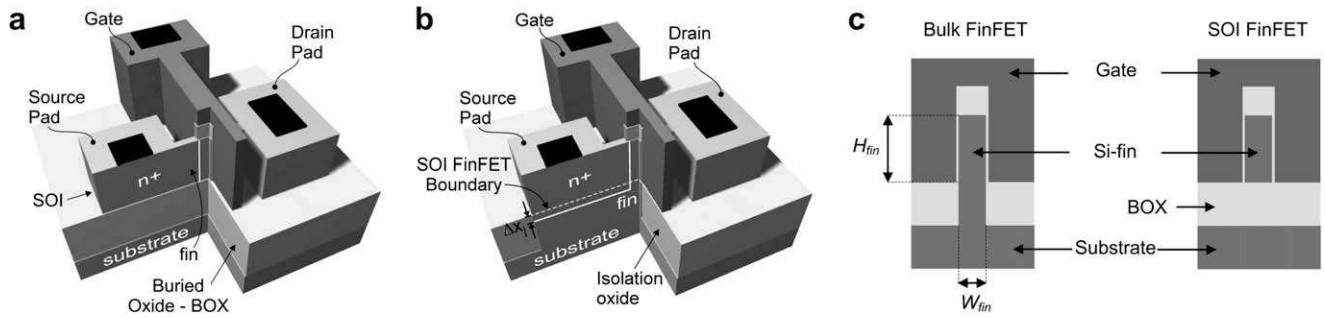


Fig. 1. Bird's eye view of 3D illustration of (a) SOI FinFET and (b) bulk FinFET. Fin to body connection can be seen in (b) which explains the name body-tied or bulk FinFET. Misalignment between gate-bottom and S/D junction depth is designated Δx_j . (c) 2D cross-section along transistor gate of bulk and SOI FinFET structures.

of 35 nm, i.e. devices are effectively double-gated since the influence from the top-gate is effectively nullified. Fin height (H_{fin}) and gate length (L_g) are set to 50 nm with variable fin widths (W_{fin}). With small S/D-to-gate overlap, effective channel length is 45 nm. Bottom oxide (BOX) thickness in the case of SOI FinFET and the isolation oxide thickness in the case of SOI FinFET and the isolation (oxide between the gate polysilicon and the substrate) are set to 50 nm. Concerning bulk FinFETs, misalignment between the bottom of the gate electrode and source/drain-to-body junction depth is designated Δx_j ; if the junction is deeper (shallower) than the bottom of the gate, then $\Delta x_j > 0$ ($\Delta x_j < 0$).

The transport model which is used for simulations is based on the drift-diffusion formalism with trap-assisted and band-to-band tunneling included in the Shockley-Read-Hall recombination. We used concentration-dependent mobility model which includes the effect of impurity scattering, and the mobility model developed by Hewlett-Packard which takes into account dependence on electric fields both parallel and perpendicular to the direction of current flow [12]. Therefore, the classical models are used in the simulation, although the effects of mobility dependence on fin width [13] or carrier energy quantization [14,15] can be expected in the actual structure. However, such analyses are valid for qualitative discussion and relative comparison of the performance of bulk and SOI FinFET structures.

3. Results and discussion

3.1. Fin width and S/D junction depth influence

The influence of gate-bottom to junction depth misalignment was examined in two directions: deeper junctions (when the gate does not control the whole channel) and shallower junctions (when the gate controls the whole channel and a portion of the fin beneath the channel). Simulated transfer characteristics are shown in Fig. 2 for SOI FinFET and bulk FinFET with source/drain junction depths extended underneath the gate by $\Delta x_j = 0$ nm (gate-bottom aligned to the junction depth) and $\Delta x_j = 20$ nm. SOI FinFET has drain-induced barrier lowering (DIBL) of 61.8 mV/V and subthreshold swing of 86.3 mV/dec, whereas bulk FinFET with junctions aligned to the bottom of the gate has DIBL of 67.3 mV/V and S of 95 mV/dec. The higher S and DIBL of bulk FinFET with junction depths corresponding to the bottom of the gate by 10.1% and 8.9%, respectively, can be attributed to higher dielectric constant of depleted silicon compared to SiO_2 , which guides the drain electric field towards the source underneath the gate. The gate-induced drain leakage is responsible for the current increase in accumulation. An increase of the source/drain junction depths by $\Delta x_j = 20$ nm with respect to the bottom of the gate deteriorates bulk FinFET characteristics greatly; having DIBL of 210.9 mV/V and S of 249.5 mV/dec, due to low gate controllability of the bottom of

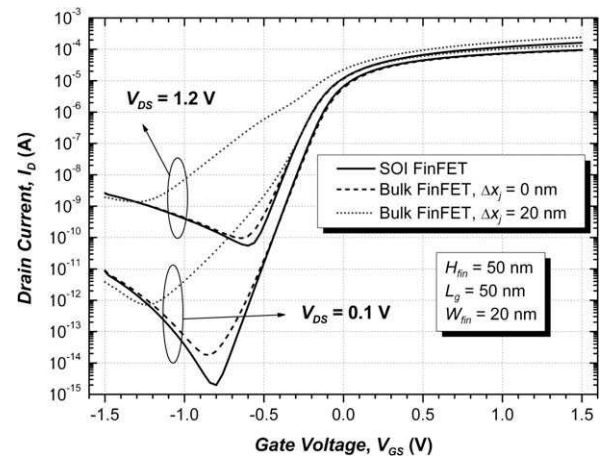


Fig. 2. Transfer characteristics for three examined structures. Subthreshold performance of bulk FinFET with junction depths aligned to gate-bottom ($\Delta x_j = 0$) is close to that of SOI FinFET, whereas deeper junctions increase leakage and deteriorate DIBL and subthreshold swing.

the channel. This can be explained from the 3D and 2D cross-sectional potential contour plot in Fig. 3 where it is clearly seen that the potential barrier between the source and drain in the fin below the bottom of the gate is lower and thinner for bulk FinFET with $\Delta x_j = 20$ nm compared to SOI FinFET and bulk FinFET with $\Delta x_j = 0$ nm, especially at the silicon-oxide interface below the gate. This causes the boost of subthreshold current and, as a consequence, the deterioration of DIBL and subthreshold swing. It can be noted that, from the results in Fig. 3, SOI FinFET and bulk FinFET with $\Delta x_j = 0$ nm have similar potential distribution and, hence, almost identical subthreshold characteristics. The simulated output characteristics for the three examined structures are shown in Fig. 4. The output characteristics are closely spaced with bulk FinFET output resistance decreasing as junction depth is increasing, due to DIBL effect. The bulk FinFET has good performance in saturation regardless of source/drain junction depth. The on-state currents, at $V_{GS} = V_{DS} = 1.2$ V, are around 140 μA , for the fin height of 50 nm. On-state current per channel width in this case is a little under 1.4 mA/ μm (depending on fin width since the channel width is $W = 2 H_{fin} + W_{fin}$), which is still far above the requirements for LSP applications stated in ITRS [9]. All these results show the importance of process variation control when the alignment between the gate-bottom and junction depth is concerned.

The idea of making the S/D-to-body junctions shallower so that the polysilicon gate electrode controls the whole channel and part of the fin under the active area comes from the Π -gate FinFET structures. Π -gate FinFETs are only fabricated in SOI wafers and they owe their name to the shape of the gate which resembles

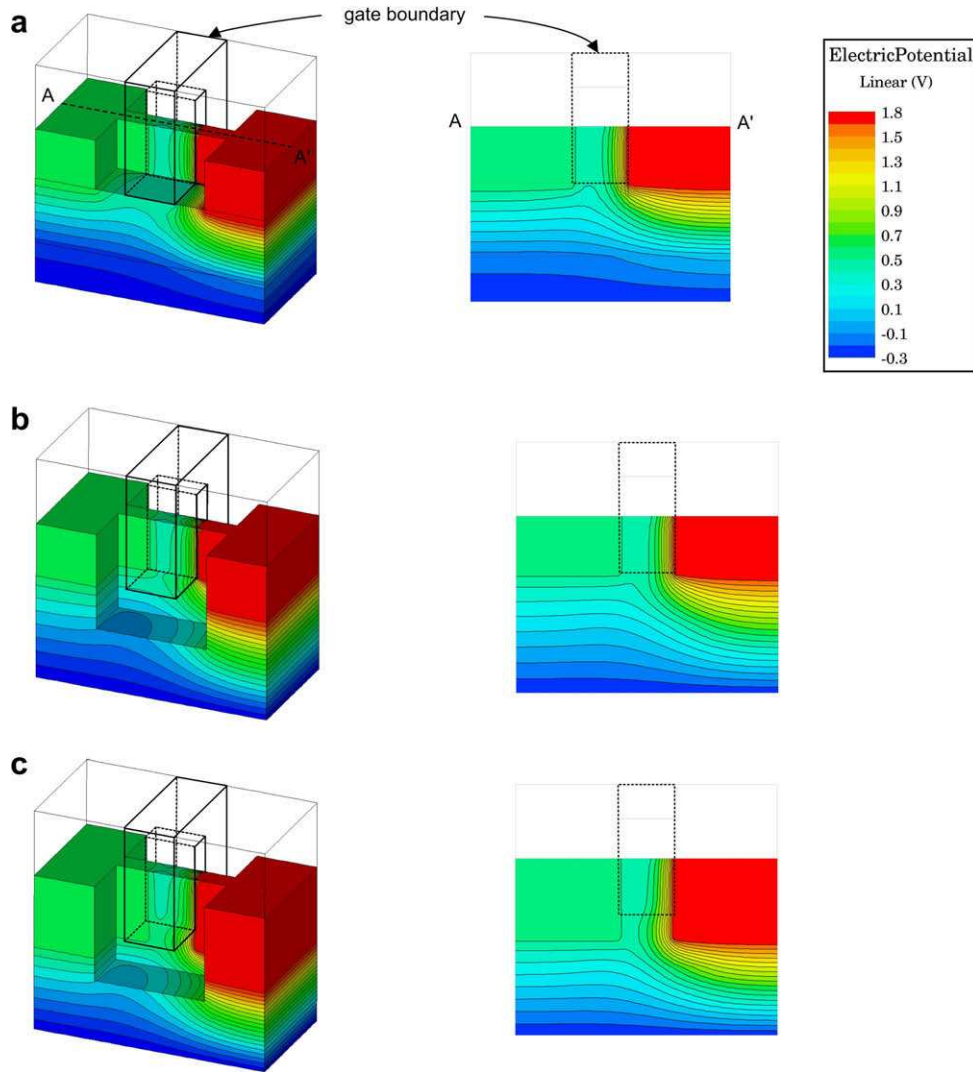


Fig. 3. 3D and 2D cross-sectional potential contour plots at threshold ($V_{GS} = -0.2$ V, $V_{DS} = 1.2$ V) for (a) SOI FinFET, (b) bulk FinFET with S/D junction depth misalignment of $\Delta x_j = 0$ nm and (c) $\Delta x_j = 20$ nm. With deeper junctions, potential barrier between the source and drain is lowered. $L_g = H_{fin} = 50$ nm, $W_{fin} = 20$ nm.

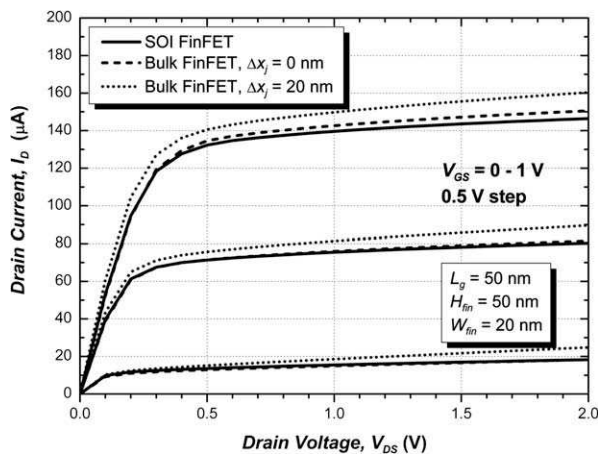


Fig. 4. Comparison of output characteristics for three examined structures. Saturation performance of all devices is good having drive current around 150 μ A with H_{fin} of 50 nm.

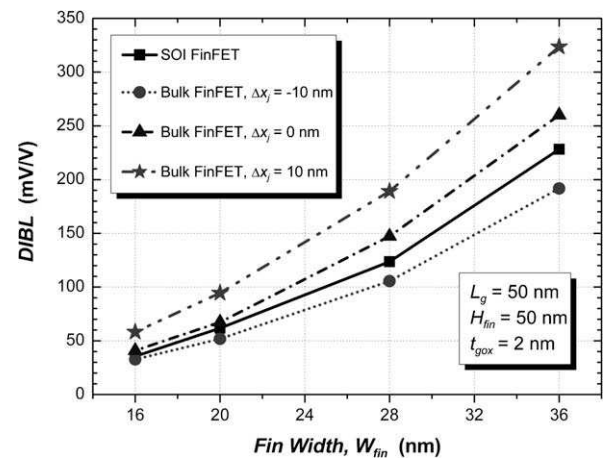


Fig. 5. DIBL versus fin width for SOI FinFET and for bulk FinFET with different S/D junction depths. DIBL is extracted as $(V_{TH,LIN} - V_{TH,SAT}) / \Delta V_{DS}$ at $I_D = 10^{-6}$ A. Shallower junctions improve DIBL of bulk FinFETs for all fin width values.

the Greek letter Π since the polysilicon gate penetrates into the bottom-oxide making the gate-bottom deeper than the silicon fin. Π -gate devices have shown excellent SCE control [16]. Depen-

dences of DIBL and S on fin width for different structures with a misalignment Δx_j as a parameter are shown in Figs. 5 and 6, respectively. An increase in S and DIBL for all structures with

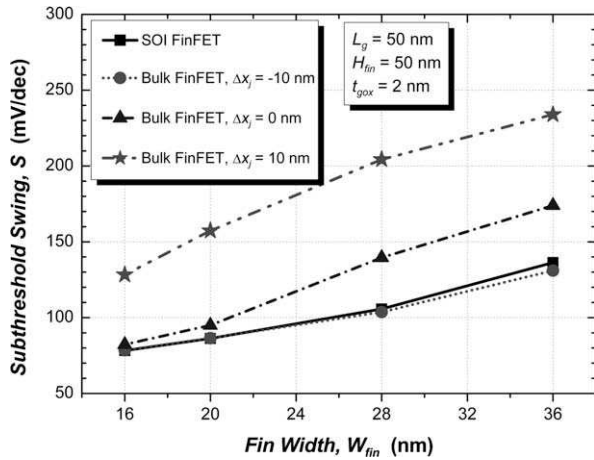


Fig. 6. Subthreshold swing versus fin width for SOI FinFET and for bulk FinFET with different S/D junction depths. S is extracted at $V_{DS} = 1.2$ V.

increasing W_{fin} is caused by the decreased gate control in wider fins. It can be noted that bulk FinFETs with wider fins are more sensitive to S/D junction depth; deeper junctions can deteriorate and shallower junctions can improve device characteristics substantially. Bulk FinFET with $\Delta x_j = -10$ nm (shallower junctions) has equal or even better subthreshold performance than the SOI FinFET, especially in the case of wider fins, e.g. $W_{fin} = 36$ nm. The trade-off between W_{fin} and Δx_j and their impact on DIBL and S are shown in Figs. 7 and 8, respectively, with the marked region showing W_{fin} and Δx_j values needed for achieving low swing S and DIBL. Bulk FinFET with shallower junctions has good subthreshold performance even with wider fins. Therefore, fin width does not have to be scaled as aggressively as previously proposed [17,18] to suppress SCE since there is a simpler way to improve the subthreshold performance.

Deeper gate electrode (shallower junctions) has an enhanced control over the bottom of the fin and its electrostatic control serves as a punch-through stopper which enhances the device subthreshold performance. Shallower S/D junctions are easily accomplished in fabrication, e.g. by regulating the parameters of implantation of S/D regions. With no new masks required, and a simple requirement on the S/D implantation, shallower junctions for the enhancement of the device characteristics presents only a minor change of the fabrication process. Due to this fact, bulk FinFET becomes an eligible candidate for standard bulk CMOS integration, and an excellent candidate for BiCMOS integration with

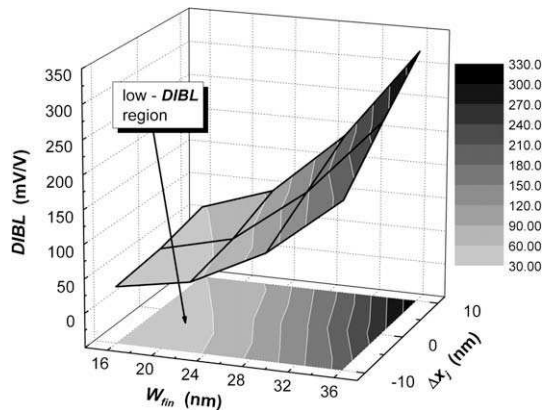


Fig. 7. Sensitivity of DIBL of bulk FinFET to fin width and junction depth misalignment. Structures with shallower junctions and narrower fins have lower DIBL.

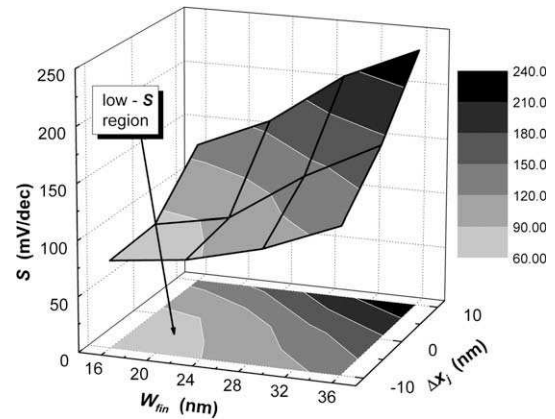


Fig. 8. Sensitivity of subthreshold swing of bulk FinFET to fin width and junction depth misalignment. Structures with shallower junctions have lower S . Structures with wider fins are more sensitive to junction depth misalignment.

pillar-like bipolar transistors [19]. Since the bottom of the gate electrode serves as a punch-through stopper, no n^+ implanted region in the bottom of the fin is needed to suppress the leakage, which was used for FinFET optimization in [20,21]. The implantation of punch-through stopper is difficult to optimize, especially in the case of higher fins, and it necessarily adds to the process complexity. Another problem with the punch-through stopper is the parasitic capacitance it introduces into the structure which could decrease device performance in high-frequency applications. From the above, it is clear that the reduction of S/D junction depth is an effective way to improve device subthreshold performance.

Shallower junctions increase the channel resistance which deteriorates the saturation performance. Therefore, an optimization of junction depth with respect to channel resistance and on-state current is necessary at each technology node. We believe that this is not a problem having in mind that the currents of 1.4 mA/ μ m were obtained in simulations whereas the ITRS requirements on saturation current for LSP (HP) applications are under 0.7 mA/ μ m (1.5 mA/ μ m) even for the 20 nm technology node.

3.2. Body doping influence

Bulk FinFET with $W_{fin} = 16$ nm and $\Delta x_j = -10$ nm is compared to SOI FinFET with identical geometrical dimensions by analyzing the influence of body doping (N_B) on device characteristics. These particular devices were examined due to almost identical subthreshold behavior, hence allowing only the influence of body doping to be investigated. Saturation and linear threshold voltage dependence on body doping is shown in Figs. 9 and 10, respectively, for two examined structures. Threshold voltage was extracted at I_D of 1 μ A and V_{DS} of 0.1 V (linear threshold voltage, $V_{TH, LIN}$) and 1.2 V (saturation threshold voltage, $V_{TH, SAT}$). Since n^+ polysilicon gates are used in simulations, threshold voltages are negative for low and medium body doping values, increasing from approximately -150 mV for $N_B = 10^{15}$ cm $^{-3}$ to 200 mV for $N_B = 5 \times 10^{18}$ cm $^{-3}$. Threshold voltage of both devices is rather insensitive to body doping up to $N_B = 10^{17}$ cm $^{-3}$, but it can be noted that the bulk FinFET exhibits more sensitivity to body doping than the SOI FinFET. Bulk FinFET threshold voltage, both in saturation and linear region, is larger than that of SOI FinFET because of its body-tied structure. Namely, the potential in the fin body around the bottom of the gate is influenced by the grounded substrate which lowers the potential of that region, thus increasing the barrier between the source and drain which leads to small increase of threshold voltage. We note that the difference in threshold voltage between the SOI and the bulk FinFET increases from the case of lin-

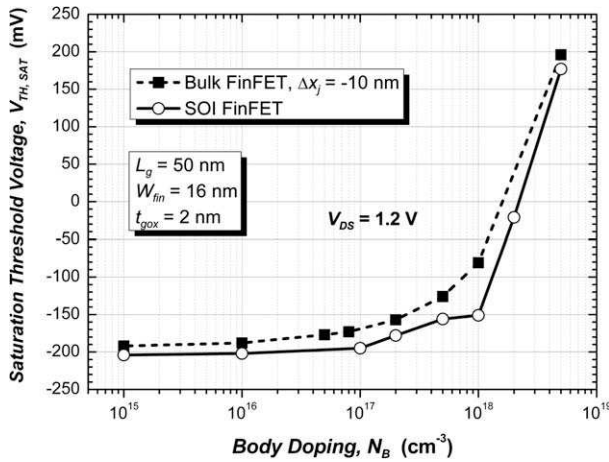


Fig. 9. Saturation threshold voltage versus body doping for SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm. $V_{TH,SAT}$ is defined at $I_D = 10^{-6}$ A and $V_{DS} = 1.2$ V. $L_g = H_{fin} = 50$ nm, $W_{fin} = 16$ nm.

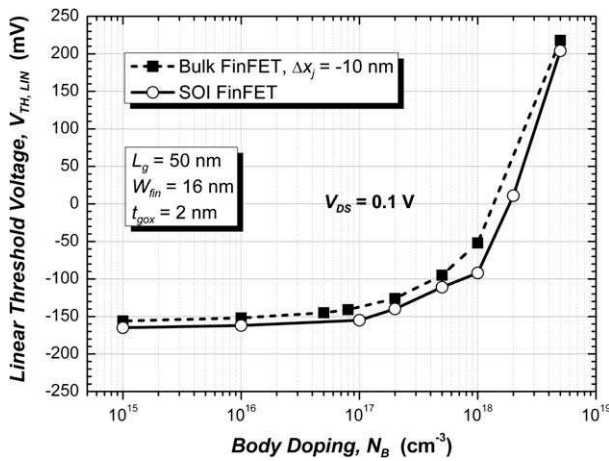


Fig. 10. Linear threshold voltage versus body doping for SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm. $V_{TH,LIN}$ is defined at $I_D = 10^{-6}$ A and $V_{DS} = 0.1$ V. $L_g = H_{fin} = 50$ nm, $W_{fin} = 16$ nm.

ear (10–40 mV) to the case of saturation threshold voltage (20–70 mV), due to slightly higher DIBL of the SOI FinFET. Negative threshold voltage in case of low body doping is not acceptable for most CMOS applications, but this can be overcome by either gate engineering, i.e. using gate material with a proper work-function, or higher channel doping. The modified gate-stacks allow the lightly doped channel to be kept, benefiting carrier mobilities. The adjustment of threshold voltage by increasing channel doping introduces threshold voltage variations due to lack of doping control in extremely scaled channels. However, before new gate-stacks are used in FinFET devices, channel doping may be used to set the threshold voltages to desired values.

For all channel doping cases, the bulk FinFET has lower DIBL values than the SOI FinFET, as presented in Fig. 11. Both structures demonstrate low DIBL, less than 40 mV/V, with difference of around 5 mV/V in favor of the bulk FinFET. Transfer characteristics for different body doping values at $V_{DS} = 1.2$ V are shown in Fig. 12, where it can be noted that the subthreshold swing is nearly the same for both structures and that it does not change significantly with increased body doping. Output characteristics in Fig. 13 for the same two body doping values and $V_{GS} - V_{TH}$ as a parameter show higher drain currents in the case of SOI FinFET. Also, increased body doping affects the bulk FinFET more than the SOI Fin-

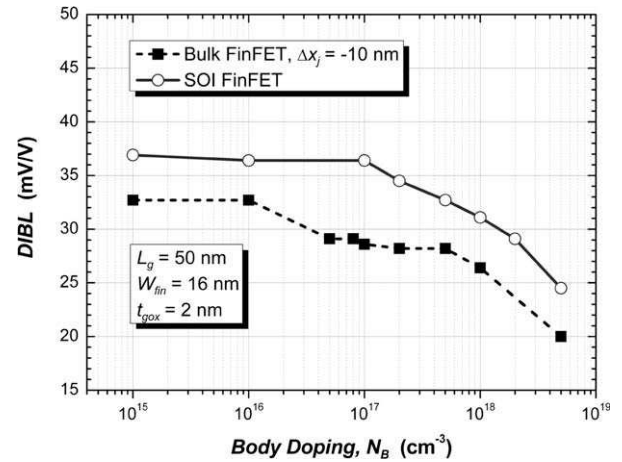


Fig. 11. DIBL versus body doping for SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm. Both devices display excellent subthreshold performance with DIBL under 40 mV/V.

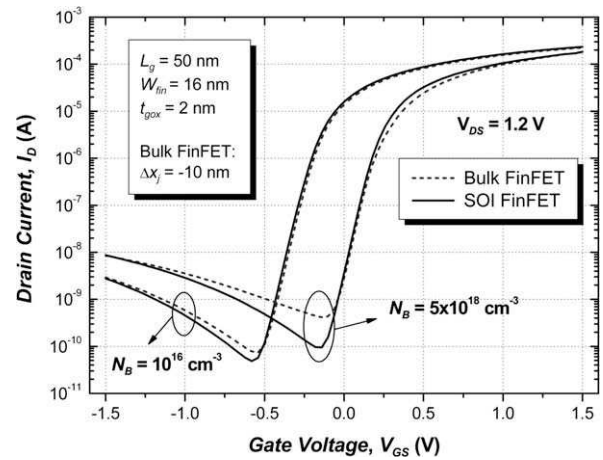


Fig. 12. Comparison of transfer characteristics of SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm for two different body doping values at $V_{DS} = 1.2$ V. Subthreshold swings are identical while bulk FinFET has slightly higher threshold voltage.

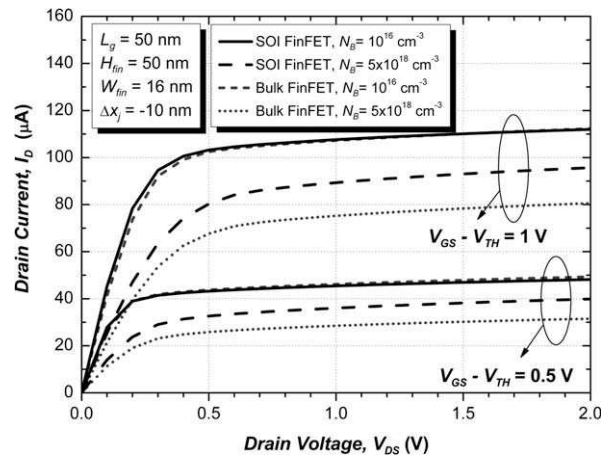


Fig. 13. Comparison of output characteristics of SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm for two different body doping and for $V_{GS} - V_{TH}$ of 0.5 and 1 V. High body doping deteriorates the on-state current more in the case of bulk FinFET than in the case of SOI FinFET.

FET. As the body doping is increased from 10^{16} cm^{-3} to $5 \times 10^{18} \text{ cm}^{-3}$ drain current decreases due to mobility degradation

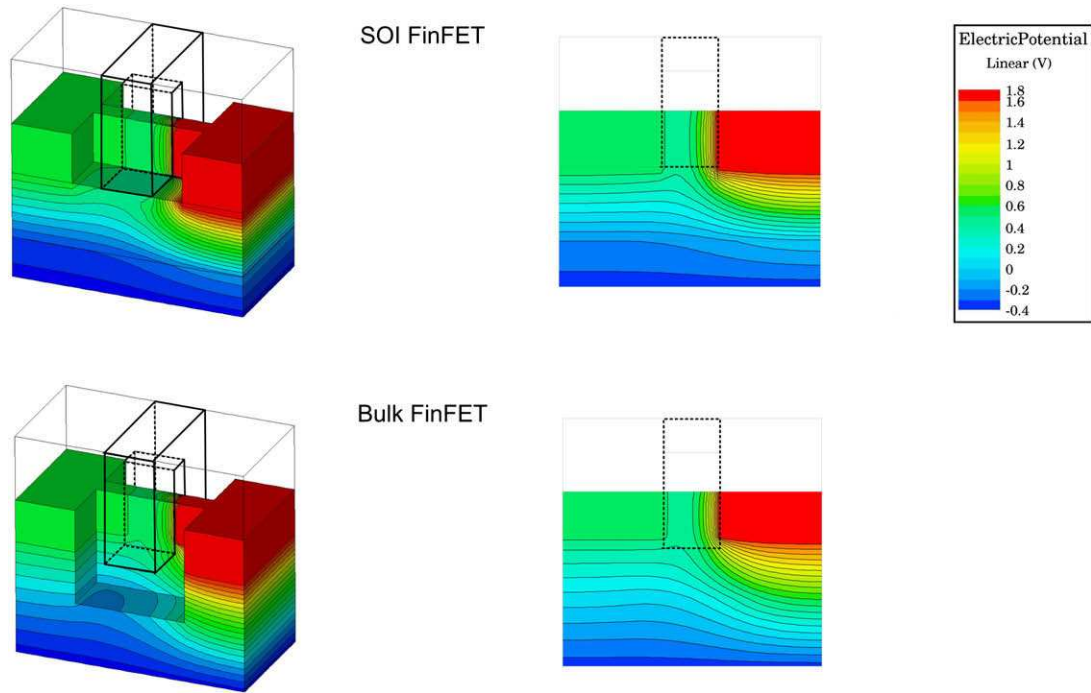


Fig. 14. 3D and 2D cross-sectional potential contour plots at threshold ($V_{GS} = -0.2$ V, $V_{DS} = 1.2$ V) for SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm. For both structures $N_B = 10^{16} \text{ cm}^{-3}$, $L_g = H_{fin} = 50$ nm, $W_{fin} = 16$ nm. In the case of low body doping, electrostatic behavior is approximately the same in both devices.

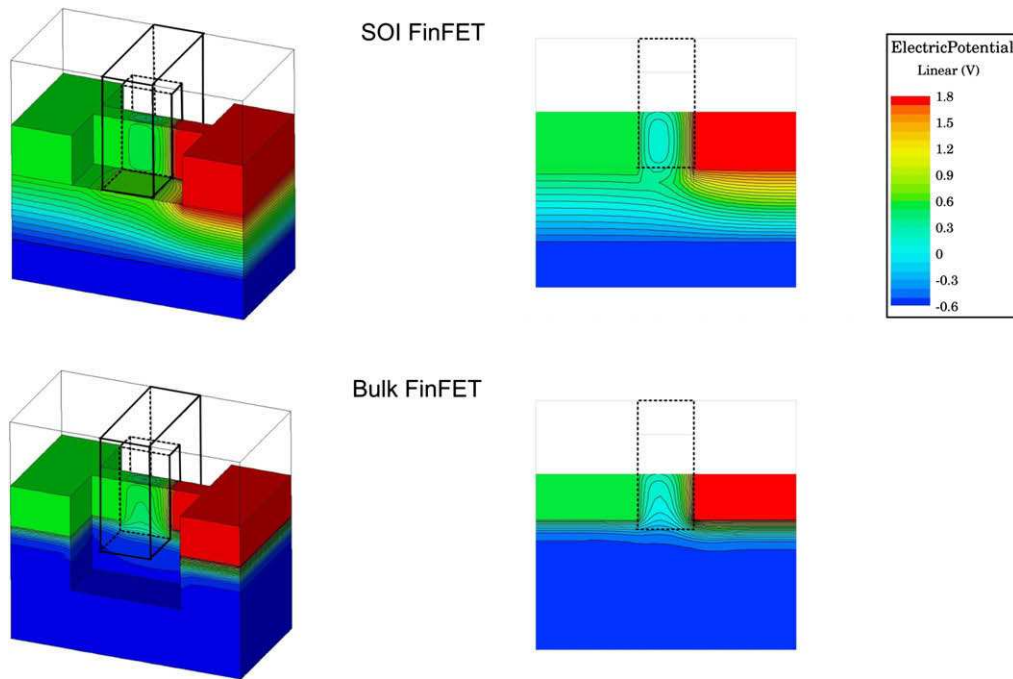


Fig. 15. 3D and 2D cross-sectional potential contour plots at threshold ($V_{GS} = +0.2$ V, $V_{DS} = 1.2$ V) for SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm. For both structures $N_B = 5 \times 10^{18} \text{ cm}^{-3}$, $L_g = H_{fin} = 50$ nm, $W_{fin} = 16$ nm.

with higher impurity scattering, but the decrease is more severe in the case of bulk FinFET where the decrease is up to 28%, for $V_{GS} - V_{TH} = 1$ V. This can be explained by the electric potential distribution in the channel shown by potential contour plot in 3D and 2D cross-sectional views along the channel in Figs. 14 and 15, for body dopings of 10^{16} cm^{-3} and $5 \times 10^{18} \text{ cm}^{-3}$, respectively. At lower doping values, potential distribution in the channel is nearly identical for both structures. Source-to-drain potential barrier is

the same at the top and at the bottom of the channel and both devices have nearly identical current–voltage characteristics. For high doping level, the bending of the energy bands in the channel region is more significant and the inversion layer is confined closer to the gate oxide interface. At the corners of the silicon fin, the electric field is coupled to the silicon layer also through the top and bottom isolation oxide layers, resulting in higher inversion charge in these regions. The consequence is the corner effect, where the

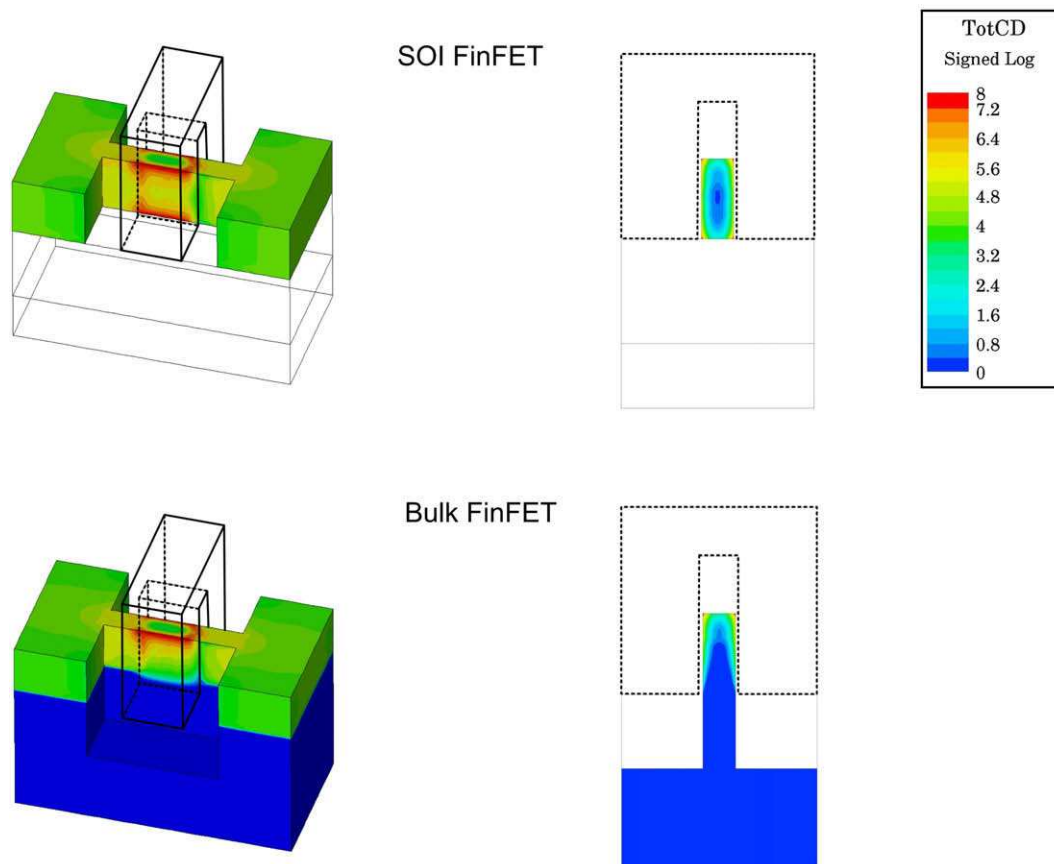


Fig. 16. 3D and 2D cross-sectional current density plots for SOI FinFET and bulk FinFET with $\Delta x_j = -10$ nm. Both structures have $N_B = 5 \times 10^{18} \text{ cm}^{-3}$, $L_g = H_{fin} = 50$ nm, $W_{fin} = 16$ nm. $V_{GS} = +0.2$ V, $V_{DS} = 1.2$ V. The difference in on-state currents from Fig. 13 is obviously caused by the corner effects.

current crowding appears in the fin corners, as evident from Fig. 16. In the case of the SOI FinFET, the current is pushed to four corners, whereas there are only two corners with increased current flow in the bulk device. With less significant corner effect, the bulk FinFET requires higher gate voltage to generate the same inversion charge for the high body doping case, which causes slightly higher threshold voltage. Higher gate voltage and electric field perpendicular to the current flow causes the electrons in the bulk FinFET to have lower mobility compared to its SOI counterpart resulting in lower on-current. In the case of low body doping, the corner effect is minimal as the additional coupling of the gate produces no significant difference in the potential distribution over the whole fin region in either device. Therefore, in order to obtain nearly the same saturation characteristics of the bulk FinFET as in the SOI device, the bulk FinFET should have a lightly doped or undoped body, whereas the threshold voltage control should be given over to metal gate with proper work function. This is fortunate from the process complexity point of view. In combination with shallower S/D junctions, which enhance the device performance, lightly doped or intrinsic transistor body would benefit drive capabilities of the bulk FinFET. Also, low body doping can alleviate discrete impurities problem and other high body doping related problems in extremely thin fins [22].

4. Conclusion

Bulk FinFET subthreshold characteristics can be improved by reducing S/D junction depth with respect to the bottom of the gate which also relaxes the demand on fin width scaling for suppression of SCEs, and improving the bulk FinFET performance to become

equal or better than the SOI counterpart. Using shallower junctions as a punch-through stopper discards the need for the highly doped region in the bottom of the fin which benefits the process cost and complexity. As far as the authors know, this paper is the first report of improvement of the bulk FinFET subthreshold performance in comparison to SOI FinFET without using punch-through stopper implantation. Method of reduction of SCEs with shallower S/D junctions is expected to work even for devices with gate lengths under 50 nm, but an additional optimization must be carried out with respect to channel series resistance at each technology node. The on-state performance of the SOI and the bulk FinFET has also been examined and compared. The higher drain current in case of the SOI FinFET with high body doping is caused by the corner effect, which effectively increases the inversion charge for the same gate voltage. In order to obtain nearly identical on-state performance as the SOI device, the bulk FinFET body should be lightly doped or intrinsic (which benefits the device drive capabilities) and the threshold voltage adjustment should be carried out by the metal gate with proper work-function.

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