

Analysis of Layout Density in FinFET Standard Cells and Impact of Fin Technology

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Abstract— In this paper, the layout density of three-terminal FinFET logic circuits is extensively analyzed. As opposite to previous works, which are focused either on single devices or simplistic circuits, this analysis explicitly includes the geometric constraints that are imposed by the standard cell approach. The impact of the fin technology is analyzed by comparing the lithography- and spacer-defined approaches, as well as evaluating the dependence of layout density on the fin height.

Results show that FinFET standard cells have a layout density that is better than bulk cells even for moderately tall fins. The fin height is also shown to be a powerful knob to improve the layout density in FinFET cells. Analysis also shows that the usually claimed 2X density improvement of the spacer-defined technology compared to the lithography-defined is dramatically reduced in real standard cells, and can be negligible for tall fins. All results are justified through considerations at the physical level of abstraction. Various versions of a 32-nm 44-gate library are laid out to carry out the analysis.

I. INTRODUCTION

CMOS devices are showing their limits at each new technology generation, as their electrical properties are rapidly degrading in the nanometer regime [1], [2]. For this reason, a considerable effort is being devoted to develop alternative devices that scale better and are compatible with the CMOS manufacturing process [2]-[4]. In particular, FinFET devices are considered an excellent replacement of bulk CMOS in future technology nodes (e.g., from 32-nm technology node on), thanks to the better control of short channel effects and leakage, as well as compatibility with standard CMOS processes [2]-[5].

Until now, research on FinFETs has been done mainly at the device and transistor level of abstraction, whereas much less understanding has been gained at the physical level. Indeed, until now FinFET layout issues were only analyzed in the simplistic case of single devices or extremely simple circuits [3], [4], [6]. Clearly, these results are not representative of real VLSI implementations, as the standard cell approach (adopted in most VLSI designs) imposes many additional geometric constraints that must be obviously considered to correctly evaluate the layout density. Moreover, general understanding of the FinFET layout density potential is made even harder by its

dependence on the specific technology adopted to manufacture the “fin” (which is the core of the FinFET). Indeed, the dependence of layout density on the fin technology cannot be grasped from the knowledge acquired in traditional bulk CMOS technology, but requires further analysis.

In this paper, the layout density of FinFET standard cells is analyzed. The impact of the fin technology is explicitly evaluated, and quantitative results are extensively justified to gain an insight into FinFET layout issues. Results obtained with FinFET cells are also compared to bulk CMOS standard cells to identify the cases where they exhibit some (dis)advantage in terms of layout density.

II. BRIEF REVIEW OF FINFETs AND THEIR LAYOUT

The structure of a three-terminal FinFET device is based on the vertical fin in Fig. 1, which is made up of a source-drain diffusion (light gray) surrounded by the gate (dark gray), and separated from it by the gate oxide (in black). The fin implements an elementary MOS device having an effective channel length equal to the fin length L_{FIN} , and an effective channel width W_{min} equal to [7]

$$W_{min} \approx 2 \cdot h_{FIN} \quad (1)$$

where it was considered that the upper side of the gate gives a negligible contribution to W , because it is separated from the fin by a thicker oxide [5].

To keep short-channel effects under control, the fin height h_{FIN} , the fin length L_{FIN} and the silicon thickness T_{SI} in Fig. 1 must be properly scaled [5]. The typical dimensions at the 32 technology node are summarized in

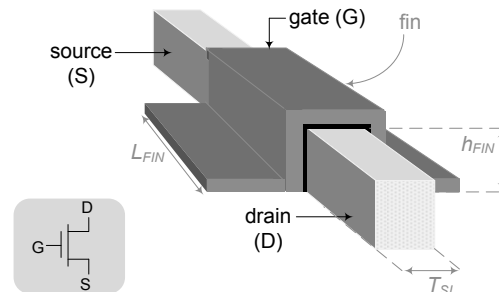


Fig. 1. Three-terminal FinFET geometrical structure.

Table I [5]. Since the FinFET fabrication differs from the bulk CMOS only for the fin, its layout design rules are given by the standard set of bulk CMOS rules and the additional set of fin-specific rules in Table I.

In general, to build a FinFET with channel width $W > W_{min}$, multiple fins sharing a common lateral diffusion are connected in parallel, whose number N_{FIN} is [5]

$$N_{FIN} = \frac{W}{W_{min}}. \quad (2)$$

As an example, Fig. 2b shows a FinFET with $N_{FIN}=4$ (a bulk device is also shown in Fig. 2a as a reference). Being N_{FIN} integer, from (2) the transistor channel width is quantized to multiples of W_{min} , although this is well known not to be a concern in the optimization of transistor sizes [3], [4].

III. UNDERSTANDING THE IMPACT OF FIN TECHNOLOGY ON THE LAYOUT DENSITY OF A SINGLE DEVICE

From Fig. 2b, the area occupied by the fins in a FinFET device is proportional to $(N_{FIN}-1) \cdot P_{FIN}$, where P_{FIN} is fin pitch (defined as the distance between the middle section of two contiguous fins). Since a significant fraction of the device layout is occupied by the fins, at the process level the transistor area can be reduced by reducing the fin pitch P_{FIN} and the number of fins N_{FIN} for a given channel width, from (1)-(2). Parameters P_{FIN} and N_{FIN} are strongly influenced by the adopted fin technology, as discussed in the following.

The minimum fin pitch P_{FIN} is set by the fin technology, which currently can be chosen between two different approaches, the lithography- and the spacer-defined technology [5], [8], [9]. The former approach is based on straightforward application of lithography steps, hence the minimum pitch P_{FIN} is limited by the resolution of the technology. On the other hand, spacer-defined technology halves the minimum fin pitch P_{FIN} through a multiple-step procedure that enables a sub-lithographic resolution [9], [10] (typical values of P_{FIN} in both FinFET technologies are reported in Table I [3], [5], [6]). For this reason, it is usually claimed that spacer-defined technology improves the FinFET layout density by a factor of 2 [9]-[11]. This usual belief will be widely commented (and negated) in the following sections.

On the other hand, the number of fins N_{FIN} for a given channel width can be reduced by increasing W_{min} from (2), which in turn is achieved by increasing the fin height h_{FIN} , from (1). However, the layout density of FinFET devices cannot be arbitrarily improved because h_{FIN} is limited by practical considerations. Indeed, the ratio h_{FIN}/T_{SI} is limited by the effectiveness of the etch technology in building tall and narrow vertical structures (i.e., with high h_{FIN}/T_{SI}) [12]. Typical feasible values of h_{FIN}/T_{SI} are in the order of a few units, and can be as high as 4 in very aggressive processes

TABLE I

LAYOUT DESIGN RULES FOR THE FIN (32-NM TECHNOLOGY NODE)

Physical fin dimensions		Fin pitch P_{FIN} [nm]	
L_{FIN} [nm]	35	lithography-defined	80
T_{SI} [nm]	23	Spacer-defined	40
$h_{FIN}=2T_{SI}$ [nm]	46		



Fig. 2a. Layout of a bulk device ($W=4W_{min}$).

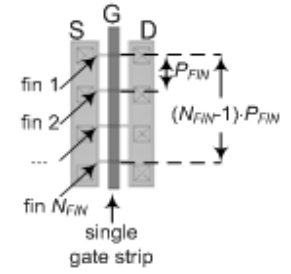


Fig. 2b. Layout of a FinFET device ($N_{FIN}=4$).

[9], [13]. Reasonable values of h_{FIN}/T_{SI} are around 2, as assumed in Table I and [5].

To evaluate the layout density of 32-nm FinFET devices in comparison with a bulk technology with same feature size, the area of a single FinFET device normalized to that of a bulk device with the same W is plotted in Fig. 3 for both a lithography- and spacer-defined technology and h_{FIN}/T_{SI} ranging from 1 to 4. From this figure, lithography-defined FinFETs with minimum fin height $h_{FIN}=T_{SI}$ have approximately the same area as bulk CMOS transistors (the average area ratio is 0.95). On the other hand, spacer-defined FinFETs with $h_{FIN}/T_{SI}=1$ have a significantly better layout density, as the normalized area is close to 0.6 regardless of W . Hence, spacer-defined technology permits a 40% device area reduction, compared with bulk CMOS technology. Moreover, the spacer-defined technology permits to improve the layout density of a single device by a factor of 1.61X, compared to the lithography-defined FinFET, according to data in Table II. This improvement is lower than the usually claimed factor of 2. This is because the device area includes also the contribution of other

TABLE II
AVERAGE LAYOUT DENSITY IMPROVEMENT OF SPACER-DEFINED COMPARED TO LITHOGRAPHY-DEFINED FINFET (IDEALLY, IT IS 2X)

h_{FIN}/T_{SI}	Single device	Std. cell
1	1.61X	1.39X
2	1.45X	1.22X
3	1.32X	1.08X
4	1.24X	1.12X

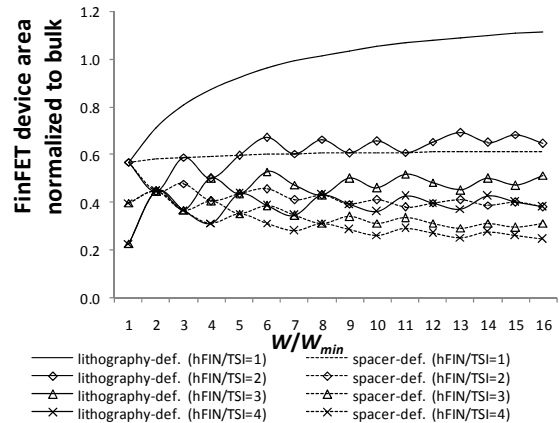


Fig. 3. Area of FinFETs normalized to bulk device with the same channel width (32-nm lithography- and spacer-defined fin technology).

polygons (e.g. the source/drain diffusion and the gate overhang in Fig. 2b) whose area is independent of P_{FIN} , and hence cannot be reduced with spacer-defined technology.

As discussed above, the adoption of a taller fin permits to improve the FinFET layout density. In particular, from Fig. 3 the area of lithography-defined (spacer-defined) FinFETs normalized to bulk CMOS reduces to 0.6 (0.4) for the moderate value of $h_{FIN}=2T_{SI}$, and 0.4 (0.3) for the aggressive fin height $h_{FIN}=4T_{SI}$. As a result, lithography-defined (spacer-defined) FinFET devices exhibit an area reduction by 40-60% (60-70%) compared to bulk CMOS transistors, for moderate (aggressively high) values of the fin height. Interestingly, under these higher values of h_{FIN} , the layout density advantage of the spacer-defined technology over the lithography-defined is only 1.45X for the moderate value $h_{FIN}=2T_{SI}$, and only 1.24X for the high value $h_{FIN}=4T_{SI}$.

IV. FINFET STANDARD CELLS: LAYOUT DENSITY ANALYSIS VS. FIN TECHNOLOGY WITH $h_{FIN}=T_{SI}$

The results in Section III give some hint on the layout density of FinFET devices, but are not representative of real standard cell circuits. Indeed, with referral to Fig. 4a that depicts the layout of a 4X NOR2 gate, the standard cell approach imposes geometrical constraints on the cell dimension (i.e., parameters H_{CELL} , H_p , H_n in Fig. 4a) and the placement of transistors within the cell (i.e., alignment of p- and n-channel gates, parallel orientation, and so on). Clearly, these constraints further degrade the layout density, as discussed in the following.

To evaluate the impact of the above constraints on the layout density of FinFET standard cells, we laid out various versions of a 44-gate library cell in the adopted 32-nm technology. The library consists of various basic logic gates (inverter, NAND2, NAND3, NAND4, NOR2, NOR3, NOR4, AOI21, AOI22, OAI21, OAI22, carry logic, ...). Each cell was implemented with different drive strengths (3-4 for each cell), ranging from 1X to 16X (up to 32 X for the inverter gate). The standard cell height H_{CELL} was set to 14 tracks of metal 2 (i.e., 1.4 μm for the adopted 32-nm technology), whereas the ground/supply rails are 2.5-track tall (i.e., 0.25 μm). The height H_p of the cell area devoted to p-channel transistors was set to 1.5 times the height H_n of the area devoted to n-channel FinFETs (which is typical value). As an example, the layout of the 4X NOR2 cell is depicted in Figs. 4b-4c for the lithography- and spacer-defined FinFET.

The area of a few selected FinFET cells normalized to the bulk CMOS counterparts is reported in Fig. 5 for $h_{FIN}=T_{SI}$ (a very similar trend was found for the other cells). The resulting average ratio between the area of FinFET cells and the bulk counterparts is reported in Table III. From this table, the area of lithography-defined FinFET cells is close to that of the bulk CMOS counterparts. In particular, the average ratio between each lithographic- defined FinFET cell and its bulk counterpart is equal to 0.95, hence FinFET cells typically allow for a modest 5% area reduction compared to bulk CMOS cells. On the other hand, from Fig. 5 and Table

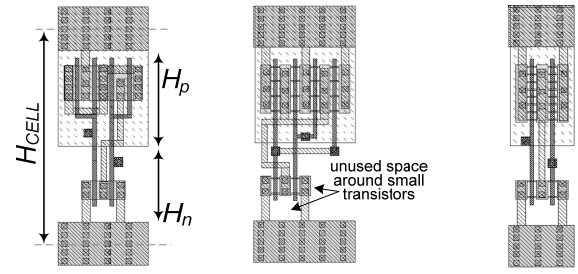


Fig. 4a. Layout of 4X NOR2 gate (bulk CMOS).

Fig. 4b. Layout of 4X NOR2 (lithography-defined FinFET).

Fig. 4c. Layout of 4X NOR2 (spacer-defined FinFET).

III, spacer-defined FinFET cells have a better layout density, with an average area saving of 32% compared to bulk cells. More specifically, from Fig. 5 the area ratio between FinFETs and bulk CMOS cells tends to decrease when increasing the cell strength. For example, this trend can be seen from the analysis of the NAND2 gate with 2X, 4X, 8X and 16X strength, and it is even more pronounced for spacer-defined FinFETs. This trend is justified by the fact that high-strength cells contain bigger transistors, whose area represents a larger fraction of the cell area (it dominates over the area of supply rail, as well as the unused space around transistors shown in Fig. 4b). Hence, high-strength cells fully benefit from the device area reduction observed in Section III. Dual considerations can be made for low-strength cells.

Regarding the comparison between lithography- and spacer-defined FinFET cells, the layout density improvement offered by the latter w.r.t. the former is found from Table III, and is reported in Table II (see last column). From the latter table, the area advantage of the spacer-defined over the lithography-defined cells is only 1.39X, which is even lower than the factor 1.61X that was found for single devices (see second column of Table II). This further reduction in the area advantage of spacer-defined technology is due to the additional geometrical constraints associated with the standard cell structure, including the fixed height H_{CELL} , the

TABLE III
AVERAGE FINFET CELL AREA NORMALIZED TO ITS BULK COUNTERPART

$h_{FIN}/T_{SI} \rightarrow$	1	2	3	4
Lithography-defined	0.95	0.7	0.59	0.58
Spacer-defined	0.68	0.57	0.55	0.52

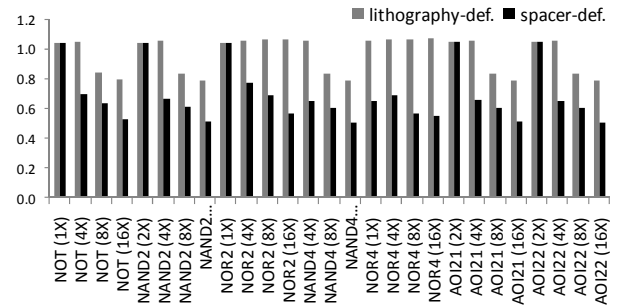


Fig. 5. Area of FinFET standard cells normalized to the bulk CMOS counterparts ($h_{FIN} = T_{SI}$).

unused space above/below small transistors that was discussed above (Fig. 4b), and the presence of polygons whose area does not shrink when reducing the fin pitch (e.g., supply rails). This explains why the usually claimed 2X improvement in the layout density of spacer-defined FinFET is significantly reduced in real circuits. In particular, this factor of 2 is reduced by 20% when considering the area of a single device (due to polygons whose area does not scale with the fin pitch), and by another 10% due to the additional geometric constraints that are imposed by standard cells.

V. IMPACT OF FIN HEIGHT H_{FIN} AND FINAL REMARKS

Let us analyze the influence of the fin height on the comparison between FinFET and bulk cells. The resulting average area of FinFET cells normalized to the bulk CMOS counterparts for $h_{FIN}/T_{SI}=2\ldots 4$ is reported in Table III. As an example, the area ratio for a few selected cells is reported in detail in Fig. 6 for the case $h_{FIN}/T_{SI}=3$.

From Table III, the area of FinFET cells always reduces when h_{FIN} is increased, as expected from the considerations in Section III. In particular, the area saving enabled by the increase in h_{FIN} is more pronounced for lithography-defined FinFETs. This is explained by observing that, compared to the spacer-defined, the area of lithography-defined FinFET cells tends to be more dominated by transistors due to the doubled fin pitch (this argument is similar to that used in Section IV to compare fin technologies). Hence, lithography-defined FinFET cells gain a larger benefit from the reduction of N_{FIN} , and hence from the increase in h_{FIN} from (1)-(2). For example, from Table III the lithography-defined (spacer-defined) FinFET cells exhibits an average area reduction by a factor of $0.95/0.58=1.64$ ($0.68/0.52=1.31$) when increasing h_{FIN} from T_{SI} to $4T_{SI}$. These results confirm that the fin height is a powerful knob to improve the FinFET layout density for any type of fin technology, and is even more powerful in lithographic-defined processes.

Regarding the comparison between the lithography- and spacer-defined technologies, the layout density improvement permitted by the latter tends to significantly reduce at higher fin heights. To clarify this point, let us consider the layout density improvement for $h_{FIN}/T_{SI}=1\ldots 4$, which is reported in Table II (see last column). From this table, the improvement offered by the spacer-defined technology reduces to 1.22X for moderately high fins ($h_{FIN}/T_{SI}=2$), and is very close to 1 for high fins ($h_{FIN}/T_{SI}=4$). This means that the usually claimed 2X improvement is almost completely lost in practical FinFET standard cells even when moderate fin heights are employed. In other words, as opposite to the usual belief, it is wrong to extrapolate the area saving in real FinFET circuits from the fin density improvement enabled by the spacer-defined technology.

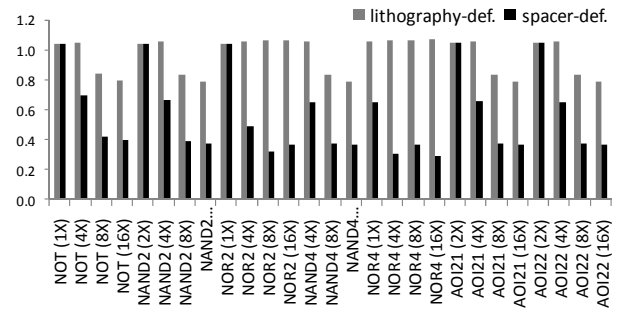


Fig. 6. Area of FinFET standard cells normalized to the bulk CMOS counterparts ($h_{FIN}=3T_{SI}$).

Finally, observe that comparison between Fig. 2 and Table III shows that results for single devices (Section III) are not consistent at all with the analysis of standard cells. This clearly confirms that results in previous works based on the analysis of a single device are not representative of the layout density of standard cell circuits.

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