

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,

AND

APPLE, INC.,

Petitioners

v.

MARLIN SEMICONDUCTOR LIMITED.

Patent Owner

Case IPR2025-00864

Patent No. 9,184,292

**DECLARATION OF DR. SANJAY BANERJEE
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,184,292**

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I, Sanjay Banerjee, declare as follows:

I. INTRODUCTION

1. I have been retained as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 9,184,292 (“the ’292 patent”) (EX1001).¹ I have been asked to consider whether prior art references disclose or suggest the features recited in claims 1-20 (“the challenged claims”) of the ’292 patent. My opinions are set forth below.

II. BACKGROUND AND QUALIFICATIONS

2. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. I have been a faculty member at UT Austin since 1987.

3. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world’s first 4-Megabit DRAM, for which I was co-

¹ In this Declaration, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’292 patent.

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recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

4. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

5. I am a leading researcher and educator in various areas of CMOS transistor device fabrication technology, including the fabrication, characterization and application of FinFETs, DRAM, SRAM and flash memory devices, and nanotechnology. I have published numerous experimental and theoretical papers on vertical transistors, including FinFETs, and relevant process technologies including lithography, reactive ion etching, high-k gate dielectric deposition by atomic layer deposition, and epitaxy of strained Si-Ge-C heterostructures. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

6. At the University of Texas, I served as the director of the Microelectronics Research Center from Sept. 1999 to Jan. 2025. I also served as the director of the South West Academy of Nanoelectronics from its inception through the end (Dec. 2017), one of three centers in the United States established to develop a replacement for MOSFETs. I have been the Site Director of the NSF Nanofabrication Coordinated Infrastructure Facility from 2004-2025.

7. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 50 Ph.D. and 60 MS students.

8. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes

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and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

9. I have previously served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry. I currently serve on the Advisory Board of Advanced Nano Devices who fabricate vertical power transistors.

10. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award

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in 1988, and several SRC Inventor Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

11. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

12. Additional details about my employment history, fields of expertise, and publications are further included in my curriculum vitae.

13. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or in any litigation involving the '292 patent.

III. MATERIALS REVIEWED

14. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding systems and processes in the field of user interface technologies.

15. In forming my opinions expressed in this Declaration, I reviewed the following materials:

EX1001	U.S. Patent No. 9,141,292 (“the ’292 patent”)
EX1004	Prosecution History of U.S. Patent App. No. 14/340,267
EX1005	U.S. Patent Application Publication No. 2008/0308848 (“Inaba”)
EX1006	U.S. Patent Application Publication No. 2011/0108920 (“Basker”)
EX1007	U.S. Patent Application Publication No. 2009/0057846 (“Doyle”)
EX1008	U.S. Patent No. 8,942,030 (“Liaw”)
EX1009	U.S. Patent No. 7,297,581 (“Hill”)
EX1010	U.S. Patent Application Publication No. 2008/0230852 (“Yu”)
EX1011	RESERVED
EX1014	U.S. Patent No. 8,625,334 (“Liaw-334”)
EX1015	U.S. Patent Application Publication No. US2008/0020515 (“White”)

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EX1016	J. Franco, et al., “Improvements of NBTI reliability in SiGe p-FETs,” <i>2010 IEEE International Reliability Physics Symposium</i> , Anaheim, CA, USA, 2010, pp. 1082-1085.
EX1017	J. Huang et al., “Mechanisms limiting EOT scaling and gate leakage currents of high-k/metal gate stacks directly on SiGe and a method to enable sub-1nm EOT,” <i>2008 Symposium on VLSI Technology</i> , Honolulu, HI, USA, 2008, pp. 82-83.
EX1018	J. Oh <i>et al.</i> , “Additive mobility enhancement and off-state current reduction in SiGe channel pMOSFETs with optimized Si Cap and high-k metal gate stacks,” <i>2009 International Symposium on VLSI Technology, Systems, and Applications</i> , Hsinchu, Taiwan, 2009, pp. 22-23.
EX1019	S. M. Sze, “Physics of Semiconductor Devices,” <i>John Wiley & Sons</i> , 1981, Chapter 8, pp. 431-456.
EX1020	J. D. Plummer, “Silicon VLSI Technology: Fundamentals, Practice and Modelling,” <i>Prentice Hall</i> , 2000, Chapter 10, pp. 637-650.
EX1021	RESERVED
EX1022	RESERVED
EX1023	U.S. Patent Application Publication No. 2007/0069302 (“Jin”)
EX1024	U.S. Patent No. 6,787,406 (“Hill-406”)
EX1025	H. Adhikari <i>et al.</i> , “High mobility SiGe shell-Si core omega gate pFETS,” <i>2009 International Symposium on VLSI Technology, Systems, and Applications</i> , Hsinchu, Taiwan, 2009, pp. 136-138
EX1026	R. Bijesh <i>et al.</i> , “Hole mobility enhancement in uniaxially strained SiGe FINFETs: Analysis and prospects,” <i>69th Device Research Conference</i> , Santa Barbara, CA, USA, 2011, pp. 237-238.
EX1027	Intel Newsroom (2011)

EX1028	Intel 22nm Announcement Presentation (2011)
EX1029	Intel 22nm Details Presentation (2011)
EX1030	S. Bedell <i>et al.</i> , “Opportunities and Challenges for Germanium and Silicon-Germanium Channel p-FETs,” <i>ECS Transactions</i> , Vol. 19, No. 1
EX1031	J. Mitard <i>et al.</i> , “High-mobility 0.85nm-EOT Si _{0.45} Ge _{0.55} -pFETs: Delivering high performance at scaled VDD,” <i>2010 International Electron Devices Meeting</i> , San Francisco, CA, USA, 2010, pp. 10.6.1-10.6.4.
EX1032	M. Poljak <i>et al.</i> , “Improving bulk FinFET DC performance in comparison to SOI FinFET,” <i>Microelectronic Engineering</i> , Vol. 86, Issue 10, Oct. 2009, Pp. 2078-2085.
EX1033	Mukherjee, Debasish and Hemanta Kr. “Static Noise Margin Analysis of SRAM Cell for High Speed Application,” <i>IJCSI International Journal of Computer Science Issues</i> , Vol. 7, Issue 5, Sept. 2010.
EX1034	V. Huard <i>et al.</i> , "NBTI degradation: From transistor to SRAM arrays," <i>2008 IEEE International Reliability Physics Symposium</i> , Phoenix, AZ, USA, 2008, pp. 289-300.
EX1035	M. Alioto, “Analysis of layout density in FinFET standard cells and impact of fin technology,” <i>Proceedings of 2010 IEEE International Symposium on Circuits and Systems</i> , Paris, France, 2010, pp. 3204-3207.
EX1036	Zheng Guo, S. Balasubramanian, R. Zlatanovici, Tsu-Jae King and B. Nikolic, “FinFET-based SRAM design,” <i>ISLPED '05. Proceedings of the 2005 International Symposium on Low Power Electronics and Design</i> , 2005., San Diego, CA, USA, 2005, pp. 2-7.
EX1037	U.S. Patent Application Publication No. 2007/0194833
EX1038	W. Qi <i>et al.</i> , “Investigation on solid phase epitaxy of deposited SiGe film on a Si substrate,” <i>Thin Solid Films</i> , Vol. 293, Issues 1–2, 30 Jan. 1997, Pp. 310-314.

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EX1039	U.S. Patent No. 8,367,498 (“Chang”)
EX1040	Cotte et al., “Predicting critical dimension uniformity in advanced electron-beam projection lithography masks,” <i>J. Vac. Sci. Technol. B</i> 21, 3027–3031 (2003).

I also considered any other documents and materials I refer to in this Declaration.

16. My opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the state of the art, the prior art, and the claims and the specification of the '292 patent at the time of the alleged invention, which I discuss below.

17. I have been asked to consider that the time of the alleged invention of the '292 patent was around early 2012 (including and up to February 9, 2012), which corresponds to the filing date of the earliest application associated with the '292 patent.

18. Based on my experience and expertise, it is my opinion that certain reference(s) disclose and/or suggest all the features recited in challenged claims of the '292 patent, as I discuss in detail below.

IV. PERSON OF ORDINARY SKILL IN THE ART AND THE TIME OF THE ALLEGED INVENTION

19. I am familiar with the level of ordinary skill in the art regarding the '292 patent as of around February 9, 2012. Considering the '292 patent, the technology, the educational level and experience of workers in the field relating to the patent, and problems and solutions in that field, and drawing on my own experience, I believe a person of ordinary skill in the art at the time of the alleged invention (around February 9, 2012) would have had a master's degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as for example, integrated circuit device (or transistor) design and/or manufacturing. Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for less formal education.

20. My opinions in this Declaration regarding the '292 patent and the prior art (including the state of the art) are from the perspective of one of ordinary skill in the art as I defined above, during the relevant timeframe (e.g., the time of the alleged invention), which I discussed above as being around February 9, 2012.

V. TECHNICAL BACKGROUND

21. Below, I present a brief overview of certain aspects of semiconductor devices and processes at the time of the alleged invention for the '292 patent. The functionalities and concepts I describe below in this technical background section reflect the state of the art that a person of ordinary skill in the art would have had knowledge of and understood prior to and at the time of the alleged invention of the '292 patent. I rely on, and incorporate as applicable (even if not expressly mentioned below in Section IX), the following disclosures and opinions to support my opinions in this Declaration, including those opinions relating to how the prior art discloses and/or suggests the challenged claims of the '292 and how and why a person of ordinary skill in the art would have been motivated to consider and combine the disclosures and suggestions from that prior art as I explain below in Section IX. The concepts below would have been within the knowledge and mindset of a person of ordinary skill in the art at the time.

A. FinFETs

1. Device Features – Fin Height and Width

22. A field-effect transistor (FET) functions essentially as a switch controlled by voltage applied to a “gate” between “source” and “drain” regions. EX1019, 9-10, 14-15, FIGs. 3, 6; EX1020, 40-51, FIG. 1-11. When the FET is

turned on, current flows between the source and drain regions through a “channel” formed under the gate of the FET. EX1019, 9-10, 14-15, FIGs. 3, 6; EX1020, 40-51. Two general types of FETs known in the art at the time include planar FETs and non-planar three-dimensional (3D) FETs, such as FinFETs. EX1032, 1. There are two types of transistors. The first type of transistor is n-type transistors in which the current is formed by the movement of electrons in the transistor channel. I’ll use “nFETs” or “nFinFETs” to represent n-type transistors or n-type FinFETs. The second-type of transistor is p-type transistors in which the current is formed by the movement of holes in the transistor channel. I’ll use “pFETs” or “pFinFETs” to represent p-type transistors or p-type FinFETs

23. The current a FinFET provides depends on its physical dimensions, including **channel width** (for *tri-gate* FinFETs: effectively w (fin width) + $2 \cdot H$ (fin height) or for *double-gate* FinFETs: $2 \cdot H$ as shown in Figure 1 below, and gate length (the dimension where the gate electrode overlapping the fin). EX1010, [0004], FIG. 1 (below).

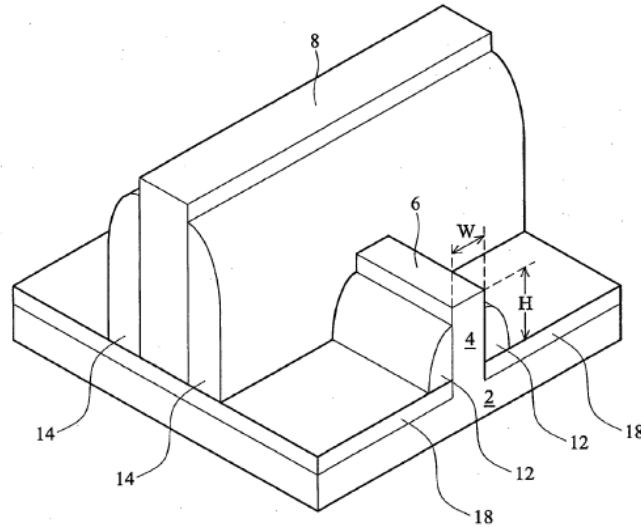


FIG. 1 (PRIOR ART)

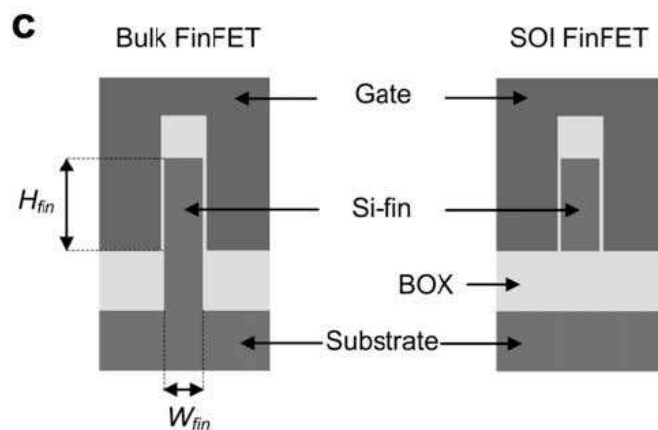
24. Adjusting fin width and/or fin height to adjust FinFET performance was routine and well-known. EX1010, [0010]; EX1033, 1-3.

2. Fabrication of FinFETs – Bulk and SOI FinFETs

25. Semiconductor devices, including FinFETs, were known to be built upon wafers. As was known in the art, a “bulk” silicon wafer is made of silicon. EX1032, 1 (“The implementation of FinFET structure in bulk silicon wafers”). Generally, the fabrication of FinFETs starts with forming their Fins or Fin structures. The Fin structures for bulk FinFETs may be formed by etching a bulk silicon substrate and are made of the same material as the substrate. EX1023, [0045]-[0048] (disclosing forming fin structures on a bulk silicon wafer by etching, e.g., “form[ing]

recesses or trenches...on the substrate”); EX1008 8:21-55. Isolation layers between fins (e.g., shallow-trench isolation (STI)), and a gate dielectric in the selected regions along the fin, are then formed. *Id.*, EX1005, [0063]. Metallization may be used to create gate, electrical terminals, and contacts on the FinFET. *See, e.g.*, EX1008, 11:52-12:4; 7:57-8:14.

26. Another type of substrate, known as silicon-on-insulator (SOI), may be used to form SOI FinFETs. EX1023, [0019], [0030]. Bulk FinFETs and SOI FinFETs have nearly identical structures as shown below. EX1032, 1-2. Thus, the fabrication processes and the layout for circuits using bulk FinFETs could be readily applied to circuits using SOI FinFETs and vice versa.



EX1032, FIG. 1C.

B. SiGe pFinFET for Performance Enhancement

27. It was known FinFET performance could be improved by incorporating germanium (Ge) or silicon germanium (SiGe) into the fins of the FinFETs, especially the fins of pFinFETs. There has been a general trend to include Ge/SiGe into the transistor's channel, which traditionally has been made of silicon. It was known “[p]lanar Si channel device may not be able to provide for the high performance needed in future MOSFETs” (EX1025, 1) and Ge was “reported to demonstrate performance improvement over Si” (*id.*). It was known that hole mobility was improved by using SiGe channel than Si channel (*id.*) and “further hole mobility enhancement in [Silicon] pFINFETs is limited.... **SiGe channel FINFET is an attractive replacement**” (EX1026, 1). Using SiGe channel in pFETs allowed lower temperature dopant activation and improved gate dielectric scalability. EX1030, 2. It was also demonstrated that pFinFETs having SiGe channels would be “viable candidates for future **high-speed applications** due to its excellent drive current performance [and other benefits].” EX1031, 1.

28. It was also known pFinFETs using SiGe fins, compared to Si fins, allow for lower power consumption and exhibit improved reliability associated with negative bias temperature instability (NBTI), which was “a major reliability problem

for the semiconductor industry.” EX1006, [0021], [0043]; EX1016, 1; EX1034, 1. Furthermore, hole mobility in SiGe was known to be approximately twice of that in Si and thus SiGe pFinFETs are faster than Si counterparts. EX1017, 1.

29. As I explained below, it was well-known that nFinFETs used Si fins and pFinFETs used SiGe fins.

C. FinFET-Based Integrated Circuits (ICs)

30. At the relevant time, FinFETs had widespread commercial use, including static random access memory (SRAM). *See generally* EX1027; EX1028, 5, 8, 10-12, 16, 24; EX1029, 2, 5-10, 14, 22-23, 27. Since the early days of planar transistors and to date, SRAM has become and remains the most popular storage solution and is incorporated in nearly all IC chips (e.g., microprocessors, etc.). EX1008, 1:20-26. A SRAM cell commonly contains multiple transistors and it would have been a routine practice to adjust/optimize the SRAM/transistor and their layout to meet performance and area requirements. After FinFETs were introduced, SRAM has been implemented using FinFETs. One reason was the 3D geometry of the fins may be scaled by, e.g., increasing the fin height, which allows for increasing “drive currents of FinFETs...without incurring the penalty of chip area.” EX1010, [0004]; EX1035, 1 (“[t]he fin height is...a powerful knob to improve the layout

density in FinFET cells”). Additionally, it was known to use certain implantation method to “produce high-density SRAM cells,” “permit[ting] reduction of SRAM cell size by approximately 40-50%.” EX1009, 1:40-42.

31. It was well-known the dimensions of the FinFETs in an SRAM cell impact SRAM cell’s performance. For example, static noise margin of an SRAM cell (quantifying amount of noise an SRAM cell can tolerate/withstand before affecting its stored data) depends on parameters involving **the channel width and channel length of the transistors** in the SRAM cell (EX1033, 1), where the channel width is a function of the **fin height**. The size of the transistors in an SRAM cell also impacts the **speed of SRAM**. Thus, a person of ordinary skill in the art would have adjusted, including determining optimal and/or workable ranges of the **fin height** to achieve certain SRAM performance parameters.

VI. THE ’292 PATENT

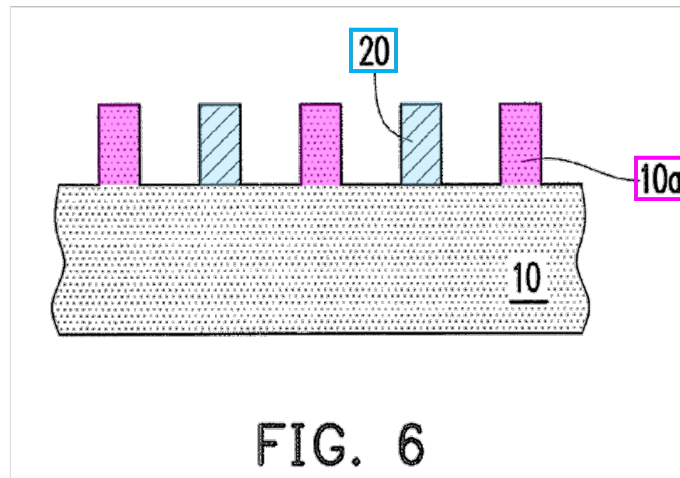
A. Description

32. The ’292 patent relates to fabricating a semiconductor fin structure for forming FinFETs. EX1001, 1:16-19. According to the ’292 patent’s described prior art issues, “the density of the fin patterns of the FinFET array is quite high..., so that the pattern development is difficult and an accurate pattern transfer is impossible,” the ’292 patent proposes a fin structure fabricated by a multi-stage process, alleging

that “since the odd fins are formed prior to the even fins, the pattern density is greatly lowered...so that the development of fin patterns is much easier,” and “the even fins can be different from the odd fins in...one of the height, the width and the material.” *Id.*, 2:16-27.

33. Figure 6 depicts a fin structure having semiconductor substrate 10 with **odd** fins 10a. EX1001, Abstract; 3:50-60. **Even** fins 20 are also formed on substrate 10 and between **odd** fins 10a. *Id.* Each of **even** fins 20 is located between two **odd** fins 10a, forming an **odd-even-odd-even-odd** pattern. *Id.*, 1:67-2:12. Notably, Fig. 6 shows the arrangement of a single **odd** fin alternating with a single **even** fin, i.e., **odd-even-odd-even-odd** fin arrangement. The semiconductor substrate 10 and **odd** fins 10a are formed of semiconductor material, e.g., silicon. *Id.*, 2:48-50. Because they are formed separately, **even** fins 20 differ from **odd** fins 10a in materials, fins widths, or fin heights. *Id.*, 3:35-49, 3:53-60.

34. The '292 patent also describes that the second/even fins 20 may be separately formed by epitaxially grown material, and may differ in height from the first/odd fins 10a. *Id.*, 3:39-41, 46-49, 57-60.



EX1001, FIG. 6 (annotated).

35. As I discuss below, the challenged claims are simply a compilation of conventional components/features disclosed/suggested by the prior art combinations discussed herein.

VII. OVERVIEW OF THE PRIOR ART

A. Inaba (EX1005)

36. U.S. Patent Application Publication No. 2008/0308848 (“Inaba”) was published December 18, 2008, from an application filed May 12, 2008. EX1005, Cover. Inaba explains in the Abstract that,

A semiconductor device according to an aspect of the invention comprises an **n-type FinFET** which is **provided on a semiconductor substrate and which includes a first fin**, a first gate electrode crossing a

channel region of the first fin via a gate insulating film in three dimensions, and contact regions provided at both end of the first fin, a **p-type FinFET which is provided on the semiconductor substrate and which includes a second fin**, a second gate electrode crossing a channel region of the second fin via a gate insulating film in three dimensions, and contact regions provided at both end of the second fin, wherein the n- and the p-type FinFET constitute an inverter circuit, and the **fin width of the contact region of the p-type FinFET is greater than the fin width of the channel region of the n-type FinFET**.

EX1005, Abstract.

37. Inaba is in the same field (FinFET devices) as the '292 patent and pertinent to a problem the '292 Patent seeks to address (FinFET devices fabrication).

EX1001, 1:15-35; EX1005, Abstract.

B. Basker (EX1006)

38. U.S. Patent Application Publication No. 2011/0108920 ("Basker") was published May 12, 2011, from an application filed November 9, 2009. EX1006, Cover. Basker explains in the Abstract that,

A device and method for fabrication of fin devices for an integrated circuit includes forming **fin structures in a**

semiconductor material of a semiconductor device wherein the semiconductor material is exposed on sidewalls of the fin structures. **A donor material is epitaxially deposited on the exposed sidewalls of the fin structures.** A condensation process is applied to **move the donor material through the sidewalls into the semiconductor material such that accommodation of the donor material causes a strain in the semiconductor material of the fin structures.** The donor material is removed, and a field effect transistor is formed from the fin structure.

EX1006, Abstract.

39. Basker is in the same field (FinFET devices) as the '292 patent and pertinent to a problem the '292 Patent seeks to address (FinFET devices fabrication). EX1001, 1:15-35; EX1006, Abstract, [0004].

C. Liaw (EX1008)

40. U.S. Patent No. 8,942,030 ("Liaw") was patented January 27, 2015, from an application filed June 25, 2010. EX1008, Cover. Liaw explains in the Abstract that,

The present disclosure provides **a static random access memory (SRAM) cell.** The SRAM cell includes a first

and a second pull-up devices; a first and a second pull-down devices configured with the first and second pull-up devices to form two cross-coupled inverters for data storage; and a first and second pass-gate devices configured with the two cross-coupled inverters to form a port for data access, wherein the first and second pull-down devices each includes a first channel doping feature of a first doping concentration, and the first and second pass-gate devices each includes a second channel doping feature of a second doping concentration greater than the first doping concentration.

EX1008, Abstract.

41. Liaw is in the same field (FinFET devices) as the '292 Patent and pertinent to a problem the '292 Patent seeks to address (FinFET devices fabrication). EX1001, 1:15-35; EX1008, 1:49-2:24.

D. Hill (EX1009)

42. U.S. Patent No. 7,297,581 ("Hill") was patented November 20, 2007, from an application filed May 17, 2005. EX1009, Cover. Hill explains in the Abstract that,

A method of doping fins of a semiconductor device that includes a substrate includes forming multiple fin

structures on the substrate, each of the fin structures including a cap formed on a fin. **The method further includes performing a first tilt angle implant process to dope a first pair of the multiple fin structures with n-type impurities and performing a second tilt angle implant process to dope a second pair of the multiple fin structures with p-type impurities.**

EX1009, Abstract.

43. Hill is in the same field (FinFET devices) as the '292 Patent and pertinent to a problem the '292 Patent seeks to address (FinFET devices fabrication). EX1001, 1:15-35; EX1009, Abstract.

E. Yu (EX1010)

44. U.S. Patent Application Publication No. 2008/0230852 ("Yu") was published September 25, 2008, from an application filed March 6, 2007. EX1010, Cover. Yu explains in the Abstract that,

A semiconductor structure includes a first semiconductor strip extending from a top surface of the semiconductor substrate into the semiconductor substrate, wherein **the first semiconductor strip has a first height.** A first insulating region is formed in the semiconductor substrate and surrounding a bottom portion of the first

semiconductor strip, wherein the first insulating region has a first top surface lower than a top surface of the first semiconductor strip. A second semiconductor strip extends from a top surface of the semiconductor substrate into the semiconductor substrate, wherein **the second semiconductor strip has a second height greater than the first height**. A second insulating region is formed in the semiconductor substrate and surrounding a bottom portion of the second semiconductor strip, wherein the second insulating region has a second top surface lower than the first top surface, and wherein the first and the second insulating regions have substantially same thicknesses.

EX1010, Abstract.

45. Yu is in the same field (FinFET devices) as the '292 Patent and pertinent to a problem the '292 Patent seeks to address (FinFET devices fabrication). EX1001, 1:15-35; EX1010, [0001], FIG. 9.

VIII. CLAIM CONSTRUCTION

46. I understand that when considering the meaning of patent claims, one must consider the language of the claims, the specification, and the prosecution history of the patent. I also understand that claim terms are typically given their ordinary and customary meanings as would have been understood by a person of

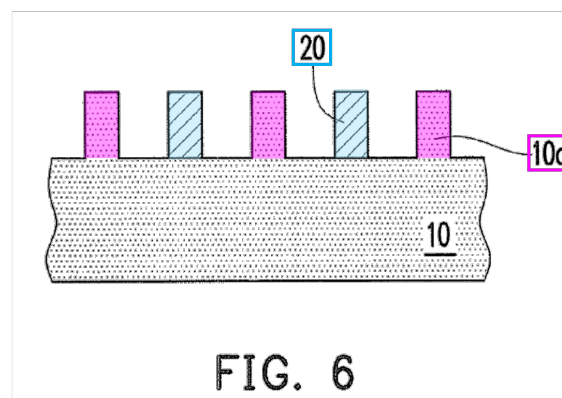
ordinary skill in the art ordinary skill in the art at the time of the invention for the patent.

47. For the '292 patent, as I explained above in Section IV, the relevant time that I have been asked to consider is around February 9, 2012.

48. For purposes of my opinions in this declaration, I have been asked to consider the challenged claims under the plain and ordinary meaning of the claim terms **except for the terms associated with the arrangement of “odd [or first]” and “even [or second]” fins (claims 1/9/15)**, which I was asked to address **(1)** under the plain and ordinary of the terms consistent with the '292 patent specification (discussed below in **Sections IX.A-IX.B**); and **(2)** under certain assumptions concerning the arrangement of the even/odd and first/second fins (discussed below in **Sections IX.C-IX.G**).

49. **With respect to (1)**, the '292 patent describes with respect to Figure 6 a structure including “**odd** fins 10a and **even** fins 20 that are arranged *alternately*.” EX1001, 3:53-56. Consistent with the figure, the specification describes an arrangement of a **single odd fin alternating with a single even fin**, i.e., **odd-even-odd-even-odd** fins, which is **the only fin arrangement** disclosed by the specification. *See* EX1001. As discussed above, I have been asked to consider the

challenged claims under their plain and ordinary meanings consistent with the '292 patent specification, including the entirety of the specification and what I have described above regarding the description associated with Figure 6, and I have applied such understandings in my analysis of the '292 patent and the prior art, as discussed below in **Sections IX.A-IX.B.**



EX1001, Figure 6 (annotated)

50. **With respect to (2)**, I have been asked to consider how the prior art meets certain claim limitations based on **certain assumptions regarding the arrangement of the even/odd and first/second fins.**

51. In particular, I was asked to assume that a structure including an arrangement of **two NMOS fins, two PMOS fins, and two NMOS fins, i.e., an arrangement of N-N-P-P-N-N fins**, meets limitations associated with the arrangement of the “odd” or “first” fins and “even” or “second” fins recited in the

'292 patent claims. Also, I was asked to assume **each pair of NMOS fins** corresponds to “a plurality of **odd [or first]** fins” and **the pair of PMOS fins** corresponds to “a plurality of **even [or second]** fins.” I have applied **such assumptions** in my analysis of the '292 patent and the prior art, as discussed below in **Sections IX.C-IX.G**.

IX. THE PRIOR ART DISCLOSES AND/OR SUGGESTS ALL RECITED FEATURES OF CLAIMS 1-20 OF THE '292 PATENT

52. In my opinion, the prior art discussed below discloses and/or suggests the limitations of claims 1-20.²

A. Basker in View of Hill Discloses and/or Suggests Claims 1, 3-9, 11-15, and 17-20

1. Claims 1, 9, and 15

- (i) [1.pre]/[9.Pre] “A semiconductor structure for forming FinFETs, comprising”

² In this section (Section IX), I refer to exhibits other than those identified prior art reference(s) that disclose and/or suggest the claimed limitations. Such exhibits reflect the state of the art known to a person of ordinary skill in the art at the time of the alleged invention.

[15.Pre] “A semiconductor structure for forming FinFET, comprising”

53. I understand that these features are preambles of claims 1, 9, and 15. I have been asked to assume that these preambles are limiting. Under that assumption, Basker discloses these limitations. Basker discloses FinFET structures for use in ICs. EX1006, Abstract (“A device and method for fabrication of **fin devices for an integrated circuit** [that] includes forming fin structures in a semiconductor material of a semiconductor device”), [0005]-[0007], [0020], [0029]. The fin structures in Basker are used for the formation of n-type FET (nFinFET) and p-type FET (pFinFET). *Id.*, [0020] (“In one example, the substrate includes silicon which is employed to form the fin for the nFET. In this example, a fin for the pFET includes silicon as well, but Germanium (Ge) is pushed into silicon to form a SiGe fin for the formation of the pFET”).

54. Specifically, Basker discloses the use of **Si fins** for **nFinFETs** and **SiGe fins** for **pFinFETs** to improve the pFinFETs’ performance. *Id.*, [0020]-[0021].

The device and method provide a p-type field effect transistor (pFET) within a target threshold voltage. **An n-type field effect transistor (nFET) is formed on a fin made from a substrate material. A corresponding**

pFET is formed on a fin which is processed by **pushing or diffusing an element into the substrate material** to form a new structure. In one example, the substrate includes silicon which is employed to form the fin for the nFET. In this example, **a fin for the pFET includes silicon as well, but Germanium (Ge) is pushed into silicon to form a SiGe fin for the formation of the pFET.** The pFET is formed by, e.g., oxidation condensation (to push Ge into a Si fin during oxidation).

Id., [0020].

In this way, the **pFET finFET with a SiGe body** achieves a corrected threshold voltage (V_t) since the dimensions of the fin are maintained and an advantageous strain is imparted to the fin. The SiGe and associated strain results from the Ge within a silicon matrix. The strain **improves pFET performance** because intermixing Ge into Si requires strain relaxation to open up the spaces in the silicon for larger Ge atoms. This is much easier to do in a direction normal to a carrier transport direction. This is an ideal combination: comparable V_t , strain, and a (110) surface for the pFET finFET. **In fact in many useful integrated circuit components, such as logic gates and in particular NAND gates, the pFET can be made to especially gain from these advantageous effects.**

Id., [0021].

55. Basker explains that the SiGe fins are formed by incorporating epitaxially-deposited material into the fins for pFinFETs. *Id.*, [0005], [0031]-[0032], [0041], claim 1. EX1013, 2 (“the solid phase epitaxy growth of SiGe by Ge condensation”).

56. Figure 8 of Basker shows the formation of a CMOS device 48 that includes nFinFET 44 and pFinFET 46 by etching a top layer of substrate 10 (*see* Figure 1) comprising a silicon layer 16 to form Si fins (20, 22) using a patterning process, as shown in Figure 2. EX1006, [0025], [0026].

Dielectric liner 18 may include a dielectric material that enable selective etching of underlying materials (e.g., layer 16). In one embodiment, layer 16 is monocrystalline silicon and liner 18 may include silicon nitride (nitride).

Liner 18 is deposited over the substrate 10.

Id., [0026]; *see also* [0027] (“a lithographic patterning process, which may include steps for forming sub-minimum feature sized fins 20 and 22”), [0034] (“a CMOS device 48 includes an nFET 44 and a pFET 46. The nFET includes fin 20 ... the pFET 46 includes fin 22”); [0034].

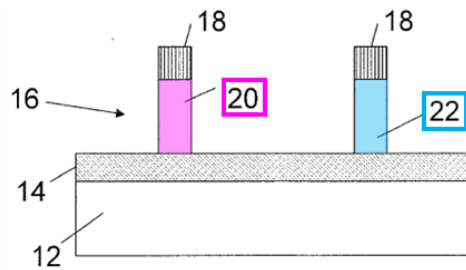


FIG. 2

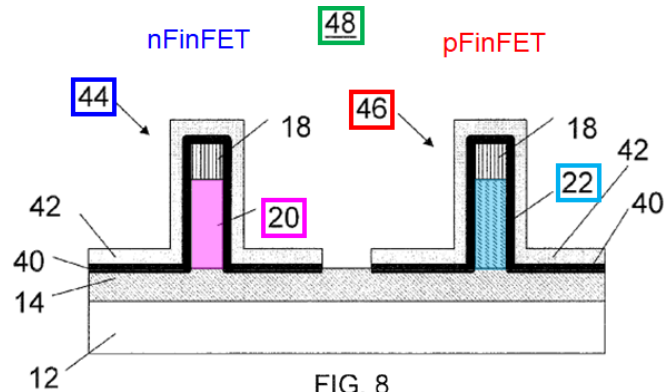


FIG. 8

EX1006, FIG. 2 (annotated) and FIG. 8 (annotated). While substrate 10 in Figure 2 shows a SOI substrate, Basker discloses substrate 10 may be bulk monocrystalline silicon. EX1006, [0025] (“substrate 10 can be...**bulk substrate that may include...monocrystalline silicon**”).

57. Referring to Figure 2 above, the Si fin 20 is then used to form the nFinFET, while the fin for pFinFET is made by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22, resulting in a SiGe fin for the pFinFET. EX1006, [0005], [0030], [0031] (“a donor layer 28 is epitaxially deposited on sidewall surfaces of fin 22...donor layer 28 includes Silicon-Germanium (SiGe). In other embodiments, donor layer 28 may include pure Ge, Ge mixed with other elements or compounds,” [0032], [0033], [0041], claim 1.

A device and method for fabrication of fin devices for an integrated circuit includes forming fin structures in a semiconductor material of a semiconductor device

wherein the semiconductor material is exposed on sidewalls of the fin structures. **A donor material is epitaxially deposited on the exposed sidewalls of the fin structures.** A condensation process is applied to **move the donor material through the sidewalls into the semiconductor material** such that accommodation of the donor material causes a strain in the **semiconductor material of the fin structures.** The donor material is removed, and a field effect transistor is formed from the fin structure.

Id., [0005]. Standard FinFET processing is then used to form nFinFETs using Si fin 20 and pFinFETs using SiGe fin 22. *Id.*

58. Accordingly, Basker discloses a “semiconductor structure” (e.g., Figure 8) “for forming FinFETs” (preambles [1.pre]/[9.pre]) or “FinFET” ([15.pre]). See Section VII.B above, and my discussion below in Sections IX.A.1(ii)-(iv).

(ii) **[1.a]/[9.a]/[15.a] “a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;”**

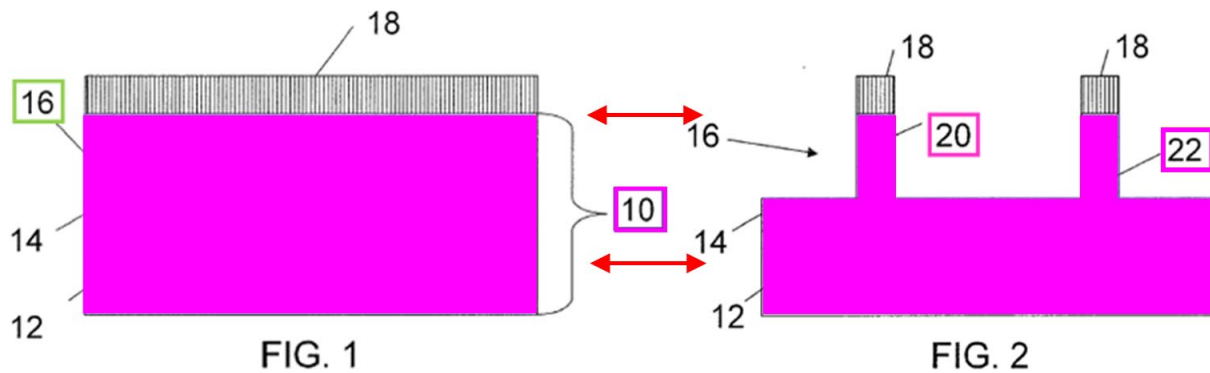
59. In my opinion, Basker discloses these limitations. As discussed for the preambles, Basker’s substrate 10 may be a bulk monocrystalline silicon substrate (“semiconductor substrate” as claimed). EX1006, [0025] (“substrate 10 can be...bulk substrate that may include...monocrystalline silicon”).

60. Figures 1 and 2 illustrate substrate 10 as a bulk monocrystalline silicon substrate (pink), where the entire substrate is made of silicon (“a semiconductor material”), including “a top portion of the semiconductor substrate” (e.g. between the red arrows).³ Basker discloses etching the monocrystalline silicon layer 16, which is a part of a “top portion” of a substrate 10 to form Si fins 20, 22 (FIG. 2). EX1005, [0025].

It should be understood that the substrate 10 may include any suitable material and is not limited to SOI. For example, **substrate 10 can be an SOI or bulk substrate that may include** Gallium Arsenide, **monocrystalline silicon**, Germanium, or any other material or combination of materials where the present principles may be applied. In some embodiments, the substrate 10 further comprises other features or structures that are formed on or in the semiconductor substrate in previous process steps.

³ Figures 1 and 2 are modified/colored in solid pink color to represent the embodiment where Basker’s substrate 10 is a bulk monocrystalline silicon substrate as expressly disclosed by Basker.

Id., [0025]; *see also* [0026]-[0029] (disclosing “Once the liner 18 is patterned, an etch process, such as, e.g., a reactive ion etch may be employed to remove a portion of layer 16”).



EX1006, FIG. 1 (left annotated) and FIG. 2 (right annotated).

(iii) [1.b] “a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material”

[9.b] “a plurality of odd fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other”

[15.b] “a plurality of first fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and”

61. It is my opinion that Basker, in view of Hill, discloses and/or suggests these limitations. Continuing my explanation in Section IX.A.1.(i), Basker discloses etching silicon substrate 10 (comprising “semiconductor material”) to form Si fin 20 for nFinFET (EX1006, [0025] (“substrate 10 can be...bulk substrate that may include...monocrystalline silicon”), [0030]-[0034]) and an additional process for forming SiGe fin 22 for pFinFET. *Id.*

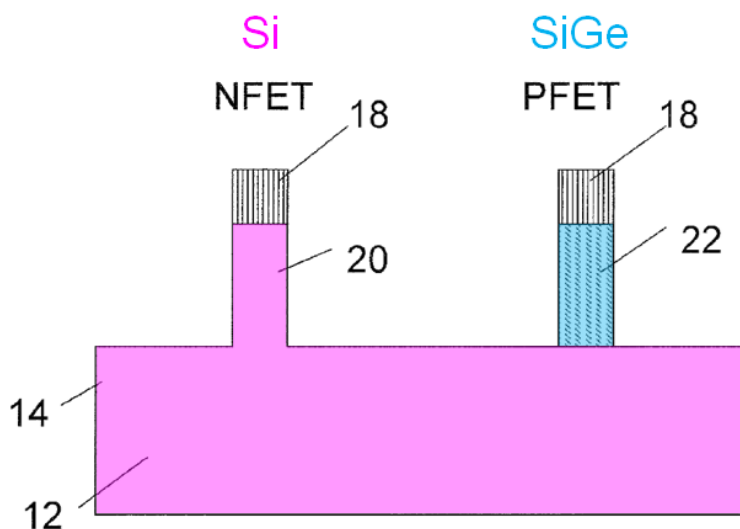


FIG. 7

EX1006, FIG. 8 (annotated). Additionally, because fin 20 is defined by a “lithographic patterning process” (EX1006, [0027]-[0028]), fin 20 is “defined from the semiconductor substrate” (limitation [1.b]) and, per my discussions above, “formed of the semiconductor material,” (limitations [9.b]/[15.b]). *See also* my discussions for limitations [1.a]/[9.a]/[15.a] in Section IX.A.1(ii). Additionally,

since Si fin 20 is formed by etching the top portion of bulk substrate 10, fin 20 (the remaining/non-etched portion of the substrate) is “in direct contact with each other” as fin 20 and substrate 10 were in unity before etching. EX1006, [0027]-[0028].

62. Basker explains that its FinFETs are for use in an IC and “[t]he circuit as described herein may be part of a design for an [IC] chip.” EX1006, [0005] (“[a] device and method for fabrication of fin devices for an integrated circuit includes forming fin structures in a semiconductor material of a semiconductor device”), [0023]-[0024].

The circuit as described herein may be part of a design for an integrated circuit chip. The chip design may be created in a graphical computer programming language, and stored in a computer storage medium (such as a disk, tape, physical hard drive, or virtual hard drive such as in a storage access network). If the designer does not fabricate chips or the photolithographic masks used to fabricate chips, the designer may transmit the resulting design by physical means (e.g., by providing a copy of the storage medium storing the design) or electronically (e.g., through the Internet) to such entities, directly or indirectly. The stored design is then converted into the appropriate format (e.g., GDSII) for the fabrication of photolithographic masks, which typically include multiple copies of the chip

design in question that are to be formed on a wafer. The photolithographic masks are utilized to define areas of the wafer (and/or the layers thereon) to be etched or otherwise processed.

Id., [0023].

The method as described herein may be used in the fabrication of integrated circuit chips. The resulting **integrated circuit chips** can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes **integrated circuit chips**, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

Id., [0024].

63. Thus, Basker does not limit its application of FinFETs to any particular IC. At the relevant time, a person of ordinary skill in the art would have understood that ICs ranged from simple combinations of logic gates to complicated circuits (e.g. microprocessors) and that SRAM circuits were prevalent and were known to be found in many electronic products (e.g., a standalone chip or part of a larger/complicated IC or CPU). Given SRAM's prevalence, a person of ordinary skill in the art, in view of Basker's guidance, would have been motivated to use FinFETs (e.g. those of Basker) to implement SRAM circuits.

64. Hill discloses implementations of SRAM circuit **using FinFETs** that reduces SRAM cell area by 40-50%.

Implementations consistent with the principles of the invention use shadow implanting of **tightly spaced FinFET devices** to produce high-density SRAM cells. Utilization of shadowed N/P implants **permits reduction of SRAM cell size by approximately 40-50%**.

EX1009, 1:40-46.

65. Hill discloses fabricating fin structures by angle implantation for ICs using FinFETs, resulting in devices with an n-p-n-p fin pattern. EX1009, 1:13-16;

1:40-42 (“Implementations consistent with the principles of the invention use shadow implanting of tightly spaced FinFET devices to produce high-density SRAM cells.”); 1:46-47 (“a method of doping fins of a semiconductor device that includes a substrate is provided”); 2:42-52 (“substrate 110 and layer 120 may include other semiconductor materials, such as germanium, or combinations of semiconductor materials”). See also Section VII.D above.

66. Also similar to Basker, Hill specifically discloses the formation of fins on a substrate for use in FinFETs. *Id.*, 1:47-48 (“The method may include forming multiple fin structures on the substrate”). Thus, a person of ordinary skill in the art would have been motivated to consider Hill’s teaching when implementing semiconductor devices similar to those of Basker.

67. Hill’s implantation method to form “tightly spaced FinFET devices to produce high-density SRAM cells” and “permits reduction of SRAM cell size by approximately 40-50%.” EX1009, 1:40-44. Hill dopes a first pair of fins with **n-type** impurities using one tilt angle implant, and dopes a second pair of fins with **p-type** impurities using another tilt angle implant.

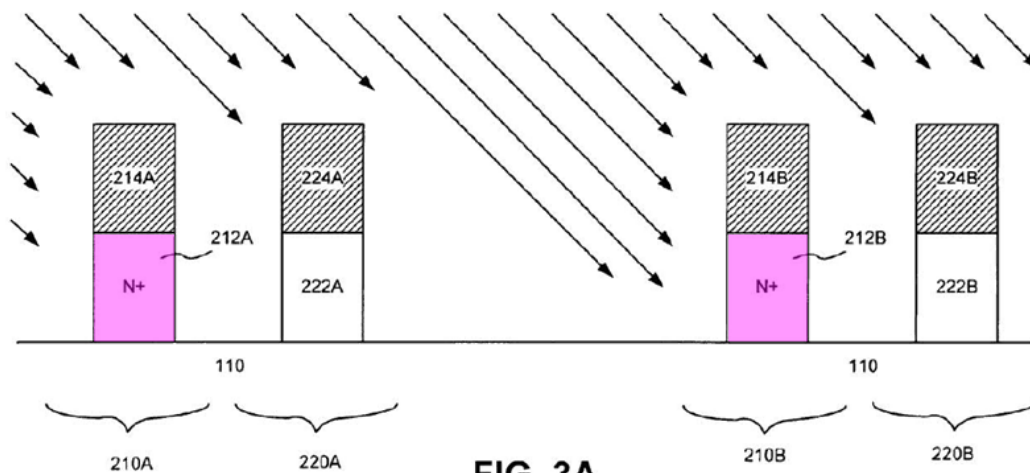
The method may further include performing a first tilt angle implant process to dope a first pair of the multiple fin structures with n-type impurities and performing a

second tilt angle implant process to dope a second pair of the multiple fin structures with p-type impurities.

Id., 1:51-54.

68. Hill does not limit which portion(s) of the FinFETs may be implanted and a person of ordinary skill in the art would have understood such implantations may be used for doping source/drain of a FinFET. *See, e.g.*, EX1024 (disclosing implantation used for doping the source/drain of FinFETs). A person of ordinary skill in the art would have also understood that such implantations were known to be used for doping other part(s) of the FinFET.

69. Figure 3A shows fins 212A, 212B, 222A, 222B, where each fin has a cap 214A, 214B, 224A, 224B.



EX1009, FIG. 3A (annotated).

Silicon layer 120 may then be etched using well-known etching techniques to form multiple fin structures 210A, 210B, 220A and 220B, as illustrated in FIG. 2A. FIG. 2B shows a three dimensional view of FIG. 2A. As shown in FIGS. 2A and 2B, fin structure 210A/220A includes a fin 212A/222A and a cap 214A/224A and fin structure 210B/220B includes a fin 212B/222B and a cap 214B/224B. Caps 214A/224A may remain covering fin 212A/222A and caps 214B/224B may remain covering fin 212B/222B.

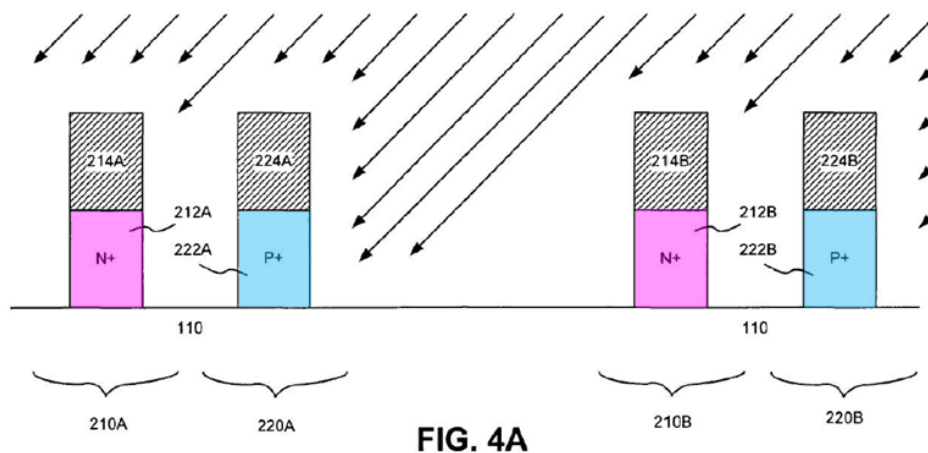
Id., 3:5-14. The height of the cap and the pitch between each fin structure are selected such that n-type impurities using a first tilt angle are implanted into fins 212A/212B (pink) while fins 222A/222B remain undoped (white) because fins 212A/212B and caps 214A/214B shield fins 222A/222B from n-type impurities.

As shown in FIGS. 3A and 3B, the implanting of n-type impurities does not dope fins 222A and 222B. There are several factors that aid in preventing the n-type impurities from reaching fins 222A and 222B. For example, the presence, height, and closeness of fin structure 210 shields or shadows fin 222, thereby blocking the n-type impurities from reaching fin 222. The presence of cap 224 also helps block the n-type impurities.

Id., 3:51-58. Subsequently, as shown in Figure 4A, p-type impurities using a second tilt angle are implanted into fins 222A/222B (blue) while n-type fins 212A/212B (pink) are shielded from p-type impurities by fins 222A/222B (blue) and caps 224A/224B.

As shown in FIGS. 4A and 4B, the implanting of p-type impurities does not dope fins 212A and 212B. There are several factors that aid in preventing the p-type impurities from reaching fins 212A and 212B. For example, the presence, height, and closeness of fin structure 220 shields or shadows fin 212 blocks the p-type impurities from reaching fin 212. The presence of cap 224 also helps block the p-type impurities.

EX1009, 4:11-18.



Id., FIG. 4A (annotated).

70. Hill's method results in closely spaced fins having a pattern of a fin with n-type impurities ("n-fin") fin 212A, a fin with p-type impurities ("p-fin") fin 222A, n-fin 212B, and p-fin 222B, i.e., an n-p-n-p-fin pattern. "Conventional processing may then be performed" on the fins to complete the FinFET-based SRAM device. *Id.*, 5:29-35 ("Conventional processing may then be performed to complete the...FinFET SRAM device...").

71. Considering the above disclosures, a person of ordinary skill in the art would have considered Hill's teachings when implementing SRAM circuits using FinFETs discussed in Basker.

72. As discussed below, the exemplary Basker-Hill combination discloses and/or suggests "a plurality of **odd** [or **first**] fins of the FinFETs..." (limitations [1.b]/[9.b]/[15.b]), "a plurality of **even** fins of the FinFETs...between the **odd** fins of the FinFETs, being **different** from the **odd** fins of the FinFETs in at least one of width and **material**" (limitations [1.c]/[9.c]), and "a plurality of **second** fins of the FinFETs..., each of the **second** fins of the FinFETs is located between two **first** fins of the FinFETs, and the **second** fins of the FinFETs are **different** from the **first** fins of the FinFETs in at least one of width and **material**" (limitation [15.c]).

73. Per my discussion above, a person of ordinary skill in the art would have been motivated and found it beneficial to combine Basker (e.g., use of Si nFinFETs and SiGe pFinFETs) and Hill (e.g., use of shadow implantation for producing high-density FinFET-based SRAM) to form a high-density FinFET-based SRAM using Si nFinFETs and SiGe pFinFETs.

74. **First**, Hill's implantation method produces "**tightly spaced FinFET devices** to produce **high-density SRAM cells**," which "permits **reduction of SRAM cell size** by approximately 40-50%." EX1009, 1:40-44. These features are beneficial because SRAM devices having reduced size would have allowed space for including/building other electronic components/features. EX1036, 1 ("As memory will continue to consume a large fraction of many future designs, scaling of memory density must continue to track the scaling trends of logic."). Additionally, high-density SRAM cells (e.g. having tightly-packed transistors/FinFETs/cells) would have increased the amount of data storage. EX1037, [0005] ("In recent years, the size of transistors including memory cells is reduced in order to **enhance the integration density** of a semiconductor memory device."). Thus, a person of ordinary skill in the art when implementing FinFET-

based IC devices as discussed in Basker would have been motivated to combine Hill's teaching.

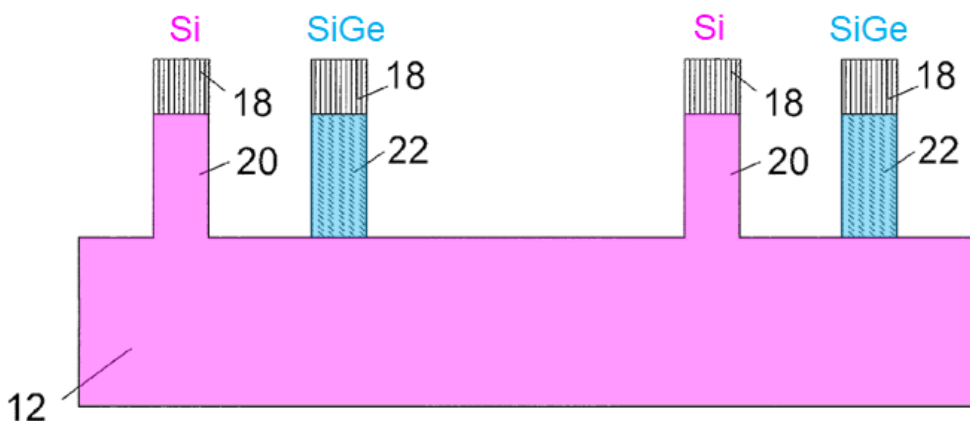
75. **Second**, implementing SiGe fins in pFinFETs (e.g., as in Basker) for an SRAM cell would have been beneficial. SRAM devices known to be used in various electronic devices to provide high-speed data storage/access. See my discussions in Sections V.B-C. As I have discussed in Section V.B (benefits of using SiGe fins for pFinFETs), a person of ordinary skill in the art would have recognized the trend toward the use of SiGe fins for pFinFETs and the associated benefits for instance, improve hole mobility and NBTI reliability. EX1016, 1, 2 (“the introduction of **Ge in the channel dramatically improved** the NBTI **reliability**”), 4; EX1017, 1 (“...SiGe (<40% Ge) is an attractive channel material beyond Si due to its **high carrier mobility** ($\sim 2\times$ Si) and compatibility to the conventional CMOS processes”); EX1018, 1 (“...**high mobility pMOSFETs** on high quality epitaxial SiGe films selectively grown on Si (100) substrates...The **mobility enhancement** afforded intrinsically by the SiGe channel (60%) is further increased by a Si cap (40%) process, resulting in a combined $\sim 100\%$ enhancement over Si channels”); EX1025, 1; EX1026, 1.

76. **Third**, Basker allows use of “the same gate dielectric...and the same gate conductor...” for both the nFinFET(s) and pFinFET(s) (EX1006, [0038]), which would have simplified the fabrication processes and reduced cost for making ICs/SRAM. EX1023, [0008] (“fabricating transistors having gate electrodes made of **two different materials is prohibitively expensive**”), [0016] (“[a] **single metal gate stack**, used for both pMOS and nMOS transistors, **simplifies fabrication**”), [0027] (“**fabrication can be greatly simplified** because there is no need for the pMOS device to have a gate metal with a different work function than that of the nMOS device”).

77. In my opinion, a person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the Basker-Hill combination. Basker itself discloses that the use of SiGe fins in pFinFETs results in “**an ideal combination**” of **beneficial features**. EX1006, [0021]. Additionally, Basker’s features may be applied to many useful IC components, which, as a person of ordinary skill in the art would have understood, include SRAM. *Id.*, [0021]. The combination of Basker and Hill would have involved application of known technologies (e.g., known use of Si nFinFETs and SiGe pFinFETs) according to known methods (e.g., known implantation method to

form high-density FinFET-based SRAM cell) to yield the predictable result of high-density SRAM cells.

78. Based on the collective teachings/suggestions of Basker and Hill (See Sections VII.B, VII.D above), a person of ordinary skill in the art would have been motivated to configure the above discussed FinFET structure of Basker (where the nFinFETs include **Si fins** and pFinFETs include **SiGe fins**) to form FinFET-based SRAM cells of high density and reduced footprint (as discussed in Hill). In one non-limiting example, a person of ordinary skill in the art would have been motivated to configure the FinFET structure to form an exemplary SRAM cell having features shown in Figure 7* (modified based on Figure 7 of Basker), i.e., an arrangement of n-/p-/n-/p-fins, where the n-fin (e.g., with n-type S/D implantation for nFinFET) includes Si and the p-fin (e.g., with p-type S/D implantation for pFinFET) includes SiGe.



EX1006, FIG. 7* (annotated).

79. A person of ordinary skill in the art would have also known that a SRAM cell stores one bit of data and multiple SRAM cells are needed for data storage. Thus, a person of ordinary skill in the art would have been motivated to replicate multiple SRAM cells. EX1037, [0017] (memory cells arranged as an array in rows and columns). Indeed, Hill discloses and/or suggests the SRAM cell is **replicated** across the substrate to form an SRAM device. EX1009, 1:13-16, 1:20-24 (“**ultra large scale integration** semiconductor devices”); 1:40-42 (“Implementations consistent with the principles of the invention use shadow implanting of tightly spaced FinFET devices to produce **high-density SRAM cells**”), 2:39-41 (“high-density SRAM cells”). Additionally, Basker expressly discloses “**multiple copies of the chip design...are to be formed**” on a substrate/wafer. EX1006, [0023] (“multiple copies of the chip design in question that are to be formed on a wafer”).

80. When forming multiple SRAM cells on the substrate in light of Hill’s teaching/suggestions, a person of ordinary skill in the art would have been motivated to configure the **arrangement/order of n-/p-/n-/p-fins** of Basker-Hill SRAM cell (e.g., Figure 7* of Basker) such that the arrangement/order was **replicated for each**

cell because of the nature of Hill's implantation process. For example, in the modified Figures 7*(a)/7*(b) of Basker below, which shows fins of two SRAM cells replicated side-by-side and subject to the shadow implantation process (as in Hill), the **odd-numbered fins** (i.e., 212A/B fins) are **n-fins**, and the **even-numbered fins** (i.e., 222A/B fins) are **p-fins**.

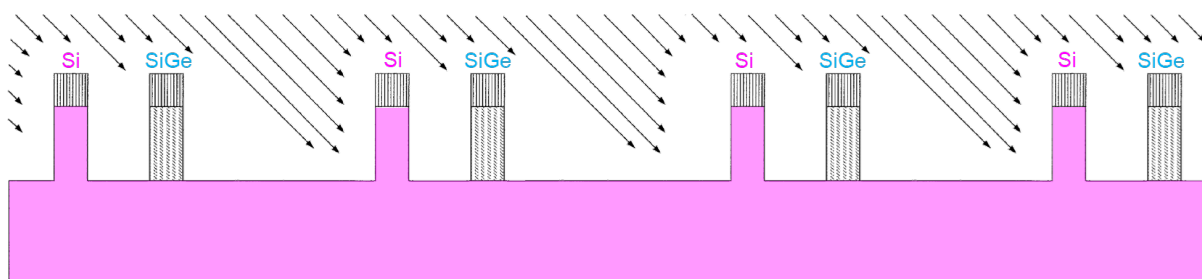


FIG. 7*(a)

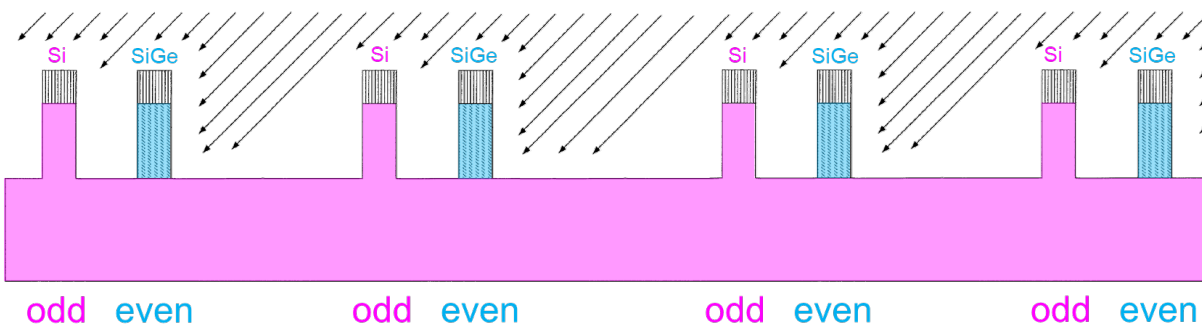


FIG. 7*(b)

81. A person of ordinary skill in the art would have been motivated to orient the **fins of multiple SRAM cells in the same direction** in view of Hill's implantation process, e.g., to avoid inconsistent doping among the fins. Thus, for the reasons stated, a person of ordinary skill in the art would have been motivated to

implement multiple SRAM cells each having an **arrangement/order of n-p-n-p-n-p-n-p-fins** in the Basker-Hill combination.

82. In my opinion, a person of ordinary skill in the art would have had the requisite skill, rationale, and knowledge in implementing the above-discussed Basker-Hill combination. Additionally, such a person would have expected to succeed in implementing the feature. This is particularly true given that Basker states its FinFET structure “may be part of a design for an [IC] chip” (EX1006, [0005], [0023]) and Hill teaches FinFET-based SRAM (EX1009, 1:40-44). A person of ordinary skill in the art would have understood that many SRAM cells may be repeated on the same substrate. EX1037, [0017] (memory cells arranged as an array in rows and columns); EX1040, 3 (“SRAM layout, consisting of the repeated unit cell”).

83. As discussed above, the Basker-Hill combination would have predictably included an arrangement of fins of FinFETs having alternating/different fin material, i.e., **Si fins** for nFinFETs (**odd**-numbered fins) and **SiGe fins** for pFinFETs (**even**-numbered fins), where the **even**-numbered fins reside between the **odd**-numbered fins, as shown in modified Figure 7*(c).

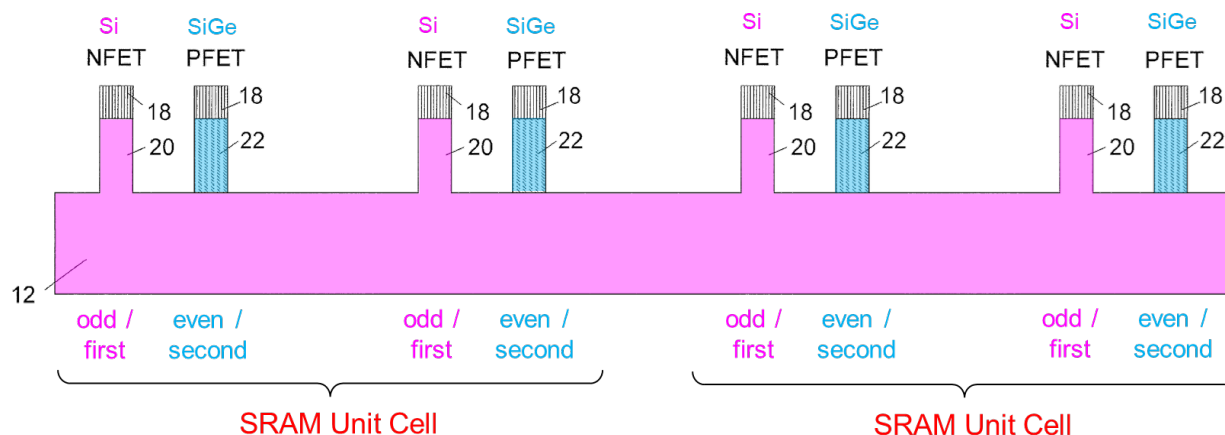


FIG. 7*(c)

84. Similarly, as shown in the modified Figure 7*(c) above, the Basker-Hill combination would have been predictably configured to include an arrangement of fins having alternating/different fin material, i.e., **Si fins** for nFinFETs (“**first**” fins) and **SiGe fins** for pFinFETs (“**second**” fins), where each of the “**second**” fins is located between two “**first**” fins.

85. Accordingly, the Basker-Hill combination discloses and/or suggests “a plurality of **odd** [or **first**] fins of the FinFETs...” (limitations [1.b]/[9.b]/[15.b]), “a plurality of **even** fins of the FinFETs...between the **odd** fins of the FinFETs, being **different** from the **odd** fins of the FinFETs in at least one of width and **material**” (limitations [1.c]/[9.c] discussed further in Section IX.A.1(iv)) and “a plurality of **second** fins of the FinFETs..., each of the **second** fins of the FinFETs is located between two **first** fins of the FinFETs, and the **second** fins of the FinFETs are

different from the **first** fins of the FinFETs in at least one of width and **material**” (limitation [15.c] discussed further in Section IX.A.1(iv)). Additionally, consistent with as discussed above, the Basker-Hill combination discloses and/or suggests “the plurality of **odd** [or **first**] fins and the **semiconductor substrate** are in **direct contact with each other**” as claimed in limitation [9.b]/[15.b].

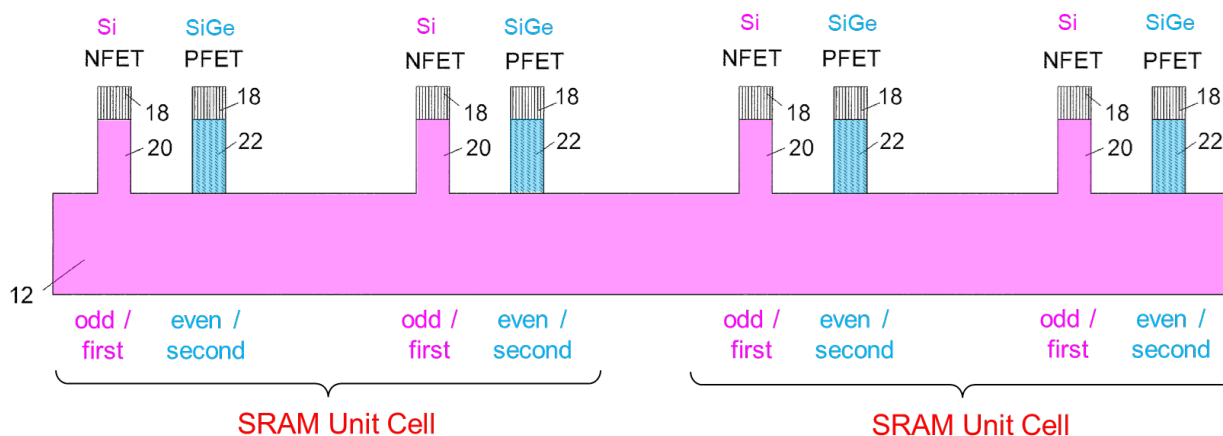
- (iv) [1.c] “a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.”

[9.c] “a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.”

[15.c] “a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.”

86. It is my opinion that the Basker-Hill combination discloses and/or suggests these limitations. The analysis above for limitations [1.b]/[9.b]/[15.b]

demonstrates how the Basker-Hill combination discloses and/or suggests “a plurality of even fins of the FinFETs...between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and **material**” (limitations [1.c]/[9.c]) and “a plurality of second fins of the FinFETs..., each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and **material**” (limitation [15.c]), which is exemplified by the modified Basker Figure 7*(c) (where such features would have been implemented in the Basker-Hill combination as discussed for limitations [1.b]/[9.b]/[15.b]). See Section IX.A.1(iii) above.



87. Per my discussion above in Section IX.A.1(ii) for limitations [1.a]/[9.a]/[15.a], Basker's fins for nFinFETs and pFinFETs are initially formed by etching a silicon substrate such that the fins protrude from the substrate.

88. Also discussed for those limitations, the fins for the pFinFETs are then converted into SiGe fins. Thus, for the reasons I have provided above, the SiGe fins are "in direct contact with the semiconductor material," which is of the top portion of the semiconductor substrate. Such features would have been implemented in the Basker-Hill combination for reasons explained above for limitations [1.b]/[9.b]/[15.b].

89. Accordingly, the Basker-Hill combination discloses and/or suggests limitations [1.c]/[9.c]/[15.c].

2. Claims 3, 11, and 17

(i) 3. "The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material."

11. "The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise an epitaxy material."

17. "The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise an epitaxy material."

90. It is my opinion that the Basker-Hill combination discloses these limitations. Per my discussion above for the preambles and limitations [1.b]/[9.b]/[15.b], Basker's SiGe fins are formed by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22. EX1006, [0005], [0020]-[0021], [0031]-[0032], [0041], claim 1 ("forming **fin structures in a semiconductor material**; **epitaxially** depositing a donor **material**...; applying a condensation process to move the donor **material** through the sidewalls **into the semiconductor material**").

91. It is my opinion that since the resulting SiGe fins incorporate the epitaxially deposited material, the resulting SiGe fins "comprise an epitaxy material." Further, a person of ordinary skill in the art would have understood that Basker's SiGe fin formation results in epitaxy material and thus the resulting SiGe fins "comprise an epitaxy material." *See, e.g.*, EX1013, 2; EX1038, 3-4. Additionally, a person of ordinary skill in the art would have known that SiGe fins could also be formed using, e.g., chemical vapor deposition (CVD) and molecular beam epitaxy (MBE), and would have used any of them. *See, e.g.*, EX1039, 4:23-5:9. Thus, in my opinion, the Basker-Hill combination would have included "[even/second] fins of the FinFETs [that] comprise an epitaxy material."

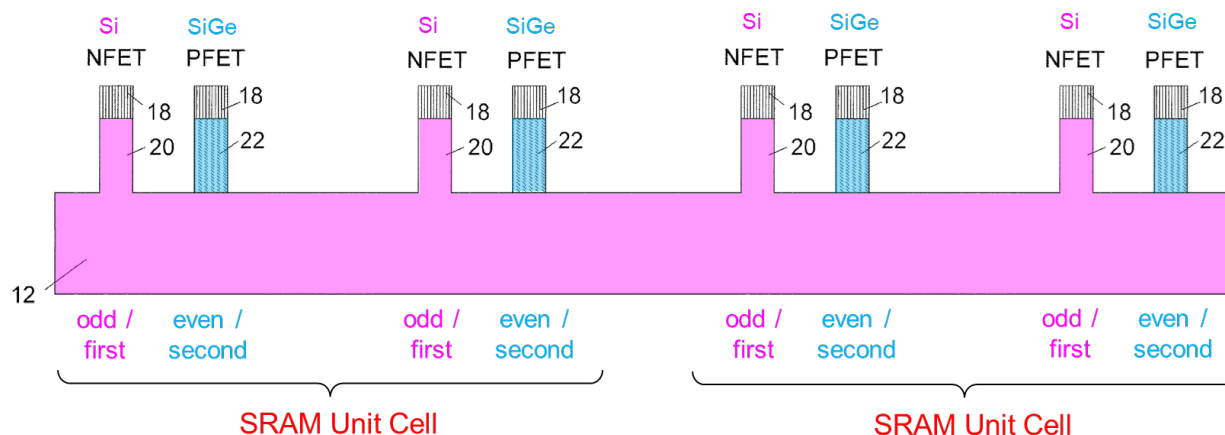


FIG. 7*(c)

3. Claims 4, 12, and 18

(i) 4. “The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.”

12. “The semiconductor structure of claim 11, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.”

18. “The semiconductor structure of claim 17, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.”

92. In my opinion, the Basker-Hill combination discloses and/or suggests these limitations. As I have discussed for limitations [1.b]/[9.b]/[15.b], the Basker-Hill combination discloses “the odd [or first] fins of the FinFETs comprise Si” because the disclosed “the odd [or first] fins” are formed by etching monocrystalline silicon substrate 10. EX1006, [0025]. Further, per my discussion for limitations

[1.b]/[9.b]/[15.b], the Basker-Hill combination discloses forming SiGe fins for pFinFETs (“even [or second] fins of the FinFETs”). See my discussion above in Section IX.A.1.

4. Claims 5, 13, and 19

(i) 5. “The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.”

13. “The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si.”

19. “The semiconductor structure of claim 15, wherein the first fins of the FinFETs comprise Si.”

93. The Basker-Hill combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18.

5. Claims 6, 14, and 20

(i) 6. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.”

14. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise SiC or SiGe.”

20. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise SiC or SiGe.”

94. The Basker-Hill combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18.

6. Claim 7

- (i) **7. “The semiconductor structure of claim 1, wherein the odd fins of the FinFETs are electrically connected to the semiconductor substrate.”**

95. It is my opinion that the Basker-Hill combination discloses and/or suggests this limitation. As discussed for limitations [1.a]/[9.a]/[15.a] and [1.b]/[9.b]/[15.b], the disclosed “odd fins of the FinFETs” are defined from a bulk monocrystalline silicon substrate 10, which would have been implemented in the Basker-Hill combination as discussed above for claim 1. EX1006, [0025] (“substrate 10 can be...[a] **bulk substrate** that may include...**monocrystalline silicon**”). Thus, the disclosed “odd fins of the FinFETs” in the Basker-Hill combination comprise silicon and are connected to the silicon substrate.

96. A person of ordinary skill in the art would have understood that, given the disclosed “odd fins of the FinFETs” and the substrate in the Basker-Hill combination are connected and both are the same semiconductor material, i.e., silicon, these fins and the substrate are electrically connected.

7. Claim 8

- (i) **8. “The semiconductor structure of claim 1, wherein the semiconductor substrate is a single layer structure.”**

97. In my opinion, the Basker-Hill combination discloses and/or suggests this limitation. As I have discussed above for limitations [1.a]/[9.a]/[15.a], substrate 10 (“semiconductor substrate”) in Basker may be bulk monocrystalline silicon substrate (EX1006, [0025]) and thus the entire substrate in the Basker-Hill combination would have been formed of “a single layer structure” of semiconductor material, i.e., silicon.

B. Basker in View of Hill and Yu Discloses and/or Suggests Claims 2, 10, and 16

1. Claims 2, 10, and 16

(i) 2. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.”

10. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.”

16. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.”

98. It is my opinion that the Basker-Hill combination in view of Yu discloses and/or suggests these limitations.

99. Per my discussion above for limitations [1.b]/[9.b]/[15.b], the Basker-Hill combination discloses “odd fins” or “first fins” (Si fins) of the FinFETs, and

“even fins” or “second fins” (SiGe fins) of the FinFETs, which are exemplified in Figure 7*(c) below. See my discussions above in Section IX.A.1.(iii).

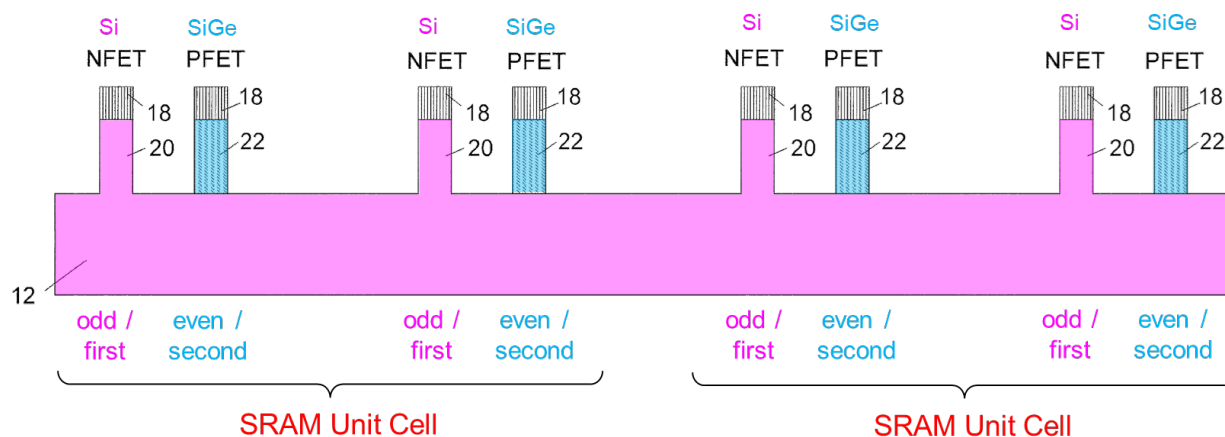


FIG. 7*(c)

100. The Basker-Hill combination does not expressly disclose “the **even** fins...are further different from the **odd** fins...**in height**” or “the **second** fins...are further different from the **first** fins...**in height**.” Nevertheless, a person of ordinary skill in the art would have been motivated to implement such features in the Basker-Hill combination in view of Yu’s teachings.

101. Like Basker, Yu discloses FinFETs for use in ICs and forming fins of the FinFETs by etching a bulk silicon substrate. EX1010, [0001] (“This invention relates generally to semiconductor devices, and more particularly to **Fin field effect transistors (FinFET)**.”), [0002], [0019] (“semiconductor chip”), [0028] (“The embodiments discussed in preceding paragraphs are **formed on bulk**

semiconductor substrate.”), [0020] (“semiconductor substrate 20 includes **silicon**”), [0021]-[0024] (describing with reference to Figures 2-5 that the substrate is etched to form fin structures); see also my discussion above Section VII.E.

An optional pad layer 22 and mask layer 24 are formed on semiconductor substrate 20. Pad layer 22 is preferably a thin film formed through a thermal process, and thus comprising silicon oxide.... Pad layer 22 may also act as an etch stop layer for etching the subsequently formed mask layer 24.

EX1010, [0021].

Photoresist 26 is formed on mask layer 24, and is then patterned, forming openings 28 in photoresist 26.... Width W1 of photoresist strip 30 preferably equals to the desired width of a fin of a FinFET. In an exemplary embodiment, width W1 is between about 15 nm and about 60 nm.

Id., [0022].

In FIG. 3, mask layer 24 and pad layer 22 are etched through openings 28, exposing underlying semiconductor substrate 20. The exposed semiconductor substrate 20 is then etched, forming trenches 32 in semiconductor substrate 20. In an exemplary

embodiment, **depth D1** of trenches 32 is substantially **close to the desired height of the fin** of the desired FinFET. Trenches 32 encircle fin 48 therebetween. Photoresist 26 is then removed.

Id., [0023].

FIG. 4 illustrates the formation and patterning of photoresist 34, which defines the pattern for forming another fin. Openings 36 are formed in photoresist 34 and define photoresist strip 38, which is surrounded by openings 36. **Mask layer 24, pad layer 22 and semiconductor substrate 20 exposed through openings 36 are then etched sequentially, forming trenches 40 in semiconductor substrate 20, as is shown in FIG. 5.** Preferably, **trenches 40 have depth D2 different from depth D1 of trenches 32.** In an exemplary embodiment, trench depth D2 is greater than about 130 percent of trench depth D1, and may even be greater than about 150 percent of trench depth D1. Trenches 40 define fin 50 therebetween.

Id., [0024].

102. Yu additionally discloses forming “customized fin heights...so that the FinFETs may have customized performance.” EX1010, [0010]. Yu discloses with

reference to Figure 5 below that fins 48 and 50 are formed to have different heights, where the height difference is made by forming trenches of different depths, i.e., D1 around fin 48 and D2 around fin 50. *Id.*, [0023]-[0024].

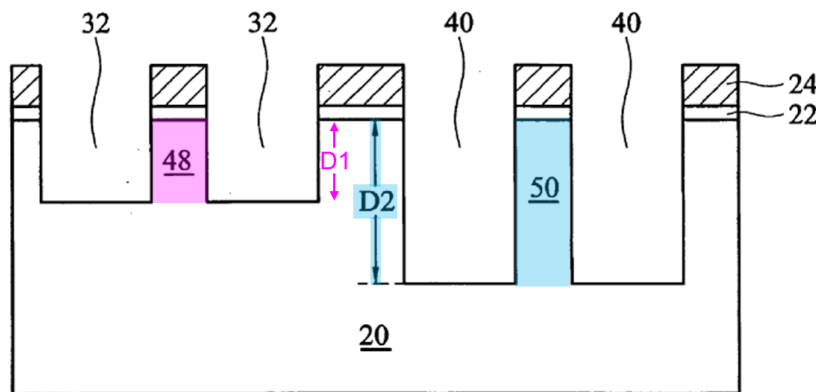


FIG. 5

EX1010, FIG. 5 (annotated). Specifically, Yu discloses that:

In FIG. 3, mask layer 24 and pad layer 22 are etched through openings 28, exposing underlying semiconductor substrate 20. The exposed semiconductor substrate 20 is then etched, forming trenches 32 in semiconductor substrate 20. **In an exemplary embodiment, depth D1 of trenches 32 is substantially close to the desired height of the fin of the desired FinFET. Trenches 32 encircle fin 48 therebetween.** Photoresist 26 is then removed.

Id., [0023].

FIG. 4 illustrates the formation and patterning of photoresist 34, which defines the pattern for forming another fin. Openings 36 are formed in photoresist 34 and define photoresist strip 38, which is surrounded by openings 36. Mask layer 24, pad layer 22 and semiconductor substrate 20 exposed through openings 36 are then etched sequentially, forming trenches 40 in semiconductor substrate 20, as is shown in FIG. 5. **Preferably, trenches 40 have depth D2 different from depth D1 of trenches 32. In an exemplary embodiment, trench depth D2 is greater than about 130 percent of trench depth D1, and may even be greater than about 150 percent of trench depth D1. Trenches 40 define fin 50 therebetween.**

Id., [0024]. Additional process steps may be applied to Fins 48 and 50 to form FinFETs 52 and 54 as shown in Figure 9 below. *Id.*, [0029], [0025]-[0027].

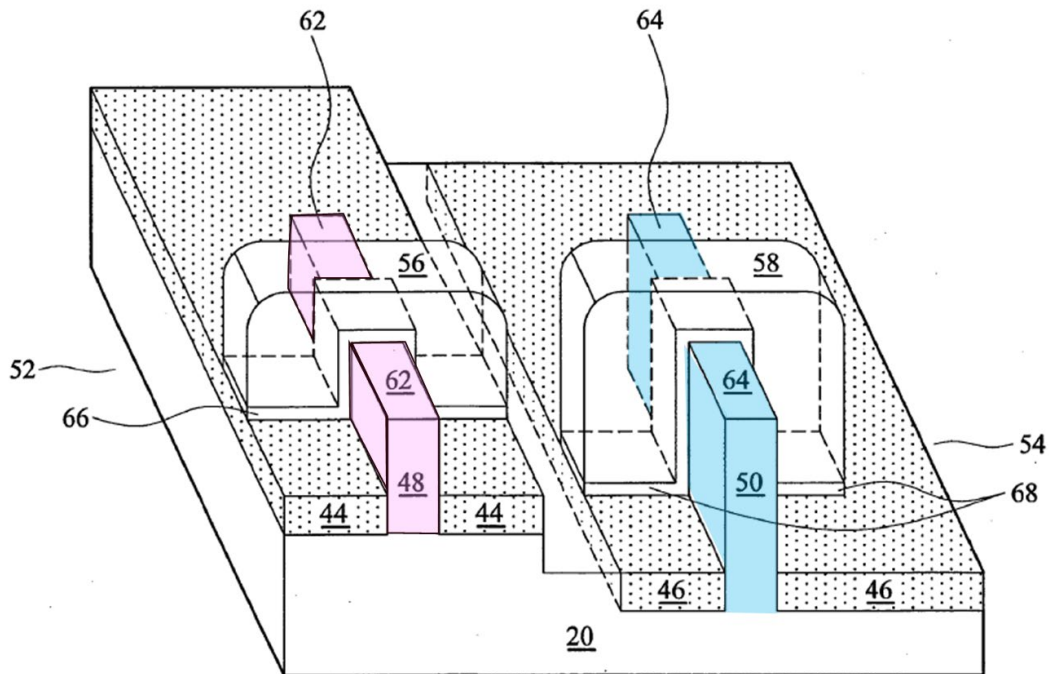


FIG. 9

EX1010, FIG. 9 (annotated).

103. Like Basker, Yu discloses FinFETs for use in ICs and forming fins of the FinFETs by etching a bulk silicon substrate. Thus, a person of ordinary skill in the art would have been motivated to consider Yu's teachings when implementing FinFET structures like those disclosed in the Basker-Hill combination.

104. In view of Yu's teachings/suggestions, including customizing "semiconductor fins with different heights on a same semiconductor chip." (EX1010, [0010], [0019]), a person of ordinary skill in the art would have been motivated to customize the fin heights of the FinFETs in an IC chip, e.g., those in

SRAM cells implemented in the Basker-Hill combination (as discussed for claims 1, 9, and 15). For example, Yu explains that performances of the FinFETs, e.g., the drive current thereof, may be modified by adjusting the channel width, which is a function of the fin height of the FinFET. *Id.*, [0002]-[0004]. Additionally, as discussed in Section V.C, a person of ordinary skill in the art at the time was aware and appreciated that the static noise margin of an SRAM cell depends on the dimensions of the FinFETs used to form the cell. For instance, the noise margin depends on the pull up ratio (PR) of the SRAM cell, which is a parameter for optimizing SRAM performance. For example, it was known that PR should be in the range of 3 to 4 for SRAM cells to be functional. EX1033, 3 (“pull-up ratio should be in...3-4...otherwise data will be [destroyed]”). PR is determined based on the pFinFET and nFinFET’s dimensions, i.e., $PR = (W_{pFET}/L_{pFET}) / (W_{nFET}/L_{nFET})$, where W is the channel width and L is the channel length of the pFinFET or nFinFET. EX1033, 1-2. Accordingly, a person of ordinary skill in the art would have been motivated to customize the fin heights to, e.g., increase W_{pFET} and/or to reduce W_{nFET} (and/or to reduce L_{pFET} and/or to increase L_{nFET}) to achieve the desired PR range.

105. As discussed above, given that the channel width W is a function of the fin height, a person of ordinary skill in the art, guided by Yu’s teaching and their

state of art knowledge, would have been motivated to customize fin heights to, e.g., increase W_{pFET} and/or to reduce W_{nFET} in an SRAM cell in the structure of the Basker-Hill combination to achieve the desired PR range. This would have resulted in the height of the pFinFET's fins ("even" or "second" fins) being different from the height of the nFinFET fins ("odd" or "first" fins) in the structure of the Basker-Hill combination.

106. A person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Basker-Hill-Yu combination, particularly given that Basker and Yu disclose multiple similar aspects of semiconductor structures and fin fabrication process steps, e.g., forming fins by etching a bulk silicon substrate. The Basker-Hill-Yu combination would have involved applications of known technologies (e.g., known process to etch a substrate to form fins of FinFETs) according to known methods (e.g., known method of forming trenches of different depths on a substrate to create height differences between fins) to yield the predictable result of a functional SRAM cell having, e.g., a proper pull-up ratio (PR) and thus static noise margin.

107. Accordingly, it is my opinion that the Basker-Hill-Yu combination discloses and/or suggests claims 2, 10, and 16.

108. Additionally, adjusting/customizing the height difference of the nFinFET and pFinFETs in an SRAM cell would have been a matter of routine optimization an SRAM cell's parameter because it affects SRAM's performance, e.g., the static noise margin of the SRAM cell. EX1033, 1; Section V.C. In fact, Yu explicitly teaches that "*customiz[ing] fin heights...so that the FinFETs may have customized performance.*" EX1010, [0004], [0010]. Therefore, a person of ordinary skill in the art would have been motivated to customize the performance of pFinFETs and nFinFETs in the structure of the Basker-Hill combination by customizing their fin heights such that the SiGe fins ("even" or "second" fins) "are...different from" Si fins ("odd" or "first" fins) "in height" to achieve an optimum SRAM design/structure. Moreover, customizing fin heights for pFinFETs and nFinFETs is well within the understanding and technical ability of a person of ordinary skill in the art. *Id.* This is especially true given that the '292 patent provides no evidence that fins having "height" difference produces any new/unexpected result.

C. Inaba Discloses and/or Suggests Claims 1, 5, 7-9, 13, 15, and 19

109. As I explained below, Inaba discloses and/or suggests “a semiconductor structure for forming FinFET[s]” as recited in the identified challenged claims.

110. Inaba initially describes its structure in the context of four embodiments. The first embodiment is discussed in connection with Figures 1-4B (EX1005, [0017]-[0024], [0051]-[0095]), the second embodiment in connection with Figures 5A-5B (*id.*, [0025]-[0026], [0096]-[0113]), the third embodiment is discussed in connection with Figures 6A-6B (*id.*, [0027]-[0028], [0114]-[0123]), and the fourth embodiment is discussed in connection with Figures 7A-10B. *Id.*, [0029]-[0038], [0125]-[0157]).

111. Inaba explains that each of these four embodiments are related and build from each other. *Id.*, [0096] (explaining that in the second embodiment, “the same parts as those in **the first embodiment** are indicated by the same reference numerals and a detailed explanation of them will be omitted”), [0114] (explaining in the third embodiment “the same parts as those in the **first and second embodiments** are indicated by the same reference numerals and a detailed explanation of them will be omitted”), [0125] (explaining in the fourth embodiment

“the same parts as those in the **first to third embodiments** are indicated by the same reference numerals and a detailed explanation of them will be omitted.)

112. Inaba describes a last embodiment in connection with Figures 11A-14, which is a modification of the first to fourth embodiments. *Id.*, [0039]-[0045], [0158]-[0177]. Consistently, Inaba explains that in this last modification embodiment, “[t]he same parts [discussed in the last embodiment] as those in the first to fourth embodiments are indicated by the same reference numerals and a detailed explanation of them will be omitted.” *Id.*, [0159].

113. Sections IX.C.1-4 below demonstrates how Inaba’s last embodiment discloses the features recited in the challenged claims. In doing so, any disclosures identified from Inaba’s other embodiments are in context of the modification to those embodiments as expressly contemplated by Inaba (as explained above). For example, a person of ordinary skill in the art would have understood from Inaba’s disclosures, the teachings related to Inaba’s other embodiments that are carried

through to the last modified embodiment are disclosures attributed to the last modified embodiment.⁴

114. I have been asked to consider a scenario where disclosures associated with Inaba's other embodiments do not apply to Inaba's last modified embodiment. In that scenario and in my opinion, a person of ordinary skill in the art would have been motivated to implement those other embodiments' features in the last modified embodiment. Such a person would have been motivated to implement those features because Inaba discloses that each of the embodiments are related and build from each other. Additionally, each of the embodiments are associated with forming an SRAM cell (e.g., Figure 1 of Inaba), and thus a person of ordinary skill in the art would have been motivated to consider and implement features from different embodiments in the modified embodiment. EX1005, [0050] ("Hereinafter, **in embodiments of the invention, an explanation will be given using an SRAM**

⁴ The same is true for Sections IX.D-IX.E, which rely on Inaba's last modified embodiment corresponding to that explained here in Section IX.C. See my discussions below in Sections IX.D-IX.E.

including an inverter circuit with the aforementioned structure as an example”),
[0053] (“FIG. 1 is an equivalent circuit diagram of an SRAM cell 20.”).

1. Claims 1, 9, and 15

(i) [1.pre]/[9.Pre] “A semiconductor structure for forming FinFETs, comprising”

[15.Pre] “A semiconductor structure for forming FinFET, comprising”

115. I understand that these features are preambles of claims 1, 9, and 15. I have been asked to assume that these preambles are limiting. Under that assumption, Inaba discloses and/or suggests the preambles of claims 1, 9 and 15. See my discussion above in Section IX.C; EX1005, Abstract, [0003], [0006], [0015]-[0016].

116. Inaba explains the known configuration of an SRAM, formed using FinFETs. EX1005, Abstract, [0047] (“an inverter circuit composed of a p-type FinFET and an n-type FinFET”), [0160] (reciting embodiments related to an SRAM cell), [0167], [0176].

117. A person of ordinary skill in the art would have understood such disclosed features are applicable to Inaba’s structure disclosed in the last modified embodiment (and associated disclosures associated with the other embodiments modified therefrom). See my discussion above in Section IX.C; EX1005, [0017], [0049], [0050] (“Hereinafter, in embodiments of the invention, an explanation will

be given using an SRAM including an inverter circuit with the aforementioned structure as an example.”), [0160] (“In the first to fourth embodiments, an SRAM cell so configured that”). For example, Inaba discloses an SRAM cell 20 having six transistors, including four nFinFETs N1-N4 and two pFinFETs” P1-P2. EX1005, [0053]-[0057] (disclosing “each of the transistors P1 to P2, N1 to N4 in the SRAM cell 20 is composed of a FinFET where a fin acting as an active region crosses a gate electrode in three dimensions, thereby forming a MIS transistor.”), FIG. 1.

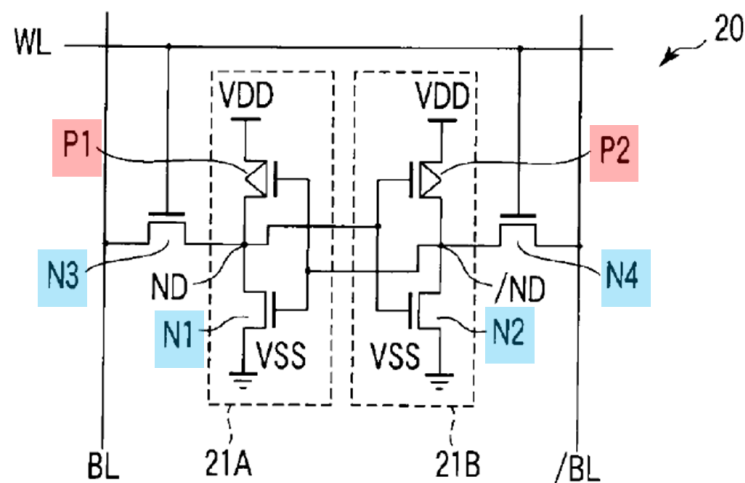


FIG. 1

EX1005, FIG. 1 (annotated).

118. Figure 11A (below) of the last embodiment shows an SRAM circuit layout including two nFinFETs N1a and N1b connected in parallel to form N1, two

nFinFETs **N2a** and **N2b** connected in parallel to form **N2**, two nFinFETs **N3** and **N4** (grey), and two pFinFETs **P1** and **P2**. EX1005, [0164]; *see also id.*, [0054].

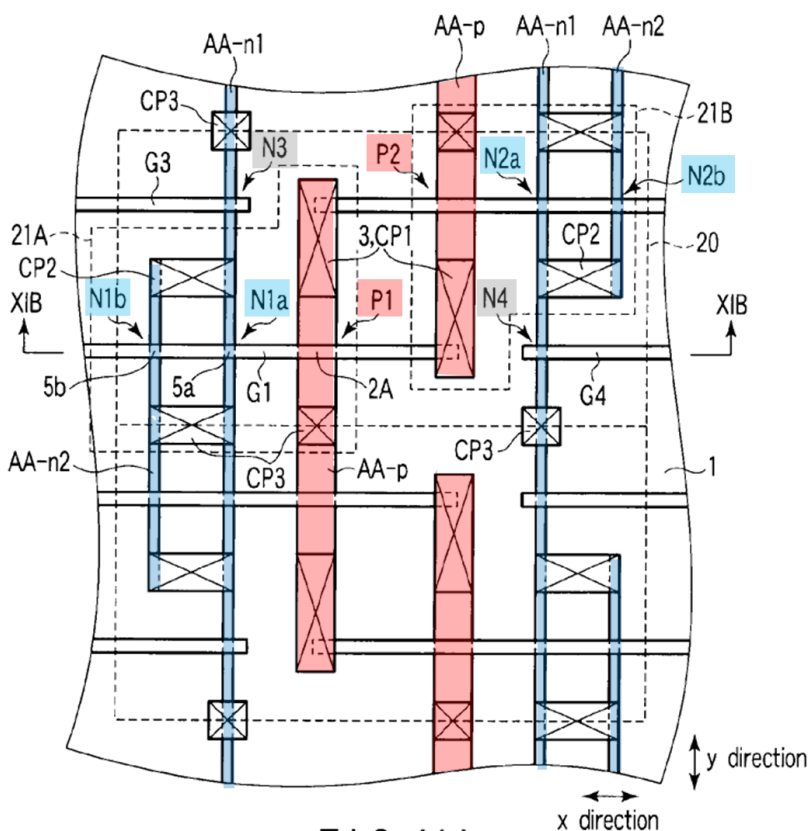


FIG. 11A

EX1005, FIG. 11A (annotated). It seems to me that in Inaba's SRAM cell, transistor N1 is formed using two nFinFETs N1a and N1b and transistor N2 is formed using two nFinFETs N2a and N2b. Moreover, because transistor N1 (shown in Figure 5A) is formed using nFinFETs N1a and N1b connected in parallel (shown in Figure 11A) (*see* EX1005, [0164]), a person of ordinary skill in the art would have understood that fin 5 (shown in Figures 5A/B) used for forming transistor N1 corresponds to

fins 5a and 5b used for forming transistors N1a and N1b (shown in Figure 11A) respectively. EX1005, [0165]; *see also id.*, [0054]. Similarly, because transistor N2 (shown in Figure 5A) is formed using transistors N2a and N2b (shown in Figure 11A), a person of ordinary skill in the art would have understood that fin 5 (shown in Figures 5A/B) used for forming transistor N2 correspond to fins 5a and 5b for transistors N2a and N2b (shown in Figure 11A) respectively.⁵

119. According to Inaba, the fabrication of SRAM cell 20⁶ includes, e.g., forming mask layer 8 (yellow), sidewall mask 10 (blue), and resist mask 11 (red) on semiconductor substrate 1 that includes p- and n-wells, as shown in Figure 13B, where mask 10 resides in the region where nFinFETs are to be formed, and a resist mask 11 is for forming pFinFETs each having a fin width greater than that of the nFinFETs. EX1005, [0169]-[0172].

⁵ While fin 5b is not shown in Figure 14, as explained below, it is present as can be seen from FIG. 14* where the cross-section line in Figure 11A has been moved north of line XIII B in Figure 13A, as discussed below for limitations [1.b]/[9.b]/[15.b].

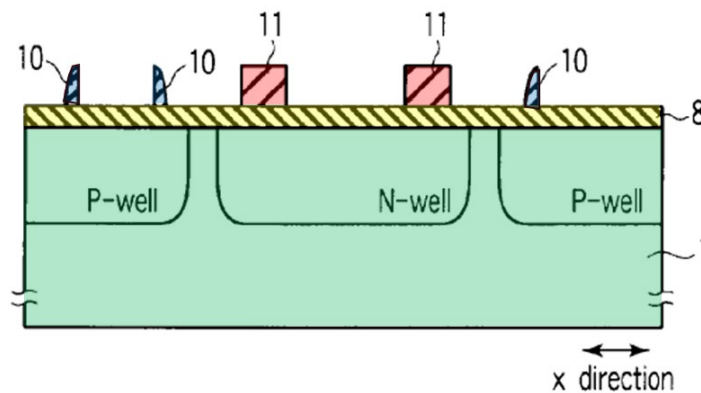
⁶ SRAM cell 20 is consistently referenced in the first to fourth and last embodiments. EX1005, FIGS. 1-2A, 5A, 6A, 7A, 11A.

First, as shown in FIGS. 12A and 12B, well regions N-well, P-well are formed in a semiconductor substrate 1. Thereafter, by the same method as in the first embodiment, **a mask layer 8 and a dummy pattern 9 are formed.** On the side face of the dummy pattern 9 in an n-type FinFET formation planned region, **a closed-loop sidewall mask 10 is formed.**

EX1005, [0171].

Next, after the dummy pattern 9 is removed, the closed-loop sidewall mask 10 is trimmed as shown in FIGS. 13A and 13B so that **a sidewall mask 10 with a two-line pattern may remain in the region where an n-type FinFET acting as a driver transistor is to be formed.** Then, in a p-type FinFET formation planned region, **a resist mask 11 with a pattern where the fin width of the p-type FinFET is greater than that of the n-type FinFET is formed.**

Id., [0172]. *See also id.*, [0158]-[0159] (disclosing an SRAM structure based on modifications of the first to fourth embodiments).



EX1005, FIG. 13B (annotated).

120. As shown in Figure 14 below, by using these masks shown in Figure 13B, substrate 1 is etched to form (1) fins 5a, 5b in the region where nFinFETs are to be formed and (2) fins 2A and 3 in the region where pFinFETs are to be formed.

Thereafter, using the sidewall mask 10 and resist mask 11, the mask layer 8 and semiconductor substrate 1 are etched by, for example, RIE techniques, thereby forming fins 5 a, 5 b as two active regions in the region where an n-type FinFET acting as a driver transistor is to be formed as shown in FIG. 14. Moreover, in the p-type FinFET formation planned region, fins 2A, 3A [sic] serving as active regions are formed. The fin widths W1, W2A of the fins 2A, 3 of the p-type FinFET are greater than the fin width W3 of the fins 5 a, 5 b of the n-type FinFET.

EX1005, [0173].

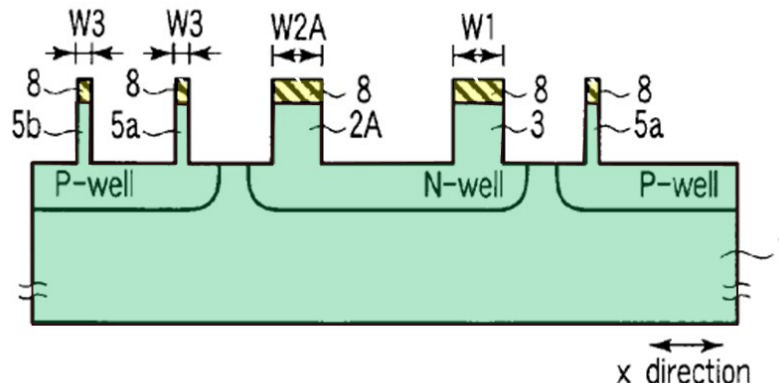
121. Gate electrodes and source/drain layers are then formed to produce the FinFETs. *Id.*, [0174]-[0176].

Thereafter, as shown in FIGS. 11A and 11B, by the same method as in the first embodiment, gate electrodes G1 to G4, a gate sidewall (not shown), an interlayer insulating layer (not shown), a source/drain diffused layer (not shown), contact plugs CP1 to CP3 are formed sequentially.

By the above processes, an SRAM cell with the β ratio=2 using FinFETs can be formed.

Accordingly, it is possible to form SRAM cells with an improved operating stability and provide an SRAM including inverter circuits composed of FinFETs with improved drive characteristics.

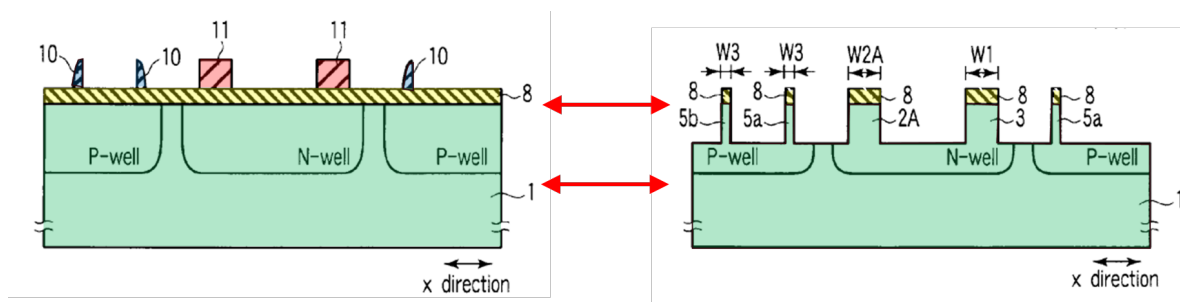
Id., [0174]-[0176].



EX1005, FIG.14 (annotated). Accordingly, Inaba discloses and/or suggests a “semiconductor structure” (e.g., as shown in Figure 14) “for forming FinFETs” (as recited in preamble [1.pre] and [9.pre]) and “forming FinFET” (as recited in preamble [15.pre]).

(ii) [1.a]/[9.a]/[15.a] “a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;”

122. It is my opinion that Inaba discloses and/or suggests these limitations. Inaba discloses substrate 1 is a “semiconductor substrate.” EX1005, [0171] (“semiconductor substrate 1”).



EX1005, FIG. 13B (left annotated) and FIG. 14 (right annotated). Inaba discloses “a top portion of the semiconductor substrate,” e.g., as shown between the red arrows, “comprises a semiconductor material.” Inaba explains substrate 1 may be a “bulk semiconductor substrate.” EX1005, [0074] (“the **bulk** semiconductor substrate 1”), [0100] (“the **bulk** semiconductor substrate 1”), [0126] (“a

semiconductor substrate in which the n- and p-type FinFETs N1 to N4, P1 to P2 are provided has been a **bulk** semiconductor substrate”), [0168] (other embodiments with a **bulk substrate** such as in the first to third embodiments can be used – “the third embodiment has been used as the basic structure [but] is not restricted to this [] one of the other embodiments may be used as the basic structure”), [0177] (disclosing that the FinFETs may be formed on a **bulk** semiconductor substrate). Given that semiconductor substrate 1 is a “bulk” substrate, the entire semiconductor substrate, including its top portion, is formed of a semiconductor material, e.g., silicon. *Id.*, [0081] (“a semiconductor substrate (e.g., an Si (100) plane single-crystal substrate) 1”). Accordingly, Inaba discloses and/or suggests “a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material.”

(iii) [1.b] “a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material”

[9.b] “a plurality of odd fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other”

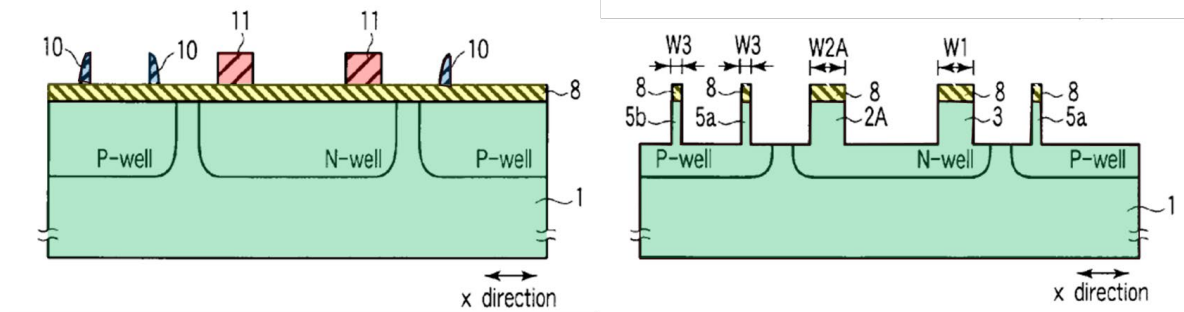
[15.b] “a plurality of first fins of the FinFETs on the semiconductor substrate and being formed of the

semiconductor material, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and”

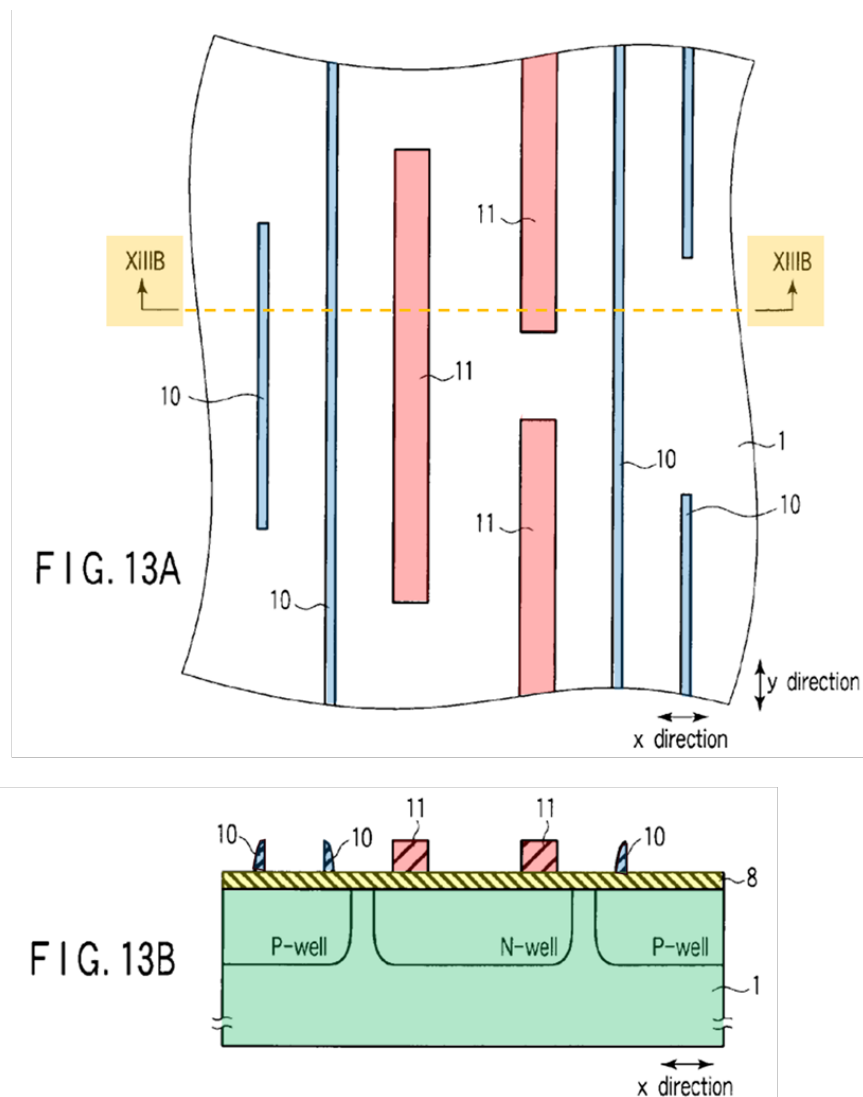
123. It is my opinion that Inaba and/or suggests discloses these limitations. As I have discussed for the preambles in Section IX.C.1(i), and as shown in Figures 13B and 14, by using mask layers 10, 11, silicon substrate 1 is etched to form (1) fins 5a, 5b in the region where nFinFETs are to be formed and (2) fins 2A and 3 in the region where pFinFETs are to be formed. EX1005, [0173].

Thereafter, **using the sidewall mask 10 and resist mask 11, the mask layer 8 and semiconductor substrate 1 are etched...thereby forming fins 5a, 5b as two active regions in the region where an n-type FinFET acting as a driver transistor is to be formed as shown in FIG. 14. Moreover, in the p-type FinFET formation planned region, fins 2A, 3A [sic] serving as active regions are formed. The fin widths W1, W2A of the fins 2A, 3 of the p-type FinFET are greater than the fin width W3 of the fins 5 a, 5 b of the n-type FinFET.**

EX1005, [0173]; *see also id.*, [0059] (“fin may be obtained by carving the semiconductor substrate into thin strips”).



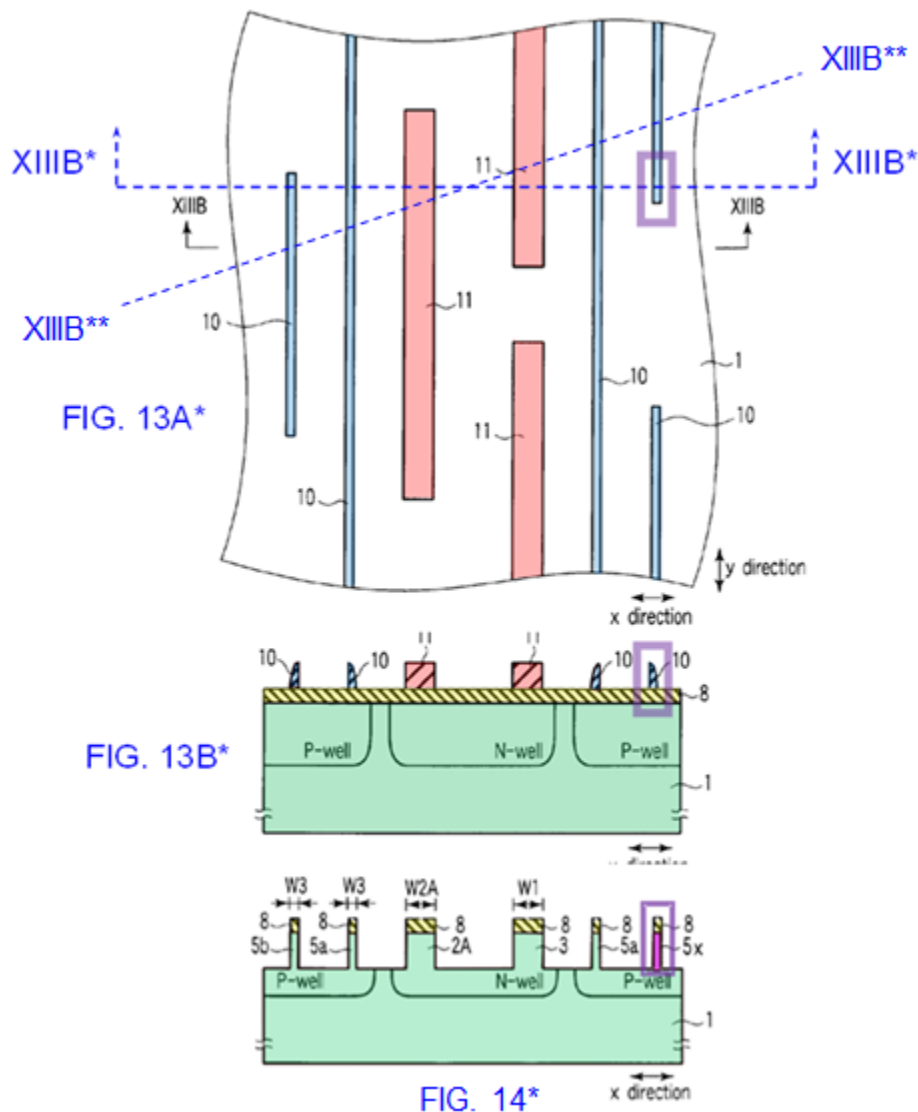
EX1005, FIG. 13B (left annotated) and FIG. 14 (right annotated). Inaba explains that “FIG. 13B is a sectional view taken along line XIII B-XIII B of FIG. 13A” as shown below. EX1005, [0044].



EX1005, FIG. 13A (top, annotated), 13B (bottom, annotated). Since there are six fins shown in the upper half of Figure 13A, a person of ordinary skill in the art would have understood that a sectional view showing six fins could be obtained, for example, along a line located just north of line XIIIIB, e.g., line XIIIIB* or XIIIIB**

as shown in Figure 13B*⁷ below. A person of ordinary skill in the art would have also understood that how the sectional view is taken would not affect the relative fin width relationship among the six fins, which can be ascertained from the top view (Fig. 13A). As shown below 13B*, the sectional view includes one additional sidewall mask 10 (purple).

⁷ FIG. 13B* is a modification of FIG. 13B based on moving the line XIIIIB in FIG. 13A to line XIIIIB* in FIG. 13A*.



124. Given that the fins are defined by the masks 10, 11 as discussed above in relation to Figure 13B, a person of ordinary skill in the art would have also understood that, following the etch process, the sectional view along line XIII B* or XIII B** includes fin 5x (purple). EX1005, [0173]. The location of fin 5x in FIG.

14*⁸ is consistent with the location of mask 10 in Figures 12A and 12B. EX1005, [0171]-[0172] (disclosing that “[o]n the side face of the dummy pattern 9 in an n-type FinFET formation planned region, a closed-loop sidewall mask 10 is formed”), [0164] (“n-type FinFETs N1a, N1b, N2a, N2b constituting a driver transistor are composed of fins acting as two active regions AA-n1, AA-n2.”). Thus, Inaba discloses forming at least six fins of FinFETs in a single SRAM cell, where widths of fins 2A and 3 (W2A and W1 respectively) are greater than the widths of fins 5a, 5b, 5x (W3), as shown in Figures 11A and 14* below.

⁸ FIG. 14* is a modification of FIG. 14 based on moving the line XIIIIB in FIG. 13A to line XIIIIB* in FIG. 13A*.

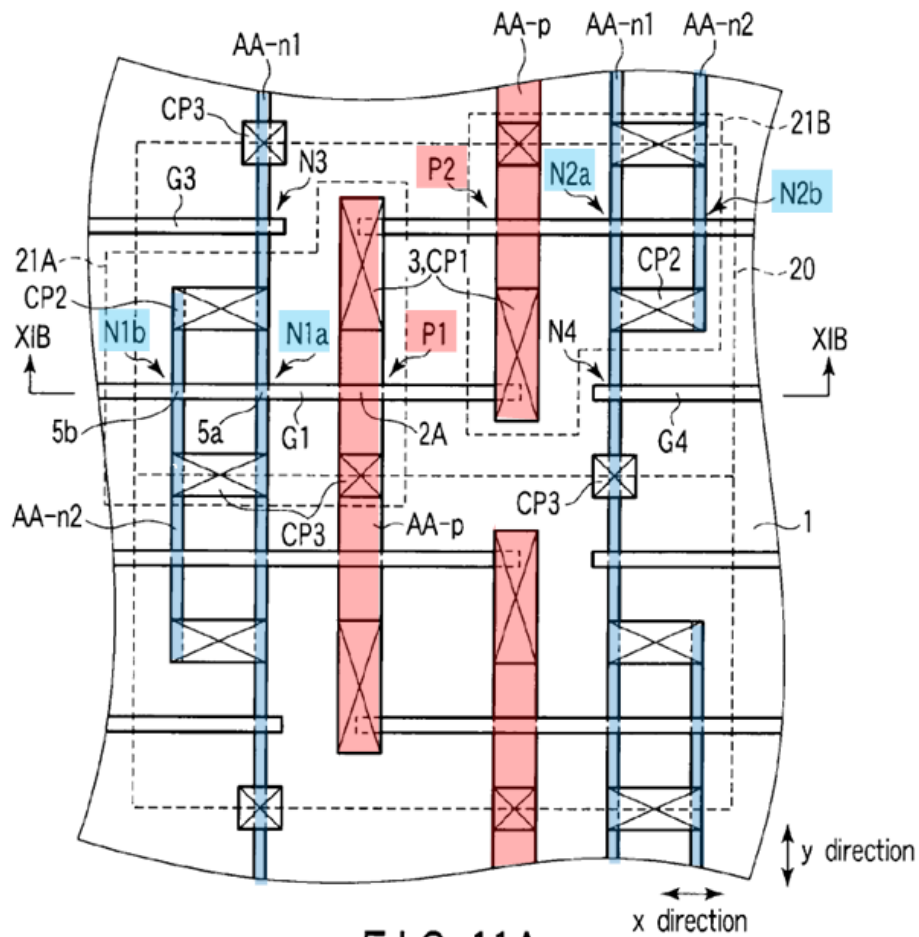


FIG. 11A

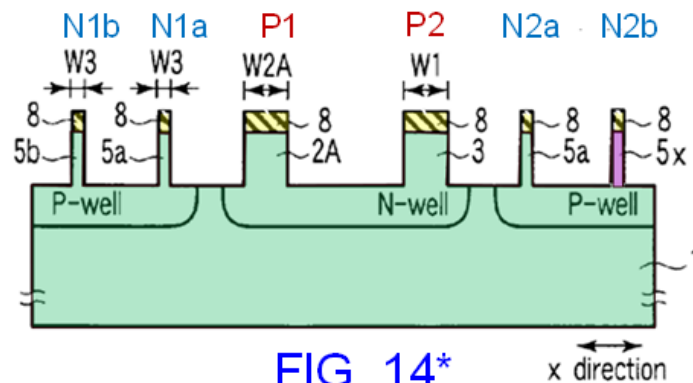


FIG. 14*

FIG. 14* (annotated and modified to include fin 5x).

125. As I discussed above in Section VIII, I have been asked to apply certain assumptions regarding limitations associated with the arrangement of the “odd” or “first” fins and “even” or “second” fins.

126. Inaba, as shown in Figure 14* below, discloses three groups of fins, e.g., Groups 1-3, where Groups 1 and 3 each corresponds to “a plurality of **odd** [or **first**] fins of the FinFETs” and Group 2 corresponds to “a plurality of **even** [or **second**] fins of the FinFETs” of claims 1/9/15 under the above-mentioned assumed interpretation. (see limitations [1.c], [9.c], [15.c] discussed in the next section).

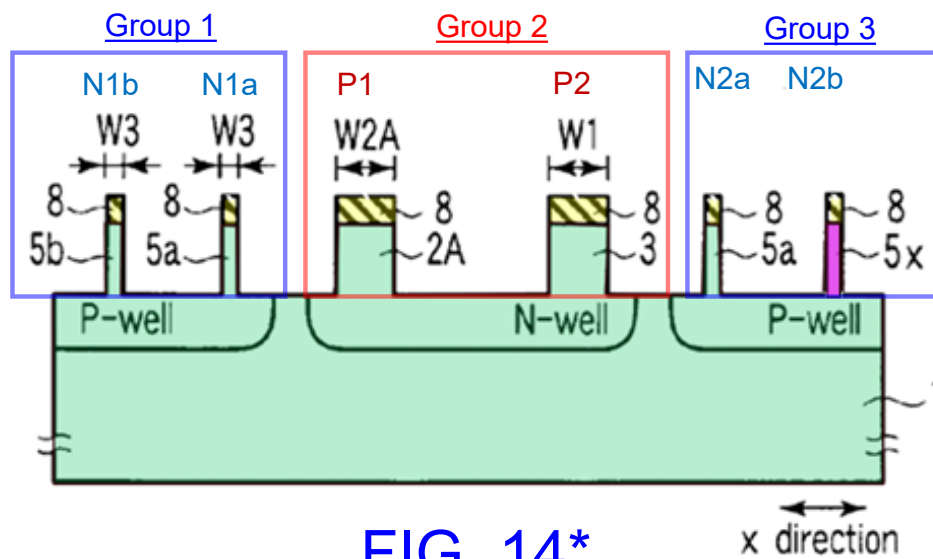


FIG. 14*

127. As shown in Figure 14* above, the Groups 1-3 fins are on semiconductor substrate 1 (“on the semiconductor substrate” as claimed) and

protrude from the substrate. Additionally, as discussed above, by using mask layers 10, 11 shown in Figure 13B*, semiconductor substrate 1 is etched to form the fins. EX1005, [0173]. Because the mask layers 10, 11 atop the substrate define the location and feature size (e.g., width) of the fins, Inaba discloses Groups 1 and 3 are “defined from the semiconductor substrate” as recited in limitation [1.b] and “formed of the semiconductor material” comprised in the top portion of the semiconductor substrate, as recited in limitations [1.b], [9.b] and [15.b]. *See also* my discussions for limitations [1.a]/[9.a]/[15.a].

128. Additionally, as shown in FIG. 14* and given that the fins are formed of the substrate by a masked etch process, Inaba discloses and/or suggests Groups 1 and 3 “fins and the semiconductor substrate are in direct contact with each other” as recited in limitations [9.b] and [15.b].

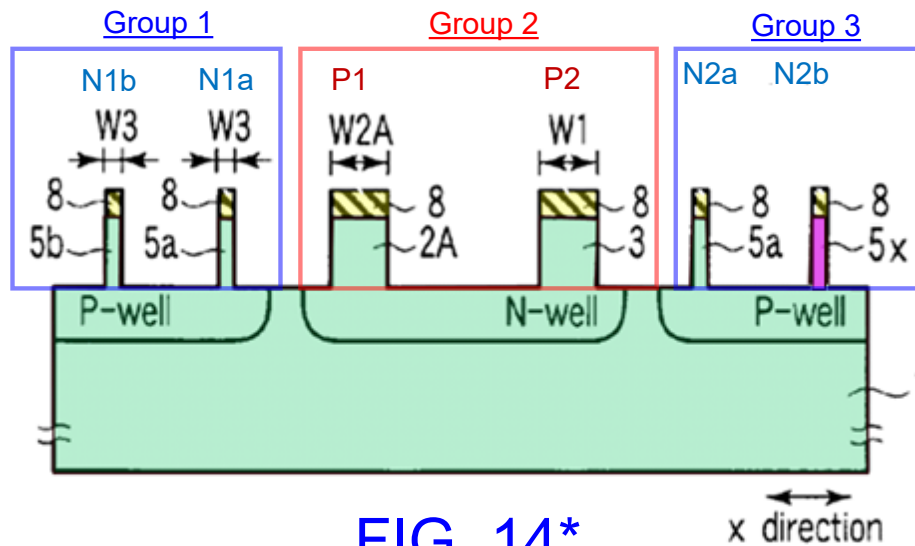
- (iv) **[1.c] “a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.”**

[9.c] “a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact

with the semiconductor material.”

[15.c] “a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.”

129. In my opinion, Inaba discloses and/or suggests these limitations. As discussed for limitations [1.b]/[9.b]/[15.b], the fins as shown in Figure 14* below, including Group 2 fins (corresponding to “a plurality of **even** [or **second**] fins of the FinFETs” of claims 1/9/15 under the assumed interpretation that I discussed in the preceding Section VIII, are on semiconductor substrate 1 (“on the semiconductor substrate” as claimed).



130. As shown in FIG. 14*, Group 2 fins reside between Groups 1 and 3 fins (“between the odd fins of the FinFETs” under the assumed interpretation discussed in Section VIII, as required by limitations [1.c] and [9.c]. Likewise, Inaba discloses “each of the second fins of the FinFETs is located between two first fins of the FinFETs,” as recited in limitation [15.c] under the assumed interpretation discussed in Section VIII, given that each of the fins in Group 2 is located between two fins, each of Groups 1 and 3.

131. Additionally, Group 2 fins are wider than Groups 1 and 3 fins and thus differ from them in width. EX1005, [0169]-[0172] (disclosing “in a p-type FinFET formation planned region, a resist mask 11 with a pattern where the fin width of the p-type FinFET is greater than that of the n-type FinFET is formed”), [0173] (“fin

widths W1, W2A of the fins 2A, 3 of the p-type FinFET are greater than the fin width W3 of the fins 5a, 5b of the n-type FinFET”).

132. Thus, Inaba discloses and/or suggests limitations [1.c], [9.c], and [15.c] under the assumed interpretation discussed in Section VIII.

2. Claims 5, 13, and 19

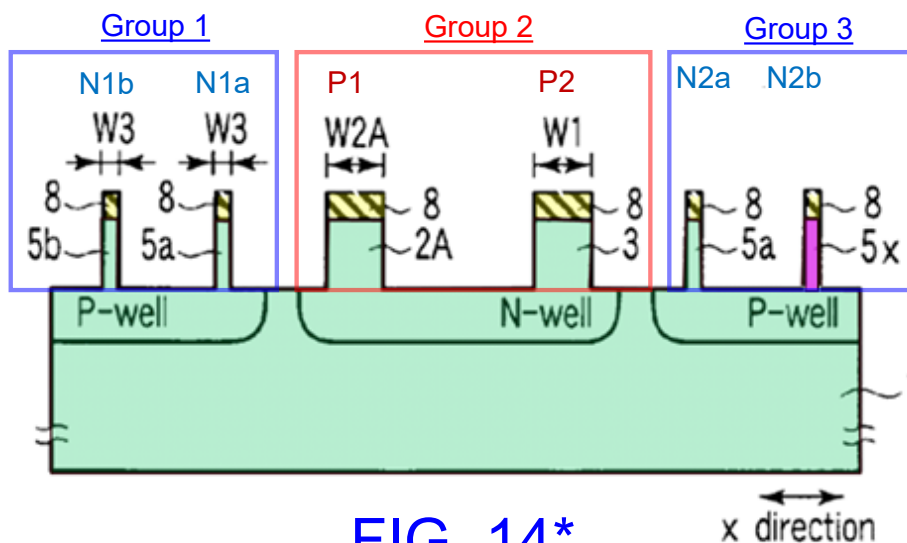
(i) 5. “The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.”

13. “The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si.”

19. “The semiconductor structure of claim 15, wherein the first fins of the FinFETs comprise Si.”

133. It is my opinion that Inaba discloses and/or suggests these limitations. Per my discussion of limitations [1.b]/[9.b]/[15.b] above, Groups 1 and 3 fins (“the odd fins of the FinFETs” under the assumed interpretation discussed in Section VIII are defined from *silicon* substrate 1 and formed of the same. EX1005, [0177] (“manufacturing method of forming FinFETs on the **bulk** semiconductor substrate as in the first to third embodiments...may be applied to...the fourth embodiment”); *see also id.*, [0081] (“a semiconductor substrate (e.g., an **Si (100) plane single-crystal substrate**) 1,” describing bulk silicon substrate used for the first

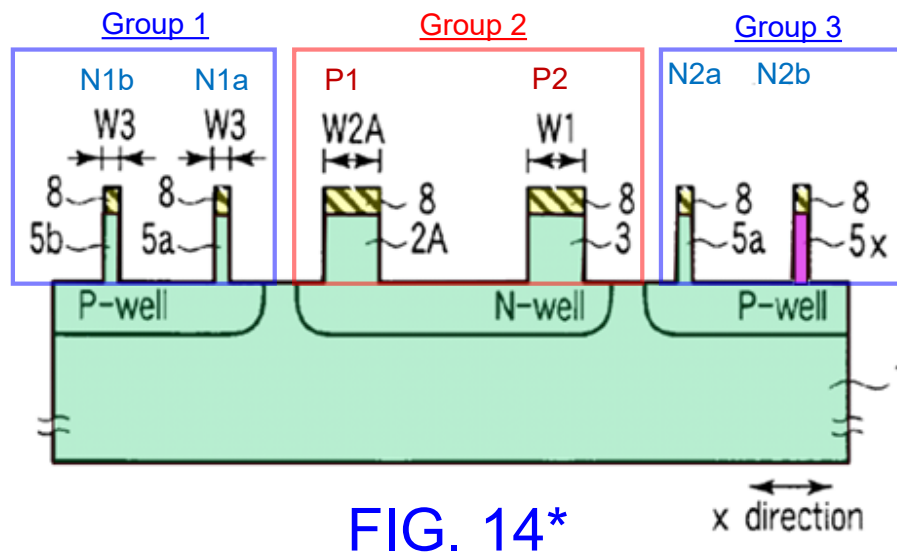
embodiment). Thus, Inaba discloses and/or suggests these limitations under the assumed interpretation discussed in Section VIII.



3. Claim 7

- (i) 7. “The semiconductor structure of claim 1, wherein the odd fins of the FinFETs are electrically connected to the semiconductor substrate.”

134. It is my opinion that Inaba discloses and/or suggests this limitation. As I have discussed for limitations [1.b]/[9.b]/[15.b], Groups 1 and 3 fins (“the odd fins of the FinFETs” under the assumed interpretation discussed in Section VIII are defined from *silicon* substrate 1 and formed of the same. Consistent with Figure 14* below, and given that the fins are formed of the substrate by a masked etch process, Groups 1 and 3 fins are connected to silicon substrate 1. EX1005, [0173].



135. A person of ordinary skill in the art would have understood, given Groups 1 and 3 fins and the substrate are connected and both are the same semiconductor material, i.e., silicon, these fins and the substrate are electrically connected. Thus, Inaba discloses claim 7 under the assumed interpretation discussed in Section VIII.

4. Claim 8

- (i) **8. “The semiconductor structure of claim 1, wherein the semiconductor substrate is a single layer structure.”**

136. In my opinion, Inaba discloses and/or suggests this limitation. Per my discussion for limitations [1.a]/[9.a]/[15.a], semiconductor substrate 1 may be a

“bulk semiconductor substrate” (EX1005, [0100], [0126], [0177]) and thus the entire substrate is formed of “a single layer structure” of semiconductor material.

D. Inaba in View of Basker Discloses and/or Suggests Claims 3, 4, 6, 11, 12, 14, 17, 18, and 20⁹

1. Claims 3, 11, and 17

(i) 3. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material.”

11. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise an epitaxy material.”

17. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise an epitaxy material.”

137. It is my opinion that Inaba in view of Basker discloses and/or suggests these limitations. Although Inaba does not expressly disclose “the [even/second] fins of the FinFETs comprise an epitaxy material,” a person of ordinary skill in the art would have been motivated to implement this feature in view of Basker.

138. As I have discussed above for limitations [1.pre]/[9.pre]/[15.pre] in Section IX.A.1(i), Basker discloses the use of Si fin for nFinFETs and SiGe fins for pFinFETs. Like Inaba, Basker discloses FinFETs formed on a bulk semiconductor

⁹ See my discussion above in Section IX.C.

substrate formed of monocrystalline silicon. EX1006, [0020], [0025] (“bulk substrate that may include...monocrystalline silicon”). Also similar to Inaba, Basker discloses an nFinFET that “is formed on a fin made from a substrate material” (*id.*, [0020]), i.e., silicon fin (*id.*, [0038]) and the fins are formed by using a mask and an etch process (*id.*, [0025]-[0029] (disclosing “Liner 18 acts as an etch mask to open up layer 16. Layer 16 provides a semiconductor material from which FETs may be formed”)). Thus, a person of ordinary skill in the art would have been motivated to consider Basker’s teachings in the same technical field when implementing semiconductor devices similar to those of Inaba.

139. Basker additionally discloses improving the pFinFET performance by adding Ge/SiGe to silicon fins to **form SiGe fins**. EX1006, [0020]-[0021].

An n-type field effect transistor (nFET) is formed on a fin made from a substrate material. A corresponding pFET is formed on a fin which is processed by pushing or diffusing an element into the substrate material to form a new structure. In one example, the substrate includes silicon which is employed to form the fin for the nFET. In this example, **a fin for the pFET includes silicon as well, but Germanium (Ge) is pushed into silicon to form a SiGe fin for the formation of the pFET.** The pFET is

formed by, e.g., oxidation condensation (to push Ge into a Si fin during oxidation).

Id., [0020].

In this way, the pFET finFET with a SiGe body achieves a corrected threshold voltage (V_t) since the dimensions of the fin are maintained and an advantageous strain is imparted to the fin. **The SiGe and associated strain results from the Ge within a silicon matrix. The strain improves pFET performance because intermixing Ge into Si requires strain relaxation to open up the spaces in the silicon for larger Ge atoms.** This is much easier to do in a direction normal to a carrier transport direction. This is an ideal combination: comparable V_t , strain, and a (110) surface for the pFET finFET. In fact in many useful integrated circuit components, such as logic gates and in particular NAND gates, the pFET can be made to especially gain from these advantageous effects.

EX1006, [0021].

140. As discussed above for claims 3/11/17 in Section IX.A.2, Basker discloses forming SiGe fins by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22. *Id.*, [0005], [0031]-[0032], [0041]; *see also id.*, [0020]-[0021], claim 1. Since the resulting SiGe fins incorporate the epitaxially deposited

material, the resulting SiGe fins “comprise an epitaxy material.” A person of ordinary skill in the art would have understood that Basker’s SiGe fin formation results in epitaxy material and thus the resulting SiGe fins “comprise an epitaxy material.” EX1013, 2 (“the solid phase epitaxy growth of SiGe by Ge condensation”); EX1038, 3-4. Additionally, a person of ordinary skill in the art would have known that SiGe fins could also be formed using, e.g., CVD and MBE, and would have found it obvious to use any of them. *See, e.g.*, EX1039, 4:23-5:9. Thus, Basker discloses and/or suggests SiGe “fins of the FinFETs comprise an epitaxy material.”

141. A person of ordinary skill in the art would have been motivated to form SiGe fins for pFinFETs in a semiconductor structure similar to that discussed in Inaba (e.g. fins 2A, 3 in Figure 14 of Inaba) in view of Basker. **First**, a person of ordinary skill in the art would understand there has been a general trend at the relevant time to include Ge/SiGe into the transistor’s channel, which traditionally has been made of silicon. EX1025, 1. In fact, it was known that “SiGe channel [FINFET] is an attractive replacement” of Si channel pFinFETs. EX1026, 1; *see also* EX1030, 2; EX1031, 1; Section V.B.

142. A person of ordinary skill in the art would have understood SiGe fins improve mobility of the charge carrier for pFinFETs and thus improve current drive of the transistors and speed of transistors' operation. EX1016, 1 (“[a] way to improve FET performance is the **use of a strained SiGe channel**.... All SiGe pFETs under test showed **better NBTI** [Negative Bias Temperature Instability] **reliability** with respect to their Si channel counterparts.”), 2 (“the introduction of Ge in the channel **dramatically improved the NBTI reliability**”), 4 (same); EX1017, 1 (“Selective, epitaxial strained SiGe...is an attractive channel material beyond Si due to its **high carrier mobility** ($\sim 2\times$ Si) and compatibility to the conventional CMOS processes....Besides high mobility, the SiGe valence band offset to Si simplifies achievement of a low pFET threshold voltage (V_t) with high-k/metal gate”); EX1018, 1 (“Results obtained in this study advance the **optimization of high mobility SiGe** as an alternative channel material for future technology nodes”); Section V.B.

143. **Second**, as Basker explains, it is “advantageous” to impart strain to the fin, and the strain caused by adding Ge to the silicon fins “improves pFET performance.” EX1006, [0021], [0031], [0038].

144. **Third**, Basker explains using a silicon fin for an nFinFET and using a SiGe fin for a pFinFET provide “the correct threshold voltages for both [nFinFET] and [pFinFET],” allowing use of “the same gate dielectric...and the same gate conductor...,” which would have simplified the fabrication processes and reduced cost. EX1006, [0038]; EX1023, [0008] (“fabricating transistors having gate electrodes made of two different materials is prohibitively expensive”), [0016] (“Engineering the band gap of the semiconductor transistor channels rather than engineering the work function of the transistor gate metal for the individual pMOS and nMOS devices **avoids the manufacturing difficulties** associated with depositing and interconnecting two separate gate metals in a dual-metal gate process.”), [0027] (“the same material is used to form the gate electrode...for pMOS device...and nMOS device.... In this manner, CMOS device **fabrication can be greatly simplified....**”); Section V.B.

145. In light of Basker’s teachings/suggestions in context of the state of art knowledge at the time, it is my opinion that a person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing the Inaba-Basker combination. Indeed, Basker itself discloses adding Ge to the silicon fin results in “an ideal combination” of beneficial features (such as proper threshold voltages for

both nFinFET and pFinFET and use of a (110) surface for the pFET FinFET. EX1006, [0021]. Additionally, Basker explains the disclosed features may be applied to many useful IC components. *Id.*, [0021] (“in many useful integrated circuit components...the pFET can be made to especially gain from these advantageous effects”). Furthermore, combining Inaba with Basker would have involved applications of known technologies (e.g., known use of SiGe for pFinFETs) according to known methods (e.g., known method of forming SiGe fins) to yield the predictable result of improved pFinFETs and other benefits discussed above in the Inaba-Basker combination.

146. Accordingly, in view of Inaba and Basker’s teachings/suggestions, a person of ordinary skill in the art would have been motivated to form pFinFETs, as disclosed in Inaba (e.g., P1 and P2 of Group 2 fins in Figure 14* below) having SiGe fins that “comprise an epitaxy material” as taught by Basker. Thus, the Inaba-Basker combination discloses and/or suggests claims 3, 7, and 11 ***under the assumed interpretation discussed in Section VIII.***

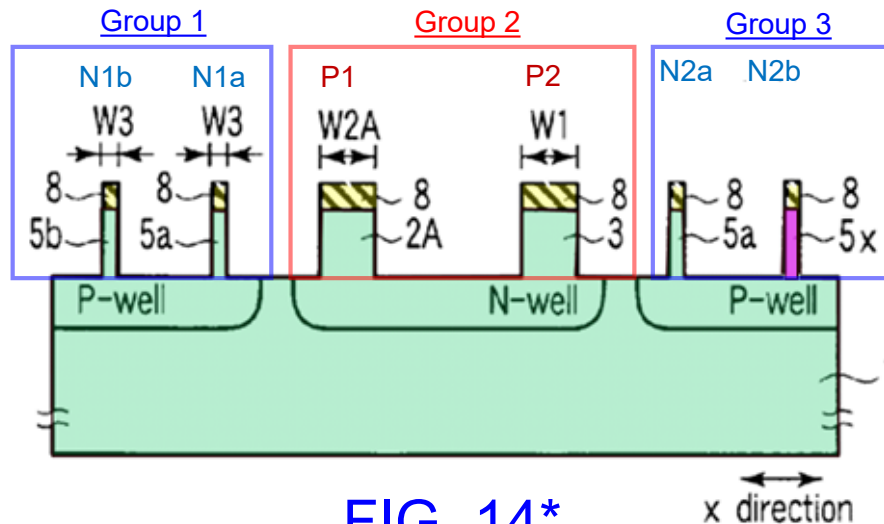


FIG. 14*

2. Claims 4, 12, and 18

(i) 4. “The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.”

12. “The semiconductor structure of claim 11, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.”

18. “The semiconductor structure of claim 17, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.”

147. It is my opinion that the Inaba-Basker combination discloses and/or suggests these limitations. See my discussion above in Sections IX.C.1(iii)-(iv), IX.D.1. Per my discussion for limitations [1.b]/[9.b]/[15.b], Inaba discloses the Groups 1 and 3 fins are formed from the **silicon** substrate. And as discussed for claims 3, 11, and 17, Inaba in view of Basker discloses forming **SiGe fins** for pFinFETs, i.e., the Group 2 fins. See my discussion above in Sections IX.C.1(iii), IX.D.1. Accordingly, for reasons explained for claims 1, 9, 15, and those for claims 3, 11, and 17, the Inaba-Basker combination discloses and/or suggests claims 4, 12, and 18 under the assumed interpretation discussed in Section VIII.

3. Claims 6, 14, and 20

(i) 6. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.”

14. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise SiC or SiGe.”

20. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise SiC or SiGe.”

148. The Inaba-Basker combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18. See my discussion above in Section IX.D.2.

E. Inaba in View of Yu Discloses and/or Suggests Claims 2, 10, and 16

1. Claims 2, 10, and 16

(i) 2. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.”

10. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.”

16. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.”

149. It is my opinion that Inaba in view of Yu discloses and/or suggests this limitation. As I have discussed for limitations [1.b]/[9.b]/[15.b], Inaba discloses “odd fins” or “first fins” (Group 1 fins, including N1a, N1b fins; Group 3 fins, including N2a, N2b fins) of the FinFETs, and “even fins” or “second fins” (Group 2 fins, including P1, P2 fins) of the FinFETs, as shown in Figure 14* below. See my discussion above in Sections IX.C.1(iii); VIII.

150. Inaba does not expressly disclose “the even fins...are further different from the odd fins...in height” or “the second fins...are further different from the first fins...in height.” Nevertheless, a person of ordinary skill in the art would have been

motivated to implement such features in the above-discussed Inaba structure¹⁰ in view of Yu's teachings.

151. Like Inaba, Yu discloses fabrication of FinFETs for use in IC (EX1010, [0001] ("This invention relates generally to semiconductor devices, and more particularly to **Fin field effect transistors (FinFET).**"), [0002] ("Transistors are key components of **modern integrated circuits**"), [0019] ("semiconductor chip")). Also similar to Inaba, Yu discloses forming fins of the FinFETs by etching a bulk silicon substrate. *Id.*, [0028] ("The embodiments discussed in preceding paragraphs are **formed on bulk semiconductor substrate.**"), [0020] ("semiconductor substrate 20 includes **silicon**"), [0021]-[0024] (describing with reference to Figures 2-5 that the substrate is etched to form fin structures). See my discussion above in Section IX.B.1. Thus, a person of ordinary skill in the art would have been motivated to consider Yu's teachings when implementing a semiconductor structure like those disclosed in Inaba.

152. Per my discussion in Section IX.B, Yu discloses forming "customized fin heights...so that the FinFETs may have customized performance." EX1010,

¹⁰ See my discussion above in Sections IX.C.1(iii)-(iv).

[0010]; *see above* Section IX.B; *see also* EX1010, [0023]-[0024] (disclosing process of forming fins of different heights), [0025]-[0027], [0029].

153. As discussed, Yu discloses customizing “semiconductor fins with different heights on a same semiconductor chip.” EX1010, [0010], [0019]. In view of Yu’s teaching, including customizing “semiconductor fins with different heights on a same semiconductor chip” (EX1010, [0010], [0019]), a person of ordinary skill in the art would have been motivated to customize the fin heights of the FinFETs in an IC chip, e.g., those in SRAM cells disclosed/suggested by Inaba as discussed for claims 1, 9, and 15 in Section IX.C.1. Further, as I have discussed for Section IX.B, Yu explains performances of the FinFETs, e.g., static noise margin depends on the dimensions of the FinFETs used to form the cell. Section IX.B.1. Also discussed therein, the static noise margin depends on the pull up ratio (PR) of the SRAM cell, where PR is a parameter for optimizing SRAM performance. For example, it has been reported that PR should be in the range of 3 to 4 for SRAM cells to be functional. Section IX.B.1; EX1033, 1-3. Accordingly, a person of ordinary skill in the art would have been motivated to customize the fin heights to, e.g., increase W_{pFET} and/or to reduce W_{nFET} (and/or to reduce L_{pFET} and/or to increase L_{nFET}) to achieve the desired PR range.

154. As discussed above, given that the channel width W is a function of the fin height, a person of ordinary skill in the art, guided by Yu's teaching and their state of art knowledge, would have been motivated to customize fin heights to, for example, increase W_{pFET} and/or to reduce W_{nFET} in an SRAM cell (in the Inaba structure discussed above) to achieve the desired PR range. This would have resulted in the height of the pFinFET's fins ("even" or "second" fins) being different from the height of the nFinFET fins ("odd" or "first" fins) in the SRAM cell of Inaba.

155. In my opinion, a person of ordinary skill in the art would have had the requisite skill, rationale, and knowledge in implementing the above-discussed Inaba-Yu combination, particularly given that Inaba and Yu shared similar fin fabrication process steps, e.g., forming fins by etching a bulk silicon substrate as discussed above. Additionally, such a person would have expected to succeed in implementing the combination. Combining Inaba with Yu would have involved applications of known technologies (e.g., known process to etch a substrate to form fins of FinFETs) according to known methods (e.g., known method of forming trenches of different depths on a substrate to create height differences between fins) to yield the predictable result of a functional SRAM cell having, e.g., a proper pull-up ratio (PR) and thus static noise margin.

156. Accordingly, in view of Inaba and Yu's teaching, a person of ordinary skill in the art would have been motivated to form nFinFETs (e.g., Groups 1 and 3 fins) with an increased height comparing to the pFinFETs (e.g., Group 2 fins). Accordingly, the Inaba-Yu combination discloses and/or suggests claims 2, 10, and 16.

157. Additionally, as discussed for Section IX.B, adjusting/customizing the height difference of the nFinFET and pFinFETs in an SRAM cell would have been a matter of routine optimization an SRAM cell's parameter because it affects SRAM's performance, e.g., the static noise margin of the SRAM cell. EX1033, 1; Section IX.B; Section V.C. This is especially true given that the '292 patent provides no evidence that fins having "height" difference produces any new/unexpected result.

F. Liaw in View of Basker Discloses and/or Suggests Claims 1, 3-9, 11-15, and 17-20

1. Claims 1, 9, and 15

(i) [1.pre]/[9.pre] "A semiconductor structure for forming FinFETs, comprising"

[15.pre] "A semiconductor structure for forming FinFET, comprising"

158. I understand that these features are preambles of claims 1, 9, and 15. I have been asked to assume that these preambles are limiting. Under that assumption, Liaw discloses and/or suggests these limitations. Liaw discloses a semiconductor device, SRAM, using FinFETs. EX1008, Abstract, 1:49-2:24, 2:61-64 (“The SRAM cell 100 includes fin field-effect transistors (FinFETs)....”), 2:64-3:21. As shown in Figure 9 below, Liaw discloses an SRAM cell 200, including four pull-down FinFETs, PD-11, PD-12, PD-21, PD-22 (blue), two pull-up FinFETs, PU-1 and PU2 (red), and four pass-gate FinFETs, PG-1, PG-2, PG-3 and PG-4 (purple).¹¹

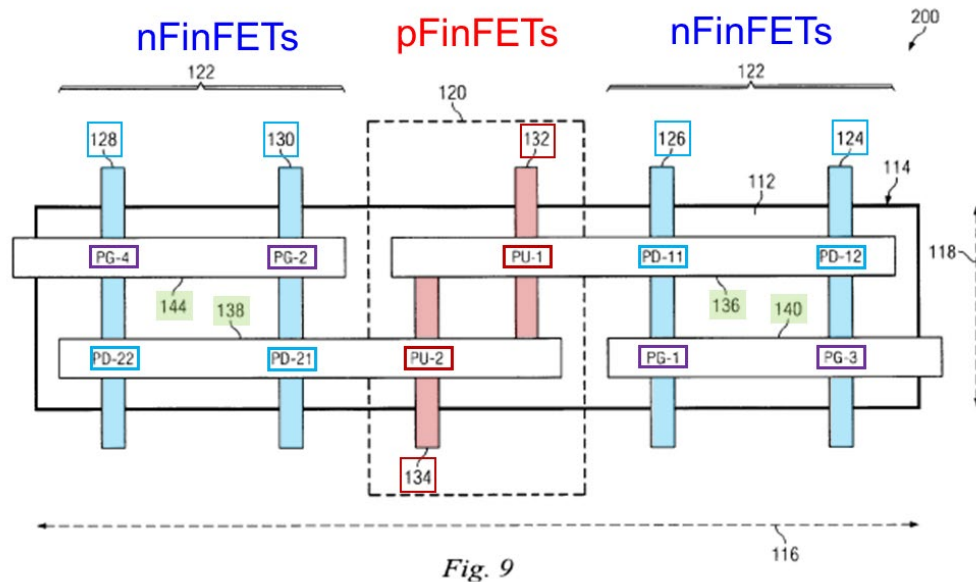
In one embodiment, the SRAM cell 200 is similar to the SRAM cell 100 of FIG. 2 except that the SRAM cell 200 includes four pull-down devices and four pass-gate devices.

¹¹ Liaw discloses that SRAM cell 200 (FIG. 9) is similar to SRAM cell 110 (FIG. 2) except that SRAM cell 200 includes four pull-down devices and four pass-gate devices. EX1008, 10:6-11. Liaw explains that SRAM cell 110 (FIG. 2) is a portion of the SRAM cell 100 (FIG. 1). *Id.*, 3:46-53. A person of ordinary skill in the art would have understood that the disclosures associated with those figures/descriptions are also associated with the features described in connection with SRAM cell 200.

The four pull-down devices are configured in the two cross-coupled inverters and are referred to as PD-11, PD-12, PD-21 and PD-22, respectively. The four pass-gate devices are configured to form a port for data access and are referred to as PG-1, PG-2, PG-3 and PG-4, respectively. In one embodiment, **the pull-down devices, pull-up devices and pass-gate devices are formed of finFETs.**

EX1008, 10:6-17. *See also* 11:16-18 (“pull-up device (PU-1)” and “pull-up device (PU-2)”).

159. Liaw explains that the pull-down device is formed with an nFinFET, the pull-up device formed with a pFinFET, and the pass-gate device formed with an nFinFET. *Id.*, 2:66-3:3; 3:22-26; *see also id.*, 1:61-2:9 (disclosing each of the pull-down and pass-gate transistors is “a n-type fin field-effect transistor (nFinFET)” and each of the pull-up transistors is “a p-type fin field-effect transistor (pFinFET)”), claim 4 (“each of the pull-up devices includes a p-type fin field-effect transistor (pFinFET)..., and each of the pull-down devices and pass-gate devices includes a n-type fin field-effect transistor (nFinFET)...”).



EX1008, FIG. 9 (annotated).

160. As shown in the Figure 9 above, nFinFETs (PG and PD FinFETs) are formed on fin active regions (referred to as “fin” or “fins” hereafter) 124, 126, 128, 130 (blue) and pFinFETs (PU FinFETs) are formed on fins 132 and 134 (red).

Various fin active regions are defined in the semiconductor substrate by isolation features and are isolated from each other by the isolation features. In one embodiment, the SRAM cell 200 includes a first active region 124, a second active region 126, a third active region 128 and a fourth active region 130 formed in the P-well 122. The SRAM cell 200 further includes a fifth active region 132 and a sixth active region 134 formed in the N-well 120. The first to sixth active regions are disposed along

the second dimension and may be extended to multiple cells. In one embodiment, the first to the fourth active regions are extended to 4 or more cells in the second direction 118. In one embodiment, each active region in the P-well includes a pull-down device and a pass-gate device.

In one embodiment, **the first active region 124 includes PD-12 and PG-3**. The source of PG-3 is electrically connected to the drain of the PD-12. Similarly, **the second active region 126 includes PD-11 and PG-1**. The source of PG-1 is electrically connected to the drain of the PD-11. **The third active region 128 includes PD-22 and PG-4**. The source of PG-4 is electrically connected to the drain of PD-22. **The fourth active region 130 includes PD-21 and PG-2**. The source of PG-2 is electrically connected to the drain of the PD-21. **The fifth active region 132 includes the first pull-up device (PU-1) and the sixth active region 134 includes the second pull-up device (PU-2).**

EX1008, 10:60-11:18.

161. Liaw explains “SRAM cell 200 [as shown in Figure 9] is formed in a unit cell region 112 of the semiconductor substrate.” *Id.*, 10:44-46 (“The SRAM cell 200 is formed **on a semiconductor substrate**. The SRAM cell 200 is formed in a unit cell region 112 of the semiconductor substrate.”).

162. Liaw discloses with reference to Figure 7, “a semiconductor structure 180 as a portion of an SRAM cell, such as the SRAM cell 100 of FIG. 1 or the SRAM cell 110 of FIG. 2.” EX1008, 8:15-17. Liaw explains Figure 7 is a sectional view of “a portion of an SRAM device constructed *according to various aspects of the present disclosure in various embodiments.*” *Id.*, 2:41-43. Additionally, Liaw discloses that “SRAM cell 200 [in Figure 9] is similar to the SRAM cell 100 of FIG. 2 except that the SRAM cell 200 includes four pull-down devices and four pass-gate devices” *Id.*, 10:8-11.

163. Thus, in my opinion, a person of ordinary skill in the art would have understood that the process/features disclosed in connection with Figure 7 are attributable to the teachings associated with SRAM cell 200 of Figure 9, and thus Liaw discloses SRAM cell 200 in one aspect, which may be, and is, constructed using the processes/features disclosed associated with Figure 7.

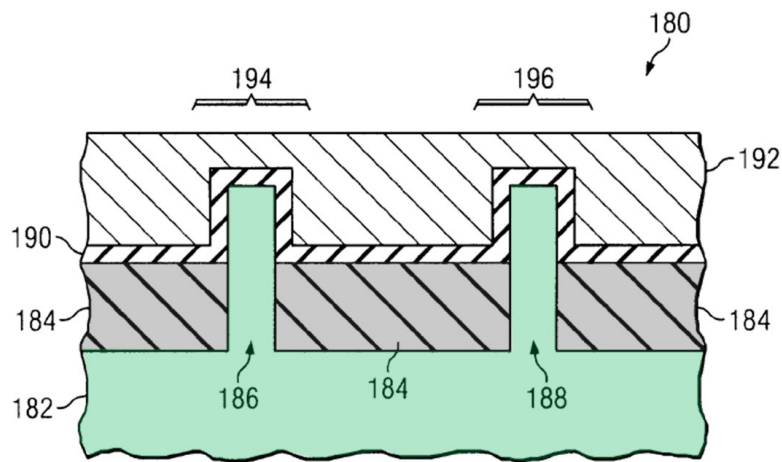


Fig. 7

EX1008, FIG. 7.

164. It is also my opinion that a person of ordinary skill in the art would have been motivated to implement a process similar to the Figure 7 process to produce Figure 9's SRAM cell 200 given that Liaw discloses applying the Figure 7 process to Figure 2's SRAM cell 110 and that SRAM cell 200 is similar to the SRAM cell 100, as discussed above. A person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing the above-discussed modification. Additionally, such a person would have expected to succeed in implementing such a process. This is particularly true because Liaw itself discloses that "SRAM cell 200 [in Figure 9] is similar to the SRAM cell 100 of FIG. 2." EX1008, 10:8-11.

165. As shown in Figure 7 above, semiconductor structure 180 includes substrate 182, e.g., a silicon substrate, and fins 186 and 188.

The semiconductor structure 180 includes a semiconductor substrate 182. The semiconductor substrate 182 includes silicon. Alternatively, the substrate includes germanium, silicon germanium or other proper semiconductor materials. **The semiconductor substrate 182 includes various isolation features 184, such as shallow trench isolation (STI), are formed in the substrate to separate various devices.** The semiconductor substrate also includes various doped regions such as n-well and p-wells. **The semiconductor structure 180 includes various fin active regions 186 and 188.**

EX1008, 8:17-27.

166. The FIG. 7 structure may be formed by “forming trenches in...substrate 182.” EX1008, 8:15-31. Thus, a person of ordinary skill in the art would have understood that fins 186 and 188 are formed by etching/removing the substrate material in certain regions, where regions between the trenches result in fins 186 and 188.

In FIG. 24, the substrate 10 is etched to form fins 12. **The fins 12 may be formed by depositing a mask layer over the substrate 10 and depositing a photoresist over the mask layer.** The photoresist can be patterned into the fin pattern by appropriate exposure to light. **The fin pattern**

is transferred to the mask layer by an etch, and the fin pattern is transferred from the mask layer to the substrate 10 by an etch. If an SOI substrate is used, the etch may be to a depth to the insulator or to a depth above or below the insulator.

In FIG. 25, **isolation structures 14 are formed between fins 12.** An insulating layer, such as a high density plasma oxide, can be deposited over the substrate 10 and fins 12 and etched back to form the isolation structures 14, according to acceptable deposition and lithography techniques. A person having ordinary skill in the art will readily understand other methods by which the fins 12 can be formed, and these methods are contemplated by embodiments. For example, an insulating layer can be formed over a substrate, trenches can be formed in the insulating layer exposing the substrate, and fins can be epitaxially grown from the substrate through the fins.

EX1014, 15:30-57. Additional features are formed on the fins of semiconductor structure 180 to form FinFETs, as shown in Figure 7.

Various gates are further formed on the fin active regions. A gate feature includes a gate dielectric layer 190 (such as silicon oxide) **and a gate electrode 192** (such as doped polysilicon) **disposed on the gate dielectric layer**

190. In another embodiment, the gate feature alternatively or additionally includes other proper materials for circuit performance and manufacturing integration...**the semiconductor substrate 180 includes a first region 194 for one or more FinFETs and a second region 196 for one or more FinFETs. In one example, the active region 186 is the third active region 132 in the n-well 120 of FIG. 2 and the active region 188 is the first active region 126 in the p-well 122 of FIG. 2.**

EX1008, 8:56-9:10.

167. According to Liaw, “SRAM cell 200 [in Figure 9] is similar to the SRAM cell 100 of FIG. 2 except that the SRAM cell 200 includes four pull-down devices and four pass-gate devices” *Id.*, 10:8-11. Thus, a person of ordinary skill in the art would have understood the process/features disclosed in connection with Figure 7 are attributable to the teachings associated with SRAM cell 200 of Figure 9, and thus Liaw discloses SRAM cell 200 may be, and is, constructed using the processes/features associated with Figure 7, including that the fins of SRAM cell 200 are formed by etching/removing the substrate material.

168. Accordingly, Liaw discloses a “semiconductor structure” (e.g., as shown in Figure 9 as modified having the fin structure shown in Figure 7) “for

forming FinFETs” (as recited in preamble [1.pre] and [9.pre]) and “forming FinFET” (as recited in preamble [15.pre]).

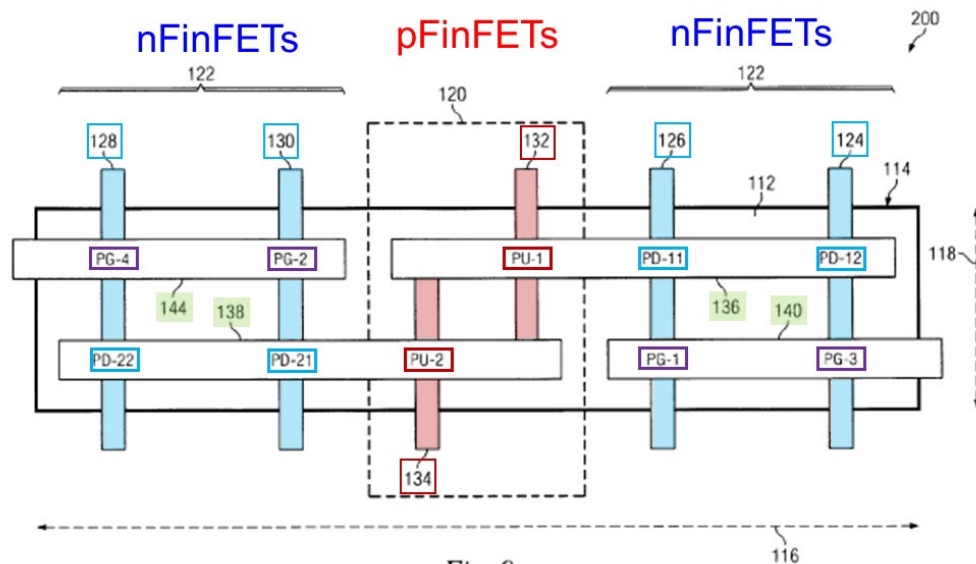
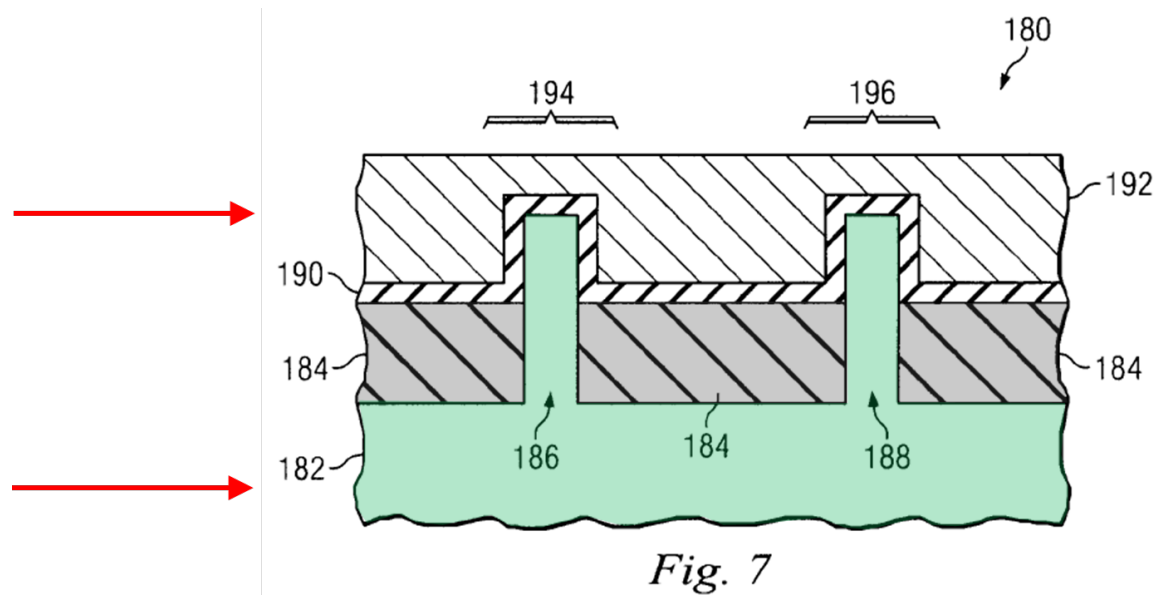


Fig. 9

EX1008, FIG. 9 (annotated).

- (ii) [1.a]/[9.a]/[15.a] “a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;”

169. It is my opinion that Liaw discloses and/or suggests these limitations. Liaw discloses substrate 182 is a “semiconductor substrate,” e.g., a silicon substrate. EX1008, 8:15-19 (“The semiconductor structure 180 includes a **semiconductor substrate 182**. The semiconductor substrate 182 includes **silicon**.”).



EX1008, FIG. 7 (annotated).

170. As I have discussed for the preambles in Section IX.F.1(i), structure 180 is formed on semiconductor substrate 182 by removing/etching the substrate material. Thus, Liaw discloses that “a top portion of the semiconductor substrate,” e.g., as shown between the red lines, “comprises a semiconductor material.” Additionally, Liaw discloses “substrate 182 includes *silicon*,” and “[a]lternatively, the substrate includes *germanium, silicon germanium or other proper semiconductor materials*.” EX1008, 8:17-19 (“The semiconductor structure 180 includes a **semiconductor substrate 182**. The semiconductor substrate 182 includes **silicon**.”).

171. A person of ordinary skill in the art would have understood that Liaw discloses that semiconductor substrate 182 may be entirely made of silicon, i.e., a bulk silicon substrate, without including “other...semiconductor materials,” confirming the top portion of the substrate comprises a semiconductor material, i.e., silicon. Thus, for the reasons I have provided above, and those for the preambles (see Section IX.F.1(i)), the modified Figure 9 structure (in view of the Figure 7 teachings of Liaw) would have predictably included a semiconductor substrate as claimed in limitations 1[a]/9[a]/15[a].

(iii) **[1.b] “a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material”**

[9.b] “a plurality of odd fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other”

[15.b] “a plurality of first fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and”

172. In my opinion, Liaw discloses and/or suggests these limitations. As discussed for the preambles and as shown in Figure 7, fins 186 and 188 on substrate

182 are formed of the semiconductor substrate material. As seen from Figure 7, Liaw's fins 186 and 188 protrude from substrate 182. Moreover, Liaw explains "substrate 180 includes a first region 194 for one or more FinFETs and a second region 196 for one or more FinFETs." EX1008, 9:4-10. Thus, Liaw discloses "fins of the FinFETs on the semiconductor substrate...being formed of the semiconductor material" recited in limitations [1.b]/[9.b]/[15.b].

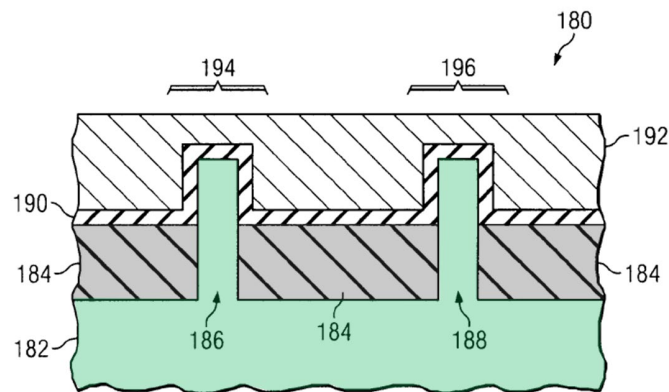


Fig. 7

EX1008, FIG. 7 (annotated).

173. Liaw discloses the fins are "defined from the semiconductor substrate" as recited in limitation [1.b]. As I have discussed for the preambles in Section IX.F.1(i), Liaw's fins are formed by etching/removing the semiconductor substrate material in certain regions, where regions between the trenches result in the fins.

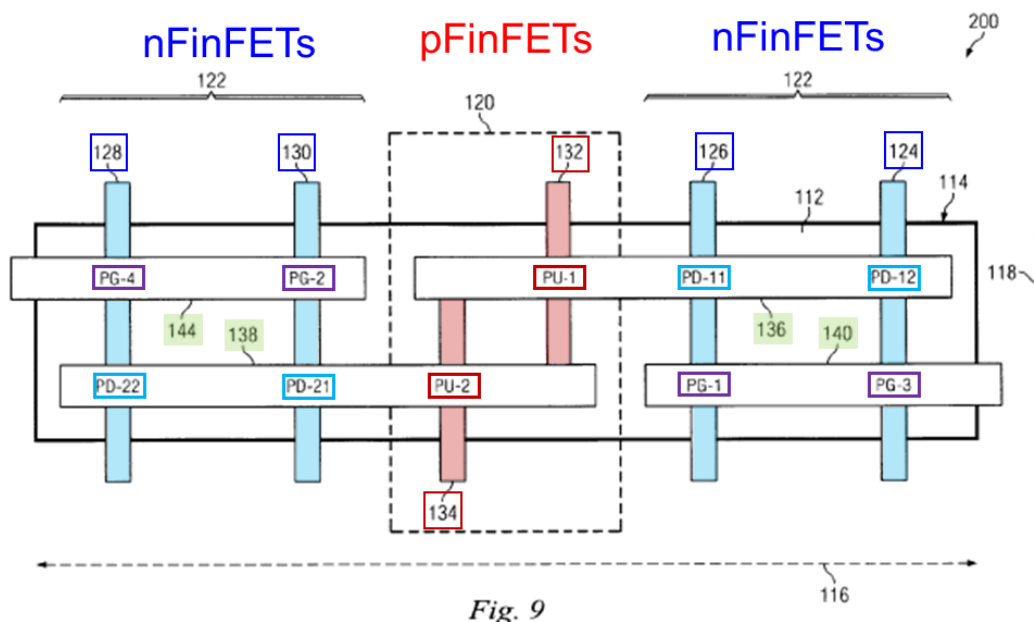
Thus, the fins are defined in certain locations of semiconductor substrate 182 (“the semiconductor substrate”).

174. Per my discussion for the preambles in Section IX.F.1(i), a person of ordinary skill in the art would have understood that SRAM cell 200 (Figure 9), may be constructed using the processes/features disclosed associated with Figure 7. Liaw’s Figure 9 shows six fins, where each of fins 124, 126, 128, 130 (blue) is associated with two nFinFETs (PG and PD FinFETs) and each of 132 and 134 (red) is associated with one pFinFET (PU FinFET).

Various fin active regions are defined in the semiconductor substrate by isolation features and are isolated from each other by the isolation features. In one embodiment, **the SRAM cell 200 includes a first active region 124, a second active region 126, a third active region 128 and a fourth active region 130 formed in the P-well 122.** The SRAM cell 200 further includes **a fifth active region 132 and a sixth active region 134 formed in the N-well 120.** The first to sixth active regions are disposed along the second dimension and may be extended to multiple cells. In one embodiment, the first to the fourth active regions are extended to 4 or more cells in the second direction 118. In one embodiment, each active region in the P-well includes a pull-down device and a pass-gate device.

In one embodiment, **the first active region 124 includes PD-12 and PG-3**. The source of PG-3 is electrically connected to the drain of the PD-12. Similarly, **the second active region 126 includes PD-11 and PG-1**. The source of PG-1 is electrically connected to the drain of the PD-11. **The third active region 128 includes PD-22 and PG-4**. The source of PG-4 is electrically connected to the drain of PD-22. **The fourth active region 130 includes PD-21 and PG-2**. The source of PG-2 is electrically connected to the drain of the PD-21. **The fifth active region 132 includes the first pull-up device (PU-1) and the sixth active region 134 includes the second pull-up device (PU-2).**

EX1008, 10:60-11:18.



EX1008, FIG. 9 (annotated).

175. As I discussed above in Section VIII, I have been asked to apply certain assumptions regarding limitations associated with the arrangement of the “odd” or “first” fins and “even” or “second” fins.

176. Liaw’s SRAM cell 200 (FIG. 9) discloses three groups of fins, e.g., Groups 1-3, where Groups 1 and 3 each corresponds to “a plurality of **odd** [or **first**] fins of the FinFETs” and Group 2 corresponds to “a plurality of **even** [or **second**] fins of the FinFETs” of claims 1/9/15 *under the assumed interpretation discussed in Section VIII*. (See my discussion in relation to limitations [1.c], [9.c], [15.c] discussed in the next section).

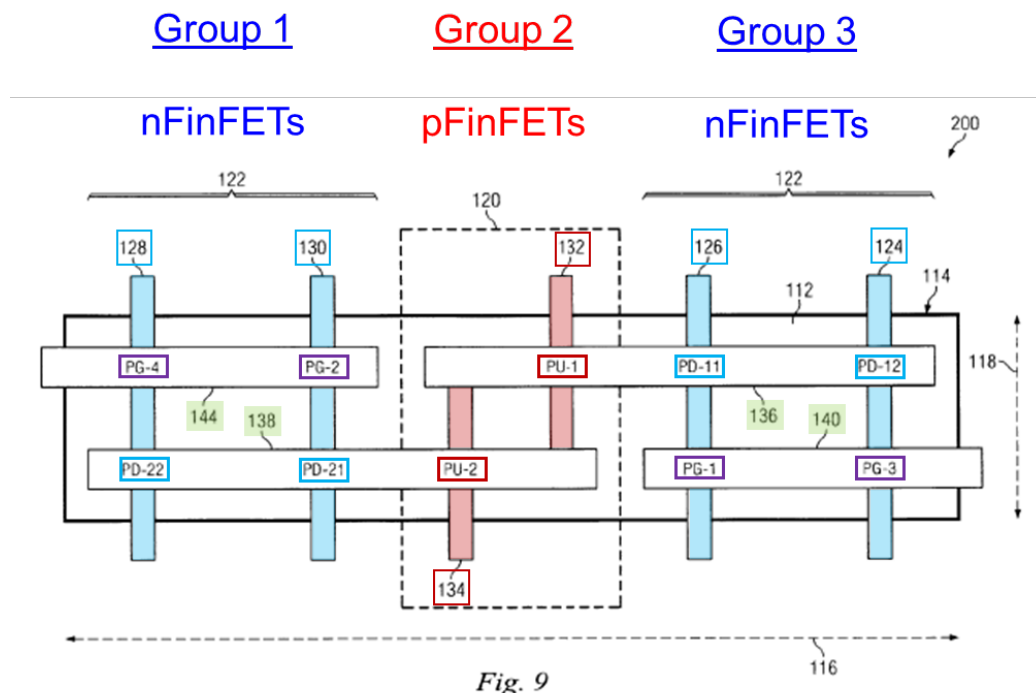


Fig. 9

EX1008, FIG.9 (annotated).

177. Groups 1-3 fins are on the semiconductor substrate (“on the semiconductor substrate” as claimed). EX1008, 10:44-45 (“The SRAM cell 200 is formed **on a semiconductor substrate.**”) As I have discussed for preambles in Section IX.F.1(i) above, SRAM cell 200 (Figure 9), may be formed by etching/removing the substrate. Thus, Groups 1 and 3 fins are “defined from the semiconductor substrate” as recited in limitation [1.b] and “formed of the semiconductor material” comprised in the top portion of the semiconductor substrate, as recited in limitations [1.b], [9.b] and [15.b]. *See also* discussions for

limitations [1.a]/[9.a]/[15.a] in Section IX.F.1(ii). Given that the fins are formed of the substrate by etching/removing the substrate material, Groups 1 and 3 fins “and the semiconductor substrate are in direct contact with each other” ([1.b]/[9.b]/[15.b]).

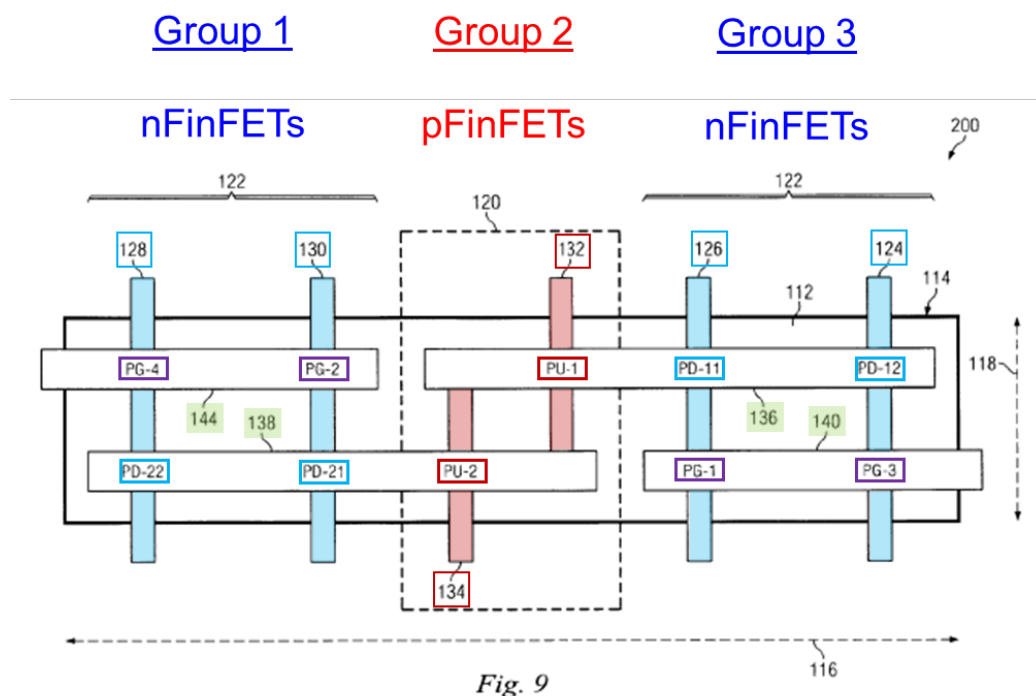
- (iv) **[1.c] “a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.”**

[9.c] “a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.”

[15.c] “a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.”

178. It is my opinion that Liaw in view of Basker discloses and/or suggests these limitations. As discussed for limitations [1.b]/[9.b]/[15.b] in Section IX.F.1(iii), Liaw’s Groups 1-3 fins are on the semiconductor substrate, including

Group 2 fins (corresponding to “a plurality of even [or second] fins of the FinFETs” of claims 1/9/15 *under the assumed interpretation that I discussed in the preceding Section VIII*, are “on the semiconductor substrate,” as claimed. EX1008, 10:44-45 (“The SRAM cell 200 is formed on a **semiconductor substrate**.”).



EX1008, FIG. 9 (annotated).

179. As shown in Figure 9, Group 2 fins reside between Groups 1 and 3 fins (“between the odd fins of the FinFETs” *under the assumed interpretation discussed in Section VIII*, as required by limitations [1.c] and [9.c]. Likewise, Liaw discloses “each of the second fins of the FinFETs is located between two first fins of the

FinFETs,” as recited in limitation [15.c] *under the assumed interpretation discussed in Section VIII*, given that each of the fins in Group 2 is located between two fins, each of Groups 1 and 3.

180. While Liaw does not expressly disclose “even [or second] fins of the FinFETs...being [or are] different from the odd [or first] fins of the FinFETs in at least one of width and material” (limitations [1.c]/[9.c]/[15.c]) *under the assumed interpretation discussed in Section VIII*, a person of ordinary skill in the art would have been motivated to implement such features in a structure like as disclosed/suggested by Liaw in view of Basker.

181. Like Liaw, Basker discloses FinFETs on a bulk silicon substrate (EX1006, [0020] (“forming a high dielectric constant (high-k)-metal gate **fin field effect transistor (FET)**”), [0025] (“**bulk substrate** that may include...**monocrystalline silicon**”)) and an nFinFET that “is formed on a fin made from a substrate material” (*id.*, [0020]), i.e., silicon fin (*id.*, [0038] (“Si fin 20”)), and the fins are formed by using an etch process (*id.*, [0025]-[0029] (disclosing “**Liner 18 acts as an etch mask to open up layer 16**. Layer 16 provides a semiconductor material from which FETs may be formed”))).

182. Moreover, both Liaw and Basker disclose using high-k metal gate for the transistors' gate. EX1006, [0020] (“a high dielectric constant **(high-k)-metal gate**”), [0034]; EX1008, 3:35-38 (“the various nFinFETs and pFinFETs are formed using **high-k metal gate technology** so the gate stacks includes a high-k dielectric material layer for gate dielectric and one or more metals for gate electrode”), 8:67-9:3 (“For a **gate stack including high-k dielectric material and metal**, the gate can be formed by a gate-last process or a high-k-last process (a complete gate-last process).”). Thus, a person of ordinary skill in the art would have been motivated to consider Basker's teachings when implementing semiconductor devices like those of Liaw.

183. Basker additionally discloses improving the pFinFET performance by adding Ge to silicon fins to **form SiGe fins**.

The device and method provide a p-type field effect transistor (pFET) within a target threshold voltage. **An n-type field effect transistor (nFET) is formed on a fin made from a substrate material.** A corresponding pFET is formed on a fin which is processed by pushing or diffusing an element into the substrate material to form a new structure. In one example, the substrate includes silicon which is employed to form the fin for the nFET. In this example, **a fin for the pFET**

includes silicon as well, but Germanium (Ge) is pushed into silicon to form a SiGe fin for the formation of the pFET. The pFET is formed by, e.g., oxidation condensation (to push Ge into a Si fin during oxidation).

EX1006, [0020].

In this way, the pFET finFET with a SiGe body achieves a corrected threshold voltage (V_t) since the dimensions of the fin are maintained and an advantageous strain is imparted to the fin. **The SiGe and associated strain results from the Ge within a silicon matrix. The strain improves pFET performance because intermixing Ge into Si requires strain relaxation to open up the spaces in the silicon for larger Ge atoms.** This is much easier to do in a direction normal to a carrier transport direction. This is an ideal combination: comparable V_t , strain, and a (110) surface for the pFET finFET. In fact in many useful integrated circuit components, such as logic gates and in particular NAND gates, the pFET can be made to especially gain from these advantageous effects.

Id., [0021]. A person of ordinary skill in the art would have been motivated to form SiGe fins for pFinFETs in a structure las disclosed/suggested by Liaw in view of Basker's teaching.

184. **First**, a person of ordinary skill in the art would have understood there has been a general trend at the relevant time to include Ge/SiGe into the transistor's channel, which traditionally has been made of silicon. EX1025, 1. In fact, it was known that "SiGe channel [FinFET] is an attractive replacement" of Si channel pFinFETs. EX1026, 1 ("**SiGe channel FINFET is an attractive replacement**"); *see also* EX1030, 2; EX1031, 1 (explaining that pFinFETs having SiGe channels would be "**viable candidates for future high-speed applications**"); Section V.B. Additionally, a person of ordinary skill in the art would have understood that SiGe fins improve hole mobility for pFinFETs and thus improve current drive of the transistors and speed of transistors' operation. EX1016, 1-2, 4; EX1017, 1; EX1018, 1; Section V.B.

185. **Second**, as Basker itself explained, it is "advantageous" to impart strain to the fin, and the strain caused by adding Ge to the silicon fins "improves pFET performance." EX1006, [0021], [0038].

186. **Third**, Basker explains using a silicon fin for an nFinFET and using a SiGe fin for a pFinFET allows the use of "the same gate dielectric...and the same gate conductor...." (EX1006, [0038]), which would have simplified the fabrication processes and reduced cost for making ICs/SRAM. EX1023, [0008] ("fabricating

transistors having **gate electrodes made of two different materials is prohibitively expensive**”), [0016] (“Engineering the band gap of the semiconductor transistor channels rather than engineering the work function of the transistor gate metal for the individual pMOS and nMOS devices **avoids the manufacturing difficulties** associated with depositing and interconnecting two separate gate metals in a dual-metal gate process.”), [0027] (“the same material is used to form the gate electrode...for pMOS device...and nMOS device.... In this manner, CMOS device **fabrication can be greatly simplified....**”); Section V.B.

187. It is my opinion that a person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing the Liaw-Basker combination. Additionally, such a person would have expected to succeed in implementing the feature. Indeed, Basker itself discloses adding Ge to the silicon fin results in “**an ideal combination**” of beneficial features. EX1006, [0021]. Basker explains the disclosed features may be applied to many useful IC components which, as a person of ordinary skill in the art would have understood, include SRAM (e.g., those disclosed in Liaw). *Id.*, [0021] (“in many useful integrated circuit components...the pFET can be made to especially gain from these advantageous effects”).

188. The modification of Liaw in view of Basker's teachings would have involved applications of known technologies (e.g., known use of SiGe for pFinFETs) according to known methods (e.g., known method of forming SiGe) to yield the predictable result of improved pFinFETs and other benefits discussed above in the Liaw-Basker combination.

189. Additionally, as discussed for claims 3/11/17 in Section IX.A.2, Basker discloses forming SiGe fins by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22. EX1006, [0005], [0020]-[0021], [0032], [0041], claim 1. Since the resulting SiGe fins incorporate the epitaxially deposited material, the resulting SiGe fins "comprise an epitaxy material." Also, a person of ordinary skill in the art would have understood that Basker's SiGe fin formation results in epitaxy material and thus the resulting SiGe fins "comprise an epitaxy material." EX1013, 2; EX1038, 3-4. Additionally, a person of ordinary skill in the art would have known that SiGe fins could also be formed using e.g., CVD and MBE, and would have been motivated to use any of them. *See, e.g.*, EX1039, 4:23-5:9. Thus, Basker discloses and/or suggests SiGe "fins of the FinFETs comprise an epitaxy material."

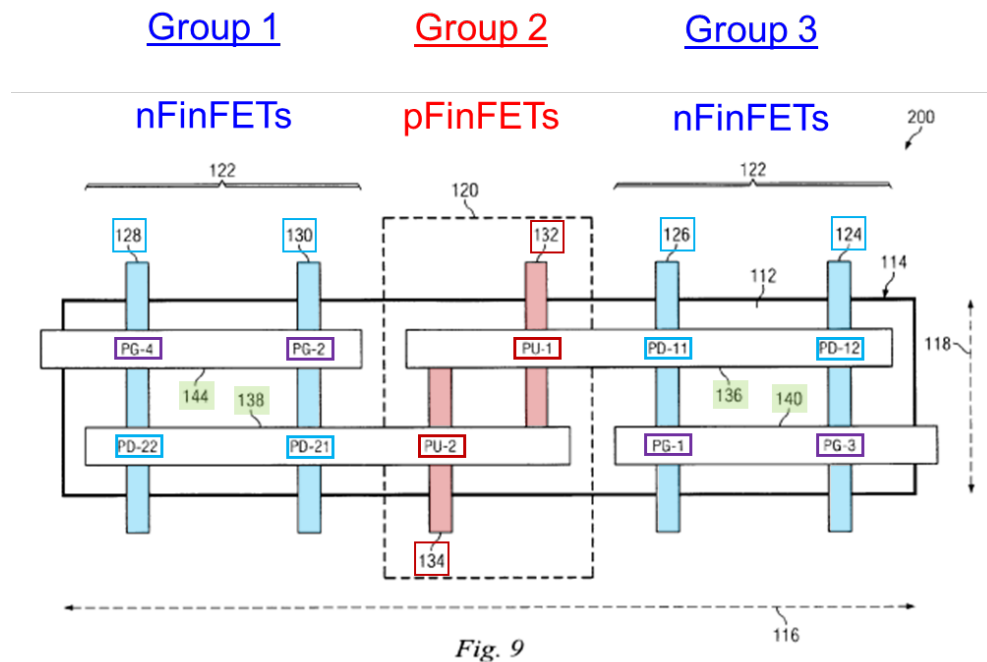
190. Additionally, considering the discussion above, a person of ordinary skill in the art would have been motivated to form SiGe fins for pFinFETs

“compris[ing] an epitaxy material” in the Liaw-Basker combination. Basker explains “[i]t is advantageous to epitaxially grow the donor layer...[comprising Ge]” using the disclosed process as it “ensure[s] good contact between the donor layer...and the sidewalls of fin...,” allowing uniform and high-quality epitaxial growth. EX1006, [0031].

191. A person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Liaw-Basker combination. Liaw and Basker share several similar features/processes, e.g., both form FinFETs on a silicon substrate, the nFinFETs are formed from the substrate material, and both use high-k metal gate for the transistors’ gate. Combining Liaw with Basker would have involved applications of known technologies (e.g., known use of SiGe for pFinFETs) according to known methods (e.g., known method of forming SiGe) to yield the predictable result of improved pFinFETs and other benefits discussed above in the Liaw-Basker combination.

192. Given that the Liaw-Basker combination discloses and/or suggests using **Silicon** fins for nFinFETs (EX1008, 8:15-31, 9:4-10) and **SiGe** fins for pFinFETs, the Liaw-Basker combination discloses “**even** [or **second**] fins of the

FinFETs...being different from the **odd** [or **first**] fins of the FinFETs in at least one of width and **material**” as recited in claims 1/9/15 *under the assumed interpretation discussed in Section VIII.*



EX1008, FIG. 9 (annotated).

2. Claims 3, 11, and 17

(i) 3. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material.”

11. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise an epitaxy material.”

17. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise an

epitaxy material.”

193. In my opinion, the Liaw-Basker combination discloses and/or suggests these limitations.

194. As discussed for claim [1.c]/[9.c]/[15.c] in Section IX.F.1(iv), a person of ordinary skill in the art would have been motivated to use SiGe fins for pFinFETs. Further, as discussed for claims 3/11/17 in Section IX.A.2, Basker discloses forming SiGe fins by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22. EX1006, [0005], [0031]-[0032], [0041]; *see also id.*, [0020]-[0021], claim 1. As discussed above, a person of ordinary skill in the art would have been motivated to form SiGe fins for pFinFETs of Liaw “compris[ing] an epitaxy material” in view Basker.

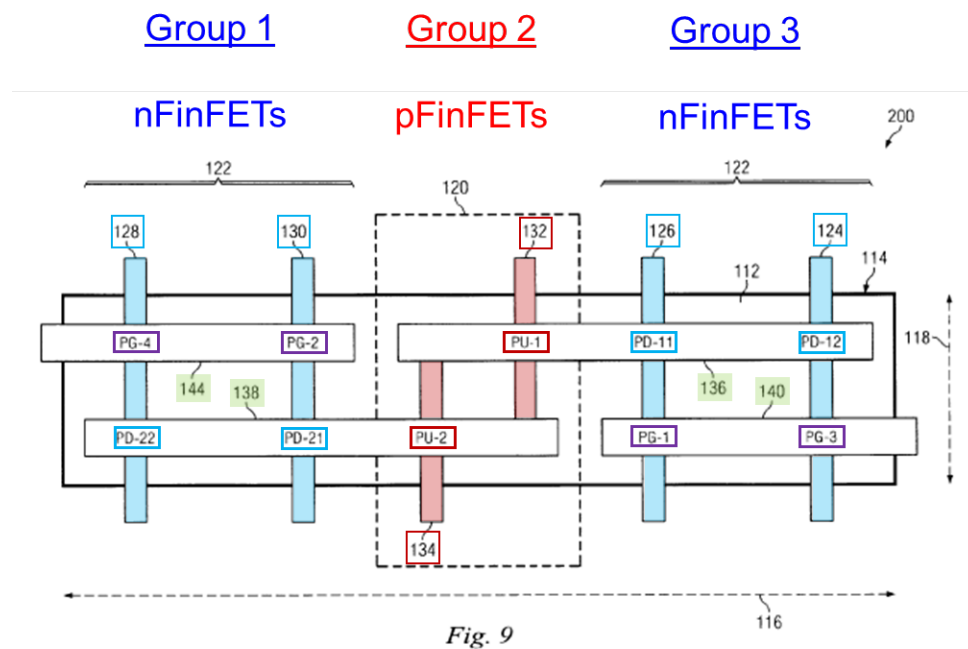
195. As discussed for limitations [1.c]/[9.c]/[15.c], a person of ordinary skill in the art would have been motivated to consider Basker’s teachings when implementing devices similar to those of Liaw. Moreover, as discussed, a person of ordinary skill in the art would have been motivated to implement SiGe fins for pFinFETs in view of Basker’s teaching. Further, such a person would have expected to succeed in implementing the feature.

196. Additionally, a person of ordinary skill in the art would have been motivated to form SiGe fins for pFinFETs “compris[ing] an epitaxy material” in the Liaw-Basker combination. Basker explains “[i]t is **advantageous** to epitaxially grow the donor layer...[comprising Ge]” using the disclosed process as it “ensure[s] good contact between the donor layer...and the sidewalls of fin...,” allowing uniform and high-quality epitaxial growth. EX1006, [0031].

197. In my opinion, a person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing the above-discussed Liaw-Basker combination. Additionally, such a person would have expected to succeed in implementing the combination.

198. Furthermore, Liaw and Basker share several similar features/processes, e.g., both form FinFETs on a silicon substrate, the nFinFETs are formed from the substrate material, and both use high-k metal gate for the transistors’ gate. Combining Liaw with Basker would have involved applications of known technologies (e.g., known use of SiGe for pFinFETs) according to known methods (e.g., known method of forming SiGe) to yield the predictable result of improved pFinFETs and other benefits discussed above in the Liaw-Basker combination.

199. Accordingly, a person of ordinary skill in the art would have been motivated to form pFinFETs (as disclosed in Liaw, e.g., PU-1 and PU-2 of Group 2 fins in Figure 9 below) having SiGe fins that “comprise an epitaxy material” (as taught in Basker).



EX1008, FIG. 9 (annotated).

3. Claims 4, 12, and 18

- (i) 4. “The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.”**

12. “The semiconductor structure of claim 11, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.”

18. “The semiconductor structure of claim 17, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.”

200. In my opinion, the Liaw-Basker combination discloses these limitations. Per my discussions for limitations [1.b]/[9.b]/[15.b], Liaw discloses “the odd [or first] fins of the FinFETs **comprise Si**” because the Groups 1 and 3 fins are formed from the silicon substrate. As I have discussed for claims 3, 11, and 17, Liaw in view of Basker discloses forming **SiGe fins** for pFinFETs, i.e., the Group 2 fins or the “even [or second] fins of the FinFETs” comprise SiGe. *See* Section IX.F.2. In my opinion, such features would have been likewise included in the Liaw-Basker combination discussed above.

4. Claims 5, 13, and 19

(i) 5. “The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.”

13. “The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si.”

19. “The semiconductor structure of claim 15, wherein the first fins of the FinFETs comprise Si.”

201. It is my opinion that the Liaw-Basker combination discloses and/or suggests these limitations for the same reasons as discussed for claims 4, 12, and 18. *See* Section IX.F.3.

5. Claims 6, 14, and 20

(i) **6. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.”**

14. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise SiC or SiGe.”

20. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise SiC or SiGe.”

202. In my opinion, the Liaw-Basker combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18. See my discussion above in Section IX.F.3.

6. Claim 7

(i) **7. “The semiconductor structure of claim 1, wherein the odd fins of the FinFETs are electrically connected to the semiconductor substrate.”**

203. It is my opinion that the Liaw-Basker combination discloses this limitation. As I have discussed for limitations [1.b]/[9.b]/[15.b], Groups 1 and 3 fins (“the odd fins of the FinFETs” *under the assumed interpretation discussed in Section VIII* are defined from and formed of *silicon* substrate 182. Consistent with Figure 7 below, Groups 1 and 3 fins are connected to silicon substrate 1. EX1008, 8:15-31.

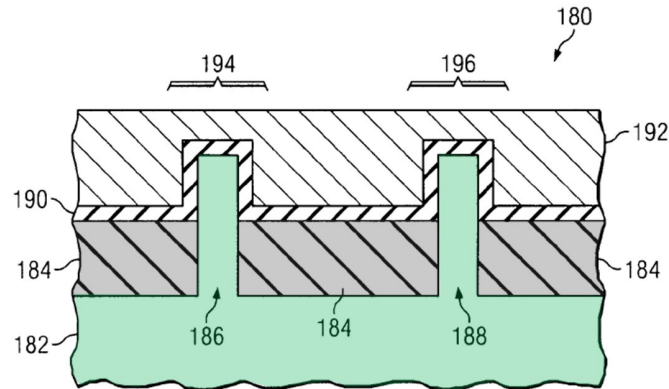


Fig. 7

EX1008, FIG. 7 (annotated).

204. A person of ordinary skill in the art would have understood that, given Groups 1 and 3 fins and the substrate are connected and both are the same semiconductor material, i.e., silicon, these fins and the substrate are electrically connected. Accordingly, the Liaw-Basker combination I have discussed above for claim 1 (Section IX.F.1) likewise discloses the features of claim 7. *Id.*

7. Claim 8

- (i) **8. “The semiconductor structure of claim 1, wherein the semiconductor substrate is a single layer structure.”**

205. It is my opinion that the Liaw-Basker combination discloses and/or suggests this limitation. As I have discussed for limitations [1.a]/[9.a]/[15.a], semiconductor substrate 182 may be a bulk silicon substrate (EX1008, 8:17-19,

9:15-25) and thus the entire substrate is formed of “a single layer structure” of semiconductor material, i.e. silicon. In my opinion, such features would have been included in the Liaw-Basker combination discussed above in Section IX.F.1 for claim 1.

G. Liaw in View of Basker and Yu Discloses and/or Suggests Claims 2, 10, and 16

1. Claims 2, 10, and 16

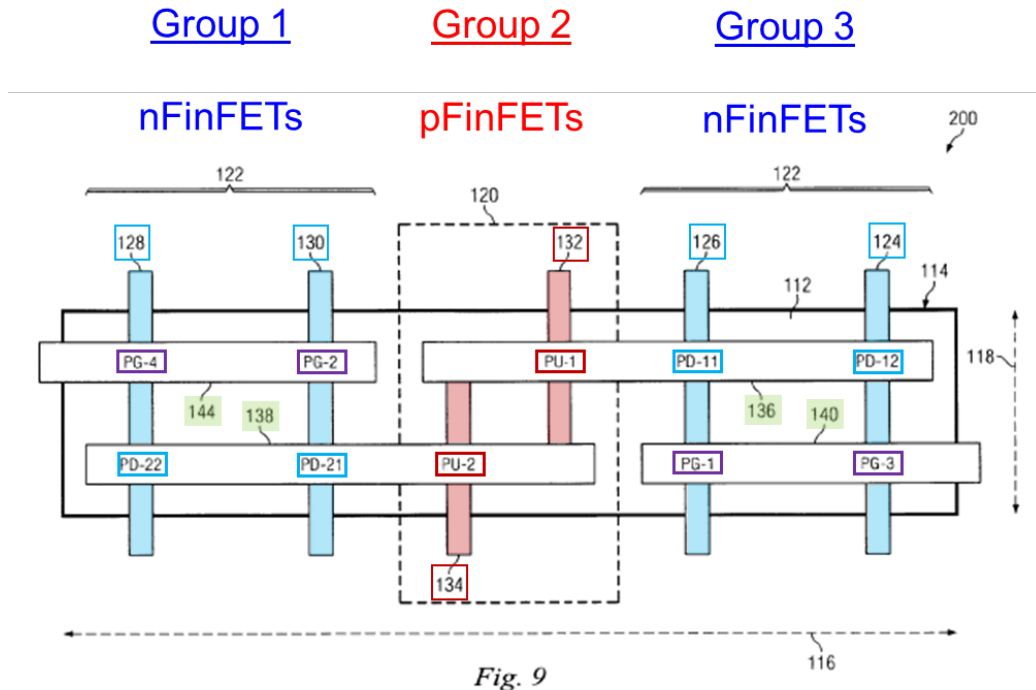
(i) 2. “The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.”

10. “The semiconductor structure of claim 9, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.”

16. “The semiconductor structure of claim 15, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.”

206. It is my opinion that the Liaw-Basker combination in view of Yu discloses and/or suggests these limitations.

207. As I have discussed for limitations [1.b]/[9.b]/[15.b] in Section IX.F, Liaw (including as modified in view of Basker, as discussed for limitations [1.c]/[9.c]/[15.c]) discloses, as shown in Figure 9 below, three groups of fins. See my discussion above in Section IX.F.1(iii).



EX1008, FIG. 9 (annotated).

208. The Liaw-Basker combination does not expressly disclose “the **even** fins...are further different from the **odd** fins...**in height**” or “the **second** fins...are further different from the **first** fins...**in height**” *under the assumed interpretation discussed in Section VIII*. Nevertheless, a person of ordinary skill in the art would have been motivated to implement such a structure in view of Yu’s teachings.

209. Like Liaw, Yu discloses fabrication of FinFETs for use in IC (EX1010, [0001] (“This invention relates generally to semiconductor devices, and more particularly to **Fin field effect transistors (FinFET).**”), [0002] (“Transistors are key

components of **modern integrated circuits**”), [0019] (“semiconductor chip”). Also like Liaw, Yu discloses forming fins of the FinFETs by etching a bulk silicon substrate. *Id.*, [0028] (“The embodiments discussed in preceding paragraphs are **formed on bulk semiconductor substrate.**”), [0020] (“semiconductor substrate 20 includes silicon”), [0021]-[0024] (describing with reference to Figures 2-5 that the substrate is etched to form fin structures).

An optional pad layer 22 and mask layer 24 are formed on semiconductor substrate 20. Pad layer 22 is preferably a thin film formed through a thermal process, and thus comprising silicon oxide. It is used to buffer semiconductor substrate 20 and mask layer 24 so that less stress is generated. **Pad layer 22 may also act as an etch stop layer for etching the subsequently formed mask layer 24.** In the preferred embodiment, mask layer 24 is formed of silicon nitride using low-pressure chemical vapor deposition (LPCVD). In other embodiments, mask layer 24 is formed by thermal nitridation of silicon, plasma enhanced chemical vapor deposition (PECVD) or plasma anodic nitridation using nitrogen-hydrogen.

EX1010, [0021].

Photoresist 26 is formed on mask layer 24, and is then patterned, forming openings 28 in photoresist 26. The

patterned photoresist 26 includes a photoresist strip 30. If viewed from the top of the structure shown in FIG. 2, photoresist strip 30 may be a rectangular-shaped strip isolated from other portions of photoresist 26 by openings 28. Width W1 of photoresist strip 30 preferably equals to the desired width of a fin of a FinFET. In an exemplary embodiment, width W1 is between about 15 nm and about 60 nm.

Id., [0022].

In FIG. 3, **mask layer 24 and pad layer 22 are etched through openings 28**, exposing underlying semiconductor substrate 20. **The exposed semiconductor substrate 20 is then etched, forming trenches 32 in semiconductor substrate 20.** In an exemplary embodiment, depth D1 of trenches 32 is substantially close to the desired height of the fin of the desired FinFET. Trenches 32 encircle fin 48 therebetween. Photoresist 26 is then removed.

Id., [0023].

FIG. 4 illustrates the formation and patterning of photoresist 34, which defines the pattern for forming another fin. Openings 36 are formed in photoresist 34 and define photoresist strip 38, which is surrounded by openings 36. **Mask layer 24, pad layer 22 and semiconductor substrate 20 exposed through openings 36 are then etched**

sequentially, forming trenches 40 in semiconductor substrate 20, as is shown in FIG. 5. Preferably, trenches 40 have depth D2 different from depth D1 of trenches 32. In an exemplary embodiment, trench depth D2 is greater than about 130 percent of trench depth D1, and may even be greater than about 150 percent of trench depth D1. Trenches 40 define fin 50 therebetween.

Id., [0024].

210. Thus, a person of ordinary skill in the art would have been motivated to consider Yu's teachings when implementing structure similar to those disclosed in the Liaw-Basker combination.

211. As I have discussed in Section IX.B.1, Yu discloses forming "customized fin heights...so that the FinFETs may have customized performance." EX1010, [0010]; *see above* Section IX.B.1; *see also* EX1010, [0023]-[0024] (disclosing process of forming fins of different heights), [0025]-[0027], [0029].

212. In view of Yu's teaching, including customizing "semiconductor fins with different heights on a same semiconductor chip" (EX1010, [0010], [0019]), a person of ordinary skill in the art would have been motivated to customize the fin heights of the FinFETs in an IC chip, e.g., those in the SRAM cells disclosed/suggested by the Liaw-Basker combination. Section IX.F.1. As discussed

for Section IX.B.1, performance of the FinFETs, e.g., static noise margin depends on the dimensions of the FinFETs used to form the cell. Section IX.B.1. Also discussed therein, the static noise margin depends on the pull up ratio (PR) of the SRAM cell, where PR a parameter for optimizing SRAM performance. For example, it has been reported that PR should be in the range of 3 to 4 for SRAM cells to be functional. Section IX.B.1; EX1033, 1-3 (“pull-up ratio should be in...3-4...otherwise data will be [destroyed]”). Accordingly, a person of ordinary skill in the art would have been motivated to customize the fin heights to, e.g., increase W_{pFET} and/or to reduce W_{nFET} (and/or to reduce L_{pFET} and/or to increase L_{nFET}) to achieve the desired PR range in the Liaw-Basker combination I have discussed above.

213. As discussed above, given that the channel width W is a function of the fin height, a person of ordinary skill in the art, guided by Yu’s teachings/suggestions and their state of art knowledge, would have been motivated to customize fin heights to, for example, increase W_{pFET} and/or to reduce W_{nFET} in an SRAM cell in the above-discussed Liaw-Basker combination to achieve the desired PR range. This would have resulted in the height of the pFinFET’s fins (“even” or “second” fins)

being different from the height of the nFinFET fins (“odd” or “first” fins) in the modified combination.

214. A person of ordinary skill in the art would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Liaw-Basker-Yu combination, particularly given that Liaw and Yu shared similar fin fabrication process steps. Combining Liaw, Basker, and Yu would have involved applications of known technologies (e.g., known process to etch a substrate to form fins of FinFETs) according to known methods (e.g., known method of forming trenches of different depths on a substrate to create height differences between fins) to yield the predictable result of a functional SRAM cell having, e.g., a proper pull-up ratio (PR) and thus static noise margin.

215. As I have discussed for Section IX.B, adjusting/customizing the height difference of the nFinFET and pFinFETs in an SRAM cell would have been a matter of routine optimization an SRAM cell’s parameter because it affects SRAM’s performance, e.g., the static noise margin of the SRAM cell. EX1033, 1; Section IX.B; Section V.C. In fact, Yu explicitly teaches that “*customiz[ing] fin heights...so that the FinFETs may have customized performance.*” EX1010, [0004], [0010]. Therefore, a person of ordinary skill in the art would have been motivated to

customize the performance of pFinFETs and nFinFETs by customizing their fin heights such that the pFinFETs' fins ("even" or "second" fins) "are...different from" nFinFETs' fins ("odd" or "first" fins) "in height" to achieve an optimum SRAM design/structure.

X. CONCLUSION

216. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: April 17, 2025


By: _____

Sanjay Banerjee