

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.,

AND

APPLE, INC.,

Petitioners

v.

MARLIN SEMICONDUCTOR LIMITED.

Patent Owner

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Case IPR2025-00864

Patent No. 9,184,292

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**PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 9,184,292**

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# **LIST OF EXHIBITS**

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| EX1001 | U.S. Patent No. 9,184,292                                                                                                                                                                |
| EX1002 | Declaration of Dr. Sanjay Banerjee.                                                                                                                                                      |
| EX1003 | Curriculum Vitae of Dr. Sanjay Banerjee.                                                                                                                                                 |
| EX1004 | Prosecution History of U.S. Patent No. 9,184,292                                                                                                                                         |
| EX1005 | U.S. Patent Application Publication No. 2008/0308848 (“Inaba”)                                                                                                                           |
| EX1006 | U.S. Patent Application Publication No. 2011/0108920 (“Basker”)                                                                                                                          |
| EX1007 | U.S. Patent Application Publication No. 2009/0057846 (“Doyle”)                                                                                                                           |
| EX1008 | U.S. Patent No. 8,942,030 (“Liaw”)                                                                                                                                                       |
| EX1009 | U.S. Patent No. 7,297,581 (“Hill”)                                                                                                                                                       |
| EX1010 | U.S. Patent Application Publication No. 2008/0230852 (“Yu”)                                                                                                                              |
| EX1011 | RESERVED                                                                                                                                                                                 |
| EX1012 | Complaint (Dkt. No. 1) in <i>Longitude Licensing Ltd. et al v. Lenovo Group Limited et al</i> , Case No. 2:25-cv-00171 (E.D.Tex. Feb. 13, 2025).                                         |
| EX1013 | S. Balakumar, et al., “Solid phase epitaxy during Ge condensation from amorphous SiGe layer on silicon-on-insulator substrate,” <i>Applied Phys. Lett.</i> , 89, 032101, 1-4, July 2006. |
| EX1014 | U.S. Patent No. 8,625,334 (“Liaw-334”)                                                                                                                                                   |
| EX1015 | U.S. Patent Application Publication No. US2008/0020515 (“White”)                                                                                                                         |
| EX1016 | J. Franco, et al., “Improvements of NBTI reliability in SiGe p-FETs,” <i>2010 IEEE International Reliability Physics Symposium</i> , Anaheim, CA, USA, 2010, pp. 1082-1085.              |

|        |                                                                                                                                                                                                                                                                                          |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EX1017 | J. Huang et al., “Mechanisms limiting EOT scaling and gate leakage currents of high-k/metal gate stacks directly on SiGe and a method to enable sub-1nm EOT,” <i>2008 Symposium on VLSI Technology</i> , Honolulu, HI, USA, 2008, pp. 82-83.                                             |
| EX1018 | J. Oh <i>et al.</i> , “Additive mobility enhancement and off-state current reduction in SiGe channel pMOSFETs with optimized Si Cap and high-k metal gate stacks,” <i>2009 International Symposium on VLSI Technology, Systems, and Applications</i> , Hsinchu, Taiwan, 2009, pp. 22-23. |
| EX1019 | S. M. Sze, “Physics of Semiconductor Devices,” <i>John Wiley &amp; Sons</i> , 1981, Chapter 8, pp. 431-456.                                                                                                                                                                              |
| EX1020 | J. D. Plummer, “Silicon VLSI Technology: Fundamentals, Practice and Modelling,” <i>Prentice Hall</i> , 2000, Chapter 10, pp. 637-650.                                                                                                                                                    |
| EX1021 | RESERVED                                                                                                                                                                                                                                                                                 |
| EX1022 | RESERVED                                                                                                                                                                                                                                                                                 |
| EX1023 | U.S. Patent Application Publication No. 2007/0069302 (“Jin”)                                                                                                                                                                                                                             |
| EX1024 | U.S. Patent No. 6,787,406 (“Hill-406”)                                                                                                                                                                                                                                                   |
| EX1025 | H. Adhikari <i>et al.</i> , “High mobility SiGe shell-Si core omega gate pFETS,” <i>2009 International Symposium on VLSI Technology, Systems, and Applications</i> , Hsinchu, Taiwan, 2009, pp. 136-138                                                                                  |
| EX1026 | R. Bijesh <i>et al.</i> , “Hole mobility enhancement in uniaxially strained SiGe FINFETs: Analysis and prospects,” <i>69th Device Research Conference</i> , Santa Barbara, CA, USA, 2011, pp. 237-238.                                                                                   |
| EX1027 | Intel Newsroom (2011)                                                                                                                                                                                                                                                                    |
| EX1028 | Intel 22nm Announcement Presentation (2011)                                                                                                                                                                                                                                              |
| EX1029 | Intel 22nm Details Presentation (2011)                                                                                                                                                                                                                                                   |

|        |                                                                                                                                                                                                                                                            |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EX1030 | S. Bedell <i>et al.</i> , “Opportunities and Challenges for Germanium and Silicon-Germanium Channel p-FETs,” <i>ECS Transactions</i> , Vol. 19, No. 1                                                                                                      |
| EX1031 | J. Mitard <i>et al.</i> , “High-mobility 0.85nm-EOT Si <sub>0.45</sub> Ge <sub>0.55</sub> -pFETs: Delivering high performance at scaled VDD,” <i>2010 International Electron Devices Meeting</i> , San Francisco, CA, USA, 2010, pp. 10.6.1-10.6.4.        |
| EX1032 | M. Poljak <i>et al.</i> , “Improving bulk FinFET DC performance in comparison to SOI FinFET,” <i>Microelectronic Engineering</i> , Vol. 86, Issue 10, Oct. 2009, Pp. 2078-2085.                                                                            |
| EX1033 | Mukherjee, Debasish and Hemanta Kr. “Static Noise Margin Analysis of SRAM Cell for High Speed Application,” <i>IJCSI International Journal of Computer Science Issues</i> , Vol. 7, Issue 5, Sept. 2010.                                                   |
| EX1034 | V. Huard <i>et al.</i> , “NBTI degradation: From transistor to SRAM arrays,” <i>2008 IEEE International Reliability Physics Symposium</i> , Phoenix, AZ, USA, 2008, pp. 289-300.                                                                           |
| EX1035 | M. Alioto, “Analysis of layout density in FinFET standard cells and impact of fin technology,” <i>Proceedings of 2010 IEEE International Symposium on Circuits and Systems</i> , Paris, France, 2010, pp. 3204-3207.                                       |
| EX1036 | Zheng Guo, S. Balasubramanian, R. Zlatanovici, Tsu-Jae King and B. Nikolic, “FinFET-based SRAM design,” <i>ISLPED '05. Proceedings of the 2005 International Symposium on Low Power Electronics and Design</i> , 2005., San Diego, CA, USA, 2005, pp. 2-7. |
| EX1037 | U.S. Patent Application Publication No. 2007/0194833 (“Takeyama”)                                                                                                                                                                                          |
| EX1038 | W. Qi et al., “Investigation on solid phase epitaxy of deposited SiGe film on a Si substrate,” <i>Thin Solid Films</i> , Vol. 293, Issues 1–2, 30 Jan. 1997, Pp. 310-314.                                                                                  |
| EX1039 | U.S. Patent No. 8,367,498 (“Chang”)                                                                                                                                                                                                                        |

|        |                                                                                                                                                                       |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EX1040 | Cotte et al., “Predicting critical dimension uniformity in advanced electron-beam projection lithography masks,” <i>J. Vac. Sci. Technol. B</i> 21, 3027–3031 (2003). |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## I. RELIEF REQUESTED

Claims 1-20 (“Challenged Claims”) should be canceled as unpatentable based on the following grounds:

| Ground       | Claim(s) Challenged             | 35 U.S.C. § | Reference(s)       |
|--------------|---------------------------------|-------------|--------------------|
| <b>1</b>     | 1, 3-9, 11-15, 17-20            | 103         | Basker + Hill      |
| <b>2</b>     | 2, 10, 16                       | 103         | Basker + Hill + Yu |
| <b>3A/3B</b> | 1, 5, 7-9, 13, 15, 19           | 102/103     | Inaba              |
| <b>4</b>     | 3, 4, 6, 11, 12, 14, 17, 18, 20 | 103         | Inaba + Basker     |
| <b>5</b>     | 2, 10, 16                       | 103         | Inaba + Yu         |
| <b>6</b>     | 1, 3-9, 11-15, 17-20            | 103         | Liaw + Basker      |
| <b>7</b>     | 2, 10, 16                       | 103         | Liaw + Basker + Yu |

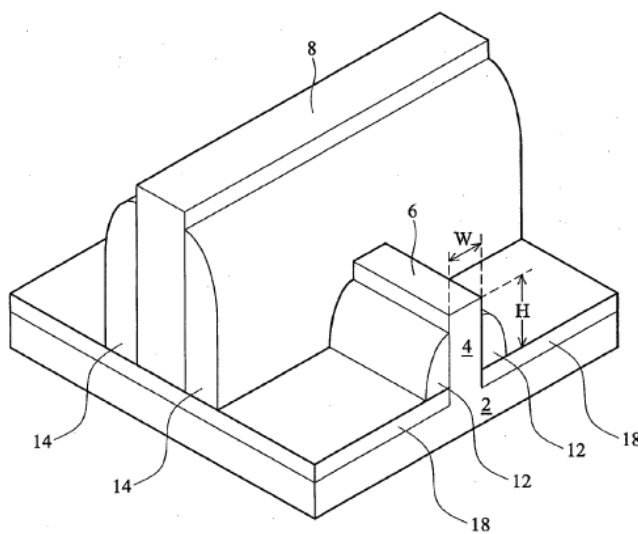
## II. STATE OF THE ART

### A. FinFETs

#### 1. Device Features – Fin Height and Width

A field-effect transistor (FET) functions essentially as a switch controlled by voltage applied to a “gate” between “source” and “drain” regions. EX1019, 9-10, 14-15, FIGs. 3, 6; EX1020, 40-51, FIG. 1-11. When the FET is turned on, current flows between the source and drain regions through a “channel” formed under the gate of the FET. EX1019, 9-10, 14-15, FIGs. 3, 6; EX1020, 40-51. Two general types of FETs known in the art at the time include a planar FETs and a non-planar three-dimensional (3D) FETs, such as FinFETs. EX1032, 1; EX1002 ¶¶21-22.

The current a FinFET provides depends on its physical dimensions, including **channel width** (for *tri-gate* FinFETs: effectively  $w$  (fin width) +  $2 \cdot H$  (fin height) or for *double-gate* FinFETs:  $2 \cdot H$  as shown in Figure 1 below) and gate length (the dimension where the gate electrode overlapping the fin). EX1010, [0004], FIG. 1 (below); EX1002, ¶23.



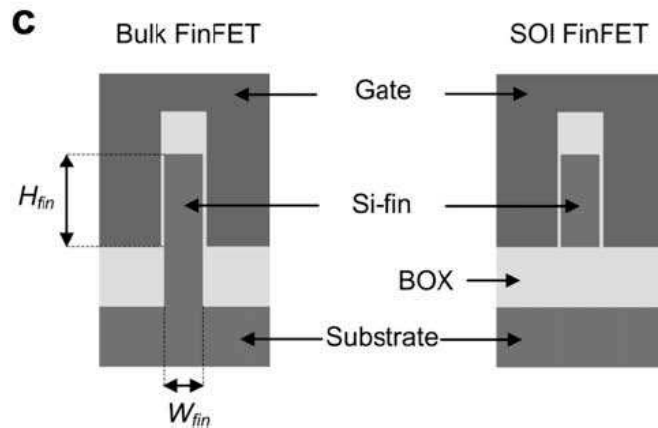
Adjusting fin width and/or fin height to adjust FinFET performance was routine and well-known. EX1010, [0010]; EX1033, 1-3. And as the prior art discussed herein illustrates, it was well-known a semiconductor structure may have FinFETs with different fin widths and/or different fin heights. *Id.*; EX1002 ¶24.

## 2. Fabrication of FinFETs – Bulk and SOI FinFETs

Semiconductor devices were known to be built upon wafers. As was known in the art, a “bulk” silicon wafer is made of silicon. EX1032, 1. Fin structures for bulk FinFETs may be formed by etching a bulk silicon substrate and are made of the

same material as the substrate. EX1023, [0045]-[0048]; EX1008 8:21-55. Isolation layers between fins (e.g., shallow-trench isolation (STI)), and a gate dielectric in the selected regions along the fin, are then deposited. *Id.*, EX1005, [0063]. Metallization may be used to create gate, electrical terminals, and contacts on the FinFET. EX1008, 11:52-12:4; 7:57-8:14. EX1002, ¶25.

Another type of substrate, known as silicon-on-insulator (SOI), may be used to form SOI FinFETs. EX1023, [0019], [0030]. Bulk FinFETs and SOI FinFETs have nearly identical structures as shown below. EX1032, 1-2. Thus, the fabrication processes and the layout for circuits using bulk FinFETs can be readily applied to circuits using SOI FinFETs and vice versa. EX1002, ¶26.



EX1032, FIG. 1C

## B. SiGe pFinFET for Performance Enhancement

It was known FinFET performance could be improved by incorporating germanium (Ge) or silicon germanium (SiGe) into the fins of the FinFETs.

EX1002 ¶27. There has been a general trend to include Ge/SiGe into the transistor's channel, which traditionally has been made of silicon. It was known “[p]lanar Si channel device may not be able to provide for the high performance needed in future MOSFETs” (EX1025, 1) and Ge was “reported to demonstrate performance improvement over Si” (*id.*). It was known hole mobility was improved by using SiGe channel than Si channel (*id.*) and “further hole mobility enhancement in [Silicon] pFINFETs is limited.... **SiGe channel FINFET is an attractive replacement**” (EX1026, 1). Using SiGe channel in pFETs allowed lower temperature dopant activation and improved gate dielectric scalability. EX1030, 2. It was also demonstrated pFinFETs having SiGe channels would be “viable candidates for future **high-speed applications** due to its excellent drive current performance [and other benefits].” EX1031, 1; EX1002, ¶27.

It was also known pFinFETs using SiGe fins, compared to Si fins, allow for **lower power consumption** and exhibit **improved reliability** associated with negative bias temperature instability (NBTI), which was “a major reliability problem for the semiconductor industry.” EX1006, [0021], [0043]; EX1016, 1; EX1034, 1. Furthermore, hole mobility in SiGe was known to be approximately twice of that in Si and thus SiGe pFinFETs are faster than Si counterparts. EX1017, 1. As explained below, it was well-known nFinFETs used Si fins and pFinFETs used SiGe fins. §VI.A.1; EX1002, ¶¶28-29.

### C. FinFET-Based Integrated Circuits (ICs)

At the relevant time, FinFETs had widespread commercial use, including static random access memory (SRAM). *See generally* EX1027; EX1028, 5, 8, 10-12, 16, 24; EX1029, 2, 5-10, 14, 22-23, 27; EX1002, ¶30. Since the early days of planar transistors and to date, SRAM has become and remains the most popular storage solution and is incorporated in nearly all IC chips (e.g., microprocessors, etc.). EX1008, 1:20-26. A SRAM cell commonly contains multiple transistors and it would have been a routine practice to adjust/optimize the SRAM/transistor and their layout to meet performance and area requirements. After FinFETs were introduced, SRAM has been implemented using FinFETs. One reason was the 3D geometry of the fins may be scaled by, e.g., increasing the fin height, which allows for increasing “drive currents of FinFETs...without incurring the penalty of chip area.” EX1010, [0004]; EX1035, 1. Additionally, it was known to use certain implantation method to “produce high-density SRAM cells,” “permit[ting] reduction of SRAM cell size by approximately 40-50%.” EX1009, 1:40-42; EX1002 ¶30.

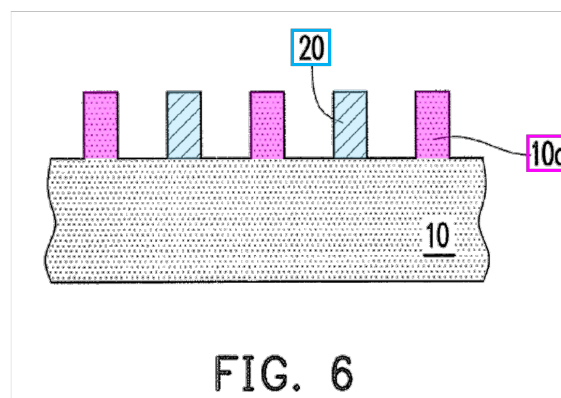
It was well-known the dimensions of the FinFETs in a SRAM cell impact SRAM cell’s performance. For example, static noise margin of a SRAM cell (quantifying amount of noise a SRAM cell can tolerate/withstand before affecting its stored data) depends on parameters involving **the channel width and channel length of the transistors** in the SRAM cell (EX1033, 1), where the channel width

is a function of the **fin height**. The size of the transistors in a SRAM cell also impacts the **speed of SRAM**. Thus, a POSITA would have adjusted, including to determine optimal and/or workable ranges of the **fin height** to achieve certain SRAM performance parameters. EX1002 ¶31.

### III. THE '292 PATENT

#### A. Overview

The '292 patent relates to fabricating a semiconductor fin structure for forming FinFETs. EX1001, 1:16-19. Figure 6 depicts a fin structure having semiconductor substrate 10 with **odd** fins 10a. EX1001, Abstract; 3:50-60. **Even** fins 20 are also formed on substrate 10 and between **odd** fins 10a. *Id.* Each of **even** fins 20 is located between two **odd** fins 10a, forming an **odd-even-odd-even-odd** pattern. *Id.*, 1:67-2:12. The semiconductor substrate 10 and **odd** fins 10a are formed of semiconductor material, e.g., silicon. *Id.*, 2:48-50. Because they are formed separately, **even** fins 20 may differ from **odd** fins 10a in materials, fins widths, or fin heights. *Id.*, 3:35-49, 3:53-60; EX1002, ¶¶32-35.



'292 Patent, Fig. 6 (annotated)

## **B. File History**

During prosecution, the Office initially rejected then-pending claims 1-18 in view of White (EX1015). EX1004, 56-61. Among other things, the Office indicated White anticipates and/or renders obvious an odd-even-odd-even-odd fin pattern with odd fins and even fins differing in fin material. *Id.*, 59; *see also id.*, 78-79, 87-94 (claim amendments). Applicant also stated “as known in the art, the ‘fin structure’ is defined as a protrusion rises above the top surface of the substrate.” *Id.*, 106. Ultimately, the Office issued a Notice of Allowance. *Id.*, 115-22, 137.

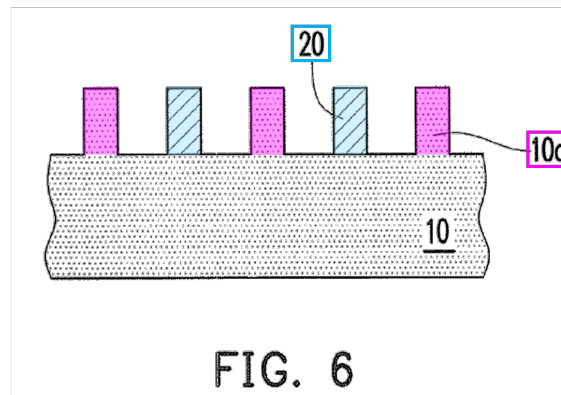
## **C. Claim Construction**

Petitioners do not believe any claims require construction to resolve the patentability disputes in this proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).<sup>1</sup>

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<sup>1</sup> Petitioners reserve all rights to raise claim construction and other arguments, including challenges under 35 U.S.C. §112, in relevant district court and/or ITC proceedings. *See Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 11–13 (Nov. 10, 2020). A comparison of the claims to any accused products in litigation may raise controversies that are not presented here given the similarities between the references and the patent. By applying the plain meaning or PO's

The '292 patent describes with respect to Figure 6 a structure including “**odd** fins 10a and **even** fins 20 that are arranged *alternately*.” EX1001, 3:53-56. Consistent with the figure, the specification describes an arrangement of **a single odd fin alternating with a single even fin**, i.e., **odd-even-odd-even-odd** fins, which is the only fin arrangement disclosed by the specification. *See generally* EX1001; EX1002, ¶49.

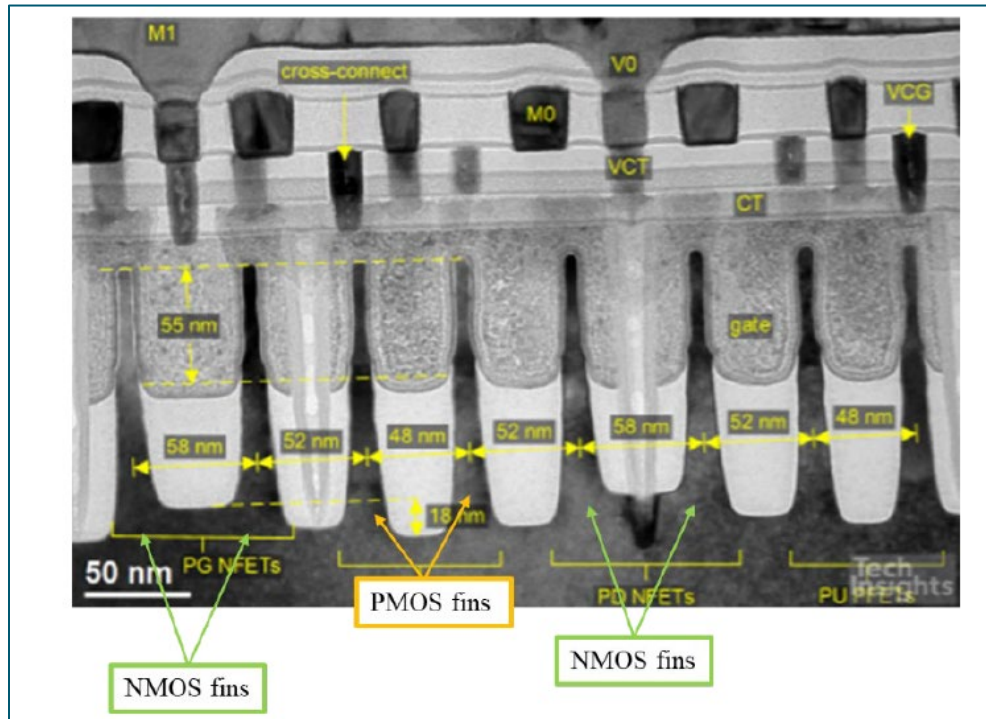


EX1001, Figure 6 (annotated)

But PO in litigation accuses a structure allegedly including a different arrangement—two same **NMOS fins**, two same **PMOS fins**, and two same **NMOS fins**, as shown in the figure below. EX1012, 45-46.

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apparent interpretation herein for this proceeding, Petitioners do not concede the claims are definite, have specification support, etc., and thus reserve the right to address any associated §112 issues in other proceedings.



PO appears to interpret the limitations associated with the arrangement of “odd [or first] fins” and “even [or second] fins” as being not limited to an arrangement of a **single odd fin alternating with a single even fin**. For example, PO accuses **each alleged pair of NMOS fins** as the “a plurality of **odd [or first] fins**” (claims 1/9/15) and **the alleged pair of PMOS fins** as “a plurality of **even [or second] fins**” (claims 1/9/15). Petitioners disagree with PO’s litigation allegations. *Philip Morris Products, S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00921, Paper 13 at 42-44 (Aug. 5, 2021) (a petitioner may “rely[] on claim constructions that it believes are incorrect.”).

Petitioners demonstrate below how the prior art discloses/suggests and renders obvious the challenged claims under the plain and ordinary meaning of the

claim terms except for the terms associated with the arrangement of “odd [or first]” and “even [or second]” fins (claims 1/9/15), which are addressed (1) under the plain and ordinary of the terms consistent with the ’292 patent specification (**Grounds 1-2**); and (2) under PO’s litigation allegations (**Grounds 3-7**). Grounds 1-2 also invalidate the challenged claims under PO’s litigation allegations. EX1002, ¶¶46-51.

#### **IV. LEVEL OF ORDINARY SKILL**

A person of ordinary skill in the art as of the claimed priority date of the ’292 patent (“POSITA”) would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as for example, integrated circuit device (or transistor) design and/or manufacturing. EX1002, ¶¶19-20.<sup>2</sup> Additional relevant education could substitute for professional experience, and significant work experience or training could substitute for less formal education. *Id.*

#### **V. PRIOR ART**

The ’292 patent issued from an application that is a division of an application filed February 9, 2012. EX1001, Cover. Petitioners here assume that is the effective

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<sup>2</sup> Petitioners submit the declaration of Dr. Sanjay Banerjee, EX1002, an expert in the field of the ’292 patent. EX1002, ¶¶1-20; EX1003.

date for the '292 patent without conceding it is entitled to such date. The above asserted prior art references qualify as prior art to the '292 patent as follows:

| Reference | Filed            | Published          | Pre-AIA Prior Art Qualification |
|-----------|------------------|--------------------|---------------------------------|
| Inaba     | May 12, 2008     | December 18, 2008  | §102(b)                         |
| Basker    | November 9, 2009 | May 12, 2011       | §§102(a), (e)                   |
| Liaw      | June 25, 2010    | December 29, 2011  | §§102(a), (e)                   |
| Hill      | December 8, 2003 | November 20, 2007  | §102(b)                         |
| Yu        | March 6, 2007    | September 25, 2008 | §102(b)                         |

## VI. DETAILED EXPLANATION OF GROUNDS<sup>3</sup>

### A. Ground 1: Claims 1, 3-9, 11-15, and 17-20 Are Obvious Over Basker and Hill

As discussed below, the Basker-Hill combination discloses and/or suggests the above-noted claims under both interpretations discussed in §III.C.

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<sup>3</sup> Petitioners' obviousness positions do not rely on any bodily incorporation of disclosed prior art feature(s). Rather, the asserted combination/modification of prior art reference(s) discussed herein rely on the collective teachings/suggestions of those the reference(s) in context of a POSITA's state of art knowledge that demonstrate how/why such a POSITA would have been motivated, and found obvious, to

## 1. Basker

Because Basker is in the same field (FinFET devices) and reasonably pertinent to a problem the '292 Patent purports to address (FinFET devices fabrication), Basker is analogous art. EX1001, 1:15-35; EX1006, Abstract, [0004]; EX1002, ¶¶38-39. Basker discloses FinFET structures for use in ICs. EX1006, Abstract, [0005]-[0007], [0020], [0029]. Basker's fin structures are used for n-type FET (nFinFET) and p-type FET (pFinFET). *Id.*, [0020]. Basker discloses use of **Si fins** for **nFinFETs** and **SiGe fins** for **pFinFETs** to improve the pFinFETs' performance. *Id.*, [0020]-[0021]. The SiGe fins are formed by incorporating epitaxially-deposited material into the fins for pFinFETs. *Id.*, [0005], [0031]-[0032], [0041], claim 1; EX1013, 2; EX1002, ¶¶52-55.

As shown in Figure 8, the formation of a CMOS device 48 includes nFinFET 44 and pFinFET 46 by etching a top layer of substrate 10 (Figure 1) comprising a silicon layer 16 to form Si fins (20, 22) using a patterning process, as shown in Figure 2. EX1006, [0025]-[0027], [0034].

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modify/configure the disclosed feature(s) from a given prior art reference in view of such collective teachings/suggestions/ knowledge.



EX1006, FIGS. 2, 8 (annotated)

While substrate 10 in Figure 2 is SOI, Basker discloses substrate 10 may be bulk monocrystalline silicon. EX1006, [0025]; EX1002, ¶56.

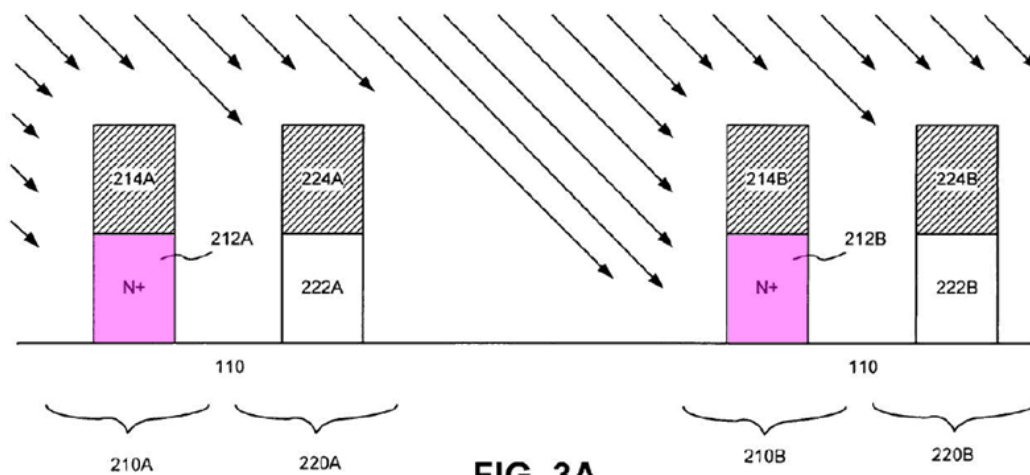
The Si fin 20 in Figure 2 is used to form the nFinFET, while the fin for pFinFET is made by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22, resulting in a SiGe fin for the pFinFET. EX1006, [0005], [0030]-[0033], [0041], claim 1. Standard FinFET processing is then used to form nFinFETs using Si fin 20 and pFinFETs using SiGe fin 22. *Id.*; EX1002, ¶¶57-58.

## 2. Hill

Because Hill is in the same field (FinFET devices) and reasonably pertinent to a problem the '292 Patent purports to address (FinFET devices fabrication), Hill is analogous art. EX1001, 1:15-35; EX1009, Abstract; EX1002, ¶¶42-43. Hill discloses implementations of SRAM circuit using FinFETs reduces SRAM cell area by 40-50%. EX1009, 1:40-46; EX1002, ¶¶64-70.

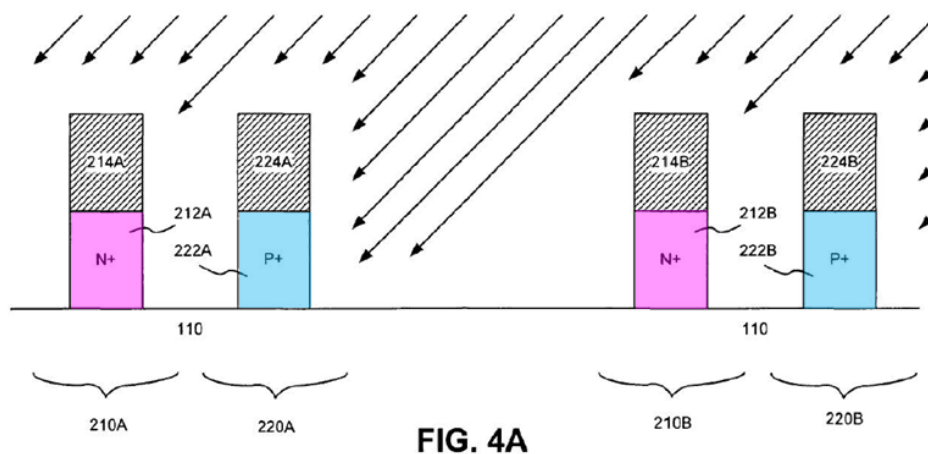
Hill discloses fabricating fin structures by angle implantation for ICs using FinFETs, resulting in devices with an n-p-n-p fin pattern. EX1009, 1:13-16; 1:40-42; 1:46-48; 2:42-52. Hill's implantation method forms "tightly spaced FinFET devices to produce high-density SRAM cells" and "permits reduction of SRAM cell size by approximately 40-50%." *Id.*, 1:40-44. Hill dopes a first pair of fins with **n-type** impurities using one tilt angle implant, and dopes a second pair of fins with **p-type** impurities using another tilt angle implant. *Id.*, 1:51-54. Hill does not limit which portion(s) of the FinFETs may be implanted and a POSITA would have understood such implantations were known to be used for doping, e.g., source/drain of a FinFET (EX1024 (disclosing implantation used for doping the source/drain of FinFETs)) and/or other part(s) of the FinFET. EX1002, ¶¶65-68.

Figure 3A shows fins 212A, 212B, 222A, 222B, where each fin has a cap 214A, 214B, 224A, 224B. EX1009, 3:5-14.



EX1009, FIG. 3A (annotated)

The height of the cap and the pitch between each fin are selected such n-type impurities using a first tilt angle are implanted into fins 212A/212B (pink) while fins 222A/222B remain undoped (white) because fins 212A/212B and caps 214A/214B shield fins 222A/222B from n-type impurities. *Id.*, 3:51-58. Subsequently, as shown in Figure 4A, p-type impurities using a second tilt angle are implanted into fins 222A/222B (blue) while n-type fins 212A/212B (pink) are shielded from p-type impurities by fins 222A/222B (blue) and caps 224A/224B. *Id.*, 4:11-18; EX1002, ¶69.



Hill, FIG. 4A (annotated)

Hill's method results in closely spaced fins having a pattern of a fin with n-type impurities ("n-fin") fin 212A, a fin with p-type impurities ("p-fin") fin 222A, n-fin 212B, and p-fin 222B, i.e., an n-p-n-p-fin pattern. "Conventional processing may then be performed" on the fins to complete the FinFET-based SRAM device. *Id.*, 5:29-35; EX1002, ¶70.

### **3. Combination of Basker and Hill**

Basker explains its FinFETs are for use in an IC and “[t]he circuit as described herein may be part of a design for an [IC] chip.” EX1006, [0005], [0023]. Thus, Basker does not limit its application of FinFETs to any particular IC. At the relevant time, a POSITA would have understood ICs ranged from simple combinations of logic gates to complicated circuits (e.g., microprocessors) and SRAM circuits were prevalent and were known to be found in many electronic products (e.g., a standalone chip or part of a larger/complicated IC or CPU). EX1002, ¶¶61-63. Given SRAM’s prevalence, a POSITA, motivated by Basker’s guidance, would have found it obvious to use FinFETs (e.g., those of Basker) to implement SRAM circuits. EX1002, ¶63.

Like Basker, Hill discloses fabrication of fin structures for ICs using FinFETs and a method for forming “tightly spaced FinFET devices to produce high-density SRAM cells” and “permits reduction of SRAM cell size by approximately 40-50%.” EX1009, 1:40-44; §VI.A.2; EX1002, ¶30. Thus, a POSITA would have considered Hill’s teachings when implementing SRAM circuits using FinFETs discussed in Basker. EX1002, ¶¶63-66.

As discussed below, the exemplary Basker-Hill combination discloses and/or suggests “a plurality of **odd** [or **first**] fins of the FinFETs...” (limitations [1.b]/[9.b]/[15.b]), “a plurality of **even** fins of the FinFETs...between the **odd** fins of the FinFETs, being **different** from the **odd** fins of the FinFETs in at least one of width and **material**” (limitations [1.c]/[9.c] discussed further in the next section), and “a plurality of **second** fins of the FinFETs..., each of the **second** fins of the FinFETs is located between two **first** fins of the FinFETs, and the **second** fins of the FinFETs are **different** from the **first** fins of the FinFETs in at least one of width and **material**” (limitation [15.c] discussed further in the next section). EX1002, ¶72.

A POSITA would have been motivated to combine Basker (e.g., use of Si nFinFETs and SiGe pFinFETs) and Hill (e.g., use of shadow implantation for producing high-density FinFET-based SRAM) to form a high-density FinFET-based SRAM using Si nFinFETs and SiGe pFinFETs. EX1002, ¶73. **First**, Hill’s implantation method produces “tightly spaced FinFET devices to produce high-density SRAM cells,” which “permits reduction of SRAM cell size by approximately 40-50%.” EX1009, 1:40-44. These features are beneficial because SRAM devices having reduced size would have allowed space for including/building other electronic components/features. EX1036, 1. Moreover, high-density SRAM cells (e.g., having tightly packed transistors/FinFETs/cells) would have increased the amount of data storage. EX1037, [0005]. Thus, a POSITA when implementing

FinFET-based IC devices as discussed in Basker would have been motivated to combine Hill's teaching. EX1002, ¶74.

**Second**, implementing SiGe fins in pFinFETs (e.g., as in Basker) for a SRAM cell would have been beneficial. EX1002, ¶75. SRAM devices were known to be used in various electronic devices to provide high-speed data storage/access. §§II.B-C. As discussed in §II.B, a POSITA would have recognized the trend toward the use of SiGe fins for pFinFETs and the associated benefits (§II.B), which, for instance, improve hole mobility and NBTI reliability. EX1002, ¶75; §II.B; EX1016, 1, 2, 4; EX1017, 1; EX1018, 1; EX1025, 1; EX1026, 1.

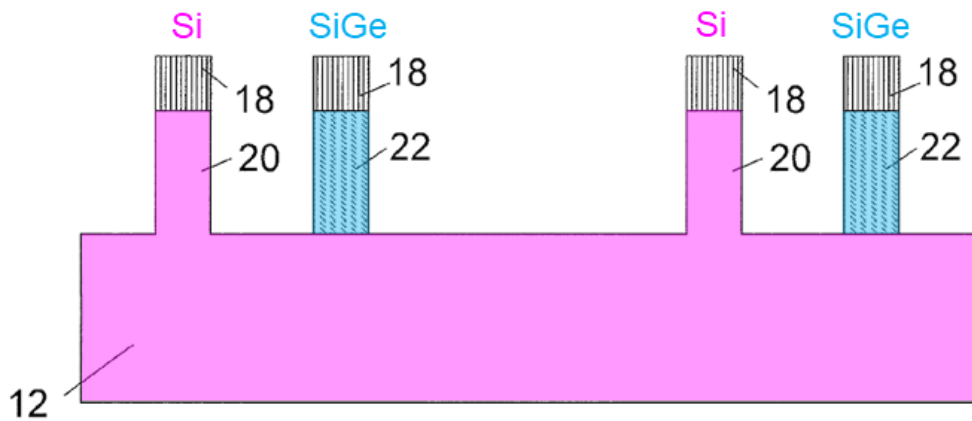
**Third**, Basker allows use of “the same gate dielectric...and the same gate conductor....” for both the nFinFET(s) and pFinFET(s) (EX1006, [0038]), which would have simplified the fabrication processes and reduced cost for making ICs/SRAM. EX1002, ¶76; EX1023, [0008], [0016], [0027].

A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the Basker-Hill combination. EX1002, ¶77. Basker itself discloses using SiGe fins in pFinFETs results in “an ideal combination” of beneficial features. EX1006, [0021]. Additionally, Basker's features may be applied to many IC components, including SRAM. *Id.* The combination of Basker and Hill would have been motivated by teaching/suggestion/motivation in the prior art (e.g., discussed above) and involved

application of known technologies (e.g., known use of Si nFinFETs and SiGe pFinFETs) according to known methods (e.g., known implantation method to form high-density FinFET-based SRAM cell) to yield the predictable result of high-density SRAM cells. *Id.*; *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

**Exemplary Combination Based on Basker's and Hill's Teaching**

Based on the collective teachings/suggestions of Basker and Hill, a POSITA would have found it obvious to configure the above discussed FinFET structure of Basker (where the nFinFETs include **Si fins** and pFinFETs include **SiGe fins**) to form FinFET-based SRAM cell of high density and reduced footprint (as discussed in Hill). EX1002, ¶78. In one non-limiting example, a POSITA would have been motivated to configure the FinFET structure to form an exemplary SRAM cell having features shown in Figure 7\* (modified based on Figure 7 of Basker), i.e., an arrangement of n-p-n-p fins, where the n-fin (e.g., with n-type S/D implantation for nFinFET) includes Si and the p-fin (e.g., with p-type S/D implantation for pFinFET) includes SiGe. EX1002, ¶78.



EX1006, FIG. 7\* (annotated)

A POSITA would have also known a SRAM cell stores one bit of data and multiple SRAM cells are needed for data storage and thus would have found it obvious to replicate multiple SRAM cells. EX1002, ¶79; EX1037, [0017]. Indeed, Hill discloses/suggests the SRAM cell is replicated across the substrate to form a SRAM device. EX1009, 1:13-16, 1:20-24; 1:40-42, 2:39-41. Basker also discloses “multiple copies of the chip design...are to be formed” on a substrate/wafer. EX1006, [0023]; EX1002, ¶79.

When forming multiple SRAM cells on the substrate in light of Hill, a POSITA would have found it obvious to configure the **arrangement/order of n-p-n-p fins** of the Basker-Hill SRAM cell (e.g., Figure 7\* of Basker) such that the arrangement/order was **replicated for each cell** because of the nature of Hill’s implantation process. EX1002, ¶80. This is exemplified using the modified Figures 7\*(a) and 7\*(b) of Basker below, which shows fins of two SRAM cells replicated

side-by-side and subject to the shadow implantation process (as in Hill), the **odd-numbered fins** are **n-fins**, and the **even-numbered fins** are **p-fins**. EX1002, ¶80.

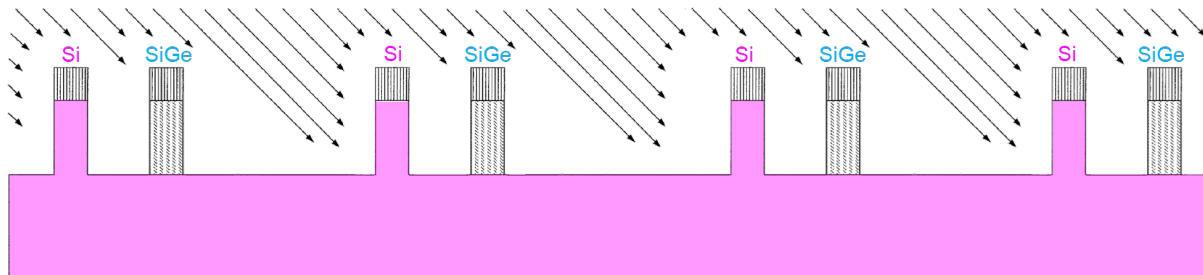


FIG. 7\*(a)

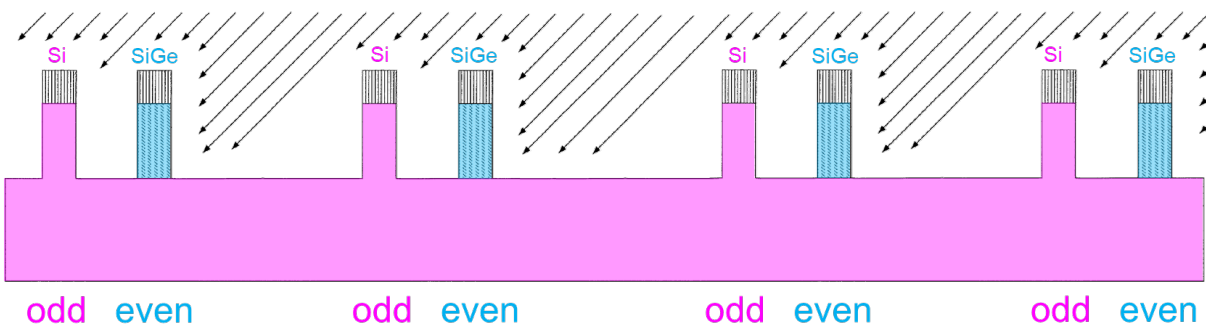


FIG. 7\*(b)

Indeed, a POSITA would have been motivated to orient the **fins of multiple SRAM cells in the same direction** in view of Hill's implantation process, e.g., to avoid inconsistent doping among the fins. EX1002, ¶81. Thus, a POSITA would have been motivated to implement multiple SRAM cells having an **arrangement/order of n-p-n-p-n-p-n-p fins** in the Basker-Hill combination. EX1002, ¶81.

A POSITA would have had the skill, rationale, and knowledge in implementing and reasonable expectation of success in achieving the above-

discussed Basker-Hill combination. This is particularly true given that Basker states its FinFET structure “may be part of a design for an [IC] chip” (EX1006, [0005], [0023]) and Hill teaches FinFET-based SRAM (EX1009, 1:40-44). A POSITA would have understood many SRAM cells may be repeated on the same substrate. EX1002, ¶¶82-85; EX1037, [0017]; EX1040, 2.

#### 4. Claims 1, 9, and 15<sup>4</sup>

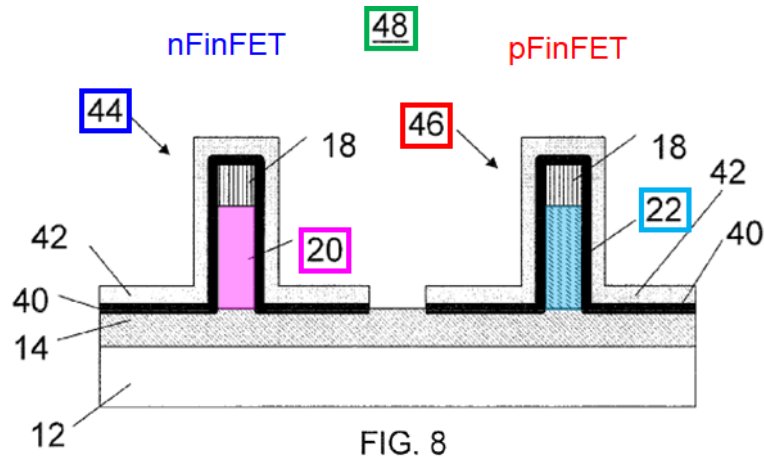
##### (i) [1.pre]/[9.pre]/[15.pre]

Basker discloses these preambles.<sup>5</sup> EX1002, ¶¶53-58; §VI.A.1. Basker discloses semiconductor FinFET structures. EX1006, Abstract, [0005]-[0007], [0020], [0029]. Basker’s fin structures are used for forming nFinFETs and pFinFETs. *Id.*, [0020]. Accordingly, Basker discloses a “semiconductor structure” (e.g., Figure 8) “for forming FinFETs” (preambles [1.pre]/[9.pre]) or “FinFET” (preamble [15.pre]). §VI.A.1; *infra* §§VI.A.4(ii)-(iv); EX1002, ¶¶53-58.

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<sup>4</sup> See Appendix A for all claim language. (§XII.)

<sup>5</sup> For purposes of all grounds herein, Petitioners do not acquiesce any of the preambles are limiting.



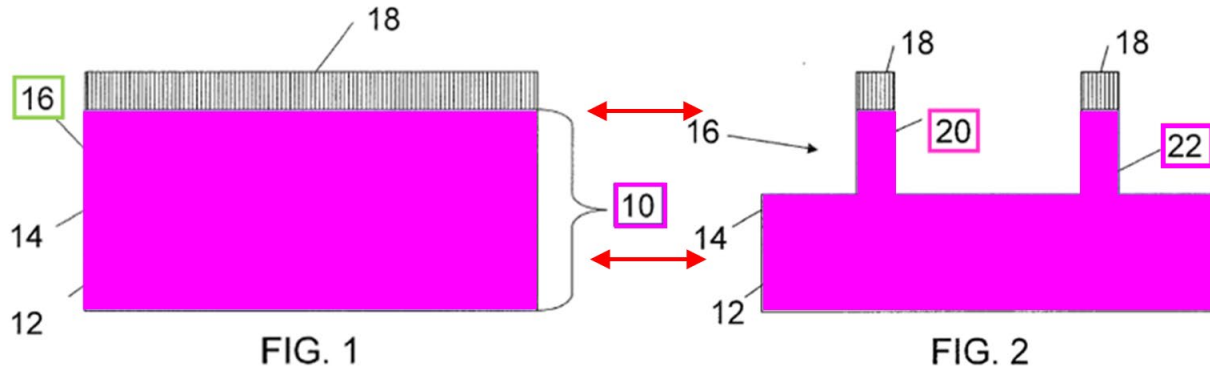
EX1006, FIG. 8 (annotated)

(ii) [1.a]/[9.a]/[15.a]

Basker discloses these limitations. EX1002, ¶¶59-60. As discussed above (§VI.A.1), Basker's substrate 10 may be a bulk monocrystalline silicon substrate ("semiconductor substrate"). EX1006, [0025]. Annotated Figures 1-2 illustrate substrate 10 as a bulk monocrystalline silicon substrate (pink), where the entire substrate is made of silicon ("a semiconductor material"), including "a top portion of the semiconductor substrate" (e.g., between the red arrows).<sup>6</sup> Indeed, Basker discloses etching monocrystalline silicon layer 16, which is a part of a "top portion"

<sup>6</sup> Figures 1 and 2 are modified/colored in solid pink color to represent the embodiment where Basker's substrate 10 is a bulk monocrystalline silicon substrate as expressly disclosed by Basker.

of substrate 10 to form Si fins 20, 22 (FIG. 2). *Id.*, [0025]-[0029]; EX1002, ¶¶59-60.



(iii) [1.b]/[9.b]/[15.b]

The Basker-Hill combination discloses/suggests these limitations. EX1002, ¶¶61-85. As explained above (§VI.A.1) and below, Basker discloses etching silicon substrate 10 (comprising “semiconductor material”) to form Si fin 20 for nFinFET (EX1006, [0025], [0030]-[0034]) and an additional process for forming SiGe fin 22 for pFinFET (*id.*).

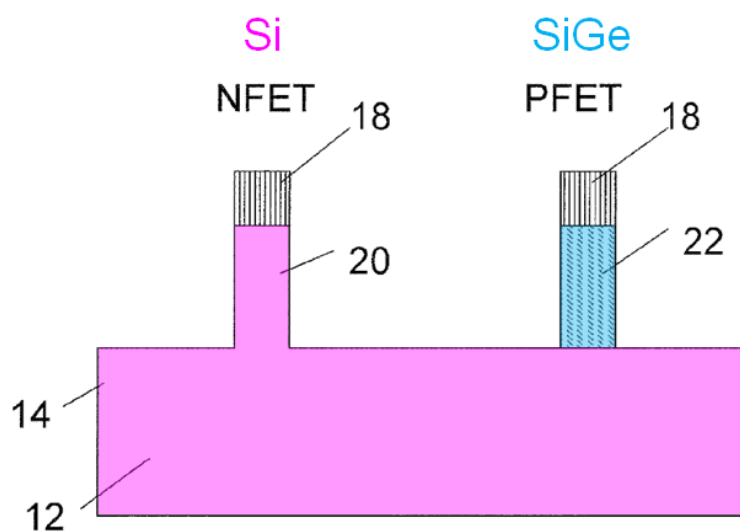


FIG. 7

EX1006, FIG. 7 (annotated)

Given fin 20 is defined by a “lithographic patterning process” (EX1006, [0027]-[0028]), fin 20 is “defined from the semiconductor substrate” (limitation [1.b]) and, as discussed above, “formed of the semiconductor material” (limitations [9.b]/[15.b]). §VI.A.4(ii). Additionally, since Si fin 20 is formed by etching the top portion of bulk substrate 10, fin 20 (the remaining/non-etched portion of the substrate) is “in direct contact with each other” as fin 20 and substrate 10 were in unity before etching. EX1006, [0027]-[0028]; EX1002, ¶61.

As discussed in §VI.A.3, the Basker-Hill combination would have predictably included an arrangement of fins of FinFETs having alternating/different fin material, i.e., **Si fins** for nFinFETs (**odd**-numbered fins) and **SiGe fins** for pFinFETs (**even**-

numbered fins), where the **even**-numbered fins reside between the **odd**-numbered fins, as shown in modified Figure 7\*(c). EX1002, ¶¶62-83.

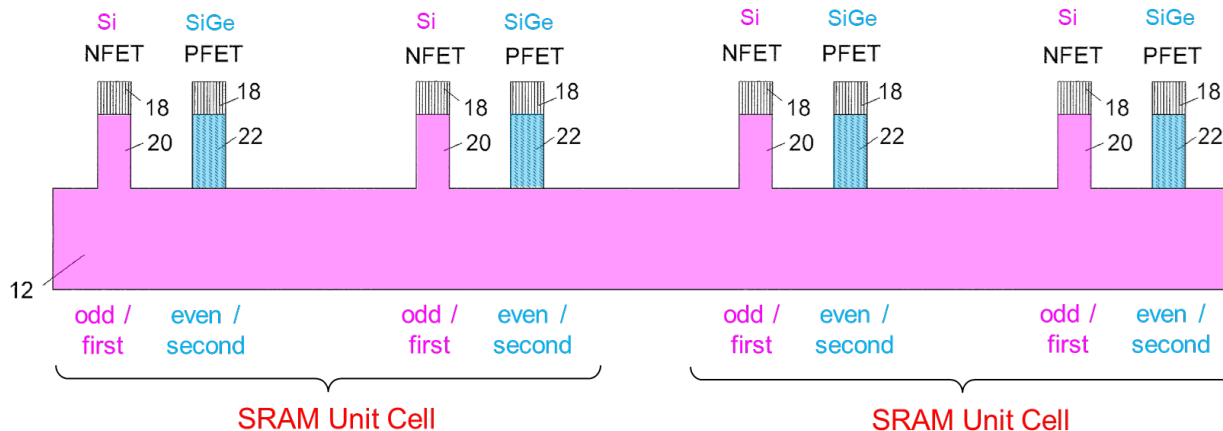


**FIG. 7\*(c)**

Likewise, as shown in the modified Figure 7\*(c) above, the Basker-Hill combination would have been predictably configured to include an arrangement of fins having alternating/different fin material, i.e., **Si fins** for nFinFETs (“**first**” fins) and **SiGe fins** for pFinFETs (“**second**” fins), where each of the “**second**” fins is located between two “**first**” fins. EX1002, ¶84.

Accordingly, the Basker-Hill combination discloses and/or suggests “a plurality of **odd** [or **first**] fins of the FinFETs...” (limitations [1.b]/[9.b]/[15.b]), “a plurality of **even** fins of the FinFETs...between the **odd** fins of the FinFETs, being **different** from the **odd** fins of the FinFETs in at least one of width and **material**” (limitations [1.c]/[9.c] discussed further in §VI.A.4(iv)), and “a plurality of **second** fins of the FinFETs..., each of the **second** fins of the FinFETs is located between

two **first** fins of the FinFETs, and the **second** fins of the FinFETs are **different** from the **first** fins of the FinFETs in at least one of width and **material**” (limitation [15.c] discussed further in §VI.A.4(iv)). EX1002, ¶85. Additionally, consistent with as discussed above, the Basker-Hill combination discloses and/or suggests “the plurality of **odd** [or **first**] fins and the **semiconductor substrate** are in **direct contact with each other**” as claimed in limitation [9.b]/[15.b]. *Id.*

(iv) [1.c]/[9.c]/[15.c]

The Basker-Hill combination discloses and/or suggests these limitations. EX1002, ¶¶86-89. The analysis for limitations [1.b]/[9.b]/[15.b] demonstrates how the Basker-Hill combination discloses and/or suggests “a plurality of even fins of the FinFETs...between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and *material*” (limitations [1.c]/[9.c]) and “a plurality of second fins of the FinFETs..., each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and *material*” (limitation [15.c]), which is exemplified by the modified Basker Figure 7\*(c) (where such features would have been implemented in the Basker-Hill combination as discussed for limitations [1.b]/[9.b]/[15.b]). *Supra* §§VI.A.3, VI.A.4(iii); EX1002, ¶86.

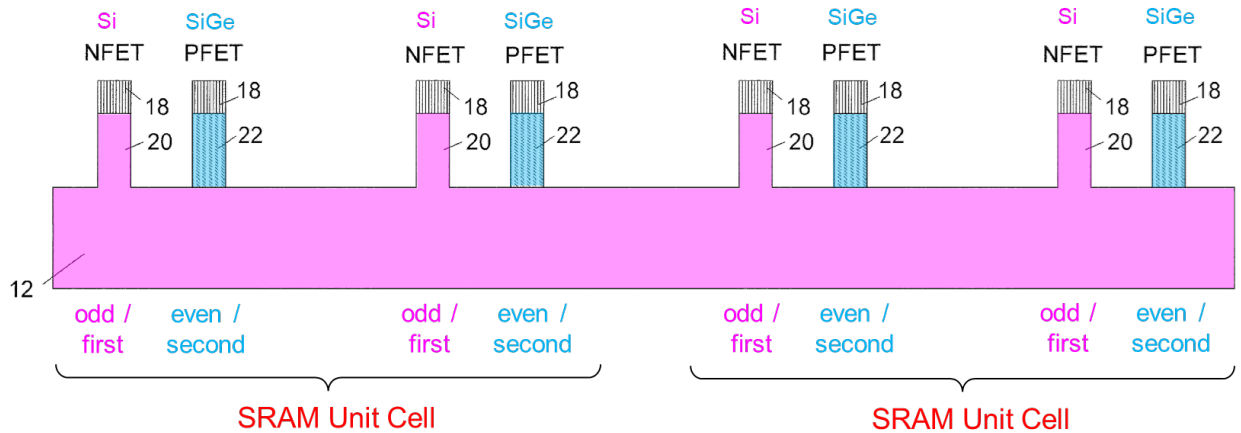


**FIG. 7\*(c)**

Additionally, as discussed above for limitations [1.a]/[9.a]/[15.a], Basker’s fins for nFinFETs and pFinFETs are initially formed by etching a silicon substrate such that the fins protrude from the substrate. §VI.A.4(ii). Also discussed therein (*id.*), the fins for the pFinFETs are then converted into SiGe fins. Thus, for reasons explained above the SiGe fins are “in direct contact with the semiconductor material,” which is of the top portion of the semiconductor substrate. Such features would have been implemented in the Basker-Hill combination for reasons explained above for limitations [1.b]/[9.b]/[15.b]. Accordingly, the Basker-Hill combination discloses and/or suggests limitations [1.c]/[9.c]/[15.c]. EX1002, ¶¶87-89.

## 5. Claims 3, 11, and 17

The Basker-Hill combination discloses these limitations. EX1002, ¶¶90-91. As discussed for the preambles and limitations [1.b]/[9.b]/[15.b], Basker’s SiGe fins are formed by epitaxially depositing a material (Ge/SiGe) and incorporating it into

fin 22. EX1006, [0005], [0020]-[0021], [0031]-[0032], [0041], claim 1. Since the resulting SiGe fins incorporate the epitaxially deposited material, the resulting SiGe fins “comprise an epitaxy material.” Also, a POSITA would have understood Basker’s SiGe fin formation results in epitaxy material and thus the resulting SiGe fins “comprise an epitaxy material.” EX1013, 2; EX1038, 3-4. Additionally, a POSITA would have known SiGe fins can also be formed using, e.g., chemical vapor deposition (CVD) and molecular beam epitaxy (MBE), and would have found it obvious to use any of them. EX1039, 4:23-5:9. Thus, the Basker-Hill combination discussed above (§VI.A.4) would have included “[even/second] fins of the FinFETs [that] comprise an epitaxy material.” EX1002, ¶¶90-91.

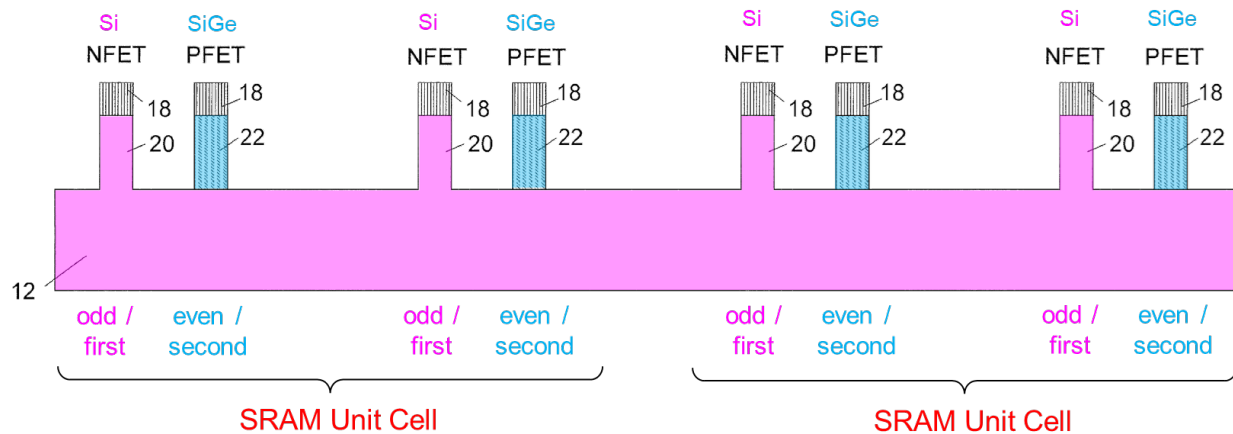


**FIG. 7\*(c)**

## 6. Claims 4, 12, and 18

The Basker-Hill combination discloses and/or suggests these limitations. EX1002, ¶92. As discussed for limitations [1.b]/[9.b]/[15.b], the Basker-Hill

combination discloses “the odd [or first] fins of the FinFETs comprise Si” because the disclosed “the odd [or first] fins” are formed by etching monocrystalline silicon substrate 10. EX1006, [0025]. As discussed therein, the Basker-Hill combination discloses forming SiGe fins for pFinFETs (“even [or second] fins of the FinFETs”). EX1002, ¶92. *Supra* §VI.A.4.

**7. Claims 5, 13, and 19**

The Basker-Hill combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18. EX1002, ¶93.

**8. Claims 6, 14, and 20**

The Basker-Hill combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18. EX1002, ¶94.

**9. Claim 7**

The Basker-Hill combination discloses and/or suggests this limitation. EX1002, ¶¶95-96. As discussed for limitations [1.a]/[9.a]/[15.a] and [1.b]/[9.b]/[15.b], the disclosed “odd fins of the FinFETs” are defined from a bulk monocrystalline silicon substrate 10, which would have been implemented in the Basker-Hill combination as discussed above for claim 1. EX1006, [0025]. Thus, the disclosed “odd fins of the FinFETs” in the Basker-Hill combination comprise silicon and are connected to the silicon substrate. A POSITA would have understood, given the disclosed “odd fins of the FinFETs” and the substrate in the

Basker-Hill combination are connected and both are the same semiconductor material, i.e., silicon, these fins and the substrate are electrically connected. EX1002, ¶¶95-96.

#### **10. Claim 8**

The Basker-Hill combination discloses and/or suggests this limitation. As discussed for limitations [1.a]/[9.a]/[15.a], substrate 10 (“semiconductor substrate”) in Basker may be bulk monocrystalline silicon substrate (EX1006, [0025]) and thus the entire substrate in the Basker-Hill combination would have been formed of “a single layer structure” of semiconductor material, i.e., silicon. EX1002, ¶97.

#### **B. Ground 2: Claims 2, 10, and 16 Are Obvious Over Basker, Hill, and Yu**

As discussed below, the Basker-Hill-Yu combination discloses and/or suggests the above-noted claims under both interpretations discussed in §III.C.

##### **1. Yu**

Because Yu is in the same field (FinFET devices) and reasonably pertinent to a problem the ‘292 Patent purports to address (FinFET devices fabrication), Yu is analogous art. EX1001, 1:15-35; EX1010, [0001], FIG. 9; EX1002, ¶¶44-45. Yu discloses FinFETs for use in ICs (EX1010, [0001]-[0002], [0019] (“semiconductor chip”)) and forming fins of the FinFETs by etching a bulk silicon substrate (*id.*, [0028], [0020]-[0024]). Yu additionally discloses forming “customized fin heights...so that the FinFETs may have customized performance.” EX1010, [0010].

Yu discloses with reference to Figure 5 (below) fins 48 and 50 are formed to have different heights, where the height difference is made by forming trenches of different depths, i.e., D1 around fin 48 and D2 around fin 50. *Id.*, [0023]-[0024]. EX1002, ¶¶101-102.

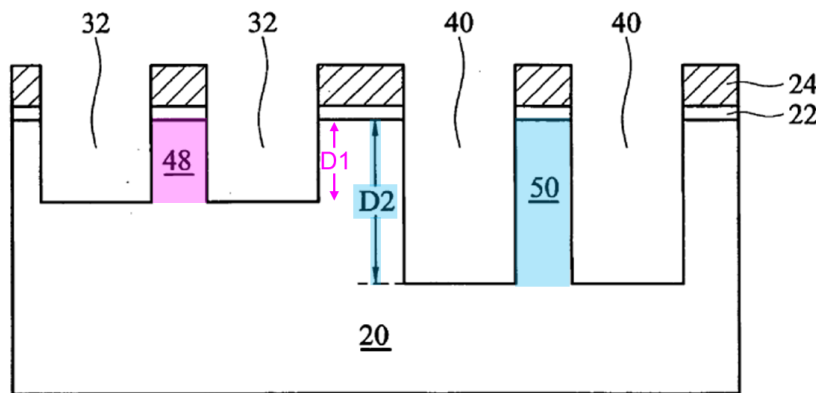


FIG. 5

EX1010, FIG. 5 (annotated)

Additional process steps may be applied to Fins 48 and 50 to form FinFETs 52 and 54 as shown in Figure 9 below. *Id.*, [0029], [0025]-[0027]; EX1002, ¶102.

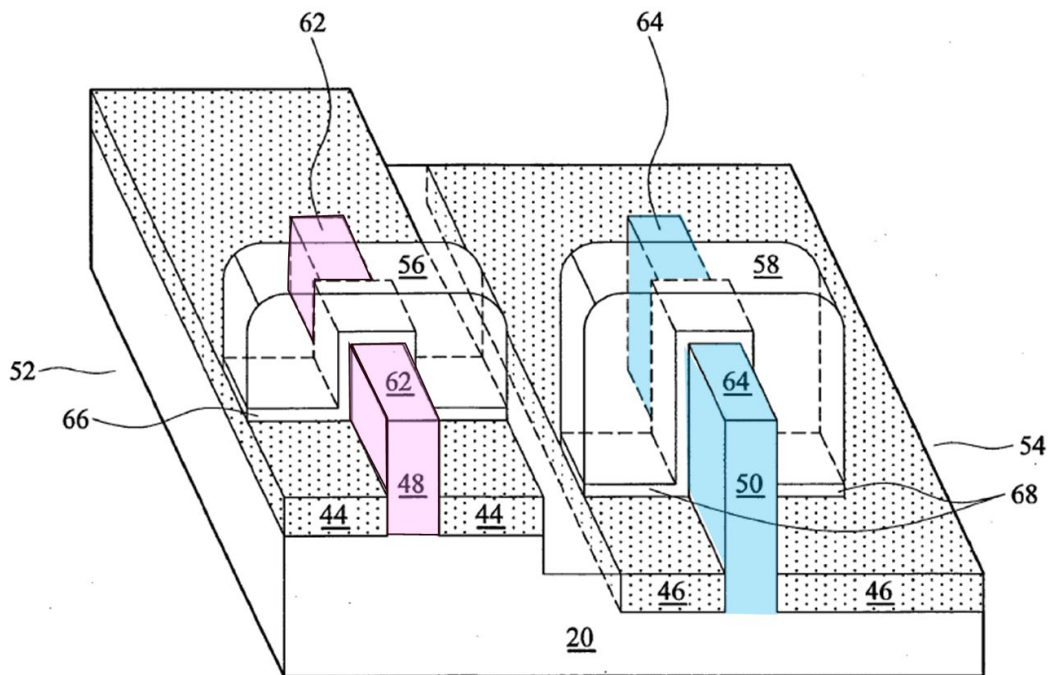


FIG. 9

EX1010, FIG. 9 (annotated)

## 2. Combination of Basker, Hill, and Yu

As discussed for claim 1 of Ground 1 for limitations [1.b]/[9.b]/[15.b], the Basker-Hill combination discloses “odd fins” or “first fins” (Si fins) of the FinFETs, and “even fins” or “second fins” (SiGe fins) of the FinFETs, which are exemplified in Figure 7\*(c) below. *Supra* §VI.A.4.(iii); EX1002, ¶¶99-107.

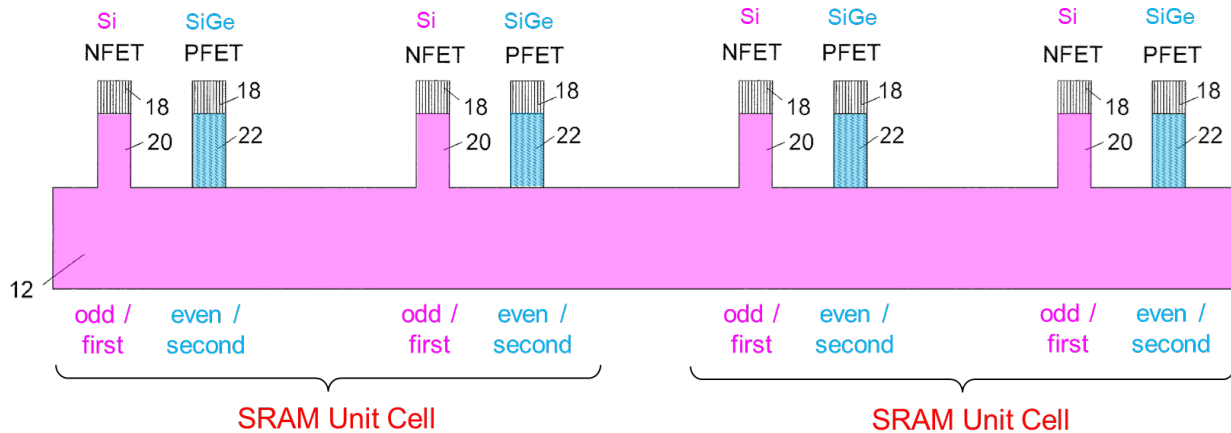


**FIG. 7\*(c)**

The Basker-Hill combination does not expressly disclose “the **even** fins...are further **different** from the **odd** fins...**in height**” or “the **second** fins...are further **different** from the **first** fins...**in height**.” Nevertheless, a POSITA would have found it obvious to implement such a structure in view of Yu’s teachings. EX1002, ¶¶99-100.

Like Basker, Yu discloses FinFETs for use in ICs and forming fins of the FinFETs by etching a bulk silicon substrate. §VI.B.1. Thus, a POSITA would have been motivated to consider Yu’s teachings when implementing FinFET structures like those disclosed in the Basker-Hill combination. EX1002, ¶100.

In view of Yu’s teachings/suggestions, including customizing “semiconductor fins with different heights on a same semiconductor chip” (EX1010, [0010], [0019]), a POSITA would have been motivated, and found obvious, to customize the fin heights of the FinFETs in an IC chip, e.g., those in the SRAM cells implemented in the Basker-Hill combination (as discussed for claims 1, 9, and 15). EX1002, ¶¶101-

104. For example, Yu explains performances of the FinFETs, e.g., the drive current thereof, may be modified by adjusting the channel width, which is a function of the fin height of the FinFET. *Id.*, [0002]-[0004]. Additionally, as discussed in §II.C, a POSITA at the time was aware and appreciated that the static noise margin of a SRAM cell depends on the dimensions of the FinFETs used to form the cell. EX1002, ¶104. For instance, the noise margin depends on the pull up ratio (PR) of the SRAM cell, which is a parameter for optimizing SRAM performance. For example, it has been reported PR should be in the range of 3 to 4 for SRAM cells to be functional. EX1033, 3; EX1002, ¶104. It was known PR is determined based on the pFinFET and nFinFET's dimensions, i.e.,  $PR = (W_{pFET}/L_{pFET}) / (W_{nFET}/L_{nFET})$ , where W is the channel width and L is the channel length of the pFinFET or nFinFET. EX1033, 1-2. Accordingly, a POSITA would have been motivated to customize the fin heights to, e.g., increase  $W_{pFET}$  and/or to reduce  $W_{nFET}$  (and/or to reduce  $L_{pFET}$  and/or to increase  $L_{nFET}$ ) to achieve the desired PR range. EX1002, ¶104.

As discussed above, given that the channel width W is a function of the fin height, a POSITA, guided by Yu's teachings and their state of art knowledge, would have found it obvious to customize fin heights to, e.g., increase  $W_{pFET}$  and/or to reduce  $W_{nFET}$  in a SRAM cell in the Basker-Hill combination to achieve the desired PR range. EX1002, ¶105. This would have resulted in the height of the pFinFET's

fins (“even” or “second” fins) being different from the height of the nFinFET fins (“odd” or “first” fins) in the Basker-Hill combination. EX1002, ¶105.

A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Basker-Hill-Yu combination, particularly given that Basker and Yu disclose multiple similar aspects of semiconductor structures and fin fabrication process steps, e.g., forming fins by etching a bulk silicon substrate. EX1002, ¶106. The Basker-Hill-Yu combination would have been motivated by teaching/suggestion/motivation in the prior art (e.g., discussed above) and involved applications of known technologies (e.g., known process to etch a substrate to form fins of FinFETs) according to known methods (e.g., known method of forming trenches of different depths on a substrate to create height differences between fins) to yield the predictable result of a functional SRAM cell having, e.g., a proper pull-up ratio (PR) and thus static noise margin. EX1002, ¶¶106-107; *KSR*, 550 U.S. at 416.

### **3. Claims 2, 10, and 16**

The Basker-Hill combination in view of Yu discloses and/or suggests these limitations. EX1002, ¶¶98-108. As discussed above in §VI.B.2, a POSITA would have been motivated, and found obvious, to customize the fin heights to, e.g., increase  $W_{pFET}$  and/or to reduce  $W_{nFET}$  (and/or to reduce  $L_{pFET}$  and/or to increase  $L_{nFET}$ ) to achieve the desired PR range in the Basker-Hill combination. §VI.B.2.

Accordingly, the Basker-Hill-Yu combination discloses and/or suggests claims 2, 10, and 16. EX1002, ¶¶98-108.

Additionally, the height difference of the nFinFET and pFinFETs in a SRAM cell was known as a “result-effective variable” because it affects SRAM’s performance, e.g., the static noise margin of the SRAM cell. EX1033, 1; §II.C. In fact, Yu explicitly teaches “*customiz[ing] fin heights...so that the FinFETs may have customized performance.*” EX1010, [0004], [0010]. Therefore, a POSITA would have been motivated to customize the performance of pFinFETs and nFinFETs in the Basker-Hill combination by customizing their fin heights such that the SiGe fins (“even” or “second” fins) “are...different from” Si fins (“odd” or “first” fins) “in height” to achieve an optimum SRAM design/structure. Thus, claims 2, 10, and 16 would have been obvious. EX1002, ¶108. *E.I. DuPont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1010 (Fed. Cir. 2018) (“discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art.”); *In re Applied Materials, Inc.*, 692 F.3d 1289, 1297 (Fed. Cir. 2012) (“A recognition in the prior art that a property is affected by the variable is sufficient to find the variable result-effective.”). Indeed, the ’292 patent provides no evidence that fins having “height” difference produces any new/unexpected result. EX1002, ¶108.

**C. Grounds 3A and 3B: Inaba anticipates (Ground 3A) and Renders Obvious (Ground 3B) Claims 1, 5, 7-9, 13, 15, and 19**

**1. Inaba**

Because Inaba is in the same field (FinFET devices) and reasonably pertinent to a problem the '292 Patent purports to address (FinFET devices fabrication), Inaba is analogous art. EX1001, 1:15-35; EX1005, Abstract; EX1002, ¶¶36-37. Inaba discloses a SRAM cell 20 having six transistors, including four nFinFETs N1-N4 and two pFinFETs P1-P2. EX1005, [0053]-[0057], FIG. 1; EX1002, ¶¶115-117.

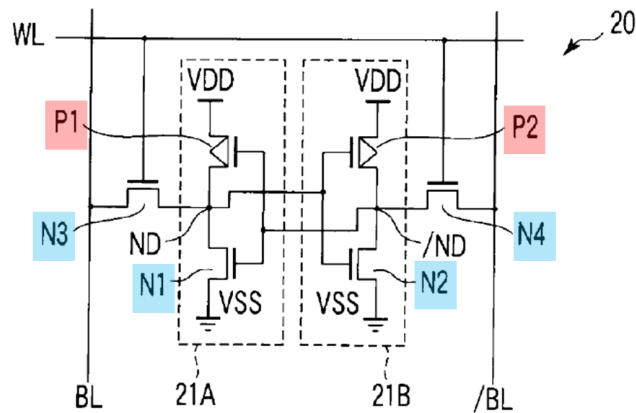


**FIG. 1**

EX1005, FIG. 1 (annotated)

Figure 11A (below) of the last embodiment shows a SRAM circuit layout including two nFinFETs N1a and N1b connected in parallel to form N1, two nFinFETs N2a and N2b connected in parallel to form N2, two nFinFETs N3 and N4 (grey), and two pFinFETs P1 and P2. EX1005, [0054], [0164].

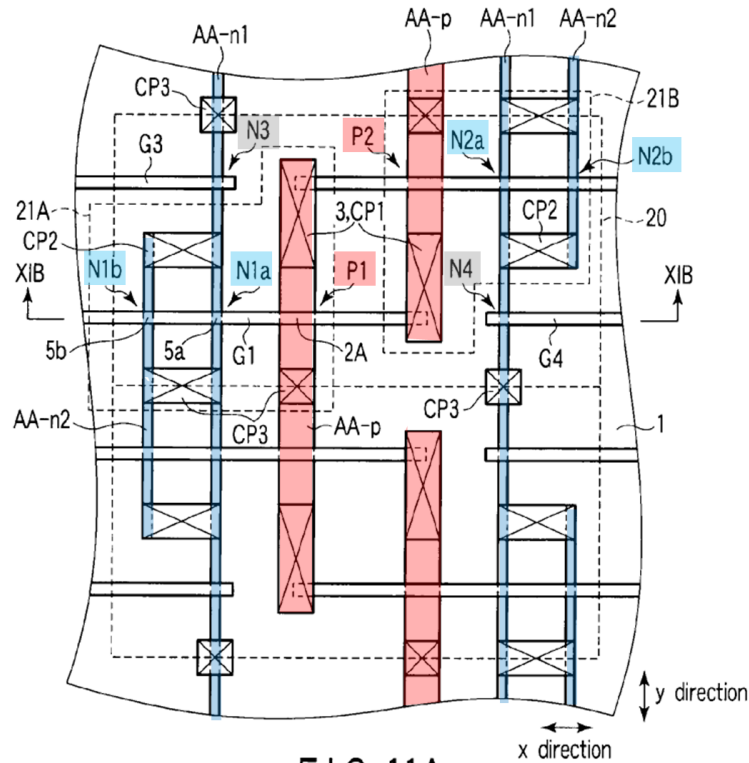


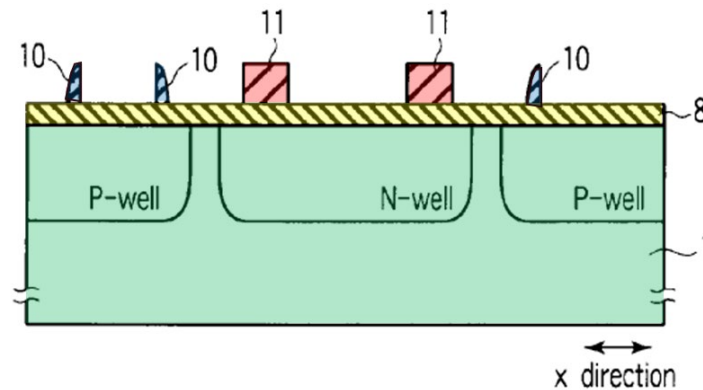
FIG. 11A

EX1005, FIG. 11A (annotated)

In Inaba's SRAM cell, transistor N1 is formed using two nFinFETs N1a and N1b and transistor N2 is formed using two nFinFETs N2a and N2b. Moreover, because transistor N1 (shown in Figure 5A) is formed using nFinFETs N1a and N1b connected in parallel (shown in Figure 11A) (EX1005, [0164]), a POSITA would have understood fin 5 (shown in Figures 5A/B) used for forming transistor N1 corresponds to fins 5a and 5b used for forming transistors N1a and N1b (shown in Figure 11A) respectively. EX1005, [0054], [0165]; EX1002, ¶118. Similarly, because transistor N2 (shown in Figure 5A) is formed using transistors N2a and N2b (shown in Figure 11A), a POSITA would have understood that fin 5 (shown in

Figures 5A/B) used for forming transistor N2 correspond to fins 5a and 5b for transistors N2a and N2b (shown in Figure 11A) respectively.<sup>7</sup> EX1002, ¶118.

According to Inaba, the fabrication of SRAM cell 20<sup>8</sup>, includes, e.g., forming mask layer 8 (yellow), sidewall mask 10 (blue), and resist mask 11 (red) on semiconductor substrate 1 that includes p- and n-wells, as shown in Figure 13B, where mask 10 resides in the region where nFinFETs are to be formed, and a resist mask 11 is for forming pFinFETs each having a fin width greater than that of the nFinFETs. EX1005, [0158]-[0159], [0169]-[0172]; EX1002, ¶119.



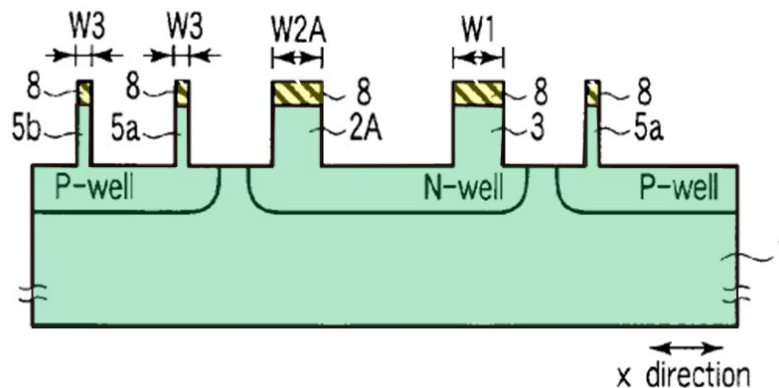
EX1005, FIG. 13B (annotated)

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<sup>7</sup> While fin 5b is not shown in Figure 14, as explained below, it is present as can be seen from FIG. 14\* where the cross-section line in Figure 11A has been moved north of line XIII B in Figure 13A, as discussed below for limitations [1.b]/[9.b]/[15.b].

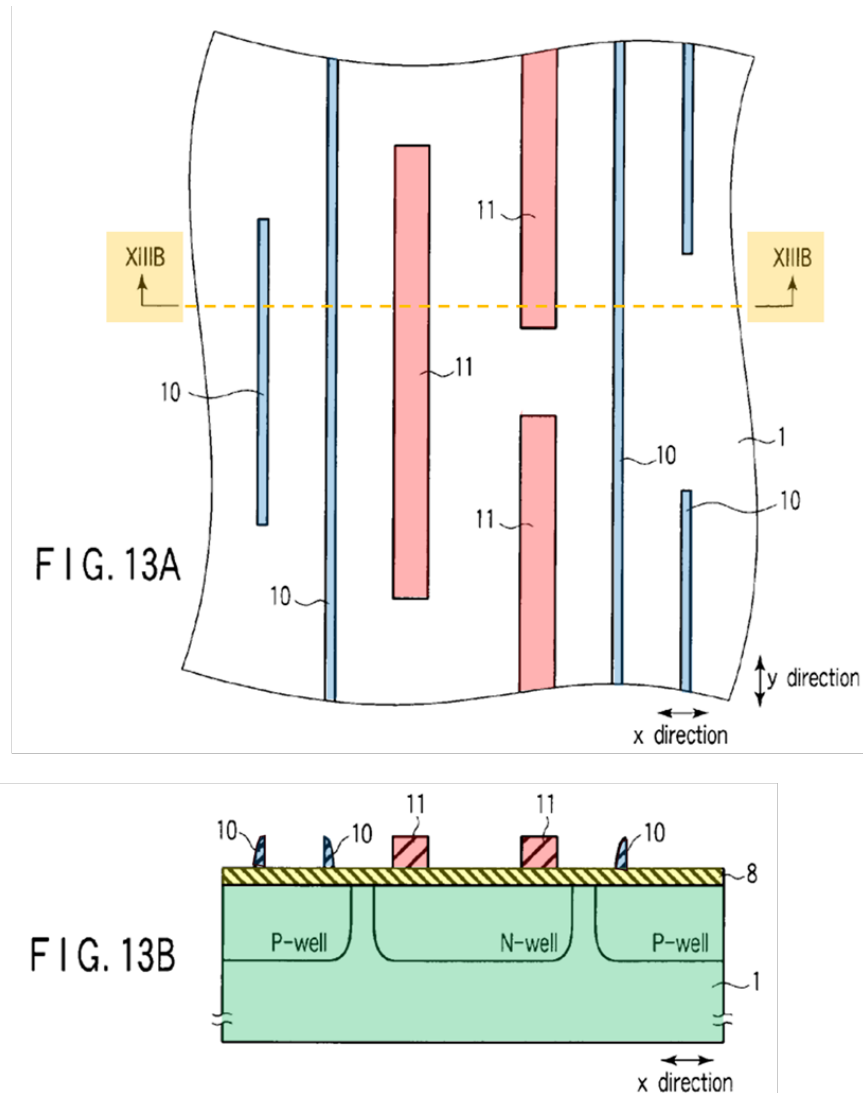
<sup>8</sup> SRAM cell 20 is consistently referenced in the first to fourth and last embodiments. EX1005, FIGS. 1-2A, 5A, 6A, 7A, 11A.

As shown in Figure 14 below, by using these masks (shown in Figure 13B), substrate 1 is etched to form (1) fins 5a, 5b in the region where nFinFETs are to be formed and (2) fins 2A and 3 in the region where pFinFETs are to be formed. EX1005, [0173]. Gate electrodes and source/drain layers are then formed to produce the FinFETs. *Id.*, [0174]-[0176]. EX1002, ¶¶120-121.



EX1005, FIG. 14 (annotated)

Inaba explains that “FIG. 13B is a sectional view taken along line XIII B-XIII B of FIG. 13A” as shown below. EX1005, [0044].



**EX1005, FIG. 13A (top, annotated), 13B (bottom, annotated)**

Since there are 6 fins shown in the upper half of Figure 13A, a POSITA would have understood that a sectional view showing 6 fins could be obtained, for example, along a line located just north of line XIII B, e.g., line XIII B\* or XIII B\*\* as shown

in Figure 13B\*<sup>9</sup> below. A POSITA would have also understood that how the sectional view is taken would not affect the relative fin width relationship among the six fins, which can be ascertained from the top view (Fig. 13A). As shown below 13B\*, the sectional view includes one additional sidewall mask 10 (purple).  
EX1002, ¶123.

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<sup>9</sup> FIG. 13B\* is a modification of FIG. 13B based on moving the line XIIIIB in FIG. 13A to line XIIIIB\* in FIG. 13A\*.

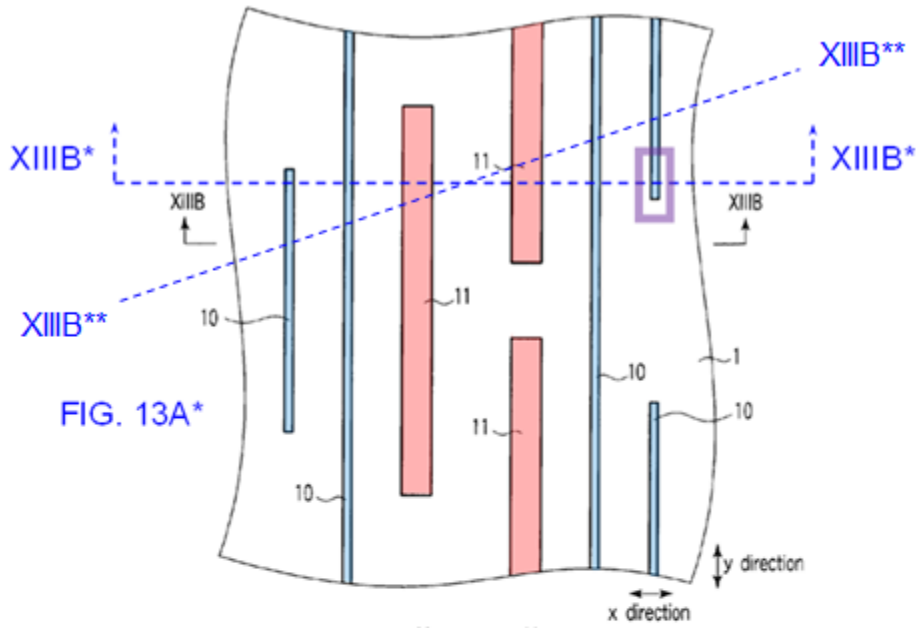


FIG. 13A\*

FIG. 13B\*

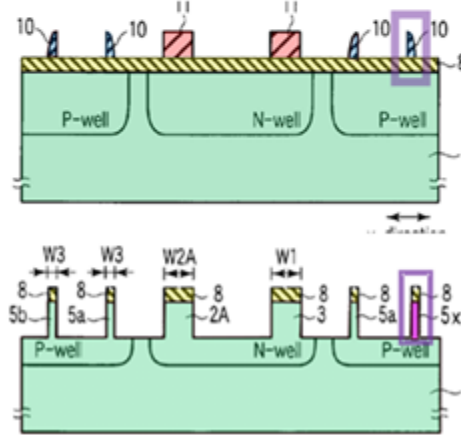
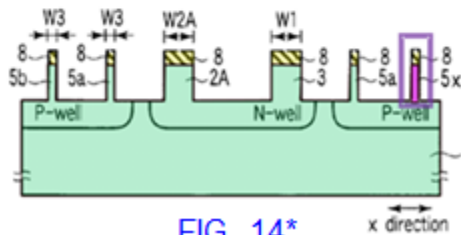


FIG. 14\*



Given that the fins are defined by the masks 10, 11 as discussed above in relation to Figure 13B, a POSITA would have also understood that, following the etch process, the sectional view along line XIIIB\* or XIIIB\*\* includes fin 5x

(purple). EX1005, [0173]; EX1002, ¶124. The location of fin 5x in Figure 14\*<sup>10</sup> is consistent with the location of mask 10 in Figures 12A and 12B and also consistent with the location of the N2b transistor in Figure 11A. EX1005, [0171]-[0172], [0164]. Thus, Inaba discloses forming at least six fins of FinFETs in a single SRAM cell, where widths of fins 2A and 3 (W2A and W1 respectively) are greater than the widths of fins 5a, 5b, 5x (W3), as shown in Figures 11A and 14\* below. EX1002, ¶124.

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<sup>10</sup> FIG. 14\* is a modification of FIG. 14 based on moving the line XIIIIB in FIG. 13A to line XIIIIB\* in FIG. 13A\*.

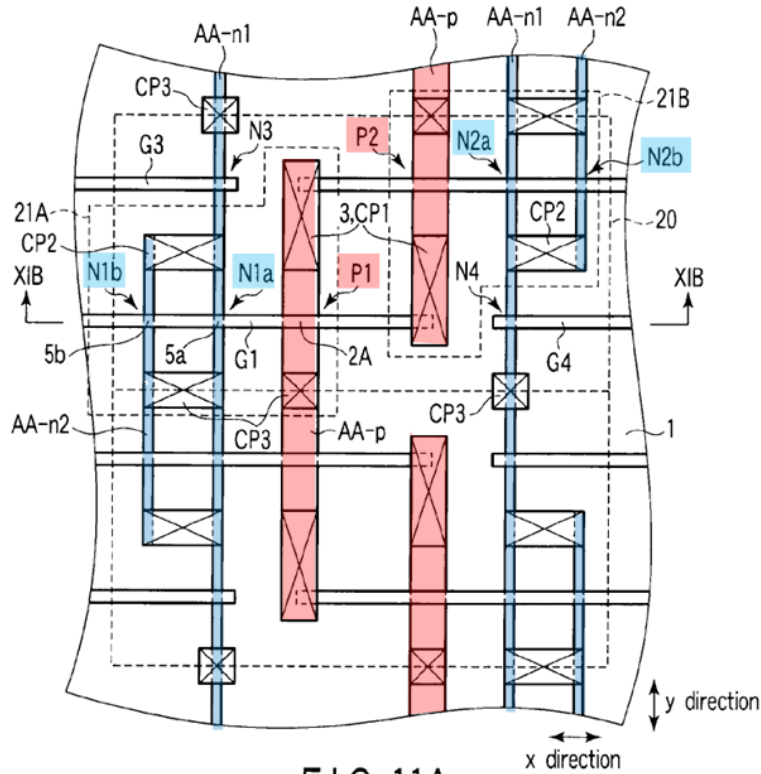


FIG. 11A

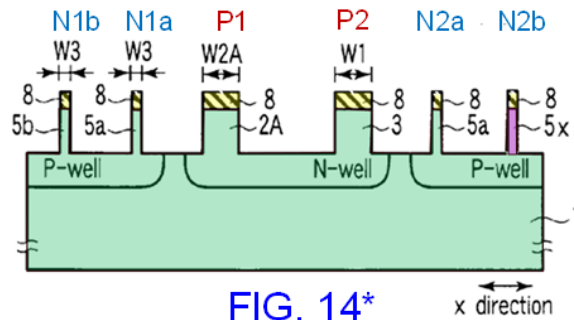


FIG. 14\*

FIG. 14\* (annotated and modified to include fin 5x)

As explained below, Inaba discloses and/or suggests “a semiconductor structure for forming FinFET[s]” as claimed.<sup>11</sup> EX1002, ¶¶109-114; §VI.C.2(i).

<sup>11</sup> *Supra* §III.C.

Inaba initially describes its structure in the context of four embodiments in connection with Figures 1-4B (first embodiment) (EX1005, [0017]-[0024], [0051]-[0095]), Figures 5A-5B (second embodiment) (*id.*, [0025]-[0026], [0096]-[0113]), Figures 6A-6B (third embodiment) (*id.*, [0027]-[0028], [0114]-[0123]), and Figures 7A-10B (fourth embodiment) (*id.*, [0029]-[0038], [0125]-[0157]). Inaba explains that each of these embodiments are related and build from each other. *Id.*, [0096], [0114], [0125]. EX1002, ¶110.

Inaba describes a last embodiment in connection with Figures 11A-14, which is a modification of the first to fourth embodiments. EX1005, [0039]-[0045], [0158]-[0177]. Consistently, Inaba explains that in the last embodiment, “[t]he same parts [discussed in the last embodiment] as those in the first to fourth embodiments are indicated by the same reference numerals and a detailed explanation of them will be omitted.” *Id.*, [0159]; EX1002, ¶¶111-112.

Ground 3A demonstrates how Inaba’s last embodiment satisfies the challenged claims. In doing so, any disclosures identified from Inaba’s other embodiments are in context of the modification to those embodiments as expressly contemplated by Inaba (as explained above, §VI.C.1). For example, a POSITA

would have understood from Inaba the teachings related to Inaba's other embodiments are attributed to the last embodiment.<sup>12</sup> EX1002, ¶113.

Ground 3B demonstrates a POSITA would have also found it obvious to implement those other embodiments' features in the last embodiment. EX1002, ¶114. A POSITA would have been motivated to implement those features at least because (1) Inaba discloses that the embodiments are related and build from each other and (2) the embodiments are disclosed in the same reference and associated with the same subject matter (forming a SRAM cell). EX1005, [0050], FIG. 1. EX1002, ¶114. *KSR*, 550 U.S. at 421 ("A person of ordinary skill is also a person of ordinary creativity, not an automaton.").

## **2. Claims 1, 9, and 15**

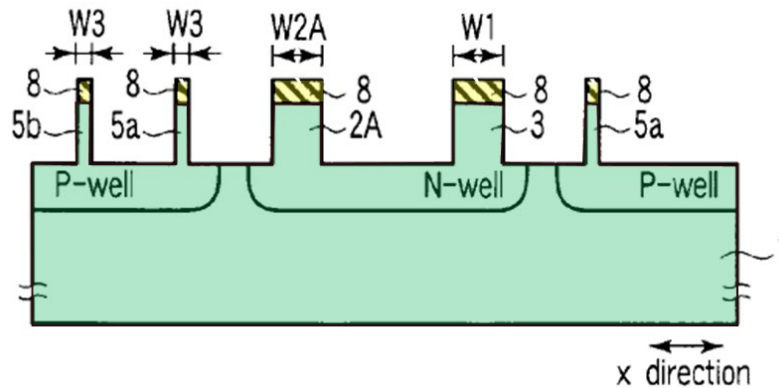
### **(i) [1.pre]/[9.pre]/[15.pre]**

Inaba discloses and/or suggests these preambles. EX1002, ¶¶115-121; *supra* §VI.C; EX1005, Abstract, [0003], [0006], [0015]-[0016]. Inaba explains a known configuration of SRAM formed using FinFETs. EX1005, Abstract, [0047], [0160], [0167], [0176]; §VI.C.1.

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<sup>12</sup> The same is true for Grounds 4-5, which rely on Inaba's last embodiment corresponding to that explained here in Grounds 3A/3B. *Infra* §§IX.D-IX.E.

As discussed in §IV.C.1, Inaba discloses and/or suggests forming fins for FinFETs on a semiconductor substrate (e.g., as shown in Figure 14). §IV.C.1.

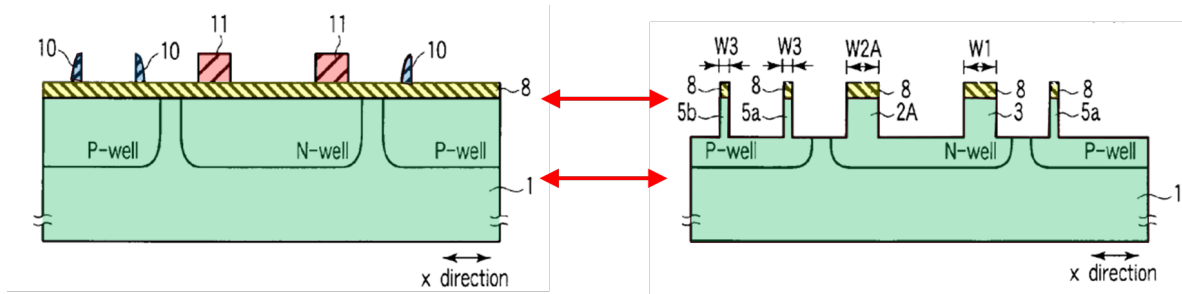


EX1005, FIG. 14 (annotated)

Accordingly, Inaba discloses and/or suggests a “semiconductor structure” (e.g., as shown in Figure 14) “for forming FinFETs” (preamble [1.pre] and [9.pre]) and “forming FinFET” (preamble [15.pre]). EX1002, ¶¶115-121.

(ii) [1.a]/[9.a]/[15.a]

Inaba discloses and/or suggests these limitations. EX1002, ¶122. Inaba discloses substrate 1 is a “semiconductor substrate.” EX1005, [0171].



EX1005, FIG. 13B (left annotated) and FIG. 14 (right annotated)

Inaba discloses “a top portion of the semiconductor substrate,” *e.g.*, as shown between the red arrows, “comprises a semiconductor material.” Inaba explains substrate 1 may be a “bulk semiconductor substrate.” EX1005, [0074], [0100], [0126], [0168], [0177]. Given that semiconductor substrate 1 is a “bulk” substrate, the entire semiconductor substrate, including its top portion, is formed of a semiconductor material, *e.g.*, silicon. *Id.*, [0081]. Accordingly, Inaba discloses and/or suggests “a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material.” EX1002, ¶122.

(iii) [1.b]/[9.b]/[15.b]

Inaba discloses these limitations under PO’s litigation allegations. §III.C; EX1002, ¶¶123-128. For example, Inaba, as shown in Figure 14\* below (discussed in §VI.C.1), discloses three groups of fins, *e.g.*, Groups 1-3, where Groups 1 and 3 each corresponds to “a plurality of **odd** [or **first**] fins of the FinFETs” and Group 2 corresponds to “a plurality of **even** [or **second**] fins of the FinFETs” of claims 1/9/15 *under PO’s litigation allegations* (see limitations [1.c]/[9.c]/[15.c] discussed in the next section). EX1002, ¶126.

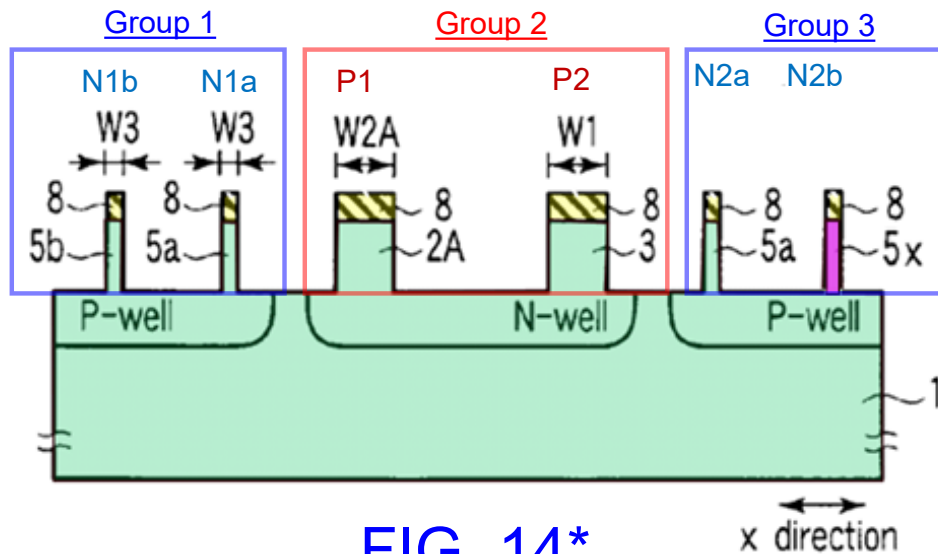


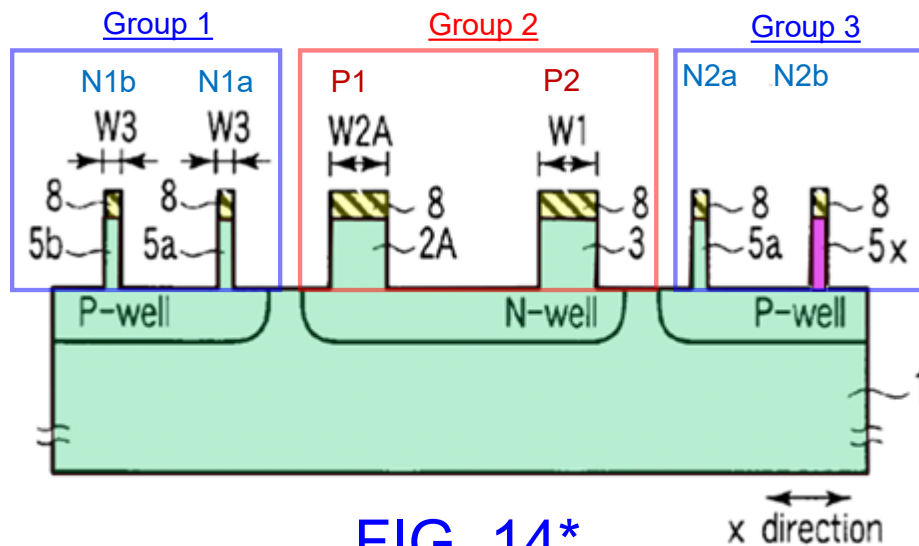
FIG. 14\*

As shown in Figure 14\* above, the Groups 1-3 fins are on semiconductor substrate 1 (“on the semiconductor substrate” as claimed) and protrude from the substrate. Additionally, as discussed above, by using mask layers 10, 11 shown in Figure 13B\*, semiconductor substrate 1 is etched to form the fins. EX1005, [0173]. Given that the mask layers 10, 11 atop the substrate define the location and feature size (e.g., width) of the fins, Inaba discloses Groups 1 and 3 are “defined from the semiconductor substrate” (limitation [1.b]) and “formed of the semiconductor material” comprised in the top portion of the semiconductor substrate (limitations [1.b]/[9.b]/[15.b]). *See also* §VI.C.2(ii). Additionally, as shown in FIG. 14\* and given that the fins are formed of the substrate by a masked etch process, Inaba

discloses and/or suggests Groups 1 and 3 “fins and the semiconductor substrate are in direct contact with each other” (limitations [9.b]/[15.b]). EX1002, ¶¶127-128.

(iv) [1.c]/[9.c]/[15.c]

Inaba discloses and/or suggests these limitations under PO’s litigation allegations. EX1002, ¶¶129-132. As discussed for limitations [1.b]/[9.b]/[15.b], the fins as shown in Figure 14\* below, including Group 2 fins (corresponding to “a plurality of even [or **second**] fins of the FinFETs” of claims 1/9/15 *under PO’s litigation allegations*), are on semiconductor substrate 1 (“on the semiconductor substrate” as claimed).



As shown in FIG. 14\*, Group 2 fins reside between Groups 1 and 3 fins (“between the odd fins of the FinFETs” under PO’s litigation allegations), as required by limitations [1.c] and [9.c]. Likewise, Inaba discloses “each of the second

fins of the FinFETs is located between two first fins of the FinFETs” (limitation [15.c]) under PO’s litigation allegations, given that each of the fins in Group 2 is located between two fins, each of Groups 1 and 3. Additionally, Group 2 fins are wider than Groups 1 and 3 fins and thus differ from them in width. EX1005, [0169]-[0173]. Thus, Inaba discloses and/or suggests limitations [1.c]/[9.c]/[15.c] under PO’s litigation allegations. EX1002, ¶¶129-132.

### 3. Claim 5, 13, and 19

Inaba discloses and/or suggests these limitations. As discussed for limitations [1.b]/[9.b]/[15.b], Groups 1 and 3 fins (“the odd fins of the FinFETs” under PO’s litigation allegations) are defined from *silicon* substrate 1 and formed of the same. EX1005, [0081], [0177]. Thus, Inaba discloses and/or suggests these limitations under PO’s litigation allegations. EX1002, ¶133.

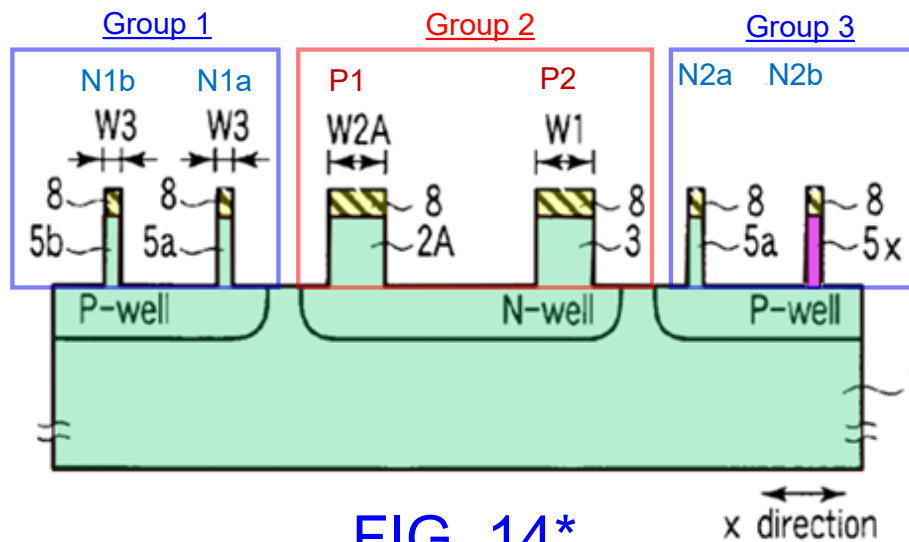
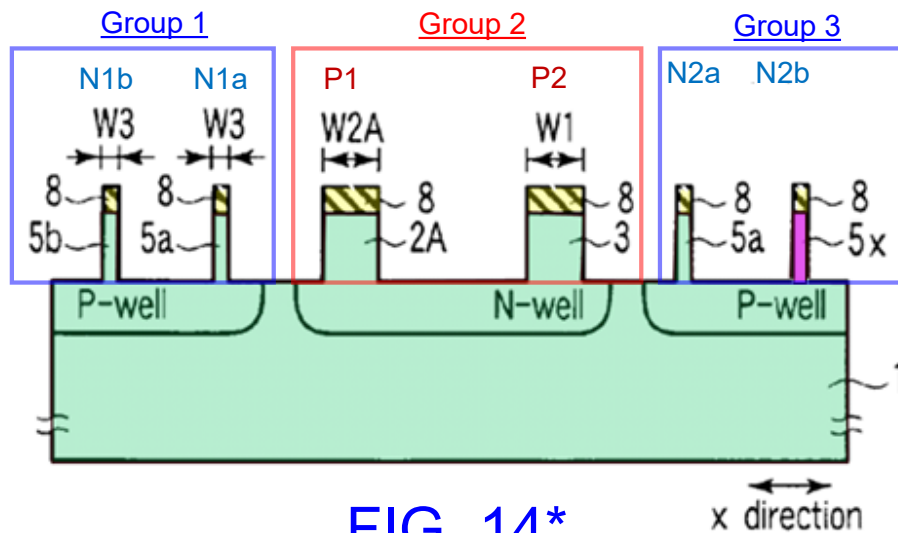


FIG. 14\*

#### 4. Claim 7

Inaba discloses and/or suggests this limitation. EX1002, ¶¶134-135. As discussed for limitations [1.b]/[9.b]/[15.b], Groups 1 and 3 fins (“the odd fins of the FinFETs” under PO’s litigation allegations) are defined from *silicon* substrate 1 and formed of the same. Consistent with Figure 14\* below, and given that the fins are formed of the substrate by a masked etch process, Groups 1 and 3 fins are connected to silicon substrate 1. EX1005, [0173].



A POSITA would have understood, given Groups 1 and 3 fins and the substrate are connected and both are the same semiconductor material, i.e., silicon, these fins and the substrate are electrically connected. Thus, Inaba discloses and/or suggests claim 7 under PO’s litigation allegations. EX1002, ¶135.

**5. Claim 8**

Inaba discloses and/or suggests this limitation. As discussed for limitations [1.a]/[9.a]/[15.a], semiconductor substrate 1 may be a “bulk semiconductor substrate” (EX1005, [0100], [0126], [0177]) and thus the entire substrate is formed of “a single layer structure” of semiconductor material. EX1002, ¶136.

**D. Ground 4: Claims 3, 4, 6, 11, 12, 14, 17, 18, and 20 Are Obvious Over Inaba and Basker**

**1. Combination of Inaba and Basker**

Although Inaba does not expressly disclose “the [even/second] fins of the FinFETs comprise an epitaxy material” (claim 3) a POSITA would have found it obvious to implement this feature in view of Basker. EX1002, ¶¶137-146.

As discussed above for limitations [1.pre]/[9.pre]/[15.pre] in Ground 1, Basker discloses the use of Si fin for nFinFETs and SiGe fins for pFinFETs. *Supra* §VI.A.4(i); §VI.A.1. Like Inaba, Basker discloses FinFETs formed on a bulk semiconductor substrate made of monocrystalline silicon. EX1006, [0020], [0025]. Also like Inaba, Basker discloses an nFinFET that “is formed on a fin made from a substrate material” (*id.*, [0020]), i.e., silicon fin (*id.*, [0038]) and the fins are formed by using a mask and an etch process (*id.*, [0025]-[0029]). Thus, a POSITA would have been motivated to consider Basker’s teachings in the same technical field when implementing the semiconductor devices of Inaba. EX1002, ¶138.

Basker additionally discloses improving the pFinFET performance by adding Ge/SiGe to silicon fins to **form SiGe fins**. EX1006, [0020]-[0021]. As discussed for claims 3/11/17 in Ground 1 (§VI.A.5), Basker discloses forming SiGe fins by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22. *Id.*, [0005], [0020]-[0021], [0031]-[0032], [0041], claim 1. Since the resulting SiGe fins incorporate the epitaxially deposited material, the resulting SiGe fins “comprise an epitaxy material.” Also, a POSITA would have understood that Basker’s SiGe fin formation results in epitaxy material and thus the resulting SiGe fins “comprise an epitaxy material.” EX1013, 2; EX1038, 3-4. Additionally, a POSITA would have known that SiGe fins can also be formed using, e.g., CVD and MBE, and would have found it obvious to use any of them. EX1039, 4:23-5:9. Thus, Basker discloses and/or suggests SiGe “fins of the FinFETs comprise an epitaxy material.” EX1002, ¶139.

A POSITA would have been motivated to form SiGe fins for pFinFETs in a semiconductor structure as discussed in Inaba (e.g. fins 2A, 3 in Figure 14 of Inaba) in view of Basker. *Id.*, ¶¶140-141. **First**, a POSITA would understand there has been a general trend at the relevant time to include Ge/SiGe into the transistor’s channel, which traditionally has been made of silicon. EX1025, 1; EX1002, ¶141. In fact, it was known that “SiGe channel [FinFET] is an attractive replacement” of Si channel pFinFETs. EX1026, 1; EX1030, 2; EX1031, 1; §II.B. A POSITA would

have understood SiGe fins improve hole mobility for pFinFETs and thus improve current drive of the transistors and speed of transistors' operation. EX1002, ¶142; EX1016, 1-2, 4; EX1017, 1; EX1018, 1; §II.B. And the use of SiGe fins also improves NBTI reliability for pFinFETs (where NBTI reliability was a major issue for the semiconductor industry), and thus improves the performance of SRAM devices as disclose in Inaba. EX1002, ¶142; EX1016, 1, 2, 4; EX1017, 1; EX1018, 1; EX1025, 1; EX1026, 1.

**Second**, as Basker explains, it is “advantageous” to impart strain to the fin, and the strain caused by adding Ge to the silicon fins “improves pFET performance.” EX1006, [0021], [0031], [0038]; EX1002, ¶143.

**Third**, Basker explains using a silicon fin for an nFinFET and using a SiGe fin for a pFinFET provide “the correct threshold voltages for both [nFinFET] and [pFinFET],” allowing use of “the same gate dielectric...and the same gate conductor...,” which would have simplified the fabrication processes and reduced cost. EX1006, [0038]; EX1002, ¶144; EX1023, [0008], [0016], [0027]; §II.B.

In view of Basker's teachings/suggestions in context of the state of art knowledge at the time, a POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving the Inaba-Basker combination. EX1002, ¶145. Indeed, Basker itself discloses adding Ge to the silicon fin results in “an ideal combination” of beneficial features (such as proper threshold

voltages for both nFinFET and pFinFET and use of a (110) surface for the pFET finFET). EX1006, [0021]. Additionally, Basker explains the disclosed features may be applied to many useful IC components. *Id.*, [0021]. Furthermore, combining Inaba with Basker would have been motivated by teaching/suggestion/motivation in the prior art (e.g., discussed above) and involved applications of known technologies (e.g., known use of SiGe for pFinFETs) according to known methods (e.g., known method of forming SiGe fins) to yield the predictable result of improved pFinFETs and other benefits discussed above in the Inaba-Basker combination. EX1002, ¶¶145-146; *KSR*, 550 U.S. at 416.

## **2. Claims 3, 11, and 17**

The Inaba-Basker combination discloses and/or suggests these limitations. EX1002, ¶¶137-146. As discussed in §VI.D.1, although Inaba does not expressly disclose “the [even or second] fins of the FinFETs comprise an epitaxy material,” a POSITA would have been motivated to implement such a feature, e.g., by forming SiGe fins for pFinFETs as discussed in Inaba in view of Basker. §VI.D.1; EX1002, ¶¶137-146.

For the reasons discussed in §VI.D.1, a POSITA would have been motivated, and found obvious, to form pFinFETs, as disclosed in Inaba (e.g., P1 and P2 of Group 2 fins in Figure 14\* below) having SiGe fins that “comprise an epitaxy material” as taught/suggested by Basker. EX1002, ¶¶137-145. Thus, the Inaba-

Basker combination discloses and/or suggests claims 3, 7, and 11 under PO's litigation allegations (§§VI.C.3; III.C). EX1002, ¶146.

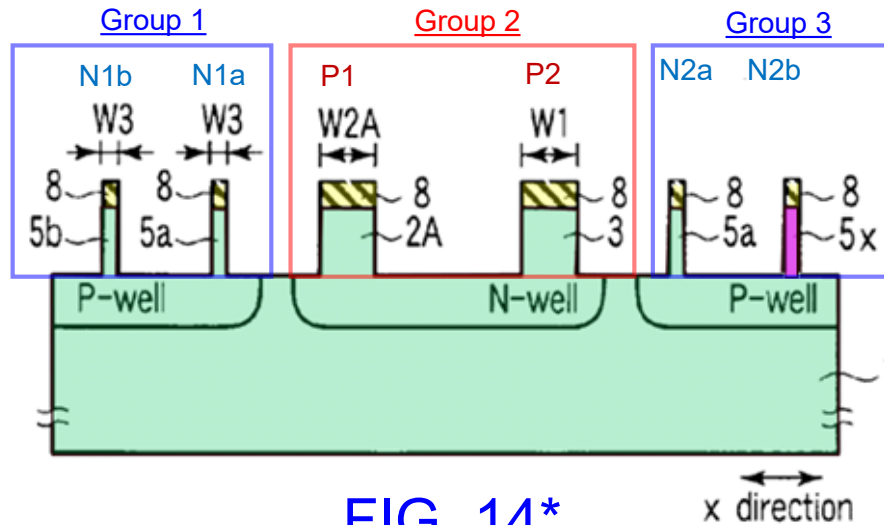


FIG. 14\*

### 3. Claims 4, 12, and 18

The Inaba-Basker combination discloses and/or suggests these limitations. *Supra* §§VI.C.2(iii)-(iv); IV.D.2. As discussed for limitations [1.b]/[9.b]/[15.b], Inaba discloses the Groups 1 and 3 fins are formed from the **silicon** substrate. And as discussed for claims 3, 11, and 17, Inaba in view of Basker discloses forming **SiGe fins** for pFinFETs, i.e., the Group 2 fins. *id.* Accordingly, for reasons explained for claims 1, 9, 15, and those for claims 3, 11, and 17, the Inaba-Basker combination discloses and/or suggests claims 4, 12, and 18 under PO's litigation allegations. EX1002, ¶147.

**4. Claim 6, 14, and 20**

The Inaba-Basker combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18. *Supra* §IV.D.3; EX1002, ¶148.

**E. Ground 5: Claims 2, 10, and 16 Are Obvious Over Inaba and Yu**

**1. Combination of Inaba and Yu**

Inaba does not expressly disclose “the **even** fins...are further **different** from the **odd** fins...**in height**” (claims 1 and 9) or “the **second** fins...are further **different** from the **first** fins...**in height**” (claim 15). Nevertheless, a POSITA would have found it obvious to implement such features in the Inaba structure view of Yu’s teachings. EX1002, ¶¶149-150; §VI.C.2(iii)-(iv).

Like Inaba, Yu discloses FinFETs for use in ICs (EX1010, [0001]-[0002], [0019] (“semiconductor chip”)) and forming fins of the FinFETs by etching a bulk silicon substrate (*id.*, [0028], [0020]-[0024]). §VI.B.1. Thus, a POSITA would have been motivated to consider Yu’s teachings when implementing a semiconductor structure like those disclosed in Inaba. EX1002, ¶151.

As discussed in §VI.B (Ground 2), Yu discloses forming “customized fin heights...so that the FinFETs may have customized performance.” EX1010, [0010]; *supra* §VI.B; EX1010, [0023]-[0029]; EX1002, ¶152. In view of Yu’s teaching, including customizing “semiconductor fins with different heights on a same semiconductor chip” (EX1010, [0010], [0019]), a POSITA would have been

motivated to customize the fin heights of the FinFETs in an IC chip, e.g., those in the SRAM cells disclosed/suggested by Inaba as discussed for claims 1, 9, and 15 in Grounds 3A/3B. EX1002, ¶153; §§VI.C.1-3. As discussed for Ground 2, Yu explains performances of the FinFETs, e.g., static noise margin depends on the dimensions of the FinFETs used to form the cell. §VI.B. Also discussed therein, the static noise margin depends on the pull up ratio (PR) of the SRAM cell, where PR is a parameter for optimizing SRAM performance. For example, it has been reported that PR should be in the range of 3 to 4 for SRAM cells to be functional. §VI.B.1; EX1033, 1-3. Accordingly, a POSITA would have been motivated to customize the fin heights to, e.g., increase  $W_{\text{pFET}}$  and/or to reduce  $W_{\text{nFET}}$  (and/or to reduce  $L_{\text{pFET}}$  and/or to increase  $L_{\text{nFET}}$ ) to achieve the desired PR range in the SRAM cell of Inaba. EX1002, ¶153.

As discussed above, given that the channel width  $W$  is a function of the fin height, a POSITA, guided by Yu's teaching and their state of art knowledge, would have found it obvious to customize fin heights to, for example, increase  $W_{\text{pFET}}$  and/or to reduce  $W_{\text{nFET}}$  in a SRAM cell (in the Inaba structure discussed above) to achieve the desired PR range. EX1002, ¶154. This would have resulted in the height of the pFinFET's fins ("even" or "second" fins) being different from the height of the nFinFET fins ("odd" or "first" fins) in the SRAM cell of Inaba. EX1002, ¶154.

A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the Inaba-Yu combination, particularly given that Inaba and Yu shared similar fin fabrication process steps, e.g., forming fins by etching a bulk silicon substrate as discussed above. EX1002, ¶155. Combining Inaba with Yu would have been motivated by teaching/suggestion/motivation in the prior art (e.g., discussed above) and involved applications of known technologies (e.g., known process to etch a substrate to form fins of FinFETs) according to known methods (e.g., known method of forming trenches of different depths on a substrate to create height differences between fins) to yield the predictable result of a functional SRAM cell, e.g., having a proper pull-up ratio (PR) and thus static noise margin. EX1002, ¶155. *KSR*, 550 U.S. at 416.

## **2. Claims 2, 10, and 16**

The Inaba-Yu combination discloses and/or suggests these limitations. EX1002, ¶¶149-157.

As discussed for limitations [1.b]/[9.b]/[15.b], Inaba discloses “odd fins” or “first fins” (Group 1 fins, including N1a, N1b fins; Group 3 fins, including N2a, N2b fins) of the FinFETs, and “even fins” or “second fins” (Group 2 fins, including P1, P2 fins) of the FinFETs under PO’s litigation allegations, as shown in Figure 14\* below. *Supra* §VI.C.2(iii)-(iv). Additionally, as discussed above in §IV.E.1, a POSITA would have been motivated to customize the fin heights to, e.g., increase

$W_{pFET}$  and/or to reduce  $W_{nFET}$  (and/or to reduce  $L_{pFET}$  and/or to increase  $L_{nFET}$ ) to achieve the desired PR range such that the Group 2 fins (“even” or “second” fins) “are...different from” Group 1/3 fins (“odd” or “first” fins) “in height.” EX1002, ¶¶149-156.

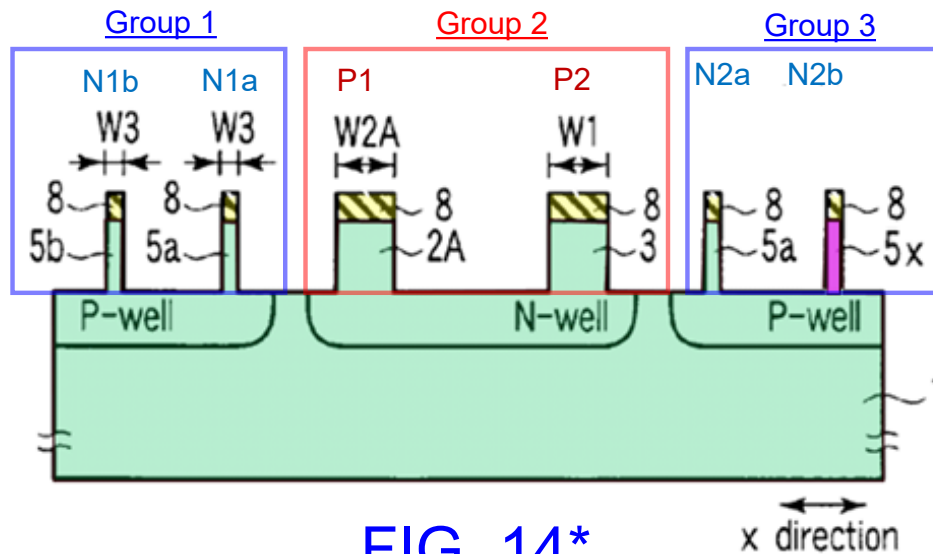


FIG. 14\*

EX1005, FIG. 14\*

Moreover, as discussed for Ground 2, a POSITA understood the height difference of the nFinFET and pFinFETs in a SRAM cell is a “result-effective variable.” EX1033, 1; §VI.B; §II.C. Thus, claims 2, 10, and 16 were obvious. *DuPont*, 904 F.3d at 1010; *Applied Materials*, 692 F.3d at 1297. This is especially true given that the ’292 patent provides no evidence that fins having “height” difference produces any new/unexpected result. EX1002, ¶157.

**F. Ground 6: Claims 1, 3-9, 11-15, and 17-20 Are Obvious Over Liaw and Basker**

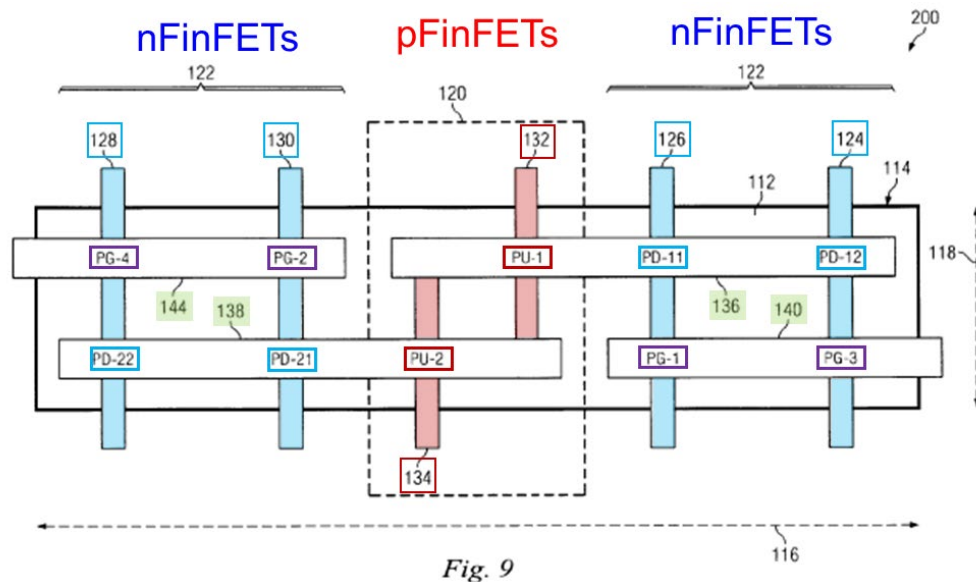
**1. Liaw**

Because Liaw is in the same field (FinFET devices) and reasonably pertinent to a problem the '292 Patent purports to address (FinFET devices fabrication), Liaw is analogous art. EX1001, 1:15-35; EX1008, 1:49-2:24; EX1002, ¶¶40-41. Liaw discloses a semiconductor device, e.g., SRAM, using FinFETs. EX1008, Abstract, 1:49-2:24, 2:61-64, 2:64-3:21. As shown in Figure 9 below, Liaw discloses a SRAM cell 200, including four pull-down FinFETs, PD-11, PD-12, PD-21, PD-22 (blue), two pull-up FinFETs, PU-1 and PU2 (red), and four pass-gate FinFETs, PG-1, PG-2, PG-3 and PG-4 (purple).<sup>13</sup> *Id.*, 10:6-17, 11:16-18. Liaw explains the pull-down device is formed with an nFinFET, the pull-up device formed with a pFinFET, and the pass-gate device formed with an nFinFET. *Id.*, 1:61-2:9, 2:66-3:3; 3:22-26,

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<sup>13</sup> Liaw discloses SRAM cell 200 (FIG. 9) is similar to SRAM cell 110 (FIG. 2) except SRAM cell 200 includes four pull-down devices and four pass-gate devices. EX1008, 10:6-11. Liaw explains SRAM cell 110 (FIG. 2) is a portion of the SRAM cell 100 (FIG. 1). *Id.*, 3:46-53. Thus, when explaining SRAM cell 200, Petitioners refer to disclosures associated those figures/descriptions, which a POSITA would have understood is associated with the features described in connection with SRAM cell 200. EX1002, ¶158.

claim 4; EX1002, ¶¶158-168.



EX1008, FIG. 9 (annotated)

As shown in the Figure 9 above, nFinFETs (PG and PD FinFETs) are formed on fin active regions (referred to as “fin” or “fins” hereafter) 124, 126, 128, 130 (blue) and pFinFETs (PU FinFETs) are formed on fins 132 and 134 (red). EX1008, 10:60-11:18. Liaw explains “SRAM cell 200 [as shown in Figure 9] is formed in a unit cell region 112 of the semiconductor substrate.” *Id.*, 10:44-46; EX1002, ¶¶160-161.

Liaw discloses with reference to Figure 7, “a semiconductor structure 180 as a portion of a SRAM cell, such as the SRAM cell 100 of FIG. 1 or the SRAM cell 110 of FIG. 2.” EX1008, 8:15-17. Liaw explains FIG. 7 is a sectional view of “a portion of a SRAM device constructed *according to various aspects of the present disclosure in various embodiments.*” *Id.*, 2:41-43; EX1002, ¶¶162-163.

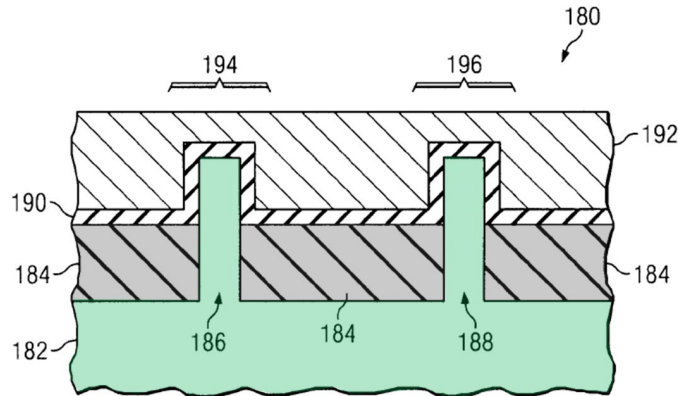


*Fig. 7*

EX1008, FIG. 7

As shown in Figure 7 above, semiconductor structure 180 includes substrate 182, e.g., a silicon substrate, and fins 186 and 188. *Id.*, 8:17-27. *Id.*, 8:21-24. The FIG. 7 structure may be formed by “forming trenches in...substrate 182.” EX1008, 8:15-31. Thus, a POSITA would have understood fins 186 and 188 are formed by etching/removing the substrate material in certain regions, where regions between the trenches result in fins 186 and 188. EX1014, 15:30-57. Additional features are formed on the fins of semiconductor structure 180 to form FinFETs, as shown in Figure 7. EX1008, 8:56-9:10; EX1002, ¶¶164-166.

According to Liaw, “SRAM cell 200 [in Figure 9] is similar to the SRAM cell 100 of FIG. 2 except that the SRAM cell 200 includes four pull-down devices and four pass-gate devices” *Id.*, 10:8-11. Thus, a POSITA would have understood the process/features disclosed in connection with Figure 7 are attributable to the teachings associated with SRAM cell 200 of Figure 9, and thus Liaw discloses

SRAM cell 200 may be, and is, constructed using the processes/features associated with Figure 7, including that the fins of SRAM cell 200 are formed by etching/removing the substrate material. EX1002, ¶167.

Further, a POSITA would have found it obvious to use the Figure 7 process to produce Figure 9's SRAM cell 200, including forming the fins by etching/removing the substrate material, given that Liaw discloses applying the Figure 7 process to Figure 2's SRAM cell 110 and that SRAM cell 200 is similar to the SRAM cell 100. *Supra*; EX1002, ¶¶158, 164. A POSITA would have had the skill, rationale, and knowledge in implementing, and reasonable expectation of success in achieving, the above-discussed modification. This is particularly true because Liaw itself discloses "SRAM cell 200 [in Figure 9] is similar to the SRAM cell 100 of FIG. 2." EX1008, 10:8-11; EX1002, ¶164.

## **2. Combination of Liaw and Basker**

Liaw does not expressly disclose "even [or second] fins of the FinFETs...being [or are] different from the odd [or first] fins of the FinFETs in at least one of width and material" (limitations [1.c]/[9.c]/[15.c]) under PO's litigation allegations. Nevertheless, a POSITA would have found it obvious to implement such features in Liaw (§VI.F.1) in view of Basker. EX1002, ¶¶178-192.

Like Liaw, Basker discloses FinFETs on a bulk silicon substrate (EX1006, [0020], [0025]) and an nFinFET "formed on a fin made from a substrate material"

(*id.*, [0020]), i.e., silicon fin (*id.*, [0038]), and the fins are formed by using an etch process (*id.*, [0025]-[0029]). §VI.A.1; §VI.F.1. Moreover, both Liaw and Basker disclose using high-k metal gate for the transistors' gate. EX1006, [0020], [0034]; EX1008, 3:35-38, 8:67-9:3. Thus, a POSITA would have been motivated to consider Basker's teachings when implementing semiconductor devices like those of Liaw. Basker additionally discloses improving the pFinFET performance by adding Ge to silicon fins to **form SiGe fins**. EX1006, [0020]-[0021]. A POSITA would have been motivated to form SiGe fins for pFinFETs in a structure as disclosed/suggested by Liaw in view of Basker's teaching. EX1002, ¶¶181-183.

**First**, a POSITA would have understood there has been a general trend at the relevant time to include Ge/SiGe into the transistor's channel, which traditionally has been made of silicon. EX1002, ¶184; EX1025, 1. In fact, it was known that "SiGe channel [FinFET] is an attractive replacement" of Si channel pFinFETs. EX1026, 1; EX1030, 2; EX1031, 1; §II.B. Indeed, a POSITA would have understood SiGe fins improve hole mobility for pFinFETs and thus improve current drive of the transistors and speed of transistors' operation. EX1002, ¶184; EX1016, 1-2, 4; EX1017, 1; EX1018, 1; §II.B. And the use of SiGe fins also improves NBTI reliability for pFinFETs (where NBTI reliability was a major issue for the semiconductor industry), and thus improves the performance of SRAM devices as

disclose in Liaw. EX1002, ¶184; EX1016, 1, 2, 4; EX1017, 1; EX1018, 1; EX1025, 1; EX1026, 1.

**Second**, as Basker itself explained, it is “advantageous” to impart strain to the fin, and the strain caused by adding Ge to the silicon fins “improves pFET performance.” EX1006, [0021], [0038]; EX1002, ¶185.

**Third**, Basker explains using a silicon fin for an nFinFET and using a SiGe fin for a pFinFET allows the use of “the same gate dielectric...and the same gate conductor...” (EX1006, [0038]), which would have simplified the fabrication processes and reduced cost for making ICs/SRAM. EX1002, ¶186; EX1023, [0008], [0016], [0027]; §II.B.

A POSITA would have had the skill, rationale, and knowledge in implementing, and reasonable expectation of success in achieving the Liaw-Basker combination. EX1002, ¶187. Basker itself discloses adding Ge to the silicon fin results in “**an ideal combination**” of beneficial features. EX1006, [0021]. Basker explains the disclosed features may be applied to many useful IC components which, as a POSITA would have understood, include SRAM (e.g., those disclosed in Liaw). *Id.*, [0021]; EX1002, ¶187. The modification of Liaw in view of Basker’s teachings would have been motivated by teaching/suggestion/motivation in the prior art (e.g., discussed above) and involved applications of known technologies (e.g., known use of SiGe for pFinFETs) according to known methods (e.g., known method of forming

SiGe) to yield the predictable result of improved pFinFETs and other benefits discussed above in the Liaw-Basker combination. EX1002, ¶188; *KSR*, 550 U.S. at 416.

Additionally, as discussed for claims 3/11/17 in Ground 1 (§VI.A.5), Basker discloses forming SiGe fins by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22. EX1006, [0005], [0020]-[0021], [0032], [0041], claim 1. Since the resulting SiGe fins incorporate the epitaxially deposited material, the resulting SiGe fins “comprise an epitaxy material.” Also, a POSITA would have understood that Basker’s SiGe fin formation results in epitaxy material and thus the resulting SiGe fins “comprise an epitaxy material.” EX1013, 2; EX1038, 3-4. Additionally, a POSITA would have known that SiGe fins can also be formed using e.g., CVD and MBE, and would have found it oblivious to use any of them. EX1039, 4:23-5:9. Thus, Basker discloses and/or suggests SiGe “fins of the FinFETs comprise an epitaxy material.” EX1002, ¶189.

A POSITA would have been motivated to form SiGe fins for pFinFETs “compris[ing] an epitaxy material” in the Liaw-Basker combination. EX1002, ¶190. Basker explains “[i]t is advantageous to epitaxially grow the donor layer...[comprising Ge]” using the disclosed process as it “ensure[s] good contact between the donor layer...and the sidewalls of fin...,” allowing uniform and high-quality epitaxial growth. EX1006, [0031]; EX1002, ¶190.

A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Liaw-Basker combination. EX1002, ¶191. Liaw and Basker share several similar features/processes, e.g., both form FinFETs on a silicon substrate, the nFinFETs are formed from the substrate material, and both use high-k metal gate for the transistors' gate. Combining Liaw with Basker would have been motivated by teaching/suggestion/motivation in the prior art (e.g., discussed above) and involved applications of known technologies (e.g., known use of SiGe for pFinFETs) according to known methods (e.g., known method of forming SiGe) to yield the predictable result of improved pFinFETs and other benefits discussed above in the Liaw-Basker combination. EX1002, ¶¶191-192; *KSR*, 550 U.S. at 416.

### **3. Claims 1, 9, and 15**

#### **(i) [1.pre]/[9.pre]/[15.pre]**

Liaw discloses and/or suggests these preambles. EX1002, ¶¶158-168. Liaw discloses a semiconductor device, e.g., SRAM, using FinFETs. EX1008, Abstract, 1:49-2:24, 2:61-64, 2:64-3:21. As discussed in §VI.F.1, Liaw discloses a “semiconductor structure” (e.g., as shown in Figure 9 as modified having the fin structure shown in Figure 7) “for forming FinFETs” ([1.pre] and [9.pre]) and “forming FinFET” ([15.pre]). EX1002, ¶168.

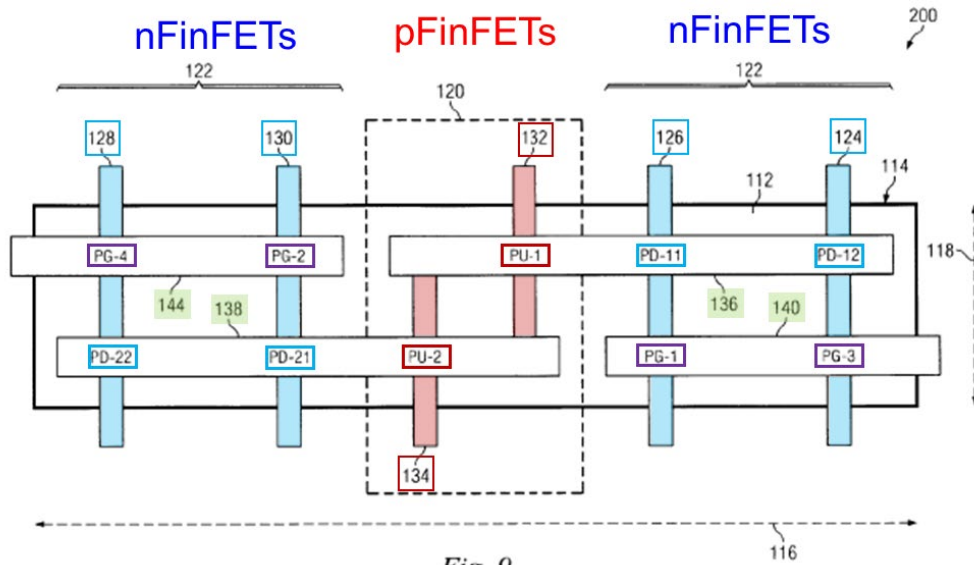


*Fig. 9*

EX1008, FIG. 9 (annotated)

**(ii) [1.a]/[9.a]/[15.a]**

Liaw discloses and/or suggests these limitations. EX1002, ¶¶169-171. Liaw discloses substrate 182 is a “semiconductor substrate,” e.g., a silicon substrate. EX1008, 8:15-19.

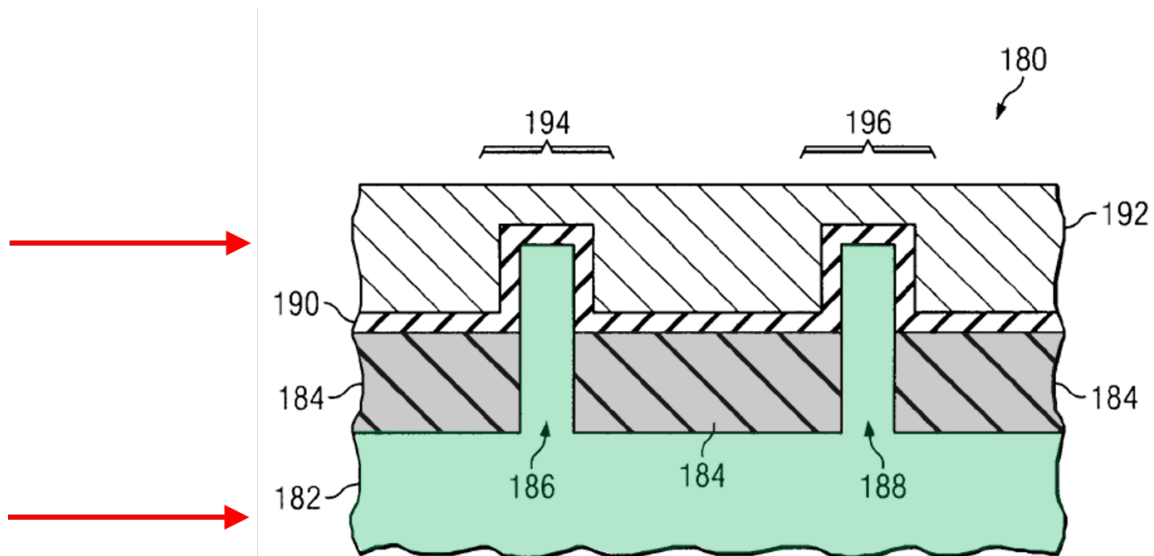


Fig. 7

EX1008, FIG. 7 (annotated)

As discussed above (§VI.F.1), structure 180 is formed on semiconductor substrate 182 by removing/etching the substrate material. Thus, Liaw discloses “a top portion of the semiconductor substrate,” e.g., as shown between the red lines, “comprises a semiconductor material.” Additionally, Liaw discloses “substrate 182 includes *silicon*,” and “[a]lternatively, the substrate includes *germanium, silicon germanium or other proper semiconductor materials*.” EX1008, 8:17-19. A POSITA would have understood that Liaw discloses that semiconductor substrate 182 may be entirely made of silicon, i.e., a bulk silicon substrate, without including “other...semiconductor materials,” confirming the top portion of the substrate comprises a semiconductor material, i.e., silicon. EX1002, ¶¶170-171.

(iii) [1.b]/[9.b]/[15.b]

Liaw discloses and/or suggests these limitations under PO's litigation allegations. EX1002, ¶¶172-177. As discussed for the preambles (§VI.F.3(i)) and as shown in Figure 7 (§VI.F.1), fins 186 and 188 are formed of the semiconductor substrate material and protrude from substrate 182. Liaw discloses substrate 180 includes regions 194/196 for FinFETs. EX1008, 9:4-10. Thus, Liaw discloses “fins of the FinFETs on the semiconductor substrate...being formed of the semiconductor material” (limitations [1.b]/[9.b]/[15.b]).

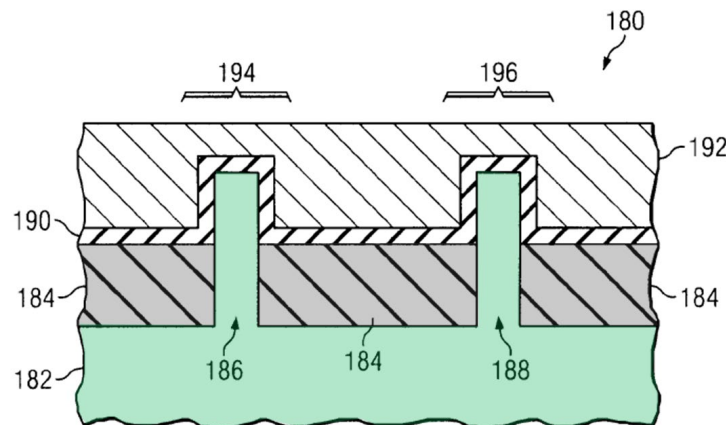


*Fig. 7*

EX1008, FIG. 7 (annotated)

Liaw discloses the fins are “defined from the semiconductor substrate” (limitation [1.b]). As discussed for the preambles (§VI.F.3(i); §VI.F.1), Liaw’s fins are formed by etching/removing the semiconductor substrate material. Thus, the fins are “defined” from semiconductor substrate 182. EX1002, ¶173.

As discussed for the preambles (§VI.F.3(i); VI.F.1), SRAM cell 200 (FIG. 9) may be constructed using the Figure 7 process. EX1002, ¶174. Liaw's Figure 9 shows six fins, where each of fins 124, 126, 128, 130 (blue) is associated with two nFinFETs (PG and PD FinFETs) and each of 132 and 134 (red) is associated with one pFinFET (PU FinFET). EX1008, 10:60-11:18.

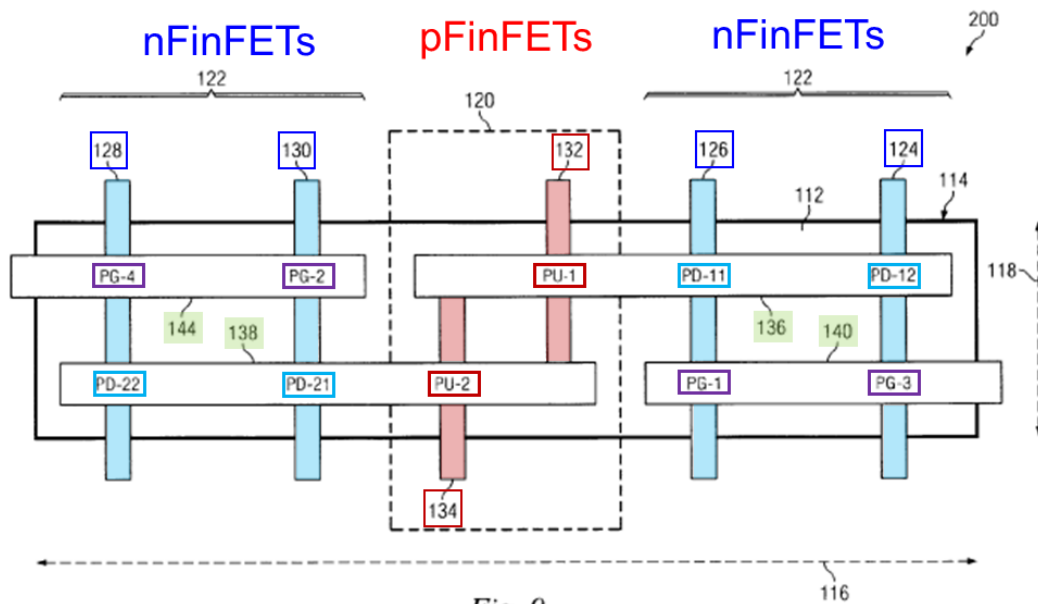
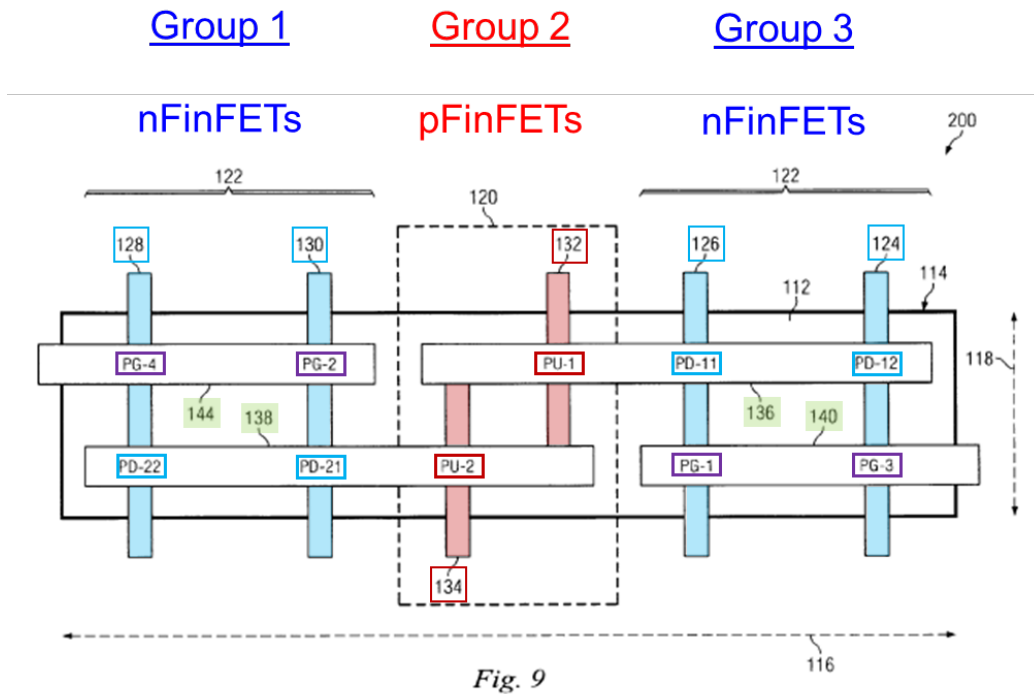


Fig. 9

EX1008, FIG. 9 (annotated)

In light of such disclosures, Liaw discloses and/or suggests limitations [1.b]/[9.b]/[15.b] under PO's litigation allegations. EX1012, 45-46; §III.C. Liaw's SRAM cell 200 (FIG. 9) discloses three groups of fins, e.g., Groups 1-3, where Groups 1 and 3 each corresponds to "a plurality of **odd** [or **first**] fins of the FinFETs" and Group 2 corresponds to "a plurality of **even** [or **second**] fins of the

FinFETs” of claims 1/9/15 under PO’s litigation allegations. (See limitations [1.c]/[9.c]/[15.c] discussed in the next section). EX1002, ¶¶175-176.



EX1008, FIG. 9 (annotated)

Groups 1-3 fins are on the semiconductor substrate (“on the semiconductor substrate” as claimed). EX1008, 10:44-45. As discussed above (§§VI.F.1, VI.F.3(i)), the fins of SRAM cell 200 (FIG. 9) may be formed by etching/removing the substrate material. Thus, Groups 1 and 3 fins are “defined from the semiconductor substrate” (limitation [1.b]) and “formed of the semiconductor material” comprised in the top portion of the semiconductor substrate (limitations [1.b], [9.b] and [15.b]). EX1002, ¶177; §VI.F.3(ii). Given that the fins are formed of the substrate by etching/removing the substrate material, Groups 1 and 3 fins “and

the semiconductor substrate are in direct contact with each other” (limitations [1.b]/[9.b]/[15.b]). EX1002, ¶177.

**(iv) [1.c]/[9.c]/[15.c]**

Liaw in view of Basker discloses and/or suggests these limitations. EX1002, ¶¶178-192. As discussed for limitations [1.b]/[9.b]/[15.b] (§VI.F.3(iii)), Liaw's Groups 1-3 fins are on the semiconductor substrate, including Group 2 fins (corresponding to "a plurality of even [or second] fins of the FinFETs" of claims 1/9/15 under PO's litigation allegations), are "on the semiconductor substrate," as claimed. EX1008, 10:44-45.

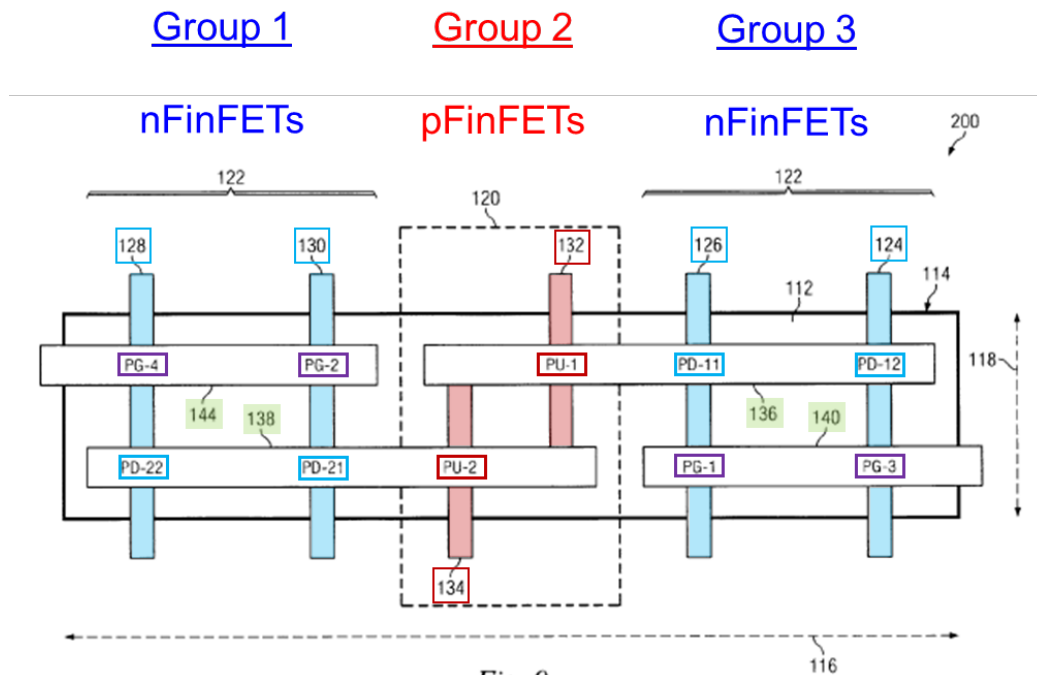


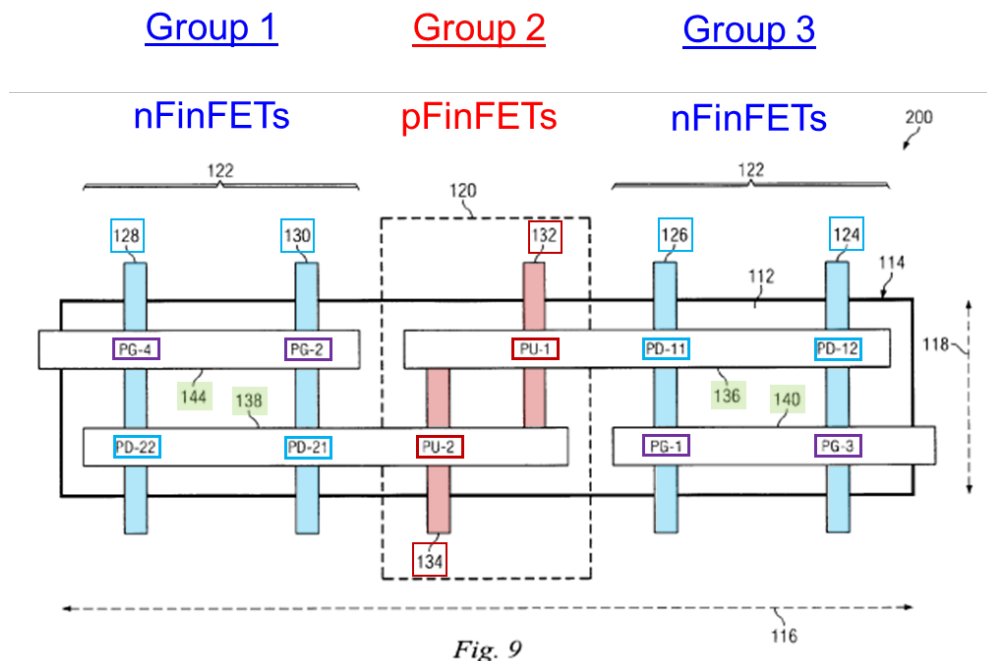
*Fig. 9*

As shown above, Group 2 fins reside between Groups 1 and 3 fins (“between the odd fins of the FinFETs” (limitations [1.c]/[9.c]) under PO’s litigation

allegations). Likewise, Liaw discloses “each of the second fins of the FinFETs is located between two first fins of the FinFETs,” (limitation [15.c]) under PO’s litigation allegation, given that each of the fins in Group 2 is located between two fins, each of Groups 1 and 3. EX1002, ¶179.

As discussed in §VI.F.2, while Liaw does not expressly disclose “even [or second] fins of the FinFETs...being [or are] different from the odd [or first] fins of the FinFETs in at least one of width and material” under PO’s litigation allegations, a POSITA would have found it obvious to implement such features in the Liaw-Basker combination. EX1002, ¶180; §VI.F.2.

As discussed in §VI.F.2, a POSITA would have been motivated to form SiGe fins for pFinFETs in the Liaw-Basker combination. §VI.F.2; EX1002, ¶¶180-191. Given that the Liaw-Basker combination discloses and/or suggests using **Silicon** fins for nFinFETs (EX1008, 8:15-31, 9:4-10) and **SiGe** fins for pFinFETs, the Liaw-Basker combination discloses “**even** [or **second**] fins of the FinFETs...being [or are] different from the **odd** [or **first**] fins of the FinFETs in at least one of width and **material**” (claims 1/9/15) under PO’s litigation allegations. EX1002, ¶192; *supra* §III.C.



EX1008, FIG. 9

#### 4. Claims 3, 11, and 17

The Liaw-Basker combination discloses and/or suggests these limitations.  
EX1002, ¶¶193-199.

As discussed for claim [1.c]/[9.c]/[15.c] for Ground 6, it would have been obvious to use SiGe fins for pFinFETs. Further, as discussed for claims 3/11/17 in Ground 1, Basker discloses forming SiGe fins by epitaxially depositing a material (Ge/SiGe) and incorporating it into fin 22. *Id.*, [0005], [0020]-[0021], [0031]-[0032], [0041], claim 1. As discussed in §VI.F.2, a POSITA would have been motivated to form SiGe fins for pFinFETs of Liaw “compris[ing] an epitaxy material” in view Basker. §VI.F.2. Accordingly, a POSITA would have found it obvious to form pFinFETs (as disclosed in Liaw, e.g., PU-1 and PU-2 of Group 2 fins in Figure

9) having SiGe fins that “comprise an epitaxy material” (as taught in Basker).  
EX1002, ¶¶199; *see also id.*, 193-198.

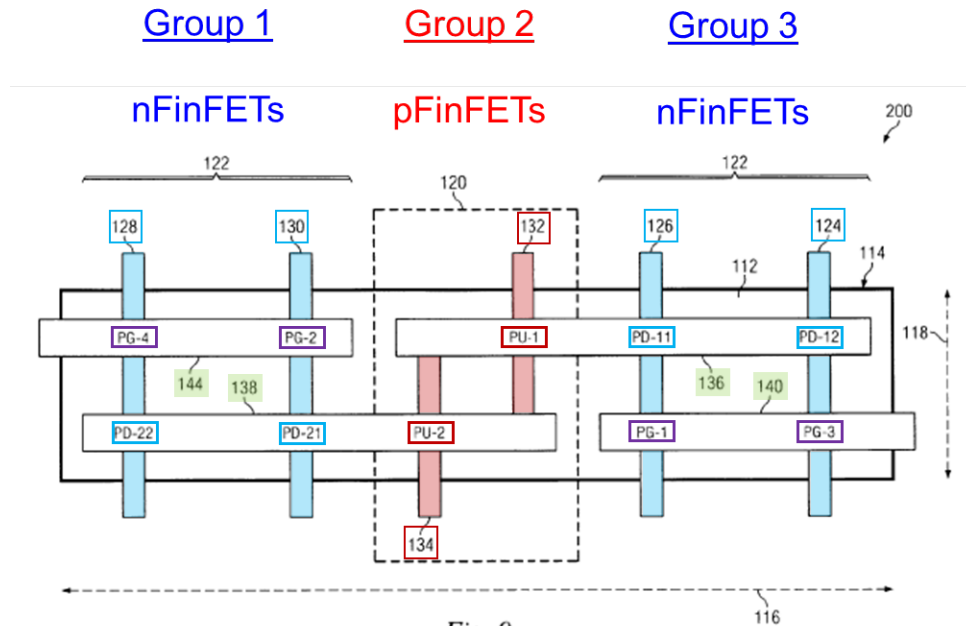


Fig. 9

## 5. Claims 4, 12, and 18

The Liaw-Basker combination discloses these limitations. As discussed for limitations [1.b]/[9.b]/[15.b] in Ground 6, Liaw discloses “the odd [or first] fins of the FinFETs **comprise Si**” because the Groups 1 and 3 fins are formed from the silicon substrate. As discussed for claims 3, 11, and 17, Liaw in view of Basker discloses forming **SiGe fins** for pFinFETs, i.e., the Group 2 fins or the “even [or second] fins of the FinFETs” comprise SiGe. §VI.F.4; EX1002, ¶200. Thus, such features would have been likewise included in the Liaw-Basker combination discussed above. *Id.*

**6. Claim 5, 13, and 19**

The Liaw-Basker combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18. EX1002, ¶201; *supra* §VI.F.5.

**7. Claim 6, 14, and 20**

The Liaw-Basker combination discloses and/or suggests these limitations for the same reasons discussed for claims 4, 12, and 18. EX1002, ¶202; *supra* §VI.F.5.

**8. Claim 7**

The Liaw-Basker combination discloses and/or suggests this limitation. EX1002, ¶¶203-204. As discussed for limitations [1.b]/[9.b]/[15.b], Groups 1 and 3 fins (“the odd fins of the FinFETs” under PO’s litigation allegations) are defined from and formed of *silicon* substrate 182. Consistent with Figure 7 below, Groups 1 and 3 fins are connected to silicon substrate 1. EX1008, 8:15-31.

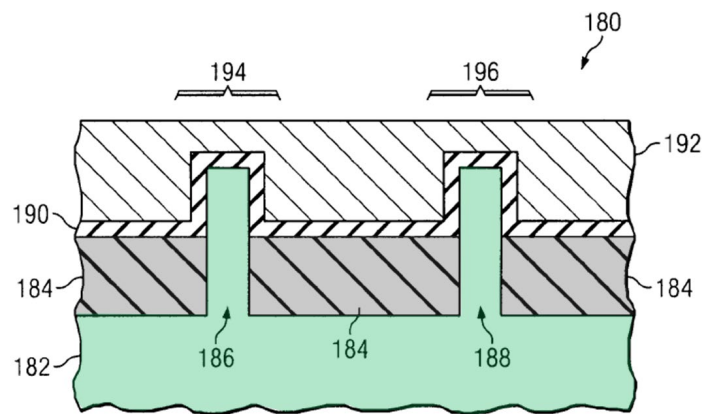


*Fig. 7*

A POSITA would have understood that, given Groups 1 and 3 fins and the substrate are connected and both are the same semiconductor material, i.e., silicon,

these fins and the substrate are electrically connected. EX1002, ¶204. Accordingly, the Liaw-Basker combination discussed above for claim 1 (§VI.F.3) likewise discloses the features of claim 7. *Id.*

## 9. Claim 8

The Liaw-Basker combination discloses and/or suggests this limitation. As discussed for limitations [1.a]/[9.a]/[15.a], substrate 182 may be a bulk silicon substrate (EX1008, 8:17-19, 9:15-25) and thus the entire substrate is formed of “a single layer structure” of semiconductor material, i.e., silicon. EX1002, ¶205. Such features would have been included in the Liaw-Basker combination discussed above for claim 1. *Id.*; *supra* §VI.F.3.

## G. Ground 7: Claims 2, 10, and 16 Are Obvious Over Liaw, Basker, and Yu

### 1. Combination of Liaw, Basker, and Yu

The Liaw-Basker combination does not expressly disclose “the **even** fins...are further different from the **odd** fins...**in height**” or “the **second** fins...are further different from the **first** fins...**in height**.” Nevertheless, a POSITA would have found it obvious to implement such a structure in view of Yu’s teachings. EX1002, ¶¶206-215.

Like Liaw, Yu discloses FinFETs for use in ICs (EX1010, [0001]-[0002], [0019] (“semiconductor chip”)) and forming fins of the FinFETs by etching a bulk silicon substrate (*id.*, [0028], [0020]-[0024]). §VI.B.1. Thus, a POSITA would have

been motivated to consider Yu's teachings when implementing a semiconductor structure like those disclosed in the Liaw-Basker combination. EX1002, ¶209.

As discussed in §VI.B.1, Yu discloses forming "customized fin heights...so that the FinFETs may have customized performance." EX1010, [0010]; §VI.B.1; EX1010, [0023]-[0027], [0029]. In view of Yu's teaching, including customizing "semiconductor fins with different heights on a same semiconductor chip" (EX1010, [0010], [0019]), a POSITA would have been motivated to customize the fin heights of the FinFETs in an IC chip, e.g., those in the SRAM cells disclosed/suggested by the Liaw-Basker combination. EX1002, ¶¶210-212; §§VI.F.1-3. As discussed for above (§VI.B.2), that performances of the FinFETs, e.g., static noise margin depends on the dimensions of the FinFETs used to form the cell. §VI.B.1. Also discussed therein, the static noise margin depends on the pull up ratio (PR) of the SRAM cell, where PR is a parameter for optimizing SRAM performance. For example, it has been reported that PR should be in the range of 3 to 4 for SRAM cells to be functional. §VI.B.2; EX1033, 1-3; EX1002, ¶212. Accordingly, a POSITA would have been motivated to customize the fin heights to, e.g., increase  $W_{pFET}$  and/or to reduce  $W_{nFET}$  (and/or to reduce  $L_{pFET}$  and/or to increase  $L_{nFET}$ ) to achieve the desired PR range in the Liaw-Basker combination discussed above. EX1002, ¶212.

As discussed above, given that the channel width  $W$  is a function of the fin height, a POSITA, guided by Yu's teachings/suggestions and their state of art

knowledge, would have found it obvious to customize fin heights to, for example, increase  $W_{\text{pFET}}$  and/or to reduce  $W_{\text{nFET}}$  in a SRAM cell in the above-discussed Liaw-Basker combination to achieve the desired PR range such that the height of the pFinFET's fins ("even" or "second" fins) would have been different from the height of the nFinFET fins ("odd" or "first" fins) in the Liaw-Basker-Yu combination. EX1002, ¶213.

A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the Liaw-Basker-Yu combination, particularly given that Liaw and Yu shared similar fin fabrication process steps. EX1002, ¶214. Combining Liaw, Basker, and Yu would have been motivated by teaching/suggestion/motivation in the prior art (e.g., discussed above) and involved applications of known technologies (e.g., known process to etch a substrate to form fins of FinFETs) according to known methods (e.g., known method of forming trenches of different depths on a substrate to create height differences between fins) to yield the predictable result of a functional SRAM cell having a proper pull-up ratio (PR) and thus static noise margin. *KSR*, 550 U.S. at 416.

## **2. Claims 2, 10, and 16**

The Liaw-Basker-Yu combination discloses and/or suggests these limitations. EX1002, ¶¶206-215. As discussed for limitations [1.b]/[9.b]/[15.b] and [1.c]/[9.c]/[15.c] in Ground 6, the Liaw-Basker combination discloses, as shown in

Figure 9 below, three groups of fins. *Supra* §§VI.F.3.(iii)-(iv). Additionally, as discussed above in §VI.G.1, a POSITA would have been motivated to customize the fin heights to, e.g., increase  $W_{\text{pFET}}$  and/or to reduce  $W_{\text{nFET}}$  (and/or to reduce  $L_{\text{pFET}}$  and/or to increase  $L_{\text{nFET}}$ ) to achieve the desired PR range in the Liaw-Basker combination such that the pFinFET fins (“even” or “second” fins) “are...different from” nFinFET fins (“odd” or “first” fins) “in height.” EX1002, ¶¶206-214.

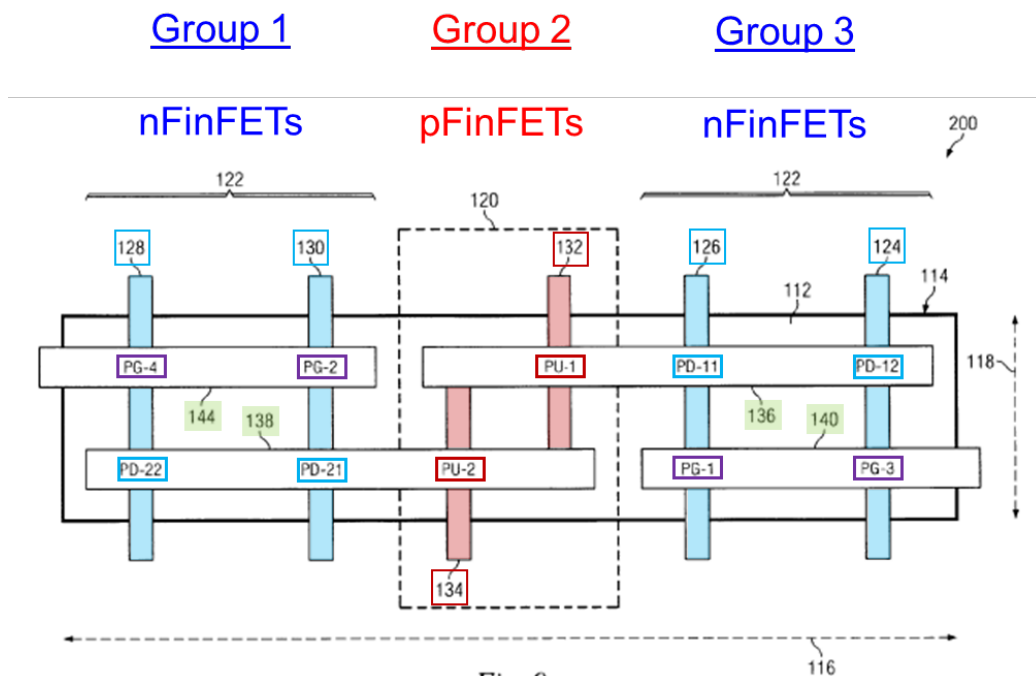


Fig. 9

EX1008, FIG. 9

As discussed for Ground 2, the height difference of the nFinFET and pFinFETs in a SRAM cell is a “result-effective variable.” EX1033, 1; §VI.B; §II.C. Thus, claims 2, 10, and 16 would have been obvious. *DuPont*, 904 F.3d at 1010; *Applied Materials*, 692 F.3d at 1297. This is especially true given that the ’292

patent provides no evidence that fins having “height” difference produces any new/unexpected result. EX1002, ¶215.

## **VII. TRIAL SHOULD BE INSTITUTED**

The Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” sets out a temporary procedure under which Co-Petitioners will have an opportunity to respond to any discretionary denial arguments Patent Owner may raise through a bifurcated briefing process. Co-Petitioners believe discretionary denial is unwarranted and, at the appropriate time, plan to rebut any claims Patent Owner may advance to the contrary.

Meanwhile, Co-Petitioners identify below several non-limiting considerations that weigh against discretionary denial:

- The ITC instituted investigation on March 21, 2025, just 23 days before this Petition was filed. The ITC has not even set a schedule, let alone issued any substantive orders. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 11 (Mar. 20, 2020) (expeditious filing weighs against denial); *SharkNinja v. iRobot Corp.*, IPR2021-00545, Paper 11, at 8 (Sept. 8, 2021) (petitioner’s diligence and remaining work at the ITC weighs against denial).
- No other forum has adjudicated these claims.

- The Challenged Claims include claims 2, 10, and 16 not asserted in the ITC.
- Co-Petitioner TSMC has a 94% institution rate and a 100% success in FWDs. Consistent with that track record, the merits here are strong, presenting Grounds addressing all claims under two interpretations.  
§III.C.
- Expert testimony is corroborated by documentary evidence.
- Each of the Petitioners (not to mention the other real parties-in-interest) is responsible for substantial and sustained investments in the U.S.<sup>14</sup>

The ITC lacks authority to invalidate the claims, but the companion district court, which will be stayed, triggered the one-year bar date, thereby limiting Co-

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<sup>14</sup> “TSMC Intends to Expand Its Investment in the United States to US **\$165 Billion** to Power the Future of AI,” <https://pr.tsmc.com/english/news/3210> (Mar. 4, 2025); “Apple Will Spend More Than **\$500 billion** in the U.S. Over the Next Four Years,” <https://www.apple.com/newsroom/2025/02/apple-will-spend-more-than-500-billion-usd-in-the-us-over-the-next-four-years/> (Feb. 24, 2025); “Trump and TSMC Announce **\$100 Billion** Plan to Build Five New US Factories,” <https://www.reuters.com/technology/tsmc-ceo-meet-with-trump-tout-investment-plans-2025-03-03/> (Mar. 4, 2025).

Petitioners' options to invalidate the Challenged Claims. *See 3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12, at 33-34 (May 26, 2020) (instituting despite parallel ITC case to preserve the "efficiency and integrity of the system"); *Emerson Electric Co., v. Sipco, LLC*, IPR2019-00547, Paper 15, at 9 (Aug. 30, 2019) (IPR proceedings not duplicative of parallel ITC case). The ITC may not even reach the issue of invalidity. (*See, e.g., Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).)

## VIII. MANDATORY NOTICES

**Real Parties-in-Interest:** Petitioners identify the following as the real parties-in-interest: TSMC and Apple, Inc., Broadcom Inc., and Qualcomm Inc.

**Related Matters:** The '292 patent is asserted in *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 1:25-cv-00215 (W.D.Tex.), *Longitude Licensing Ltd. et al. v. Lenovo Group Limited et al.*, Case No. 2:25-cv-00171 (E.D.Tex.), and *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 337-3809 (ITC).

### **Counsel and Service Information:**

Petitioners identify the following lead and backup counsel and Petitioners each consents and requests that all service and correspondence to them respectively and/or collectively in this matter be electronically provided at the below-provided e-mail addresses.

**Lead counsel:** Naveen Modi (Reg. No. 46,224) (counsel for TSMC)

### **Backup counsel:**

#### **Counsel for TSMC:**

- (1) Joseph E. Palys (Reg. No. 46,508);
- (2) Howard Herr (*pro hac vice* to be requested);
- (3) Joseph Rumpler (Reg. No. 71,544);
- (4) Jeremy S. Rashid (Reg. No. 76,229); and
- (5) Jacob Rothenberg (Reg. No. 77,891).

**Service information:** Paul Hastings LLP, 2050 M St., Washington, D.C., 20036, Tel.: 202.398.1700, Fax: 202.398.1705, email: **PH-TSMC-Marlin-IPR@paulhastings.com**.

Counsel for Apple, Inc.:

(1) W. Karl Renner (Reg. No. 41,265)

(2) Jeremy J. Monaldo (Reg. No. 58,680)

(3) Alexander Berg, (Reg. No. 79,866)

**Service information:** Apple consents to electronic service by email at [IPR50095-0270IP1@fr.com](mailto:IPR50095-0270IP1@fr.com) (referencing No. 50095-0270IP1 and cc'ing [PTABInbound@fr.com](mailto:PTABInbound@fr.com), [axf-ptab@fr.com](mailto:axf-ptab@fr.com), [jjm@fr.com](mailto:jjm@fr.com), and [berg@fr.com](mailto:berg@fr.com)).

## **IX. PAYMENT OF FEES**

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

## **X. GROUNDS FOR STANDING**

Petitioners certify that the '292 patent is available for review, and Petitioners are not barred/estopped from requesting review on the grounds identified herein.

## **XI. CONCLUSION**

For the reasons given above, Petitioners request IPR be instituted for the challenged claims.

Petition for *Inter Partes* Review  
Patent No. 9,184,292

Respectfully submitted,

Dated: April 17, 2025

By: /Naveen Modi/  
Naveen Modi (Reg. No. 46,224)  
Counsel for Petitioner TSMC

## **XII. APPENDIX A (CLAIM LISTING)**

### Claim 1

[1.pre] A semiconductor structure for forming FinFETs, comprising

[1.a] a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

[1.b] a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material; and

[1.c] a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

### Claim 2

The semiconductor structure of claim 1, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

Claim 3

The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise an epitaxy material.

Claim 4

The semiconductor structure of claim 3, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

Claim 5

The semiconductor structure of claim 1, wherein the odd fins of the FinFETs comprise Si.

Claim 6

The semiconductor structure of claim 1, wherein the even fins of the FinFETs comprise SiC or SiGe.

Claim 7

The semiconductor structure of claim 1, wherein the odd fins of the FinFETs are electrically connected to the semiconductor substrate.

Claim 8

The semiconductor structure of claim 1, wherein the semiconductor substrate is a single layer structure.

Claim 9

[9.pre] A semiconductor structure for forming FinFETs, comprising

[9.a] a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

[9.b] a plurality of odd fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of odd fins and the semiconductor substrate are in direct contact with each other; and

[9.c] a plurality of even fins of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being different from the odd fins of the FinFETs in at least one of width and material, wherein the plurality of even fins are in direct contact with the semiconductor material.

Claim 10

The semiconductor structure of claim 9, wherein the even fins of the FinFETs are further different from the odd fins of the FinFETs in height.

Claim 11

The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise an epitaxy material.

Claim 12

The semiconductor structure of claim 11, wherein the odd fins of the FinFETs comprise Si and the even fins of the FinFETs comprise SiC or SiGe.

Claim 13

The semiconductor structure of claim 9, wherein the odd fins of the FinFETs comprise Si.

Claim 14

The semiconductor structure of claim 9, wherein the even fins of the FinFETs comprise SiC or SiGe.

Claim 15

[15.pre] A semiconductor structure for forming FinFET, comprising

[15.a] a semiconductor substrate, wherein a top portion of the semiconductor substrate comprises a semiconductor material;

[15.b] a plurality of first fins of the FinFETs on the semiconductor substrate and being formed of the semiconductor material, wherein the plurality of first fins and the semiconductor substrate are in direct contact with each other; and

[15.c] a plurality of second fins of the FinFETs on the semiconductor substrate, each of the second fins of the FinFETs is located between two first fins of the FinFETs, and the second fins of the FinFETs are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.

Claim 16

The semiconductor structure of claim 15, wherein the second fins of the FinFETs are further different from the first fins of the FinFETs in height.

Claim 17

The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise an epitaxy material.

Claim 18

The semiconductor structure of claim 17, wherein the first fins of the FinFETs comprise Si and the second fins of the FinFETs comprise SiC or SiGe.

Claim 19

The semiconductor structure of claim 15, wherein the first fins of the FinFETs comprise Si.

Claim 20

The semiconductor structure of claim 15, wherein the second fins of the FinFETs comprise SiC or SiGe.

**CERTIFICATE OF COMPLIANCE**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,184,292 contains, as measured by the word-processing system used to prepare this paper, 13,998 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Date: April 17, 2025

By: /Naveen Modi/  
Naveen Modi (Reg. No. 46,224)  
Counsel for Petitioner TSMC

Paul Hastings LLP  
2050 M Street NW  
Washington, DC 20036  
202-551-1700

**CERTIFICATE OF SERVICE**

I hereby certify that on April 17, 2025, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,184,292 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on The USPTO's Patent Center website:

**23900 - J.C. PATENTS**  
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A courtesy copy was also sent via overnight mail to Patent Owner's litigation counsel listed below:

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