

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
and APPLE INC.
Petitioners,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-00864
U.S. Patent No. 9,184,292 B2

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph McAlexander
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	Webster's Dictionary, "contact"

I. Summary

The Petition fails because it does not identify any teaching of the claimed even/second fins “in **direct contact** with the [substrate’s] semiconductor material” limitation required in every challenged claim. Indeed, Grounds 3A-7 do not even allege that any of the asserted references disclose or make obvious this “direct contact” limitation; instead, these Grounds simply ignore the “direct contact” requirement. And although Grounds 1-2 at least address the “direct contact” requirement, they not only fail to identify any such “direct contact,” they effectively concede and establish its absence from the asserted references.

Accordingly, the Petition should be denied because, among other reasons, none of the grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teach or make obvious each limitation in any challenged claim.

The Direct Contact Limitation: The challenged ’292 Patent describes and claims an alternate approach to forming fins for FinFET transistors, wherein different sets of fins can have different attributes, including, for example, the way they are fabricated, the materials from which they are made, and their dimensions. The ’292 Patent alternately refers to these different sets of fins as “odd” or “first” fins on the one hand, and “even” or “second” fins on the other. The patent’s

Figure 6 illustrates an embodiment of odd/first fins 10a (blue), even/second fins 20 (green), and a semiconductor substrate 10 (also blue).

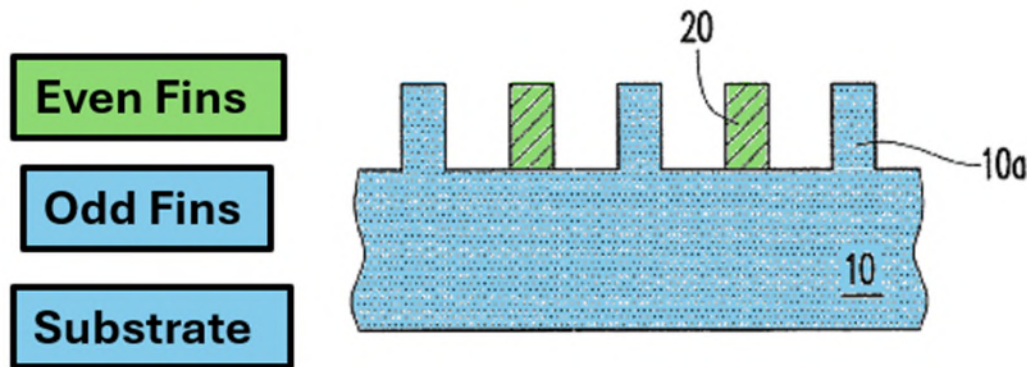


FIG. 6

(EX1001 at Fig 6) (colors and annotations added).¹

The '292 Patent describes an illustrative method for fabricating these different sets of fins so that they have different attributes. For example, to make one set of fins (the odd/even fins), the patent describes starting with a substrate of semiconductor material 10, and then etching away portions of that substrate semiconductor material, with the remaining material forming the fins. In this manner, the fins are formed from and are unitary with the substrate's semiconductor material:

¹ Unless otherwise indicated, all colors and annotations to the '292 Patent's figures are added.

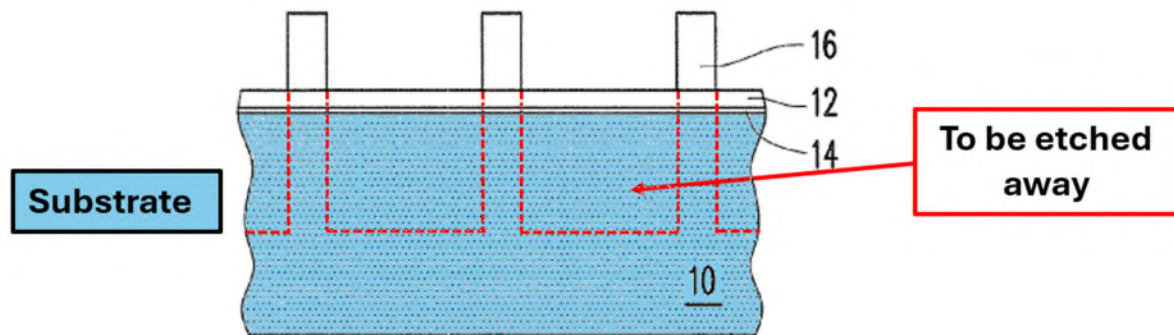


FIG. 1

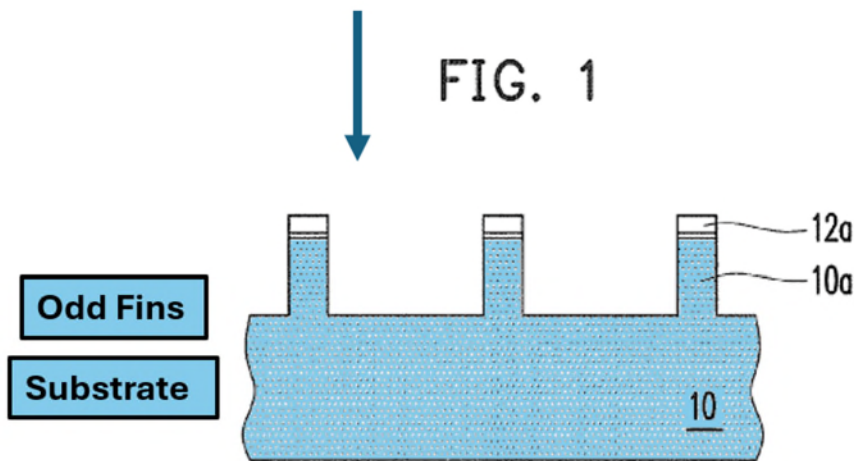


FIG. 2

(EX1001 at 2:53-64, Figs. 1-2).

The '292 Patent describes that the even/second set of fins may be made in a different way. For example, instead of forming the even/second fins from the substrate's material, they may be grown or deposited on top of the substrate material:

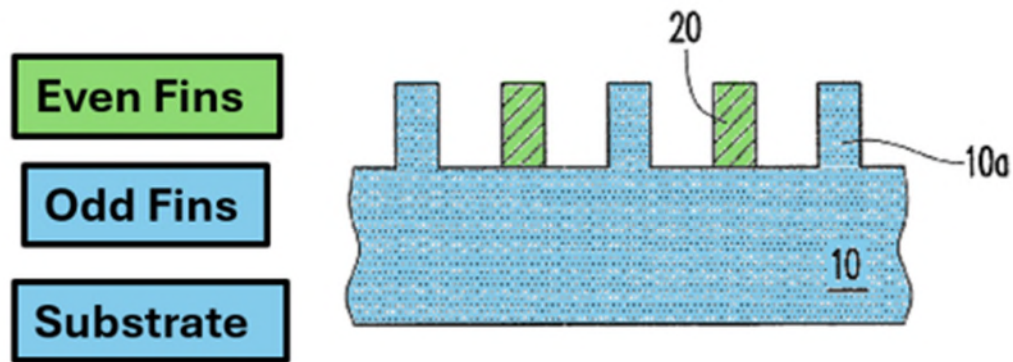


FIG. 6

(EX1001 at 3:50-52, Fig. 6).

As a result, the even/second fins may differ from the odd/first fins in material composition, dimensions and, as illustrated below, may be in direct contact with the semiconductor substrate material (rather than be carved from it):

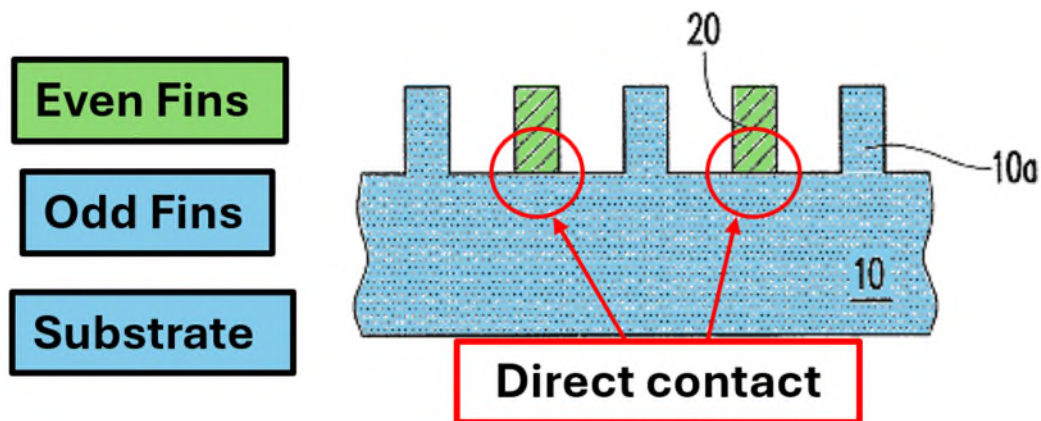


FIG. 6

(E.g., EX1001 at Fig. 6).

The Petition's Deficient Grounds: All of the challenged claims require the foregoing direct contact. For example, exemplary claim 1 recites that the claimed

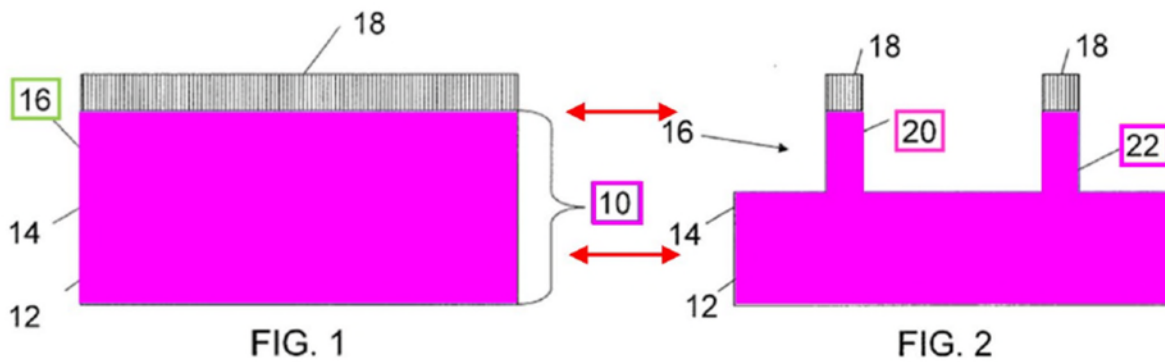
“plurality of even fins are in **direct contact** with the [substrate’s] semiconductor material.” (EX1001 at claim 1).²

Grounds 3A-7 simply ignore this “direct contact” requirement and do not attempt to identify it in any references or proposed combinations. (*E.g.*, Petition at 52-53, 77-79). For this reason alone, these grounds fail to establish the required reasonable likelihood of success.

The remaining grounds, Grounds 1-2, rely on the *Basker* reference as allegedly teaching the “direct contact” limitation. But the Petition identifies no such teaching or disclosure in *Basker*. The Petition cannot because *Basker*’s fins are formed **from** the substrate semiconductor material, not **in direct contact** with it.

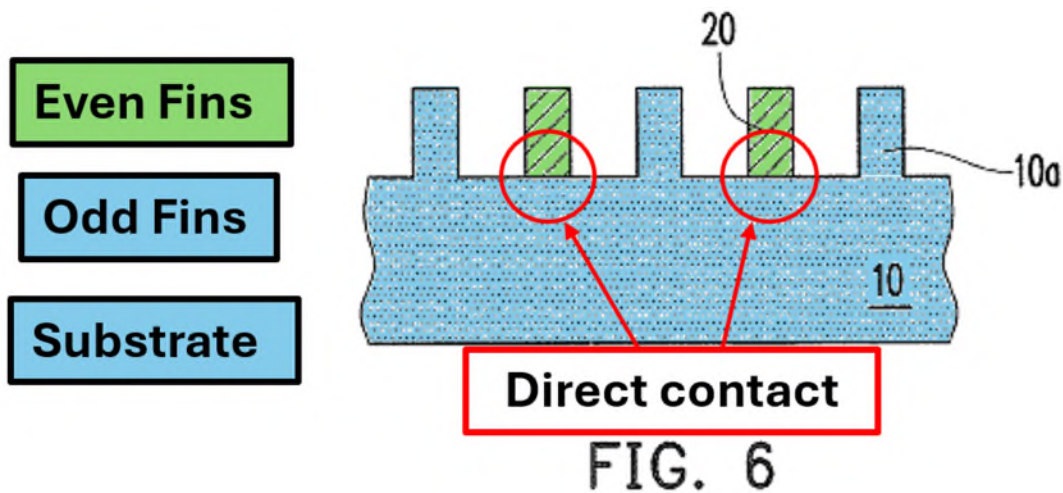
Indeed, the Petition itself admits, describes, and illustrates that in *Basker*, the purported odd/first fins and even/second fins are all made the same way, by etching away substrate semiconductor material to form the fins. (Petition at 23-24). The Petition illustrates this formation of the fins from the substrate’s semiconductor material in its following annotated *Basker* Figures:

² Unless otherwise indicated, all emphasis in quotations is added.



(Petition at 23-24).

The Petition does not even assert or attempt to show that a surface of any fin is touching (in “contact” with) a surface of the semiconductor material. It cannot, because as illustrated in the Petition’s own figures above, there is no surface of the fin that touches a different surface of the substrate’s semiconductor material; they are a single unitary integral body, with no distinct or contacting surfaces between them. This is completely opposite from the ’292 Patent, wherein the even/second fin is grown on the substrate semiconductor material and thus has a bottom surface that directly touches a top surface of the semiconductor material:



(*E.g.*, EX1001 at Fig. 6).

Thus, the Petition should be denied because, among other reasons, none of the grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teach or make obvious the “direct contact” limitation required in every challenged claim.

II. Semiconductor Transistor Technology Primer

The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (*e.g.*, fin) transistors; and (3) common process steps for creating transistors. (EX2001, ¶5).

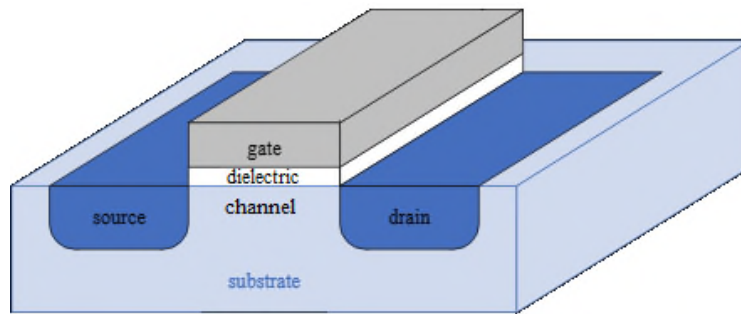
A. Basic Transistor Components

Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (i.e., turning electrical current on and off) and amplification (i.e., increasing the amplitude of a signal while retaining its electrical characteristics). (EX2002 at 1-2). Where earlier tube devices used a vacuum to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. (EX2002 at 3; EX2001, ¶6).

One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. (EX2002 at 29-34). In a conductor (e.g., a metal), electric current can flow freely. (EX2002 at 29). A dielectric (e.g., silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. (EX2002 at 30). Semiconductors (e.g., silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. (EX2002 at 31-34; EX2001, ¶7).

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel.

(See, e.g., EX2002 at 510-511). The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



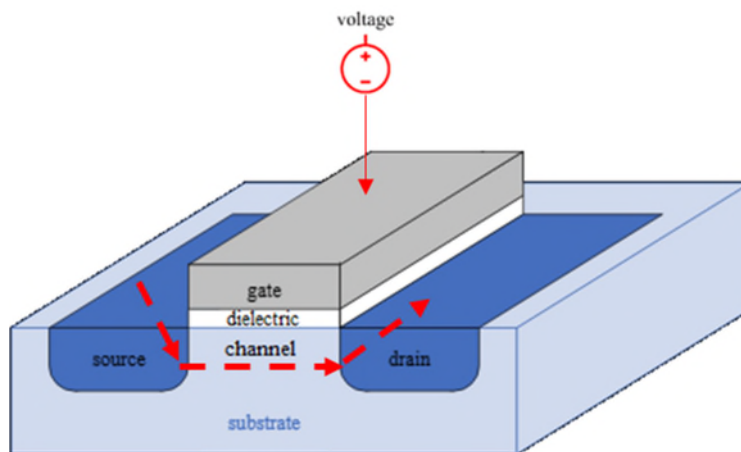
(See, e.g., EX2002 at 510-511; EX2001, ¶8).

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). (EX2002 at 26-28, 427-28). The channel is a region under the gate and between the source and drain, and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). (EX2002 at 510-511; EX2001, ¶9).

The gate is a conductor located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. (EX2002 at 510-511). When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation

of a “field effect” in the channel. (EX2002 at 510-511). This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). (EX2002 at 510-511; EX2001, ¶10).

As illustrated below, this field effect allows electrical current to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping the flow of electrical current. (EX2001, ¶11).



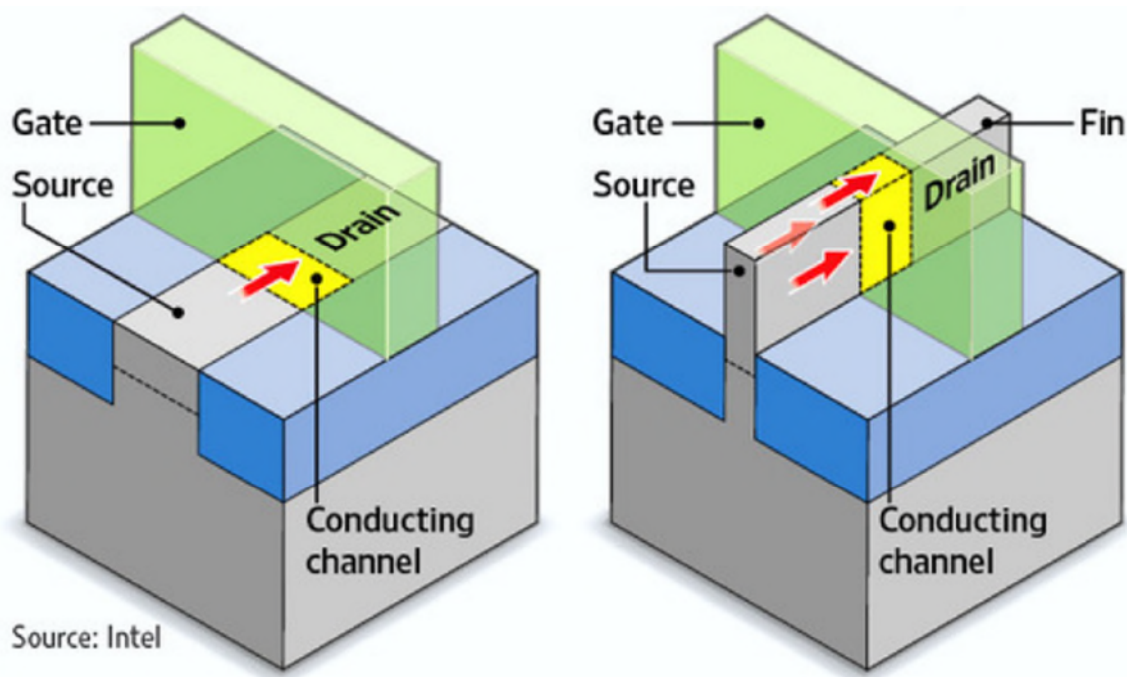
B. Planar vs. Three-Dimensional Transistors

Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more on a chip has been constant

and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.” (EX2001, ¶12).

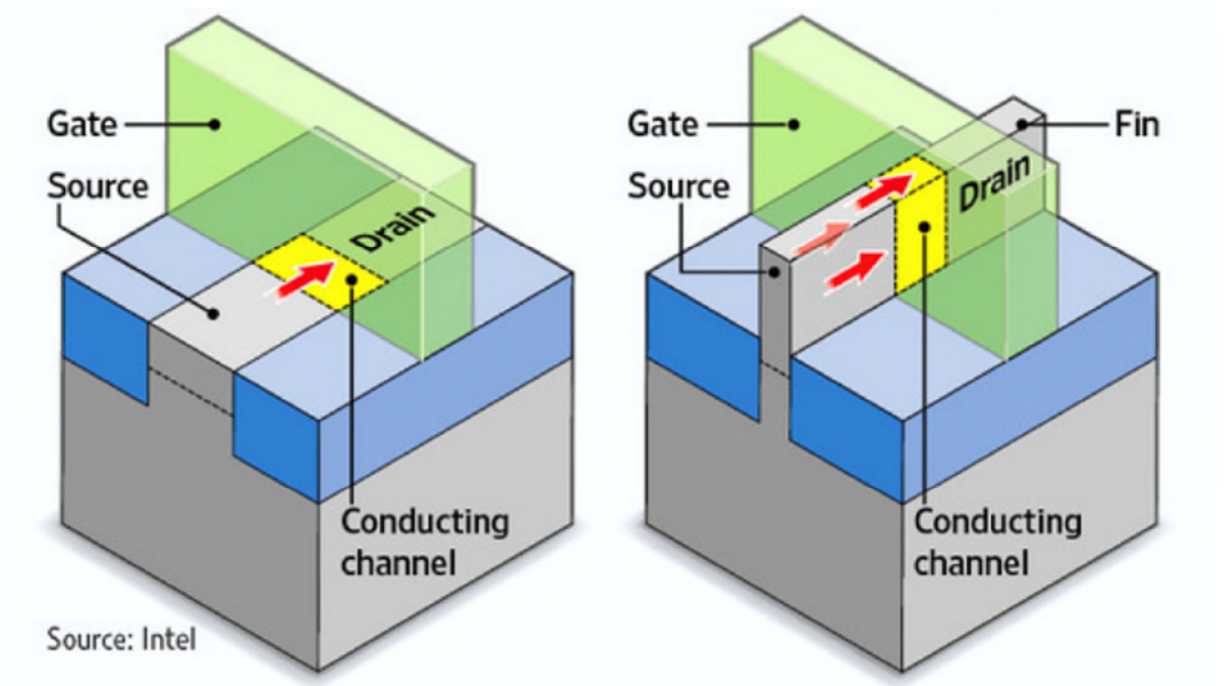
The simplified illustrative FET transistors illustrated in the previous section all feature a gate built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors. (EX2001, ¶13).

In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



(EX2001, ¶14).

In contrast, as illustrated below in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.



(EX2001, ¶15).

Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip. In addition, because

FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip. (EX2001, ¶16).

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. (EX2001, ¶17).

In the first stage, the semiconductor material itself is created. (EX2002 at 13). For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. (EX2002 at 13; EX2001, ¶18).

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” (EX2002 at 13-14). A wafer acts as a semiconductor substrate on and in which transistors may be formed. (EX2001, ¶19).

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. (EX2002 at 14).

Thousands of integrated circuits can be formed on the substrate of a single wafer. (EX2002 at 14; EX2001, ¶20).

In the packaging stage, the wafer is separated into individual chips. (EX2002 at 14-15; EX2001, ¶21).

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in the wafer's substrate. (EX2002 at 14). These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). (See EX2002 at 29-31, 71). For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. (EX2001, ¶22).

Layering is the operation used to add thin layers to the semiconductor substrate. (EX2002 at 72). The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. (EX2002 at 72; EX2001, ¶23).

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to

the semiconductor substrate additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. (EX2002 at 72; EX2001, ¶24).

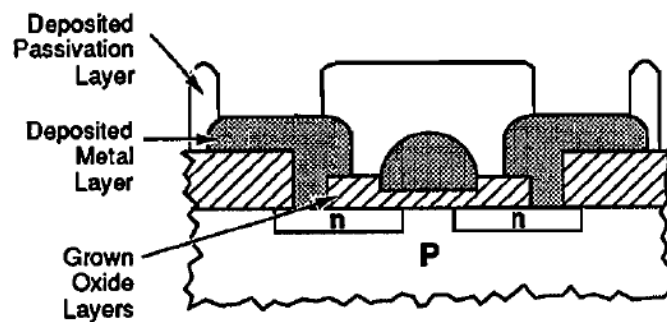


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. (EX2002 at 72-73). This creates a pattern on the wafer surface. (EX2002 at 72-73; EX2001, ¶25).

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. (EX2002 at 72-73; EX2001, ¶26). For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

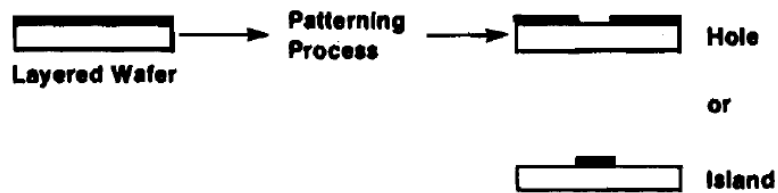


Figure 4.7 Patterning.

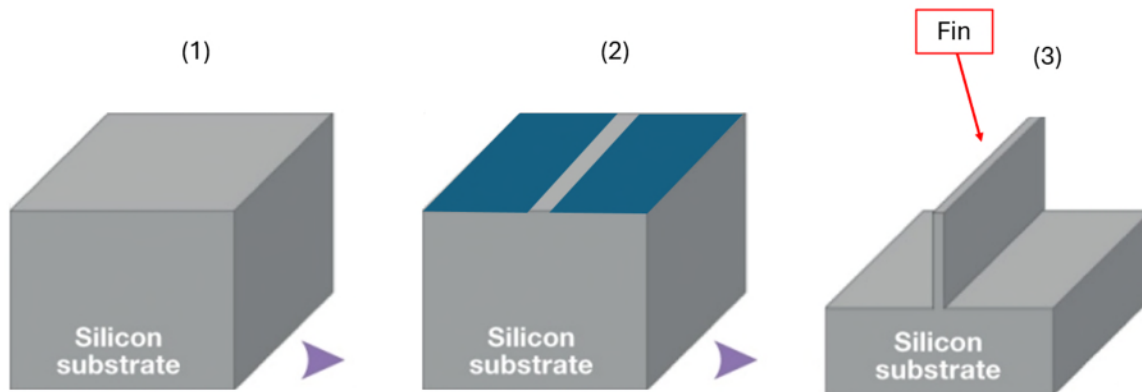
The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

(EX2002 at 73; EX2001, ¶27).

III. The Challenged '292 Patent

As the Petition acknowledges, a conventional method for forming the fins of an array of FinFETs was to (1) start with the wafer's semiconductor substrate; (2) apply the photomask pattern to the substrate; and (3) etch away portions of the substrate as defined by the pattern to form the fins. (Petition at 2-3; EX2001, ¶37).



The challenged '292 Patent recognized that this conventional use of patterning to form all FinFET fins from a semiconductor substrate had several drawbacks. For example:

[I]n the current FinFET process, the density of the fin patterns of the FinFET array is quite high and the thickness of the photoresist layer is quite large, so that the pattern development is difficult and accurate pattern transfer is impossible.

(EX1001 at 1:31-35; EX2001, ¶38).

The '292 Patent describes and claims an alternate approach to forming the fins, wherein different sets of fins could have different attributes, including, for example, the way they are fabricated, the materials from which they are made, and their dimensions. (EX2001, ¶39).

A. Different Sets of Fins

Instead of forming a single set of homogenous fins on a semiconductor chip, the '292 Patent describes forming different sets of fins on the same chip, each set differing from the other in one or more ways. For example, one set of fins could

be made in a different manner than the other set; one set of fins could have a different material composition than the other set of fins; and/or each fin set could have different dimensions from the other, such as different heights or different widths. (*E.g.*, EX1001 at Fig. 6, 3:37-49; EX2001, ¶40).

The '292 Patent alternately refers to these different sets of fins as odd or first fins, on the one hand, and even or second fins on the other. The patent's Figure 6 illustrates an embodiment of odd fins 10a (blue) and even fins 20 (green) and a semiconductor substrate 10 (also blue).

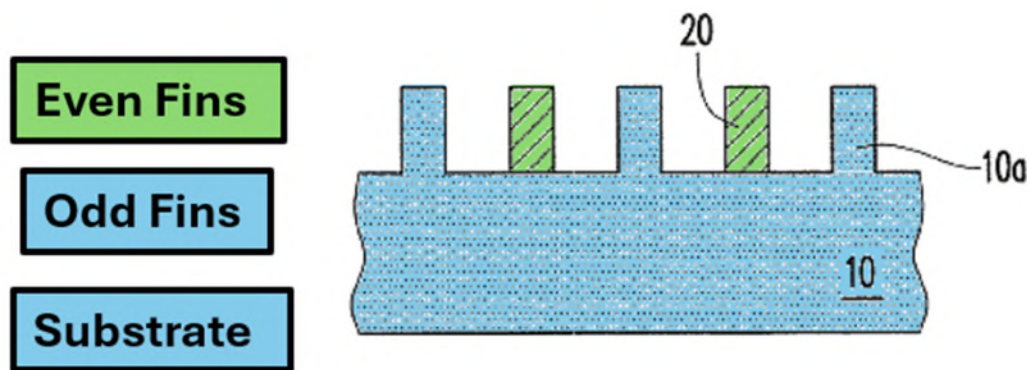


FIG. 6

(EX1001 at Fig 6; EX2001, ¶41) (colors and annotations added).

B. Fabricating The “Odd” Fins

The '292 Patent describes a non-limiting illustrative method for fabricating these different sets of fins so that they can have different attributes, including different fabrication processes, dimensions, and materials. (EX2001, ¶42).

For example, to make one set of fins (the “odd” fins), the patent describes starting with a silicon semiconductor substrate 10, illustrated in the following annotated Figure 1:

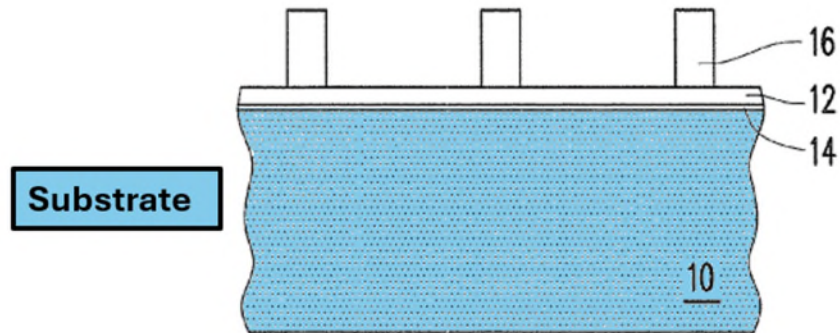
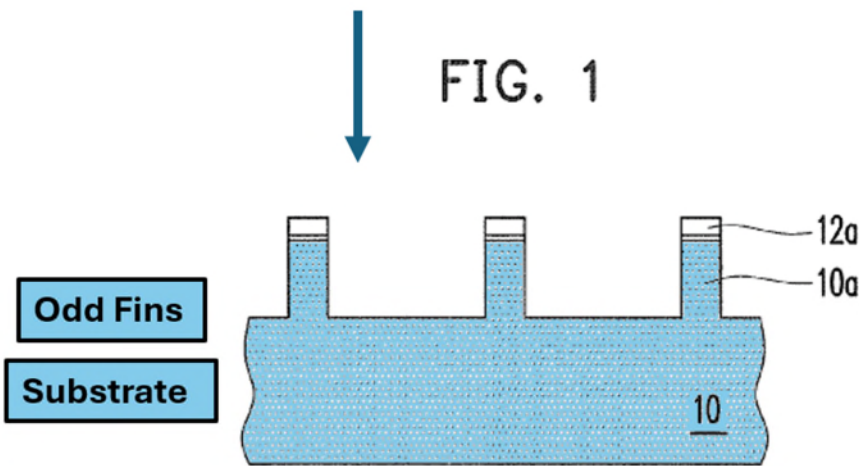
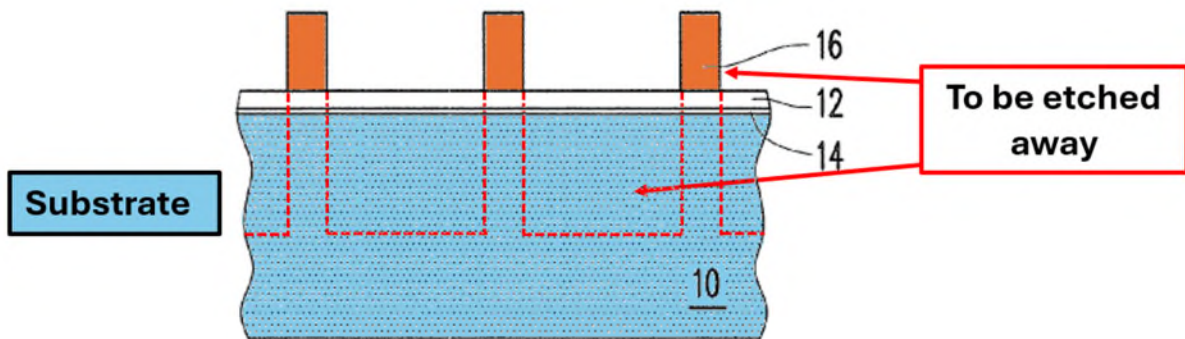


FIG. 1

(EX1001 at 2:48-50, Fig. 1; EX2001, ¶43).

This silicon substrate is then patterned to form a set of odd/first fins from the semiconductor substrate 10. For example, to perform this patterning, a patterned photoresist layer 16 (shown in orange below) may be deposited on the silicon substrate in the intended locations of the odd fins. Portions of the substrate are then etched away, excepting where the etching process is blocked by the patterned photoresist layer. The photoresist layers are consumed in this etching step and, as illustrated below in annotated Figure 2, patterning the substrate in this manner results in a plurality of odd fins 10a formed from the silicon substrate itself:



(EX1001 at 2:53-64, Figs. 1-2; EX2001, ¶44).

C. Fabricating The “Even” Fins

The '292 Patent further describes a different method for fabricating a set of even/second fins, so that those even fins differ from the odd fins. For example, the patent describes using layering and patterning to form spacers (annotated in yellow) located near the odd fins, as illustrated in Figure 4 below:

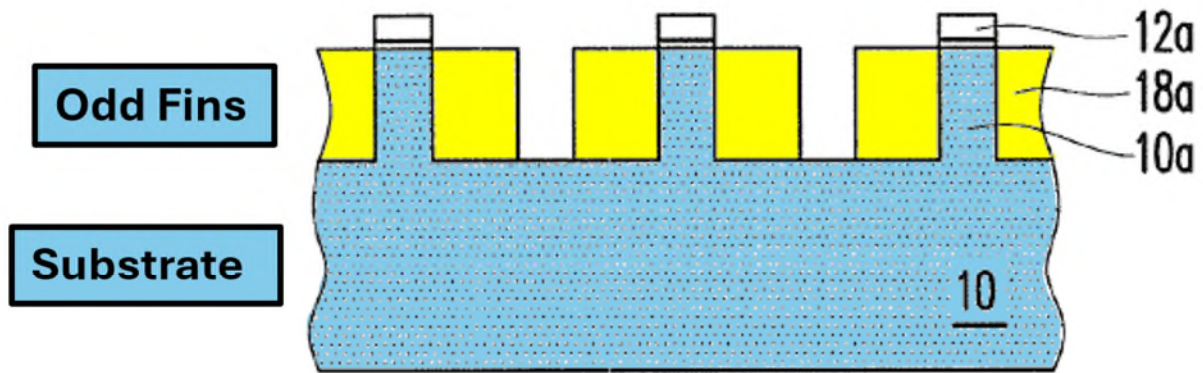


FIG. 4

(EX1001 at 2:65-3:16, Fig. 4; EX2001, ¶45).

Next, a material (such as SiGe) is grown in the gaps between the spacers:

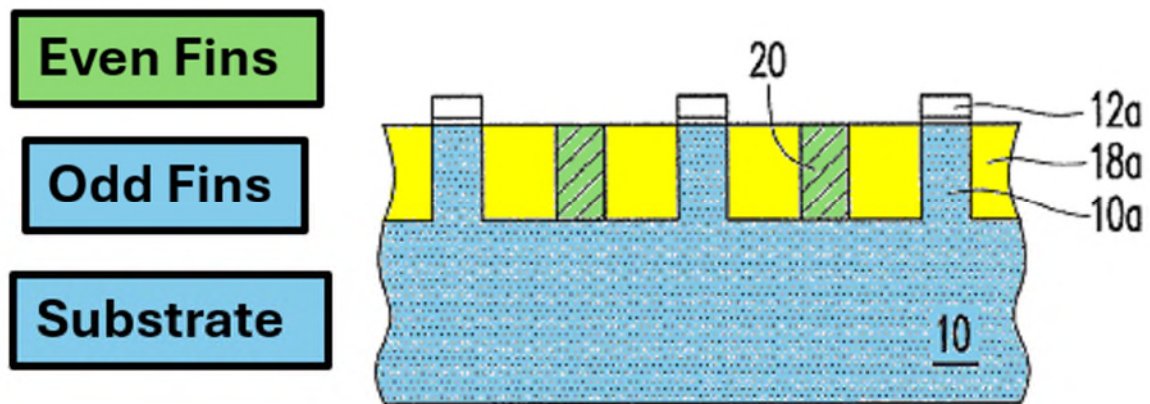


FIG. 5

(EX1001 at 3:29-34, Fig. 5; EX2001, ¶46).

Finally, the spacers are removed, leaving behind the odd/first set of fins 10a and the even/second set of fins 20:

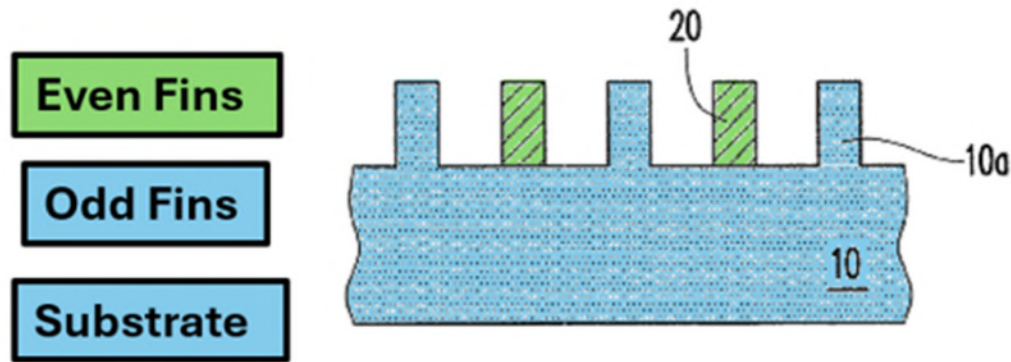
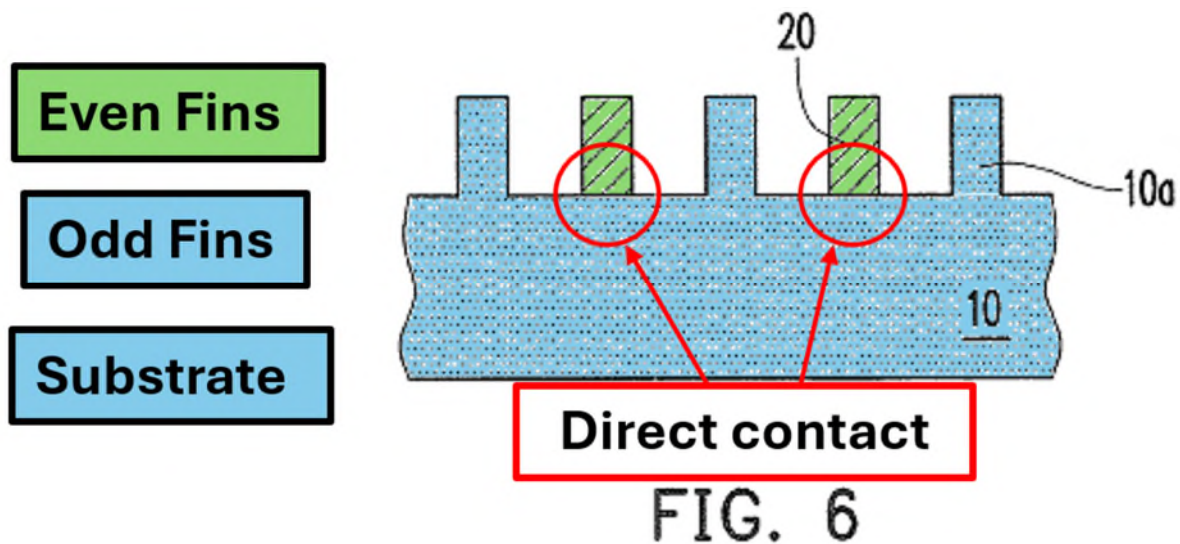


FIG. 6

(EX1001 at 3:50-52, Fig. 6; EX2001, ¶47).

D. Different Attributes of the Odd /First Fins and the Even/Second Fins

The foregoing illustrative process results in a semiconductor structure comprising fins with different attributes. For example, because the odd fins are patterned from the silicon substrate but the even fins are grown on the silicon substrate, the even fins are in direct contact with the substrate material and the odd fins are not. Instead, the odd fins are formed from the substrate material itself:



(*E.g.*, EX1001 at Fig. 6; EX2001, ¶48).

Similarly, in this illustration, because the odd fins are formed from the substrate material, they are the same material as that substrate (in this example, silicon). In contrast, the even fins in this example have a material composition different from the substrate and odd fins (in this example, silicon germanium). (*E.g.*, EX1001 at 3:37-41; EX2001, ¶49).

In addition, by controlling the even fin growth process and/or selectively sizing and orienting the spacers—and the gaps therebetween—the even fins may be formed having different dimensions than the odd fins, including the fin width or height. (*E.g.*, EX1001 at 3:42-49; EX2001, ¶50).

E. The Challenged Claims

The Petition challenges '292 Patent claims 1-20. Each of these claims incorporates one or more of the foregoing differences between the claims and the

asserted prior art. For example, all of the claims recite that the even/second fins are in direct contact with the substrate's semiconductor material and are different from the claimed odd/first fins in either material or width. Independent claim 1 is exemplary of these common limitations found in every challenged claim:

1. A semiconductor structure for forming FinFETs, comprising
a semiconductor substrate, wherein a top portion of **the semiconductor substrate comprises a semiconductor material**;
a plurality of odd fins of the FinFETs on the semiconductor substrate, being defined from the semiconductor substrate and being formed of the semiconductor material; and
a plurality of **even fins** of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being **different from the odd fins** of the FinFETs **in at least one of width and material**, wherein the plurality of **even fins are in direct contact with the semiconductor material**.

(EX1001 at claim 1; EX2001, ¶51).

The remaining independent claims 9 and 15 (and their dependent claims) also include these limitations. Claim 9 identically recites “a plurality of **even fins** of the FinFETs on the semiconductor substrate between the odd fins of the FinFETs, being **different from the odd fins** of the FinFETs **in at least one of width and material**, wherein the plurality of **even fins are in direct contact with the semiconductor material**.” (EX1001 at claim 9; EX2001, ¶52).

Claim 15 also claims these limitations, but for a plurality of “second” fins rather than a plurality of “even” fins: **“the second fins are different from the first fins of the FinFETs in at least one of width and material, wherein the plurality of second fins are in direct contact with the semiconductor material.”** (EX1001 at claim 15; EX2001, ¶53).

IV. PTAB Should Deny the Petition Because It Fails to Establish the Required Likelihood of Success

The Petition asserts eight different grounds against various selections of claims:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1	1, 3-9, 11-15, 17-20	103	Basker + Hill
2	2, 10, 16	103	Basker + Hill + Yu
3A/3B	1, 5, 7-9, 13, 15, 19	102/103	Inaba
4	3, 4, 6, 11, 12, 14, 17, 18, 20	103	Inaba + Basker
5	2, 10, 16	103	Inaba + Yu
6	1, 3-9, 11-15, 17-20	103	Liaw + Basker
7	2, 10, 16	103	Liaw + Basker + Yu

(Petition at 1). The Petition should be denied because, among other reasons, none of these grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teach or make obvious each limitation in any challenged claim. (EX2001, ¶54).

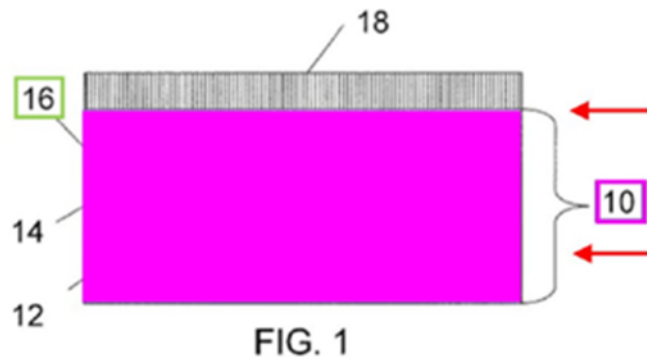
For example, each ground fails to identify a reference that teaches the claimed even/second fins “in direct contact with the [substrate’s] semiconductor material” limitation required in every challenged claim. Grounds 1-2 rely on the *Basker* reference as supposedly teach this “direct contact” limitation; Grounds 3A-5 and Grounds 6-7 ignore the limitation altogether. (EX2001, ¶55).

“Contact” occurs where two different surfaces touch one another, where there is a “union or junction of surfaces.” (EX2003 at 249). But none of these references teach an even/second fin having a surface that touches a surface of the substrate semiconductor material, and Petitioners have identified no reason for finding otherwise. Instead, in each of these references, the alleged even/second fins are admittedly made in a conventional manner, by etching away portions of the substrate’s semiconductor material to form the fins, just as the alleged odd/first fins are. In other words, these fins are not formed in direct contact with the substrate semiconductor material; they are formed from that substrate semiconductor material itself—there are no surfaces of the fin touching a different surface of the semiconductor material because, as the Petition concedes, the fins and substrate semiconductor material do not have any surfaces distinct from one another but are a single unitary body. (EX2001, ¶56).

A. Grounds 1-2: Basker Does Not Teach The Claimed “Direct Contact”

Grounds 1-2 rely solely on the *Basker* reference (EX1006) as allegedly teaching the claimed even/second fins “in direct contact with the [substrate’s] semiconductor material” limitation required in every challenged claim. (*E.g.*, Petition at 25, 28). But the Petition identifies no such teaching or disclosure in *Basker*. The Petition cannot because *Basker*’s fins are formed **from** the substrate semiconductor material, not **in direct contact** with it. (EX2001, ¶57).

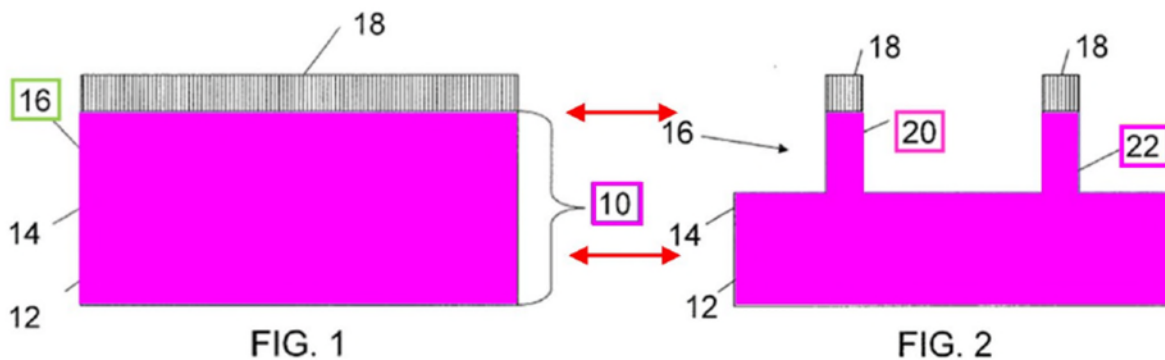
As the Petition itself describes, Basker starts with substrate 10 comprising silicon semiconductor material, as shown in this annotated figure from the Petition:



(Petition at 23-24; EX1006 at ¶0024, Fig. 1; EX2001, ¶58).

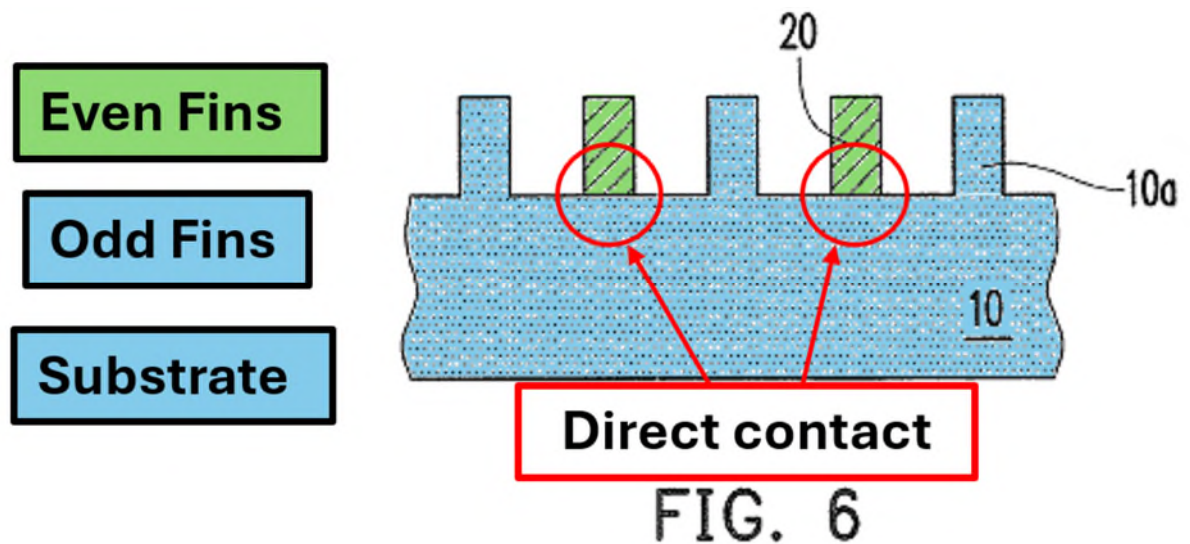
As the Petition further describes, the alleged odd/first fins 20 and alleged even/second fins 22 are then formed by patterning the substrate’s semiconductor material. Specifically, portions of the substrate’s semiconductor material are etched away to form the alleged odd/first fins 20 and alleged even/second fins 22.

(Petition at 23-24; EX1006 at ¶¶ 26-28, Figs. 1-2). The Petition illustrates this formation of the fins from the substrate's semiconductor material in the following annotated Figure:



(Petition at 23-24; EX1006 at ¶¶ 26-28, Figs. 1-2; EX2001, ¶59).

The Petition does not even assert or attempt to show that a surface of any fin is touching another surface of the semiconductor material. It cannot, because as illustrated in the Petition's own figures above, there is no surface of any fin that touches a different surface of the substrate's semiconductor material because each of the fins and the substrate are a single unitary integral body, with no distinct surfaces between them. This is in direct contrast with the even/second fin of the '292 Patent, which is grown on the substrate semiconductor material and thus has a bottom surface that directly touches a top surface of the semiconductor material:



(EX2001, ¶60).

Nonetheless, the Petition asserts that because each of these fins is formed from the semiconductor substrate material, they are also somehow in direct contact with that same material. The Petition does not explain how the “contact” limitation is supposedly met here. Instead, the Petition merely concludes that since fins 20 and 22 were “formed by etching the top partition of bulk substrate 10, the [fins 20 and 22] (the remaining/non-etched portion of the substrate) [are] ‘in direct contact with [the substrate’s semiconductor material]’ as the fin[s] and substrate 10 were in unity before etching.” (Petition at 25 (analyzing fin 20) and 28 (applying that same analysis to fin 22)). This conclusory sentence is the total extent of the

Petition's attempt to identify the "direct contact" requirement in *Basker*.³

(EX2001, ¶61).

But the Petition does not explain this conclusion, and there is no reasonable explanation because the conclusion makes no sense. In fact, the fins are **not in direct contact** with the substrate's semiconductor material; as the Petition concedes, they are **formed from** the substrate's semiconductor material. The fins cannot be formed from and integral with the substrate material and simultaneously have their own distinct surfaces that are touching distinct surfaces of that same substrate material. And the Petition does not explain how the fin somehow has a surface that touches another surface of the substrate semiconductor material when

³ *Basker* later describes doping the top of silicon fin 22 with germanium so that it further comprises silicon germanium. (EX1006 at ¶ 31). But this does not change the fact that fin 22 is formed from the substrate semiconductor material, rather than having a distinct surface touching a surface of that substrate material, and the Petition does not contend otherwise. Instead, the Petition relies solely on its argument that the fins are somehow in direct contact with the substrate material because they were literally carved from that substrate material. (Petition at 25 (analyzing fin 20) and 28 (applying that same analysis to fin 22)).

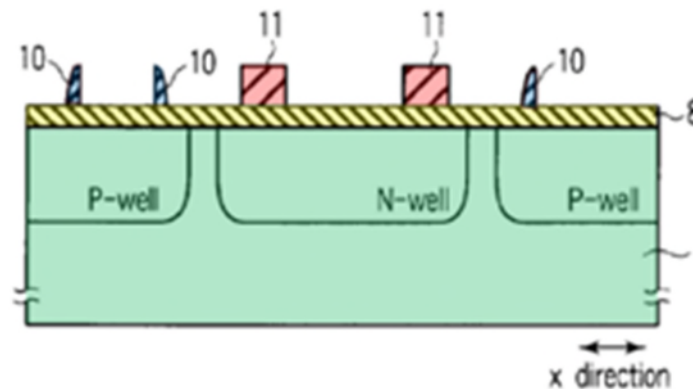
the fin is that semiconductor material. There is no explanation, and the Petition thus fails to establish a reasonable likelihood of success for Grounds 1-2. (EX2001, ¶62).

B. Grounds 3A-5: Inaba Does Not Teach The Claimed “Direct Contact”

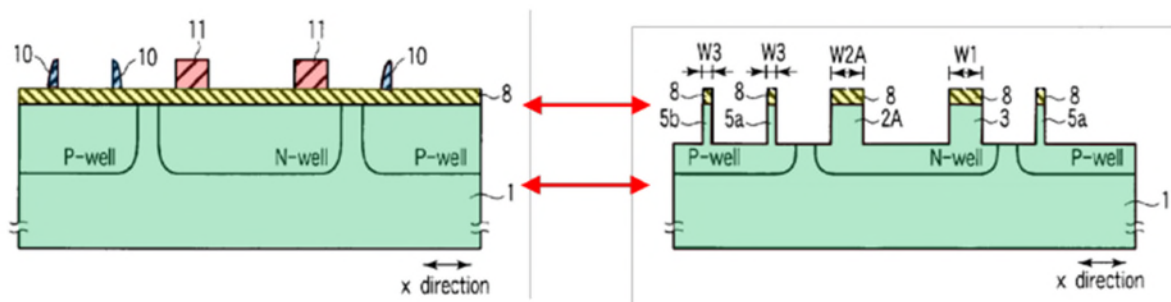
Although Grounds 3A-5 rely on *Inaba* (EX1005) as teaching the alleged odd/first fins and even/second fins, the Petition does not allege that *Inaba*—or any other references asserted in these Grounds—teaches that the alleged even/second fins are “in direct contact with the [substrate’s] semiconductor material” limitation required in every challenged claim. (*E.g.*, Petition at 52-53). Instead, the Petition’s analysis for these grounds ignores this requirement all together, addressing only whether the alleged even/second fins meet different requirements (such as whether theses fins are on, between, and wider), but not addressing the additional “direct contact” requirement. (Petition at 52-53). For this reason alone, Grounds 3A-5 fail. (EX2001, ¶63).

Although the analysis can and should stop there, the Petition’s allegations concerning *Inaba* and its alleged odd/first fins establish that none of *Inaba*’s fins are in direct contact with the substrate’s semiconductor material—as with *Basker*, *Inaba*’s fins are formed from the substrate semiconductor material, not in direct contact with it. (EX2001, ¶64).

Indeed, the Petition itself describes and illustrates that in *Inaba*, all of the fins are formed from the substrate semiconductor material. The Petition describes and illustrates that *Inaba* starts with a substrate of semiconductor material, which the Petition annotates below in green:



(Petition at 49-50). The Petition then describes and illustrates that in *Inaba*, fins are then formed by patterning the substrate's semiconductor material. Specifically, portions of the substrate's semiconductor material are etched away to form the fins 2, 3, 5a, 5b, and 5x. (Petition at 51). The Petition illustrates *Inaba*'s formation of the fins from the substrate's semiconductor material in the following annotated Figure:



(Petition at 49-51; EX2001, ¶65).

Thus, as the Petition itself illustrates, there is no surface of the *Inaba* fins that touches a different surface of the substrate’s semiconductor material because they are a single unitary integral body, with no distinct surfaces between them. There is thus no “direct contact” as required by all challenged claims. (EX2001, ¶66).

Accordingly, the Petition does not even argue that *Inaba* (or any other Grounds 3A-5 references) teaches or make obvious even/second fins that “are in direct contact with the [substrate] semiconductor material.” It could not because all fins are simply made of the semiconductor substrate, and that material cannot be in contact with itself. Because the Petition’s Grounds 3A-5 ignore and do not establish a reasonable likelihood of success on this required limitation, they provide no basis for instituting. (EX2001, ¶67).

C. Grounds 6-7: Liaw Does Not Teach The Claimed “Direct Contact”

Finally, Grounds 6-7 suffer from at least the same flaws as Grounds 1-5. To start (and identical to the *Inaba* Grounds), although Grounds 3A-5 rely on *Liaw* (EX1008) as teaching the alleged odd/first fins and even/second fins, the Petition does not allege that *Liaw*—or any other references asserted in these Grounds—teaches that the alleged even/second fins are “in direct contact with the

[substrate's] semiconductor material" limitation required in every challenged claim. (*E.g.*, Petition at 77-79). Instead, the Petition's analysis for these grounds ignores this requirement all together, addressing only whether the alleged even/second fins meet different requirements (such as whether theses fins are on, between, and wider), but **not** addressing the additional "direct contact" requirement. (Petition at 77-79). For this reason alone, Grounds 6-7 fail. (EX2001, ¶68).

And although the analysis can and should stop there, the Petition's allegations concerning *Liaw* and its alleged odd/first fins establish that **none** of *Liaw*'s fins are in direct contact with the substrate's semiconductor material—as with *Basker* and *Inaba*, *Liaw*'s fins are **formed from** the substrate semiconductor material, not **in direct contact** with it. (EX2001, ¶69).

Indeed, the Petition admits and describes that *Liaw* discloses making its fins in the same manner as *Basker* and *Inaba*: starting with a substrate semiconductor material and patterning that material to form the fins. For example, the Petition states that *Liaw* starts with a substrate of semiconductor material and then forms *Liaw*'s fins 186 and 188 "by etching/removing the substrate material in certain regions," as illustrated in the Petition's following annotated figure:

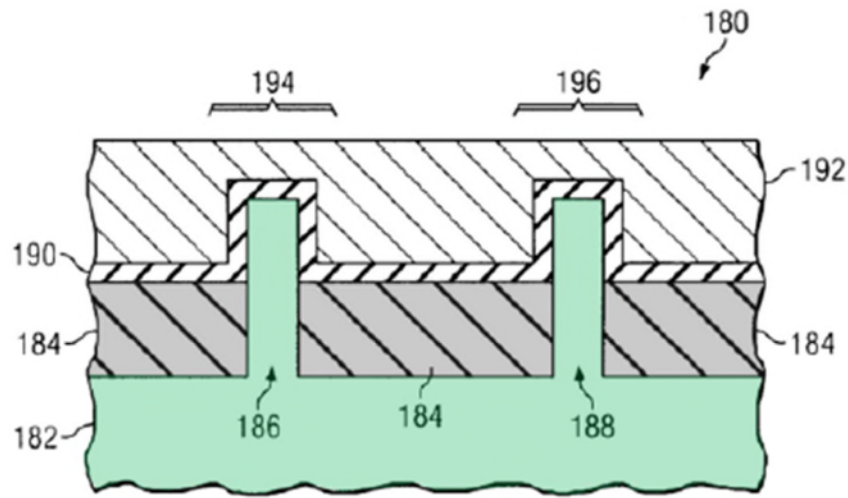


Fig. 7

EX1008, FIG. 7

(Petition at 66, 73, 74, 76; EX2001, ¶70).

Thus, the Petition itself establishes that there is no surface of the *Liaw* fins that touches a different surface of the substrate's semiconductor material because they are a single unitary integral body, with no distinct surfaces between them. There is thus no "direct contact" as required by all challenged claims. (EX2001, ¶71).

Accordingly, the Petition does not even argue that *Liaw* (or any other Grounds 6-7 references) teaches or make obvious even/second fins that “are in direct contact with the [substrate] semiconductor material.” It could not because all fins are simply made of the semiconductor substrate, and that material cannot be in contact with itself. Because the Petition’s Grounds 6-7 ignore and do not establish a reasonable

likelihood of success on this required limitation, they provide no basis for instituting.
(EX2001, ¶72).

V. Conclusion

For the foregoing reasons, the Board should deny institution of the Petition.

Dated: August 15, 2025

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 5,234. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

Dated: August 15, 2025

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CERTIFICATE OF SERVICE

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