

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD. and
APPLE, INC.,
Petitioners

v.

MARLIN SEMICONDUCTOR LIMITED.
Patent Owner

Case IPR2025-00864
Patent No. 9,184,292

PETITIONERS' CURRENT LIST OF EXHIBITS

LIST OF EXHIBITS

Ex. No.	Description	Previously Submitted
EX1001	U.S. Patent No. 9,184,292	X
EX1002	Declaration of Dr. Sanjay Banerjee.	X
EX1003	Curriculum Vitae of Dr. Sanjay Banerjee.	X
EX1004	Prosecution History of U.S. Patent No. 9,184,292	X
EX1005	U.S. Patent Application Publication No. 2008/0308848 (“Inaba”)	X
EX1006	U.S. Patent Application Publication No. 2011/0108920 (“Basker”)	X
EX1007	U.S. Patent Application Publication No. 2009/0057846 (“Doyle”)	X
EX1008	U.S. Patent No. 8,942,030 (“Liaw”)	X
EX1009	U.S. Patent No. 7,297,581 (“Hill”)	X
EX1010	U.S. Patent Application Publication No. 2008/0230852 (“Yu”)	X
EX1011	RESERVED	
EX1012	Complaint (Dkt. No. 1) in <i>Longitude Licensing Ltd. et al v. Lenovo Group Limited et al</i> , Case No. 2:25-cv-00171 (E.D.Tex. Feb. 13, 2025).	X
EX1013	S. Balakumar, et al., “Solid phase epitaxy during Ge condensation from amorphous SiGe layer on silicon-on-insulator substrate,” <i>Applied Phys. Lett.</i> , 89, 032101, 1-4, July 2006.	X
EX1014	U.S. Patent No. 8,625,334 (“Liaw-334”)	X

EX1015	U.S. Patent Application Publication No. US2008/0020515 (“White”)	X
EX1016	J. Franco, et al., “Improvements of NBTI reliability in SiGe p-FETs,” <i>2010 IEEE International Reliability Physics Symposium</i> , Anaheim, CA, USA, 2010, pp. 1082-1085.	X
EX1017	J. Huang et al., “Mechanisms limiting EOT scaling and gate leakage currents of high-k/metal gate stacks directly on SiGe and a method to enable sub-1nm EOT,” <i>2008 Symposium on VLSI Technology</i> , Honolulu, HI, USA, 2008, pp. 82-83.	X
EX1018	J. Oh <i>et al.</i> , “Additive mobility enhancement and off-state current reduction in SiGe channel pMOSFETs with optimized Si Cap and high-k metal gate stacks,” <i>2009 International Symposium on VLSI Technology, Systems, and Applications</i> , Hsinchu, Taiwan, 2009, pp. 22-23.	X
EX1019	S. M. Sze, “Physics of Semiconductor Devices,” <i>John Wiley & Sons</i> , 1981, Chapter 8, pp. 431-456.	X
EX1020	J. D. Plummer, “Silicon VLSI Technology: Fundamentals, Practice and Modelling,” <i>Prentice Hall</i> , 2000, Chapter 10, pp. 637-650.	X
EX1021	RESERVED	X
EX1022	RESERVED	
EX1023	U.S. Patent Application Publication No. 2007/0069302 (“Jin”)	X
EX1024	U.S. Patent No. 6,787,406 (“Hill-406”)	X
EX1025	H. Adhikari <i>et al.</i> , “High mobility SiGe shell-Si core omega gate pFETS,” <i>2009 International Symposium on VLSI Technology, Systems, and Applications</i> , Hsinchu, Taiwan, 2009, pp. 136-138	X

EX1026	R. Bijesh <i>et al.</i> , “Hole mobility enhancement in uniaxially strained SiGe FINFETs: Analysis and prospects,” <i>69th Device Research Conference</i> , Santa Barbara, CA, USA, 2011, pp. 237-238.	X
EX1027	Intel Newsroom (2011)	X
EX1028	Intel 22nm Announcement Presentation (2011)	X
EX1029	Intel 22nm Details Presentation (2011)	X
EX1030	S. Bedell <i>et al.</i> , “Opportunities and Challenges for Germanium and Silicon-Germanium Channel p-FETs,” <i>ECS Transactions</i> , Vol. 19, No. 1	X
EX1031	J. Mitard <i>et al.</i> , “High-mobility 0.85nm-EOT Si _{0.45} Ge _{0.55} -pFETs: Delivering high performance at scaled VDD,” <i>2010 International Electron Devices Meeting</i> , San Francisco, CA, USA, 2010, pp. 10.6.1-10.6.4.	X
EX1032	M. Poljak <i>et al.</i> , “Improving bulk FinFET DC performance in comparison to SOI FinFET,” <i>Microelectronic Engineering</i> , Vol. 86, Issue 10, Oct. 2009, Pp. 2078-2085.	X
EX1033	Mukherjee, Debasish and Hemanta Kr. “Static Noise Margin Analysis of SRAM Cell for High Speed Application,” <i>IJCSI International Journal of Computer Science Issues</i> , Vol. 7, Issue 5, Sept. 2010.	X
EX1034	V. Huard <i>et al.</i> , “NBTI degradation: From transistor to SRAM arrays,” <i>2008 IEEE International Reliability Physics Symposium</i> , Phoenix, AZ, USA, 2008, pp. 289-300.	X
EX1035	M. Alioto, “Analysis of layout density in FinFET standard cells and impact of fin technology,” <i>Proceedings of 2010 IEEE International Symposium on Circuits and Systems</i> , Paris, France, 2010, pp. 3204-3207.	X

EX1036	Zheng Guo, S. Balasubramanian, R. Zlatanovici, Tsu-Jae King and B. Nikolic, "FinFET-based SRAM design," <i>ISLPED '05. Proceedings of the 2005 International Symposium on Low Power Electronics and Design, 2005.</i> , San Diego, CA, USA, 2005, pp. 2-7.	X
EX1037	U.S. Patent Application Publication No. 2007/0194833 ("Takeyama")	X
EX1038	W. Qi et al., "Investigation on solid phase epitaxy of deposited SiGe film on a Si substrate," <i>Thin Solid Films</i> , Vol. 293, Issues 1–2, 30 Jan. 1997, Pp. 310-314.	X
EX1039	U.S. Patent No. 8,367,498 ("Chang")	X
EX1040	Cotte et al., "Predicting critical dimension uniformity in advanced electron-beam projection lithography masks," <i>J. Vac. Sci. Technol. B</i> 21, 3027–3031 (2003).	X
EX1041	Docket Navigator list of district court cases and inter partes review proceedings involving U.S. Patent No. 9,184,292, last accessed on Aug. 11, 2025	
EX1042	Continuity Application 14/340,267 data sheet, last accessed Aug. 11, 2025 and available at https://patentcenter.uspto.gov/applications/14340267/continuity?application=	
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EX1048	U.S. Patent No. 8,618,556 ("Wu")	
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1100	Institution Decisions for TSMC, based on Lex Machina data.	

1101	<i>Certain Integrated Circuits With Voltage Regulators And Products Containing Same</i> , Inv. No. 337-TA-1024, USITC Order 55 (Aug. 31, 2018).	
1102	<i>Certain Personal Computer/Consumer Electronic Convergent Devices, Components Thereof, And Products Containing Same</i> , Inv. No. 337-TA-558 (USITC Order 6 (Feb. 7, 2006).	
1103	<i>Certain Unmanned Aerial Vehicles And Components Thereof</i> , Inv. No. 337-TA-1133, USITC Comm’n Op. (Sept. 8, 2020).	
1104	Jennifer Nall, <i>How delayed Notice of Date Accorded mailings may affect inter partes review</i> , DLA Piper (last visited Aug. 8, 2025), available at https://www.dlapiper.com/en/insights/publications/intellectual-property-news/2025/how-delayed-notice-of-date-accorded-mailings-may-affect-inter-partes-review .	
1105	Memorandum from Scott R. Boalick to PTAB AIA Paneling re: Notice of Filing Date Accorded for AIA Petitions (July 18, 2025).	
1106	Final Written Decision Outcomes for TSMC, available at https://law.lexmachina.com/party/ptab?filing_date-from=2012-09-16&filing_date-to=&final_decision_date-from=2013-07-17&final_decision_date-to=&new_trial_flow-exclude=PreI_AS&party_role-include=Petitioner&filters=true&id=26931&id=20676624&id=64431208&tab=ptab_trial_flow&view=analytics&cols=trial%2Cfiled%2Cinstitution_decision_date%2Cpatent%2Cpetitioners%2Cpatent_owners%2Ctrial_resolution%2Cfinal_decision_date .	
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1108	<i>Certain Foreign-Fabricated Semiconductor Devices, Products Containing The Same, And Components Thereof</i> , Inv. No. 337-TA-1443, USITC Order 10 (May 7, 2025).	

1109	<i>Certain Power Inverters And Converters, Vehicles Containing The Same, And Components Thereof</i> , Inv. No. 337-TA-1267, USITC Order 6 (Aug. 4, 2021).	
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1113	Letter from Billie Chen to Under Secretary Andrei Iancu regarding USPTO Request for Comments on Discretion to Institute Trials Before the Patent Trial and Appeal Board, Docket No. PTO-C-2020-055.	
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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on August 15, 2025, I caused a true and correct copy of the foregoing Petitioner's Current List of Exhibits to be served electronically on counsel for Patent Owner at the following addresses:

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