

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Tien-Yu Lu
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP2505USA

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6970373		2005-11-29	Datta	
	2	7994583		2011-08-09	Inaba	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
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NON-PATENT LITERATURE DOCUMENTS								
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		
EXAMINER SIGNATURE			
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2015-07-06
Name/Print	Winston Hsu	Registration Number	41,526

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

**LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD
THEREOF**

As the below named inventor, I hereby declare that:
This declaration is directed to:

☒ The attached application, or

☐ United States application number _____ filed on _____, or

☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUL 02 2015 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP2505USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Tien-Yu Lu**

Date: **JUL 02 2015**

Signature:

Tien - Yu Lu

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
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Docket No NAUP2505USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chang-Hung Chen**

Date: JUL 02 2015

Signature:

Chang-Hung Chen

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I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

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representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

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Docket No NAUP2505USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Yu-Tse Kuo**

Date: **JUL 02 2015**

Signature: Yu Tse Kuo

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representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the purposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this JUL 02 2015 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP2505USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chun-Hsien Huang**

Date: **JUL 02 2015**

Signature: Chun - Hsien Huang

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82A (07-12)

Approved for use through 11/30/2014. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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REGISTERED PRACTITIONERS**

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Application Number	N/A
Filing Date	N/A
First Named Inventor	Tien-Yu Lu
Title	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	NAUP2505USA

SIGNATURE of Applicant or Patent Practitioner

Signature	/Winston Hsu/	Date	07/06/2015
Name	Winston Hsu	Telephone	3027291562
Registration Number	41,526		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

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- ☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

OR

27765

- ☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

- ☒ The address associated with the above-mentioned Customer Number

OR

- ☐ The address associated with Customer Number:

OR

Firm or Individual Name				
Address				
City	State	Zip		
Country				
Telephone	Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

UNITED MICROELECTRONICS CORP.

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	MAY 12 2015
Name	Chia-Tsung Hung		
Title	CHAIRMAN		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

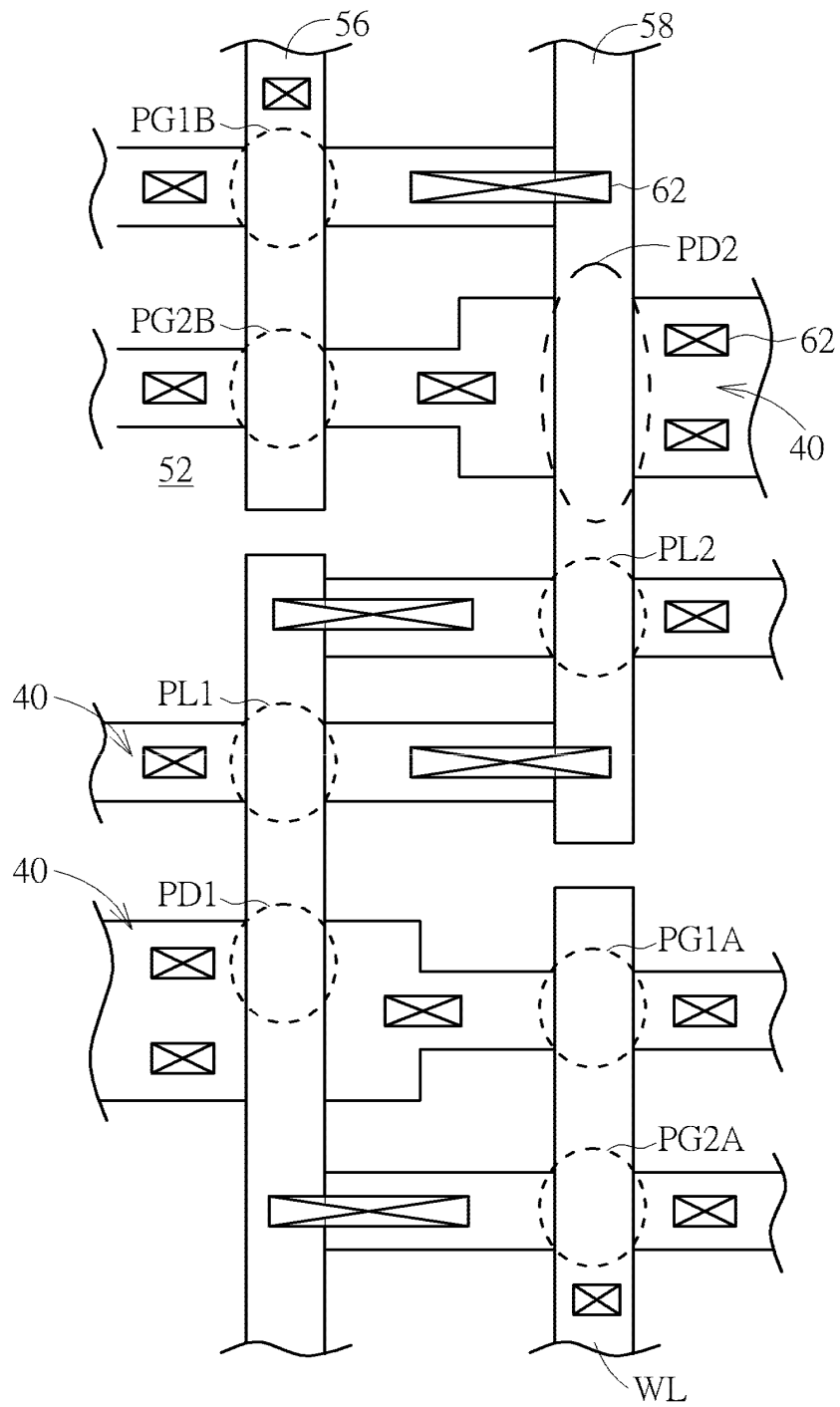


FIG. 1

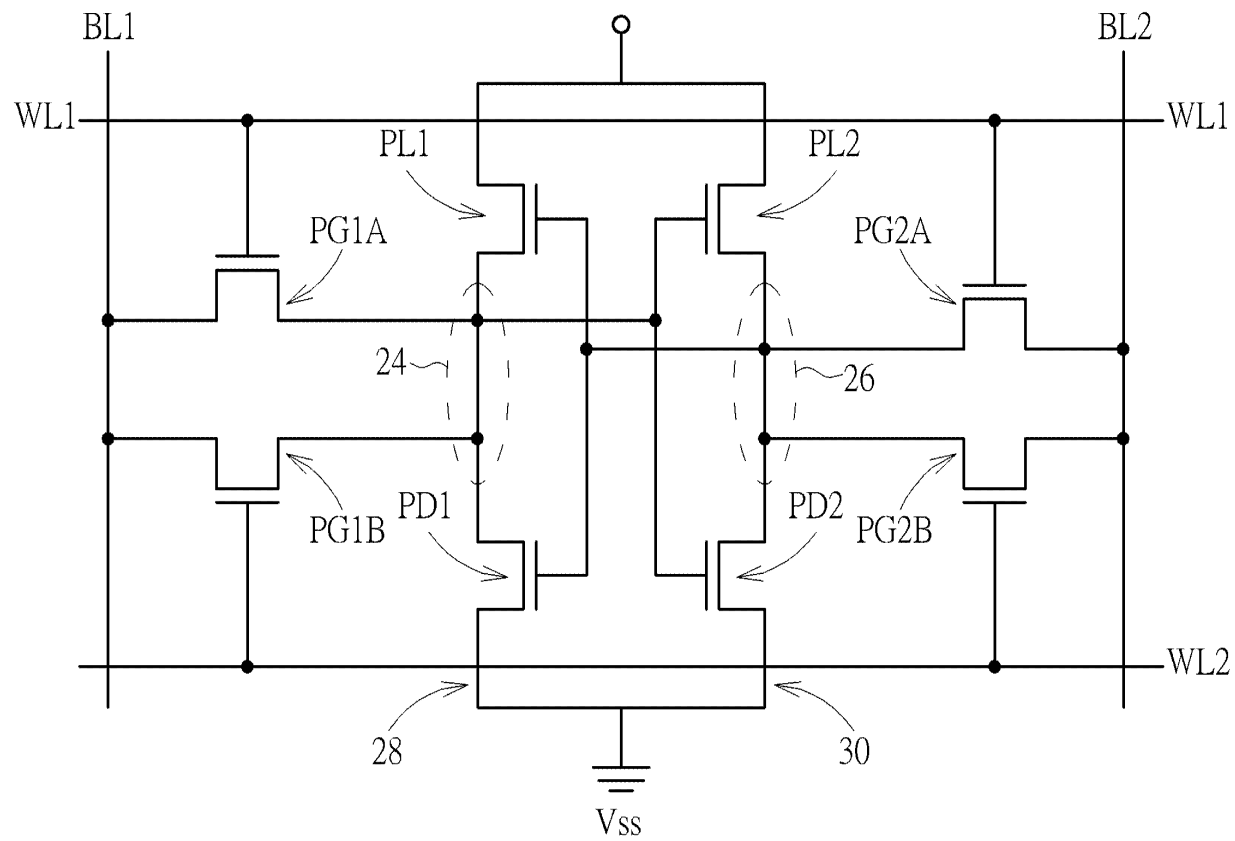


FIG. 2

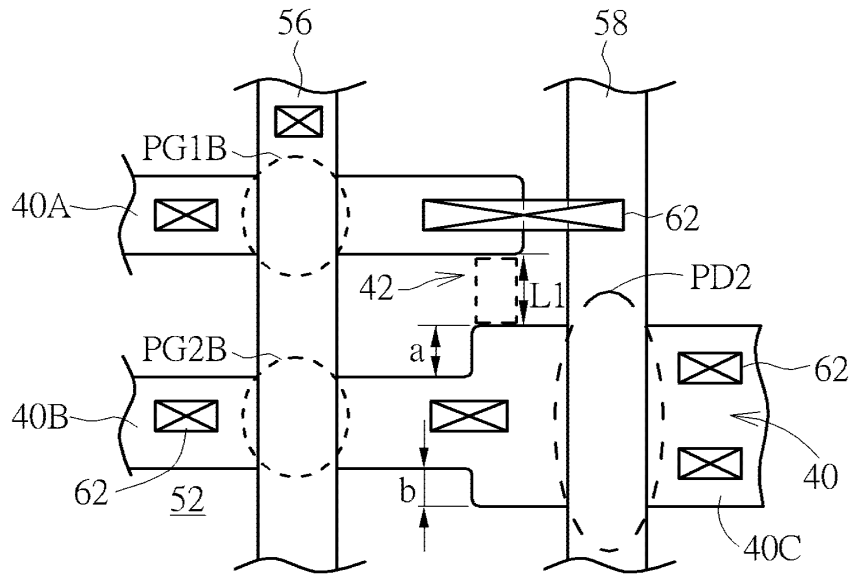


FIG. 3

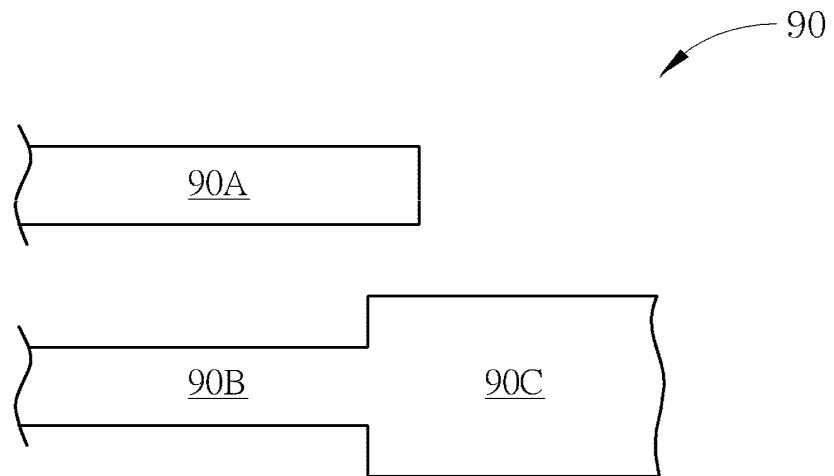


FIG. 4

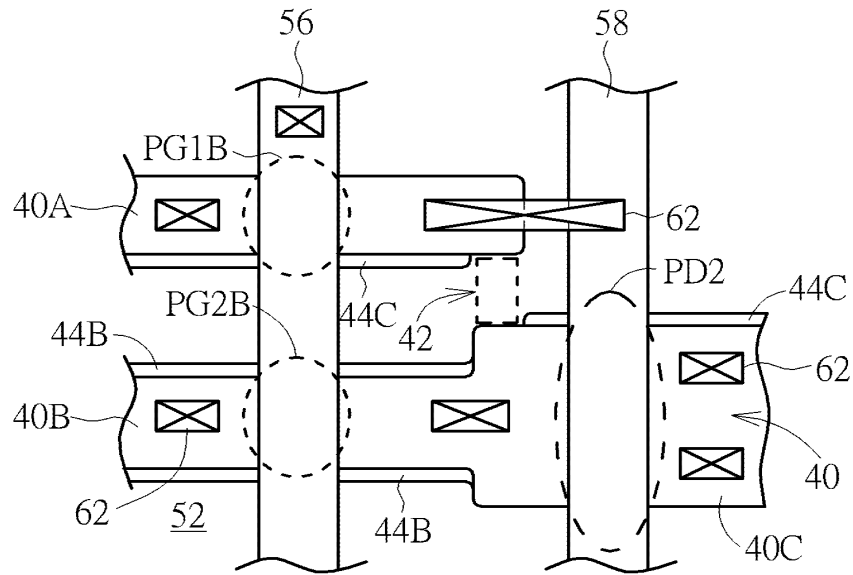


FIG. 5

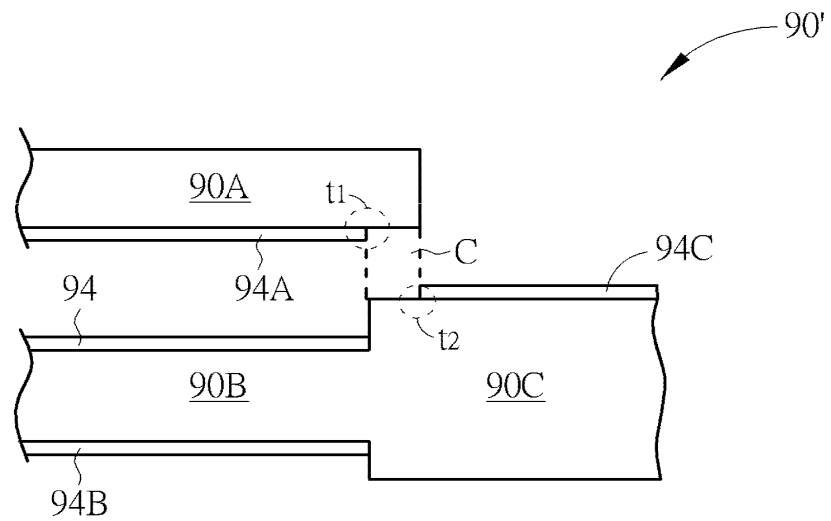


FIG. 6

Abstract of Disclosure

The present invention provides a layout pattern of an 8-transistor static random access memory (8T-SRAM), at least including a first diffusion region, a second diffusion region and a third diffusion region disposed on a substrate, a critical dimension region being disposed between the first diffusion region and the third diffusion region. The critical dimension region directly contacts the first diffusion region and the third diffusion region, a first extra diffusion region, a second extra diffusion region and a third extra diffusion region disposed surrounding and directly contacting the first diffusion region, the second diffusion region and the third diffusion region respectively. The first, the second and the third extra diffusion region are not disposed within the critical dimension region.

Claims

What is claimed is:

1. A layout pattern of an eight transistors static random access memory (8T-SRAM), comprising:

a first diffusion region, a second diffusion region and a third diffusion region disposed on a substrate, a critical dimension region being disposed between the first diffusion region and the third diffusion region, wherein the critical dimension region directly contacts the first diffusion region and the third diffusion region; and

a first extra diffusion region, a second extra diffusion region and a third extra diffusion region disposed surrounding and directly contacting the first diffusion region, the second diffusion region and the third diffusion region respectively, wherein the first, the second and the third extra diffusion region are not disposed within the critical dimension region.

2. The layout pattern of an 8T-SRAM of claim 1, wherein the 8T-SRAM includes a plurality of SRAM cells, each SRAM cell comprising:

a first pull-up transistor and a second pull-up transistor;
a first pull-down transistor and a second pull-down transistor;
a first up access transistor and a second up access transistor;
and

a first down access transistor and a second down access transistor.

3. The layout pattern of an 8T-SRAM of claim 2, wherein the first diffusion region corresponds to the first down access transistor, the second diffusion region corresponds to the second down access transistor, and the third diffusion region corresponds to the second pull-down transistor.

4. The layout pattern of an 8T-SRAM of claim 1, wherein the length of the critical dimension region is equal to or smaller than 54 nanometers (nm).

5. The layout pattern of an 8T-SRAM of claim 1, wherein the width of first extra diffusion region, the width of the second extra diffusion region and the width of the third extra diffusion region is between 5-10 nm.

6. The layout pattern of an 8T-SRAM of claim 1, further comprising at least two gate structures, wherein the first diffusion region, the second diffusion region and the third diffusion region are disposed on two sides of the two gate structures.

7. The layout pattern of an 8T-SRAM of claim 1, wherein the layout pattern is formed through a photomask, the pattern on the photomask comprising:

 a first pattern, a second pattern and a third pattern, corresponding to the first diffusion region, the second diffusion region and the third diffusion region respectively; and

 a plurality of extra patterns, including at least one first extra pattern, at least one second extra pattern and at least one third extra pattern, corresponding to the first extra diffusion region, the second extra diffusion region and the third extra diffusion region respectively.

8. The layout pattern of an 8T-SRAM of claim 7, wherein an L-shaped angle is disposed between the first extra pattern and the first pattern, and another L-shaped angle is disposed between the third extra pattern and the third pattern.

9. The layout pattern of an 8T-SRAM of claim 1, wherein the second diffusion region is shifted apart from the third diffusion region.

10. A method for forming a layout pattern of an eight transistors static random access memory (8T-SRAM), comprising:

 forming a first diffusion region, a second diffusion region and a third diffusion region disposed on a substrate, a critical dimension region being defined and disposed between the first diffusion region

and the third diffusion region, wherein the critical dimension region directly contacts the first diffusion region and the third diffusion region; and

forming a first extra diffusion region, a second extra diffusion region and a third extra diffusion region disposed surrounding and directly contacting the first diffusion region, the second diffusion region and the third diffusion region respectively, wherein the first, the second and the third extra diffusion region are not disposed within the critical dimension region.

11.The method of claim 10, wherein the 8T-SRAM includes a plurality of SRAM cells, each SRAM cell comprising:

- a first pull-up transistor and a second pull-up transistor;
- a first pull-down transistor and a second pull-down transistor;
- a first up access transistor and a second up access transistor;

and

- a first down access transistor and a second down access transistor.

12.The method of claim 11, wherein the first diffusion region corresponds to the first down access transistor, the second diffusion region corresponds to the second down access transistor, and the third diffusion region corresponds to the second pull-down transistor.

13.The method of claim 10, wherein the length of the critical dimension region is equal to or smaller than 54 nanometers (nm).

14. The method of claim 10, wherein the width of first extra diffusion region, the width of the second extra diffusion region and the width of the third extra diffusion region is between 5-10 nm.

15.The method of claim 10, further comprising forming at least two gate structures, wherein the first diffusion region, the second diffusion region and the third diffusion region are disposed on two sides of the two gate structures.

16. The method of claim 10, wherein the layout pattern is formed through a photomask, the pattern on the photomask comprising:

a first pattern, a second pattern and a third pattern, corresponding to the first diffusion region, the second diffusion region and the third diffusion region respectively; and

a plurality of extra patterns, including at least one first extra pattern, at least one second extra pattern and at least one third extra pattern, corresponding to the first extra diffusion region, the second extra diffusion region and the third extra diffusion region respectively.

17. The method of claim 16, wherein an L-shaped angle is disposed between the first extra pattern and the first pattern, and another L-shaped angle is disposed between the third extra pattern and the third pattern.

18. The method of claim 10, wherein the second diffusion region is shifted apart from the third diffusion region.

19. The method of claim 10, wherein the first diffusion region, the second diffusion region, the third diffusion region and the first extra diffusion region, the second extra diffusion region, and the third extra diffusion region are formed simultaneously.

Title

LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF

Background of the Invention

1. Field of the Invention

[0001] The invention relates to a static random access memory (SRAM), and more particularly, to a layout pattern of an 8 transistors SRAM (8T-SRAM).

2. Description of the Prior Art

[0002] An embedded static random access memory (SRAM) comprises a logic circuit and a static random access memory connected to the logic circuit. SRAM is a kind of volatile memory cell, which means it preserves data only while power is continuously applied. SRAM is built of cross-coupled inverters that store data during the time that power remains applied, unlike dynamic random access memory (DRAM) that needs to be periodically refreshed. Because of its high access speed, SRAM is also used in computer systems as a cache memory.

[0003] However, as pitch of the exposure process decreases, it has been difficult for the current SRAM architecture to produce desirable patterns. Hence, how to enhance the current SRAM architecture for improving exposure quality has become an important task in this field.

Summary of the Invention

[0004] The present invention provides a layout pattern of an 8-transistor static random access memory (8T-SRAM), at least comprising a first diffusion region, a second diffusion region and a third diffusion region disposed on a substrate, a critical dimension region being disposed between the first diffusion region and the third diffusion region, wherein the critical dimension region directly contacts the first diffusion region and the third diffusion region, a first extra diffusion region, a second extra diffusion region and a third extra diffusion region disposed surrounding and directly

contacting the first diffusion region, the second diffusion region and the third diffusion region respectively, wherein the first, the second and the third extra diffusion region are not disposed within the critical dimension region.

[0005] The present invention further provides a method for forming a layout pattern of an 8-transistor static random access memory (8T-SRAM), at least comprising: a first diffusion region, a second diffusion region and a third diffusion region are formed and disposed on a substrate, a critical dimension region being defined and disposed between the first diffusion region and the third diffusion region, wherein the critical dimension region directly contacts the first diffusion region and the third diffusion region, and a first extra diffusion region, a second extra diffusion region and a third extra diffusion region are formed, surrounding and directly contacting the first diffusion region, the second diffusion region and the third diffusion region respectively, wherein the first, the second and the third extra diffusion region are not disposed within the critical dimension region.

[0006] One preferred embodiment of the present invention further forms the extra diffusion regions surrounding each diffusion region, so the beta ratio can be increased, and thereby improve the performance of the 8T-SRAM, but the 8T-SRAM still maintains a good stability. In addition, each extra diffusion region will not disposed within the critical dimension region. Therefore, the extra diffusion regions will not influence the length or the width of the critical dimension region, thereby preventing the shorting issues.

[0007] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0008] Fig. 1 illustrates a layout diagram of a SRAM according to a first preferred embodiment of the present invention.

[0009] Fig. 2 illustrates a circuit diagram of an eight-transistor SRAM (8T-SRAM) cell of a SRAM of the present invention.

[0010] FIG.3 shows the partial enlarged diagram of FIG.1.

[0011] FIG.4 shows a photomask corresponds to the diffusion regions of FIG.3.

[0012] Fig. 5 illustrates a layout diagram of a SRAM according to a second preferred embodiment of the present invention.

[0013] FIG.6 shows a photomask corresponds to the diffusion regions of FIG.5.

Detailed Description

[0014] To provide a better understanding of the present invention to users skilled in the technology of the present invention, preferred embodiments are detailed as follows. The preferred embodiments of the present invention are illustrated in the accompanying drawings with numbered elements to clarify the contents and the effects to be achieved.

[0015] Please note that the figures are only for illustration and the figures may not be to scale. The scale may be further modified according to different design considerations. When referring to the words “up” or “down” that describe the relationship between components in the text, it is well known in the art and should be clearly understood that these words refer to relative positions that can be inverted to obtain a similar structure, and these structures should therefore not be precluded from the scope of the claims in the present invention.

[0016] Referring to FIGS. 1-2, FIG. 1 illustrates a layout diagram of a static random access memory (SRAM) according to a preferred embodiment of the present invention, and FIG. 2 illustrates a circuit diagram of an eight-transistor SRAM (8T-SRAM) cell of a SRAM of the present invention.

[0017] As shown in FIGS. 1-2, the SRAM device of the present invention preferably includes at least one SRAM cell, each SRAM cell including an eight-transistor SRAM (8T-SRAM) cell 10.

[0018] In this embodiment, each 8T-SRAM cell 10 is composed of a first pull-up transistor PL1, a second pull-up transistor PL2, a first pull-down transistor PD1, a second pull-down transistor PD2, a first up access transistor PG1A, a first down access transistor PG1B, a second up access transistor PG2A and a second down access transistor PG2B. These eight transistors constitute a set of flip-flops. The first and the second pull-up transistors PL1 and PL2, and the first and the second pull-down transistors PD1 and PD2 constitute a latch that stores data in the storage nodes 24 and 26. Since the first and the second pull-up transistors PL1 and PL2 act as power load devices, they can be replaced by resistors. Under this circumstance, the static random access memory becomes a four-transistor SRAM (4T-SRAM). In this embodiment, the first and the second pull-up transistors PL1 and PL2 preferably share a source/drain region and electrically connect to a voltage source Vcc, the first and the second pull-down transistors PD1 and PD2 share a source/drain region and electrically connect to a voltage source Vss.

[0019] Preferably, the first and the second pull-up transistors PL1 and PL2 of the 8T-SRAM cell 10 are composed of p-type metal oxide semiconductor (PMOS) transistors; the first and the second pull-down transistors PD1 and PD2, the first up and the second up access transistors PG1A and PG2A, and the first up and the second down access transistors PG1B and PG2B are composed of n-type metal oxide semiconductor (NMOS) transistors. The first pull-up transistor PL1 and the first pull-down transistor PD1 constitute an inverter, which further form a series circuit 28. One end of the series circuit 28 is connected to a voltage source Vcc and the other end of the series circuit 28 is connected to a voltage source Vss. Similarly, the second pull-up transistor PL2 and the second pull-down transistor PD2 constitute another inverter and a series circuit 30. One end of the

series circuit 30 is connected to the voltage source Vcc and the other end of the series circuit 30 is connected to the voltage source Vss.

[0020] The storage node 24 is connected to the respective gates G of the second pull-down transistor PD2 and the second pull-up transistor PL2. The storage node 24 is also connected to the drains D of the first pull-down transistor PD1, the first pull-up transistor PL1, the first up access transistor PG1A, and the first down access transistor PG1B. Similarly, the storage node 26 is connected to the respective gates G of the first pull-down transistor PD1 and first the pull-up transistor PL1. The storage node 26 is also connected to the drains D of the second pull-down transistor PD2, the second pull-up transistor PL2, the second up access transistor PG2A and the second down access transistor PG2B. The gates of the first up access transistor PG1A and the second up access transistor PG2A are respectively coupled to a first word line (WL1); the gates of the first down access transistor PG1B and the second down access transistor PG2B are respectively coupled to a second word line (WL2); the source S of the first up access transistor PG1A and the second up access transistor PG2A are respectively coupled to a first bit line (BL1); the source S of the first down access transistor PG1B and the second down access transistor PG2B are respectively coupled to a second bit line (BL2).

[0021] In this embodiment, the SRAM cell 10 is disposed on a substrate 52, such as a silicon substrate or silicon-on-insulator (SOI) substrate. The substrate may be a planar substrate, or a plurality of fin-shaped structures (not shown) may be formed on the substrate 52. Next, a plurality of gate structures 56 and 58 are formed on the substrate 52. In this embodiment, take a planar 8T-SRAM as an example. In other words, this embodiment does not include the fin-shaped structures, but the present invention is not limited thereto. In another case, the fin-shaped structures may also be comprised within the scope of the present invention.

[0022] Afterwards, an ion implantation process and an anneal process are performed in sequence, to form a plurality of diffusion regions 40 in the substrate 52 and surrounding each transistor (including the first pull-up transistor PL1, the second pull-up transistor PL2...), wherein the diffusion regions 40 are disposed on two sides of the gate structure 56, 58. The diffusion regions 40 mentioned above are used as the source/drain region of each transistor. Next, a plurality of contact plugs 62 are formed, wherein each contact plug 62 may be a single layer contact or a multiple layer contact, disposed on the diffusion region 40 (the source/drain region of each transistor), used as to electrically connect the voltage source Vcc, the voltage source Vss, the word lines WL1, WL2 or the bit lines BL1, BL2. In another case, the contact plug 62 may contact the source/drain region of the gate structure 56 and the gate structure 58 simultaneously, used as the share contact of the 8T-SRAM cell. In addition, the shallow trench isolation (STI, not shown) may be formed and surrounding each diffusion region 40. This is well known to those skilled in the art, and will not be described here.

[0023] In order to clearly describe the feature of the diffusion region of the present invention, FIG.3 shows the partial enlarged diagram of FIG.1. FIG.4 shows a photomask corresponds to the diffusion regions of FIG.3. It is noteworthy that the diffusion regions and partial gate structures compose the active area, and other regions are STI. The photomask shown in FIG.4 is the masks covering the active area, and STI is then formed in the substrate and out of the active area. Please refer to FIG.3, the first down access transistor PG1B, the second down access transistor PG2B and the second pull-down transistor PD2 of the 8T-SRAM are shown in FIG.3. The diffusion region that surrounds the first down access transistor PG1B is defined as the first diffusion region 40A; the diffusion region that surrounds the second down access transistor PG2B is defined as the second diffusion region 40B, the diffusion region that surrounds the second pull-down transistor PD2 is defined as the third diffusion region 40C, and the region having minimum spaces that are disposed between every two

adjacent and separated apart diffusion regions is defined as the critical dimension region 42. For example, the first diffusion region 40A and the third diffusion region 40C do not contact each other, therefore, the region that disposed between first diffusion region 40A and the third diffusion region 40C and with the minimum spaces is defined as the critical dimension region 42. The first to the third diffusion regions mentioned above are used as the source/drain regions of the first down access transistor PG1B, the second down access transistor PG2B and the second pull-down transistor PD2 respectively, and all of them are composed of n-type metal oxide semiconductor (NMOS) transistors, so they can be formed simultaneously, but not limited thereto. Afterwards, please refer to FIG.4, the photomask 90 at least includes a plurality of first patterns 90A (only shown one in FIG.4) corresponds to the first diffusion region 40A; a plurality of second patterns 90B (only shown one in FIG.4) corresponds to the second diffusion region 40B; a plurality of third patterns 90C (only shown one in FIG.4) corresponds to the third diffusion region 40C. It can be understood that there are only parts of the photomask patterns shown in FIG.4, so the actual photomask should include more patterns than FIG.4 shows, and correspond to each diffusion region shown in FIG.1.

[0024] With the miniaturization of components, the spacing between elements is also decreased. However, while forming the diffusion regions 40A-40C, different diffusion regions cannot contact each other (for example, the first diffusion region 40A cannot contact the second diffusion region 40B or the third diffusion region 40C), so as to prevent the shorting issue. In the present invention, applicant's experiment found that the critical dimension during the lithography step is about 54nm. In other words, during the step for forming the STI, a plurality of hard masks are formed and cover the active areas, and the minimum distance between every two adjacent hard masks is about 54nm. Please refer to FIG.3. The length L1 of the critical dimension region 42 should be larger than or equal to 54nm. When the condition is satisfied, the spaces between each the

diffusion region 40 can be decreased, but different diffusion regions 40 are still separated and will not contact each other, so as to prevent the shoring issue of the 8T-SRAM. In addition, in one layout pattern of the present invention, the second diffusion region 40B is shifted from the third diffusion region 40C. In other words, the length a and the length b shown in FIG.3 are different. It can be understood that the layout pattern of the present invention is not limited to the patterns shown in FIG.3, and can be adjusted according to actual requirements.

[0025] The following description will detail the different embodiments of the SRAM of the present invention. To simplify the description, the following description will detail the dissimilarities among the different embodiments and the identical features will not be redundantly described. In order to compare the differences between the embodiments easily, the identical components in each of the following embodiments are marked with identical symbols.

[0026] In 8T-SRAM, the beta ratio (β ratio) will influence the performance and the stability of the 8T-SRAM, wherein the beta ratio is equal to the ratio of the passing current of the pull down transistor (such as PD2) to the passing current of the access transistor (such as PG2B). Generally, the beta ratio balances performance and stability. One purpose of the present invention is to increase the beta ratio and to improve the performance of an 8T-SRAM, but still maintain good stability.

[0027] Fig. 5 illustrates a layout diagram of a SRAM according to a second preferred embodiment of the present invention. Please refer to FIG.5, the difference between this embodiment and the first preferred embodiment is further forming a plurality of extra diffusion regions 44 surrounding the first diffusion region 40A, the second diffusion region 40B and the third diffusion region 40C mentioned above. The extra diffusion regions 44 include at least one extra

diffusion region 44A, at least one extra diffusion region 44B and at least one extra diffusion region 44C, wherein the extra diffusion region 44A directly contacts the first diffusion region 40A; the extra diffusion region 44B directly contacts the second diffusion region 40B; and the extra diffusion region 44C directly contacts the third diffusion region 40C. Preferably, each extra diffusion region 44 and the first, the second and the third diffusion regions can be formed simultaneously. In other words, the extra diffusion regions 44 can be deemed as the extending portions of the first diffusion region 40A, the second diffusion region 40B and the third diffusion region 40C. In this embodiment, the width of each extra diffusion region 44 is about 5-10 nm, and it may slightly increase the area of the diffusion region. According to the applicant's experiment, the beta ratio can be increased while the area of the diffusion region is increased. For example, in this embodiment, without forming the diffusion region 44, the beta ratio is about 1.80-1.90, and after the diffusion regions 44 are formed, the beta ratio is increased to about 1.90-2.06, and the entire performance of 8T-SRAM also improves about 3%.

[0028] It can be understood that even though the extra diffusion regions 44 are only disposed surrounding the first diffusion region 40A, the second diffusion region 40B and the third diffusion region 40C in FIG.5, the extra diffusion region of the present invention can further be disposed surrounding the diffusion regions of other transistors, such as the diffusion region 40 shown in FIG.1. Besides, the diffusion regions 44 still satisfy the condition that they are not disposed within the critical dimension region 42, so as to prevent the shorting issue of the 8T-SRAM.

[0029] In order to prevent the shorting issue after further forming the extra diffusion regions 44, the extra diffusion regions 44 of the present invention will not be disposed within the critical dimension region 42. Therefore, the extra diffusion regions 44 will not influence the length or the width of the critical dimension region

42, and the length (or the width) of the critical dimension region 42 is still maintained in minimum spaces during the lithography step, thereby preventing the shorting issues.

[0030] Besides, the first diffusion region 40A, the second diffusion region 40B, the third diffusion region 40C and the extra diffusion regions 44 are preferably formed through a photomask. Please refer to FIG.6, which shows a partial photomask used for forming each diffusion region. The photomask 90' includes a plurality of first patterns 90A corresponding to the first diffusion regions 40A; a plurality of second patterns 90B corresponding to the second diffusion regions 40B; a plurality of third patterns 90C corresponding to the third diffusion regions 40C; and a plurality of extra patterns 94, including the extra patterns 94A, 94B and 94C, respectively correspond to the extra diffusion regions 44A-44C mentioned above. In addition, the photomask may further comprise other patterns (not shown), corresponding to the diffusion regions of other transistors shown in FIG.1. Preferably, each extra pattern 94 is a stripe-shaped structure, disposed surrounding the first pattern 90A, the second pattern 90B and the third pattern 90C, but not disposed within the region that corresponds to the critical dimension region 42 (such as the region C shown in FIG.6). In this embodiment, an L-shaped angle t1 is disposed between the first pattern 90A and the extra pattern 94A, another L-shaped angle t2 is disposed between the third pattern 90C and the extra pattern 94C, and the region C is disposed between the L-shaped angle t1 and the L-shaped angle t2.

[0031] Compared with the first preferred embodiment, the second preferred embodiment further forms the extra diffusion regions surrounding each diffusion region, so the beta ratio can be increased, and thereby improves the performance of the 8T-SRAM, but the 8T-SRAM still maintains a good stability. In addition, each extra diffusion region will not be disposed within the critical dimension region. Therefore, the extra diffusion regions will not influence the length or the width of the critical dimension region, thereby preventing

the shorting issues.

[0032] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		
First Named Inventor/Applicant Name:		Tien-Yu Lu		
Filer:		Winston Hsu/Hitomi Lin		
Attorney Docket Number:		NAUP2505USA		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
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Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
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Application Number:	14792636
International Application Number:	
Confirmation Number:	6268
Title of Invention:	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Tien-Yu Lu
Customer Number:	27765
Filer:	Winston Hsu/Kate Yeh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP2505USA
Receipt Date:	07-JUL-2015
Filing Date:	
Time Stamp:	06:17:25
Application Type:	Utility under 35 USC 111(a)

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RAM confirmation Number	8736
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2295934.PDF	1671289	no	8
			2381ea071e5a7921c569b2b4a8092ac8997e2cd4		
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2295908.PDF	26661	no	3
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5	Power of Attorney	2295903.pdf	330761	no	2
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Warnings:					
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6	Drawings-only black and white line drawings	2295689.PDF	62012	no	4
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Warnings:					
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7	Abstract	2295688.PDF	25068	no	1
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Warnings:					
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8	Claims	2295687.PDF	32365	no	4
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Warnings:					
Information:					
9	Specification	2295686.PDF	76583	no	11
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Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	35082	no	2
			f88d7c7a9d16516f95fe910a79ebbe06b0a5d89e		
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP2505USA
		Application Number	
Title of Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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Inventor Information:

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Legal Name					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP2505USA
		Application Number	
Title of Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		

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For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence information of this application.

Customer Number	27765		
Email Address	winstonhsu@naipo.com	Add Email	Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP2505USA
		Application Number	
Title of Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		

Application Information:

Title of the Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		
Attorney Docket Number	NAUP2505USA	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	4	Suggested Figure for Publication (if any)	

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For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country of origin

Publication Information:

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP2505USA
		Application Number	
Title of Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		

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Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
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201510336560.9	CN	2015-06-17	
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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP2505USA
		Application Number	
Title of Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		

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In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

☒ Assignee
 ☐ Legal Representative under 35 U.S.C. 117
 ☐ Joint Inventor

☐ Person to whom the inventor is obligated to assign.
 ☐ Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name

UNITED MICROELECTRONICS CORP.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP2505USA
		Application Number	
Title of Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		

Mailing Address Information:			
Address 1	No.3, Li-Hsin Road 2,		
Address 2	Science-Based Industrial Park		
City	Hsin-Chu City	State/Province	
Country i	TW	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button. Add			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
Remove				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add				

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP2505USA
		Application Number	
Title of Invention	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Winston Hsu/			Date (YYYY-MM-DD)	2015-07-06
First Name	Winston	Last Name	Hsu	Registration Number	41526
Additional Signature may be generated within this form by selecting the Add button.					Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/792,636	07/07/2015	2812	1600	NAUP2505USA	19	2

CONFIRMATION NO. 6268

FILING RECEIPT

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116



0000000076378478

Date Mailed: 07/21/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Tien-Yu Lu, Taichung City, TAIWAN;
Chang-Hung Chen, Tainan City, TAIWAN;
Yu-Tse Kuo, Tainan City, TAIWAN;
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Applicant(s)

UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

CHINA 201510336560.9 06/17/2015

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 07/20/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/792,636**

Projected Publication Date: 12/22/2016

Non-Publication Request: No

Early Publication Request: No
Title

LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/792,636	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	19	minus 20 = *				x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



证 明

本证明之附件是向本局提交的下列专利申请文件副本。

申 请 号：201510336560.9

申 请 类 型：发明专利

发 明 创 造 名 称：八晶体管静态随机存取存储器的布局图案与形成方
法

申 请 日：2015 年 06 月 17 日

申 请 人：联华电子股份有限公司

发明人或设计人：吕添裕、陈昌宏、郭有策、黄俊宪

局长

申长雨

2016 年 02 月 29 日



PYJ10374

权 利 要 求 书

1. 一种八晶体管静态随机存取存储器的布局图案, 包含:

5 第一扩散区、第二扩散区以及第三扩散区, 位于一基底上, 其中该第三扩散区与该第一扩散区之间存在有一极限间距区, 且该极限间距区直接接触该第一扩散区与该第三扩散区; 以及

10 第一增设扩散区、第二增设扩散区与第三增设扩散区, 分别沿着该第一扩散区、该第二扩散区与该第三扩散区的外围排列, 并分别直接接触该第一扩散区、该第二扩散区与该第三扩散区, 其中该增设扩散区不位于该极限间距区的范围内。

2. 如权利要求 1 所述的布局图案, 其中该八晶体管静态随机存取存储器包含多个静态随机存取存储器单元, 每一个静态随机存取存储器单元包含:

15 第一上拉晶体管以及第二上拉晶体管;
第一下拉晶体管以及第二下拉晶体管;
第一上存取晶体管以及第二上存取晶体管; 以及
第一下存取晶体管以及第二下存取晶体管。

3. 如权利要求 2 所述的布局图案, 其中该第一扩散区对应至该第一下存取晶体管, 该第二扩散区对应至该第二下存取晶体管, 而该第三扩散区则对应该第二下拉晶体管。

20 4. 如权利要求 1 所述的布局图案, 其中该极限间距区的长度小于或等于 54 纳米。

5. 如权利要求 1 所述的布局图案, 其中该第一增设扩散区、该第二增设扩散区与该第三增设扩散区的宽度介于 5~10 纳米。

25 6. 如权利要求 1 所述的布局图案, 还包含至少两栅极结构, 其中该第一扩散区、该第二扩散区与该第三扩散区位于该两栅极结构的两侧。

7. 如权利要求 1 所述的布局图案, 其中该布局图案由一光掩模形成, 该光掩模上的图案包含:

30 第一图案、第二图案、第三图案, 分别对应到该第一扩散区、该第二扩散区以及该第三扩散区; 以及

多个增设图案, 分别对应该第一增设扩散区、该第二增设扩散区与该第三增设扩散区。



8. 如权利要求 7 所述的布局图案,其中该第一增设图案与该第一图案之间具有至少一 L 型夹角,该第三增设图案与该第三图案之间具有至少一 L 型夹角。

5 9. 如权利要求 1 所述的布局图案,其中该第二扩散区与该第三扩散区之间有一错位。

10. 一种八晶体管静态随机存取存储器(8T-SRAM)的布局图案的形成方法,包含:

10 形成一第一扩散区、一第二扩散区以及一第三扩散区于一基底上,其中该第三扩散区与该第一扩散区之间存在有一极限间距区,且该极限间距区直接接触该第一扩散区与该第三扩散区;以及

形成一第一增设扩散区、一第二增设扩散区与一第三增设扩散区,分别沿着该第一扩散区、该第二扩散区与该第三扩散区的外围排列,并分别直接接触该第一扩散区、该第二扩散区与该第三扩散区,其中该增设扩散区不位于该极限间距区的范围内。

15 11. 如权利要求 10 所述的形成方法,其中该八晶体管静态随机存取存储器包含多个静态随机存取存储器单元,每一个静态随机存取存储器单元包含:

第一上拉晶体管以及第二上拉晶体管;

第一下拉晶体管以及第二下拉晶体管;

20 第一上存取晶体管以及一第二上存取晶体管;以及
第一下存取晶体管以及第二下存取晶体管。

12. 如权利要求 11 所述的形成方法,其中该第一扩散区对应至该第一下存取晶体管,该第二扩散区对应至该第二下存取晶体管,而该第三扩散区则对应该第二下拉晶体管。

25 13.如权利要求 10 所述的形成方法,其中该极限间距区的长度小于或等于 54 纳米。

14. 如权利要求 10 所述的形成方法,其中该第一增设扩散区、该第二增设扩散区与该第三增设扩散区的宽度介于 5~10 纳米。

30 15. 如权利要求 10 所述的形成方法,还包含形成至少两栅极结构,其中该第一扩散区、该第二扩散区与该第三扩散区位于该两栅极结构的两侧。

16. 如权利要求 10 所述的形成方法,其中该布局图案由一光掩模形成,



该光掩模上的图案包含:

第一图案、第二图案、第三图案,分别对应到该第一扩散区、该第二扩散区以及该第三扩散区;以及

5 多个增设图案,分别对应该第一增设扩散区、该第二增设扩散区与该第三增设扩散区。

17. 如权利要求 16 所述的形成方法,其中该第一增设图案与该第一图案之间具有至少一 L 型夹角,该第三增设图案与该第三图案之间具有至少一 L 型夹角。

10 18. 如权利要求 10 所述的形成方法,其中该第二扩散区与该第三扩散区之间有一错位。

19. 如权利要求 10 所述的形成方法,其中该第一扩散区、该第二扩散区、该第三扩散区与该增设扩散区同时形成。



PYJ10374

说明书

八晶体管静态随机存取存储器 的布局图案与形成方法

5

技术领域

本发明涉及一种静态随机存取存储器(static random access memory, SRAM), 尤其是一种八晶体管静态随机存取存储器(8T-SRAM)的布局图案。

10

背景技术

在一嵌入式静态随机存取存储器(embedded static random access memory, embedded SRAM)中, 包含有逻辑电路(logic circuit)和与逻辑电路连接的静态随机存取存储器。静态随机存取存储器本身属于一种挥发性(volatile)的存储单元(memory cell), 亦即当供给静态随机存取存储器的电力消失之后, 所存储的数据会同时抹除。静态随机存取存储器存储数据的方式是利用存储单元内晶体管的导电状态来达成, 静态随机存取存储器的设计是采用互耦合晶体管为基础, 没有电容器放电的问题, 不需要不断充电以保持数据不流失, 也就是不需作存储器更新的动作, 这与同属挥发性存储器的动态随机存取存储器(Dynamic Random Access Memory, DRAM)利用电容器带电状态存储数据的方式并不相同。静态随机存取存储器的存取速度相当快, 因此有在电脑系统中当作快取存储器(cache memory)等的应用。

然而随着制作工艺线宽与曝光间距的缩减, 现今 SRAM 元件的制作难以利用现有的架构曝出所要的图案。因此如何改良现有 SRAM 元件的架构来提升曝光的品质即为现今一重要课题。

25

发明内容

本发明提供一种八晶体管静态随机存取存储器(8T-SRAM)的布局图案, 包含一第一扩散区、一第二扩散区以及一第三扩散区位于一基底上, 其中该第三扩散区与该第一扩散区之间存在有一极限间距区, 且该极限间距区直接接触该第一扩散区与该第三扩散区, 以及一第一增设扩散区、一第二增设扩散区与一第三增设扩散区, 分别沿着该第一扩散区、该第二扩散区与该第三



扩散区的外围排列，并分别直接接触该第一扩散区、该第二扩散区与该第三扩散区，其中该增设扩散区不位于该极限间距区的范围内。

本发明另提供一种八晶体管静态随机存取存储器(8T-SRAM)的布局图案的形成方法，包含：形成一第一扩散区、一第二扩散区以及一第三扩散区于基底上，其中该第三扩散区与该第一扩散区之间存在有一极限间距区，且该极限间距区直接接触该第一扩散区与该第三扩散区，以及形成一第一增设扩散区、一第二增设扩散区与一第三增设扩散区，分别沿着该第一扩散区、该第二扩散区与该第三扩散区的外围排列，并分别直接接触该第一扩散区、该第二扩散区与该第三扩散区，其中该增设扩散区不位于该极限间距区的范围内。

本发明的一实施例中，由于额外形成增设扩散区在原先的扩散区外围，因此可以提高贝塔值，进而提升 8T-SRAM 的效能，但仍可控制 8T-SRAM 的稳定度在一定范围。此外增设扩散区并不会形成在原先各扩散区之间的极限间距区内，因此不易因为形成增设扩散区而造成短路现象。

附图说明

图 1 为本发明优选实施例的一静态随机存取存储器的布局图；

图 2 为本发明静态随机存取存储器中一组八晶体管静态随机存取存储器(eight-transistor SRAM, 8T-SRAM)存储单元的电路图；

图 3 为图 1 的局部放大图；

图 4 为一光掩模对应图 3 的扩散区的示意图；

图 5 为部分的本发明第二实施例中静态随机存取存储器布局图；

图 6 为一光掩模对应图 5 的扩散区的示意图。

主要元件符号说明

PL1 第一上拉晶体管

PL2 第二上拉晶体管

PD1 第一下拉晶体管

PD2 第二下拉晶体管

PG1A 第一上存取晶体管

PG1B 第一下存取晶体管

PG2A 第二上存取晶体管



	PG2B 第二下存取晶体管
	WL 字符线
	BL 位线
	Vcc 电压源
5	Vss 电压源
	10 八晶体管静态随机存取存储器
	24 存储节点
	26 存储节点
	28 串接电路
10	30 串接电路
	40 扩散区
	40A 第一扩散区
	40B 第二扩散区
	40C 第三扩散区
15	42 极限间距区
	44 增设扩散区
	44A 第一增设扩散区
	44B 第二增设扩散区
	44C 第三增设扩散区
20	52 基底
	56 栅极结构
	58 栅极结构
	62 接触结构
	90 光掩模
25	90' 光掩模
	90A 第一图案
	90B 第二图案
	90C 第三图案
	94 增设图案
30	94A 第一增设图案
	94B 第二增设图案



94C 第三增设图案

L1 长度

t1 夹角

t2 夹角

5 a 长度

b 长度

C 区域

具体实施方式

10 为使熟悉本发明所属技术领域的一般技术者能更进一步了解本发明，下文特列举本发明的优选实施例，并配合所附的附图，详细说明本发明的构成内容及所欲达成的功效。

为了方便说明，本发明的各附图仅为示意以更容易了解本发明，其详细的比例可依照设计的需求进行调整。在文中所描述对于图形中相对元件的上下关系，在本领域的人都应能理解其是指物件的相对位置而言，因此都可以
15 翻转而呈现相同的构件，此都应同属本说明书所揭露的范围，在此容先叙明。

请参照图 1 与图 2，图 1 为本发明优选实施例的一静态随机存取存储器的布局图，图 2 为本发明静态随机存取存储器中一组八晶体管静态随机存取存储器(eight-transistor SRAM, 8T-SRAM)存储单元的电路图。

20 如图 1 与图 2 所示，本发明的静态随机存取存储器优选包含至少一组静态随机存取存储器单元，其中每一静态随机存取存储器单元包含一八晶体管静态随机存取存储单元(eight-transistor SRAM, 8T-SRAM)10。

在本实施例中，各 8T-SRAM 存储单元 10 优选由一第一上拉晶体管 (Pull-Up transistor)PL1、一第二上拉晶体管 PL2、一第一下拉晶体管 (Pull-Down transistor)PD1、一第二下拉晶体管 PD2、一第一上存取晶体管 (Access transistor)PG1A、一第一下存取晶体管 PG1B、一第二上存取晶体管 PG2A 以及一第二下存取晶体管 PG2B 构成正反器(flip-flop)，其中第一上拉晶体管 PL1 和第二上拉晶体管 PL2、第一下拉晶体管 PD1 和第二下拉晶体管 PD2 构成栓锁电路(latch)，使数据可以栓锁在存储节点(Storage Node)
25 或 26。另外，第一上拉晶体管 PL1 和第二上拉晶体管 PL2 是作为主动负载之用，其亦可以一般的电阻来取代做为上拉元件，在此情况下即为四晶体管
30



静态随机存取存储器(four-transistor SRAM, 4T-SRAM)。另外在本实施例中，第一上拉晶体管 PL1 和第二上拉晶体管 PL2 各自的一源极区域电连接至一电压源 Vcc，第一下拉晶体管 PD1 和第二下拉晶体管 PD2 各自的一源极区域电连接至一电压源 Vss。

5 一般而言，8T-SRAM 存储单元 10 的第一上拉晶体管 PL1、第二上拉晶体管 PL2 是由 P 型金属氧化物半导体(P-type metal oxide semiconductor, PMOS)晶体管所组成，而第一下拉晶体管 PD1、第二下拉晶体管 PD2 和第一上存取晶体管 PG1A、第一下存取晶体管 PG1B、第二上存取晶体管 PG2A、
10 第二下存取晶体管 PG2B 则是由 N 型金属氧化物半导体(N-type metal oxide semiconductor, NMOS)晶体管所组成。其中，第一上拉晶体管 PL1 和第一下拉晶体管 PD1 一同构成一反向器(inverter)，且这两者所构成的串接电路 28 其两端点分别耦接于一电压源 Vcc 与一电压源 Vss；同样地，第二上拉晶体管 PL2 与第二下拉晶体管 PD2 构成另一反向器，而这两者所构成的串接电路 30 其两端点也分别耦接于电压源 Vcc 与电压源 Vss。

15 此外，在存储节点 24 处，分别电连接有第二下拉晶体管 PD2 和第二上拉晶体管 PL2 的栅极(gate)G、及第一下拉晶体管 PD1、第一上拉晶体管 PL1 和第一上存取晶体管 PG1A 与第一下存取晶体管 PG1B 的漏极(Drain)D；同样地，在存储节点 26 上，也分别电连接有第一下拉晶体管 PD1 和第一上拉晶体管 PL1 的栅极 G、及第二下拉晶体管 PD2、第二上拉晶体管 PL2 和
20 第二上存取晶体管 PG2A 与第二下存取晶体管 PG2B 的漏极 D。至于第一上存取晶体管 PG1A 和第二上存取晶体管 PG2A 的栅极 G 则耦接至第一字符线(Word Line)WL1；第一下存取晶体管 PG1B 和第二下存取晶体管 PG2B 的栅极 G 则耦接至第二字符线 WL2，而第一上存取晶体管 PG1A 和第二上存取晶体管 PG2A 的源极(Source)S 耦接至相对应的第一位线(Bit Line)BL1；
25 第一下存取晶体管 PG1B 和第二下存取晶体管 PG2B 的源极 S 则耦接至相对应的第二位线 BL2。

在本实施例中，8T-SRAM 存储单元 10 设于一基底 52 上，例如一硅基底或硅覆绝缘(SOI)基板，基底 52 可为一平面结构，或是选择性设置有多个鳍状结构(图未示)，以及多个栅极结构 56、58 位于基底 52 上。本实施例中
30 以平面式 8T-SRAM 存储单元为例说明，代表不需形成鳍状结构于基底 52 上，但在本发明的其他实施例中，可形成鳍状结构于基底上，也属于本发明



的涵盖范围。

接着，在各预定形成的晶体管(包含上述的第一上拉晶体管 PL1、第二上拉晶体管 PL2 等...)的栅极结构周围，依序进行一离子掺杂步骤以及一加热步骤，形成多个扩散区 40 于基底 52 中，并且位于各个栅极结构 56、58 的
5 两侧。上述的扩散区 40 作为各晶体管结构的源/漏极使用。之后，再形成多个接触结构 62，其中接触结构 62 可能为单层接触结构或是多层接触结构，位于各扩散区 40(源/漏极)上，用以在后续步骤中电连接电压源 Vcc、电压源 Vss、字符线 WL1、WL2 或是位线 BL1、BL2 等，或着接触结构 62 可能同时接触栅极结构 56、58 以及各晶体管结构的源/漏极，当作 8T-SRAM 存储
10 单元的共用接触(share contact)使用。此外，各扩散区 40 周围设有浅沟隔离(图未示)。上述技术属于本领域的常见技术，在此不另外多加赘述。

为了更清楚说明本发明扩散区的特征，图 3 为图 1 的局部放大图。图 4 则绘示一光掩模对应图 3 的扩散区。值得注意的是，图 3 中的扩散区与部分栅极结构构成主动区(active area)，而其他的区域都为浅沟隔离。而图 4 上所
15 绘示的光掩模图案，用来形成覆盖于主动区上的掩模，而掩模外则形成浅沟隔离。请参考图 3，8T-SRAM 存储单元的第一下存取晶体管 PG1B、第二下存取晶体管 PG2B 与第二下拉晶体管 PD2 绘示于图 3 中。定义第一下存取晶体管 PG1B 周围的扩散区为第一扩散区 40A、第二下存取晶体管 PG2B 周围的扩散区定义为第二扩散区 40B、第二下拉晶体管 PD2 周围的扩散区则定义
20 为第三扩散区 40C，而任意两个不直接接触的扩散区之间，其最小间距处则定义为极限间距区(critical dimension region)42。举例来说，本实施例中第一扩散区 40A 与第三扩散区 40C 不直接接触，因此上述两者之间的具有最小间距的区域就定义为极限间距区 42。上述第一~第三扩散区用来当作第一下存取晶体管 PG1B、第二下存取晶体管 PG2B 与第二下拉晶体管 PD2 的源/
25 漏极，且都由 N 型金属氧化物半导体(NMOS)晶体管所组成，故优选可同时形成，但不限于此。接着请参考图 4，光掩模 90 上至少包含有多个第一图案 90A，(图中仅显示一个)对应上述的第一扩散区 40A；多个第二图案 90B(图中仅显示一个)，对应上述的第二扩散区 40B；多个第三图案 90C(图中仅显示一个)，对应上述的第三扩散区 40C。可理解的是，由于图 4 仅绘出部分光
30 掩模图案，因此光掩模上应包含更多图案，分别对应到图 1 中所绘示的各晶体管周围的扩散区。

值得注意的是,随着元件的微小化,各元件之间彼此的间距也随之减小。但是在形成上述扩散区 40A~40C 时,需避免特定扩散区彼此之间互相接触以造成短路问题(例如第一扩散区 40A 不可与第二扩散区 40B 或是第三扩散区 40C 接触)。申请人经实验之后,发现受光刻步骤中最小曝光间距(critical dimension)的限制之下,扩散区之间的最小间距约为 54 纳米。也就是说,在形成浅沟隔离的过程中,先形成多个掩模层覆盖住主动区,而该些掩模层彼此之间的最小间距约为 54 纳米。因此请参考图 3,极限间距区 42 长度 L1 需大于或是等于 54 纳米。当满足上述条件时,各扩散区 40 之间的间距可有效缩小,但是仍不会互相接触而造成 8T-SRAM 存储单元短路。另外,在本发明的其中一布局图案中,第二扩散区 40B 与第三扩散区 40C 之间有一错位,换句话说,图 3 上的长度 a 与长度 b 并不相等。可理解的是,本发明的布局图案不以图 3 上为限而可依照实际需求调整,以达到元件缩小化的目的。

下文将针对本发明的静态随机存取存储器的不同实施样态进行说明,且为简化说明,以下说明主要针对各实施例不同之处进行详述,而不再对相同之处作重复赘述。此外,本发明的各实施例中相同的元件是以相同的标号进行标示,以利于各实施例间互相对照。

在 8T-SRAM 中,贝塔值(beta ratio)将会影响 8T-SRAM 的效能与稳定度。其中贝塔值等于在 8T-SRAM 操作状态下,通过下拉晶体管(例如 PD2)的电流除以通过存取晶体管(例如 PG2B)的比值。一般来说,当贝塔值提高时,8T-SRAM 的效能(performance)将会随之提高,但是当贝塔值过高,又可能导致 8T-SRAM 的稳定度降低。因此,贝塔值应维持一相对稳定的范围内。本发明中,其中一目的是提高 8T-SRAM 的贝塔值以提升效能,却又不影响 8T-SRAM 的稳定度。

在本发明的第二实施例中,请参考图 5,其绘示部分的本发明第二实施例中静态随机存取存储器布局图。与本发明第一优选实施例不同之处在于,除了形成第一扩散区 40A、第二扩散区 40B 与第三扩散区 40C 之外,更在上述的各扩散区周围形成多个增设扩散区 44,分别定义为增设扩散区 44A、增设扩散区 44B 与增设扩散区 44C。其中增设扩散区 44A 与第一扩散区 40A 直接相连;增设扩散区 44B 与第二扩散区 40B 直接相连;增设扩散区 44C 与第三扩散区 40C 直接相连。且各增设扩散区 44 与上述的第一~第三扩散区优选同时制作,换句话说,增设扩散区 44 可视为第一扩散区 40A、第二



扩散区 40B 与第三扩散区 40C 的延伸。本实施例中，增设扩散区 44 的宽度大约介于 5~10 纳米之间，可稍微增加扩散区的面积。根据申请人的实验结果，增加扩散区的面积，对于贝塔值可达到提升的作用。以本实施例为例，未形成增设扩散区 44 时，贝塔值大约在 1.80~1.90 之间，而增加了增设扩散区 44 之后，贝塔值可提升至 1.90~2.06，而整体 8T-SRAM 的效能也可提升约 3%。

可理解的是，虽然图 5 仅针对第一扩散区 40A、第二扩散区 40B 与第三扩散区 40C 的周围形成增设扩散区 44。但是本发明的增设扩散区可以形成于其他晶体管的扩散区的周围，例如图 1 所示的各扩散区 40。但仍需满足增设扩散区 44 不设置于极限间距区的条件，以避免 8T-SRAM 造成短路问题。

值得注意的是，为了避免形成增设扩散区 44 后可能产生的短路问题，本发明的增设扩散区 44 并不会形成在极限间距区 42 内。如此一来，在极限间距区 42 两侧的扩散区，彼此之间的距离仍维持在制作工艺中可达到的最小间距，并不会因为形成增设扩散区 44 而产生短路问题。

除此之外，上述的第一扩散区 40A、第二扩散区 40B、第三扩散区 40C 与增设扩散区 44 优选由一光掩模所形成。可参考图 6，其绘示形成各扩散区的光掩模的局部图，光掩模 90' 上至少包含有多个第一图案 90A，对应上述的第一扩散区 40A；多个第二图案 90B，对应上述的第二扩散区 40B；多个第三图案 90C，对应上述的第三扩散区 40C；多个增设图案 94，包含增设图案 94A、94B 以及 94C，分别对应上述的增设扩散区 44A~44C。此外光掩模上可包含其他图案(图未示)，对应图 1 上的其他晶体管的扩散区。优选而言，增设图案 94 为长条形，设置在第一图案 90A、第二图案 90B 与第三图案 90C 的周围，但不位于光掩模图案上对应至极限间距区 42 的范围内(如图 6 上的区域 C)。以本发明为例，第一图案 90A 与增设图案 94A 之间具有一 L 型夹角 t_1 ，而第三图案 90C 与增设图案 94C 之间也具有一 L 型夹角 t_2 ，而区域 C 则位于 L 型夹角 t_1 与 L 型夹角 t_2 之间。

本发明的第二优选实施例，相较于第一优选实施例，由于额外形成增设扩散区在原先的扩散区外围，因此可以提高贝塔值，进而提升 8T-SRAM 的效能，但仍可控制 8T-SRAM 的稳定度在一定范围。此外增设扩散区并不会形成在原先各扩散区之间的极限间距区内，因此不易因为形成增设扩散区而造成短路现象。



以上所述仅为本发明的优选实施例，凡依本发明权利要求所做的均等变化与修饰，都应属本发明的涵盖范围。



PYJ10374

说明书附图

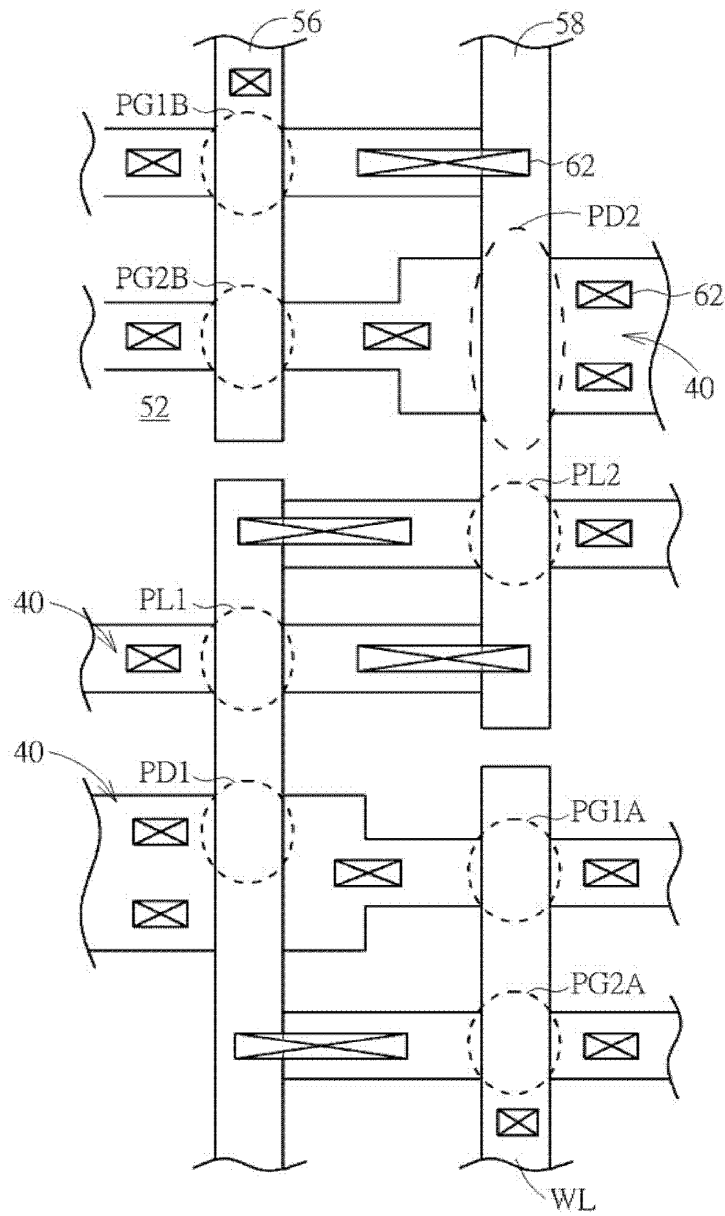


图 1

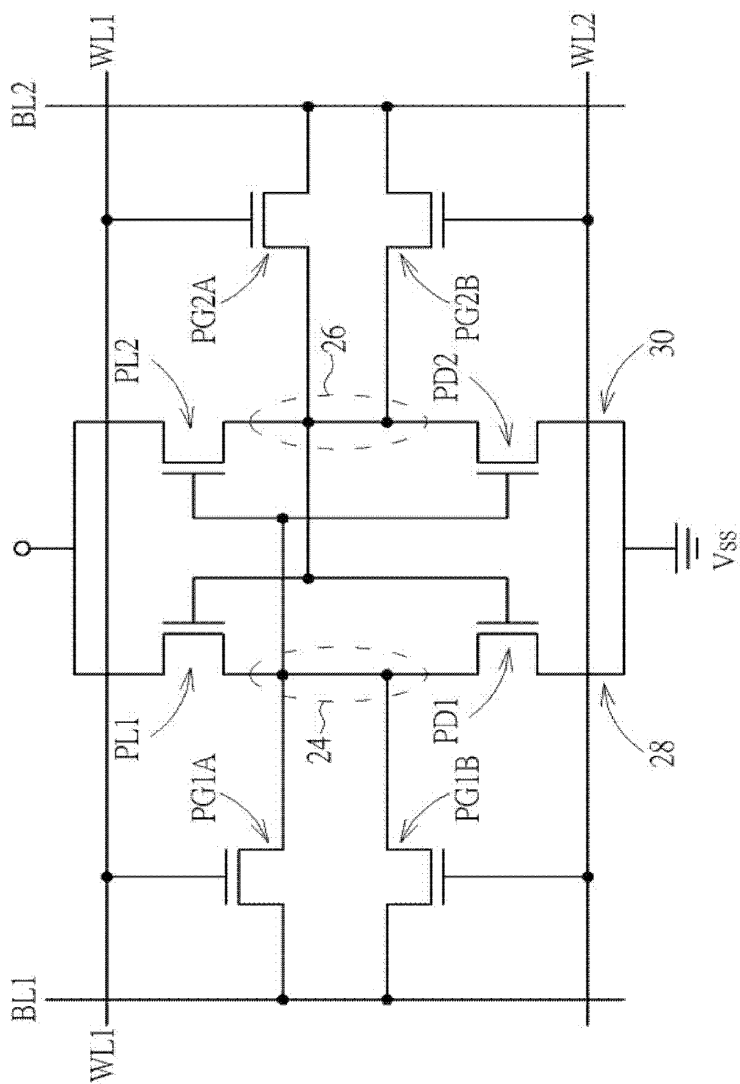
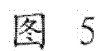


图 2

Diagram illustrating a multi-layered structure 90. The structure consists of three main layers: 90A (top), 90B (middle), and 90C (bottom). Layer 90B is wider than 90A and 90C, and its right side is irregular. Layer 90C is wider than 90A and 90B, and its right side is irregular. The layers are stacked vertically.

图 4





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NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 06/06/2016
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

NGUYEN, DAO H

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 06/06/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/792,636	07/07/2015	Tien-Yu Lu	NAUP2505USA	6268

TITLE OF INVENTION: LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	09/06/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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14/792,636 07/07/2015 Tien-Yu Lu NAUP2505USA 6268

TITLE OF INVENTION: LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional UNDISCOUNTED \$960 \$0 \$0 \$960 09/06/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, DAO H	2818	365-154000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

NGUYEN, DAO H

ART UNIT	PAPER NUMBER
----------	--------------

2818

DATE MAILED: 06/06/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/792,636	Applicant(s) LU ET AL.	
	Examiner DAO H. NGUYEN	Art Unit 2818	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 07/07/2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-19. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/bph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>07/07/2015</u> | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other ____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. | |

/DAO H NGUYEN/
Primary Examiner, Art Unit 2818

05/30/2016

DETAILED ACTION

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This Office Action is in response to the communications dated 07/07/2015.

Claims 1-19 are pending in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 07/07/2015. The references cited on the PTOL 1449 form have been considered.

Foreign Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Allowance / Reason for Allowance

4. **Claims 1-19 are allowed.**

The following is an examiner's statement of reason for allowance:

Claims 1-9: None of the references of record teaches or suggests the claimed layout pattern of an eight transistors static random access memory (8T-SRAM) (in combination(s) as set forth in the claim(s)) comprising:

a first, a second, and a third extra diffusion regions disposed surrounding and directly contacting the first, the second, and the third diffusion regions, respectively, wherein the first, the second and the third extra diffusion regions are not disposed within the critical dimension region.

Claims 10-19: None of the references of record teaches or suggests the claimed method for forming a layout pattern of an eight transistors static random access memory (8T-SRAM) (in combination(s) as set forth in the claim(s)) comprising:

forming a first, a second, and a third extra diffusion regions disposed surrounding and directly contacting the first, the second, and the third diffusion regions, respectively, wherein the first, the second and the third extra diffusion regions are not disposed within the critical dimension region.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke, can be reached on (571)272-1657. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1633.

/DAO H NGUYEN/
Primary Examiner, Art Unit 2818
May 30, 2016

Notice of References Cited	Application/Control No. 14/792,636	Applicant(s)/Patent Under Reexamination LU ET AL.	
	Examiner DAO H. NGUYEN	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2010/0103719 A1	04-2010	Lee; Cheng Hung	G11C11/412	365/154
*	B	US-7,952,912 B2	05-2011	Kulkarni; Jaydeep P.	G11C11/413	365/154
*	C	US-2007/0279965 A1	12-2007	Nakazato; Takaaki	G11C11/4125	365/154
*	D	US-2013/0154027 A1	06-2013	Liaw; Jhon-Jhy	H01L27/1104	257/390
*	E	US-2015/0302917 A1	10-2015	Grover; Anuj	G11C11/412	365/51
*	F	US-2011/0075470 A1	03-2011	LIAW; Jhon Jhy	G11C8/16	365/154
*	G	US-2013/0181297 A1	07-2013	Liaw; Jhon-Jhy	G11C11/412	257/390
*	H	US-2013/0141963 A1	06-2013	Liaw; Jhon-Jhy	G11C11/412	365/156
*	I	US-8,913,455 B1	12-2014	Camarota; Rafael C.	H01L21/8238	365/154
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	7059	((memory SRAM static near random near2 memory) and (pull near up near2 (transistor FET MOSFET TFT)) and (pull near down near2 (transistor FET MOSFET TFT)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:14
L11	7057	10 and (@ad<"201506017" @lad<"20150617")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:15
L12	2882	11 and (access\$3 trafer\$3 pass\$3) adj3 (transistor FET MOSFET FINFET TFT)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:18
L15	122	12 and (critical\$3 near (dimension size area region part portion space gap distance))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:31
L18	2769	12 and ((dimension size area region part portion space gap distance))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:32
L20	1286	18 and ((source darin source/drian) near5 (dimension size area region part portion space gap distance))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:32
L21	371	20 and (second another addition\$4) adj2 (pull near up near2 (transistor FET MOSFET TFT))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:35
L22	362	20 and (second another addition\$4) adj2 (pull near down near2 (transistor FET MOSFET TFT))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:35
L23	310	21 and 22	US-PGPUB; USPAT;	OR	ON	2016/05/30 11:35

			USOCR; FPRS; EPO; JPO; IBM_TDB			
L24	295	23 not 15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 11:36
L25	6	("2013/0154027").URPN.	USPAT	OR	ON	2016/05/30 11:40
L26	3	("2010/0103719").URPN.	USPAT	OR	ON	2016/05/30 11:46
S1	0	14/792636	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 18:30
S2	5248	257/369.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 19:13
S3	1624	H01L27/1108.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 19:14
S4	12764	H01L27/0207.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 19:14
S5	638	H01L29/0684.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 19:14
S6	0	Lu-Tien-Yu.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:05
S7	14	Chen-Chang-Hung.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:06
S8	4	Kuo-Yu-Tse.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2016/05/29 21:06

			JPO; IBM_TDB			
S9	69	Huang-Chun-Hsien.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:06
S10	87	S7 S8 S9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:06
S11	2	("6970373" "7994583").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:07
S12	798	((8T near (RAM SRAM)) (Eight near (transistor FET MOSFET FINFET TFT) near3 (RAM Memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:12
S13	0	S10 and S12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:12
S14	944	((8T near (RAM SRAM)) (Eight near (transistor FET MOSFET FINFET TFT) near5 (RAM Memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:12
S15	0	S10 and S14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:13
S16	7	S10 and (RAM SRAM memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:13
S17	0	United adj "Microelectronics." "as." and ((8T near (RAM SRAM)) (Eight near (transistor FET MOSFET FINFET TFT) near5 (RAM Memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:14
S18	2	United adj Microelectronics.as. and ((8T near (RAM SRAM)) (Eight near (transistor FET MOSFET FINFET TFT) near5 (RAM Memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2016/05/29 21:14

			JPO; IBM_TDB			
S19	0	("2014/0160840").URPN.	USPAT	OR	ON	2016/05/29 21:15
S20	3684	257/368.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:26
S21	6510	438/106.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:28
S22	4101	H01L27/1052.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:29
S23	2025	H01L29/42392.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 21:29
S24	4776	438/107.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:15
S25	0	G01C11/4125.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:23
S26	4682	365/154.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:24
S27	5499	365/203.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:24
S28	238	365/185.07.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:24
S29	946	365/189.14.ccls.	US-PGPUB; USPAT;	OR	ON	2016/05/29 22:24

			USOCR; FPRS; EPO; JPO; IBM_TDB			
S30	1410	257/e27.099.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:29
S31	5538	257/e27.112.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:29
S32	1903	257/e21.661.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:29
S33	3361	257/e27.06.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:36
S34	4950	H01L27/1104.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:36
S35	2751	257/e27.062.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:37
S36	6298	G11C11/412.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:41
S37	2333	H01L21/845.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:47
S38	2819	438/128.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:48
S39	2033	257/390.ccls.	US-PGPUB; USPAT;	OR	ON	2016/05/29 22:48

			USOCR; FPRS; EPO; JPO; IBM_TDB			
S40	1130	G11C11/4125.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/29 22:50
S41	6956	memory and (pull near up near2 (transistor FET MOSFET TFT)) and (pull near down near2 (transistor FET MOSFET TFT))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 00:23
S46	6956	memory and (pull near up near2 (transistor FET MOSFET TFT)) and (pull near down near2 (transistor FET MOSFET TFT))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2016/05/30 00:28

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1237	((memory SRAM static near random near2 memory) and (pull near up near2 (transistor FET MOSFET TFT)) and (pull near down near2 (transistor FET MOSFET TFT))).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 11:06
L3	9	1 and ((extra exten\$4) near2 (diffusion dop\$4 implantati\$3 implantati\$3)).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 11:07
L4	2	1 and (critical\$3 near (dimension size area region part portion space gap distance)).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 11:08
L5	560	1 and ((dimension size area region part portion space gap distance)).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 11:08
L6	23	5 and (layout lay near out).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 11:11
L8	195	5 and (source drain source/drain) with (well extension diffusi\$3)	US- PGPUB; USPAT	OR	ON	2016/05/30 11:13
L9	187	8 not (3 4 6)	US- PGPUB; USPAT	OR	ON	2016/05/30 11:13
L13	288	5 and ((access\$3 trafer\$3 pass\$3) adj3 (transistor FET MOSFET FINFET TFT)).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 11:18
L14	130	13 not (3 4 6 9)	US- PGPUB; USPAT	OR	ON	2016/05/30 11:18
L33	6	("2007/0279965").URPN.	USPAT	OR	ON	2016/05/30 11:49
L34	20	("20020071305" "20050276095"	US-	OR	ON	2016/05/30

		"20060102957" "20060175606" "20060212509" "20060227595" "20070035986" "20070165447" "20070201262" "20070236985" "20070279965" "4620297" "5796659" "6744661" "6775178" "6975532" "7050324" "7177177" "7328413" "7508697").PN. OR ("7952912").URPN.	US- PGPUB; USPAT			11:50
S42	62	((8T near3 (RAM SRAM)) (Eight near (transistor FET MOSFET FINFET TFT) near3 (RAM Memory))).clm.	US- PGPUB; USPAT	OR	ON	2016/05/29 21:21
S43	0	S42 and critical\$3 near2 region.clm.	US- PGPUB; USPAT	OR	ON	2016/05/29 21:21
S44	0	S42 and diffusion\$33 near2 region.clm.	US- PGPUB; USPAT	OR	ON	2016/05/29 21:22
S45	0	S42 and diffusion\$3.clm.	US- PGPUB; USPAT	OR	ON	2016/05/29 21:25
S47	1159	(memory and (pull near up near2 (transistor FET MOSFET TFT)) and (pull near down near2 (transistor FET MOSFET TFT))).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 00:28
S48	8	S47 and ((extra exten\$4) near2 (diffusion dop\$4)).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 00:29
S49	2	S47 and (critical\$3 near (dimension size area region part portion space gap distance)).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 00:32
S50	10	S47 and ((8T near3 (RAM SRAM)) (Eight near (transistor FET MOSFET FINFET TFT) near3 (RAM SRAM Memory))).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 00:34
S51	82	((8T near3 (RAM SRAM)) (Eight near (transistor FET MOSFET FINFET TFT) near3 (RAM SRAM Memory))).clm.	US- PGPUB; USPAT	OR	ON	2016/05/30 00:34
S52	72	S51 not (S48 S49 S50)	US- PGPUB; USPAT	OR	ON	2016/05/30 00:35

5/ 30/ 2016 11:54:10 AM

C:\Users\dnghuyen15\Documents\EAST\Workspaces\14792636.wsp

Issue Classification 	Application/Control No. 14792636	Applicant(s)/Patent Under Reexamination LU ET AL.	
	Examiner DAO H NGUYEN	Art Unit 2818	

CPC						
Symbol					Type	Version
H01L		27		1108	F	2013-01-01
H01L		27	/	0207	I	2013-01-01
H01L		29	/	0684	I	2013-01-01
G11C		11	/	412	I	2013-01-01
H01L		21	/	845	I	2013-01-01
H01L		27	/	1052	I	2013-01-01
H01L		29	/	42392	A	2013-01-01
G11C		11	/	4125	A	2013-01-01
H01L		27	/	1104	A	2013-01-01
			/			
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			/			
			/			
			/			
			/			

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/DAO H NGUYEN/ Primary Examiner.Art Unit 2818	05/30/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2 & 5

Issue Classification 	Application/Control No. 14792636	Applicant(s)/Patent Under Reexamination LU ET AL.
	Examiner DAO H NGUYEN	Art Unit 2818

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION									
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED				
365		154				G	1	1	C	11 / 00 (2006.0)					
CROSS REFERENCE(S)						H	0	1	L	27 / 088 (2006.0)					
						H	0	1	L	27 / 11 (2006.01.01)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)														
365	185.07	189.14	203												
257	368	369	390												
257	E27.06	E27.062	E27.099	E27.112	E21.661										
438	106	107	128												

NONE		Total Claims Allowed:	
		19	
(Assistant Examiner)	(Date)		
/DAO H NGUYEN/ Primary Examiner.Art Unit 2818	05/30/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2 & 5



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CONFIRMATION NO. 6268

SERIAL NUMBER 14/792,636	FILING or 371(c) DATE 07/07/2015 RULE	CLASS 257	GROUP ART UNIT 2818	ATTORNEY DOCKET NO. NAUP2505USA		
APPLICANTS UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN; INVENTORS Tien-Yu Lu, Taichung City, TAIWAN; Chang-Hung Chen, Tainan City, TAIWAN; Yu-Tse Kuo, Tainan City, TAIWAN; Chun-Hsien Huang, Tainan City, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** CHINA 201510336560.9 06/17/2015 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/20/2015						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/DAO H NGUYEN/</u> Examiner's Signature		☐ Met after Allowance DHN Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 4	TOTAL CLAIMS 19	INDEPENDENT CLAIMS 2
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 14792636	Applicant(s)/Patent Under Reexamination LU ET AL.
	Examiner DAO H NGUYEN	Art Unit 2818

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 11/412, 11/4125	05/30/2016	DHN
H01L 27/1108, 27/0207, 27/1052, 27/1104	05/30/2016	DHN
H01L 29/0684, 29/42392	05/30/2016	DHN
H01L 21/845	05/30/2016	DHN

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
365	154, 185.07, 189.14, 203	05/30/2016	DHN
257	368, 369, 390	05/30/2016	DHN
257	e27.06, e27.062, e27.099, e27.112	05/30/2016	DHN
257	e21.661	05/30/2016	DHN
438	106, 107, 128	05/30/2016	DHN

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (see attached search history)	05/30/2016	DHN

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	See attached search history	05/30/2016	DHN

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Tien-Yu Lu
	Art Unit	~~N/A~~
	Examiner Name	~~N/A~~ Dao Nguyen
	Attorney Docket Number	NAUP2505USA

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6970373		2005-11-29	Datta	
	2	7994583		2011-08-09	Inaba	

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS								
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.H.N./

Receipt date: 07/07/2015

14792636 - GAU: 2818

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Tien-Yu Lu
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP2505USA

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		
EXAMINER SIGNATURE			
Examiner Signature	/Dao H. Nguyen/		Date Considered 05/29/2016
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.H.N./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Tien-Yu Lu
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP2505USA

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2015-07-06
Name/Print	Winston Hsu	Registration Number	41,526

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.H.N./

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Bertha Chang	(Depositor's name)
/Bertha Chang/	(Signature)
06/24/2016	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/792,636	07/07/2015	Tien-Yu Lu	NAUP2505USA	6268

TITLE OF INVENTION:

LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$960	\$0	\$0	\$960	09/06/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, DAO H	2818	365-154000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev. 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
 1 Winston Hsu
 2 Scott Margo
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

UNITED MICROELECTRONICS CORP.

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

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- ☐ A check is enclosed.
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5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Winston Hsu/

Date 06/23/2016

Typed or printed name Winston Hsu

Registration No. 41526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:		14792636		
Filing Date:		07-Jul-2015		
Title of Invention:		LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF		
First Named Inventor/Applicant Name:		Tien-Yu Lu		
Filer:		Winston Hsu/Bertha Chang		
Attorney Docket Number:		NAUP2505USA		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	26148308
Application Number:	14792636
International Application Number:	
Confirmation Number:	6268
Title of Invention:	LAYOUT PATTERN FOR 8T-SRAM AND THE MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Tien-Yu Lu
Customer Number:	27765
Filer:	Winston Hsu/Bertha Chang
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP2505USA
Receipt Date:	24-JUN-2016
Filing Date:	07-JUL-2015
Time Stamp:	03:45:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	062416INTEFSW00006884503105
Deposit Account	503105
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

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 37 CFR 1.20 (Post Issuance fees)
 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2591643.PDF	99698	no	1
			533dfe2028bd70d37a93e4a8148d6ec72cc d1724		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30685	no	2
			c9ed1c33b0b8eb0eb6037fe3dc90de28b26 8803b		

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Total Files Size (in bytes):	130383
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/792,636	07/26/2016	9401366	NAUP2505USA	6268

27765 7590 07/05/2016
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

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Chun-Hsien Huang, Tainan City, TAIWAN;

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