US 20070158756A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2007/0158756 A1

(43) Pub. Date: Jul. 12, 2007

Dreeskornfeld et al.

(54) **PRODUCTION METHOD FOR A FINFET TRANSISTOR ARRANGEMENT, AND CORRESPONDING FINFET TRANSISTOR ARRANGEMENT**

(76) Inventors: **Lars Dreeskornfeld**, Dresden (DE); **Franz Hofmann**, Munchen (DE); **Johannes Richard Luyken**, Munchen (DE); **Michael Specht**, Munchen (DE)

Correspondence Address:
JENKINS, WILSON, TAYLOR & HUNT, P. A.
SUITE 1200, UNIVERSITY TOWER
3100 TOWER BOULEVARD
DURHAM, NC 27707 (US)

(21) Appl. No.: **11/649,470**

(22) Filed: **Jan. 4, 2007**

(30) **Foreign Application Priority Data**

Jan. 12, 2006 (DE)..... 102006001680.7-33

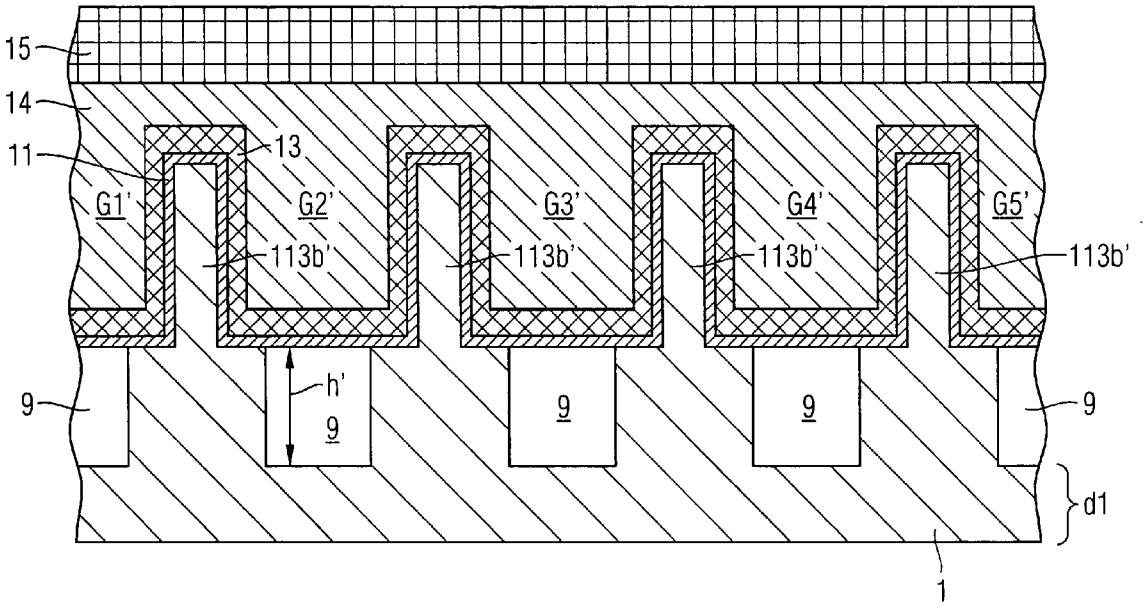
Publication Classification

(51) **Int. Cl.**
H01L 29/76 (2006.01)

(52) **U.S. Cl.** **257/374**

(57) **ABSTRACT**

The present invention provides a production method for a FinFET transistor arrangement, and a corresponding FinFET transistor arrangement. The method comprises the following steps: provision of a substrate (**106, 108**); formation of an active region (**1**) on the substrate, said active region having a source region (**114**), a drain region (**116**) and an intervening fin-like channel region (**113*b*'; 113*b*"**) for each individual FinFET transistor; formation of a gate dielectric (**11**) and a gate region (**13, 14, 15**) over the fin-like channel region (**113*b*'; 113*b*"**) for each individual FinFET transistor; the formation of the fin-like channel region (**113*b*'; 113*b*"**) having the following steps: formation of a hard mask (**S1-S4**) on the active region (**1**), said hard mask having a pad oxide layer (**30**), an overlying pad nitride layer (**50**) and nitride sidewall spacers (**7**); anisotropic etching of the active layer (**1**) using the hard mask (**S1-S4**) for the formation of STI trenches (**G1-G5**); filling of the STI trenches (**G1-G5**) with an STI oxide filling (**9**); polishing-back of the STI oxide filling (**9**) as far as the top side of the hard mask (**S1-S4**); etching-back of the polished-back STI oxide filling (**9**) as far as a residual height (h') in the STI trenches (**G1-G5**); selective removal of the pad nitride layer (**50**) and the nitride sidewall spacers (**7**) with respect to the pad oxide layer (**30**), the etched-back STI oxide filling (**9**) and the active region (**1**) for the formation of a modified hard mask (**S1'-S4'**); anisotropic etching of the active layer (**1**) using the modified hard mask (**S1'-S4'**) for the formation of widened STI trenches (**G1'-G5'**), the fin-like channel regions (**113*b*'; 113*b*"**) of the active region (**1**) remaining for each individual FinFET transistor.



TSMC EXHIBIT 1045
TSMC v. Marlin Semiconductor Ltd.
IPR2025-00864

FIG 1A

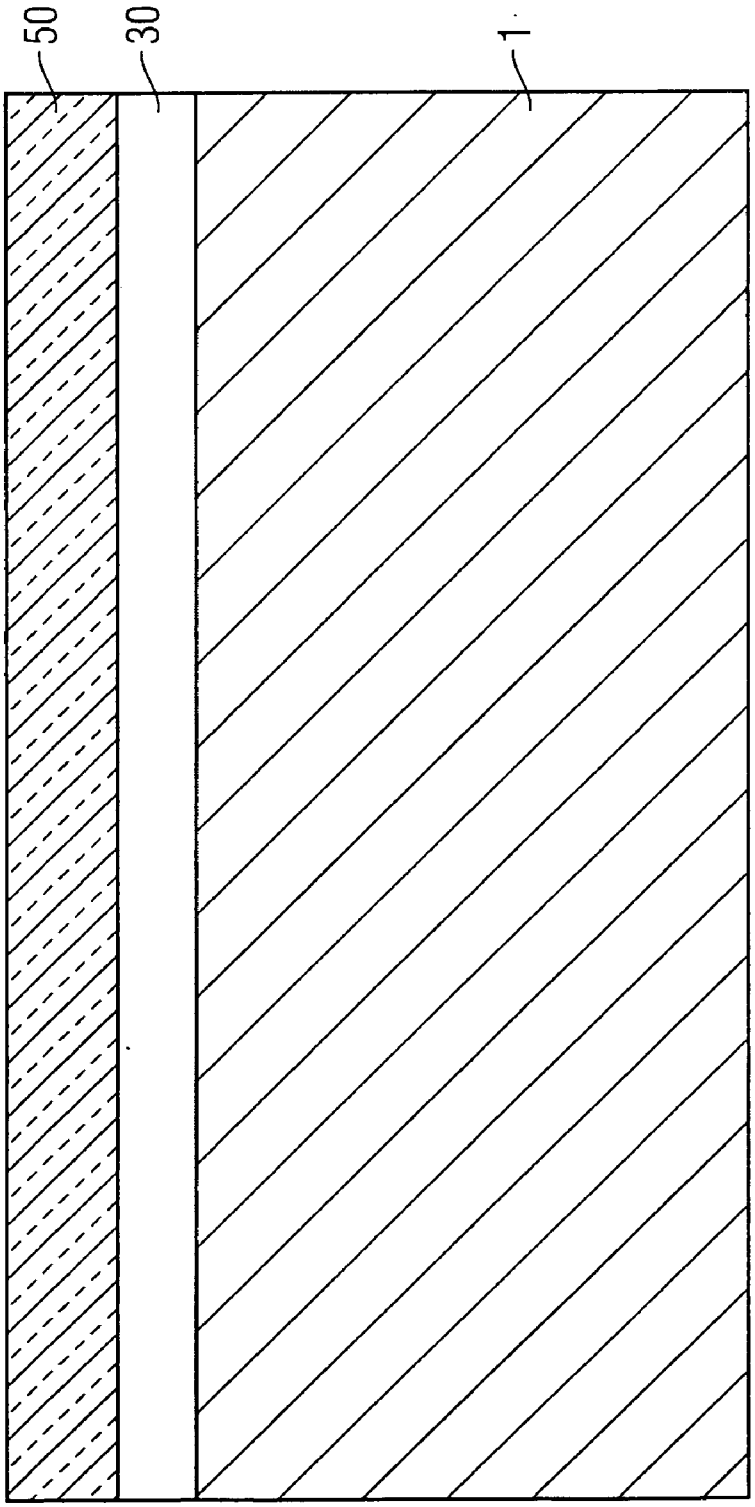
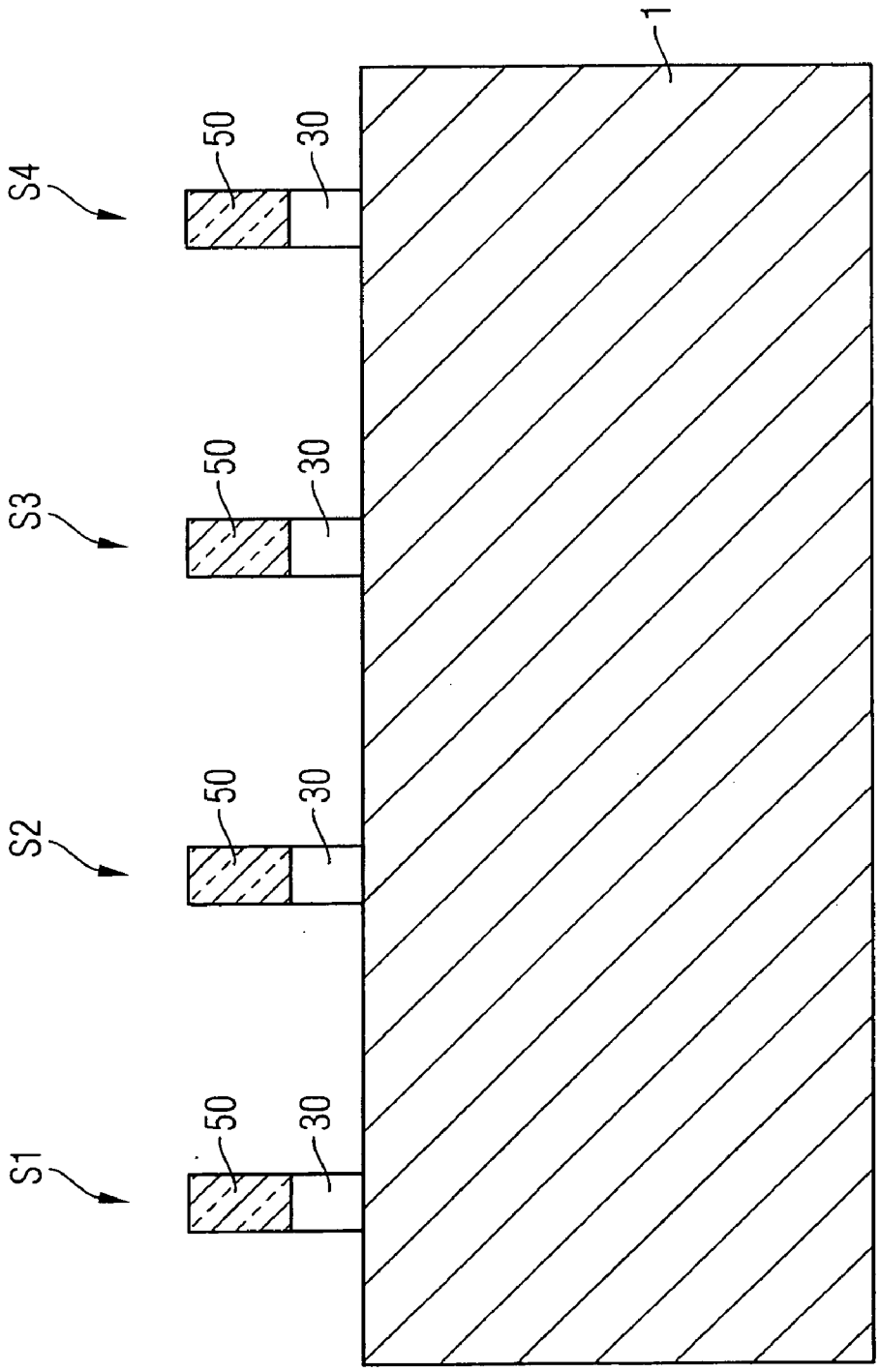


FIG 1B



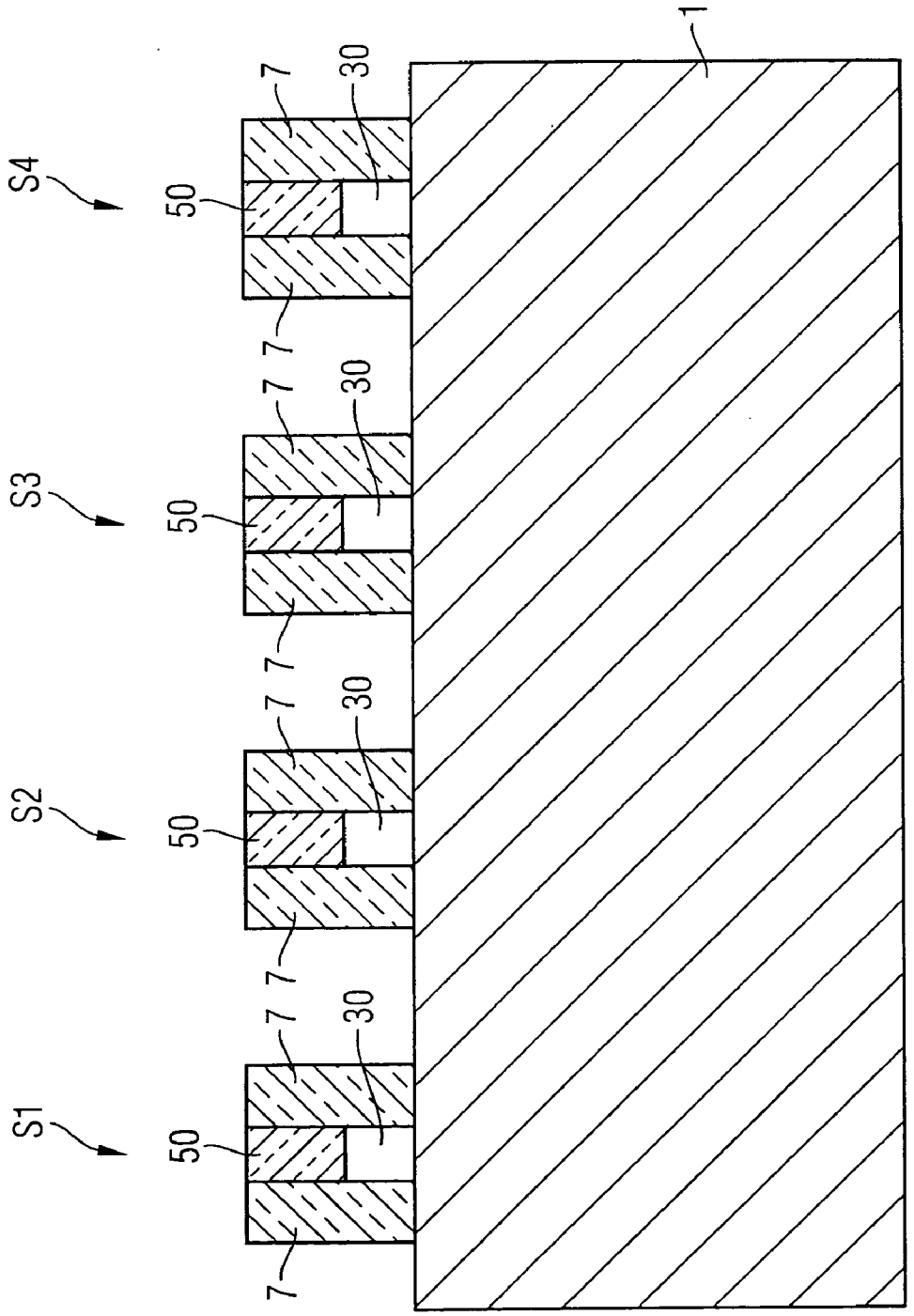
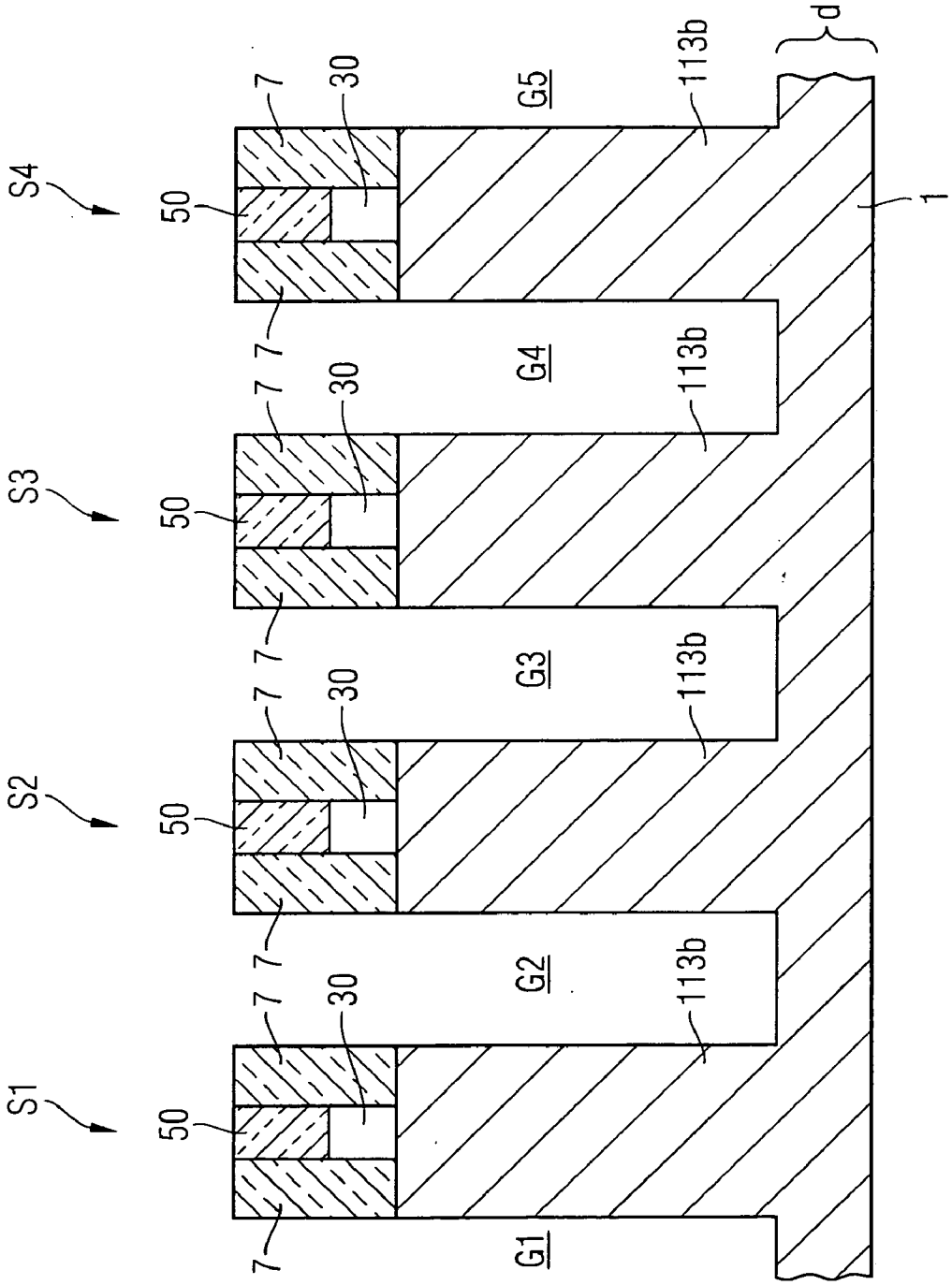


FIG 1C

FIG 1D



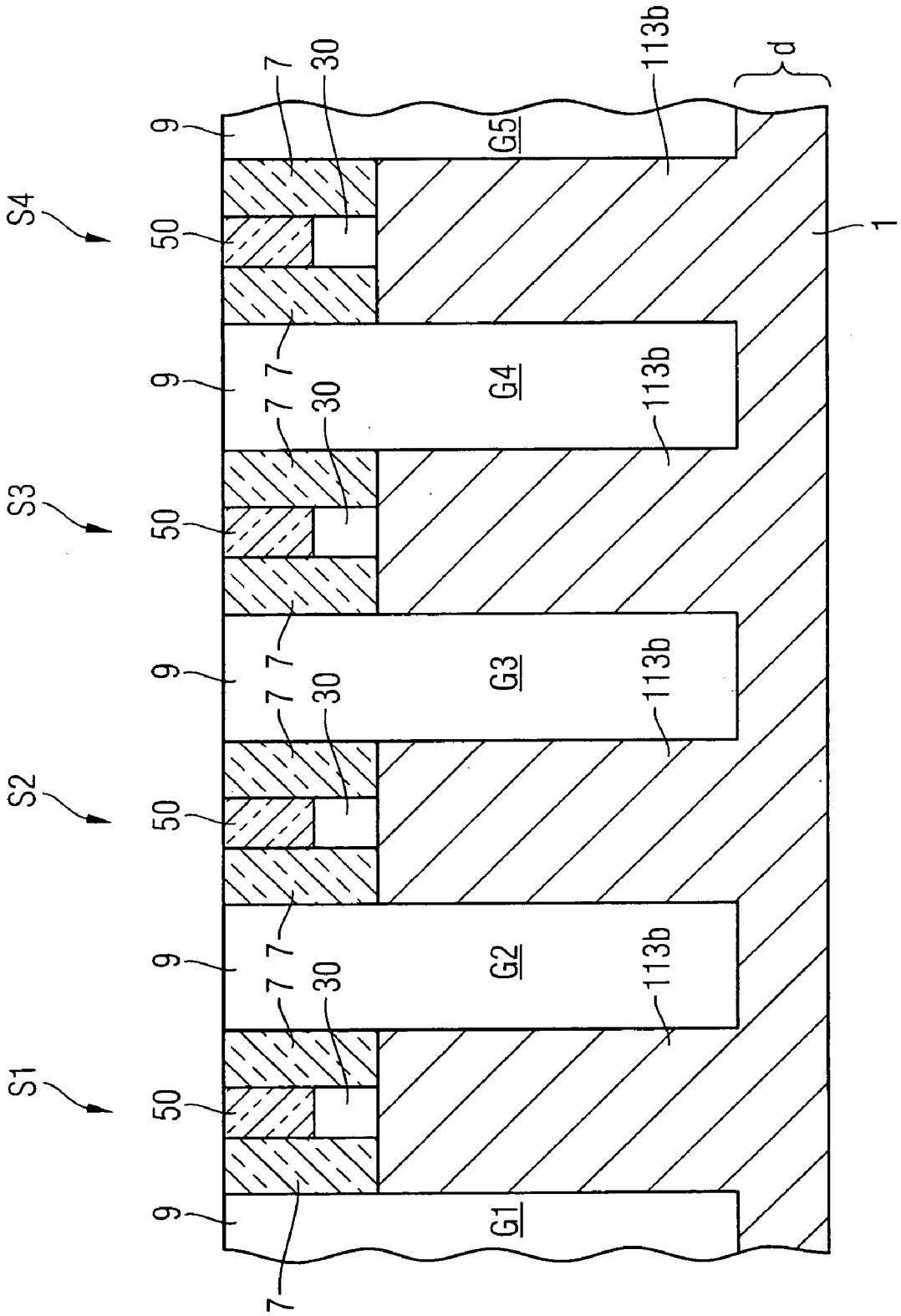


FIG 1E

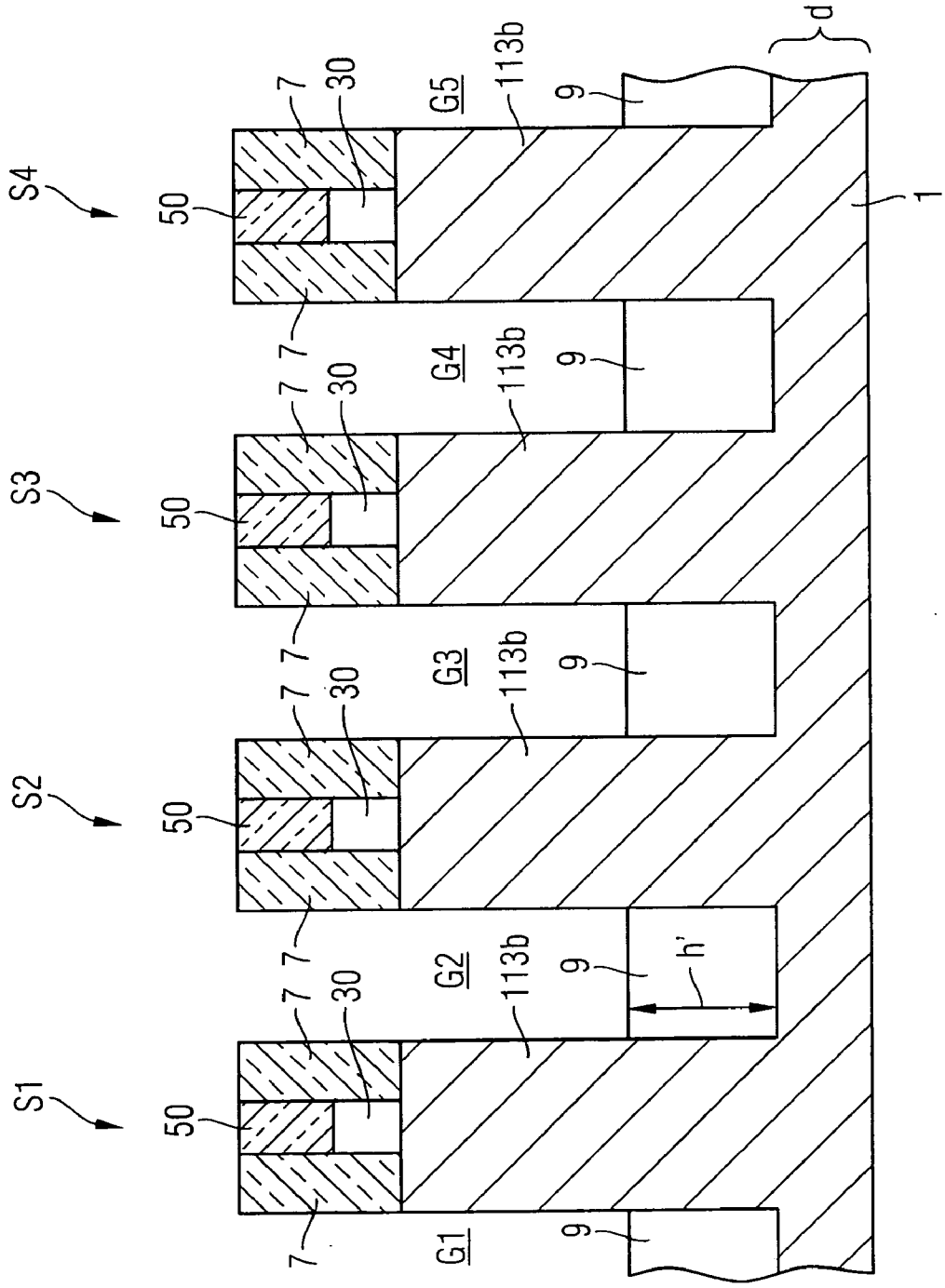


FIG 1F

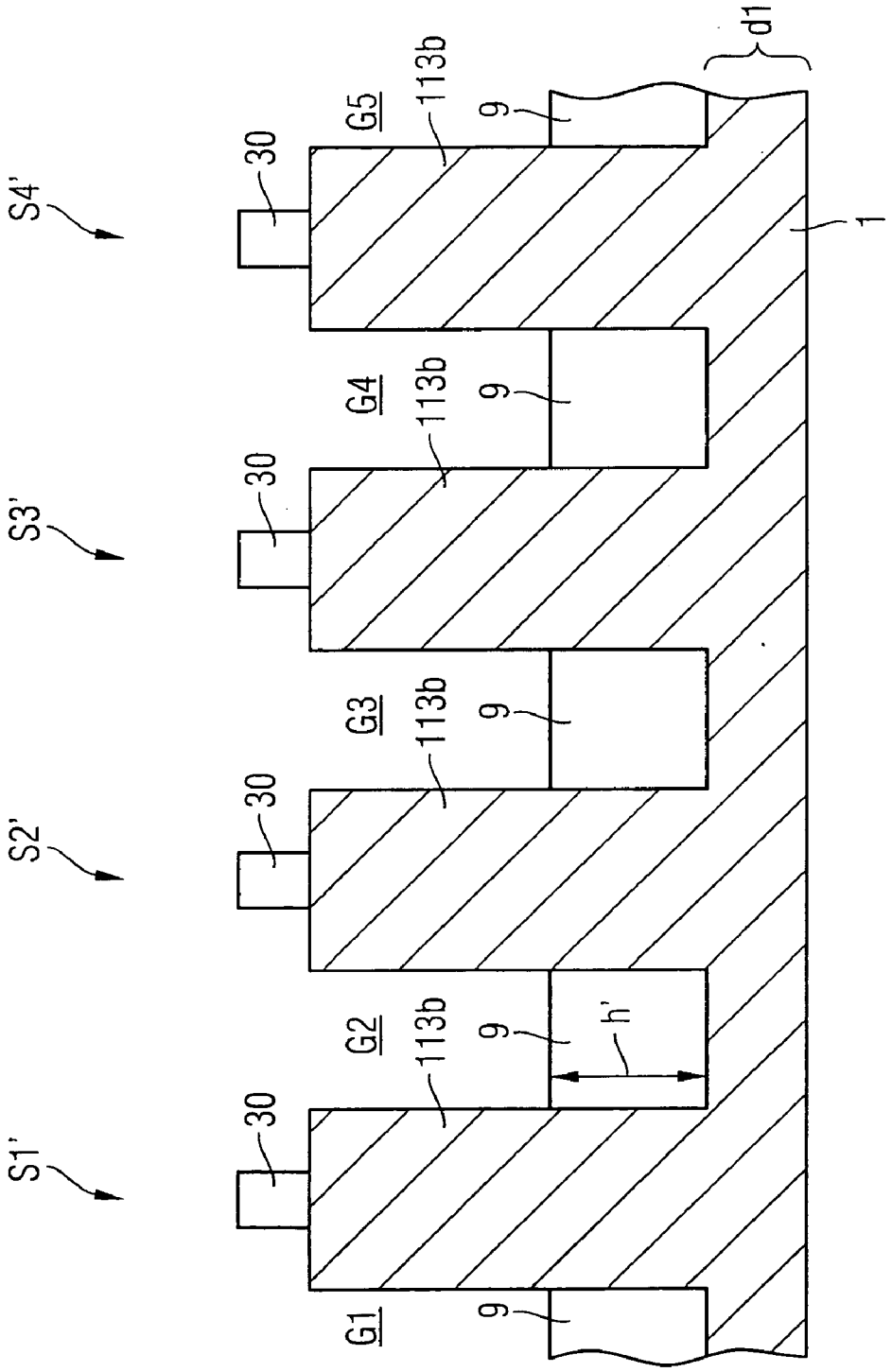

S1'
S2'
S3'
S4'
30
30
30
30
G1
G2
G3
G4
G5
113b
113b
113b
113b
9
9
9
9
9
h'
d1
1

FIG 1G

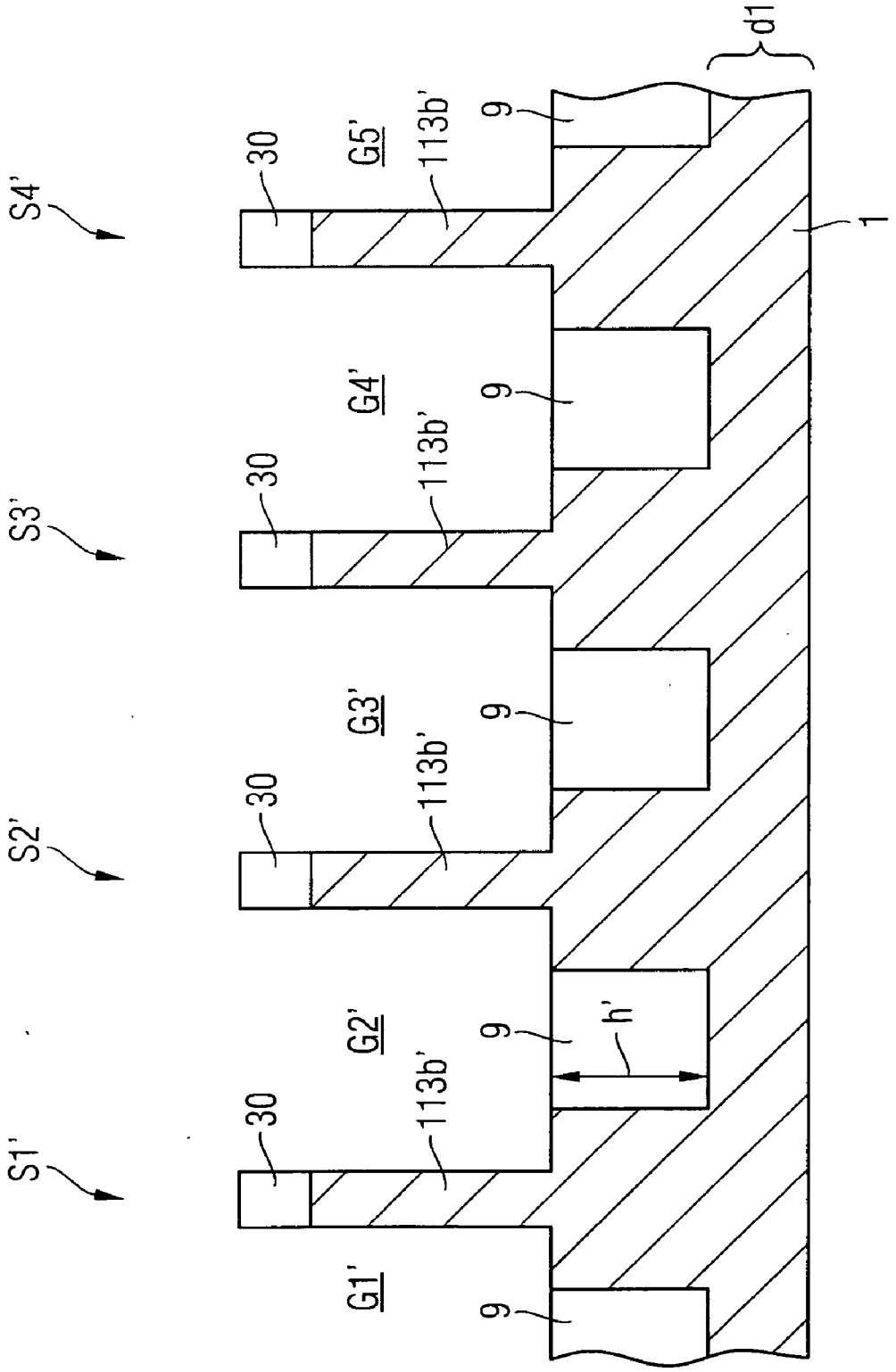
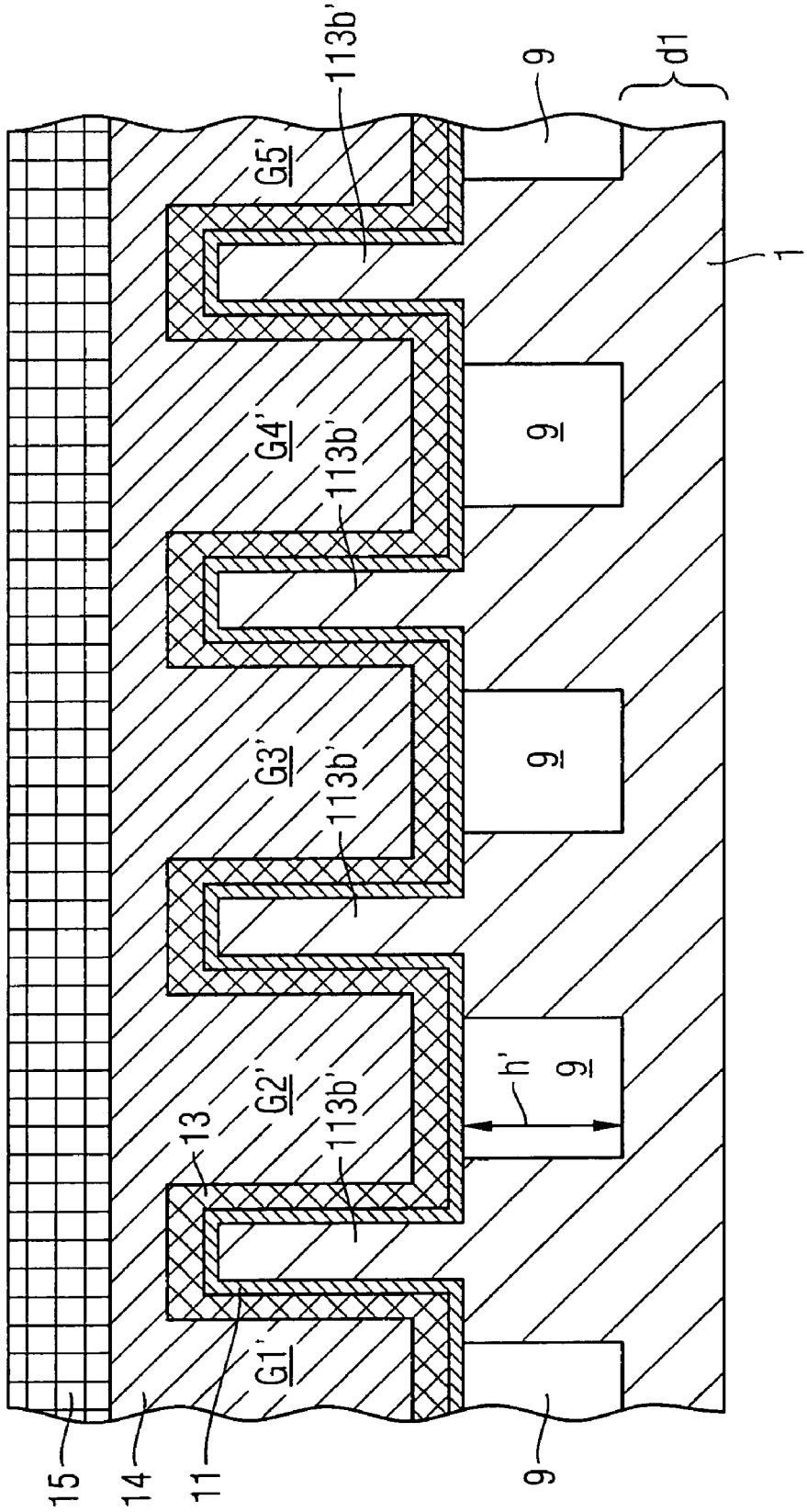

S1'
S2'
S3'
S4'
30
30
30
30
G1'
G2'
G3'
G4'
G5'
113b'
113b'
113b'
113b'
9
9
9
9
9
h'
d1
1

FIG 1H

FIG 1I



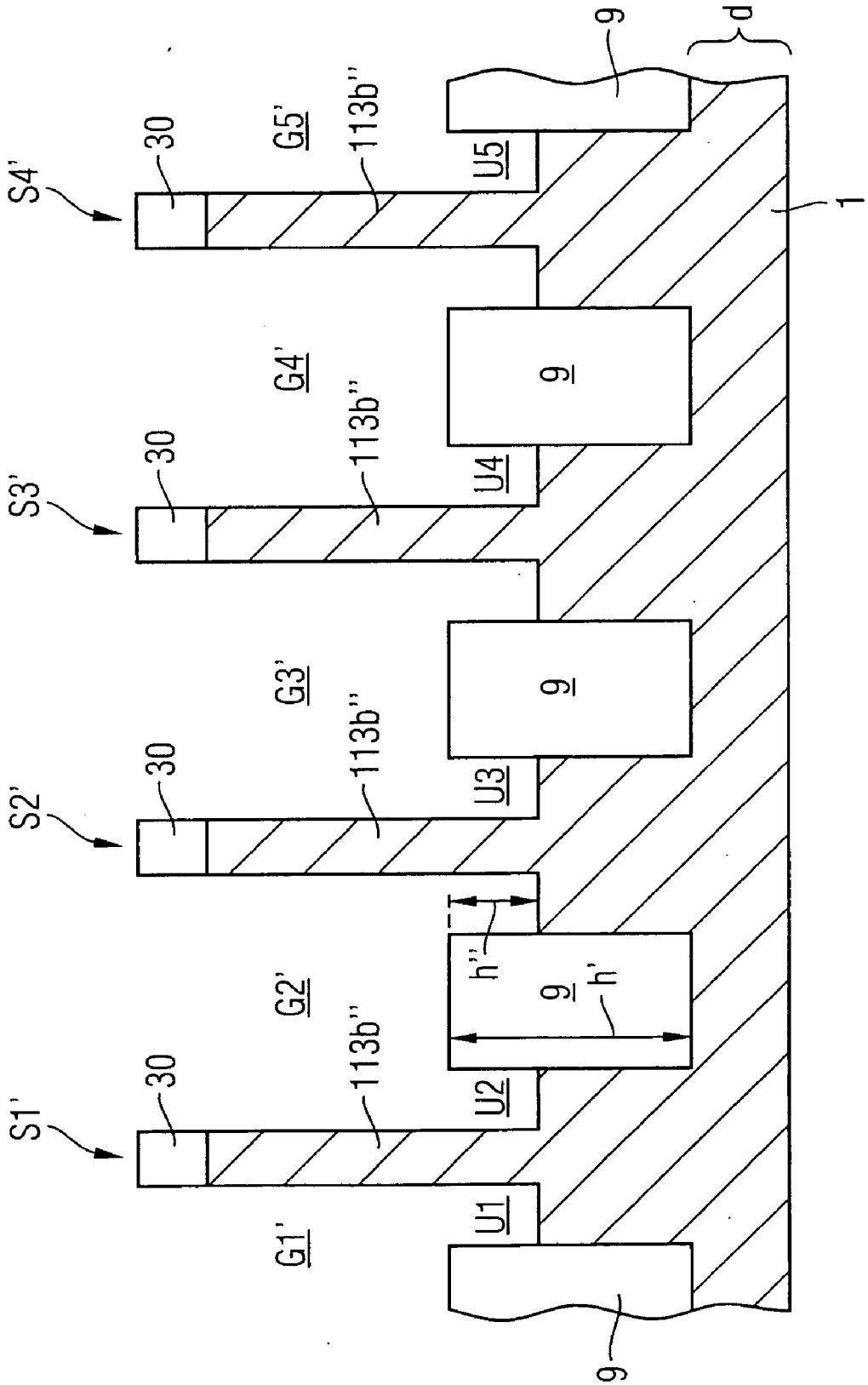

S1'
S2'
S3'
S4'
30
30
30
30
G1'
G2'
G3'
G4'
G5'
113b''
113b''
113b''
113b''
U1
U2
U3
U4
U5
9
9
9
9
9
h''
h'
d
1

FIG 2A

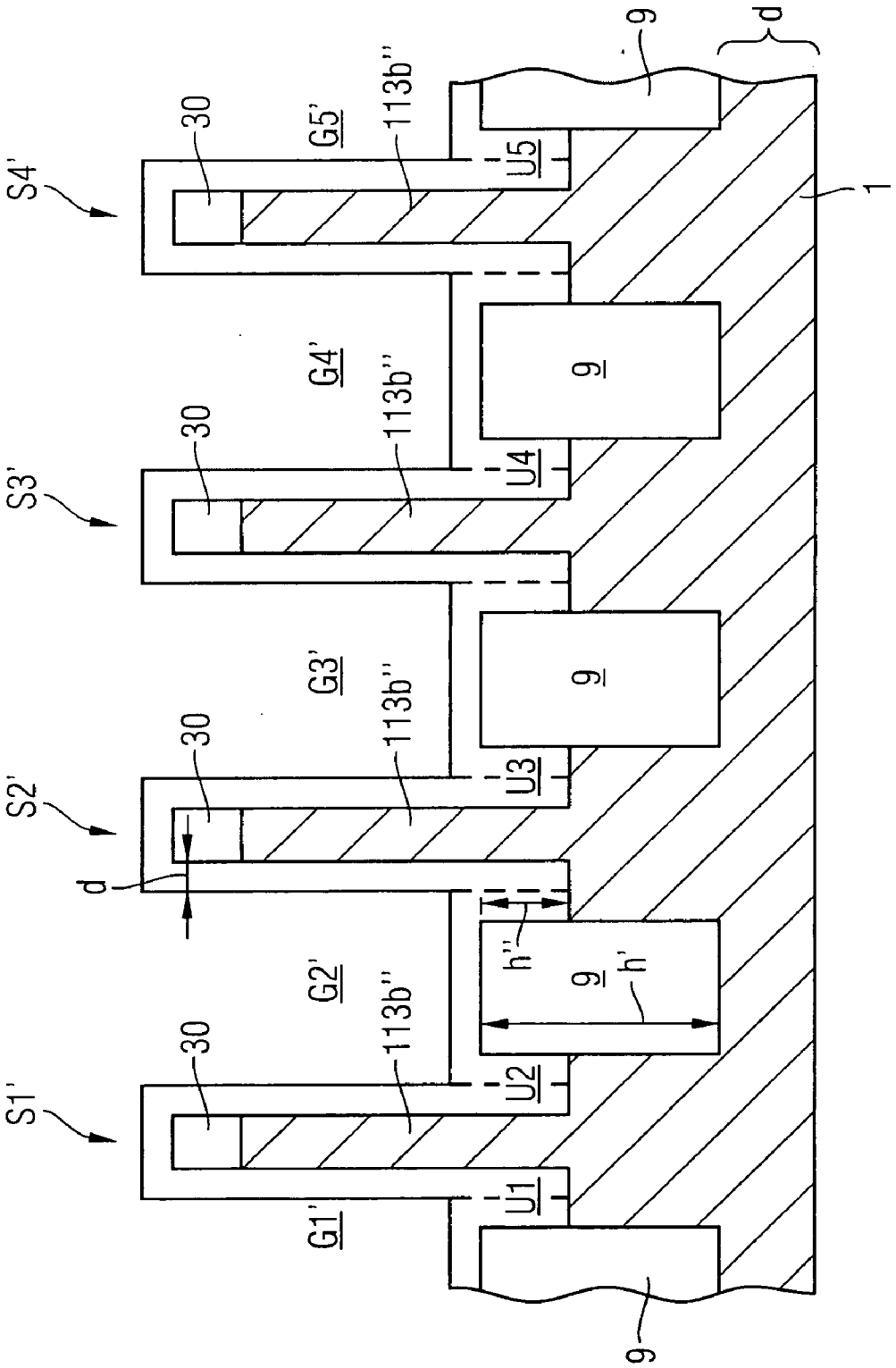

S1'
S2'
S3'
S4'
30
30
30
30
G1'
G2'
G3'
G4'
G5'
113b''
113b''
113b''
113b''
U1
U2
U3
U4
U5
9
9
9
9
9
d
d
h''
h'
1

FIG 2B

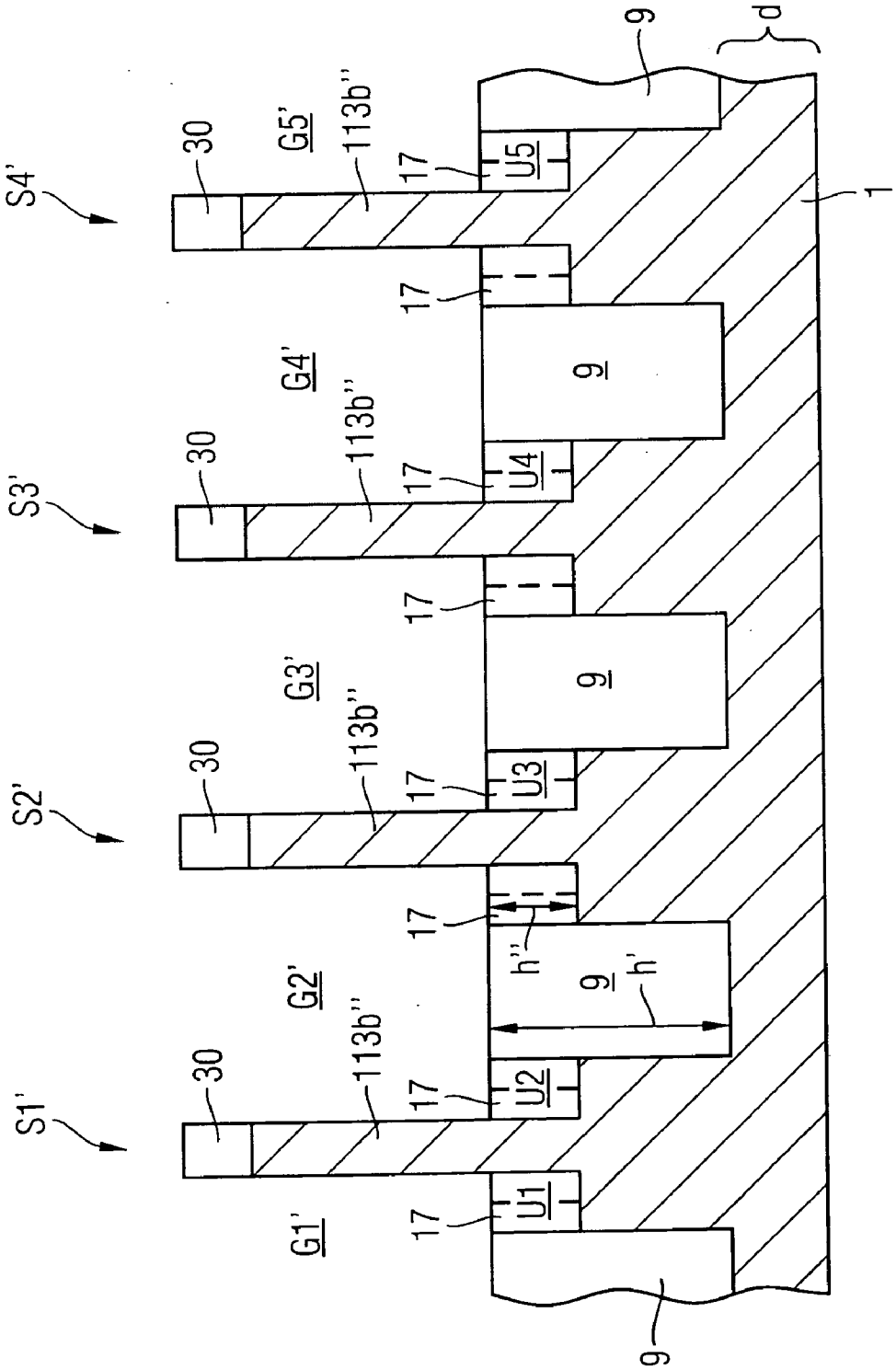


FIG 2C

FIG 2D

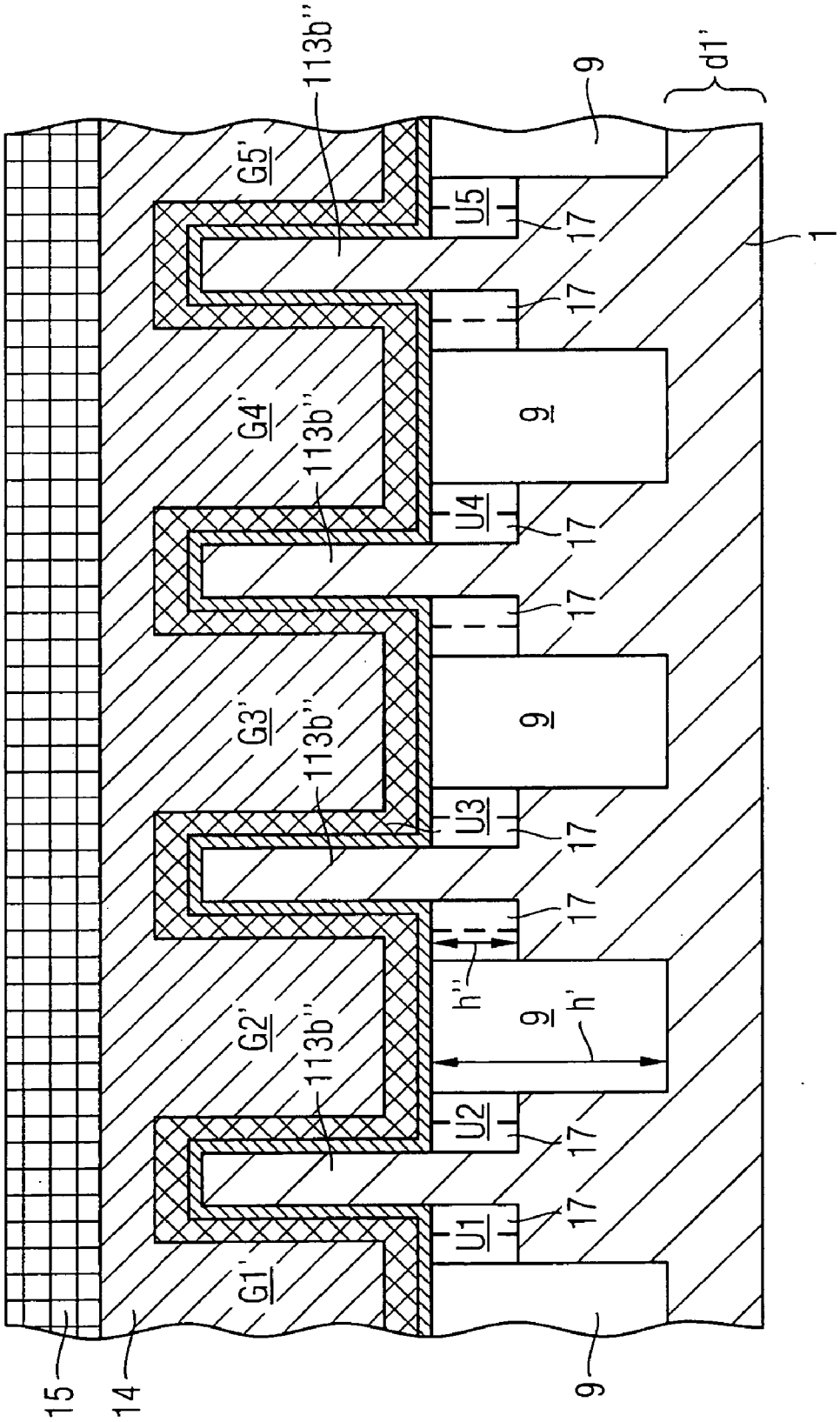

113b''
9
d1'
G5'
U5
17
1
17
G4'
113b''
9
U4
17
17
G3'
113b''
9
U3
17
17
h''
h'
9
G2'
113b''
U2
17
17
U1
G1'
15
14
9

FIG 3A

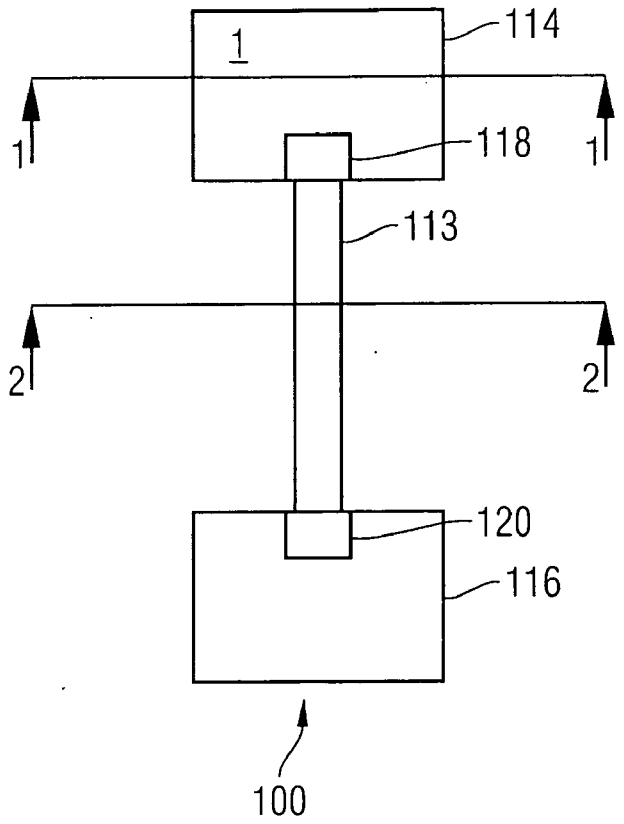


FIG 3B

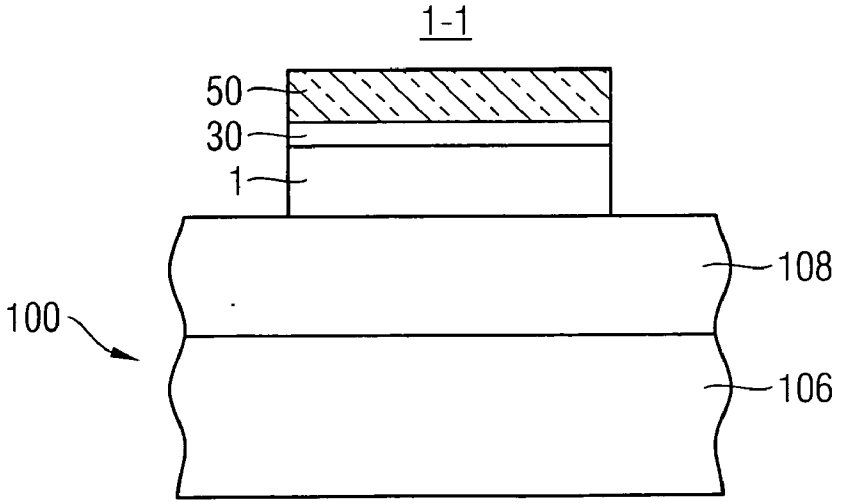


FIG 3C

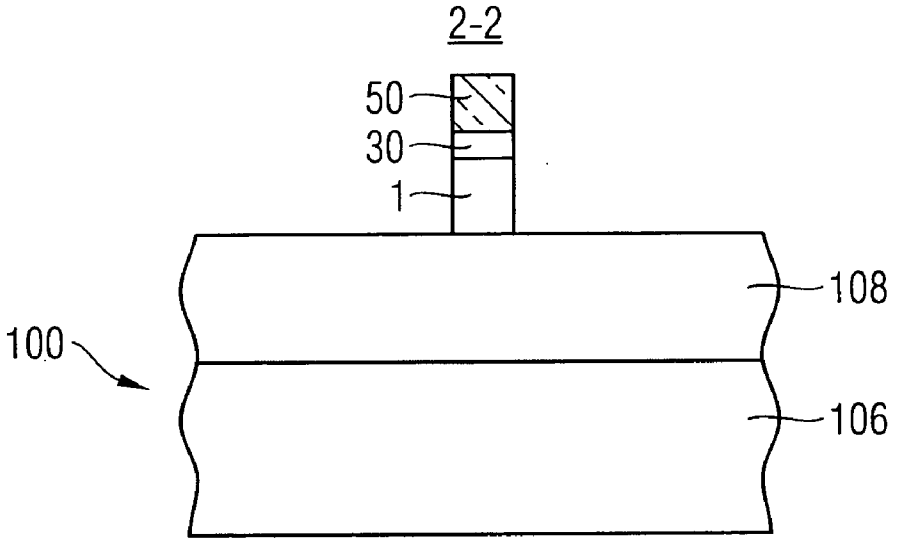


FIG 3D

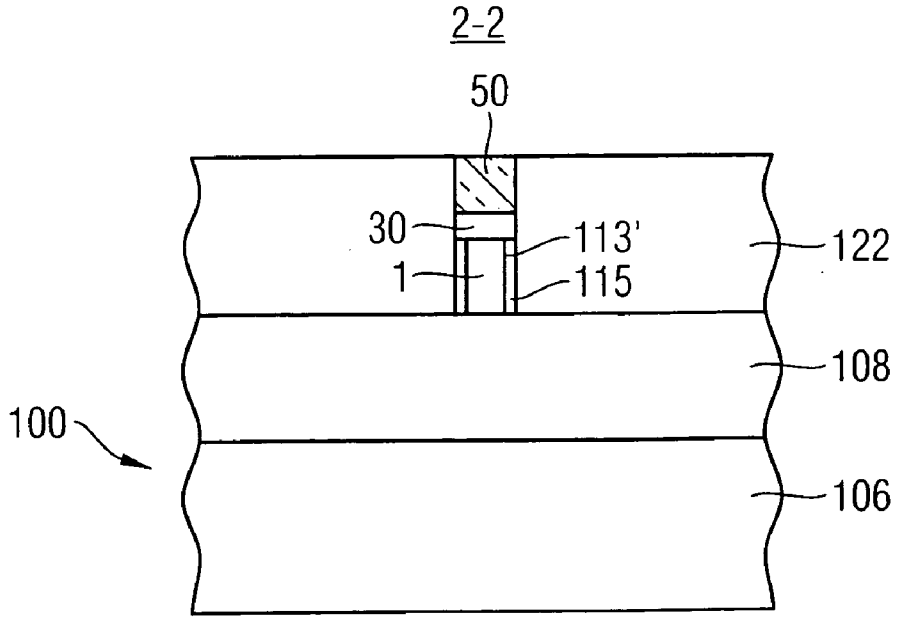


FIG 4A

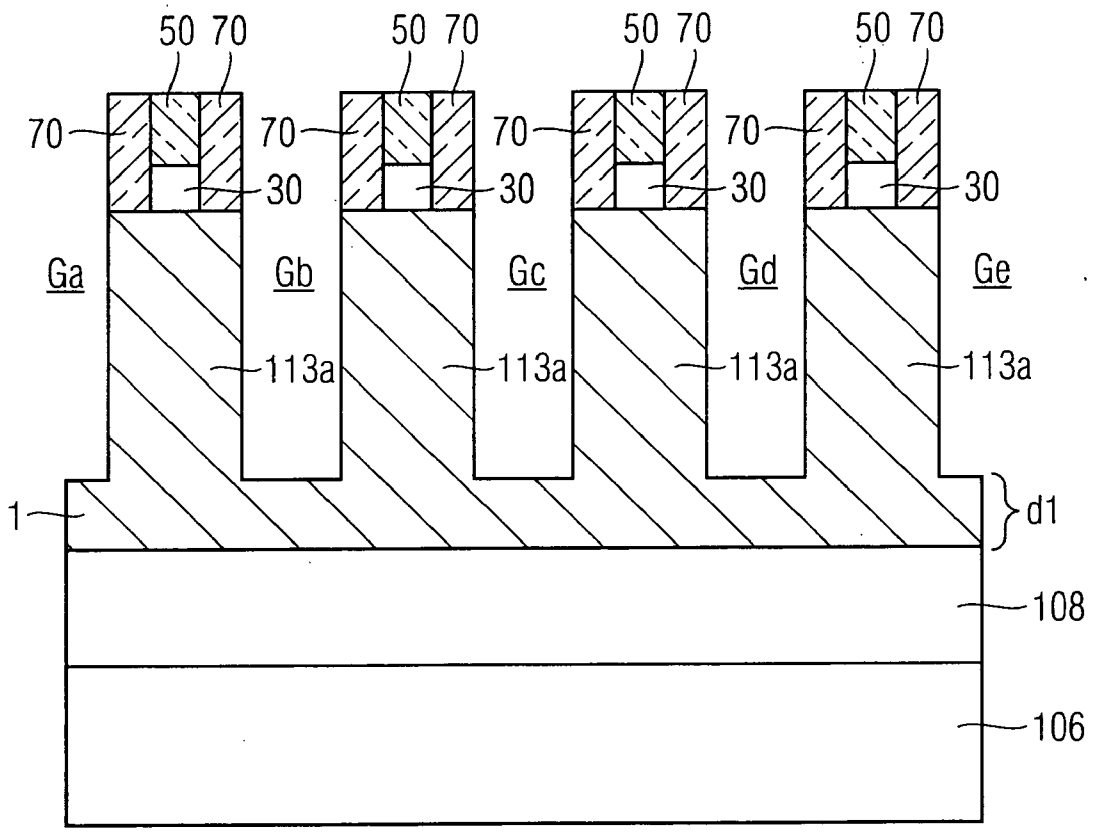
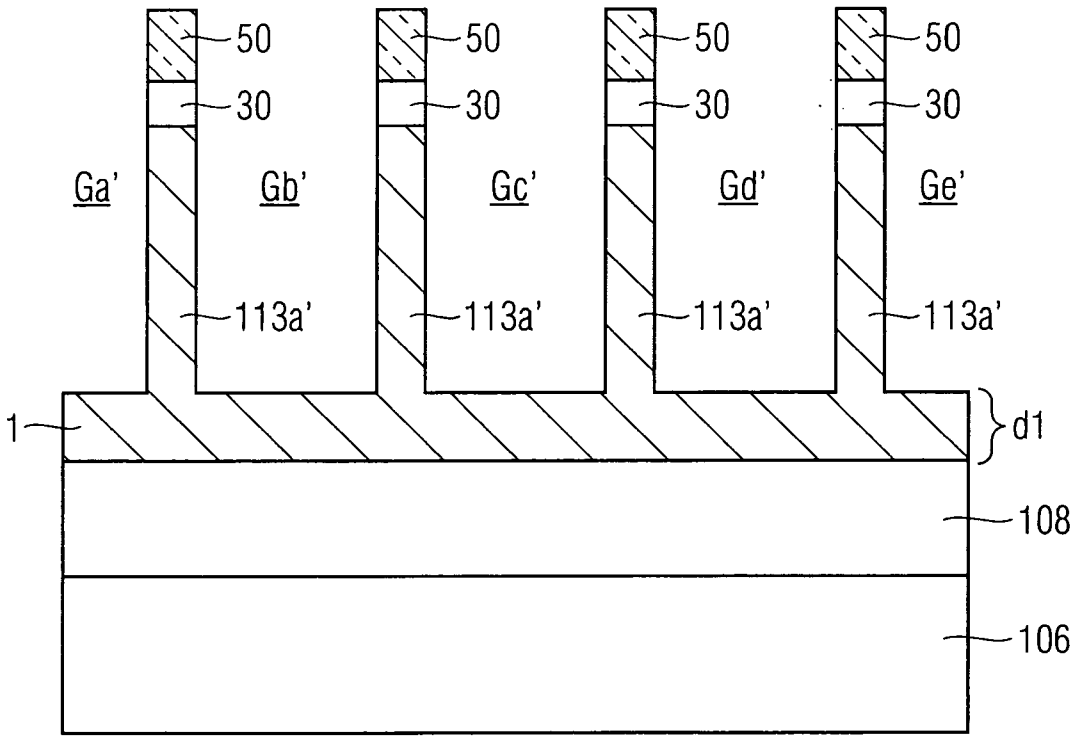

50 70
50 70
50 70
50 70
70
70
70
70
30
30
30
30
Ga
Gb
Gc
Gd
Ge
113a
113a
113a
113a
1
d1
108
106

FIG 4B


50
50
50
50
30
30
30
30
Ga'
Gb'
Gc'
Gd'
Ge'
113a'
113a'
113a'
113a'
1
d1
108
106

PRODUCTION METHOD FOR A FINFET TRANSISTOR ARRANGEMENT, AND CORRESPONDING FINFET TRANSISTOR ARRANGEMENT

[0001] The present invention relates to a production method for a FinFET transistor arrangement, and a corresponding FinFET transistor arrangement.

[0002] Although applicable to any integrated circuits, in principle, the present invention and also the problems on which it is based will be explained with regard to integrated memory circuits using silicon technology with FinFET transistors.

[0003] FinFET transistors (fin field-effect transistors) have a channel region in the form of a fin at which a gate with a corresponding gate electrode is provided on a plurality of sides. An arrangement of this type enables a double gate structure with improved short-channel effects and transistors having gate lengths of the order of magnitude of 10 to 30 nm. FinFET transistors of this type have recently been used to an increased extent in integrated memory circuits using silicon technology.

[0004] FIGS. **3***a-c* are schematic illustrations of a FinFET transistor known from EP 1 202 335 A2, FIG. **3***a* being a top view and FIGS. **3***b,c* being cross sections along the lines **1-1** and **2-2**, respectively, from FIG. **3***a*.

[0005] FIG. **3***a* shows a top view of an SOI substrate (SOI=silicon-on-insulator) **100**. The SOI substrate **100** comprises a carrier substrate **106** in the form of a silicon wafer and also an oxide layer **108** provided thereon and an active silicon layer **1**. In accordance with the illustration of FIGS. **3***b,c*, a hard mask structure comprising a pad oxide layer **30** and a pad nitride layer **50** situated over the latter is provided on the active silicon layer **1**. The pad oxide layer **30** and the pad nitride layer **50** have a thickness of typically 30 to 120 nm and define etching regions for the formation of STI trenches (STI=shallow trench isolation) which isolate the FinFET transistors from one another and from other components.

[0006] The active silicon layer **1** is patterned with the aid of the hard mask comprising the pad oxide layer **30** and the pad nitride layer **50** in such a way that it forms an elongate narrow channel region **113** between two rectangular source and drain regions **114**, **116**. Reference symbols **118**, **120** designate contact regions for the source region **114** and the drain region **116**, respectively. The process state shown in FIGS. **3***a-c* corresponds to a state with uncovered channel region **113**, over which a gate dielectric and gate structure is yet to be formed along the direction **2-2** in FIG. **3***a*, for which various possibilities are suitable in accordance with the prior art.

[0007] FIG. **3***d* is a schematic illustration of a possible fin and gate structure for the FinFET transistor known from EP 1 202 335 A2 proceeding from FIG. **3***c*, as can be gathered from WO 2004/068589.

[0008] In the case of the process variant in accordance with FIG. **3***d*, which is known from WO 2004/068589 A1, firstly an STI oxide (not shown) is deposited, and is removed in direction **2-2** of FIG. **3***a* along the gate structures to be provided. The channel region **113** (also designated as fin region) is subsequently thinned by means of an isotropic silicon etch, which leads to a thinned channel region **113'**. Afterwards, a gate dielectric **115** is provided on the active silicon layer **1** of the thinned channel region **113'**. Finally, an elongate gate region **122** is provided over the gate dielectric **115** along the direction **2-2** of FIG. **3***a*, after which the relevant FinFET transistor is completed.

[0009] In the case of the variant in accordance with FIG. **3***d*, it is disadvantageous that fluctuations of the width of the fin-like channel regions **113'** occur after the isotropic thinning.

[0010] FIGS. **4***a,b* are two schematic illustrations of two exemplary fin structures of a FinFET transistor arrangement comprising the FinFET transistors known from EP 1 202 335 A2.

[0011] In the case of the variants shown in FIGS. **4***a,b*, a sublithographic hard mask is formed on the active silicon layer **1**, said hard mask having the pad oxide layer **30**, the pad nitride layer **50** and, in the case of the variant in accordance with FIG. **4***a*, sidewall spacers **70** composed of silicon nitride and provided laterally with respect thereto.

[0012] In the case of the variants in accordance with FIGS. **4***a,b*, firstly STI trenches Ga, Gb, Gc, Gd, Ge are etched, which define fin-like channel regions **113***a* and **113***a'*, respectively, where the active silicon layer **1** remains. In the case of these variants, moreover, in contrast to the variant in accordance with FIGS. **3***a-c*, the active silicon layer **1** is not etched through completely, rather a residual thickness d**1** of the active silicon layer **1** remains.

[0013] The disadvantage of the variant in accordance with FIG. **4***a* is that the fin-like channel regions **113***a* are relatively wide.

[0014] The disadvantage of the variant in accordance with FIG. **4***b* is that after the anisotropic etch of the active silicon layer **1** and after the filling of the widened STI trenches Ga'-Ge', only very little of the pad nitride layer **50** is still available as a CMP stop. (CMP=chemical mechanical polishing), which leads to considerable problems in the planarization of the STI oxide (not shown).

[0015] The object on which the present invention is based is to provide an improved production method for a FinFET transistor arrangement, and a corresponding FinFET transistor arrangement, having an excellent scalability and a robust production method.

[0016] In accordance with the present invention, this object is achieved by means of the production method according to Claim **1** and, respectively, the corresponding FinFET transistor arrangement in accordance with Claim **8**.

[0017] What is particularly advantageous about the subject matter of the invention is the fact that enough nitride can remain for the CMP step and the fin-like channel regions can nevertheless be made very narrow.

[0018] Advantageous developments and improvements of the production method according to Claim **1** and, respectively, the corresponding FinFET transistor arrangement according to Claim **8** are found in the dependent claims.

[0019] In accordance with one preferred embodiment, the anisotropic etching of the active layer using the modified hard mask is effected as far as the residual height of the etched-back STI oxide filling.

[0020] In accordance with a further preferred embodiment, the anisotropic etching of the active layer using the modified hard mask is effected as far as below the residual height of the etched-back STI oxide filling, with the result that a respective gap region arises between the fin-like channel region and the etched-back STI oxide filling, and that the respective gap region is filled with an insulation layer prior to the formation of the gate dielectric and the gate region. It is thus possible to avoid parasitic transistors at the base of the fin-like channel regions.

[0021] In accordance with a further preferred embodiment, the filling of the respective gap region is effected by deposition and anisotropic etching-back of an oxide layer with a thickness of approximately half the width of the gap regions.

[0022] In accordance with a further preferred embodiment, the modified hard mask is removed prior to the formation of the gate dielectric and the gate region over the fin-like channel region.

[0023] In accordance with a further preferred embodiment, the following steps are carried out for the formation of the gate dielectric and the gate region over the fin-like channel region: deposition of the gate dielectric, deposition of a TaN layer over the gate dielectric, and filling of the modified STI trenches with a polysilicon filling.

[0024] In accordance with a further preferred embodiment, the polysilicon filling (**14**) is planarized and a metal silicide layer (**15**) is deposited over it.

[0025] Preferred embodiments of the invention are illustrated in the drawings and are explained in the description below.

[0026] In the figures:

[0027] FIGS. **1***a-i* show schematic cross sections along the line **2-2** from FIG. **3***a* of a production method for a FinFET transistor arrangement and of a corresponding FinFET transistor arrangement as a first embodiment of the present invention;

[0028] FIGS. **2***a-d* show schematic cross sections along the line **2-2** from FIG. **3***a* of a production method for a FinFET transistor arrangement and of a corresponding FinFET transistor arrangement as a second embodiment of the present invention;

[0029] FIGS. **3***a-c* show schematic illustrations of a FinFET transistor known from EP 1 202 335 A2, FIG. **3***a* being a top view and FIGS. **3***b,c* being cross sections along the lines **1-1** and **2-2**, respectively, from FIG. **3***a;*

[0030] FIG. **3***d* shows a schematic illustration of a possible fin and gate structure for the FinFET transistor known from EP 1 202 335 A2, proceeding from FIG. **3***c*, as can be gathered from WO 2004/068589; and

[0031] FIGS. **4***a,b* show a schematic illustration of an exemplary fin structure of a FinFET transistor arrangement comprising the FinFET transistors known from EP 1 202 335 A2.

[0032] In the figures, identical reference symbols designate identical or functionally equivalent components.

[0033] FIG. **1***a-i* are schematic cross sections along the line **2-2** from FIG. **3***a* of a production method for a FinFET transistor arrangement and of a corresponding FinFET transistor arrangement as a first embodiment of the present invention.

[0034] Only the cross section in direction **2-2** from FIG. **3***a* is illustrated in the description of the embodiments in accordance with FIGS. **1***a-i* and FIGS. **2***a-d*. The rest of the known process steps for producing the source and drain regions **114**, **116** and also the carrier substrate **106** and the oxide layer **108** are omitted in the relevant illustrations for the purpose of simplification. In this connection, reference is made to the entire scope of the illustration in accordance with FIGS. **3***a-c*.

[0035] FIG. **1***a* shows the active silicon layer **1** with the pad oxide layer **3** situated thereon and the overlying pad nitride layer **50**. This is followed, referring to FIG. **1***b*, by a patterning of the pad oxide layer **30** and the pad nitride layer **50** to form a hard mask with-hard mask regions S**1**, S**2**, S**3**, S**4** corresponding to the later position of the fin-like channel regions using customary photolithographic technology.

[0036] At the hard mask regions S**1**-S**4**, in accordance with FIG. **1***c*, nitride spacers **7** are provided on both sides by deposition and anisotropic etching-back of a silicon nitride layer.

[0037] Afterwards, in accordance with FIG. **1***d*, STI trenches G**1**-G**5** are etched in the active silicon layer **1** using the hard mask regions S**1**-S**4**, which define fin-like regions **113***b* as precursors of the later channel regions in the remaining active silicon layer **1**.

[0038] Afterwards, the STI trenches G**1**-G**5** are filled with an STI oxide filling **9**, after which the STI oxide filling **9** is polished back as far as the top side as the hard mask regions S**1**-S**4**. On account of the hard mask regions S**1**-S**4** widened by the sidewall spacers **7**, in the cell array shown there is an area ratio of STI oxide filling **9** to hard mask regions S**1**-S**4** of 1:1, which means that enough nitride is available for stopping the CMP process. This leads to the process state in accordance with FIG. **1***e*.

[0039] Referring further to FIG. **1***f*, the STI oxide filling **9** is then etched back down to a residual height h' with respect to the bottoms of the STI trenches G**1**-G**5**.

[0040] Then, in accordance with FIG. **1***g*, that part of the hard mask regions S**1**-S**4** which comprises the pad nitride layer **50** is removed selectively with respect to the pad oxide layer **30**, with respect to the active silicon substrate **1** and with respect to the STI oxide filling **9** by means of a corresponding selective etch, for example a wet-chemical etch. Narrowed hard mask regions S**1'**-S**4'** remain which are composed only of the pad oxide layer **30**.

[0041] As illustrated in FIG. **1***h*, this is followed by an anisotropic silicon etch using the narrowed hard mask regions S**1'**-S**4'** as a mask, which reaches in the depth as far as the height h' of the etched-back STI oxide filling **9**. The thinned fin-like channel regions **113***b*' remain, a respective region with an STI oxide filling **9** being provided between adjacent fin-like channel regions **113***b*' in the active silicon substrate **1**. In this case, the STI oxide filling **9** prevents the silicon between the fin-like channel regions **113***b*' from being etched away even more deeply in the course of the silicon etch in accordance with FIG. **1***h*.

[0042] In a concluding process step sequence, which is illustrated in FIG. **1***i*, the remaining hard mask regions S**1**'-S**4**' composed of the pad oxide layer **30** are removed and an ONO dielectric layer **11** is then deposited. Afterwards, a TaN layer **13** is deposited over the resulting structure. The upper regions of the trenches G**1**'-G**5**' are then filled with a polysilicon layer **14**, which is subsequently planarized by means of a CMP process. Finally, a tungsten-silicon layer **50** is deposited over the planar structure. A photolithography step (not shown) is effected for the definition of gate interconnects running in direction **2**-**2** form FIG. **3***a*. Finally, the superfluous regions of the layers **11**, **13**, **14**, **15** are removed using the photresist mask, not shown, and the photresist is stripped, which leads to the state in accordance with FIG, **1***i*. In the course of the pad oxide etch, the STI oxide filling is slightly incipiently etched in the process, but this is insignificant in the case of a thin pad oxide layer **30**. If the small steps that arise from this are disturbing, the silicon etch could be carried out with a corresponding bias as far as below the top side of the STI oxide filling **9** (cf. the second embodiment explained below).

[0043] FIGS. **2***a-d* are schematic cross sections along the line **2**-**2** from FIG. **3***a* of a production method for a FinFET transistor arrangement, and of a corresponding FinFET transistor arrangement as a second embodiment of the present invention.

[0044] The process sequence of the second embodiment in accordance with FIGS. **2***a-d* follows the process state in accordance with FIG. **1***h*. In contrast to the process state in accordance with FIG. **1***h*, in accordance with FIG. **2***a*, the anisotropic silicon etch is continued as far as below the height h' of the remaining STI oxide filling **9**. This produces gap regions U**1**-U**5** surrounding the remaining STI oxide filling **9**. This has the particular effect that there is no longer any parasitic transistor present at the base point of the thinned fin-like channel region **113***b*". The gap regions U**1**-U**5** have a height h" in this case.

[0045] Referring further to FIG. **2***b*, a thin oxide layer **17** is deposited, the thickness of which corresponds approximately to half the width of the gap regions U**1**-U**5**, as indicated by the dashed line in the gap regions U**1**-U**5** in FIG. **2***b*. This is followed by a wet-chemical etching-back of the thin oxide layer **17** in such a way that the latter remains only in the gap regions U**1**-U**5**, as can be seen from FIG. **2***c*.

[0046] The remaining course of the process, the result of which is illustrated in FIG. **2***d*, takes place completely analogously to the course of the process that has already been described thoroughly in connection with FIG. **1***i*.

[0047] The second embodiment involves, in particular, preventing the gate dielectric from running over pointed edges of the silicon in the lower region of the STI oxide filling.

[0048] Although the present invention has been described with regard to preferred embodiments, it is not restricted thereto, but rather can be modified in various ways which appear clear to the person skilled in the art.

[0049] In particular, the selection of the materials is only an example and can be varied diversely.

[0050] In particular, it is possible to use a different gate dielectric instead of ONO. The SONOS-like transistors, floating gate transistors and logic transistors can thus be produced according to the invention.

1. Production method for a FinFET transistor arrangement comprising the following steps:

provision of a substrate (**106**, **108**);

formation of an active region (**1**) on the substrate, said active region having a source region (**114**), a drain region (**116**) and an intervening fin-like channel region (**113***b*'; **113***b*") for each individual FinFET transistor;

formation of a gate dielectric (**11**) and a gate region (**13**, **14**, **15**) over the fin-like channel region (**113***b*'; **113***b*") for each individual FinFET transistor;

the formation of the fin-like channel region (**113***b*'; **113***b*") having the following steps:

formation of a hard mask (S**1**-S**4**) on the active region (**1**), said hard mask having a pad oxide layer (**30**), an overlying pad nitride layer (**50**) and nitride sidewall spacers (**7**);

anisotropic etching of the active layer (**1**) using the hard mask (S**1**-S**4**) for the formation of STI trenches (G**1**-G**5**);

filling of the STI trenches (G**1**-G**5**) with an STI oxide filling (**9**);

polishing-back of the STI oxide filling (**9**) as far as the top side of the hard mask (S**1**-S**4**);

etching-back of the polished-back STI oxide filling (**9**) as far as a residual height (h') in the STI trenches (G**1**-G**5**);

selective removal of the pad nitride layer (**50**) and the nitride sidewall spacers (**7**) with respect to the pad oxide layer (**30**), the etched-back STI oxide filling (**9**) and the active region (**1**) for the formation of a modified hard mask (S**1**'-S**4**');

anisotropic etching of the active layer (**1**) using the modified hard mask (S**1**'-S**4**') for the formation of widened STI trenches (G**1**'-G**5**'), the fin-like channel regions (**113***b*'; **113***b*") of the active region (**1**) remaining for each individual FinFET transistor.

2. Production method according to claim 1, characterized in that the anisotropic etching of the active layer (**1**) using the modified hard mask (S**1**'-S**4**') is effected as far as the residual height (h') of the etched-back STI oxide filling (**9**).

3. Production method according to claim 1, characterized in that the anisotropic etching of the active layer (**1**) using the modified hard mask (S**1**'-S**4**') is effected as far as below the residual height (h') of the etched-back STI oxide filling (**9**), with the result that a respective gap region (u**1**-u**5**) arises between the fin-like channel region (**113***b*") and the etched-back STI oxide filling (**9**), and in that the respective gap region (u**1**-u**5**) is filled with an insulation layer (**17**) prior to the formation of the gate dielectric (**11**) and the gate region (**13**, **14**, **15**).

4. Production method according to claim 3, characterized in that the filling of the respective gap region (u**1**-u**5**) is effected by deposition and anisotropic etching-back of an oxide layer (**17**) with a thickness of approximately half the width of the gap regions (u**1**-u**5**).

5. Production method according to one of the preceding claims, characterized in that the modified hard mask (S**1**'-

S5') is removed prior to the formation of the gate dielectric (**11**) and the gate region (**13**, **14**, **15**) over the fin-like channel region (**113***b*'; **113***b*")

6. Production method according to one of the preceding claims, characterized in that the following steps are carried out for the formation of the gate dielectric (**11**) and the gate region (**13**, **14**, **15**) over the fin-like channel region (**113***b*'; **113***b*"):

deposition of the gate dielectric (**11**);

deposition of a TaN layer (**13**) over the gate dielectric (**11**); and

filling of the modified STI trenches (G**1**'-G**5**') with a polysilicon filling (**14**).

7. Production method according to claim 6, characterized in that the polysilicon filling (**14**) is planarized and a metal silicide layer (**15**) is deposited over it.

8. FinFET transistor arrangement comprising:

a substrate (**106**, **108**);

an active region (**1**) on the substrate, said active region having a source region (**114**), a drain region (**116**) and an intervening fin-like channel region (**113***b*'; **113***b*") for each individual FinFET transistor;

a gate dielectric (**11**) and a gate region (**13**, **14**, **15**) over the fin-like channel region (**113***b*'; **113***b*") for each individual FinFET transistor;

a respective region with an STI oxide filling (**9**), over which region the gate dielectric (**11**) and the gate region (**13**, **14**, **15**) run, being provided between adjacent fin-like channel regions (**113***b*'; **113***b*") in the active region (**1**).

9. FinFET transistor arrangement according to llaim **8**, characterized in that the STI oxide filling (**9**) reaches as far as the underside of the fin-like channel regions (**113***b*'; **113***b*").

10. FinFET transistor arrangement according to claim 8, characterized in that the STI oxide filling (**9**) reaches as far as above the underside of the fin-like channel. regions (**113***b*'; **113***b*") and a gap region (u**1**-u**5**) filled with an insulating filling (**17**) is provided between the respective fin-like channel region (**113***b*") and the STI oxide filling (**9**).

* * * * *