

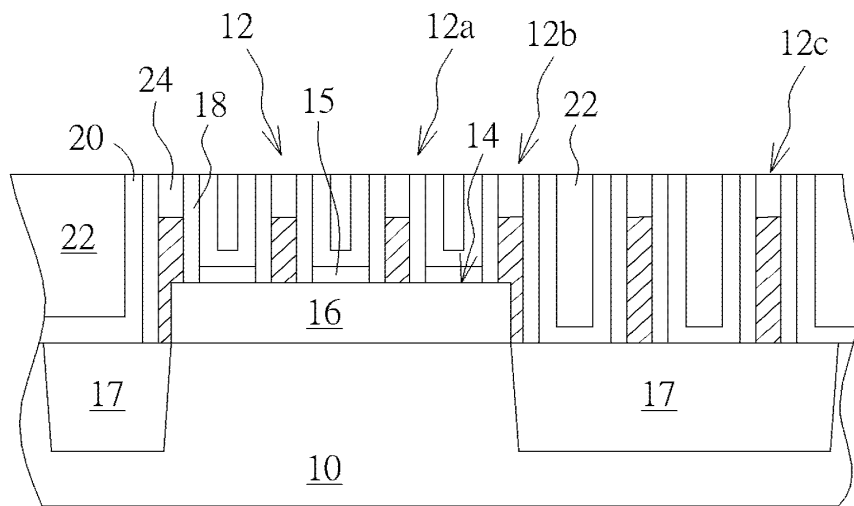


FIG. 1

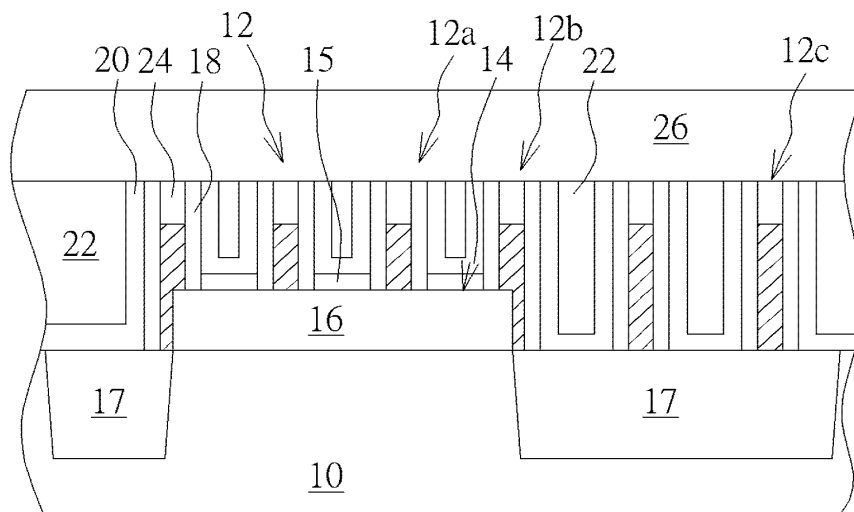


FIG. 2

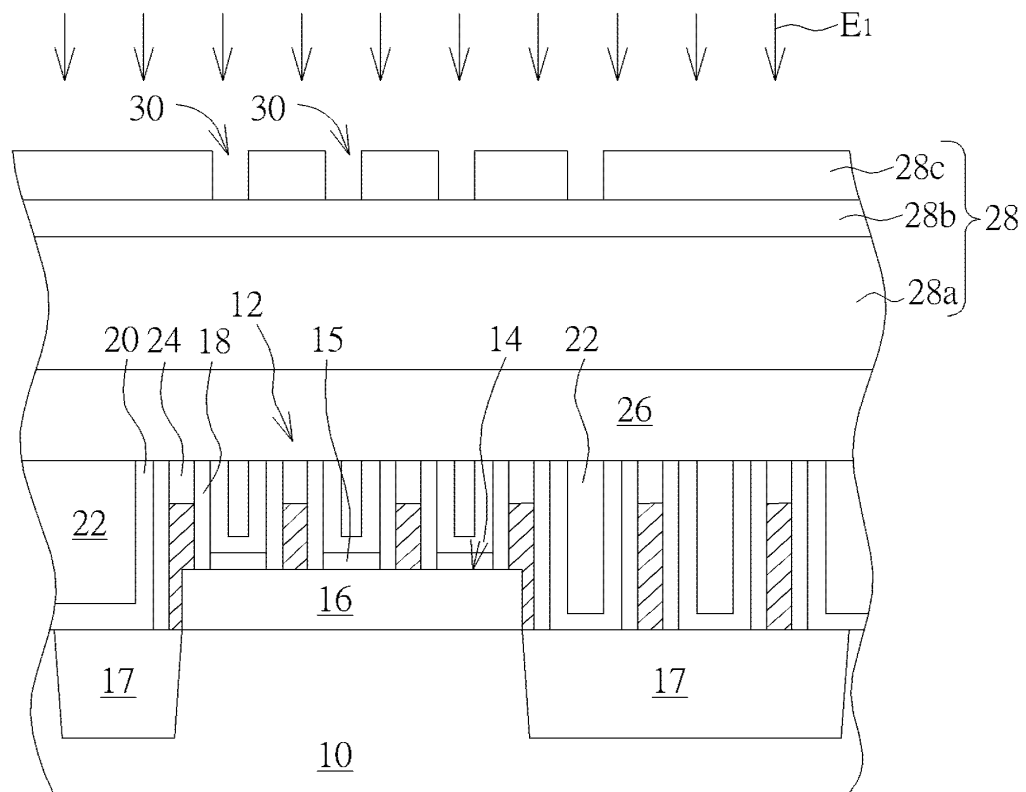


FIG. 3

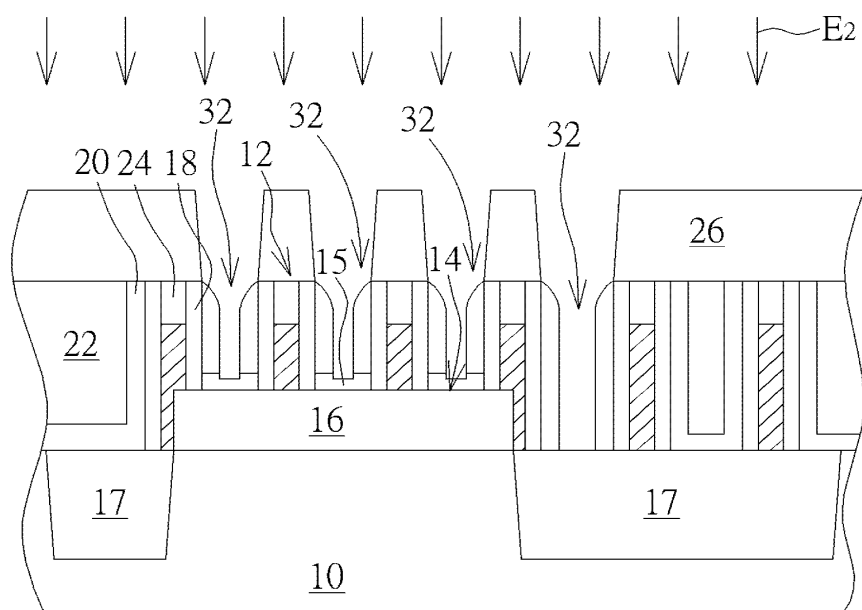


FIG. 4

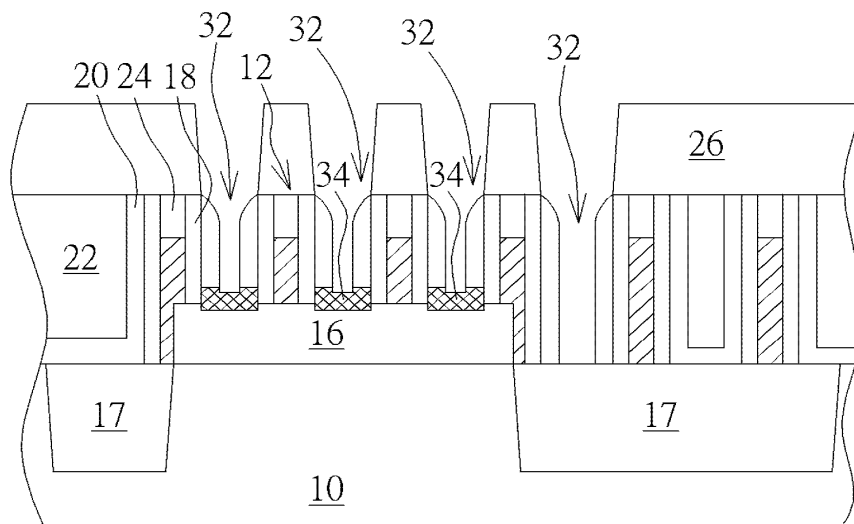


FIG. 5

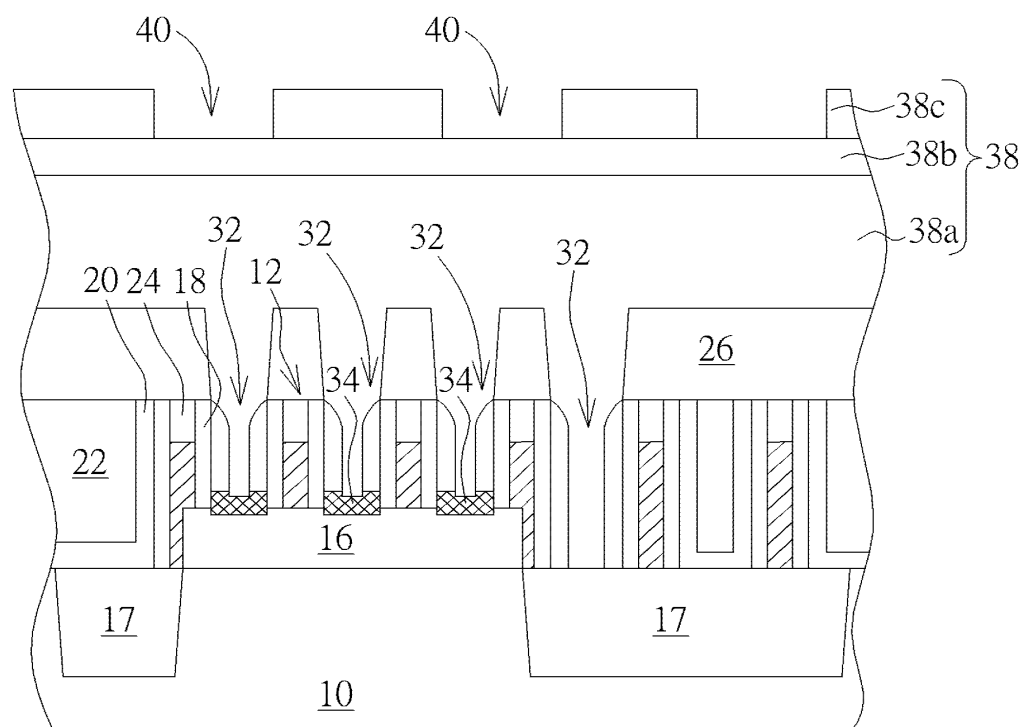


FIG. 6

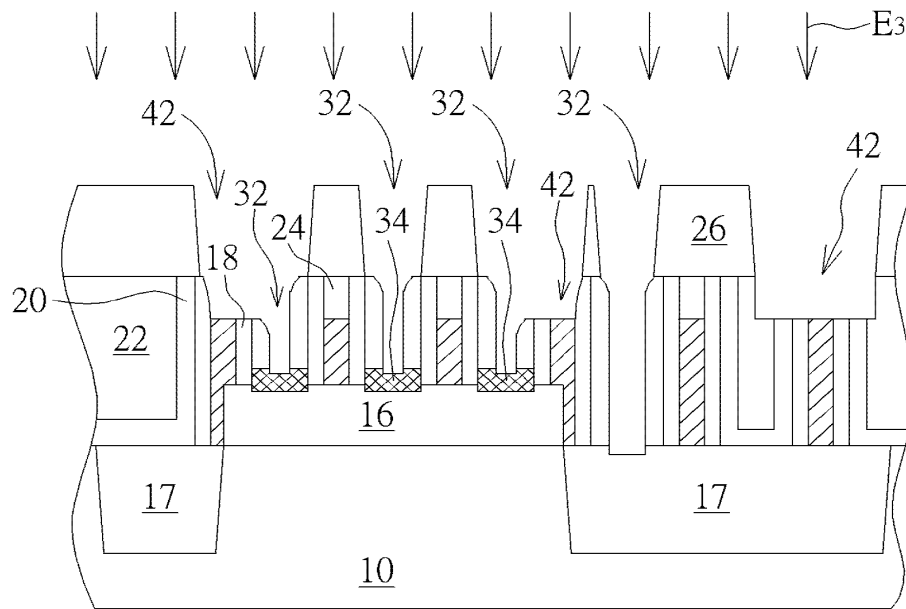


FIG. 7

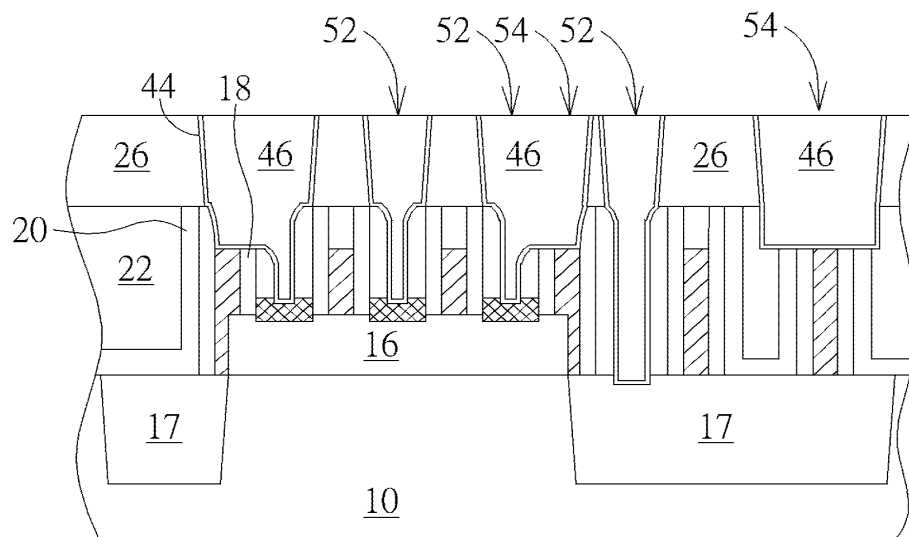


FIG. 8

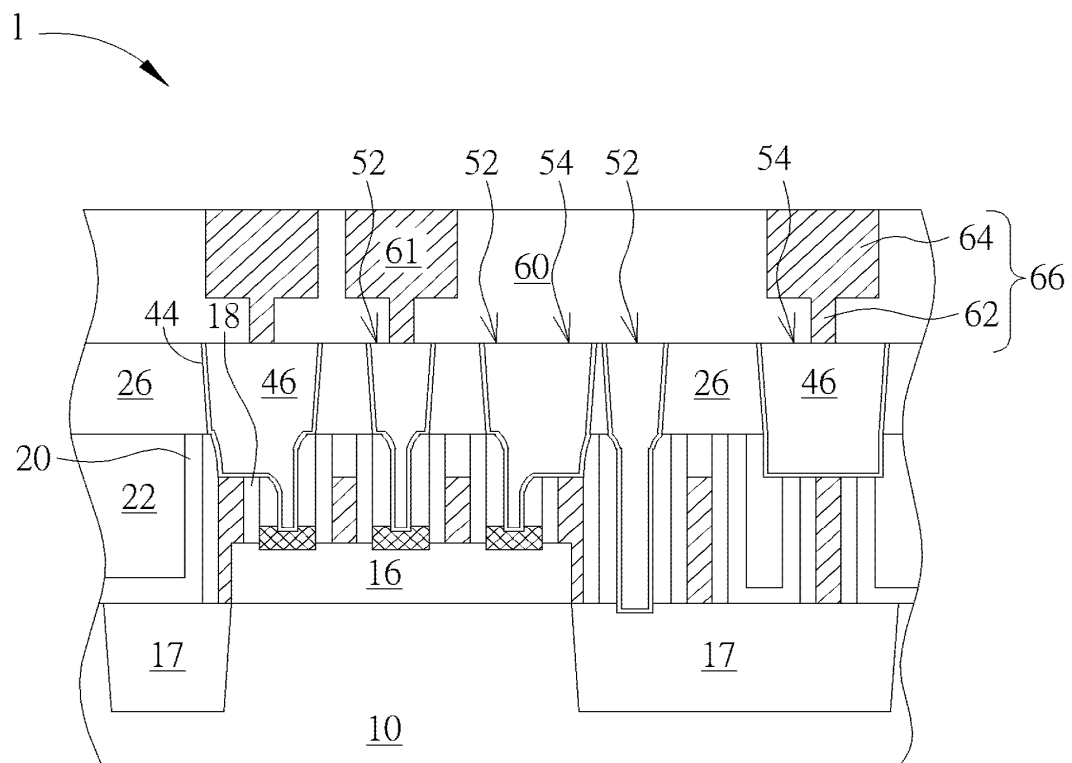


FIG. 9

Abstract of Disclosure

The present invention provides a manufacturing method of a semiconductor structure, comprising the following steps. First, a substrate is provided, a first dielectric layer is formed on the substrate, a metal gate is disposed in the first dielectric layer and at least one source/drain region (S/D region) is disposed on two sides of the metal gate, a second dielectric layer is then formed on the first dielectric layer, a first etching process is then performed to form a plurality of first trenches in the first dielectric layer and the second dielectric layer, wherein the first trenches expose each S/D region. Afterwards, a salicide process is performed to form a salicide layer in each first trench, a second etching process is then performed to form a plurality of second trenches in the first dielectric layer and the second dielectric layer, and the second trenches expose the metal gate.

Claims

What is claimed is:

1. A semiconductor structure, comprising:
 - a substrate;
 - a first dielectric layer disposed on the substrate;
 - a metal gate disposed in the first dielectric layer;
 - a source/drain region (S/D region) disposed on two sides of the metal gate; and
 - a hard mask disposed on the metal gate, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.
2. The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.
3. The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.
4. The semiconductor device of claim 2, further comprising a plurality of first contacts disposed in the first dielectric layer and in the second dielectric layer that are electrically connected to parts of the S/D region, wherein each first contact is a monolithically formed structure.
5. The semiconductor device of claim 4, further comprising a plurality of second contacts disposed in the first dielectric layer and in the second dielectric layer that are electrically connected to parts of the metal gate, wherein each second contact is a monolithically formed structure.
6. The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.
7. The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.
8. The semiconductor device of claim 5, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

9. The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

10. A manufacturing method of a semiconductor device, at least comprising the following steps:

providing a substrate, wherein a first dielectric layer is formed on the substrate, at least one metal gate is formed in the first dielectric layer and at least one source drain region (S/D region) is disposed on two sides of the metal gate;

forming a second dielectric layer on the first dielectric layer;

performing a first etching process to form a plurality of first trenches in the first dielectric layer and the second dielectric layer, wherein each first trench exposes each S/D region;

performing a salicide process to form a salicide layer in each first trench; and

performing a second etching process to form a plurality of second trenches in the first dielectric layer and the second dielectric layer, wherein each first trench exposes each metal gate.

11. The method of claim 10, further comprising forming a hard mask on the top surface of each metal gate after the first dielectric layer is formed.

12. The method of claim 11, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

13. The method of claim 10, further comprising forming at least one fin structure on the substrate.

14. The method of claim 10, wherein parts of the second trenches and parts of the first trenches partially overlap each others.

15. The method of claim 10, further comprising filling a metal layer in each first trench and each second trench simultaneously to form a plurality of first contacts and a plurality of second contacts respectively.

16. The method of claim 15, further comprising forming a plurality of third contacts

electrically connected to parts of the first contacts or parts of the second contacts, wherein each third contact is a monolithically formed structure.

17. The method of claim 16, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

18. The method of claim 10, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

19. The method of claim 11, wherein when performing the first etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is larger than 5.

20. The method of claim 11, wherein when performing the second etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is smaller than 5.

Title

SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

Background of the Invention

1. Field of the Invention

[0001] The present invention relates generally to semiconductor manufacturing process, and more specifically, to a method using a hard mask on the metal gate to form contacts structure simultaneously during a plurality of etching processes.

2. Description of the Prior Art

[0002] Along with the continuous miniaturization of the Integrated Circuits (IC), the line width of interconnections and the feature size of semiconductor devices have continuously shrunk. In general, discrete devices in integrated circuits are connected to each other through contact plugs (or contact slots) and interconnection structures, and their related fabrication methods have become an important matter in the next-generation semiconductor devices.

[0003] In current fabricating processes, due to the limitations of the back end of the line (BEOL) process capacity, the yield of contact plugs with high aspect ratio (HAR) is relatively low and cannot reach the new requirements. In order to overcome this drawback, a double patterning technique, generally including two photolithographic and two etching processes (2P2E) has been invented in order to fabricate required device patterns. Generally, a contact is divided into two parts, a lower contact structure and an upper contact structure (i.e. the metal level zero, M0). After the lower contact structure is formed completely, the M0 is continuously formed. The M0 can be a pole structure or a slot structure. However, since the upper contact structure (M0) and the lower contact structure are formed in different steps, a barrier layer will exist between the upper contact structure (M0) and the lower contact structure, thereby affecting the conductivity of the contact. Besides, the manufacturing process is too complex.

[0004] Accordingly, in order to overcome the above-mentioned drawbacks, there is a need to provide a modified method for fabricating interconnection structures with better yields.

Summary of the Invention

[0005] To solve the issues mentioned above, the present invention provides a semiconductor device comprising a substrate, a first dielectric layer disposed on the substrate, a metal gate disposed in the first dielectric layer, a source/drain region (S/D region) disposed on two sides

of the metal gate, and a hard mask disposed on the metal gate, wherein the top surface of the hard mask and the top of the first dielectric layer are on the same level.

[0006] The present invention further comprises a manufacturing method for forming the semiconductor device at least comprising the following steps: first, a substrate is provided, a first dielectric layer is formed on the substrate, a metal gate is disposed in the first dielectric layer and at least one source/drain region (S/D region) is disposed on two sides of the metal gate; a second dielectric layer is then formed on the first dielectric layer, a first etching process is then performed, to form a plurality of first trenches in the first dielectric layer and the second dielectric layer, wherein the first trenches expose each S/D region. Afterwards, a salicide process is performed to form a salicide layer in each first trench; a second etching process is then performed to form a plurality of second trenches in the first dielectric layer and the second dielectric layer, and the second trenches expose the metal gate.

[0007] The present invention further comprises a hard mask on the metal gate, and uses etching gases with different etching rates to selectively etch the hard mask and the dielectric layer disposed above. In this way, the contacts disposed correspondingly to the metal gate and the contacts disposed correspondingly to the S/D region can be formed simultaneously, and replace the 0th metal layer (M0) and the lower contact structure in a conventional process, thereby reducing the manufacturing steps.

[0008] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0009] FIGS.1-9 are schematic diagrams illustrating a manufacturing method of the FinFET semiconductor device according to a first preferred embodiment of the present invention.

Detailed Description

[0010] To provide a better understanding of the present invention to users skilled in the technology of the present invention, preferred embodiments are detailed as follows. The preferred embodiments of the present invention are illustrated in the accompanying drawings with numbered elements to clarify the contents and effects to be achieved.

[0011] Please note that the figures are only for illustration and the figures may not be to scale.

The scale may be further modified according to different design considerations. When referring to the words “up” or “down” that describe the relationship between components in the text, it is well known in the art and should be clearly understood that these words refer to relative positions that can be inverted to obtain a similar structure, and these structures should therefore not be precluded from the scope of the claims in the present invention.

[0012] Please refer to FIGS.1~9 are schematic diagrams illustrating a manufacturing method of the FinFET semiconductor device according to a first preferred embodiment of the present invention. As shown in FIG.1, a substrate 10 is first provided, wherein the substrate 10 comprises at least one metal gate 12 disposed on the substrate 10 and at least one source/drain region (S/D region) 14 disposed on two sides of the metal gate 12. Besides, the substrate 10 selectively comprises at least one fin structure 16. In this embodiment, the metal gate 12 comprises metal materials, the S/D region 14 can be formed on two sides of the metal gate 12 of the substrate 10 through an ion implantation process, or formed on the fin structure 16 disposed on two sides of the metal gate 12. The method of the present invention further comprises forming at least one shallow trench isolation (STI) 17 in the substrate 10 surrounding the metal gate 12, to isolate the metal gate 12 from the fin structures 16 and others electric elements on the substrate 10. In this embodiment, the metal gate may cross the fin structure disposed on the substrate 10 (such as the metal gate 12a shown in FIG.1), or be disposed on the STI 17 (such as the metal gate 12c shown in FIG.1) and be used as a dummy gate, or may disposed on the edge of the fin structure 16 to protect the fin structure 16 (such as the metal gate 12b shown in FIG.1).

[0013] In addition, the method of the present invention further comprises selectively forming an epoxy layer 15 on the S/D region 14. Afterwards, a spacer 18 and a contact etching stop layer (CESL) 20 may be formed on two sides of the metal gate 12. A first dielectric layer 22 is then formed on the substrate 10, and a planarization process is then performed, such as a chemical mechanical polishing (CMP), to have the top surface of the metal gate 12 and the top surface of the first dielectric layer 22 on the same level. It is worth noting that in this embodiment, an etching process is performed after the metal gate 12 is completed, to remove parts of the metal gate 12, and a hard mask 24 is then formed to replace the upper portion of the metal gate 12. Another planarization process is then performed to remove the extra hard mask 24. In other words, in the present embodiment, a hard mask 24 is disposed on the top of the metal gate 12, and the top surface of the hard mask 24 and the top surface of the first dielectric layer 22 are on the same level. Besides, since the hard mask 24 replaces some top portion of the metal gate 12,

the hard mask 24 is therefore disposed only on the metal gate 12, and disposed between the spacers 18. In addition, since parts of the spacer 18 and parts of the CESL 20 are removed during another planarization process, so the spacer 18 and the CESL 20 have a truncated top surface. In the present embodiment, the spacer 18, the CESL 20 and the hard mask 24 mainly comprise silicon nitride, and the first dielectric layer 22 mainly comprises silicon oxide, but not limited thereto. These elements and the manufacturing methods thereof are well known to persons of ordinary skills in the art and the details will not be described here.

[0014] As shown in FIG.2, a second dielectric layer 26 is then formed on the first dielectric layer 22. According to the preferred embodiment, the photoresist layer 28 sequentially includes an organic dielectric layer (ODL) 28a, a silicon-containing hard mask bottom anti-reflecting coating (SHB) 28b and a photoresist (PR) layer 28c. In short, the photoresist layer 28 is a tri-layer structure consisting of an ODL/SHB/PR structure, but not limited thereto. Afterwards, in order to form the metal plug that is electrically connected to the S/D region 14 (wherein the metal plug can replace the M0 and the lower contacts structure electrically connected to the S/D region in conventional process, denoted here as the 0th metal contact, M0CT), a photo-etching process is performed to pattern the photoresist layer 28c and to form a plurality of openings 30, wherein each opening 30 is at least disposed correspondingly to the S/D region 14 disposed below, but not limited thereto. Parts of the openings 30 may be disposed correspondingly to the STI 17 surrounding the metal gate 12 to reduce the pattern density difference between the region including the transistor (mainly comprising the metal gate 12, the S/D region 14 and the fin structure 16) and the periphery region.

[0015] Afterwards, as shown in FIGS.3~4, at least one etching process E1 is performed to transfer the pattern to others layer disposed below, wherein the etching process E1 comprises: from top to bottom, etching the SHB 28b, the ODL 28a, the second dielectric layer 26 and the first dielectric layer 22 in sequence, until exposing the CESL 20. As shown in FIG.4, another etching process E2 is then performed, parts of the CESL 20 are removed to expose the epoxy layer 15 disposed below and to form a plurality of first trenches 32, wherein each first trench 32 exposes the epoxy layer 15. It is worth noting that since the epoxy layer is selectively formed, each first trench 32 may therefore directly expose the S/D region 14. Besides, according to different embodiments, parts of the first trenches 32 may be disposed on STI 17.

[0016] The etching process of the present invention uses etching gases, which may comprise per fluorocarbon gases, such as tetrafluoromethane (CF₄), fluoroform (CHF₃), hexafluoride- 1,3

+ butadiene (C₄F₆), and further comprises oxygen and argon, but not limited thereto. It is worth noting that the higher the ratio of per fluorocarbon gases to oxygen in the etching gas is, the higher the selectivity of the silicon nitride to silicon oxide will be. In other words, the more per fluorocarbon gases are present in the etching gas, the faster the etching rate will be for etching the silicon nitride, compared with the etching rate for etching the silicon oxide. In this embodiment, the main material of the first dielectric layer 22 and the second dielectric layer 26 is silicon oxide, the main material of the CESL 20 is silicon nitride, and the etching gas in etching process E1 is a high selectivity gas (to silicon nitride and silicon oxide), and the selectivity is preferably larger than 5, so the etching rate for etching the second dielectric layer 26 and etching the first dielectric layer 22 will be relatively fast, but the etching rate for etching the CESL 20 is relatively slow when the etching process E1 is performed. The etching rate for etching the second dielectric layer 26 and etching the first dielectric layer 22 is at least five times higher than the etching rate for etching the CESL 20, so the CESL 20 is not easily etched through during the etching process E1, and the etching will stop on the surface of the CESL 20. Afterwards, the etching gas is adjusted for the etching process E2, and the CESL 20 disposed on the bottom of the first trenches 32 will be removed during the etching process E2.

[0017] As shown in FIG.5, a salicide (self-aligned silicide) process is performed to the epoxy layer 15 to form a salicide layer 34 on the bottom of the first trenches 32. The salicide process mainly comprises filling a metal layer (not shown) in each first trench 32, and a thermal process is then performed to form a salicide layer 34 on the interface between the metal layer and the silicon-containing surface. Afterwards, the metal layer disposed in the first trenches 32 is removed. It is worth noting that since the salicide layer 34 is only formed on the silicon-containing surface, it may therefore be formed on the fin structure 16, on the epoxy layer 15 or on the substrate 10, but will not be formed on the STI 17.

[0018] As shown in FIG.6, a photoresist layer 38 is then formed, wherein the material of the photoresist layer 38 may be the same as the material of the photoresist layer 28, comprising an organic dielectric layer (ODL) 38a, a silicon-containing hard mask bottom anti-reflecting coating (SHB) 38b and a photoresist layer 38c. Afterwards, in order to form the metal plug that is electrically connected to the metal gate 12 (wherein the metal plug can replace the M0 and the lower contacts structure electrically connected to the metal gate in conventional process, denoted here as the 0th metal gate contact, M0PY), a photo-etching process is performed to pattern the photoresist layer 38c and to form a plurality of openings 40, wherein each opening 40 is at least disposed correspondingly to the metal gate 12, but not limited thereto. Parts of the opening 40

may be disposed correspondingly to the STI 17.

[0019] As shown in FIG.7, an etching process E3 is then performed to transfer the pattern to other layers disposed below, wherein the etching process E3 comprises etching in sequence from top to bottom: the SHB 38b, the ODL 38a, the second dielectric layer 26 and the hard mask 24. It is worth noting that in the etching process E3, the volume ratio of the per fluorocarbon gases to oxygen is adjusted to have an etching rate for etching the silicon nitride similar to the etching rate for etching the silicon oxide. In other words, the etching gas used in the etching process E3 has a low-selectivity for the silicon nitride and silicon oxide (the selectivity is preferably smaller than 5), so the etching gas can therefore remove the silicon nitride and remove the silicon oxide simultaneously. After the etching process E3 is performed, the top of the metal gate 12 can be exposed, besides, a plurality of second trenches 42 can be formed. Afterwards, the remaining photoresist layer and the ODL 38a disposed in the first trenches 32 or in the second trenches 42 can be removed through an ash process or other suitable processes.

[0020] As shown in FIG.8, a barrier layer 44 and a metal layer 46 are filled in each first trench 32 and each second trench 42 simultaneously, wherein the barrier layer 44 may comprise titanium nitride (TiN), tantalum nitride (TaN) or Ti/TiN multiple barrier layers to improve the adhesivity between the inner surface of each trench and the metal layer formed in the following steps. The metal layer 46 preferably comprises tungsten (W) that has better gap fill performances. A planarization process is then performed to remove the extra barrier layer and the metal layer disposed on the top surface of the second dielectric layer 26 to simultaneously form a plurality of first contacts 52 and a plurality of second contacts 54 in the first dielectric layer 22 and in the second dielectric layer 26, wherein each first contact 52 at least is electrically connected to parts of the S/D region 14 (in other words, the first contacts 52 of the present embodiment are the M0CT mentioned above), each second contact 54 is at least electrically connected to parts of the metal gate 12 (in other words the second contacts 54 of the present embodiment are the M0PY mentioned above). In addition, since the first contacts 52 and the second contacts 54 are filled by the metal layer 46 and completed simultaneously, each first contact 52 and each second contact 54 is a monolithically formed structure. It is worth noting that in the present invention, parts of the second trenches 42 and parts of the first trenches 32 are partially overlapped, so parts of the first contact 52 will be connected to parts of the second contacts 54 (such as the second contact 54A shown in FIG.8). These connection portions of the first contacts 52 and the second contacts 54 may be used as share contacts of a semiconductor device, but not limited thereto.

[0021] As shown in FIG.9, a metal interconnect process is performed, comprising forming a third dielectric layer 60 on the top of the second dielectric layer 26, wherein the third dielectric layer 60 is like the inter metal dielectric (IMD) in conventional technology, and forming a plurality of via holes (not shown) and a plurality of trace patterns (not shown) through an etching process or other methods. Finally, a metal layer 61 is simultaneously filled in each via hole and each trace pattern, and a planarization process is performed to remove the extra metal layer on the surface of the third dielectric layer 60 to complete a plurality of via hole structures 62 and a plurality of trace structures 64 simultaneously. In this embodiment, the via hole structures 62 and the corresponding trace structures 64 can be regarded as third contacts 66, wherein each third contact 66 is a monolithically formed structure. Each via hole structure 62 directly contacts the first contacts 52 or the second contacts 54 disposed below along a vertical direction. The trace structures 64 are on a same level, and electrically connected to others elements along a horizontal direction. The via hole structures 62 may have rectangular, circular or other block shapes, and the trace structures 64 may be lines or have striped shapes when viewed from top views, but not limited thereto.

[0022] It is worth noting that in the manufacturing process mentioned above, the first trenches 32 are formed before the second trenches 42 are formed, however, the present invention is not limited thereto. In another embodiment of the present invention, a low-selectivity etching gas may be used to form the second trenches 42, and a high-selectivity etching gas is then used to form the first trenches 32. A barrier layer 44 and a metal layer 46 are then filled into the first trenches 32 and the second trenches 42. A planarization process is then performed to complete a plurality of first contacts 52 and a plurality of second contacts 54. This manufacturing sequence should be comprised in the scope of the present invention.

[0023] A semiconductor device 1 of the present invention can be formed through the manufacturing process mentioned above, wherein the final structure is shown in FIG.9. Please refer to FIGS.1~9. The semiconductor device 1 at least comprises a substrate 10, a first dielectric layer 22 disposed on the substrate 10, a metal gate 12 disposed in the first dielectric layer 22, a S/D region 14 disposed on two sides of the metal gate 12, and a hard mask 24 disposed on the metal gate 12, wherein the top surface of the hard mask 24 and the top of the first dielectric layer 22 are on the same level, a second dielectric layer 26 disposed on the first dielectric layer 22. The present invention further comprises a plurality of first contacts 52 disposed in the first dielectric layer 22 and in the second dielectric layer 26 electrically connected to parts of the S/D region 14, wherein each first contact 52 is a monolithically formed structure, and a plurality of second

contacts 54 disposed in the first dielectric layer 22 and in the second dielectric layer 26 electrically connected to parts of the metal gate 12, wherein each second contact 54 is a monolithically formed structure. In addition, the semiconductor device 1 selectively comprises the following components: an epoxy layer 15 disposed on the S/D region 14, a STI 17 disposed in the substrate 10 surrounding the metal gate 12, at least a spacer 18 and at least a CESL 20 disposed on two sides of the metal gate 12, wherein both of the two elements have a truncated top surface, a fin structure 16 disposed on the substrate 10, a salicide layer 34 disposed between each S/D region 14 and each first contact 52, a third dielectric layer 60 disposed on the second dielectric layer 26, and a plurality of third contacts 66 disposed on parts of the first contacts 52 or on parts of the second contacts 54, wherein each third contact 66 is a monolithically formed structure, and each third contact 66 comprises a via hole structure 62 and a trace structure 64, wherein each via hole structure 62 and each trace structure 64 comprise the same material, and contact each other. The other components, material properties, and manufacturing methods of the semiconductor device 1 are similar to those of the first preferred embodiment detailed above and will not be redundantly described.

[0024] In summary, the present invention comprises a hard mask on a metal gate, and uses etching gases with different etching rates to selectively etch the hard mask and the dielectric layer disposed above. Therefore, contacts disposed correspondingly to the metal gate and contacts disposed correspondingly to the S/D region can be formed simultaneously, and replace the 0th metal layer (M0) and the lower contact structures of conventional process, thereby reducing the manufacturing steps.

[0025] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						
	1							

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott Margo/	Date (YYYY-MM-DD)	2013-05-02
Name/Print	Scott Margo	Registration Number	56277

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1622USA
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Ching-Wen		Hung		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tainan City	Country of Residence i	TW		
Mailing Address of Inventor:					
Address 1		No.12, Aly. 9, Ln. 872, Ziqiang Rd., Yongkang Dist.			
Address 2					
City	Tainan City	State/Province			
Postal Code			Country i	TW	
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chih-Sen		Huang		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Tainan City	Country of Residence i	TW		
Mailing Address of Inventor:					
Address 1		No.476, Longmujiang Rd., Shanhua Dist.			
Address 2					
City	Tainan City	State/Province			
Postal Code			Country i	TW	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

Correspondence Information:

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1622USA
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence Information of this application.

Customer Number	27765		
Email Address	scottmargo@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		
Attorney Docket Number	NAUP1622USA	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	5	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.			
Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1622USA
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1622USA
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1				Remove	
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.					
Clear					
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117		☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.			☐ Person who shows sufficient proprietary interest		
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:					
Name of the Deceased or Legally Incapacitated Inventor :					
If the Applicant is an Organization check here. ☒					
Organization Name		UNITED MICROELECTRONICS CORP.			
Mailing Address Information:					
Address 1		No.3, Li-Hsin Road 2,			
Address 2		Science-Based Industrial Park			
City		Hsin-Chu City	State/Province		
Country ⁱ		TW	Postal Code		
Phone Number			Fax Number		

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1622USA
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1				
Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).				
				Remove
If the Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee Data may be generated within this form by selecting the Add button.				Add

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Scott Margo/			Date (YYYY-MM-DD)	2013-05-02
First Name	Scott	Last Name	Margo	Registration Number	56277
Additional Signature may be generated within this form by selecting the Add button.					Add

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1622USA
		Application Number	
Title of Invention	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

27765

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

27765

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

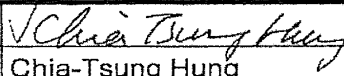
Assignee Name and Address:

UNITED MICROELECTRONICS CORP.
No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	SEP 26 2012
Name	Chia-Tsung Hung	Telephone	+886-3-5782258
Title	CHAIRMAN		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

NAU.0

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: UNITED MICROELECTRONICS CORP.

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

UNITED MICROELECTRONICS CORP., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Scott Margo/

05/02/2013

Signature

Date

Scott Margo

56277

Printed or Typed Name

Title or Registration Number

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application number _____ filed on _____, or
- ☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this APR 25 2013. (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1622USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Ching-Wen Hung**

Date: **APR 25 2013**

Signature: Ching-Wen Hung

NPO#NAU-PI622-USA:0
CUST#UMCD-2012-0430

Page 2 of 4

F#NPO-P0002E-US1201
DSC0-102U001135

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

As the below named inventor, I hereby declare that:
This declaration is directed to:

- ☒ The attached application, or
☐ United States application number _____ filed on _____, or
☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

I hereby sell, assign and transfer to ASSIGNEE and the successors and assignees of the ASSIGNEE the entire right, title and interest in and to any and all improvements which are disclosed in the invention as above-identified application and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof.

I hereby covenant that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

I further covenant that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to I and will testify as to the same in any interference, litigation proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal

representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.

IN WITNESS WHEREOF, I have hereunto set hand and seal this APR 25 2013 (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1622USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chih-Sen Huang**

Date: **APR 25 2013**

Signature:

Chih-Sen Huang

NPO#NAU-P1622-USA:0
CUST#UMCD-2012-0430

Page 4 of 4

F#NPO-P0002E-US1201
DSC0-102U001135

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		
First Named Inventor/Applicant Name:		Ching-Wen Hung		
Filer:		Winston Hsu/Sandra Yen		
Attorney Docket Number:		NAUP1622USA		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	15670075
Application Number:	13875293
International Application Number:	
Confirmation Number:	7170
Title of Invention:	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Ching-Wen Hung
Customer Number:	27765
Filer:	Winston Hsu/Shelley Kuo
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1622USA
Receipt Date:	02-MAY-2013
Filing Date:	
Time Stamp:	03:49:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	7673
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Authorization to access Appl. by Trilateral Office	1635149.PDF	37518	no	1
			cb0f17309ba75beee4601e939c2b5dc329f9a3bd		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	1633934.PDF	104263	no	5
			5ede2db664c625e7ca7c4ab80f77fada5a65054d		
Warnings:					
Information:					
3	Abstract	1633933.PDF	36268	no	1
			80c4bdec9a24553c0e6e0881fe2a3a5d41c6f40f		
Warnings:					
Information:					
4	Claims	1633932.PDF	43353	no	3
			57caf656d1bee9147c79ee19f2caf8bd9a68e478		
Warnings:					
Information:					
5	Specification	1633931.PDF	111730	no	8
			3938902e4181869e41e6697b7000b6f656a940879		
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Form (SB08)	1635150.PDF	42258	no	7
			962cb6cb8dba1e96393c2f00423b53868e9136dd		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
7	Application Data Sheet	1635159.PDF	1619409	no	7
			b32421cd2cd67ca57e9bbea621ca888aed2dd3		
Warnings:					
Information:					

8	Oath or Declaration filed	1634037.PDF	144935 10ac1ee041e5bf6f61d398fb7deac252b5a7ed9	no	4
Warnings:					
Information:					
9	Power of Attorney	1634036.pdf	1507680 b2ff12275218a844d14c6efc4b1d6665f43b4c6	no	7
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	32904 1ce96691bbc85d6fe7046abd9d26f8f9b17c583b	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			3680318		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

As the below named inventor, I hereby declare that:
This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application number _____ filed on _____, or
- ☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In consideration of the payment by **UNITED MICROELECTRONICS** having a postal address of **CORP.**

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

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IN WITNESS WHEREOF, I have hereunto set hand and seal this APR 25 2013. (Date of signing)

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1622USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Ching-Wen Hung**

Date: **APR 25 2013**

Signature: Ching-Wen Hung

NPO#NAU-P1622-USA:0
CUST#UMCD-2012-0430

Page 2 of 4

F#NPO-P0002E-US1201
DSC0-102U001135

**COMBINE DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION
USING AN APPLICATION DATA SHEET (37 CFR 1.76) AND ASSIGNMENT**

Title of Invention:

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This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application number _____ filed on _____, or
- ☐ PCT international application number _____ filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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In consideration of the payment by **UNITED MICROELECTRONICS CORP.** having a postal address of _____

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

(referred to as "ASSIGNEE" below) to I of the sum of One Dollar (\$ 1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

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Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use this form for each additional inventor.

Docket No NAUP1622USA

LEGAL NAME OF INVENTOR(ASSIGNOR)

Inventor: **Chih-Sen Huang**

Date: **APR 25 2013**

Signature: Chih-Sen Huang

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/875,293	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)
	Total (37 CFR 1.16(i))	*	**	=	x	=	x
	Independent (37 CFR 1.16(h))	*	***	=	x	=	x
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE		TOTAL ADD'L FEE
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)
	Total (37 CFR 1.16(i))	*	**	=	x	=	x
	Independent (37 CFR 1.16(h))	*	***	=	x	=	x
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE		TOTAL ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/875,293	05/02/2013	2812	1600	NAUPI622USA	20	2

CONFIRMATION NO. 7170

27765

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

FILING RECEIPT



0000000061711152

Date Mailed: 06/12/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Ching-Wen Hung, Tainan City, TAIWAN;
Chih-Sen Huang, Tainan City, TAIWAN;

Applicant(s)

UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN

Assignment For Published Patent Application

UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 06/03/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/875,293**

Projected Publication Date: 11/06/2014

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA

CONFIRMATION NO. 7170

POA ACCEPTANCE LETTER

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116



Date Mailed: 06/12/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/02/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/ldvan/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA	7170

27765 7590 08/06/2014
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

HUYNH, ANDY

ART UNIT	PAPER NUMBER
----------	--------------

2818

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

08/06/2014

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 13/875,293	Applicant(s) HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☐ Claim(s) _____ is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☒ Claim(s) 1-20 are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____ | 4) ☐ Other: _____ |

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Claims **1-20** are pending in the application.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims **1-9**, drawn to a device, classified in class 257, subclass 365.
- II. Claims **10-20**, drawn to a method, classified in class 438, subclass 284.

The inventions are distinct, each from the other because of the following reasons:

Inventions of II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by the processes materially different from those of the group II invention, for instance, in Claim **10**, selectively depositing process may be used to form a plurality of trenches in the first dielectric layer and the second dielectric layer instead of using etching process.

Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a

serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable on the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and the product claims are subsequently found allowable, withdrawn process claims that depend from or otherwise require all the limitations of the allowable product claim will be considered for rejoinder. All claims directed to a nonelected process invention must require all the limitations of an allowable product claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101,102,

103 and 112. Until all claims to the elected product are found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained.

Withdrawn process claims that are not commensurate in scope with an allowable product claim will not be rejoined. See MPEP § 821.04(b). Additionally, in order to retain the right to rejoinder in accordance with the above policy, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272-1781. The examiner can normally be reached on Monday-Friday from 6:30 AM to 3:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

Art Unit: 2818

applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andy Huynh/
Primary Examiner, Art Unit 2818

<i>Index of Claims</i> 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	07/31/2014								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
	7	÷								
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	20	÷								

**SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD
THEREOF**

Appl. No.	: 13/875,293	Confirmation No.	7170
First Named Inventor	: Ching-Wen Hung		
Filed	: May 2, 2013		
TC/A.U.	: 2818		
Examiner	: Huynh, Andy		
Docket No.	: NAUP1622USA		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

- 5 In response to the Office action of August 06, 2014, please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

- 10 **Remarks/Arguments** begin on page 7 of this paper.

Amendments to the Claims:

Listing of Claims:

1. (original) A semiconductor structure, comprising:
 - a substrate;
 - 5 a first dielectric layer disposed on the substrate;
 - a metal gate disposed in the first dielectric layer;
 - a source/drain region (S/D region) disposed on two sides of the metal gate;
 - and
 - a hard mask disposed on the metal gate, wherein the top surface of the hard
 - 10 mask and the top surface of the first dielectric layer are on the same level.
- 2.(original) The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.
- 15 3.(original) The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.
- 4.(original) The semiconductor device of claim 2, further comprising a plurality
- 20 of first contacts disposed in the first dielectric layer and in the second dielectric layer that are electrically connected to parts of the S/D region, wherein each first contact is a monolithically formed structure.
- 5.(original) The semiconductor device of claim 2, further comprising a plurality
- 25 of second contacts disposed in the first dielectric layer and in the second dielectric layer that are electrically connected to parts of the metal gate, wherein each second contact is a monolithically formed structure.
- 6.(original) The semiconductor device of claim 1, further comprising at least one
- 30 fin structure disposed on the substrate.

7.(original) The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

5 8.(original) The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

9.(original) The semiconductor device of claim 8, wherein each third contact
10 comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

10.(withdrawn) A manufacturing method of a semiconductor device, at least comprising the following steps:

15 providing a substrate, wherein a first dielectric layer is formed on the substrate, at least one metal gate is formed in the first dielectric layer and at least one source drain region (S/D region) is disposed on two sides of the metal gate;

 forming a second dielectric layer on the first dielectric layer;

 performing a first etching process to form a plurality of first trenches in the
20 first dielectric layer and the second dielectric layer, wherein each first trench exposes each S/D region;

 performing a salicide process to form a salicide layer in each first trench;

and

 performing a second etching process to form a plurality of second trenches
25 in the first dielectric layer and the second dielectric layer, wherein each first trench exposes each metal gate.

11.(withdrawn) The method of claim 10, further comprising forming a hard mask on the top surface of each metal gate after the first dielectric layer is formed.

30

12.(withdrawn) The method of claim 11, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

13.(withdrawn) The method of claim 10, further comprising forming at least one
5 fin structure on the substrate.

14.(withdrawn) The method of claim 10, wherein parts of the second trenches and parts of the first trenches partially overlap each others.

10 15.(withdrawn) The method of claim 10, further comprising filling a metal layer in each first trench and each second trench simultaneously to form a plurality of first contacts and a plurality of second contacts respectively.

15 16.(withdrawn) The method of claim 15, further comprising forming a plurality of third contacts electrically connected to parts of the first contacts or parts of the second contacts, wherein each third contact is a monolithically formed structure.

17.(withdrawn) The method of claim 16, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace
20 structure comprise the same material and contact each other directly.

18.(withdrawn) The method of claim 10, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top
25 surface.

19.(withdrawn) The method of claim 11, wherein when performing the first etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is larger than 5.

30 20.(withdrawn) The method of claim 11, wherein when performing the second

Appl. No. 13/875,293
Reply to Office action of August 06, 2014

etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is smaller than 5.

Appl. No. 13/875,293
Reply to Office action of August 06, 2014

Amendments to the Specification:

Please replace the original title with the following new title:

“SEMICONDUCTOR STRUCTURE”

Electronic Acknowledgement Receipt	
EFS ID:	19962041
Application Number:	13875293
International Application Number:	
Confirmation Number:	7170
Title of Invention:	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Ching-Wen Hung
Customer Number:	27765
Filer:	Winston Hsu/Connie Chen
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1622USA
Receipt Date:	26-AUG-2014
Filing Date:	02-MAY-2013
Time Stamp:	05:20:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2041118.PDF	624171 afd382b42dd9870afedcab078cf30738fa29eb6	no	2

Warnings:

Information:

2	Response to Election / Restriction Filed	2041117.PDF	76345 3077346c5e22243a5301841fb7a606d86bd ba765	no	1
Warnings:					
Information:					
3	Claims	2041116.PDF	81711 885ff71ceabd187f428378223d49a2ff9e23 723	no	4
Warnings:					
Information:					
4	Specification	2041114.PDF	75614 ccbf16a72a1bd69a9395cbe2c01698e2cb2 25afb	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			857841		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record
5 in the application file.

1. Election/Restriction

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9, drawn to a device, classified in class 257, subclass 365.

10 ***II. Claims 10-20, drawn to a method, classified in class 438, subclass 284.***

The inventions are distinct, each from the other because of the following reasons:

*Inventions of II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the
15 product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by the processes materially different from those of the group II invention, for instance, in Claim 10, selectively depositing process may be used to form a
20 plurality of trenches in the first dielectric layer and the second dielectric layer instead of using etching process.*

Response:

Applicant hereby elects **invention I** in response to the above restriction
25 requirement. The claims readable upon the elected invention I are claims 1-9. Claims 10-20 are withdrawn, and no new matter is introduced by this amendment.

2. Amendment to Title of the Invention:

The original title has been amended to be descriptive to the invention. The
30 original title, "SEMICONDUCTOR STRUCTURE AND MANUFACTURING

METHOD THEREOF” is now more descriptively entitled as, “SEMICONDUCTOR STRUCTURE”. No new matter is introduced.

5 Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

/Scott Margo/

Date: 08/26/2014

10 Scott Margo, Patent Agent No. 56,277
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : ScottMargo@naipo.com

15 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/875,293	Filing Date 05/02/2013	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	(Column 4)	RATE (\$)	ADDITIONAL FEE (\$)
	08/26/2014	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	* 20	Minus ** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus *** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	0
		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	*	Minus **	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus ***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LYNNELL JOHNSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PLUS Search Results for S/N 13875293, Searched Thu Aug 28 14:56:41 EDT 2014
The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

5760429 99	4449285 98
6022804 99	
5661061 99	
5976391 99	
5326670 99	
5482784 99	
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5360763 98	
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA	7170

27765 7590 09/23/2014
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

HUYNH, ANDY

ART UNIT	PAPER NUMBER
----------	--------------

2818

NOTIFICATION DATE	DELIVERY MODE
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09/23/2014

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 13/875,293	Applicant(s) HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08/26/14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) 10-20 is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-9 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 05/02/13 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date <u>05/02/13</u> | 4) ☐ Other: _____ |

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Election/Restrictions

This is responsive to Applicant's Response to Restriction Requirement and Amendment filed August 26, 2014. By the Response and Amendment, Applicant has elected without traverse the Invention **I**, including Claims **1-9**, for examination on the merits. The title has been amended. Accordingly, Claims **10-20** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 05/02/13 made of record. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claims **1 and 6** are rejected under 35 U.S.C. 102(a)(2) as being anticipated by US 2014/0048888 to Chen et al. hereinafter as “Chen.”

Regarding Claim **1**, Chen discloses a semiconductor structure, comprising:

a substrate 202;

a first dielectric layer 228 disposed on the substrate 202;

a metal gate 214 disposed in the first dielectric layer 228;

a source/drain region (S/D region) 208 disposed on two sides of the metal gate 214;

and

a hard mask 216 disposed on the metal gate 214, wherein the top surface of the hard mask 216 and the top surface of the first dielectric layer 228 are on the same level (Fig. 12, ¶¶ [0009]-[0034]).

Regarding Claim **6**, Chen discloses the semiconductor device further comprising at least one fin structure 212 disposed on the substrate 202 (Fig. 12).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **2-5 and 7-9** are rejected under 35 U.S.C. 103 as being unpatentable over US 2014/0048888 to Chen et al. hereinafter as “Chen” as applied to claim **1** above, and further in view of US 2013/0154022 to Chung et al. hereinafter as “Chung.”

Regarding Claim **2**, Chen does not disclose the semiconductor device further comprising a second dielectric layer disposed on the first dielectric layer. Chung discloses a semiconductor device comprising a second dielectric layer 70 disposed on a first dielectric layer 54 (Fig. 10, ¶ [0026]). It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to form a second dielectric layer disposed on a first dielectric layer, as disclosed by Chung, in Chen to arrive the claimed feature in order for protection and further processing.

Regarding Claim **3**, Chen in view of Chung discloses the semiconductor device further comprising an etching stop layer 218 disposed on two sides of the metal gate 214, and the etching stop layer 218 has a truncated top surface (Chen, Fig. 12).

Regarding Claims **4 and 5**, Chen in view of Chung discloses the semiconductor device further comprising a plurality of first contacts 72 disposed in the first dielectric layer 54 and in the second dielectric layer 70 that are electrically connected to parts of the S/D region 144/244,

wherein each first contact is a monolithically formed structure; and further comprising a plurality of second contacts 72 disposed in the first dielectric layer 54 and in the second dielectric layer 72 that are electrically connected to parts of the metal gate 268, wherein each second contact 72 is a monolithically formed structure (Chung, Fig. 10).

Regarding Claim 7, Chen does not disclose the semiconductor device further comprising a salicide layer disposed between each S/D region and each first contact. Chung discloses a semiconductor device further comprising a salicide layer 146/246 disposed between each S/D region 144/244 and each first contact 72 (Fig. 10, ¶¶ [0016] and [0026]).

Regarding Claims 8 and 9, Chen in view of Chung discloses the semiconductor device further comprising further comprising a plurality of third contacts 72 disposed on parts of the first contacts 72 and on parts of the second contacts 72, wherein each third contact 72 is a monolithically formed structure; wherein each third contact 72 comprises a via hole structure (not labeled) and a trace structure (not labeled), wherein the via hole structure and the trace structure comprise the same material and contact each other directly (Chung, Fig. 10).

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 6:30 AM to 3:00 PM. If attempts to reach the examiner by

Art Unit: 2818

telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Andy Huynh/
Primary Examiner, Art Unit 2818

Notice of References Cited	Application/Control No. 13/875,293	Applicant(s)/Patent Under Reexamination HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2013/0154022	06-2013	Chung et al.	257/369
*	B	US-2014/0048888	02-2014	Chen et al.	257/369
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7013446		2006-03-14	Ohba; Hisayoshi	all
	2	7521324		2009-04-21	Ohmi; Tadahiro	all
	3	7592270		2009-09-22	Teo; Lee Wee	all
	4	7531437		2009-05-12	Brask; Justin K.	all
	5	6921963		2005-07-26	Krivokapic; Zoran	all
	6	7091551		2006-08-15	Anderson; Brent A.	all
	7	7309626		2007-12-18	leong; Mei-Kei	all
	8	7214620		2007-05-08	Kim; Hyun-Su	all

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

	9	6855607		2005-02-15	Achuthan; Krishnashree	all
	10	7250658		2007-07-31	Doris; Bruce B.	all
	11	6492216		2002-12-10	Yeo; Yee-Chia	all
	12	7087477		2006-08-08	Fried; David M.	all
	13	7247887		2007-07-24	King; Tsu-Jae	all
	14	7352034		2008-04-01	Booth, Jr.; Roger Allen	all
	15	7569857		2009-08-04	Simon, legal representative; David	all
	16	5998873		1999-12-07	Blair; Christopher S.	all
	17	7112495		2006-09-26	Ko; Chih-Hsin	all
	18	6043138		2000-03-28	Ibok; Effiong E.	all
	19	7470570		2008-12-30	Beintner; Jochen	all

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20100040768		2010-02-18	Dhindsa; Rajinder;	all
	2	20080061366		2008-03-13	Liu; Che-Hung;	all
	3	20100129994		2010-05-27	Awad; Yousef;	all
	4	20040195624		2004-10-07	Liu, Chee-Wee;	all
	5	20060099830		2006-05-11	Walther; Steven R.;	all
	6	20080157208		2008-07-03	Fischer; Kevin J.;	all
	7	20090269916		2009-10-29	KANG; Inkuk;	all
	8	20100144121		2010-06-10	Chang; Cheng-Hung;	all
	9	20090057759		2009-03-05	Obradovic; Borna;	all

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

	10	20070015365		2007-01-18	Chen; Hsien-Wei;	all
	11	20070072376		2007-03-29	Chen; John;	all
	12	20100044783		2010-02-25	Chuang; Harry;	all
	13	20070218661		2007-09-20	Shroff; Mehul D.;	all
	14	20090200494		2009-08-13	Hatem; Christopher R.;	all
	15	20100048027		2010-02-25	Cheng; Kangguo;	all
	16	20050051825		2005-03-10	Fujiwara, Makoto;	all
	17	20060286729		2006-12-21	Kavalieros; Jack;	all
	18	20070158756		2007-07-12	Dreeskornfeld; Lars;	all
	19	20090242964		2009-10-01	Akil; Nader;	all
	20	20100072553		2010-03-25	XU; Jeff J.;	all

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

	21	20100167506		2010-07-01	LIN; Simon Su-Horng;	all
	22	20090124097		2009-05-14	Cheng; Kangguo;	all
	23	20070108528		2007-05-17	Anderson; Brent A.;	all
	24	20120068234		2012-03-22	Soss	
	25	20120139061		2012-06-07	Ramachandran	

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.H./

Receipt date: 05/02/2013

13875293 - GAU: 2818

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

EXAMINER SIGNATURE			
Examiner Signature	/Andy Huynh/	Date Considered	09/09/2014
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ching-Wen Hung
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1622USA

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Scott Margo/	Date (YYYY-MM-DD)	2013-05-02
Name/Print	Scott Margo	Registration Number	56277

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.H./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	50	("5760429" "6022804" "5661061" "5976391" "5326670" "5482784" "4978594" "5252433" "5360763" "5385867" "5420070" "5426016" "5436411" "5721155" "5731601" "5982545" "6114237" "4308339" "4411719" "4535026" "4878102" "4952272" "4999318" "5304626" "5304828" "5334544" "5403700" "5767002" "5841180" "5851880" "5866484" "6013925" "6025646" "6028629" "6043145" "6090640" "6103455" "6106352" "6137064" "6163075" "6229186" "4311533" "4316203" "4354897" "4374912" "4390394" "4397079" "4414314" "4432037" "4449285").pn.	US-PGPUB; USPAT	OR	ON	2014/08/31 11:53
S2	44	("7013446" "7521324" "7592270" "7531437" "6921963" "7091551" "7309626" "7214620" "6855607" "7250658" "6492216" "7087477" "7247887" "7352034" "7569857" "5998873" "7112495" "6043138" "7470570" "20100040768" "20080061366" "20100129994" "20040195624" "20060099830" "20080157208" "20090269916" "20100144121" "20090057759" "20070015365" "20070072376" "20100044783" "20070218661" "20090200494" "20100048027" "20050051825" "20060286729" "20070158756" "20090242964" "20100072553" "20100167506" "20090124097" "20070108528" "20120068234" "20120139061").pn.	US-PGPUB; USPAT	OR	ON	2014/09/02 14:35
S3	1442	substrate same (dielectric oxide insulat\$3) same (metal\$3 conduct\$3) same gate same source same drain same (hard near mask)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/09 12:38
S4	22987105	@ad< "20130502" @rlad< "20130502"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2014/09/09 12:39
S5	1128	S3 and S4	US-PGPUB; USPAT; EPO; JPO	OR	ON	2014/09/09 12:39
S6	7663	substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3)	US-PGPUB; USPAT;	OR	ON	2014/09/17 08:22

		near gate\$1) and source and drain and (hard near mask)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S7	23001216	@ad< "20130502" @rlad< "20130502"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2014/09/17 08:23
S8	7447	S6 and S7	US-PGPUB; USPAT; EPO; JPO	OR	ON	2014/09/17 08:23
S9	577	S8 and ((top near surface\$1) with (coplanar level))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/17 08:29
S10	50	((top near surface\$1 near hard near mask) with (coplanar level)) with (dielectric oxide insulat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/17 08:34
S11	44	S10 and S7	US-PGPUB; USPAT; EPO; JPO	OR	ON	2014/09/17 08:34
S12	31	S9 and (top near surface\$1 near hard near mask)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/17 09:05

EAST Search History (Interference)

<This search history is empty>

9/ 17/ 2014 1:38:26 PM**C:\Users\ahuyinh\Documents\EAST\Workspaces\13875293.wsp**

<i>Index of Claims</i> 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	07/31/2014	09/17/2014						
	1	÷	✓						
	2	÷	✓						
	3	÷	✓						
	4	÷	✓						
	5	÷	✓						
	6	÷	✓						
	7	÷	✓						
	8	÷	✓						
	9	÷	✓						
	10	÷	N						
	11	÷	N						
	12	÷	N						
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	14	÷	N						
	15	÷	N						
	16	÷	N						
	17	÷	N						
	18	÷	N						
	19	÷	N						
	20	÷	N						

Search Notes 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS Search	8/31/14	AH
EAST Search	9/9/14	AH
EAST Search	9/17/14	AH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA

CONFIRMATION NO. 7170

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

PUBLICATION NOTICE



0000000071730118

Title:SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF

Publication No.US-2014-0327080-A1

Publication Date:11/06/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

SEMICONDUCTOR STRUCTURE

Appl. No. : 13/875,293 Confirmation No. 7170
First Named Inventor : Ching-Wen Hung
Filed : May 2, 2013
TC/A.U. : 2818
Examiner : Huynh, Andy
Docket No. : NAUP1622USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

5 In response to the Office action of September 23, 2014, please amend the
above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2
of this paper.

Amendments to the Drawings begin on page 6 of this paper.

Remarks/Arguments begin on page 7 of this paper.

Replacement sheet

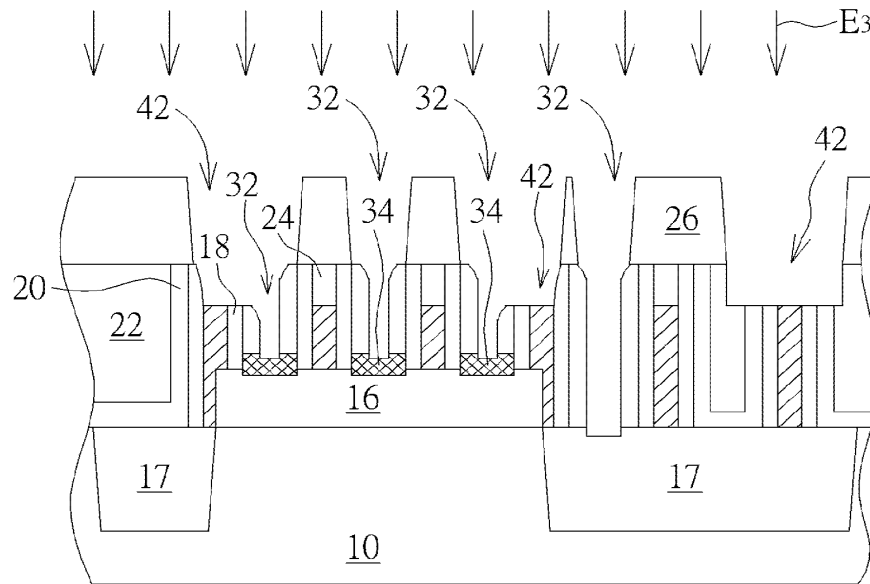


FIG. 7

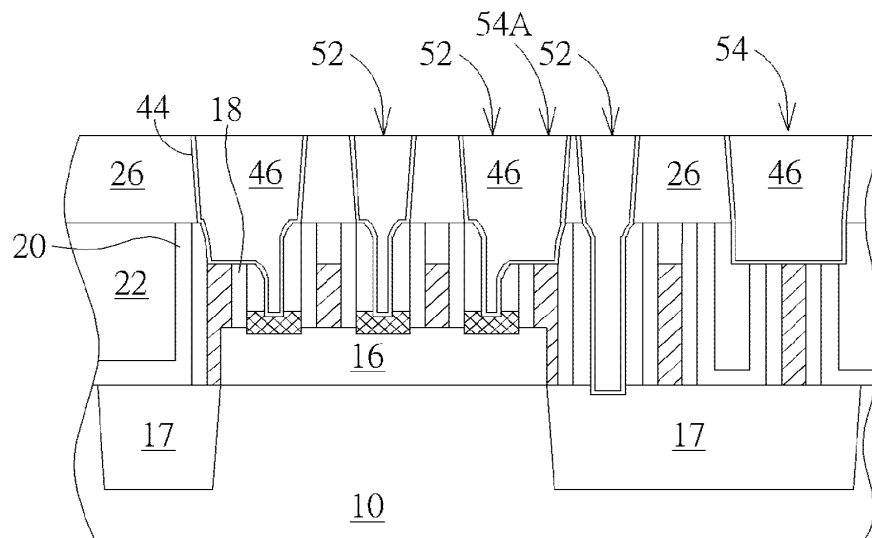


FIG. 8

Amendments to the Claims:

Listing of Claims:

1. (currently amended) A semiconductor structure, comprising:
- 5 a substrate;
- a first dielectric layer disposed on the substrate;
- a metal gate disposed in the first dielectric layer;
- a spacer disposed on two sides of the metal gate, wherein the spacer has a
truncated top surface;
- a source/drain region (S/D region) disposed on two sides of the metal gate;
- 10 and
- a hard mask disposed on the metal gate, wherein the top surface of the hard
mask and the top surface of the first dielectric layer are on the same level.
- 2.(original) The semiconductor device of claim 1, further comprising a second
- 15 dielectric layer disposed on the first dielectric layer.
- 3.(original) The semiconductor device of claim 2, further comprising an etching
stop layer disposed on two sides of the metal gate, and the etching stop layer has a
truncated top surface.
- 20
- 4.(original) The semiconductor device of claim 2, further comprising a plurality
of first contacts disposed in the first dielectric layer and in the second dielectric layer
that are electrically connected to parts of the S/D region, wherein each first contact is
a monolithically formed structure.
- 25
- 5.(original) The semiconductor device of claim 2, further comprising a plurality
of second contacts disposed in the first dielectric layer and in the second dielectric
layer that are electrically connected to parts of the metal gate, wherein each second
contact is a monolithically formed structure.
- 30

6.(original) The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

7.(original) The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

8.(original) The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

10

9.(original) The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

15 10.(withdrawn) A manufacturing method of a semiconductor device, at least comprising the following steps:

providing a substrate, wherein a first dielectric layer is formed on the substrate, at least one metal gate is formed in the first dielectric layer and at least one source drain region (S/D region) is disposed on two sides of the metal gate;

20

forming a second dielectric layer on the first dielectric layer;

performing a first etching process to form a plurality of first trenches in the first dielectric layer and the second dielectric layer, wherein each first trench exposes each S/D region;

performing a salicide process to form a salicide layer in each first trench;

25

and

performing a second etching process to form a plurality of second trenches in the first dielectric layer and the second dielectric layer, wherein each first trench exposes each metal gate.

30 11.(withdrawn) The method of claim 10, further comprising forming a hard mask

on the top surface of each metal gate after the first dielectric layer is formed.

12.(withdrawn) The method of claim 11, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

5

13.(withdrawn) The method of claim 10, further comprising forming at least one fin structure on the substrate.

14.(withdrawn) The method of claim 10, wherein parts of the second trenches
10 and parts of the first trenches partially overlap each others.

15.(withdrawn) The method of claim 10, further comprising filling a metal layer in each first trench and each second trench simultaneously to form a plurality of first contacts and a plurality of second contacts respectively.

15

16.(withdrawn) The method of claim 15, further comprising forming a plurality of third contacts electrically connected to parts of the first contacts or parts of the second contacts, wherein each third contact is a monolithically formed structure.

17.(withdrawn) The method of claim 16, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

20

18.(withdrawn) The method of claim 10, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

25

19.(withdrawn) The method of claim 11, wherein when performing the first etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is larger than 5.

30

20.(withdrawn) The method of claim 11, wherein when performing the second etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is smaller than 5.

5

SEMICONDUCTOR STRUCTURE

Appl. No. : 13/875,293 Confirmation No. : 7170
First Named Inventor : Ching-Wen Hung
Filed : May 2, 2013
TC/A.U. : 2818
Examiner : Huynh, Andy
Docket No. : NAUP1622USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Subject: Reminder of the Title Change

5 Dear Sir,

The applicant has requested to substitute the title of the current invention in the Response to Office action (Amendment to the Specification) submitted on 08/26/2014. However, so far the title showed on PAIR still has not been changed.

10

Please amend the title of the invention as “**SEMICONDUCTOR STRUCTURE**” according to the request presented in the said communication.

Your attention and assistance in this matter is greatly appreciated.

15

Sincerely yours,

/Scott Margo/

Date: 11/30/2014

Scott Margo, Patent Agent No. 56,277

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

Electronic Acknowledgement Receipt	
EFS ID:	20821341
Application Number:	13875293
International Application Number:	
Confirmation Number:	7170
Title of Invention:	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Ching-Wen Hung
Customer Number:	27765
Filer:	Winston Hsu/Lydia Wei
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1622USA
Receipt Date:	01-DEC-2014
Filing Date:	02-MAY-2013
Time Stamp:	03:26:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2118850.PDF	718011 da66769b5b6fc4b464cf5e8ee008ea2424a8fc6c	no	8

Warnings:

Information:

2	Amendment/Req. Reconsideration-After Non-Final Reject	2118849.PDF	78909 bee9036882c8f655d665197be2eb17d9300 cbef4	no	1
Warnings:					
Information:					
3	Drawings-only black and white line drawings	2118848.PDF	69437 f9b72a1b86872b464f1a42eb785fa441f812 ac6	no	1
Warnings:					
Information:					
4	Claims	2118847.PDF	87620 193efac8faaf9b00cfae1d2ebe874e811f84 cb1	no	4
Warnings:					
Information:					
5	Miscellaneous Incoming Letter	NAUP1622USA0_A2_2_Remind er.pdf	585356 a1bbafb64a558b2763e9647a827194023a6 80d88	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1539333		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Appl. No. 13/875,293
Reply to Office action of September 23, 2014

Amendments to the Drawings:

The replacement sheet of drawings is attached, having amended Figure 8 thereon.
Figure 8 has been amended to be electronically reproducible.

Attachment: Replacement Sheet 1 page

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record
5 in the application file.

1. Claim Rejections —35 USC 102/103

Claims 1 and 6 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by US 2014/0048888 to Chen et al. hereinafter as “Chen.”

10

Claims 2-5 and 7-9 are rejected under 35 U.S.C. 103 as being unpatentable over US 2014/0048888 to Chen et al. hereinafter as “Chen” as applied to claim 1 above, and further in view of US 2013/0154022 to Chung et al. hereinafter as “Chung.”

15

Response:

Claim 1 has been amended to overcome the claim rejections. Specifically, the limitation of “a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface” is added in claim 1. The above limitation is fully supported by
20 paragraph [0013] (shown as below) and FIGS. 1-9 of the present specification. No new matter is introduced.

“[0013] In addition, the method of the present invention further comprises selectively forming an epoxy layer 15 on the S/D region 14. Afterwards, a spacer 18
25 and a contact etching stop layer (CESL) 20 may be formed on two sides of the metal gate 12. A first dielectric layer 22 is then formed on the substrate 10, and a planarization process is then performed, such as a chemical mechanical polishing (CMP), to have the top surface of the metal gate 12 and the top surface of the first dielectric layer 22 on the same level. It is worth noting that in this embodiment, an
30 etching process is performed after the metal gate 12 is completed, to remove parts of the metal gate 12, and a hard mask 24 is then formed to replace the upper portion of

the metal gate 12. **Another planarization process** is then performed to remove the extra hard mask 24. In other words, in the present embodiment, a hard mask 24 is disposed on the top of the metal gate 12, and the top surface of the hard mask 24 and the top surface of the first dielectric layer 22 are on the same level. Besides, since the
5 hard mask 24 replaces some top portion of the metal gate 12, the hard mask 24 is therefore disposed only on the metal gate 12, and disposed between the spacers 18. In addition, **since parts of the spacer 18 and parts of the CESL 20 are removed during another planarization process, so the spacer 18 and the CESL 20 have a truncated top surface**. In the present embodiment, the spacer 18, the CESL 20 and the hard
10 mask 24 mainly comprise silicon nitride, and the first dielectric layer 22 mainly comprises silicon oxide, but not limited thereto. These elements and the manufacturing methods thereof are well known to persons of ordinary skills in the art and the details will not be described here.”

15 In the present invention, as shown in FIG.1 below, after the first dielectric layer 22 is formed, a planarization process such as CMP is performed to have the top surface of the metal gate 12 and the top surface of the first dielectric layer 22 on the same level, and afterwards, in order to remove parts of the metal gate 12 (especially the upper portion of the metal gate), an etching process is then performed, and the hard mask 24 is then formed
20 on the upper portion of the metal gate 12. Next, another CMP is then performed, to remove the extra hard mask 24. However, since parts of the spacer 18 and parts of the CESL 20 are removed during another planarization process, so the spacer 18 and the CESL 20 have a truncated top surface.

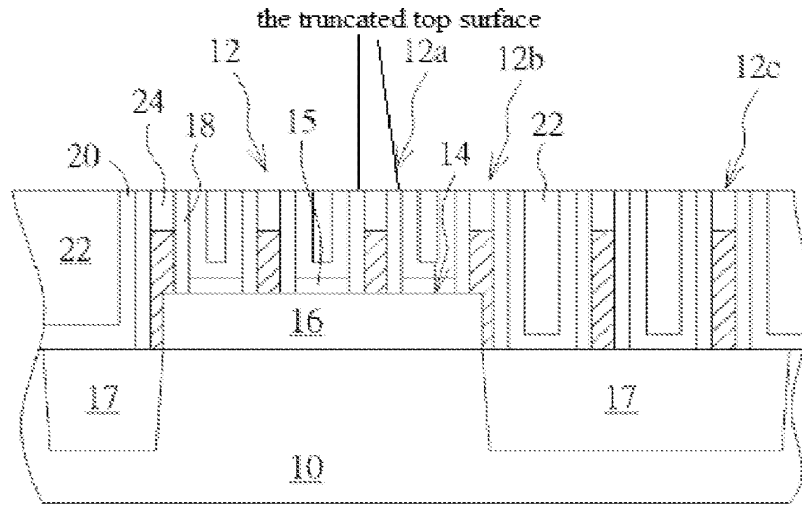


FIG. 1

However, in Chen's invention (US 2014/0048888), as shown in FIG.10 below, the spacer 218n does not have a truncated top surface.

5

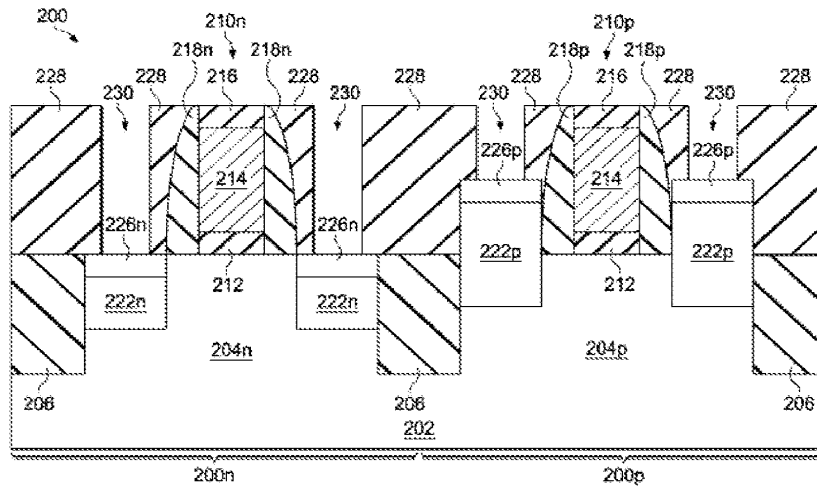


FIG. 10

Similarly, in Chung's invention (US 2013/0154022), as shown in FIGS.3 and 9 below, the spacer 143 does not have a truncated top surface either.

5

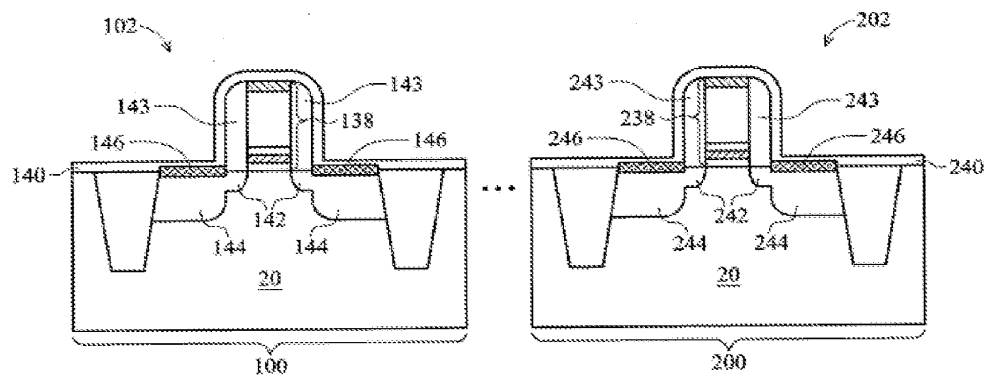


Fig. 3

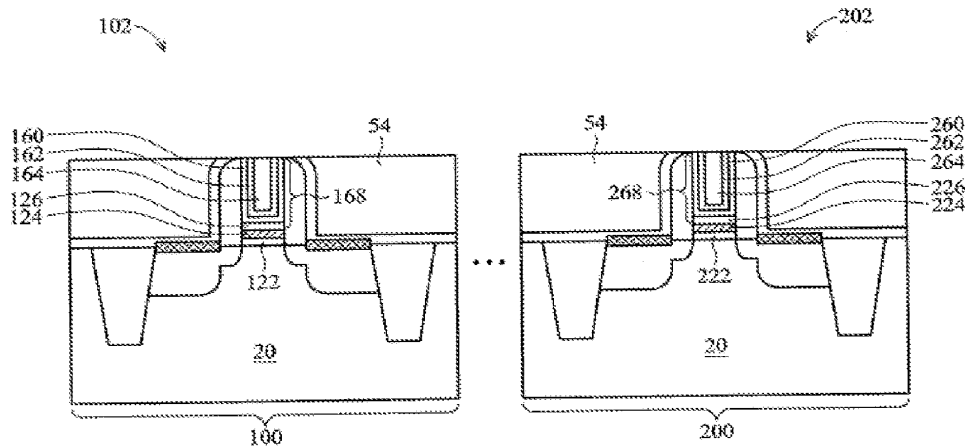


Fig. 9

If the applicant tries to modify Chen by using the combination of Chung, it is far from obvious to obtain the semiconductor structure has a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface, as recited in the amended claim 1.

The applicant also would like to point out that, referring to MPEP 2143.03, all claim limitations must be considered during obviousness rejection: "**All words in a claim must be considered in judging the patentability of that claim against the prior art.**" The applicant also submits that Chen, in view of Chung, does not disclose nor suggest all of the claim limitations of the respective claims. Therefore the applicant advocates that those cited reference could not be combined obviously to obtain the present invention.

As the above features are absent in Chen's invention and Chung's invention, the applicant submits that the present invention is patentable over the cited references.

Reconsideration of the amended claim 1 is respectfully requested. As claims 2-9 are dependent upon claim 1, the applicant submits that, if claim 1 is found allowable, claims 2-9 should additionally be found allowable.

5 **2. Amendments to the Drawings**

In addition, FIG.8 has been amended, since the label 54A of the second contact which recited in paragraph [0020] of the present specification wasn't shown in original FIG.8, therefore the applicant amends FIG.8, especially the label "54A" is added in in FIG.8, the amendment is fully supported by paragraph [0020] (shown as
10 below) of the present specification. No new matter is introduced.

*"[0020] As shown in FIG.8, a barrier layer 44 and a metal layer 46 are filled in each first trench 32 and each second trench 42 simultaneously, wherein the barrier layer 44 may comprise titanium nitride (TiN), tantalum nitride (TaN) or Ti/TiN
15 multiple barrier layers to improve the adhesivity between the inner surface of each trench and the metal layer formed in the following steps. The metal layer 46 preferably comprises tungsten (W) that has better gap fill performances. A planarization process is then performed to remove the extra barrier layer and the metal layer disposed on the top surface of the second dielectric layer 26 to
20 simultaneously form a plurality of first contacts 52 and a plurality of second contacts 54 in the first dielectric layer 22 and in the second dielectric layer 26, wherein each first contact 52 at least is electrically connected to parts of the S/D region 14 (in other words, the first contacts 52 of the present embodiment are the M0CT mentioned above), each second contact 54 is at least electrically connected to parts of the metal
25 gate 12 (in other words the second contacts 54 of the present embodiment are the M0PY mentioned above). In addition, since the first contacts 52 and the second contacts 54 are filled by the metal layer 46 and completed simultaneously, each first contact 52 and each second contact 54 is a monolithically formed structure. It is worth noting that in the present invention, parts of the second trenches 42 and parts of
30 the first trenches 32 are partially overlapped, so parts of the first contact 52 will be*

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/875,293	Filing Date 05/02/2013	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED (Column 1)	NUMBER EXTRA (Column 2)	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT	DATE	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	12/01/2014						
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/THUY TA/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA	7170

27765 7590 01/28/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
HUYNH, ANDY

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
01/28/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 13/875,293	Applicant(s) HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/01/14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) 10-20 is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-9 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date ____. | 4) ☐ Other: ____. |

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

This is responsive to Applicant's Amendment filed December 1, 2014. By the Amendment, Claims **10-20** have been withdrawn. Claim **1** has been amended.

Response to Arguments

Applicant's arguments, see Remarks filed December 1, 2014, with respect to the rejection have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1 and 6** are rejected under 35 U.S.C. 103 as being unpatentable over US 2014/0048888 to Chen et al. hereinafter as "Chen'888" in view of US 2009/0236669 to Chen et al. hereinafter as "Chen'669."

Regarding Claim **1**, Chen'888 discloses a semiconductor structure, comprising:

a substrate 202;
a first dielectric layer 228 disposed on the substrate 202;
a metal gate 214 disposed in the first dielectric layer 228;
a source/drain region (S/D region) 208 disposed on two sides of the metal gate 214;
and
a hard mask 216 disposed on the metal gate 214, wherein the top surface of the hard mask 216 and the top surface of the first dielectric layer 228 are on the same level (Fig. 12, ¶¶ [0009]-[0034]).

Chen'888 does not disclose a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface. Chen'669 discloses a semiconductor device comprising a spacer 82 disposed on two sides of the metal gate 80, wherein the spacer 82 has a truncated top surface (Fig. 14, ¶¶ [0015]-[0035]). It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to utilize the teaching of the spacer has a truncated top surface, as disclosed by Chen'669, to incorporate into Chen'888 to arrive the claimed invention, wherein a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface. It is proper to combine Chen'888 and Chen'669, since they both teach an analogous art of relating to a semiconductor device having a metal gate transistor.

Regarding Claim 6, Chen'888 discloses the semiconductor device further comprising at least one fin structure 212 disposed on the substrate 202 (Fig. 12).

Claims **2-5 and 7-9** are rejected under 35 U.S.C. 103 as being unpatentable over US 2014/0048888 to Chen et al. hereinafter as “Chen’888” in view of US 2009/0236669 to Chen et al. hereinafter as “Chen’669” and further in view of US 2013/0154022 to Chung et al. hereinafter as “Chung.”

Regarding Claim **2**, Chen’888 in view of Chen’669 does not disclose the semiconductor device further comprising a second dielectric layer disposed on the first dielectric layer. Chung discloses a semiconductor device comprising a second dielectric layer 70 disposed on a first dielectric layer 54 (Fig. 10, ¶ [0026]). It would have been obvious to one having ordinary skill in the art before the effective filing date of the claimed invention to form a second dielectric layer disposed on a first dielectric layer, as disclosed by Chung, in Chen’888 in view of Chen’669 to arrive the claimed feature in order for protection and further processing.

Regarding Claim **3**, Chen’888 in view of Chen’669 further in view of Chung discloses the semiconductor device further comprising an etching stop layer 218 disposed on two sides of the metal gate 214, and the etching stop layer 218 has a truncated top surface (Chen’888, Fig. 12).

Regarding Claims **4 and 5**, Chen’888 in view of Chen’669 further in view of Chung discloses the semiconductor device further comprising a plurality of first contacts 72 disposed in the first dielectric layer 54 and in the second dielectric layer 70 that are electrically connected to parts of the S/D region 144/244, wherein each first contact is a monolithically formed structure; and further comprising a plurality of second contacts 72 disposed in the first dielectric layer 54

and in the second dielectric layer 72 that are electrically connected to parts of the metal gate 268, wherein each second contact 72 is a monolithically formed structure (Chung, Fig. 10).

Regarding Claim 7, Chen'888 in view of Chen'669 does not disclose the semiconductor device further comprising a salicide layer disposed between each S/D region and each first contact. Chung discloses a semiconductor device further comprising a salicide layer 146/246 disposed between each S/D region 144/244 and each first contact 72 (Fig. 10, ¶¶ [0016] and [0026]).

Regarding Claims 8 and 9, Chen'888 in view of Chen'669 further in view of Chung discloses the semiconductor device further comprising further comprising a plurality of third contacts 72 disposed on parts of the first contacts 72 and on parts of the second contacts 72, wherein each third contact 72 is a monolithically formed structure; wherein each third contact 72 comprises a via hole structure (not labeled) and a trace structure (not labeled), wherein the via hole structure and the trace structure comprise the same material and contact each other directly (Chung, Fig. 10).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

This action is a final rejection and is intended to close the prosecution of this application. Applicant's reply under 37 CFR 1.113 to this action is limited either to an appeal to the Board of Patent Appeals and Interferences or to an amendment complying with the requirements set forth below.

If applicant should desire to appeal any rejection made by the examiner, a Notice of Appeal must be filed within the period for reply identifying the rejected claim or claims appealed. The Notice of Appeal must be accompanied by the required appeal fee.

If applicant should desire to file an amendment, entry of a proposed amendment after final rejection cannot be made as a matter of right unless it merely cancels claims or complies with a formal requirement made earlier. Amendments touching the merits of the application which otherwise might not be proper may be admitted upon a showing a good and sufficient reasons why they are necessary and why they were not presented earlier.

A reply under 37 CFR 1.113 to a final rejection must include the appeal from, or cancellation of, each rejected claim. The filing of an amendment after final rejection, whether or not it is entered, does not stop the running of the statutory period for reply to the final rejection unless the examiner holds the claims to be in condition for allowance. Accordingly, if a Notice of Appeal has not been filed properly within the period for reply, or any extension of this period

obtained under either 37 CFR 1.136(a) or (b), the application will become abandoned. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272- 1781. The examiner can normally be reached on Monday - Friday, 6:30AM – 3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andy Huynh/

Primary Examiner, Art Unit 2818

Notice of References Cited	Application/Control No. 13/875,293	Applicant(s)/Patent Under Reexamination HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0236669	09-2009	Chen et al.	257/380
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S17	9	substrate and gate and (hard near mask) and spacer\$1 and (truncat\$3 with (top near surface\$1))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/12 13:16
S18	44	substrate and gate and (hard near mask) and spacer\$1 and truncat\$3 and (top near surface\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/12 13:19
S19	10	gate same spacer\$1 same truncat\$3 same (top near surface\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/12 13:25
S20	550	gate and spacer\$1 and truncat\$3 and (top near surface\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/12 13:28
S21	23182669	@ad< "20130502" @rlad< "20130502"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2015/01/12 13:28
S22	530	S20 and S21	US-PGPUB; USPAT; EPO; JPO	OR	ON	2015/01/12 13:28
S23	172	gate same (sidewall\$1 spacer\$1) and (truncat\$3 same top)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/01/15 10:34
S24	23190834	@ad< "20130502" @rlad< "20130502"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2015/01/15 10:35
S25	141	S23 and S24	US-PGPUB; USPAT; EPO; JPO	OR	ON	2015/01/15 10:35

EAST Search History (Interference)

< This search history is empty >

1/ 15/ 2015 1:21:40 PM**C:\Users\ahuyinh\Documents\EAST\Workspaces\13875293.wsp**

Search Notes 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS Search	8/31/14	AH
EAST Search	9/9/14	AH
EAST Search	9/17/14	AH
EAST Search	1/12,15/15	AH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47									
CLAIM		DATE							
Final	Original	07/31/2014	09/17/2014	01/15/2015					
	1	÷	✓	✓					
	2	÷	✓	✓					
	3	÷	✓	✓					
	4	÷	✓	✓					
	5	÷	✓	✓					
	6	÷	✓	✓					
	7	÷	✓	✓					
	8	÷	✓	✓					
	9	÷	✓	✓					
	10	÷	N	N					
	11	÷	N	N					
	12	÷	N	N					
	13	÷	N	N					
	14	÷	N	N					
	15	÷	N	N					
	16	÷	N	N					
	17	÷	N	N					
	18	÷	N	N					
	19	÷	N	N					
	20	÷	N	N					

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (09-08)

Approved for use through 10/31/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	13/875,293	Filing Date	2013-05-02	Docket Number (if applicable)	NAUP1622USA	Art Unit	2818
First Named Inventor	Ching-Wen Hung			Examiner Name	Huynh, Andy		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503105

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (09-08)

Approved for use through 10/31/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Scott Margo/	Date (YYYY-MM-DD)	2015-04-08
Name	Scott Margo	Registration Number	56277

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

SEMICONDUCTOR STRUCTURE

Appl. No. : 13/875,293 Confirmation No. : 7170
First Named Inventor : Ching-Wen Hung
Filed : May 2, 2013
TC/A.U. : 2818
Examiner : Huynh, Andy
Docket No. : NAUP1622USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Subject: Reminder of the Title Change

5 Dear Sir,

The applicant has requested to substitute the title of the current invention in the Response to Office action (Amendment to the Specification) submitted on 08/26/2014. However, so far the title showed on PAIR still has not been changed.

10

Please amend the title of the invention as “**SEMICONDUCTOR STRUCTURE**” according to the request presented in the said communication.

Your attention and assistance in this matter is greatly appreciated.

15

Sincerely yours,

/Scott Margo/

Date: 04/08/2015

Scott Margo, Patent Agent No. 56,277

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Electronic Patent Application Fee Transmittal				
Application Number:		13875293		
Filing Date:		02-May-2013		
Title of Invention:		SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF		
First Named Inventor/Applicant Name:		Ching-Wen Hung		
Filer:		Winston Hsu/Eve Hsieh		
Attorney Docket Number:		NAUP1622USA		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	21998515
Application Number:	13875293
International Application Number:	
Confirmation Number:	7170
Title of Invention:	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Ching-Wen Hung
Customer Number:	27765
Filer:	Winston Hsu/Eve Hsieh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1622USA
Receipt Date:	08-APR-2015
Filing Date:	02-MAY-2013
Time Stamp:	05:23:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1200
RAM confirmation Number	6688
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2220020.PDF	725964	no	6
			e07afc9452318c3d96d97370cb3471d5ff58a336		
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	2220019.PDF	79580	no	1
			e148c00675cace3361be9238a6903ffbfb9d2642		
Warnings:					
Information:					
3	Claims	2220018.PDF	85639	no	4
			fe36493bc6d58b143bc55045619b5b642db4d2ed		
Warnings:					
Information:					
4	Request for Continued Examination (RCE)	2219197.pdf	466069	no	3
			2ad44eec59698a8b764452f8396adb97a5307ee0		
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
5	Miscellaneous Incoming Letter	REMINDER.pdf	585389	no	2
			c975153ff5075574918d9d11d80c566240a20238		
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30522	no	2
			f03a03b0ba78c97fcc685bf4354a35d46f8da09		
Warnings:					
Information:					
Total Files Size (in bytes):			1973163		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Request for Continued Examination:

5 The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

10 Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record in the application file.

1. Claim Rejections —35 USC 103

15 *Claims 1 and 6 are rejected under 35 U.S.C. 102(a)(2) as being anticipated by US 2014/0048888 to Chen et al. hereinafter as “Chen’888 in view of US 2009/0126669 to Chen et al. hereinafter as “Chen’669.”*

20 *Claims 2-5 and 7-9 are rejected under 35 U.S.C. 103 as being unpatentable over US 20 14/0048888 to Chen et al. hereinafter as “Chen’888” in view of US 2009/0126669 to Chen et al. hereinafter as “Chen’669, and further in view of US 2013/0154022 to Chung et al. hereinafter as “Chung.”*

Response:

25 Claim 1 has been amended to overcome the claim rejections. Specifically, the limitation of “the first contacts” and “the second contacts” are added in claim 1, and at least one of the first contacts **directly connects** at least one of the second contacts. In addition, the limitation of “a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface” is canceled from claim 1. The above limitations are fully supported by original claims 4-5 and FIG. 9 (shown as below) of the present specification. No new matter is introduced.

30

The present invention, as shown in FIGS.4 and FIG.9 below, comprises a plurality of first contact 52 that are electrically connected to the S/D region, and a plurality of second contacts 54 (54A) that are electrically connected to the metal gate 12, wherein
5 at least one of the first contacts 52 directly connects at least one of the second contacts 54(54A).

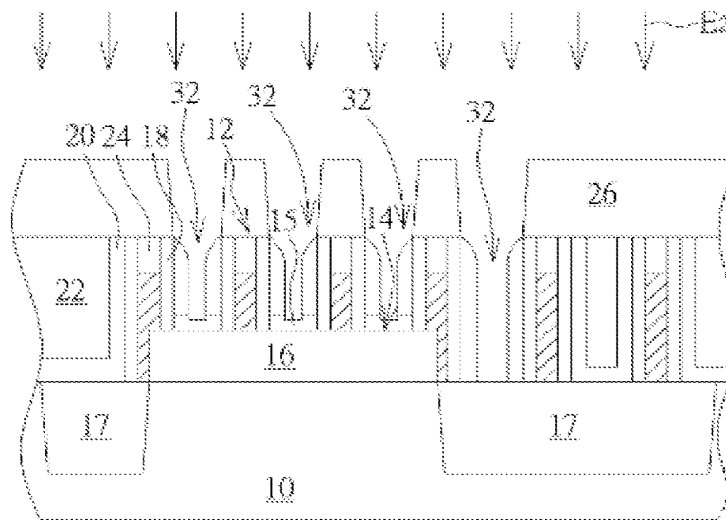


FIG. 4

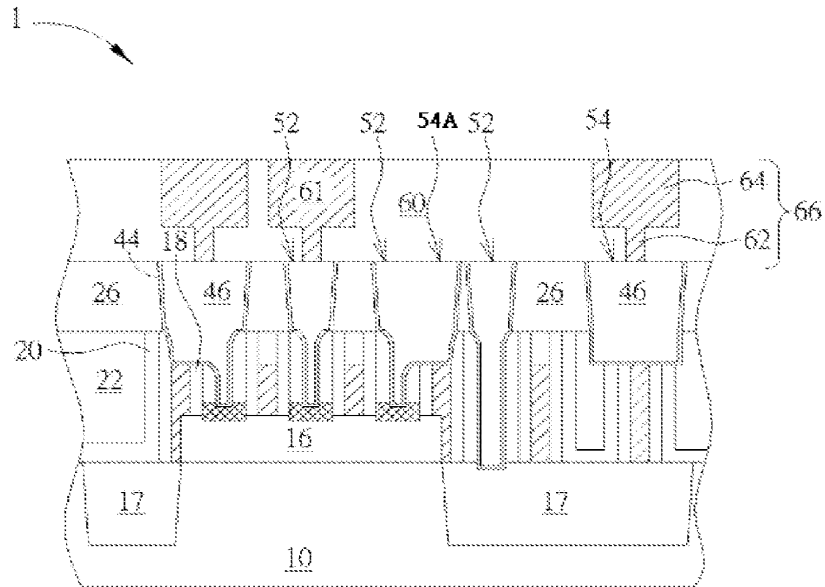


FIG. 9

However, neither Chen'888 (US 2014/0048888) nor Chen'669 (US 2009/0236669) discloses the first contacts being electrically connected to the S/D region, and the second contacts being electrically connected to the metal gate simultaneously, as shown in FIG.10 of Chen'888 and FIG.14 of Chen'669 below:

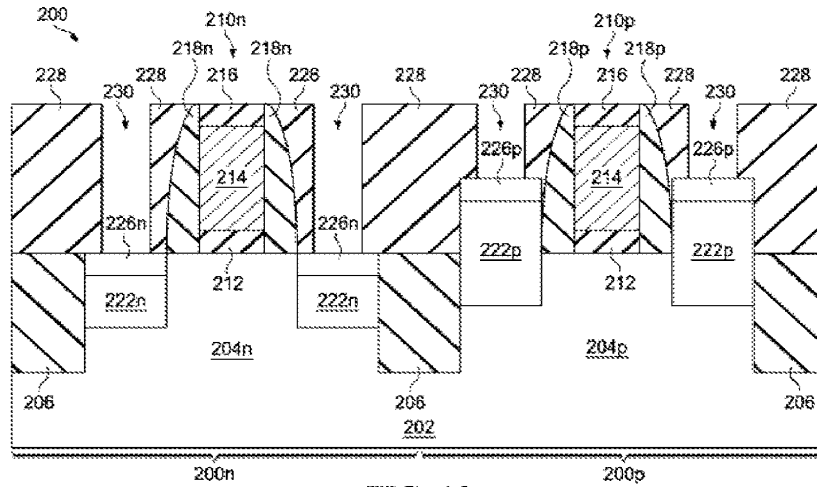


FIG. 10

Chen'888

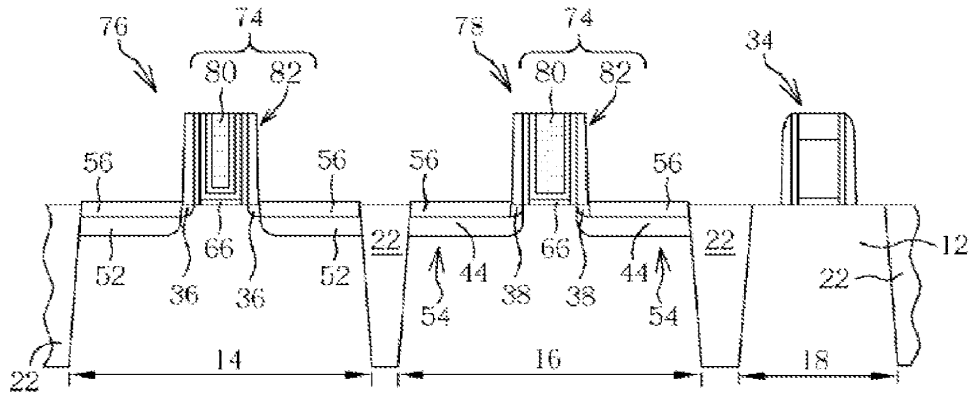


FIG. 14

Chen'669

5

Similarly, in Chung's invention (US 2013/0154022), as shown in FIG.10 below,

the contacts 72 can be deemed as the first contacts and the second contacts of the present invention, but in Chung's invention there is not any first contact, which is connected to a second contact directly, each contact 72 being separated with each other.

5

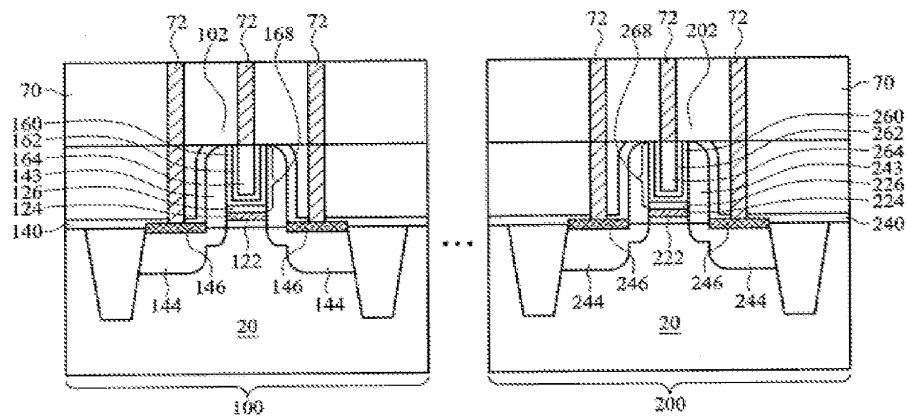


Fig. 10

Chung

If Examiner tries to modify Chen'888 and Chen'669 by using the combination of
 10 Chung, it is far from obvious to obtain the semiconductor structure having the first contacts and the second contacts simultaneously, and at least one of the first contacts directly connects at least one of the second contacts, as recited in the amended claim 1.

15 The applicant also would like to point out that, referring to MPEP 2143.03, all claim limitations must be considered during obviousness rejection: "**All words in a claim must be considered in judging the patentability of that claim against the prior art.**" The applicant also submits that Chen'888, in view of Chen'669 and Chung,

does not disclose nor suggest all of the claim limitations of the respective claims. Therefore the applicant advocates that those cited reference could not be combined obviously to obtain the present invention.

5 As the above features are absent in each cited reference, the applicant submits that the present invention is patentable over the cited references. Reconsideration of the amended claim 1 is respectfully requested. As claims 2-9 are dependent upon claim 1, the applicant submits that, if claim 1 is found allowable, claims 2-9 should additionally be found allowable.

10

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

15

/Scott Margo/

Date: 04/08/2015

Scott Margo, Patent Agent No. 56,277

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

20

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

25

SEMICONDUCTOR STRUCTURE

Appl. No. : 13/875,293 Confirmation No. : 7170
First Named Inventor : Ching-Wen Hung
Filed : May 2, 2013
TC/A.U. : 2818
Examiner : Huynh, Andy
Docket No. : NAUP1622USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

Sir:

- 5 In response to the Office action of January 28, 2015, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

5 **Listing of Claims:**

1. (currently amended) A semiconductor structure, comprising:

 a substrate;

 a first dielectric layer disposed on the substrate;

10 [[a]] at least two metal gate-gates disposed in the first dielectric layer;

 a source/drain region (S/D region) disposed between [[on]] two ~~sides of the metal gate-gates~~;

a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;

15 a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gate, wherein at least one of the first contacts directly connects at least one of the second contacts; and

 a hard mask disposed on one of the metal ~~gate-gates~~, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

20

2.(original) The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

3.(original) The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

25

4.(currently amended) The semiconductor device of claim 2, ~~further comprising a plurality of wherein the~~ first contacts disposed in the first dielectric layer and in the second dielectric layer ~~that are electrically connected to parts of the S/D region,~~

30

~~wherein and~~ each first contact is a monolithically formed structure.

5 5.(currently amended) The semiconductor device of claim 2, ~~further comprising a plurality of wherein the~~ second contacts disposed in the first dielectric layer and in the second dielectric layer ~~that are electrically connected to parts of the metal gate,~~
~~wherein and~~ each second contact is a monolithically formed structure.

6.(original) The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

10

7.(original) The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

15 8.(original) The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

20 9.(original) The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

10.(withdrawn) A manufacturing method of a semiconductor device, at least comprising the following steps:

25 providing a substrate, wherein a first dielectric layer is formed on the substrate, at least one metal gate is formed in the first dielectric layer and at least one source drain region (S/D region) is disposed on two sides of the metal gate;

forming a second dielectric layer on the first dielectric layer;

30 performing a first etching process to form a plurality of first trenches in the first dielectric layer and the second dielectric layer, wherein each first trench exposes each S/D region;

performing a salicide process to form a salicide layer in each first trench; and
performing a second etching process to form a plurality of second trenches in the
first dielectric layer and the second dielectric layer, wherein each first trench exposes
each metal gate.

5

11.(withdrawn) The method of claim 10, further comprising forming a hard mask on
the top surface of each metal gate after the first dielectric layer is formed.

12.(withdrawn) The method of claim 11, wherein the top surface of the hard mask and
10 the top surface of the first dielectric layer are on the same level.

13.(withdrawn) The method of claim 10, further comprising forming at least one fin
structure on the substrate.

15 14.(withdrawn) The method of claim 10, wherein parts of the second trenches and
parts of the first trenches partially overlap each others.

15.(withdrawn) The method of claim 10, further comprising filling a metal layer in
each first trench and each second trench simultaneously to form a plurality of first
20 contacts and a plurality of second contacts respectively.

16.(withdrawn) The method of claim 15, further comprising forming a plurality of
third contacts electrically connected to parts of the first contacts or parts of the second
contacts, wherein each third contact is a monolithically formed structure.

25

17.(withdrawn) The method of claim 16, wherein each third contact comprises a via
hole structure and a trace structure, wherein the via hole structure and the trace
structure comprise the same material and contact each other directly.

30 18.(withdrawn) The method of claim 10, further comprising an etching stop layer

disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

5 19.(withdrawn) The method of claim 11, wherein when performing the first etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is larger than 5.

10 20.(withdrawn) The method of claim 11, wherein when performing the second etching process, the ratio of the etching rate for etching the first dielectric layer to the etching rate for etching the second dielectric layer is smaller than 5.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/875,293	Filing Date 05/02/2013	☐ To be Mailed
---	--	---------------------------	---------------------------------------

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

(Column 1)	(Column 2)		RATE (\$)	FEE (\$)
FOR	NUMBER FILED	NUMBER EXTRA		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	* 0	x \$80 =	0
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	* 0	x \$420 =	0
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	0

APPLICATION AS AMENDED – PART II

(Column 1)	(Column 2)	(Column 3)		RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	04/08/2015	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	* 20	Minus ** 20	= 0	x \$80 = 0
	Independent (37 CFR 1.16(h))	* 2	Minus *** 3	= 0	x \$420 = 0
	☐ Application Size Fee (37 CFR 1.16(s))				
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
					TOTAL ADD'L FEE
					0

(Column 1)	(Column 2)	(Column 3)		RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	*	Minus **	=	x \$ =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x \$ =
	☐ Application Size Fee (37 CFR 1.16(s))				
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
					TOTAL ADD'L FEE

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/GERALDINE STANLEY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA	7170

27765	7590	04/27/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION		
P.O. BOX 506		
MERRIFIELD, VA 22116		

EXAMINER
HUYNH, ANDY

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
04/27/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com

Office Action Summary	Application No. 13/875,293	Applicant(s) HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04/08/15.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) 10-20 is/are withdrawn from consideration.
- 6) ☒ Claim(s) 1-9 is/are allowed.
- 7) ☐ Claim(s) _____ is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☒ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 05/02/13 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____ | 4) ☐ Other: _____ |

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission and Amendment filed with RCE on April 8, 2015 have been entered. In view of the Amendment, Claims **1, 4 and 5** have been amended. Claims **1-20** are pending in the application.

Response to Arguments

Applicants' arguments, see Remarks filed June 29, 2012, with respect to the rejection of Claims **1-9** have been fully considered and they are persuasive. Therefore, the rejection has been rendered moot.

Examiner's Amendment

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR

1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

This application is in condition for allowance except for the following formal matters:

1) The amended Claim 1 is not complete. The feature of “a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;” is missing after the phrase of “at least two metal gates disposed in the first dielectric layer;” in line 4; and “one of the metal [gate]” should be –one of the metal gates--, in line 10.

2) The title of the invention is not descriptive. The title of the disclosure is objected to because it does not direct to the claimed invention. It is noticed that the claims are drawn to a semiconductor device. Correction is required. See MPEP § 608.01(b).

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

2) Cancellation of non-elected Claims **10-20**.

Allowable Subject Matter

Claims **1-9** are allowed.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272-1781. The examiner can normally be reached on Monday-Friday 6:30am-3:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Andy Huynh/
Primary Examiner, Art Unit 2818

Search Notes 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/665 OR H01L21/823814 OR H01L2924/0002 OR H01L21/28518 OR H01L21/823807	4/19/15	AH

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	365, 369, E21.421, E27.062, E29.264	4/19/15	AH

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS Search	8/31/14	AH
EAST Search	9/9/14	AH
EAST Search	9/17/14	AH
EAST Search	1/12,15/15	AH
EAST Search	4/19/15	AH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	365, 369, E21.421, E27.062, E29.264	4/19/15	AH

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<i>Index of Claims</i> 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47									
CLAIM		DATE							
Final	Original	07/31/2014	09/17/2014	01/15/2015	04/19/2015				
	1	÷	✓	✓	=				
	2	÷	✓	✓	=				
	3	÷	✓	✓	=				
	4	÷	✓	✓	=				
	5	÷	✓	✓	=				
	6	÷	✓	✓	=				
	7	÷	✓	✓	=				
	8	÷	✓	✓	=				
	9	÷	✓	✓	=				
	10	÷	N	N	N				
	11	÷	N	N	N				
	12	÷	N	N	N				
	13	÷	N	N	N				
	14	÷	N	N	N				
	15	÷	N	N	N				
	16	÷	N	N	N				
	17	÷	N	N	N				
	18	÷	N	N	N				
	19	÷	N	N	N				
	20	÷	N	N	N				

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S26	23296977	@ad< "20130502" @rlad< "20130502"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2015/04/19 10:45
S27	6	substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and source and drain and (hard near mask) and (sidewall\$1 spacer\$1) and (truncat\$3 same top) and contact\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:47
S28	6724	substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and (source drain) and (hard near mask) and (sidewall\$1 spacer\$1) and contact\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:50
S29	6454	S28 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:50
S30	18	S29 and truncat\$3 and (top near surface\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:52
S31	26	S29 and truncat\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:52
S32	3182	S29 and (top near surface\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:53
S33	131	H01L29/66515 H01L29/665 H01L29/7839	US-PGPUB; USPAT	OR	ON	2015/04/19 11:15
S34	107	S33 AND ((H01L29/665 OR H01L21/823814 OR H01L2924/0002 OR H01L21/28518	US-PGPUB; USPAT	OR	ON	2015/04/19 11:16

		OR H01L21/823807).CPC.)				
S35	88	S34 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:16
S36	1194	257/365.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 11:19
S37	1132	S36 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:19
S38	4175	257/369.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 11:31
S39	4061	S38 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:32
S40	2393	257/E27.062.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 11:54
S41	2380	S40 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:54
S42	775	257/E29.264.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 12:17
S43	757	S42 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 12:17
S44	549	257/E21.421.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 12:23
S45	547	S44 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 12:23
S46	39	((hung near ching-wen) (huang near chih-sen)).in.	US-PGPUB; USPAT	OR	ON	2015/04/19 13:53

EAST Search History (Interference)

Ref	Hits	Search Query	DBs	Default	Plurals	Time
-----	------	--------------	-----	---------	---------	------

#				Operator		Stamp
S47	147	(substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and (source drain) and (hard near mask) and (sidewall\$1 spacer\$1) and contact\$2).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/19 13:56
S48	41	(substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and (source drain) and (hard near mask) and (sidewall\$1 spacer\$1) and contact\$2 and (top near surface)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/19 13:57

4/ 19/ 2015 9:03:08 PM

C:\ Users\ ahuynh\ Documents\ EAST\ Workspaces\ 13875293.wsp

SEMICONDUCTOR STRUCTURE

Appl. No. : 13/875,293 Confirmation No. 7170
First Named Inventor : Ching-Wen Hung
Filed : May 2, 2013
TC/A.U. : 2818
Examiner : Huynh, Andy
Docket No. : NAUP1622USA
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

In response to the Office action of April 27, 2015, please amend the above-identified
5 application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3
of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Claims:

Listing of Claims:

1. (currently amended) A semiconductor structure, comprising:
- 5 a substrate;
- a first dielectric layer disposed on the substrate;
- at least two metal gates disposed in the first dielectric layer;
- a spacer disposed on two sides of the metal gate, wherein the spacer has a
truncated top surface;
- a source/drain region (S/D region) disposed between two metal gates;
- 10 a plurality of first contacts disposed in the first dielectric layer that are
electrically connected to parts of the S/D region;
- a plurality of second contacts disposed in the first dielectric layer that are
electrically connected to one of the metal ~~gate-gates~~, wherein at least one of the first
contacts directly connects at least one of the second contacts; and
- 15 a hard mask disposed on one of the metal gates, wherein the top surface of the
hard mask and the top surface of the first dielectric layer are on the same level.
- 2.(original) The semiconductor device of claim 1, further comprising a second
dielectric layer disposed on the first dielectric layer.
- 20
- 3.(original) The semiconductor device of claim 2, further comprising an etching stop
layer disposed on two sides of the metal gate, and the etching stop layer has a
truncated top surface.
- 25
- 4.(previously presented) The semiconductor device of claim 2, wherein the first
contacts disposed in the first dielectric layer and in the second dielectric layer and
each first contact is a monolithically formed structure.
- 30
- 5.(previously presented) The semiconductor device of claim 2, wherein the second
contacts disposed in the first dielectric layer and in the second dielectric layer and

each second contact is a monolithically formed structure.

6.(original) The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

5

7.(original) The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

8.(original) The semiconductor device of claim 3, further comprising a plurality of
10 third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

9.(original) The semiconductor device of claim 8, wherein each third contact
15 comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

10-20.(canceled)

20

Appl. No. 13/875,293
Reply to Office action of April 27, 2015

Amendments to the Specification:

Please replace the original title with the following new title:

“SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE
5 GATE STRUCTURE”

Electronic Acknowledgement Receipt	
EFS ID:	22435728
Application Number:	13875293
International Application Number:	
Confirmation Number:	7170
Title of Invention:	SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF
First Named Inventor/Applicant Name:	Ching-Wen Hung
Customer Number:	27765
Filer:	Winston Hsu/Eve Hsieh
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1622USA
Receipt Date:	27-MAY-2015
Filing Date:	02-MAY-2013
Time Stamp:	04:20:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Arguments/Remarks Made in an Amendment	2260136.PDF	583629 7064a5d448a2b13260b4bae82e0fbd9dd5d3dd2	no	2

Warnings:

Information:

2	Response after Ex Parte Quayle Action	2260135.PDF	77514 d0fae5585b1272d0e269c4c2ef3bfaf7ae7242b	no	1
Warnings:					
Information:					
3	Claims	2260134.PDF	79510 4ae6eac702dd425e5388d354f3ed76c7a8bd7a94	no	2
Warnings:					
Information:					
4	Specification	2260132.PDF	76923 d7596d5802e536ae556563793e20c2d50111892df	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			817576		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

REMARKS/ARGUMENTS

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by electronic mail. I understand that a copy of these communications will be made of record
5 in the application file.

1. Amendment to the claims

Claim 1 have been amended as suggested by the Examiner, and the applicant agrees with the Examiner's proposed amendment.
10

In addition, Claims 10-20 have been canceled.

2. Amendment to the specification

The title of the invention has been replaced with:
15

SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE
STRUCTURE

Applicants submit that the new title is now indicative of the invention to which the claims are directed. Reconsideration of the new title is respectfully requested.
20

3. Allowable Subject Matter

Claims 1-9 are deemed allowable by the Examiner. The applicant is grateful for the allowance.

Applicant respectfully requests that a timely Notice of Allowance be issued in this
25 case.

Appl. No. 13/875,293
Reply to Office action of April 27, 2015

Sincerely yours,

/Scott Margo/

Date: 05/26/2015

Scott Margo, Patent Agent No. 56,277

5 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : ScottMargo@naipo.com

- 10 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/875,293	Filing Date 05/02/2013	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

(Column 1) (Column 2)

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT	05/27/2015	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 9	Minus	** 20	= 0	x \$80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
TOTAL ADD'L FEE						0	

(Column 1) (Column 2) (Column 3)

AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
TOTAL ADD'L FEE							

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DEBRA SAVOY/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 06/08/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

HUYNH, ANDY

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 06/08/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA	7170

TITLE OF INVENTION: SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	09/08/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

27765 7590 06/08/2015

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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13/875,293 05/02/2013 Ching-Wen Hung NAUP1622USA 7170

TITLE OF INVENTION: SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional UNDISCOUNTED \$960 \$0 \$0 \$960 09/08/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
HUYNH, ANDY	2818	257-365000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA	7170

27765 7590 06/08/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

HUYNH, ANDY

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 06/08/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/875,293	Applicant(s) HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment filed 05/27/15.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-9. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/ANDY HUYNH/ Primary Examiner, Art Unit 2818	
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The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

This is responsive to Applicant's Amendment filed May 27, 2015. By the Amendment, the title of the invention and Claim 1 has been amended. Claims 10-20 have been canceled. Claims 1-9 are pending in the application.

Response to Amendment

The objections to the application set out by the Examiner in the Quayle Office Action of April 27, 2015, have been complied with, so that this application is now in condition for allowance.

Allowable Subject Matter

Claims 1-9 are allowed.

Claims 1-9 are considered allowable since the prior made of record and considered pertinent to the applications' disclosure do not teach or suggest the claimed limitations. The prior art of record, whether taken alone or in combination, fails to teach or render obvious a semiconductor structure comprising all of the limitations as recited in Claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh whose telephone number is (571) 272-1781. The examiner can normally be reached on Monday-Friday 6:30am-3:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Andy Huynh/

Primary Examiner, Art Unit 2818

Search Notes 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/665 OR H01L21/823814 OR H01L2924/0002 OR H01L21/28518 OR H01L21/823807	4/19/15	AH

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	365, 369, E21.421, E27.062, E29.264	4/19/15	AH

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS Search	8/31/14	AH
EAST Search	9/9/14	AH
EAST Search	9/17/14	AH
EAST Search	1/12,15/15	AH
EAST Search	4/19/15	AH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	365, 369, E21.421, E27.062, E29.264	4/19/15	AH

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Issue Classification 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.	
	Examiner ANDY HUYNH	Art Unit 2818	

CPC						
Symbol					Type	Version
H01L		29	/	66515	F	2013-01-01
H01L		29	/	665	I	2013-01-01
H01L		29	/	7839	I	2013-01-01
H01L		29	/	41791	I	2013-01-01
H01L		29	/	66795	I	2013-01-01
H01L		29	/	785	I	2013-01-01
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
		9	
(Assistant Examiner)	(Date)		
/ANDY HUYNH/	06/01/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9

Issue Classification 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17												
2	2		18												
3	3		19												
4	4		20												
5	5														
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7	7														
8	8														
9	9														
	10														
	11														
	12														
	13														
	14														
	15														
	16														

NONE		Total Claims Allowed: 9	
(Assistant Examiner)	(Date)		
/ANDY HUYNH/ Primary Examiner.Art Unit 2818	06/01/2015	O.G. Print Claim(s) 1	O.G. Print Figure 9
(Primary Examiner)	(Date)		



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BIB DATA SHEET

CONFIRMATION NO. 7170

SERIAL NUMBER 13/875,293	FILING or 371(c) DATE 05/02/2013 RULE	CLASS 257	GROUP ART UNIT 2818	ATTORNEY DOCKET NO. NAUP1622USA		
APPLICANTS UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN INVENTORS Ching-Wen Hung, Tainan City, TAIWAN; Chih-Sen Huang, Tainan City, TAIWAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 06/03/2013						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /ANDY HUYNH/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 5	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S26	23296977	@ad< "20130502" @rlad< "20130502"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2015/04/19 10:45
S27	6	substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and source and drain and (hard near mask) and (sidewall\$1 spacer\$1) and (truncat\$3 same top) and contact\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:47
S28	6724	substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and (source drain) and (hard near mask) and (sidewall\$1 spacer\$1) and contact\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:50
S29	6454	S28 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:50
S30	18	S29 and truncat\$3 and (top near surface\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:52
S31	26	S29 and truncat\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:52
S32	3182	S29 and (top near surface\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 10:53
S33	131	H01L29/66515 H01L29/665 H01L29/7839	US-PGPUB; USPAT	OR	ON	2015/04/19 11:15
S34	107	S33 AND ((H01L29/665 OR H01L21/823814 OR H01L2924/0002 OR H01L21/28518	US-PGPUB; USPAT	OR	ON	2015/04/19 11:16

		OR H01L21/823807).CPC.)				
S35	88	S34 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:16
S36	1194	257/365.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 11:19
S37	1132	S36 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:19
S38	4175	257/369.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 11:31
S39	4061	S38 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:32
S40	2393	257/E27.062.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 11:54
S41	2380	S40 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 11:54
S42	775	257/E29.264.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 12:17
S43	757	S42 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 12:17
S44	549	257/E21.421.ccls.	US-PGPUB; USPAT	OR	ON	2015/04/19 12:23
S45	547	S44 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/19 12:23
S46	39	((hung near ching-wen) (huang near chih-sen)).in.	US-PGPUB; USPAT	OR	ON	2015/04/19 13:53

EAST Search History (Interference)

Ref	Hits	Search Query	DBs	Default	Plurals	Time
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#				Operator		Stamp
S47	147	(substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and (source drain) and (hard near mask) and (sidewall\$1 spacer\$1) and contact\$2).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/19 13:56
S48	41	(substrate and (dielectric oxide insulat\$3) and ((metal\$3 conduct\$3) near gate\$1) and (source drain) and (hard near mask) and (sidewall\$1 spacer\$1) and contact\$2 and (top near surface)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/19 13:57

6/ 1/ 2015 9:13:13 AM

C:\ Users\ ahuynh\ Documents\ EAST\ Workspaces\ 13875293.wsp

<i>Index of Claims</i> 	Application/Control No. 13875293	Applicant(s)/Patent Under Reexamination HUNG ET AL.
	Examiner ANDY HUYNH	Art Unit 2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant								☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE											
Final	Original	07/31/2014	09/17/2014	01/15/2015	04/19/2015	06/01/2015							
1	1	÷	✓	✓	=	=							
2	2	÷	✓	✓	=	=							
3	3	÷	✓	✓	=	=							
4	4	÷	✓	✓	=	=							
5	5	÷	✓	✓	=	=							
6	6	÷	✓	✓	=	=							
7	7	÷	✓	✓	=	=							
8	8	÷	✓	✓	=	=							
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	14	÷	N	N	N	-							
	15	÷	N	N	N	-							
	16	÷	N	N	N	-							
	17	÷	N	N	N	-							
	18	÷	N	N	N	-							
	19	÷	N	N	N	-							
	20	÷	N	N	N	-							

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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27765 7590 06/08/2015

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P.O. BOX 506
MERRIFIELD, VA 22116

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Shelley Kuo	(Depositor's name)
/Shelley Kuo/	(Signature)
08/26/2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	05/02/2013	Ching-Wen Hung	NAUP1622USA	7170

TITLE OF INVENTION:

SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$960	\$0	\$0	\$960	09/08/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
Huynh, Andy	2818	257-365000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Winston Hsu
2 Scott Margo
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

UNITED MICROELECTRONICS CORP.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
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☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3105 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Winston Hsu/

Date 08/25/2015

Typed or printed name Winston Hsu

Registration No. 41,526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal				
Application Number:		13875293		
Filing Date:		02-May-2013		
Title of Invention:		SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE		
First Named Inventor/Applicant Name:		Ching-Wen Hung		
Filer:		Winston Hsu/Shelley Kuo		
Attorney Docket Number:		NAUP1622USA		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	23310739
Application Number:	13875293
International Application Number:	
Confirmation Number:	7170
Title of Invention:	SEMICONDUCTOR STRUCTURE WITH HARD MASK DISPOSED ON THE GATE STRUCTURE
First Named Inventor/Applicant Name:	Ching-Wen Hung
Customer Number:	27765
Filer:	Winston Hsu/Shelley Kuo
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1622USA
Receipt Date:	26-AUG-2015
Filing Date:	02-MAY-2013
Time Stamp:	03:33:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	12564
Deposit Account	503105
Authorized User	HSU, WINSTON
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NAUP1622USA0_AN_1_NP072.pdf	334397	no	1
			9a9b102daa48aeba5822307cf615e85ffd2a34		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30444	no	2
			ef200112515610e2b5a2a77300cd5b48af84096f		

Warnings:

Information:

Total Files Size (in bytes):	364841
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/875,293	09/29/2015	9147747	NAUP1622USA	7170

27765 7590 09/09/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 35 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Ching-Wen Hung, Tainan City, TAIWAN;
Chih-Sen Huang, Tainan City, TAIWAN;
UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN

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