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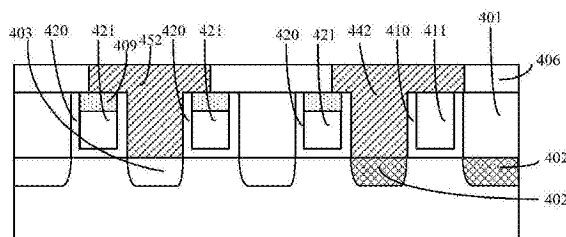
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(54)发明名称

半导体结构及其形成方法

(57)摘要

半导体结构及其形成方法,其中,半导体结构的形成方法包括:半导体衬底表面的第一介质层内具有第一开口和第二开口,第一开口两侧的半导体衬底内都具有第一掺杂区,第一开口内具有第一金属栅,第二开口内具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;在第一介质层表面覆盖第二介质层,第二介质层相对于第三介质层具有刻蚀选择性;在第二介质层和第一介质层内形成第一接触层,第一接触层与至少一个第一掺杂区和至少一个第一金属栅电连接。所述半导体结构的形成工艺简单。



1. 一种半导体结构的形成方法,其特征在于,包括:

提供半导体衬底,所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底的第一开口和第二开口,第一开口两侧的半导体衬底内均具有第一掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;

在所述第一金属栅、第三介质层和第一介质层表面覆盖第二介质层,所述第二介质层相对于第三介质层具有刻蚀选择性;

在所述第二介质层和第一介质层内形成第四开口,所述第四开口暴露出至少一个第一掺杂区和第一金属栅的表面;

在所述第四开口内形成第一接触层,所述第一接触层与第一金属栅以及至少一个第一掺杂区电连接。

2. 如权利要求1所述半导体结构的形成方法,其特征在于,所述第四开口还暴露出部分第三介质层表面;位于所述第四开口内的第一接触层与所述第二金属栅之间通过所述第三介质层电隔离。

3. 如权利要求1所述半导体结构的形成方法,其特征在于,所述第一开口的数量大于或等于1,所述第二开口的数量大于或等于1。

4. 如权利要求1所述半导体结构的形成方法,其特征在于,所述第四开口的形成方法为:在所述第二介质层表面形成掩膜层,所述掩膜层暴露出与至少一个第一掺杂区和至少一个第一金属栅位置对应的第二介质层表面;以所述掩膜层为掩膜,采用各向异性的干法刻蚀工艺刻蚀所述第二介质层和第一介质层,直至暴露出第一掺杂区表面为止。

5. 如权利要求1所述半导体结构的形成方法,其特征在于,所述第一开口、第二开口和第一掺杂区的形成工艺为:在半导体衬底表面形成第二伪栅极结构和若干相邻的第一伪栅极结构,所述第一伪栅极结构和第二伪栅极结构的材料为多晶硅;采用离子注入工艺在各第一伪栅极结构两侧的半导体衬底内分别形成第一掺杂区;在形成所述第一掺杂区之后,在所述半导体衬底、第一伪栅极结构和第二伪栅极结构的侧壁和顶部表面沉积第一介质薄膜;采用化学机械抛光工艺去除高于第一伪栅极结构和第二伪栅极结构表面的第一介质薄膜,形成与第一伪栅极结构和第二伪栅极结构表面齐平的第一介质层;在形成所述第一介质层之后,去除所述第一伪栅极结构并形成第一开口,去除所述第二伪栅极结构并形成第二开口。

6. 如权利要求5所述半导体结构的形成方法,其特征在于,在形成第一介质薄膜之前,在所述半导体衬底、第一伪栅极结构和第二伪栅极结构的侧壁和顶部表面沉积阻挡层,所述阻挡层的材料为氮化硅、氮氧化硅、碳化硅或碳氮化硅;所述化学机械抛光工艺停止于所述阻挡层表面,并进行过抛光暴露出第一伪栅极结构和第二伪栅极结构表面。

7. 如权利要求1所述半导体结构的形成方法,其特征在于,还包括:在栅介质层两侧的半导体衬底表面形成侧墙,所述侧墙的材料为氧化硅、氮化硅和低K介质材料中的一种或多种组合。

8. 如权利要求1所述半导体结构的形成方法,其特征在于,还包括:在第一栅介质层和第一金属栅之间形成第一功函数层,以及位于第二栅介质层和第二金属栅之间的第二功函数层,所述第一功函数层和第二功函数层的材料为钛、钽、氮化钛、氮化钽、钴、氮化钛铝、钛铝钴、钨、铜锰、氮化钛铝、钛铝或钨。

9. 如权利要求1所述半导体结构的形成方法,其特征在于,所述栅介质层的材料为高K介质材料,所述第一金属栅和第二金属栅的材料为铜、钨、铝或银,所述第一介质层和第二介质层的材料为氧化硅和低K介质材料中的一种,所述第三介质层的材料为氮化硅,所述第一接触层的材料为钛或钨。

10. 一种半导体结构,其特征在于,包括:半导体衬底;位于所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底的第一开口和第二开口,第一开口两侧的半导体衬底内均具有第一掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;位于所述第一金属栅、第三介质层和第一介质层表面的第二介质层,所述第二介质层相对于第三介质层具有刻蚀选择性;位于所述第二介质层和第一介质层内的第四开口,所述第四开口暴露出至少一个第一掺杂区和至少一个第一金属栅的表面;位于所述第四开口内的第一接触层,所述第一接触层与第一金属栅以及至少一个第一掺杂区电连接。

11. 如权利要求10所述半导体结构,其特征在于,所述第四开口还暴露出部分第三介质层表面;位于所述第四开口内的第一接触层与所述第二金属栅之间通过所述第三介质层电隔离。

12. 如权利要求10所述半导体结构,其特征在于,所述第一开口的数量大于或等于1,所述第二开口的数量大于或等于1。

13. 如权利要求10所述半导体结构,其特征在于,还包括:位于第一介质层与半导体衬底和栅介质层之间的阻挡层,所述阻挡层的材料为氮化硅、氮氧化硅、碳化硅或碳氮化硅。

14. 如权利要求10所述半导体结构,其特征在于,还包括:位于栅介质层两侧的半导体衬底表面的侧墙,所述侧墙的材料为氧化硅、氮化硅和低K介质材料中的一种或多种组合。

15. 如权利要求10所述半导体结构,其特征在于,还包括:位于栅介质层和第一金属栅之间的第一功函数层,以及位于栅介质层和第二金属栅之间的第二功函数层,所述第一功函数层和第二功函数层的材料为钛、钽、氮化钛、氮化钽、钴、氮化钛铝、钛铝钴、钨、铜锰、氮化钛铝、钛铝或钨。

16. 如权利要求10所述半导体结构,其特征在于,所述栅介质层的材料为高K介质材料,所述第一金属栅和第二金属栅的材料为铜、钨、铝或银,所述第一介质层和第二介质层的材料为氧化硅和低K介质材料中的一种,所述第三介质层的材料为氮化硅,所述第一接触层的材料为钛或钨。

17. 一种半导体结构的形成方法,其特征在于,包括:

提供半导体衬底,所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底第一开口、以及若干相邻的第二开口,第一开口两侧的半导体衬底内均具有

第一掺杂区,相邻的第二开口之间的半导体衬底内具有第二掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;

在所述第一金属栅、第三介质层和第一介质层表面覆盖第二介质层,所述第二介质层的材料相对于第三介质层具有刻蚀选择性;

在第二介质层和第一介质层内形成第四开口和第五开口,所述第四开口至少暴露出第一金属栅表面,所述第五开口暴露出至少一个第二掺杂区表面;

在所述第四开口内形成第一接触层,在所述第五开口形成第二接触层,所述第一接触层至少与第一金属栅电连接,所述第二接触层与至少一个第二掺杂区电连接。

18.如权利要求17所述半导体结构的形成方法,其特征在于,所述第四开口还暴露出至少一个第一掺杂区的表面;位于所述第四开口内的所述第一接触层与第一金属栅以及至少一个第一掺杂区电连接。

19.如权利要求18所述半导体结构的形成方法,其特征在于,所述第四开口和第五开口的形成方法为:在所述第二介质层表面形成掩膜层,所述掩膜层具有第六开口和第七开口,所述第六开口暴露出与第一金属栅以及至少一个第一掺杂区位置对应的第二介质层表面,所述第七开口暴露出与至少一个第二掺杂区表面位置对应的第二介质层表面;以所述掩膜层为掩膜,采用各向异性的干法刻蚀工艺刻蚀所述第二介质层和第一介质层,直至暴露出第一掺杂区和第二掺杂区的表面为止。

20.如权利要求17所述半导体结构的形成方法,其特征在于,所述第四开口的底部具有第一介质层与第一掺杂区电隔离;位于所述第四开口内的第一接触层仅与第一金属栅电连接,且与所述第一掺杂区通过第一介质层电隔离。

21.如权利要求20所述半导体结构的形成方法,其特征在于,所述第四开口和第五开口的形成方法为:在所述第二介质层表面形成掩膜层,所述掩膜层具有第六开口和第七开口,所述第六开口暴露出与第一金属栅位置对应的第二介质层表面,所述第七开口暴露出与至少一个第二掺杂区的位置对应的第二介质层表面;以所述掩膜层为掩膜,采用各向异性的干法刻蚀工艺刻蚀所述第六开口和第七开口底部的第二介质层直至暴露出第一介质层为止,在所述第六开口底部形成暴露出第一金属栅的第四开口;在所述第四开口内形成保护层,以所述保护层和掩膜层为掩膜,继续采用各向异性的干法刻蚀工艺刻蚀所述第一介质层,直至暴露出第二掺杂区的表面为止,形成第五开口,并去除所述保护层。

22.如权利要求17所述半导体结构的形成方法,其特征在于,所述第四开口还暴露出部分第三介质层表面;位于所述第四开口内的第一接触层与所述第二金属栅之间通过所述第三介质层电隔离。

23.如权利要求17所述半导体结构的形成方法,其特征在于,所述第五开口还暴露出部分第三介质层表面;位于所述第五开口内的第二接触层与所述第二金属栅之间通过所述第三介质层电隔离。

24.如权利要求17所述半导体结构的形成方法,其特征在于,所述第一开口的数量大于或等于1,所述第二开口的数量大于或等于1。

25. 如权利要求17所述半导体结构的形成方法,其特征在于,还包括:在栅介质层两侧的半导体衬底表面形成侧墙,所述侧墙的材料为氧化硅、氮化硅和低K介质材料中的一种或多种组合。

26. 如权利要求17所述半导体结构的形成方法,其特征在于,所述第一开口、第二开口和第一掺杂区的形成工艺为:在半导体衬底表面形成若干相邻的第一伪栅极结构、和若干相邻的第二伪栅极结构,所述第一伪栅极结构和第二伪栅极结构的材料为多晶硅;采用离子注入工艺在各第一伪栅极结构两侧的半导体衬底内均形成第一掺杂区,在第二伪栅极结构之间的半导体衬底内形成第二掺杂区;在形成所述第一掺杂区和第二掺杂区之后,在所述半导体衬底、第一伪栅极结构和第二伪栅极结构的侧壁和顶部表面沉积第一介质薄膜;采用化学机械抛光工艺去除高于第一伪栅极结构和第二伪栅极结构表面的第一介质薄膜,形成与第一伪栅极结构和第二伪栅极结构表面齐平的第一介质层;在形成所述第一介质层之后,去除所述第一伪栅极结构并形成第一开口,去除所述第二伪栅极结构并形成第二开口。

27. 如权利要求26所述半导体结构的形成方法,其特征在于,在形成第一介质薄膜之前,在所述半导体衬底、第一伪栅极结构和第二伪栅极结构的侧壁和顶部表面沉积阻挡层,所述阻挡层的材料为氮化硅、氮氧化硅、碳化硅或碳氮化硅;所述化学机械抛光工艺停止于所述阻挡层表面,并进行过抛光暴露出第一伪栅极结构和第二伪栅极结构表面。

28. 如权利要求17所述半导体结构的形成方法,其特征在于,还包括:在栅介质层和第一金属栅之间形成第一功函数层,以及位于栅介质层和第二金属栅之间的第二功函数层,所述第一功函数层和第二功函数层的材料为钛、钽、氮化钛、氮化钽、钴、氮化钛铝、钛铝钴、钒、铜锰、氮化钛铝、钛铝或钨。

29. 如权利要求17所述半导体结构的形成方法,其特征在于,所述介质层的材料为高K介质材料,所述第一金属栅和第二金属栅的材料为铜、钨、铝或银,所述第一介质层和第二介质层的材料为氧化硅和低K介质材料中的一种,所述第三介质层的材料为氮化硅,所述第一接触层的材料为钛或钨。

30. 一种半导体结构,其特征在于,包括:半导体衬底,所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底第一开口、以及若干相邻的第二开口,第一开口两侧的半导体衬底内均具有第一掺杂区,相邻的第二开口之间的半导体衬底内具有第二掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;位于所述第一金属栅、第三介质层和第一介质层表面的第二介质层,所述第二介质层的材料相对于第三介质层具有刻蚀选择性;位于所述第二介质层和第一介质层内的第四开口和第五开口,所述第四开口暴露出至少一个第一金属栅表面,所述第五开口暴露出至少一个第二掺杂区表面;位于所述第四开口内的第一接触层,以及位于所述第五开口内的第二接触层,所述第一接触层至少与第一金属栅电连接,所述第二接触层与至少一个第二掺杂区电连接,所述第一接触层与至少一个第一金属栅电连接,所述第二接触层与至少一个第二掺杂区电连接。

31. 如权利要求30所述半导体结构,其特征在于,所述第一接触层与第一金属栅以及至少一个第一掺杂区电连接。

32. 如权利要求30所述半导体结构,其特征在于,所述第一接触层与第一金属栅电连接,且与所述第一掺杂区通过第一介质层电隔离。

33. 如权利要求30所述半导体结构,其特征在于,所述第一开口的数量大于或等于1,所述第二开口的数量大于或等于1。

34. 如权利要求30所述半导体结构,其特征在于,所述第四开口还暴露出部分第三介质层表面;位于所述第四开口内的第一接触层与所述第二金属栅之间通过所述第三介质层电隔离。

35. 如权利要求30所述半导体结构,其特征在于,所述第五开口还暴露部分出所述第三介质层表面;位于所述第五开口内的第二接触层与所述第二金属栅之间通过所述第三介质层电隔离。

36. 如权利要求30所述半导体结构,其特征在于,位于第一介质层与半导体衬底、第一栅介质层和第二栅介质层之间的阻挡层,所述阻挡层的材料为氮化硅、氮氧化硅、碳化硅或碳氮化硅。

37. 如权利要求30所述半导体结构,其特征在于,还包括:位于栅介质层两侧的半导体衬底表面的侧墙,所述侧墙的材料为氧化硅、氮化硅和低K介质材料中的一种或多种组合。

38. 如权利要求30所述半导体结构,其特征在于,还包括:位于栅介质层和第一金属栅之间的第一功函数层,以及位于栅介质层和第二金属栅之间的第二功函数层,所述第一功函数层和第二功函数层的材料为钛、钽、氮化钛、氮化钽、钴、氮化钛铝、钛铝钴、钌、铜锰、氮化钛铝、钛铝或钨。

39. 如权利要求30所述半导体结构,其特征在于,所述栅介质层的材料为高K介质材料,所述第一金属栅和第二金属栅的材料为铜、钨、铝或银,所述第一介质层和第二介质层的材料为氧化硅和低K介质材料中的一种,所述第三介质层的材料为氮化硅,所述第一接触层的材料为钛或钨。

## 半导体结构及其形成方法

### 技术领域

[0001] 本发明涉及半导体制造技术领域,尤其涉及半导体结构及其形成方法。

### 背景技术

[0002] 随着集成电路制造技术的快速发展,促使集成电路中的半导体器件,尤其是MOS (Metal Oxide Semiconductor,金属-氧化物-半导体)器件的尺寸不断地缩小,以此满足集成电路发展的小型化和集成化的要求。在MOS晶体管器件的尺寸持续缩小的过程中,现有工艺以氧化硅或氮氧化硅作为栅介质层的工艺受到了挑战。以氧化硅或氮氧化硅作为栅介质层所形成的晶体管出现了一些问题,包括漏电流增加以及杂质的扩散,从而影响晶体管的阈值电压,进而影响半导体器件的性能。

[0003] 为解决以上问题,含有高K介质层和金属栅极结构的晶体管被提出。所述含有高K介质层和金属栅极结构的晶体管采用高K(介电常数)材料代替常用的氧化硅或氮氧化硅栅介质材料,能够使晶体管尺寸缩小的同时,减小漏电流的产生,并提高晶体管的性能。

[0004] 现有技术具有高K介质层和金属栅极结构的晶体管如图1所示,包括:位于半导体衬底100表面的第一介质层105,所述第一介质层105内具有暴露出半导体衬底100表面的开口(未示出);位于所述开口的侧壁和底部表面的高K栅介质层101;位于所述高K栅介质层101表面的金属栅极层103,位于高K栅介质层101和金属栅极层103两侧的半导体衬底100表面的侧墙104;位于高K栅介质层101、金属栅极层103和侧墙104两侧的半导体衬底100内的源区106a和漏区106b。

[0005] 在形成如图1所示晶体管之后,进行半导体器件的后段工艺(BEOL, Back End Of Line),使所述晶体管的源极、漏极或栅极能够与集成电路中的其他半导体器件电连接。

[0006] 然而,现有的具有高K介质层和金属栅极结构的晶体管的后段工艺较为复杂,会增加工艺时间及成本。

[0007] 更多含有晶体管的后段工艺的相关资料请参考公开号为US2007/0210339的美国专利文件。

### 发明内容

[0008] 本发明解决的问题是提供半导体结构及其形成方法,改善具有高K介质层和金属栅极结构的晶体管的后段工艺,从而提高工艺效率,减少工艺成本。

[0009] 为解决上述问题,本发明提供一种半导体结构的形成方法,包括:提供半导体衬底,所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底的第一开口和第二开口,第一开口两侧的半导体衬底内均具有第一掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;在所述

第一金属栅、第三介质层和第一介质层表面覆盖第二介质层,所述第二介质层相对于第三介质层具有刻蚀选择性;在所述第二介质层和第一介质层内形成第四开口,所述第四开口暴露出至少一个第一掺杂区和第一金属栅的表面;在所述第四开口内形成第一接触层,所述第一接触层与第一金属栅以及至少一个第一掺杂区电连接。

[0010] 相应地,本发明还提供一种半导体结构,包括:半导体衬底;位于所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底第一开口和第二开口,第一开口两侧的半导体衬底内均具有第一掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;位于所述第一金属栅、第三介质层和第一介质层表面的第二介质层,所述第二介质层相对于第三介质层具有刻蚀选择性;位于所述第二介质层和第一介质层内的第四开口,所述第四开口暴露出至少一个第一掺杂区和至少一个第一金属栅的表面;位于所述第四开口内的第一接触层,所述第一接触层与第一金属栅以及至少一个第一掺杂区电连接。

[0011] 本发明还提供一种半导体结构的形成方法,包括:提供半导体衬底,所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底第一开口、以及若干相邻的第二开口,第一开口两侧的半导体衬底内均具有第一掺杂区,相邻的第二开口之间的半导体衬底内具有第二掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;在所述第一金属栅、第三介质层和第一介质层表面覆盖第二介质层,所述第二介质层的材料相对于第三介质层具有刻蚀选择性;在第二介质层和第一介质层内形成第四开口和第五开口,所述第四开口至少暴露出第一金属栅表面,所述第五开口暴露出至少一个第二掺杂区表面;在所述第四开口内形成第一接触层,在所述第五开口形成第二接触层,所述第一接触层至少与第一金属栅电连接,所述第二接触层与至少一个第二掺杂区电连接。

[0012] 相应的,本发明还提供一种半导体结构,包括:半导体衬底,所述半导体衬底表面具有第一介质层,所述第一介质层内具有暴露出半导体衬底第一开口、以及若干相邻的第二开口,第一开口两侧的半导体衬底内均具有第一掺杂区,相邻的第二开口之间的半导体衬底内具有第二掺杂区,所述第一开口和第二开口的底部和侧壁表面具有栅介质层,所述第一开口的栅介质层表面具有第一金属栅,所述第二开口的栅介质层表面具有第二金属栅,所述第二金属栅的顶部表面低于所述第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层,所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;位于所述第一金属栅、第三介质层和第一介质层表面的第二介质层,所述第二介质层的材料相对于第三介质层具有刻蚀选择性;位于所述第二介质层和第一介质层内形成第四开口和第五开口,所述第四开口暴露出至少一个第一金属栅表面,所述第五开口暴露出至少一个第二掺杂区表面;位于所述第四开口内的第一接

触层,以及位于所述第五开口内的第二接触层,所述第一接触层至少与第一金属栅电连接,所述第二接触层与至少一个第二掺杂区电连接。

[0013] 与现有技术相比,本发明的技术方案具有以下优点:

[0014] 使所述第二金属栅的顶部表面低于第一金属栅的顶部表面,并在所述第二金属栅表面形成第三介质层,使所述第三介质层的表面与第一金属栅的顶部表面齐平,且所述第三介质层相对于第一介质层具有刻蚀选择性;当后续形成第二介质层之后,在所述第二介质层和第一介质层内形成暴露出至少一个第一掺杂区和第一金属栅的第四开口时,所述第三介质层能够保护所述第二金属栅的表面;并使后续形成于所述第四开口内的第一接触层与第二金属栅电隔离的同时,与至少一个第一掺杂区和至少一个第一金属栅电连接;所述第一接触层能够作为连接第一掺杂区和第一金属栅的共享接触结构(Share Contact);其次,所述第四开口仅需采用一次刻蚀工艺即可形成,而且后续仅采用一次填充金属的工艺即可形成第一接触层,能够简化工艺。

[0015] 半导体结构中,第二金属栅的顶部表面、低于第一金属栅的顶部表面,且所述第二金属栅表面具有第三介质层;所述第一金属栅、第三介质层和第一介质层表面具有第二介质层,而所述第二介质层和第一介质层内的第四开口暴露出至少一个第一掺杂区和第一金属栅的表面;因此,位于所述第四开口内具有第一接触层能够与至少一个第一掺杂区和第一金属栅电连接,作为共享接触结构,且所述第一接触层的结构简单,有利于半导体器件的集成。

[0016] 在另一半导体结构的形成方法中,在所述第二介质层和第一介质层内形成暴露出至少一个第一金属栅的第四开口的同时,形成暴露出至少一个第二掺杂区表面的第五开口;从而,后续能够在所述第四开口内形成第一接触层的同时,能够在所述第五开口内形成第二接触层;所述第一接触层能够与至少一个第一金属栅电连接,而与第二金属栅通过第三介质层电隔离;所述第二介质层能够与第二掺杂区电连接,且与第二金属栅通过第三介质层电隔离,能够用于作为自对准接触结构(SAC, Self-Aligned Contact);所述第一接触层和第二接触层同时形成,进一步简化了工艺。

[0017] 所述半导体结构中,位于所述第一金属栅、第三介质层和第一介质层表面的第二介质层和第一介质层内同时具有第一接触层和第二接触层;所述第一接触层能够与至少一个第一金属栅电连接,而与第二金属栅通过第三介质层电隔离;而所述第二接触层能够与第二掺杂区电连接,且与第二金属栅通过第三介质层电隔离,能够用于作为自对准接触结构;所述第一接触层和第二接触层的结构简单,有利于半导体器件的集成。

## 附图说明

[0018] 图1是现有技术具有高K介质层和金属栅极结构的晶体管的剖面结构示意图;

[0019] 图2是在具有高K介质层和金属栅极结构的晶体管的后段工艺中所形成共享接触结构示意图;

[0020] 图3至图7是本发明第一实施例所述的半导体结构的形成过程的剖面结构示意图;

[0021] 图8和图9是本发明第二实施例所述的半导体结构的形成过程的剖面结构示意图。

## 具体实施方式

[0022] 如背景技术所述,现有的具有高K介质层和金属栅极结构的晶体管的后段工艺较为复杂,会增加工艺时间及成本。

[0023] 经过本发明的发明人研究发现,请参考图2,现有的具有高K介质层和金属栅极结构的晶体管的后段工艺中,所形成的电互连结构包括共享接触结构(Share Contact),所述共享接触结构由位于源区106a表面的第一导电插塞124、位于金属栅极层103表面的第二导电插塞125、以及位于第一导电插塞124和第二导电插塞125表面的导电层126构成。

[0024] 其中,所述第一导电插塞124和第二导电插塞125需要通过沉积工艺在第一开口和第二开口内填充金属,并采用化学机械抛光工艺去除高于第二介质层120表面的金属,所述导电层126也需要通过沉积工艺、以及所述沉积工艺之后的刻蚀工艺形成。所述共享接触结构的过程较为复杂,不利于提高效率以及降低成本;其次,由于第一开口和第二开口的深宽比较大,容易在填充的金属内产生缺陷,导致器件性能不良;并且,由于所述第一导电插塞124和第二导电插塞125顶部表面的面积相对于第二介质层120的面积过小,后续化学机械抛光工艺时容易造成所述第二介质层120表面的形貌不良,使器件的稳定性降低。

[0025] 经过本发明的发明人进一步研究,提出了一种半导体结构的形成方法,能够简化形成共享接触结构的工艺,并使所形成的共享接触结构简单,有利于半导体器件的集成。

[0026] 为使本发明的上述目的、特征和优点能够更加明显易懂,下面结合附图对本发明的具体实施方式做详细的说明。

[0027] 第一实施例

[0028] 图3至图7是本发明第一实施例所述的半导体结构的形成过程的剖面结构示意图。

[0029] 请参考图3,提供半导体衬底400,所述半导体衬底400表面具有第一介质层401,所述第一介质层401内具有第二开口(未示出)和第一开口(未示出),所述第一开口和第二开口暴露出半导体衬底400,各第一开口两侧的半导体衬底400内均具有第一掺杂区402,所述第一开口底部和侧壁表面具有第一栅介质层410,所述第一栅介质层410表面具有第一金属栅411,所述第二开口底部和侧壁表面具有第二栅介质层420,所述第二栅介质层420表面具有第二金属栅421,所述第一金属栅411和第二金属栅421的表面均与所述第一介质层401的表面齐平。

[0030] 所述半导体衬底400用于为后续工艺提供工作平台;所述半导体衬底400为硅衬底、硅锗衬底、碳化硅衬底、绝缘体上硅(SOI)衬底、绝缘体上锗(GOI)衬底、玻璃衬底或III-V族化合物衬底(例如氮化硅或砷化镓等)。

[0031] 所述第一栅介质层410和第二栅介质层420的材料为高K介质材料,所述高K介质材料包括:氧化铪、氧化锆、氧化铪硅、氧化镧、氧化锆硅、氧化钛、氧化钽、氧化钡锆钛、氧化钡钛、氧化锆钛或氧化铝;所述第一金属栅411和第二金属栅421的材料为金属,所述金属包括:铜、钨、铝或银。

[0032] 所述第一开口的数量等于1或大于1;当所述第一开口的数量大于1,且若干第一开口相邻时,所述第一掺杂区402位于相邻第一开口之间的半导体衬底400内;所述第一掺杂区402作为所形成的晶体管内的源区和漏区;此外,所述第一开口能够与第二开口相邻,且第一掺杂区402位于相邻第一开口和第二开口之间的半导体衬底400内;此外,所述第二开口的数量也能够等于1或大于1,而相邻的第二开口之间具有第二掺杂区403,且位于边缘的第二开口与位于边缘的第一开口相邻;在本实施例中,所述第一开口为1个,所述第二开口

的数量为3个,且3个第二开口相邻。

[0033] 在一实施例中,所述第一栅介质层410和第一金属栅411之间具有第一功函数层(未示出),所述第二栅介质层420和第二金属栅421之间具有第二功函数层(未示出);所述第一功函数层和第二功函数层的材料为钛、钽、氮化钛、氮化钽、钴、氮化钛铝、钛铝钴、钨、铜锰、氮化钛铝、钛铝或钨;所述第一功函数层和第二功函数层用于调节所形成的晶体管的阈值电压,当所形成的晶体管为PMOS管时,所述第一功函数层或第二功函数层的材料需具有较高的功函数,当所形成的晶体管为NMOS管时,所述第一功函数层或第二功函数层的材料需具有较低的功函数,以降低所形成的晶体管的阈值电压。

[0034] 在另一实施例中,所述第一栅介质层410和第二栅介质层420的表面还形成有保护层(未示出),所述保护层的材料为氮化钛或氮化钽,用于隔离所述第一栅介质层410与第一金属栅411,以及第二栅介质层420与第二金属栅421;所述保护层用于防止在晶体管的形成过程中,杂质经过栅介质层进入功函数层或金属栅内造成污染,或在晶体管工作时,防止在所述栅介质层和金属栅之间产生漏电流,提高隔离效果。

[0035] 所述第一开口、第二开口、第一掺杂区402和第二掺杂区403的形成工艺为:在半导体衬底400表面形成若干相邻的第一伪栅极结构(未示出)和第二伪栅极结构(未示出),所述第一伪栅极结构和第二伪栅极结构的材料为多晶硅;采用离子注入工艺在各第一伪栅极结构两侧的半导体衬底400内形成第一掺杂区402,在相邻第二伪栅极结构之间的半导体衬底400内形成第二掺杂区403;在形成所述第一掺杂区402和第二掺杂区403之后,在所述半导体衬底400、第一伪栅极结构和第二伪栅极结构的侧壁和顶部表面沉积第一介质薄膜;采用化学机械抛光工艺去除高于第一伪栅极结构和第二伪栅极结构表面的第一介质薄膜,形成与第一伪栅极结构和第二伪栅极结构表面齐平的第一介质层401;在形成所述第一介质层401之后,去除所述第一伪栅极结构和以形成第一开口,去除所述第二伪栅极结构以形成第二开口。

[0036] 在形成所述第一开口和第二开口之后,在所述第一开口的侧壁和底部表面沉积栅介质薄膜;在所述栅介质薄膜表面沉积填充所述第一开口的栅电极薄膜;采用化学机械抛光工艺去除高于所述第一介质层401表面的栅介质薄膜和栅电极薄膜,在第一开口内形成第一栅介质层410和第一金属栅411,在第二开口内形成第二栅介质层420和第二金属栅421。

[0037] 在一实施例中,在形成第一介质薄膜之前,还包括:在所述半导体衬底400、第一伪栅极结构和第二伪栅极结构的侧壁和顶部表面沉积阻挡层,所述阻挡层的材料为氮化硅、氮氧化硅、碳化硅或碳氮化硅,且与第一介质层的材料不同;所述阻挡层用于在为采用化学机械抛光工艺去除高于伪栅极结构表面的第一介质薄膜时,定义所述抛光工艺的停止位置,所述化学机械抛光工艺停止于所述阻挡层后,再进行过抛光,以暴露出第一伪栅极结构和第二伪栅极结构的表面。

[0038] 在另一实施例中,在形成所述第一伪栅极结构和第二伪栅极结构之后,形成第一掺杂区402之前,分别在所述第一伪栅极结构和第二伪栅极结构两侧的半导体衬底400表面形成侧墙,所述侧墙的材料为氧化硅、氮化硅和低K介质材料中的一种或多种组合。

[0039] 需要说明的是,由于所述第一栅介质层410和第二栅介质层420的材料为高K介质材料,因此,所述第一栅介质层410和第二栅介质层420与半导体衬底400之间的界面不匹

配,因此需要在第一开口和第二开口内沉积栅介质薄膜之前,采用热氧化工艺在所述第一开口和第二开口底部的半导体衬底400表面形成氧化硅层(未示出),以键合所述第一栅介质层410和第二栅介质层420与半导体衬底400,从而减少漏电流,使器件性能稳定。

[0040] 请参考图4,刻蚀部分所述第二金属栅421,形成第三开口(未示出),使所述第二金属栅421的顶部表面低于所述第一金属栅411的顶部表面;在所述第三开口内形成第三介质层409,所述第三介质层409的表面与第一金属栅411的顶部表面齐平,且所述第三介质层409相对于第一介质层401具有刻蚀选择性。

[0041] 为满足不同工业需求,形成高度不一的晶体管,需要经过刻蚀使所述第二金属栅421顶部表面低于第一金属栅411;而在所述第二金属栅421顶部表面低于第一金属栅411后,在所述第二金属栅421表面形成第三介质层409,能够使所述第二金属栅421与后续形成的第一接触层电隔离。

[0042] 所述第三开口的形成工艺为刻蚀工艺,较佳的是各向异性的干法刻蚀工艺;本发明的实施例中,为避免刻蚀工艺中第一金属栅411被刻蚀,还包括:在进行所述刻蚀工艺之前,在所述第一金属栅411表面形成保护层;在所述刻蚀工艺之后,去除所述保护层。

[0043] 需要说明的是,在本发明的其他实施例中,当第二金属栅421和第二栅介质层420之间还具有第二功函数层时,所述功函数层也需要被刻蚀,在此不再赘述。

[0044] 由于后续形成的第一接触层仅需电连接第一金属411和第一掺杂区402,因此,在第一接触层电连接第一掺杂区402和第一金属栅411时,所述第三介质层409能够使所述第一接触层电隔离所述第二金属栅421;此外,所述第三介质层409同时形成于所述第二功函数层和第二金属栅421表面,起到电隔离的作用。

[0045] 所述第三介质层409的材料为氮化硅,形成工艺为:在所述刻蚀第二金属栅421之后,在所述第三开口内、以及第一介质层401和第一金属栅411表面沉积第三介质薄膜;采用化学机械抛光工艺去除高于第一介质层401表面的第三介质薄膜,在所述第二金属栅421表面形成第三介质层409。

[0046] 请参考图5,在所述第一金属栅411、第三介质层409和第一介质层401表面覆盖第二介质层406,所述第二介质层406相对于第三介质层409具有刻蚀选择性;在所述第二介质层406表面形成掩膜层407,所述掩膜层407暴露出至少一个第一掺杂区402和第一金属栅411位置对应的第二介质层406表面。

[0047] 所述第二介质层406的材料为氧化硅和低K介质材料中的一种,所述第二介质层406的形成工艺为沉积工艺,较佳的是化学气相沉积工艺;由于所述第二介质层406形成于第一金属栅411的表面,后续形成于第二介质层406内的第一接触层用于电连接第一金属栅411。

[0048] 所述掩膜层407具有暴露出至少一个第一掺杂区402和第一金属栅411对应位置的第二介质层表面的第六开口440,第六开口440定义了后续形成的第一接触层的位置。所述掩膜层407的材料为光刻胶,其形成工艺为:在所述第二介质层406表面采用旋涂工艺形成光刻胶薄膜;对所述光刻胶薄膜进行曝光显影以图形化,去除与第一金属栅411和第一掺杂区402位置对应的光刻胶薄膜,形成掩膜层407。

[0049] 在本实施例中,所述掩膜层407仅暴露出一个第一金属栅411以及一个第一掺杂区402的对应位置,使后续以所述掩膜层407为掩膜形成的第二开口能够暴露出一个第一金属

栅411和一个第一掺杂区402对应位置,则形成于所述第二开口内的第一接触层能够使所述第一金属栅411和第一掺杂区402电连接,从而构成共享接触结构。

[0050] 需要说明的是,本实施例的掩膜层407还可以暴露出部分与第二金属栅421的位置对应的第二介质层406表面,所述掩膜层407暴露出的区域变大,降低了对于光刻工艺的精度要求;由于所述第二金属栅421表面具有第三介质层409,且所述第三介质层409相对于第二介质层406具有刻蚀选择性,而所述第二金属栅421两侧还具有侧墙;在后续刻蚀形成第二开口时,所述第三介质层409和侧墙能够保护第二金属栅421和第二栅介质层420不受损伤;从而避免了光刻工艺暴露出第一金属栅411时,由于工艺误差而额外暴露出第二金属栅421的问题,进而保证所形成的器件性能稳定。

[0051] 在另一实施例中,所述掩膜层同时暴露出所述第一金属栅411,及其两侧的第一掺杂区402的对应位置;当以所述掩膜层为掩膜,刻蚀第一介质层401和第二介质层406之后,所形成的第二开口能够暴露出所述第一金属栅411、及其两侧的第一掺杂区402表面;使后续形成于所述第二开口内的第一接触层能够与所述第一金属栅411、及其两侧的第一掺杂区402同时电连接。

[0052] 在其他实施例中,当所述第一开口的数量大于1时,所述掩膜层能够暴露出任一第一掺杂区、以及位于所述第一掺杂区两侧的第一金属栅的对应位置,使后续所形成的第一接触层能够同时与所述地任一第一掺杂区、及其两侧的第一金属栅电连接。

[0053] 所述掩膜层409所暴露出的区域尺寸及位置能够根据所需形成的第一接触层的具体工艺需求而进行调整,在此不应过于限定。

[0054] 请参考图6,所述掩膜层407为掩膜,刻蚀所述第二介质层406和第一介质层401,直至暴露出至少一个第一掺杂区402和第一金属栅411表面为止,形成第四开口441。

[0055] 所述刻蚀所述第二介质层406和第一介质层401的工艺较佳的是各向异性的干法刻蚀工艺;由于所述第二介质层406的材料与所述第一金属栅411的材料不同,因此刻蚀所述第二介质层406的工艺不会损伤所述第一金属栅411表面,而位于所述第一金属栅411和第二金属栅421之间的第一介质层401继续被刻蚀;在刻蚀所述第一介质层401时,由于侧墙的保护,使第一金属栅411和第二金属栅421的侧壁表面免受损伤;因此,仅需进行一次光刻和刻蚀工艺即可形成同时暴露出第一掺杂区402和第一金属栅411的第四开口441;而后续仅需采用一次沉积和抛光工艺即可形成同时电连接第一掺杂区402和第一金属栅411的第一接触层,所形成的第一接触层能够作为共享接触结构,而所述第一接触层的形成工艺简单,能够降低工艺成本,且提高工艺效率;而且,所述第四开口441的顶部尺寸较大,使形成于所述第四开口441内的第一接触层的顶部表面尺寸较大,后续采用抛光工艺去除高于第二介质层406表面的金属材料时,对所述第二介质层406的损伤较小,所形成的器件性能更为稳定。

[0056] 所述第二金属栅421的表面具有第三介质层409的保护,因此所形成的第四开口441不会暴露出所述第二金属栅421,后续形成于所述第四开口441内的第一接触层与所述第二金属栅421通过所述第三介质层409电隔离;需要说明的是,在所述刻蚀工艺中,由于部分厚度的第三介质层409会被去除,因此,所述第三介质层409的厚度需要根据所述刻蚀工艺而定,以保证所述第三介质层409的隔离效果。

[0057] 在一实施例中,当所述第一介质层401与半导体衬底400、第一栅介质410和第二栅

介质420之间具有阻挡层时,在刻蚀所述第一介质层401时,与第一栅介质410和第二栅介质420接触的阻挡层被保留,能够进一步保护第一金属栅411和第二金属栅421的侧壁在刻蚀工艺中不受损伤;而位于第四开口441底部的阻挡层在去除第一介质层401之后被去除。

[0058] 在另一实施例中,当所述掩膜层同时暴露出所述第一金属栅411,及其两侧的第一掺杂区402的对应位置时,刻蚀所形成的第四开口能够暴露出所述第一金属栅411,及其两侧的第一掺杂区402表面,后续所形成的第一接触层能够同时电连接所述第一金属栅411,及其两侧的第一掺杂区402。

[0059] 在其他实施例中,所述第一开口的数量大于1,且掩膜层能够暴露出任一第一掺杂区402、以及位于所述第一掺杂区402两侧的第一金属栅411的对应位置时,刻蚀形成的第四开口能够同时暴露出所述第一掺杂区402、及其两侧的第一金属栅411,使后续所形成的第一接触层能够同时与所述第一掺杂区402、以及位于所述第一掺杂区402两侧的第一金属栅411电连接。

[0060] 请参考图7,所述第四开口441(如图6所示)内填充满金属,形成第一接触层442,所述第一接触层442的表面与所述第二介质层406的顶部表面齐平,且所述第一接触层442与至少一个第一金属栅411和至少一个第一掺杂区402电连接。

[0061] 需要说明的是,在所述第四开口441内填充满金属之前,所述去除掩膜层407(如图6所示)。

[0062] 所述第一接触层442的形成步骤为:采用沉积工艺或电镀工艺填充钛或钨金属;在所述第四开口441内填充满金属之后,采用化学机械抛光工艺去除高于第二介质层406表面的金属。

[0063] 由于所述第四开口441的顶部尺寸较大,有利于填充的钛或钨金属,使所形成的第一接触层442的质量良好,所形成的器件性能稳定。而且,所述化学机械抛光工艺去除高于第二介质层406表面的金属时,对所述第二介质层406的表面损伤减小,有利于提高所形成的器件稳定性。

[0064] 在一实施例中,在填充导电材料之前,在所述第二介质层406表面、以及第四开口441的侧壁和底部表面形成停止层(未图出),所述第一接触层442形成于所述停止层表面,所述停止层的材料为氮化钛或氮化钽;所述停止层定义了化学机械抛光的停止位置,当抛光至所述停止层之后,再进行一定的过抛光,以暴露出第二介质层406表面。

[0065] 在本实施例中,所述第一接触层442能够与第一金属栅411和至少一个第一掺杂区402电连接,形成共享接触结构;在另一实施例中,所述第四开口能够同时暴露出所述第一金属栅411,及其两侧的第一掺杂区402表面,使所述第一接触层442能够同时电连接所述第一金属栅411,及其两侧的第一掺杂区402。

[0066] 在其他实施例中,所述第一开口的数量大于1,且第四开口能够同时暴露出所述第一掺杂区402、及其两侧的第一金属栅411,所形成的第一接触层能够同时与所述第一掺杂区402、以及位于所述第一掺杂区402两侧的第一金属栅411电连接。

[0067] 本实施例中,刻蚀所述第二金属栅的顶部,使所述第二金属栅低于第一金属栅的顶部表面,并在所述第二金属栅表面形成第三介质层,所述第三介质层相对于第一介质层以及后续形成的第二介质层均具有刻蚀选择性;因此,在所述第二介质层和第一介质层内形成暴露出至少一个第一掺杂区和至少一个第一金属栅的第四开口时,所述第三介质层能

够保护所述第二金属栅的表面,并使后续形成于所述第四开口内的第一接触层与第二金属栅电隔离;所述第一接触层能够同时与至少一个第一掺杂区和至少一个第一金属栅电连接,并与第二金属栅电隔离,即作为连接第一掺杂区和第一金属栅的共享接触结构;其次,所述第四开口仅需采用一次刻蚀工艺即可形成,而且后续仅采用一次填充金属的工艺即可形成第一接触层,能够简化工艺。

[0068] 相应的,本实施例还提供一种半导体结构,请继续参考图6,包括:半导体衬底400,所述半导体衬底400表面具有第一介质层401,所述第一介质层401内具有若干相邻的第一开口、以及若干相邻的第二开口,所述第一开口和第二开口暴露出半导体衬底400,各第一开口两侧的半导体衬底400内分别具有第一掺杂区402;位于所述第一开口底部和侧壁表面的第一栅介质层410,位于所述第一栅介质层410表面的第一金属栅411,所述第一金属栅411的表面与所述第一介质层401的表面齐平;所述第二开口底部和侧壁表面的第二栅介质层420,位于所述第二栅介质层420表面的第二金属栅421,所述第二金属栅421的顶部表面低于所述第一金属栅411的顶部表面;位于所述第二金属栅421表面的第三介质层409,所述第三介质层409的表面与第一金属栅411的顶部表面齐平,且所述第三介质层409相对于第一介质层401具有刻蚀选择性;覆盖于所述第一金属栅411、第三介质层409和第一介质层401表面的第二介质层406,所述第二介质层406相对于第三介质层409具有刻蚀选择性;位于所述第二介质层406和第一介质层401内的第四开口,所述第四开口暴露出至少一个第一掺杂区402和至少一个第一金属栅411的表面;位于所述第四开口内的第一接触层442,所述第一接触层442的表面与所述第二介质层406的顶部表面齐平,且所述第一接触层442与至少一个第一掺杂区402和至少一个第一金属栅411电连接。

[0069] 本实施例的半导体结构中,第一接触层与至少一个第一掺杂区和至少一个第一金属栅电连接,并与第二金属栅通过第三介质层电隔离,作为共享接触结构,且所述第一接触层的结构简单,有利于半导体器件的集成。

## [0070] 第二实施例

[0071] 与本发明的第一实施例不同,本发明的第二实施例中,能够同时形成第一接触层和第二接触层,所述第一接触层作为共享接触结构,而所述第二接触层作为自对准接触结构。

[0072] 在形成如第一实施例的图4所示结构的基础上,请参考图8,在所述第三介质层409、第一金属栅411和第一介质层401表面形成第二介质层406,所述第二介质层406相对于所述第三介质层409具有刻蚀选择性;在所述第二介质层406表面形成掩膜层407,所述掩膜层407内具有第六开口(未示出)和第七开口(未示出),所述第六开口暴露出与至少一个第一金属栅411位置对应的第二介质层406表面,所述第七开口暴露出与至少一个第二掺杂区403的位置对应的第二介质层406表面;以所述掩膜层407为掩膜,刻蚀所述第二介质层406和第一介质层401,在第二介质层406和第一介质层401内形成第四开口441和第五开口451,所述第四开口441暴露出至少一个第一金属栅411表面,所述第五开口451暴露出至少一个第二掺杂区403表面。

[0073] 所述第二介质层406和掩膜层407的材料及形成工艺如第一实施例所述的第二介质层和掩膜层,在此不作赘述。

[0074] 所述掩膜层407在暴露出与至少一个第一金属栅411位置对应的同时,所述第七开

口还暴露出与至少一个第二掺杂区403的位置对应的第二介质层406表面;同时刻蚀第二介质层406和第一介质层401,能够形成暴露出至少一个第一金属栅411的第四开口441,以及暴露出至少一个第二掺杂区403的第五开口451;进而,后续能够同时在第四开口441内形成第一接触层,在第五开口451内形成第二接触层,从而使半导体器件的形成工艺进一步简化;其中,所述第二接触层为自对准接触结构,而第一接触层为共享接触结构。

[0075] 所述掩膜层407内的第七开口定义了后续需要形成第二接触层的位置及图形,使所述第二接触层能够与至少一个第二掺杂区403电连接;由于第二金属栅421表面均形成有第三介质层409,且所述第三介质层409相对于第二介质层406和第一介质层401具有刻蚀选择性,使刻蚀第二介质层406的工艺停止于所述第三介质层409表面,而位于相邻第二金属栅421之间的第一介质层401继续被刻蚀,并暴露出第二掺杂区403;后续形成于所述第二掺杂区403表面的第二接触层能够通过所述第三介质层409与第二金属栅421电隔离;因此,所述第七开口能够在暴露出所述第二掺杂区403的对应位置的同时,暴露出部分第三介质层409的对应位置,使所述第七开口的尺寸较大,降低了形成所述第七开口时对于光刻工艺的精度要求。

[0076] 在一实施例中,所述第四开口441能够同时暴露出至少一个第一金属栅411表面、以及至少一个第一掺杂区402的表面;则后续形成于所述第四开口441内的所述第一接触层与至少一个第一掺杂区402和至少一个第一金属栅411电连接,使所述第一接触层作为共享接触结构;在本实施例中,所述第四开口441暴露出第一金属栅411和第一掺杂区402的表面,所述第四开口441和第五开口451的形成方法为:以所述掩膜层407为掩膜,采用各向异性的干法刻蚀工艺刻蚀所述第二介质层和第一介质层,直至暴露出第一掺杂区402和第二掺杂区403的表面为止。

[0077] 本实施例中的第四开口441的实施例与第一实施例中的第四开口相同,在此不做赘述。

[0078] 在另一实施例中,所述第四开口能够仅暴露出至少一个第一金属栅的表面,而所述第四开口的底部具有第一介质层401与第一掺杂区电隔离402;则形成于所述第四开口内的第一接触层与至少一个第一金属栅411电连接,且与所述第一掺杂区402通过第一介质层401电隔离,使所述第一接触层仅用于使第一金属栅411与其他器件电连接;所述第四开口和第五开口的形成方法为:以所述掩膜层407为掩膜,采用各向异性的干法刻蚀工艺刻蚀所述第六开口和第七开口底部的第二介质层406直至暴露出第一介质层401为止,在所述第六开口底部形成暴露出第一金属栅411的第四开口;在所述第四开口内形成保护层,以所述保护层和掩膜层为掩膜,继续采用各向异性的干法刻蚀工艺刻蚀所述第一介质层401,直至暴露出第二掺杂区403的表面为止,形成第五开口,并去除所述保护层。

[0079] 请参考图9,在所述第四开口441(如图8所示)和第五开口451(如图8所示)内填充金属,在所述第四开口441内形成第一接触层442,在所述第五开口451形成第二接触层452,所述第一接触层442和第二接触层452的表面与所述第二介质层406的顶部表面齐平,所述第一接触层442与至少一个第一金属栅411电连接,所述第二接触层452与至少一个第二掺杂区403电连接。

[0080] 所述第一接触层442第二接触层452的材料和形成工艺与第一实施例的第一接触层相同,在此不做赘述。

[0081] 在本实施例中,所述第一接触层408与所述第一金属栅411和第一掺杂区402a电连接,作为共享接触结构;所述第二接触层452与第二掺杂区403电连接,与第二金属栅421之间分别由第三介质层409电隔离,作为自对准接触结构。

[0082] 在其他实施例中,所述第一接触层与至少一个第一金属栅411电连接,且与所述第一掺杂区402通过第一介质层401电隔离,使所述第一接触层仅用于使第一金属栅411与其他器件电连接,以满足具体的工业需求。

[0083] 本实施例能够在形成第一接触层的同时,形成第二接触层,进一步简化了工艺;所述第一接触层能够同时与至少一个第一掺杂区和至少一个第一金属栅电连接,而与第二金属栅通过第三介质层电隔离,能够作为连接第一掺杂区和第一金属栅的共享接触结构;所述第二接触层能够与第二掺杂区电连接,且与第二金属栅通过第三介质层电隔离,能够用于作为自对准接触结构。

[0084] 相应的,本实施例还提供一种半导体结构,本实施例的半导体结构相对于第一实施例所述的半导体结构,其区别在于,请继续参考图9,所述第二介质层406和第一介质层401内具有第四开口和第五开口,所述第四开口暴露出至少一个第一金属栅411表面,所述第五开口暴露出至少一个第二掺杂区403表面;所述第四开口内具有第一接触层442,所述第五开口内具有第二接触层452,所述第一接触层442和第二接触层452的表面与所述第二介质层406的顶部表面齐平,所述第一接触层442与至少一个第一金属栅411电连接,所述第二接触层452与至少一个第二掺杂区403电连接。

[0085] 本实施例的半导体结构中,所述第一接触层能够同时与至少一个第一金属栅电连接,而与第二金属栅通过第三介质层电隔离,能够用于使第一金属栅与其他半导体器件电连接;而所述第二接触层能够与第二掺杂区电连接,且与第二金属栅通过第三介质层电隔离,能够用于作为自对准接触结构。

[0086] 需要说明的是,上述所有实施例仅以平面结构的晶体管为例进行说明。在其他实施例中,所述晶体管结构还可以为三维结构,例如,鳍式场效应管(FinFET)。尤其是在三维结构的晶体管中,本发明实施例所述的晶体管的形成方法具有较好的效果,能够形成性能良好且稳定的三维结构晶体管。具体过程请参考前文的相关描述,在此不再赘述。

[0087] 本发明虽然已以较佳实施例公开如上,但其并不是用来限定本发明,任何本领域技术人员在不脱离本发明的精神和范围内,都可以利用上述揭示的方法和技术内容对本发明技术方案做出可能的变动和修改,因此,凡是未脱离本发明技术方案的内容,依据本发明的技术实质对以上实施例所作的任何简单修改、等同变化及修饰,均属于本发明技术方案的保护范围。

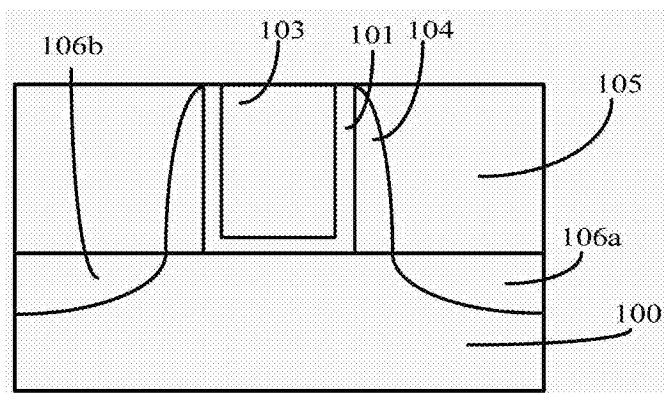


图1

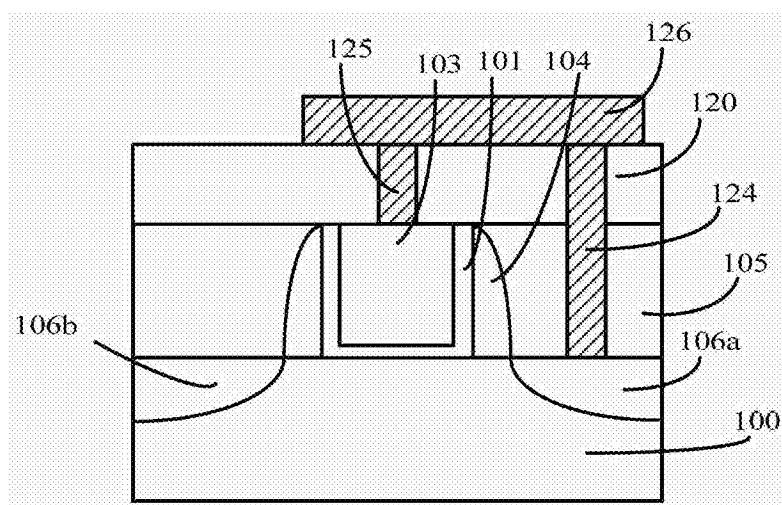


图2

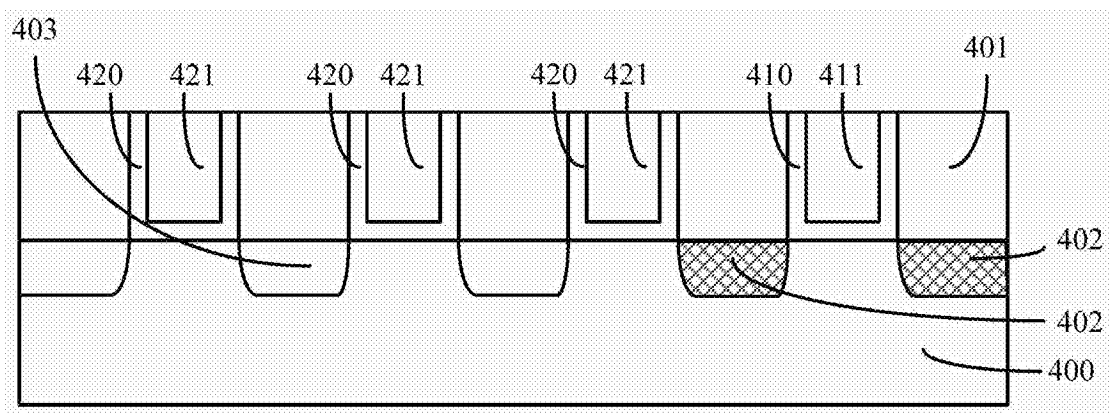


图3

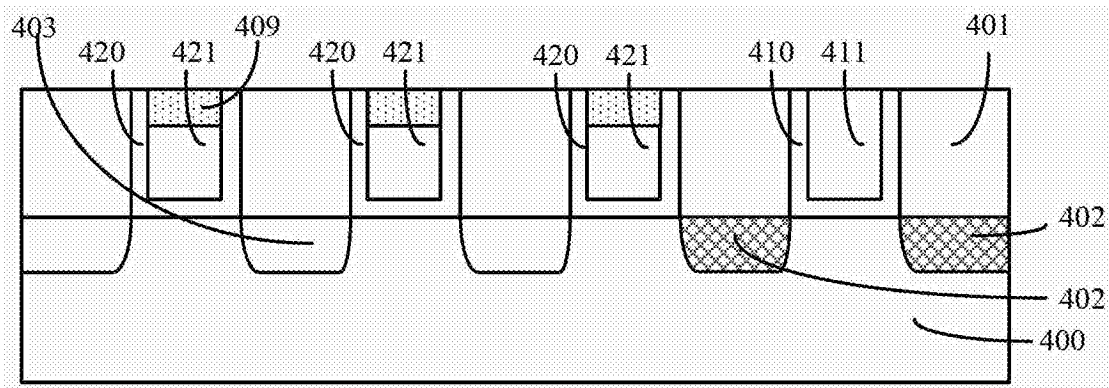


图4

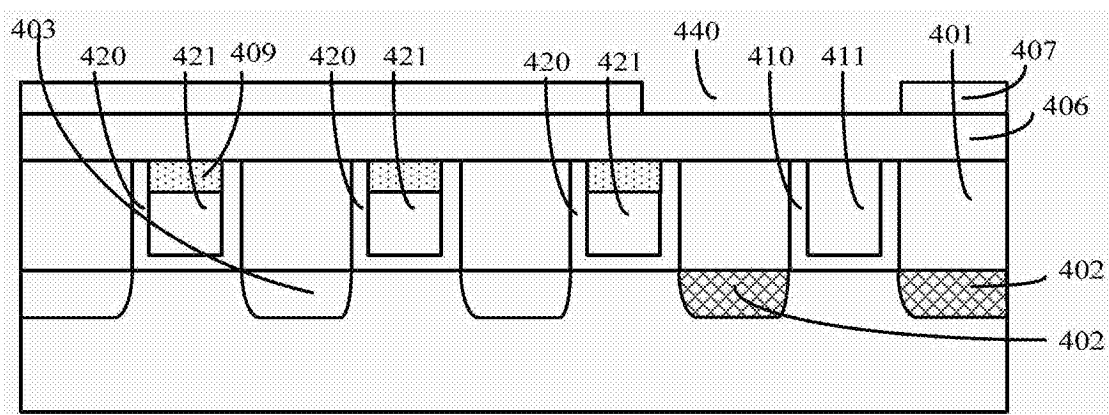


图5

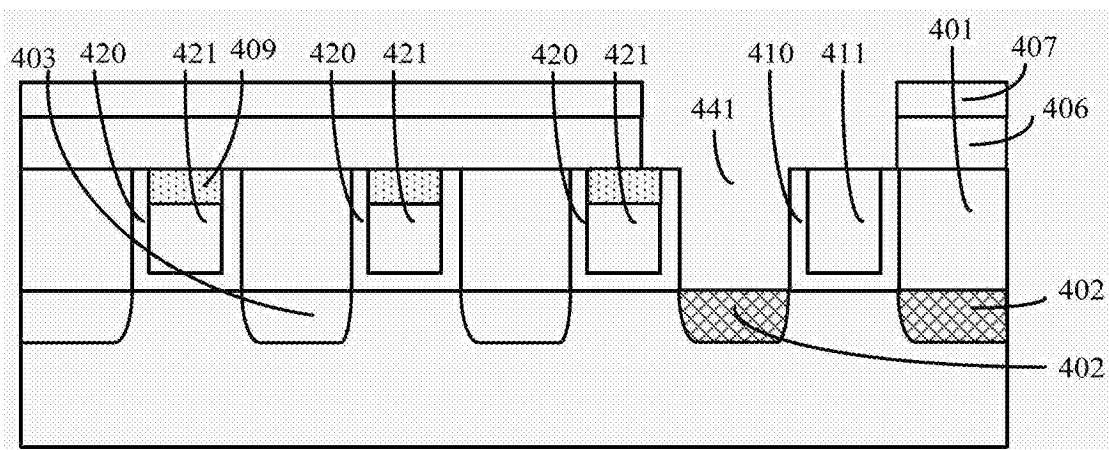


图6

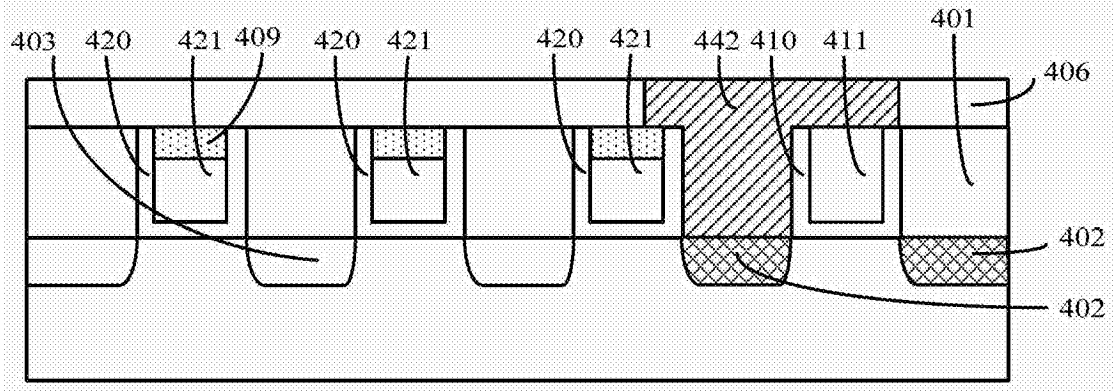


图7

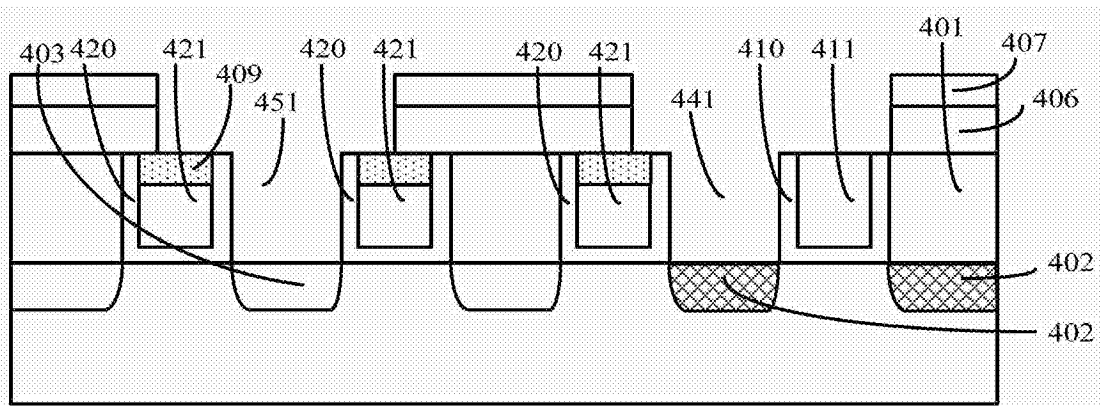


图8

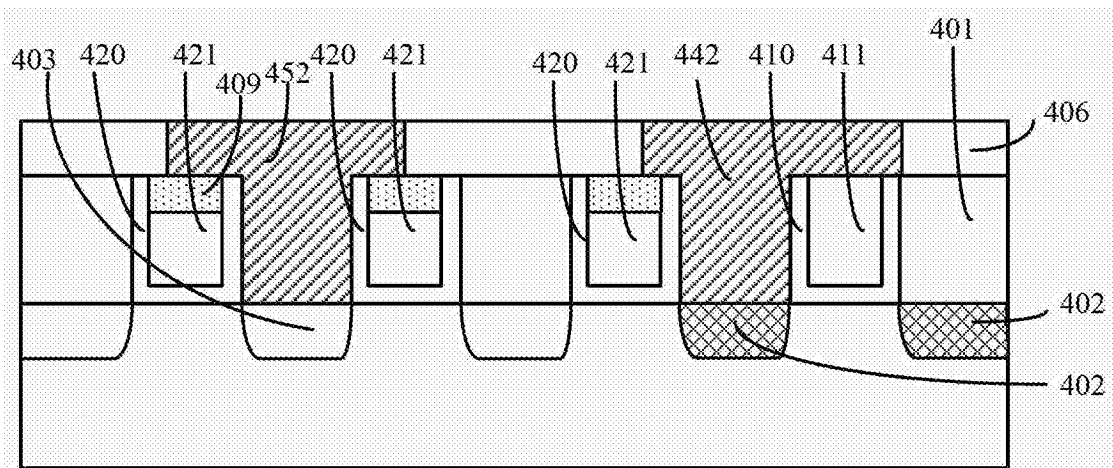


图9



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*H01L 29/78*(2006.01)

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Reviewer He Bei

Claims 5 pages Specification 11 pages

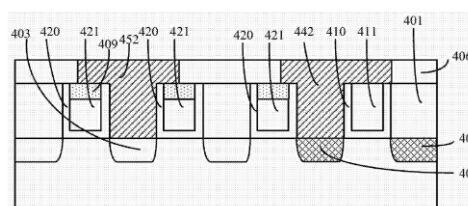
Drawings 3 pages

### (54) Title of Invention

Semiconductor Structure and Method for  
Forming the Same

### (57) Abstract

A semiconductor structure and a method for forming the same, wherein the method for forming the semiconductor structure comprises: a first opening and a second opening are provided in a first dielectric layer on the surface of a semiconductor substrate, first doped regions are provided in the semiconductor substrate on both sides of the first opening, a first metal gate is provided in the first opening, a second metal gate is provided in the second opening, a top surface of the second metal gate is lower than a top surface of the first metal gate, and a third dielectric layer is provided on the surface of the second metal gate, a surface of the third dielectric layer is flush with a top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer; a second dielectric layer is covered on the surface of the first dielectric layer, and the second dielectric layer has an etching selectivity relative to the third dielectric layer; a first contact layer is formed in the second dielectric layer and the first dielectric layer, and the first contact layer is electrically connected to at least one first doped region and at least one first metal gate. The formation process of the said semiconductor structure is simple.



1. A method for forming a semiconductor structure, comprising:

A semiconductor substrate is provided, wherein a first dielectric layer is provided on the surface of the semiconductor substrate, a first opening and a second opening are provided in the first dielectric layer for exposing the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than a top surface of the first metal gate, a third dielectric layer is provided on the surface of the second metal gate, a surface of the third dielectric layer is flush with a top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer;

A second dielectric layer is covered on the surface of the first metal gate, the third dielectric layer and the first dielectric layer, and the second dielectric layer has an etching selectivity relative to the third dielectric layer;

A fourth opening is formed in the second dielectric layer and the first dielectric layer, wherein the fourth opening exposes a surface of at least one first doped region and a first metal gate;

A first contact layer is formed in the fourth opening, and the first contact layer is electrically connected to the first metal gate and at least one first doped region.

2. The method for forming a semiconductor structure as claimed in claim 1 is characterized in that the fourth opening also exposes a portion of the surface of the third dielectric layer; the first contact layer located in the fourth opening and the second metal gate are electrically isolated by the third dielectric layer.

3. The method for forming a semiconductor structure as claimed in claim 1 is characterized in that the number of the first openings is greater than or equal to 1, and the number of the second openings is greater than or equal to 1.

4. The method for forming a semiconductor structure as claimed in claim 1 is characterized in that the method for forming the fourth opening is: forming a mask layer on the surface of the second dielectric layer, the mask layer exposing the surface of the second dielectric layer corresponding to the position of at least one first doped region and at least one first metal gate; using the mask layer as a mask, etching the second dielectric layer and the first dielectric layer by an anisotropic dry etching process until the surface of the first doped region is exposed.

5. The method for forming a semiconductor structure as claimed in claim 1, characterized in that the formation process of the first opening, the second opening and the first doped region is: forming a second dummy gate structure and a plurality of adjacent first dummy gate structures on the surface of a semiconductor substrate, wherein the materials of the first dummy gate structure and the second dummy gate structure are polysilicon; using an ion implantation process to form first doped regions in the semiconductor substrate on both sides of each first dummy gate structure; after forming the first doped region, depositing a first dielectric film on the sidewalls and top surfaces of the semiconductor substrate, the first dummy gate structure and the second dummy gate structure; using a chemical mechanical polishing process to remove the first dielectric film above the surfaces of the first dummy gate structure and the second dummy gate structure to form a first dielectric layer flush with the surfaces of the first dummy gate structure and the second dummy gate structure; after forming the first dielectric layer, removing the first dummy gate structure and forming the first opening, and removing the second dummy gate structure and forming the second opening.

6. The method for forming a semiconductor structure as claimed in claim 5 is characterized in that, before forming the first dielectric film, a barrier layer is deposited on the sidewalls and top surfaces of the semiconductor substrate, the first dummy gate structure and the second dummy gate structure, and the material of the barrier layer is silicon nitride, silicon oxynitride, silicon carbide or silicon carbonitride; the chemical mechanical polishing process stops at the surface of the barrier layer, and over-polishing is performed to expose the surfaces of the first dummy gate structure and the second dummy gate structure.

7. The method for forming a semiconductor structure as claimed in claim 1 is characterized in that it also includes: forming sidewalls on the surface of the semiconductor substrate on both sides of the gate dielectric layer, and the material of the sidewalls is one or more combinations of silicon oxide, silicon nitride and low-K dielectric materials.

8. The method for forming a semiconductor structure as claimed in claim 1 is characterized in that it also includes: forming a first work function layer between the first gate dielectric layer and the first metal gate, and a second work function layer located between the second gate dielectric layer and the second metal gate, wherein the material of the first work function layer and the second work function layer is titanium, tantalum, titanium nitride, tantalum nitride, cobalt, titanium aluminum nitride, titanium aluminum cobalt, ruthenium, copper manganese, titanium aluminum nitride, titanium aluminum or lanthanum.

9. The method for forming a semiconductor structure as claimed in claim 1 is characterized in that the material of the gate dielectric layer is a high-K dielectric material, the material of the first metal gate and the second metal gate is copper, tungsten, aluminum or silver, the material of the first dielectric layer and the second dielectric layer is one of silicon oxide and a low-K dielectric material, the material of the third dielectric layer is silicon nitride, and the material of the first contact layer is titanium or tungsten.

10. A semiconductor structure, characterized in that it comprises: a semiconductor substrate; a first dielectric layer located on the surface of the semiconductor substrate, a first opening and a second opening are provided in the first dielectric layer to expose the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than the top surface of the first metal gate, and a third dielectric layer is provided on the surface of the second metal gate, the surface of the third dielectric layer is flush with the top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer; a second dielectric layer located on the surfaces of the first metal gate, the third dielectric layer and the first dielectric layer, the second dielectric layer has an etching selectivity relative to the third dielectric layer; a fourth opening located in the second dielectric layer and the first dielectric layer, the fourth opening exposing the surface of at least one first doped region and at least one first metal gate; a first contact layer located in the fourth opening, the first contact layer being electrically connected to the first metal gate and at least one first doped region.

11. The semiconductor structure as claimed in claim 10 is characterized in that the fourth opening also exposes a portion of the surface of the third dielectric layer; the first contact layer located in the fourth opening and the second metal gate are electrically isolated by the third dielectric layer.

12. The semiconductor structure as claimed in claim 10 is characterized in that the number of the first openings is greater than or equal to 1, and the number of the second openings is greater than or equal to 1.

13. The semiconductor structure as claimed in claim 10 is characterized in that it also includes: a barrier layer located between the first dielectric layer and the semiconductor substrate and the gate dielectric layer, wherein the barrier layer is made of silicon nitride, silicon oxynitride, silicon carbide or silicon carbonitride.

14. The semiconductor structure as claimed in claim 10 is characterized in that it also includes: sidewalls on the surface of the semiconductor substrate on both sides of the gate dielectric layer, and the material of the sidewalls is one or more combinations of silicon oxide, silicon nitride and low-K dielectric materials.

15. The semiconductor structure as claimed in claim 10 is characterized in that it also includes: a first work function layer between the first gate dielectric layer and the first metal gate, and a second work function layer located between the second gate dielectric layer and the second metal gate, wherein the material of the first work function layer and the second work function layer is titanium, tantalum, titanium nitride, tantalum nitride, cobalt, titanium aluminum nitride, titanium aluminum cobalt, ruthenium, copper manganese, titanium aluminum nitride, titanium aluminum or lanthanum.

16. The semiconductor structure as claimed in claim 10 is characterized in that the material of the gate dielectric layer is a high-K dielectric material, the material of the first metal gate and the second metal gate is copper, tungsten, aluminum or silver, the material of the first dielectric layer and the second dielectric layer is one of silicon oxide and a low-K dielectric material, the material of the third dielectric layer is silicon nitride, and the material of the first contact layer is titanium or tungsten.

17. A method for forming a semiconductor structure, comprising:

A semiconductor substrate is provided, wherein a first dielectric layer is provided on the surface of the semiconductor substrate, a first opening and a plurality of adjacent second opening are provided in the first dielectric layer for exposing the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a second doped region is provided in the

semiconductor substrate between adjacent second openings, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than a top surface of the first metal gate, a third dielectric layer is provided on the surface of the second metal gate, a surface of the third dielectric layer is flush with a top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer;

A second dielectric layer is covered on the surface of the first metal gate, the third dielectric layer and the first dielectric layer, and the material of the second dielectric layer has an etching selectivity relative to the third dielectric layer;

A fourth opening and a fifth opening are formed in the second dielectric layer and the first dielectric layer, wherein the fourth opening at least exposes a surface of the first metal gate, and the fifth opening exposes a surface of at least one second doped region;

A first contact layer is formed in the fourth opening, and a second contact layer is formed in the fifth opening, wherein the first contact layer is electrically connected to at least the first metal gate, and the second contact layer is electrically connected to at least one second doped region.

18. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that the fourth opening also exposes the surface of at least one first doped region; and the first contact layer located in the fourth opening is electrically connected to the first metal gate and at least one first doped region.

19. The method for forming a semiconductor structure as claimed in claim 18 is characterized in that the method for forming the fourth opening and the fifth opening is: forming a mask layer on the surface of the second dielectric layer, the mask layer having a sixth opening and a seventh opening, the sixth opening exposing the surface of the second dielectric layer corresponding to the position of the first metal gate and at least one first doped region, and the seventh opening exposing the surface of the second dielectric layer corresponding to the position of the surface of at least one second doped region; using the mask layer as a mask, etching the second dielectric layer and the first dielectric layer by an anisotropic dry etching process until the surfaces of the first doped region and the second doped region are exposed.

20. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that the bottom of the fourth opening has a first dielectric layer electrically isolated from the first doped region; the first contact layer located in the fourth opening is electrically connected only to the first metal gate, and is electrically isolated from the first doped region by the first dielectric layer.

21. The method for forming a semiconductor structure as claimed in claim 20 is characterized in that the method for forming the fourth opening and the fifth opening is: forming a mask layer on the surface of the second dielectric layer, the mask layer having a sixth opening and a seventh opening, the sixth opening exposing the surface of the second dielectric layer corresponding to the position of the first metal gate, and the seventh opening exposing the surface of the second dielectric layer corresponding to the position of at least one second doped region; using the mask layer as a mask, etching the second dielectric layer at the bottom of the sixth opening and the seventh opening by an anisotropic dry etching process until the first dielectric layer is exposed, and forming a fourth opening exposing the first metal gate at the bottom of the sixth opening; forming a protective layer in the fourth opening, using the protective layer and the mask layer as masks, continuing to etch the first dielectric layer by an anisotropic dry etching process until the surface of the second doped region is exposed, forming the fifth opening, and removing the protective layer.

22. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that the fourth opening also exposes a portion of the surface of the third dielectric layer; the first contact layer located in the fourth opening and the second metal gate are electrically isolated by the third dielectric layer.

23. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that the fifth opening also exposes a portion of the surface of the third dielectric layer; the second contact layer located in the fifth opening and the second metal gate are electrically isolated by the third dielectric layer.

24. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that the number of the first openings is greater than or equal to 1, and the number of the second openings is greater than or equal to 1.

25. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that it also includes: forming sidewalls on the surface of the semiconductor substrate on both sides of the gate dielectric layer, and the material of the sidewalls is one or more combinations of silicon oxide, silicon nitride and low-K dielectric materials.

26. The method for forming a semiconductor structure as claimed in claim 17, characterized in that the formation process of the first opening, the second opening and the first doped region is: forming a second dummy gate structure and a plurality of adjacent first dummy gate structures on the surface of a semiconductor substrate, wherein the materials of the first dummy gate structure and the second dummy gate structure are polysilicon; using an ion implantation process to form first doped regions in the semiconductor substrate on both sides of each first dummy gate structure; forming the second doped region in the semiconductor substrate between adjacent second dummy gate structures; after forming the first doped region and the second doped region, depositing a first dielectric film on the sidewalls and top surfaces of the semiconductor substrate, the first dummy gate structure and the second dummy gate structure; using a chemical mechanical polishing process to remove the first dielectric film above the surfaces of the first dummy gate structure and the second dummy gate structure to form a first dielectric layer flush with the surfaces of the first dummy gate structure and the second dummy gate structure; after forming the first dielectric layer, removing the first dummy gate structure and forming the first opening, and removing the second dummy gate structure and forming the second opening.

27. The method for forming a semiconductor structure as claimed in claim 26 is characterized in that, before forming the first dielectric film, a barrier layer is deposited on the sidewalls and top surfaces of the semiconductor substrate, the first dummy gate structure and the second dummy gate structure, and the material of the barrier layer is silicon nitride, silicon oxynitride, silicon carbide or silicon carbonitride; the chemical mechanical polishing process stops at the surface of the barrier layer, and over-polishing is performed to expose the surfaces of the first dummy gate structure and the second dummy gate structure.

28. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that it also includes: forming a first work function layer between the first gate dielectric layer and the first metal gate, and a second work function layer located between the second gate dielectric layer and the second metal gate, wherein the material of the first work function layer and the second work function layer is titanium, tantalum, titanium nitride, tantalum nitride, cobalt, titanium aluminum nitride, titanium aluminum cobalt, ruthenium, copper manganese, titanium aluminum nitride, titanium aluminum or lanthanum.

29. The method for forming a semiconductor structure as claimed in claim 17 is characterized in that the material of the gate dielectric layer is a high-K dielectric material, the material of the first metal gate and the second metal gate is copper, tungsten, aluminum or silver, the material of the first dielectric layer and the second dielectric layer is one of silicon oxide and a low-K dielectric material, the material of the third dielectric layer is silicon nitride, and the material of the first contact layer is titanium or tungsten.

30. A semiconductor structure, characterized in that it comprises: a semiconductor substrate; a first dielectric layer located on the surface of the semiconductor substrate, a first opening and a plurality of adjacent second openings are provided in the first dielectric layer to expose the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a second doped region is provided in the semiconductor substrate between adjacent second openings, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than the top surface of the first metal gate, and a third dielectric layer is provided on the surface of the second metal gate, the surface of the third dielectric layer is flush with the top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer; a second dielectric layer located on the surfaces of the first metal gate, the third dielectric layer and the first dielectric layer, the materials of the second dielectric layer has an etching selectivity relative to the third dielectric layer; the fourth and fifth openings located in the second dielectric layer and the first dielectric layer, the fourth opening exposing the surface of at least one first metal gate, the fifth opening exposing the surface of at least one second doped region; a first contact layer located in the fourth opening, a second contact layer located in the fifth opening; the first contact layer being electrically connected to at least one first metal gate, the second contact layer being electrically connected to at least one second doped region.

31. The semiconductor structure as claimed in claim 30 is characterized in that the first contact layer is electrically connected to the first metal gate and at least one first doped region.

32. The semiconductor structure as claimed in claim 30 is characterized in that the first contact layer is electrically connected to the first metal gate and is electrically isolated from the first doped region by a first dielectric layer.

33. The semiconductor structure as claimed in claim 30 is characterized in that the number of the first openings is greater than or equal to 1, and the number of the second openings is greater than or equal to 1.

34. The semiconductor structure as claimed in claim 30 is characterized in that the fourth opening also exposes a portion of the surface of the third dielectric layer; the first contact layer located in the fourth opening and the second metal gate are electrically isolated by the third dielectric layer.

35. The semiconductor structure as claimed in claim 30 is characterized in that the fifth opening also exposes a portion of the surface of the third dielectric layer; the second contact layer located in the fifth opening and the second metal gate are electrically isolated by the third dielectric layer.

36. The semiconductor structure as claimed in claim 30 is characterized in that it includes a barrier layer located between the first dielectric layer and the semiconductor substrate, the first gate dielectric layer, and the second gate dielectric layer, wherein the barrier layer is made of silicon nitride, silicon oxynitride, silicon carbide or silicon carbonitride.

37. The semiconductor structure as claimed in claim 30 is characterized in that it also includes: sidewalls on the surface of the semiconductor substrate on both sides of the gate dielectric layer, and the material of the sidewalls is one or more combinations of silicon oxide, silicon nitride and low-K dielectric materials.

38. The semiconductor structure as claimed in claim 30 is characterized in that it also includes: a first work function layer between the first gate dielectric layer and the first metal gate, and a second work function layer located between the second gate dielectric layer and the second metal gate, wherein the material of the first work function layer and the second work function layer is titanium, tantalum, titanium nitride, tantalum nitride, cobalt, titanium aluminum nitride, titanium aluminum cobalt, ruthenium, copper manganese, titanium aluminum nitride, titanium aluminum or lanthanum.

39. The semiconductor structure as claimed in claim 30 is characterized in that the material of the gate dielectric layer is a high-K dielectric material, the material of the first metal gate and the second metal gate is copper, tungsten, aluminum or silver, the material of the first dielectric layer and the second dielectric layer is one of silicon oxide and a low-K dielectric material, the material of the third dielectric layer is silicon nitride, and the material of the first contact layer is titanium or tungsten.

## Semiconductor Structure and Method for Forming the Same

### Technical Field

[0001] The present invention relates to the field of semiconductor manufacturing technology, and more particularly to a semiconductor structure and a method for forming the same.

### Background Technology

[0002] With the rapid development of integrated circuit manufacturing technology, the size of semiconductor devices in integrated circuits, especially MOS (Metal Oxide Semiconductor) devices, has been continuously reduced to meet the requirements of miniaturization and integration of integrated circuit development. As the size of MOS transistor devices continues to shrink, the existing process of using silicon oxide or silicon oxynitride as the gate dielectric layer has been challenged. Transistors formed using silicon oxide or silicon oxynitride as gate dielectric layers have some problems, including increased leakage current and diffusion of impurities, which affect the threshold voltage of the transistor and further affect the performance of the semiconductor device.

[0003] In order to solve the above problems, a transistor containing a high-K dielectric layer and a metal gate structure is proposed. The transistor containing a high-K dielectric layer and a metal gate structure uses a high-K (dielectric constant) material to replace the commonly used silicon oxide or silicon oxynitride gate dielectric material, which can reduce the size of the transistor, reduce the generation of leakage current, and improve the performance of the transistor.

[0004] A transistor with a high-K dielectric layer and a metal gate structure in the prior art is shown in Fig. 1, comprising: a first dielectric layer 105 located on the surface of a semiconductor substrate 100, wherein the first dielectric layer 105 has an opening (not shown) exposing the surface of the semiconductor substrate 100; a high-K gate dielectric layer 101 located on the sidewalls and bottom surface of the opening; a metal gate layer 103 located on the surface of the high-K gate dielectric layer 101, and sidewalls 104 located on the surface of the semiconductor substrate 100 on both sides of the high-K gate dielectric layer 101 and the metal gate layer 103; and a source region 106a and a drain region 106b in the semiconductor substrate 100 located on both sides of the high-K gate dielectric layer 101, the metal gate layer 103 and the sidewalls 104.

[0005] After forming the transistor as shown in Fig. 1, the back end of line (BEOL) process of the semiconductor device is performed to enable a source, a drain or a gate of the transistor to be electrically connected to other semiconductor devices in an integrated circuit.

[0006] However, the BEOL process of the existing transistor with a high-K dielectric layer and a metal gate structure is relatively complicated, which will increase the process time and cost.

[0007] For more information on the BEOL process of transistors, please refer to U.S. patent document with publication number US2007/0210339.

### Summary of the Invention

[0008] The problem solved by the present invention is to provide a semiconductor structure and a method for forming the same, so as to improve the BEOL process of a transistor having a high-K dielectric layer and a metal gate structure, thereby improving the process efficiency and reducing the process cost.

[0009] To address the aforementioned problem, the present invention provides a method for forming a semiconductor structure, comprising: a semiconductor substrate; a first dielectric layer located on the surface of the semiconductor substrate, a first opening and a second opening are provided in the first dielectric layer to expose the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than the top surface of the first metal gate, and a third dielectric layer is provided on the surface of the second metal gate, the surface of the third dielectric layer is flush with the top surface of the first metal gate, and the third dielectric layer has an etching selectivity

relative to the first dielectric layer; the surfaces of the first metal gate, the third dielectric layer and the first dielectric layer covered by the second dielectric layer, the second dielectric layer has an etching selectivity relative to the third dielectric layer; a fourth opening formed in the second dielectric layer and the first dielectric layer, the fourth opening exposing the surface of at least one first doped region and the first metal gate; a first contact layer located in the fourth opening, the first contact layer being electrically connected to the first metal gate and at least one first doped region.

[0010] Accordingly, the present invention also provides a semiconductor structure, comprising: a semiconductor substrate; a first dielectric layer located on the surface of the semiconductor substrate, a first opening and a second opening are provided in the first dielectric layer to expose the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than the top surface of the first metal gate, and a third dielectric layer is provided on the surface of the second metal gate, the surface of the third dielectric layer is flush with the top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer; a second dielectric layer located on the surfaces of the first metal gate, the third dielectric layer and the first dielectric layer, the second dielectric layer has an etching selectivity relative to the third dielectric layer; a fourth opening located in the second dielectric layer and the first dielectric layer, the fourth opening exposing the surface of at least one first doped region and at least one first metal gate; a first contact layer located in the fourth opening, the first contact layer being electrically connected to the first metal gate and at least one first doped region.

[0011] The present invention also provides a method for forming a semiconductor structure, comprising: a semiconductor substrate; a first dielectric layer located on the surface of the semiconductor substrate, a first opening and a second opening are provided in the first dielectric layer to expose the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than the top surface of the first metal gate, and a third dielectric layer is provided on the surface of the second metal gate, the surface of the third dielectric layer is flush with the top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer; the surfaces of the first metal gate, the third dielectric layer and the first dielectric layer covered by the second dielectric layer, the second dielectric layer has an etching selectivity relative to the third dielectric layer; a fourth opening formed in the second dielectric layer and the first dielectric layer, the fourth opening exposing the surface of at least one first doped region and the first metal gate; a first contact layer located in the fourth opening, the first contact layer being electrically connected to the first metal gate and at least one first doped region.

[0012] Accordingly, the present invention also provides a semiconductor structure, comprising: a semiconductor substrate; a first dielectric layer located on the surface of the semiconductor substrate, a first opening and a second opening are provided in the first dielectric layer to expose the semiconductor substrate, a first doped region is provided in the semiconductor substrate on both sides of the first opening, a gate dielectric layer is provided on the bottom and sidewall surfaces of the first opening and the second opening, a first metal gate is provided on the surface of the gate dielectric layer of the first opening, a second metal gate is provided on the surface of the gate dielectric layer of the second opening, a top surface of the second metal gate is lower than the top surface of the first metal gate, and a third dielectric layer is provided on the surface of the second metal gate, the surface of the third dielectric layer is flush with the top surface of the first metal gate, and the third dielectric layer has an etching selectivity relative to the first dielectric layer; a second dielectric layer located on the surfaces of the first metal gate, the third dielectric layer and the first dielectric layer, the second dielectric layer has an etching selectivity relative to the third dielectric layer; a fourth opening located in the second dielectric layer and the first dielectric layer, the fourth opening exposing the surface of at least one first doped region and at least one first metal

gate; a first contact layer located in the fourth opening, the first contact layer being electrically connected to the first metal gate and at least one first doped region.

[0013] Compared with the prior art, the technical solution of the present invention has the following advantages:

[0014] Make the top surface of the second metal gate lower than the top surface of the first metal gate, and form a third dielectric layer on the surface of the second metal gate, so that the surface of the third dielectric layer is flush with the top surface of the first metal gate, and the third dielectric layer has etching selectivity relative to the first dielectric layer; when the second dielectric layer is subsequently formed, a fourth opening is formed in the second dielectric layer and the first dielectric layer to expose at least one first doped region and the first metal gate, the third dielectric layer can protect the surface of the second metal gate; and the first contact layer subsequently formed in the fourth opening is electrically isolated from the second metal gate while being electrically connected to at least one first doped region and at least one first metal gate; the first contact layer can serve as a shared contact structure (Share Contact) connecting the first doped region and the first metal gate; secondly, the fourth opening can be formed by only one etching process, and the first contact layer can be formed by only one metal filling process, which can simplify the process.

[0015] In a semiconductor structure, a top surface of a second metal gate is lower than a top surface of a first metal gate, and a third dielectric layer is provided on the surface of the second metal gate; the surfaces of the first metal gate, the third dielectric layer and the first dielectric layer have a second dielectric layer, and fourth openings in the second dielectric layer and the first dielectric layer expose surfaces of at least one first doped region and the first metal gate; therefore, a first contact layer is provided in the fourth opening and is electrically connected to at least one first doped region and the first metal gate as a shared contact structure, and the structure of the first contact layer is simple, which is beneficial to the integration of semiconductor devices.

[0016] In another method for forming a semiconductor structure, a fifth opening exposing the surface of at least one second doped region is formed while a fourth opening exposing at least one first metal gate is formed in the second dielectric layer and the first dielectric layer; thereby, a second contact layer can be formed in the fifth opening while a first contact layer can be formed in the fourth opening; the first contact layer can be electrically connected to at least one first metal gate and electrically isolated from the second metal gate by a third dielectric layer; the second dielectric layer can be electrically connected to the second doped region and electrically isolated from the second metal gate by the third dielectric layer, and can be used as a self-aligned contact structure (SAC); the first contact layer and the second contact layer are formed simultaneously, which further simplifies the process.

[0017] In the semiconductor structure, the second dielectric layer and the first dielectric layer located on the surface of the first metal gate, the third dielectric layer and the first dielectric layer have a first contact layer and a second contact layer at the same time; the first contact layer can be electrically connected to at least one first metal gate, and is electrically isolated from the second metal gate by the third dielectric layer; and the second contact layer can be electrically connected to the second doped region, and is electrically isolated from the second metal gate by the third dielectric layer, and can be used as a self-aligned contact structure; the structures of the first contact layer and the second contact layer are simple, which is conducive to the integration of semiconductor devices.

### Description of the Drawings

[0018] Fig. 1 is a schematic cross-sectional structure diagram of a transistor having a high-K dielectric layer and a metal gate structure in the prior art;

[0019] Fig. 2 is a schematic diagram of a shared contact structure formed in a BEOL process of a transistor having a high-K dielectric layer and a metal gate structure;

[0020] Fig. 3 to Fig. 7 are schematic cross-sectional views of a process for forming a semiconductor structure according to the first embodiment of the present invention;

[0021] Fig. 8 and Fig. 9 are schematic cross-sectional views of a process for forming a semiconductor structure according to the second embodiment of the present invention;

### Specific Embodiments

[0022] As described in the background technology, the BEOL process of the existing transistor with a high-K dielectric layer and a metal gate structure is relatively complicated, which will increase the process time and cost.

[0023] The inventors of the present invention have found through research, please refer to Fig. 2, that in the BEOL process of the existing transistor with a high-K dielectric layer and a metal gate structure, the electrical interconnection structure formed includes a shared contact structure (Share Contact), and the shared contact structure is composed of a first conductive plug 124 located on the surface of the source region 106a, a second conductive plug 125 located on the surface of the metal gate layer 103, and a conductive layer 126 located on the surfaces of the first conductive plug 124 and the second conductive plug 125.

[0024] Wherein, the first conductive plug 124 and the second conductive plug 125 need to be filled with metal in the first opening and the second opening through a deposition process, and the metal above the surface of the second dielectric layer 120 is removed by a chemical mechanical polishing process, and the conductive layer 126 also needs to be formed by a deposition process and an etching process after the deposition process. The process of the shared contact structure is relatively complicated, which is not conducive to improving efficiency and reducing costs; secondly, since the depth-to-width ratio of the first opening and the second opening is relatively large, defects are easily generated in the filled metal, resulting in poor device performance; and, since the area of the top surface of the first conductive plug 124 and the second conductive plug 125 is too small relative to the area of the second dielectric layer 120, the subsequent chemical mechanical polishing process is likely to cause poor morphology on the surface of the second dielectric layer 120, thereby reducing the stability of the device.

[0025] After further research by the inventors of the present invention, a method for forming a semiconductor structure is proposed, which can simplify the process of forming a shared contact structure and make the formed shared contact structure simple, which is conducive to the integration of semiconductor devices.

[0026] In order to make the above-mentioned objectives, features and advantages of the present invention more obvious and easy to understand, the specific embodiments of the present invention are described in detail below in conjunction with the accompanying drawings.

[0027] First embodiment

[0028] Fig. 3 to Fig. 7 are schematic cross-sectional views of a process for forming a semiconductor structure according to a first embodiment of the present invention.

[0029] Referring to Fig. 3, a semiconductor substrate 400 is provided, wherein the surface of the semiconductor substrate 400 has a first dielectric layer 401, the first dielectric layer 401 has a second opening (not shown) and a first opening (not shown), the first opening and the second opening expose the semiconductor substrate 400, the semiconductor substrate 400 on both sides of each first opening has a first doped region 402, the bottom and sidewall surfaces of the first opening have a first gate dielectric layer 410, the surface of the first gate dielectric layer 410 has a first metal gate 411, the bottom and sidewall surfaces of the second opening have a second gate dielectric layer 420, the surface of the second gate dielectric layer 420 has a second metal gate 421, and the surfaces of the first metal gate 411 and the second metal gate 421 are both flush with the surface of the first dielectric layer 401.

[0030] The semiconductor substrate 400 is used to provide a working platform for subsequent processes; the semiconductor substrate 400 is a silicon substrate, a silicon substrate, a silicon carbide substrate, a silicon-on-insulator (SOI) substrate, a germanium-on-insulator (GOI) substrate, a glass substrate or a III-V compound substrate (such as silicon nitride or gallium arsenide, etc.).

[0031] The material of the first gate dielectric layer 410 and the second gate dielectric layer 420 is a high-K dielectric material, and the high-K dielectric material includes: hafnium oxide, zirconium oxide, hafnium silicon oxide, lanthanum oxide, zirconium silicon oxide, titanium oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide or aluminum oxide; the material of the first metal gate 411 and the second metal gate 421 is a metal, and the metal includes: copper, tungsten, aluminum or silver.

[0032] The number of the first openings is equal to 1 or greater than 1; when the number of the first openings is greater than 1, and several first openings are adjacent to each other, the first doped region 402 is located in the semiconductor substrate 400 between adjacent first openings; the first doped region 402 serves as a source region and a drain region in the formed transistor; in addition, the first opening can be adjacent to the second opening, and the first doped region 402 is located in the semiconductor substrate 400 between adjacent first openings and the second opening; in addition, the number of the second openings can also be equal to 1 or greater than 1, and there is a second doped region 403 between adjacent second openings, and the second opening located at the edge is adjacent to the first opening located at the edge; in this embodiment, the number of the first opening is 1, the number of the second

openings is 3, and the 3 second openings are adjacent to each other.

[0033] In one embodiment, a first work function layer (not shown) is provided between the first gate dielectric layer 410 and the first metal gate 411, and a second work function layer (not shown) is provided between the second gate dielectric layer 420 and the second metal gate 421; the materials of the first work function layer and the second work function layer are titanium, tantalum, titanium nitride, tantalum nitride, cobalt, titanium aluminum nitride, titanium aluminum cobalt, ruthenium, copper manganese, titanium aluminum nitride, titanium aluminum or lanthanum; the first work function layer and the second work function layer are used to adjust the threshold voltage of the formed transistor, when the formed transistor is a PMOS transistor, the material of the first work function layer or the second work function layer needs to have a higher work function, when the formed transistor is an NMOS transistor, the material of the first work function layer or the second work function layer needs to have a lower work function to reduce the threshold voltage of the formed transistor.

[0034] In another embodiment, a protective layer (not shown) is further formed on the surfaces of the first gate dielectric layer 410 and the second gate dielectric layer 420. The material of the protective layer is titanium nitride or tantalum nitride, and is used to isolate the first gate dielectric layer 410 from the first metal gate 411, and the second gate dielectric layer 420 from the second metal gate 421; the protective layer is used to prevent impurities from passing through the gate dielectric layer into the work function layer or the metal gate to cause contamination during the formation of the transistor, or to prevent leakage current from being generated between the gate dielectric layer and the metal gate when the transistor is working, thereby improving the isolation effect.

[0035] The formation process of the first openings, second openings, first doped regions 402, and second doped regions 403 is as follows: forming a plurality of adjacent first dummy gate structures (not shown) and second dummy gate structures (not shown) on the surface of the semiconductor substrate 400, wherein the materials of the first dummy gate structures and second dummy gate structures are polysilicon; using an ion implantation process to form first doped regions 402 in the semiconductor substrate 400 on both sides of each first dummy gate structure, and forming second doped regions 403 in the semiconductor substrate 400 between adjacent second dummy gate structures; after forming the first doped regions 402 and second doped regions 403, depositing a first dielectric film on the sidewalls and top surfaces of the semiconductor substrate 400, the first dummy gate structures, and the second dummy gate structures; using a chemical mechanical polishing process to remove the first dielectric film above the surfaces of the first dummy gate structures and second dummy gate structures, thereby forming a first dielectric layer 401 flush with the surfaces of the first dummy gate structures and second dummy gate structures; after forming the first dielectric layer 401, removing the first dummy gate structures to form the first openings, and removing the second dummy gate structures to form the second openings.

[0036] After forming the first opening and the second opening, a gate dielectric film is deposited on the sidewall and bottom surface of the first opening; a gate electrode film is deposited on the surface of the gate dielectric film to fill the first opening; a chemical mechanical polishing process is used to remove the gate dielectric film and the gate electrode film above the surface of the first dielectric layer 401, so as to form a first gate dielectric layer 410 and a first metal gate 411 in the first opening, and a second gate dielectric layer 420 and a second metal gate 421 in the second opening.

[0037] In one embodiment, before forming the first dielectric film, the method further includes: depositing a barrier layer on the sidewalls and top surfaces of the semiconductor substrate 400, the first dummy gate structure and the second dummy gate structure, wherein the material of the barrier layer is silicon nitride, silicon oxynitride, silicon carbide or silicon carbonitride, and is different from the material of the first dielectric layer; the barrier layer is used to define the stop position of the polishing process when the first dielectric film above the surface of the dummy gate structure is removed by a chemical mechanical polishing process, and after the chemical mechanical polishing process stops at the barrier layer, over-polishing is performed to expose the surfaces of the first dummy gate structure and the second dummy gate structure.

[0038] In another embodiment, after forming the first dummy gate structure and the second dummy gate structure and before forming the first doped region 402, sidewalls are formed on the surface of the semiconductor substrate 400 on both sides of the first dummy gate structure and the second dummy gate structure, respectively, and the material of the sidewalls is one or more combinations of silicon oxide, silicon nitride and low-K dielectric materials.

[0039] It should be noted that, since the materials of the first gate dielectric layer 410 and the second gate dielectric layer 420 are high-K dielectric materials, the interfaces between the first gate dielectric layer 410 and the second gate dielectric layer 420 and the semiconductor substrate 400 do not match.

Therefore, before depositing the gate dielectric film in the first opening and the second opening, it is necessary to use a thermal oxidation process to form a silicon oxide layer (not shown) on the surface of the semiconductor substrate 400 at the bottom of the first opening and the second opening to bond the first gate dielectric layer 410 and the second gate dielectric layer 420 to the semiconductor substrate 400, thereby reducing leakage current and stabilizing device performance.

[0040] Referring to Fig. 4, a portion of the second metal gate 421 is etched to form a third opening (not shown), so that the top surface of the second metal gate 421 is lower than the top surface of the first metal gate 411; a third dielectric layer 409 is formed in the third opening, the surface of the third dielectric layer 409 is flush with the top surface of the first metal gate 411, and the third dielectric layer 409 has an etching selectivity relative to the first dielectric layer 401.

[0041] In order to meet different industrial needs and form transistors with different heights, it is necessary to etch the top surface of the second metal gate 421 to make it lower than the first metal gate 411; and after the top surface of the second metal gate 421 is lower than the first metal gate 411, a third dielectric layer 409 is formed on the surface of the second metal gate 421, so as to electrically isolate the second metal gate 421 from the first contact layer formed subsequently.

[0042] The process for forming the third opening is an etching process, preferably an anisotropic dry etching process; in the embodiment of the present invention, in order to prevent the first metal gate 411 from being etched during the etching process, it also includes: before performing the etching process, forming a protective layer on the surface of the first metal gate 411; after the etching process, removing the protective layer.

[0043] It should be noted that, in other embodiments of the present invention, when a second work function layer is provided between the second metal gate 421 and the second gate dielectric layer 420, the work function layer also needs to be etched, which will not be described in detail herein.

[0044] Since the first contact layer formed subsequently only needs to electrically connect the first metal 411 and the first doped region 402, when the first contact layer is electrically connected to the first doped region 402 and the first metal gate 411, the third dielectric layer 409 can electrically isolate the first contact layer from the second metal gate 421; in addition, the third dielectric layer 409 is simultaneously formed on the surfaces of the second work function layer and the second metal gate 421, thereby playing a role of electrical isolation.

[0045] The material of the third dielectric layer 409 is silicon nitride, and the formation process is as follows: after etching the second metal gate 421, a third dielectric film is deposited in the third opening and on the surfaces of the first dielectric layer 401 and the first metal gate 411; a chemical mechanical polishing process is used to remove the third dielectric film above the surface of the first dielectric layer 401, and the third dielectric layer 409 is formed on the surface of the second metal gate 421.

[0046] Referring to Fig. 5, a second dielectric layer 406 is covered on the surfaces of the first metal gate 411, the third dielectric layer 409 and the first dielectric layer 401, and the second dielectric layer 406 has an etching selectivity relative to the third dielectric layer 409; a mask layer 407 is formed on the surface of the second dielectric layer 406, and the mask layer 407 exposes the surface of the second dielectric layer 406 corresponding to the position of at least one first doped region 402 and the first metal gate 411.

[0047] The material of the second dielectric layer 406 is one of silicon oxide and low-K dielectric materials, and the formation process of the second dielectric layer 406 is a deposition process, preferably a chemical vapor deposition process; since the second dielectric layer 406 is formed on the surface of the first metal gate 411, the first contact layer subsequently formed in the second dielectric layer 406 is used to electrically connect to the first metal gate 411.

[0048] The mask layer 407 has a sixth opening 440 exposing the surface of the second dielectric layer at a position corresponding to at least one first doped region 402 and the first metal gate 411. The sixth opening 440 defines a position of a first contact layer to be formed subsequently. The material of the mask layer 407 is photoresist, and its formation process is: forming a photoresist film on the surface of the second dielectric layer 406 by a spin coating process; exposing and developing the photoresist film for patterning, removing the photoresist film corresponding to the position of the first metal gate 411 and the first doped region 402, and forming the mask layer 407.

[0049] In the present embodiment, the mask layer 407 only exposes a first metal gate 411 and a corresponding position of a first doped region 402, so that a second opening subsequently formed

using the mask layer 407 as a mask can expose a first metal gate 411 and a corresponding position of a first doped region 402, and the first contact layer formed in the second opening can electrically connect the first metal gate 411 and the first doped region 402, thereby forming a shared contact structure.

[0050] It should be noted that, the mask layer 407 of the present embodiment can also expose a portion of the surface of the second dielectric layer 406 corresponding to the position of the second metal gate 421, and the area exposed by the mask layer 407 becomes larger, thereby reducing the precision requirement for the photolithography process; since the surface of the second metal gate 421 has the third dielectric layer 409, and the third dielectric layer 409 has etching selectivity relative to the second dielectric layer 406, and the second metal gate 421 also has sidewalls on both sides; when the second opening is subsequently etched to form the second opening, the third dielectric layer 409 and the sidewalls can protect the second metal gate 421 and the second gate dielectric layer 420 from being damaged; thereby avoiding the problem of additionally exposing the second metal gate 421 due to process errors when the photolithography process exposes the first metal gate 411, thereby ensuring the stability of the performance of the formed device.

[0051] In another embodiment, the mask layer simultaneously exposes the first metal gate 411 and the corresponding positions of the first doped regions 402 on both sides thereof; when the first dielectric layer 401 and the second dielectric layer 406 are etched using the mask layer as a mask, the formed second opening can expose the first metal gate 411 and the surfaces of the first doped regions 402 on both sides thereof; so that the first contact layer subsequently formed in the second opening can be electrically connected to the first metal gate 411 and the first doped regions 402 on both sides thereof at the same time.

[0052] In other embodiments, when the number of the first openings is greater than 1, the mask layer can expose any first doped region and the corresponding positions of the first metal gate located on both sides of the first doped region, so that the subsequently formed first contact layer can be electrically connected to any first doped region and the first metal gates on both sides of the first doped region at the same time.

[0053] The size and position of the area exposed by the mask layer 409 can be adjusted according to the specific process requirements of the first contact layer to be formed, and should not be overly limited here.

[0054] Referring to Fig. 6, the mask layer 407 is a mask, and the second dielectric layer 406 and the first dielectric layer 401 are etched until at least one first doped region 402 and a surface of the first metal gate 411 are exposed, thereby forming a fourth opening 441.

[0055] The process of etching the second dielectric layer 406 and the first dielectric layer 401 is preferably an anisotropic dry etching process; since the material of the second dielectric layer 406 is different from that of the first metal gate 411, the process of etching the second dielectric layer 406 will not damage the surface of the first metal gate 411, and the first dielectric layer 401 between the first metal gate 411 and the second metal gate 421 continues to be etched; when etching the first dielectric layer 401, due to the protection of the sidewall, the sidewall surfaces of the first metal gate 411 and the second metal gate 421 are protected from damage; therefore, only one photolithography and etching process is required to form the fourth opening 441 simultaneously exposing the first doped region 402 and the first metal gate 411; and subsequently, only one deposition and polishing process is required to form a first contact layer that is electrically connected to the first doped region 402 and the first metal gate 411 at the same time. The formed first contact layer can be used as a shared contact structure, and the formation process of the first contact layer is simple, which can reduce the process cost and improve the process efficiency; moreover, the top size of the fourth opening 441 is relatively large, so that the top surface size of the first contact layer formed in the fourth opening 441 is relatively large. When the polishing process is subsequently used to remove the metal material higher than the surface of the second dielectric layer 406, the damage to the second dielectric layer 406 is relatively small, and the performance of the formed device is more stable.

[0056] The surface of the second metal gate 421 is protected by the third dielectric layer 409, so the formed fourth opening 441 will not expose the second metal gate 421, and the first contact layer subsequently formed in the fourth opening 441 is electrically isolated from the second metal gate 421 by the third dielectric layer 409; it should be noted that, in the etching process, since a part of the thickness of the third dielectric layer 409 will be removed, the thickness of the third dielectric layer 409 needs to be determined according to the etching process to ensure the isolation effect of the third dielectric layer 409.

[0057] In one embodiment, when a barrier layer is provided between the first dielectric layer 401 and the semiconductor substrate 400, the first gate dielectric 410 and the second gate dielectric

420, when the first dielectric layer 401 is etched, the barrier layer in contact with the first gate dielectric 410 and the second gate dielectric 420 is retained, which can further protect the side walls of the first metal gate 411 and the second metal gate 421 from being damaged during the etching process; and the barrier layer located at the bottom of the fourth opening 441 is removed after the first dielectric layer 401 is removed.

[0058] In another embodiment, when the mask layer simultaneously exposes the first metal gate 411 and the corresponding positions of the first doped regions 402 on both sides thereof, the etching-formed fourth opening can expose the first metal gate 411 and the surfaces of the first doped regions 402 on both sides, enabling the subsequently formed first contact layer to simultaneously electrically connect the first metal gate 411 and the first doped regions 402 on both sides thereof.

[0059] In other embodiments, when the number of the first openings is greater than 1 and the mask layer is capable of exposing any first doped region 402 and the corresponding positions of the first metal gate 411 located on both sides of the first doped region 402, the fourth opening formed by etching can simultaneously expose the first doped region 402 and the first metal gate 411 on both sides thereof, so that the first contact layer formed subsequently can be electrically connected to the first doped region 402 and the first metal gate 411 located on both sides of the first doped region 402 at the same time.

[0060] Referring to Fig. 7, the fourth opening 441 (as shown in Fig. 6) is filled with metal to form a first contact layer 442. The surface of the first contact layer 442 is flush with the top surface of the second dielectric layer 406, and the first contact layer 442 is electrically connected to at least one first metal gate 411 and at least one first doped region 402.

[0061] It should be noted that, before the fourth opening 441 is filled with metal, the mask layer 407 is removed (as shown in Fig. 6).

[0062] The first contact layer 442 is formed by: filling titanium or tungsten metal by a deposition process or an electroplating process; after the fourth opening 441 is filled with metal, removing the metal above the surface of the second dielectric layer 406 by a chemical mechanical polishing process.

[0063] Since the top size of the fourth opening 441 is relatively large, it is conducive to the filling of titanium or tungsten metal, so that the quality of the formed first contact layer 442 is good and the performance of the formed device is stable. Furthermore, when the chemical mechanical polishing process removes the metal above the surface of the second dielectric layer 406, the surface damage of the second dielectric layer 406 is reduced, which is beneficial to improving the stability of the formed device.

[0064] In one embodiment, before filling the conductive material, a stop layer (not shown) is formed on the surface of the second dielectric layer 406 and the sidewalls and bottom surfaces of the fourth opening 441, and the first contact layer 442 is formed on the surface of the stop layer. The material of the stop layer is titanium nitride or tantalum nitride; the stop layer defines the stop position of chemical mechanical polishing. After polishing to the stop layer, a certain amount of over-polishing is performed to expose the surface of the second dielectric layer 406.

[0065] In the present embodiment, the first contact layer 442 can be electrically connected to the first metal gate 411 and at least one first doped region 402 to form a shared contact structure; in another embodiment, the fourth opening can simultaneously expose the first metal gate 411 and the surfaces of the first doped regions 402 on both sides thereof, so that the first contact layer 442 can be electrically connected to the first metal gate 411 and the first doped regions 402 on both sides thereof at the same time.

[0066] In other embodiments, when the number of the first openings is greater than 1, the fourth opening can simultaneously expose the first doped region 402 and the first metal gates 411 on both sides thereof, enabling the formed first contact layer to electrically connect both the first doped region 402 and the first metal gates 411 on both sides of the first doped region 402 at the same time.

[0067] In this embodiment, etch the top of the second metal gate so that it is lower than the top surface of the first metal gate, and form a third dielectric layer on the surface of the second metal gate, so that the third dielectric layer has etching selectivity relative to both the first dielectric layer and the subsequently formed second dielectric layer; therefore, when a fourth opening is formed in the second dielectric layer and the first dielectric layer to expose at least one first doped region and the first metal gate, the third dielectric layer can protect the surface of the second metal gate, and

ensure electrical isolation between the subsequently formed first contact layer within the fourth opening and the second metal gate; the first contact layer is capable of electrically connecting at least one first doped region and at least one first metal gate while remaining electrically isolated from the second metal gate, thereby serving as a shared contact structure that links the first doped region and the first metal gate; secondly, the fourth opening can be formed by only one etching process, and the first contact layer can be formed by only one metal filling process, which can simplify the process.

[0068] Accordingly, this embodiment further provides a semiconductor structure, please continue to refer to Fig. 6, comprising: a semiconductor substrate 400, wherein the surface of the semiconductor substrate 400 has a first dielectric layer 401, the first dielectric layer 401 has a plurality of adjacent first openings and a plurality of adjacent second openings, the first openings and the second openings expose the semiconductor substrate 400, and the semiconductor substrate 400 has a first doped region 402 on both sides of each first opening; a first gate dielectric layer 410 located at the bottom and sidewall surfaces of the first opening, a first metal gate 411 located at the surface of the first gate dielectric layer 410, the surface of the first metal gate 411 is flush with the surface of the first dielectric layer 401; a second gate dielectric layer 420 located at the bottom and sidewall surfaces of the second opening, a second metal gate 421 located at the surface of the second gate dielectric layer 420, the top surface of the second metal gate 421 is lower than the top surface of the first metal gate 411; a third dielectric layer 409 located on the surface of the second metal gate 421, the surface of the third dielectric layer 409 being flush with the top surface of the first metal gate 411, and the third dielectric layer 409 having an etching selectivity relative to the first dielectric layer 401; a second dielectric layer 406 covering the first metal gate 411, the third dielectric layer 409 and the surface of the first dielectric layer 401, the second dielectric layer 406 having an etching selectivity relative to the third dielectric layer 409; a fourth opening located in the second dielectric layer 406 and the first dielectric layer 401, the fourth opening exposing the surface of at least one first doped region 402 and at least one first metal gate 411; a first contact layer 442 located in the fourth opening, the surface of the first contact layer 442 being flush with the top surface of the second dielectric layer 406, and the first contact layer 442 being electrically connected to at least one first doped region 402 and at least one first metal gate 411.

[0069] In the semiconductor structure of this embodiment, the first contact layer is electrically connected to at least one first doped region and at least one first metal gate, and is electrically isolated from the second metal gate by the third dielectric layer, serving as a shared contact structure. The structure of the first contact layer is simple, which is conducive to the integration of semiconductor devices.

[0070] Second embodiment

[0071] Different from the first embodiment of the present invention, in the second embodiment of the present invention, a first contact layer and a second contact layer can be formed simultaneously, the first contact layer serves as a shared contact structure, and the second contact layer serves as a self-aligned contact structure.

[0072] On the basis of forming the structure shown in Fig. 4 of the first embodiment, please refer to Fig. 8, a second dielectric layer 406 is formed on the surfaces of the third dielectric layer 409, the first metal gate 411 and the first dielectric layer 401, and the second dielectric layer 406 has an etching selectivity relative to the third dielectric layer 409; a mask layer 407 is formed on the surface of the second dielectric layer 406, and the mask layer 407 has a sixth opening (not shown) and a seventh opening (not shown), the sixth opening exposes the surface of the second dielectric layer 406 corresponding to the position of at least one first metal gate 411, and the seventh opening exposes the surface of the second dielectric layer 406 corresponding to the position of at least one second doped region 403; using the mask layer 407 as a mask, the second dielectric layer 406 and the first dielectric layer 401 are etched, and a fourth opening 441 and a fifth opening 451 are formed in the second dielectric layer 406 and the first dielectric layer 401, the fourth opening 441 exposes the surface of at least one first metal gate 411, and the fifth opening 451 exposes the surface of at least one second doped region 403.

[0073] The materials and formation process of the second dielectric layer 406 and the mask layer 407 are the same as those of the second dielectric layer and the mask layer described in the first embodiment, and are not described in detail herein.

[0074] While the mask layer 407 exposes the position corresponding to at least one first metal gate 411, the seventh opening also exposes the surface of the second dielectric layer 406

corresponding to the position of at least one second doped region 403; the second dielectric layer 406 and the first dielectric layer 401 are etched simultaneously to form a fourth opening 441 exposing at least one first metal gate 411 and a fifth opening 451 exposing at least one second doped region 403; furthermore, subsequently, a first contact layer can be formed in the fourth opening 441 and a second contact layer can be formed in the fifth opening 451 at the same time, thereby further simplifying the formation process of the semiconductor device; wherein, the second contact layer is a self-aligned contact structure, and the first contact layer is a shared contact structure.

[0075] The seventh opening in the mask layer 407 defines the position and pattern of the second contact layer to be formed subsequently, so that the second contact layer can be electrically connected to at least one second doped region 403; since the third dielectric layer 409 is formed on the surface of the second metal gate 421, and the third dielectric layer 409 has an etching selectivity relative to the second dielectric layer 406 and the first dielectric layer 401, the process of etching the second dielectric layer 406 stops at the surface of the third dielectric layer 409, while the first dielectric layer 401 located between adjacent second metal gates 421 continues to be etched, and the second doped region 403 is exposed; the second contact layer formed subsequently on the surface of the second doped region 403 can be electrically isolated from the second metal gate 421 through the third dielectric layer 409; therefore, the seventh opening can expose the corresponding position of the second doped region 403 while exposing the corresponding position of part of the third dielectric layer 409, so that the size of the seventh opening is larger, and the precision requirement for the photolithography process when forming the seventh opening is reduced.

[0076] In one embodiment, the fourth opening 441 can simultaneously expose the surface of at least one first metal gate 411 and the surface of at least one first doped region 402; then the first contact layer subsequently formed in the fourth opening 441 is electrically connected to at least one first doped region 402 and at least one first metal gate 411, so that the first contact layer serves as a shared contact structure; in this embodiment, the fourth opening 441 exposes the surfaces of the first metal gate 411 and the first doped region 402, and the formation method of the fourth opening 441 and the fifth opening 451 is: using the mask layer 407 as a mask, anisotropic dry etching process is adopted to etch the second dielectric layer and the first dielectric layer until the surfaces of the first doped region 402 and the second doped region 403 are exposed.

[0077] The embodiment of the fourth opening 441 in this embodiment is the same as the fourth opening in the first embodiment, and will not be described in detail herein.

[0078] In another embodiment, the fourth opening can only expose the surface of at least one first metal gate, and the bottom of the fourth opening has a first dielectric layer 401 electrically isolated from the first doped region 402; the first contact layer formed in the fourth opening is electrically connected to at least one first metal gate 411, and is electrically isolated from the first doped region 402 through the first dielectric layer 401, so that the first contact layer is only used to electrically connect the first metal gate 411 with other devices; the fourth opening and the fifth opening are formed by: using the mask layer 407 as a mask, etching the second dielectric layer 406 at the bottom of the sixth opening and the seventh opening by an anisotropic dry etching process until the first dielectric layer 401 is exposed, and forming a fourth opening exposing the first metal gate 411 at the bottom of the sixth opening; forming a protective layer in the fourth opening, using the protective layer and the mask layer as masks, continuing to etch the first dielectric layer 401 by an anisotropic dry etching process until the surface of the second doped region 403 is exposed, forming a fifth opening, and removing the protective layer.

[0079] Referring to Fig. 9, the fourth opening 441 (as shown in Fig. 8) and the fifth opening 451 (as shown in Fig. 8) are filled with metal, a first contact layer 442 is formed in the fourth opening 441, and a second contact layer 452 is formed in the fifth opening 451. The surfaces of the first contact layer 442 and the second contact layer 452 are flush with the top surface of the second dielectric layer 406. The first contact layer 442 is electrically connected to at least one first metal gate 411, and the second contact layer 452 is electrically connected to at least one second doped region 403.

[0080] The materials and formation process of the first contact layer 442 and the second contact layer 452 are the same as those of the first contact layer of the first embodiment, and are not described in detail here.

[0081] In the present embodiment, the first contact layer 408 is electrically connected to the first metal gate 411 and the first doped region 402a, serving as a shared contact structure; the second contact layer 452 is electrically connected to the second doped region 403, and is electrically isolated from the second metal gate 421 by the third dielectric layer 409, serving as a self-aligned contact structure.

[0082] In other embodiments, the first contact layer is electrically connected to at least one first metal gate 411, and is electrically isolated from the first doped region 402 by the first dielectric layer 401, so that the first contact layer is only used to electrically connect the first metal gate 411 to other devices to meet specific industrial needs.

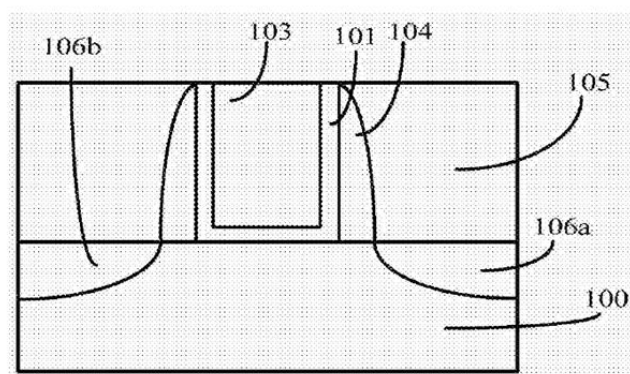
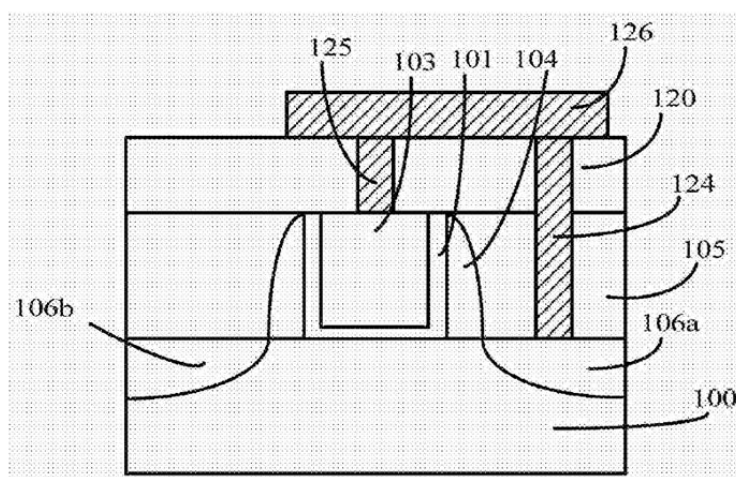
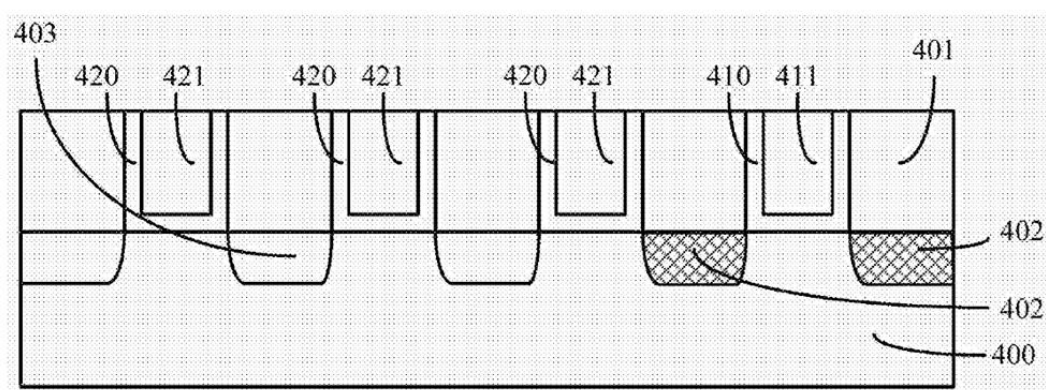
[0083] This embodiment can form a second contact layer while forming a first contact layer, further simplifying the process; the first contact layer can be electrically connected to at least one first doped region and at least one first metal gate at the same time, and be electrically isolated from the second metal gate by a third dielectric layer, and can serve as a shared contact structure connecting the first doped region and the first metal gate; the second contact layer can be electrically connected to the second doped region, and be electrically isolated from the second metal gate by a third dielectric layer, and can be used as a self-aligned contact structure.

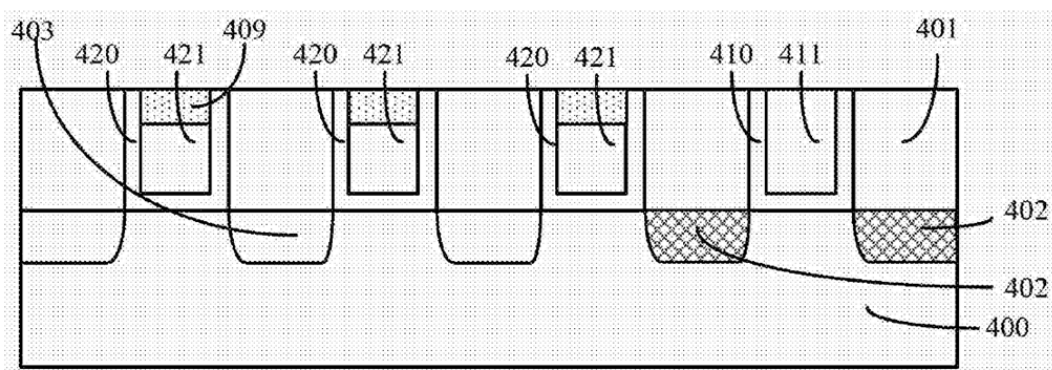
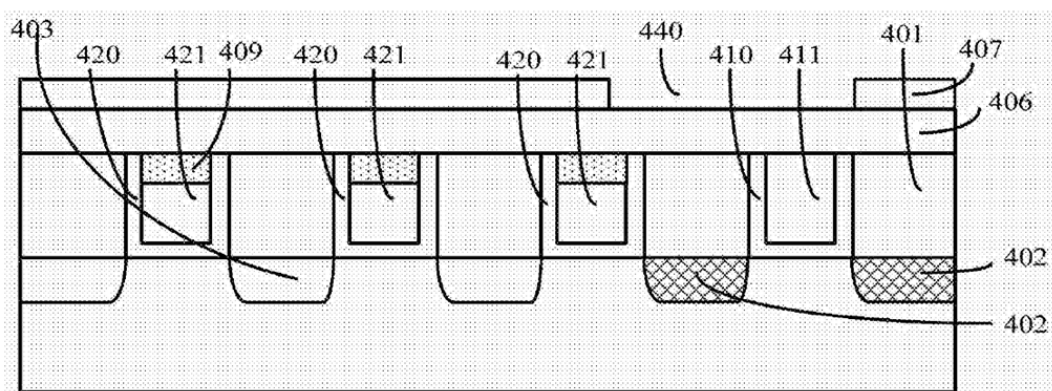
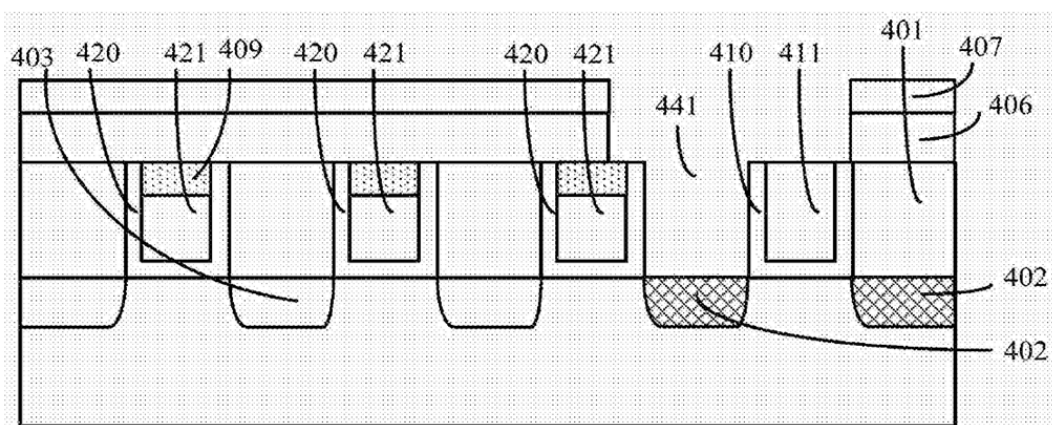
[0084] Accordingly, the present embodiment further provides a semiconductor structure. The difference between the semiconductor structure of the present embodiment and the semiconductor structure of the first embodiment is that, please continue to refer to Fig. 9, the second dielectric layer 406 and the first dielectric layer 401 have a fourth opening and a fifth opening, the fourth opening exposes the surface of at least one first metal gate 411, and the fifth opening exposes the surface of at least one second doped region 403; the fourth opening has a first contact layer 442, and the fifth opening has a second contact layer 452, the surfaces of the first contact layer 442 and the second contact layer 452 are flush with the top surface of the second dielectric layer 406, the first contact layer 442 is electrically connected to at least one first metal gate 411, and the second contact layer 452 is electrically connected to at least one second doped region 403.

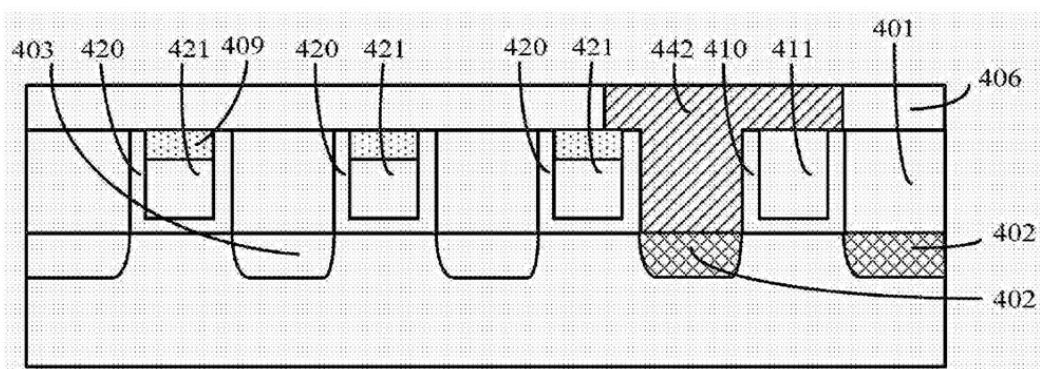
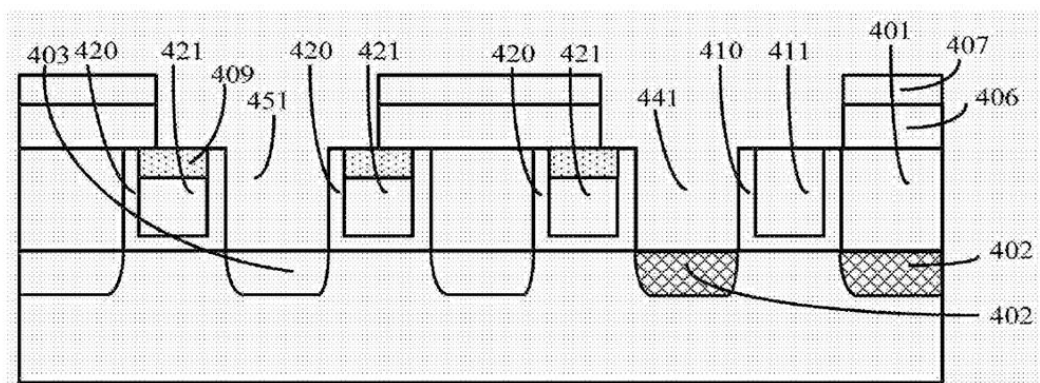
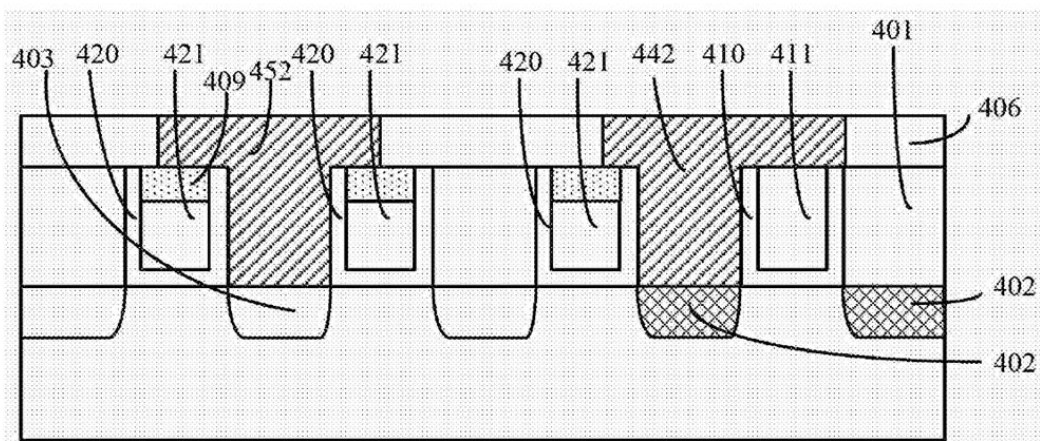
[0085] In the semiconductor structure of this embodiment, the first contact layer can be electrically connected to at least one first metal gate at the same time, and is electrically isolated from the second metal gate by the third dielectric layer, and can be used to electrically connect the first metal gate to other semiconductor devices; and the second contact layer can be electrically connected to the second doped region, and is electrically isolated from the second metal gate by the third dielectric layer, and can be used as a self-aligned contact structure.

[0086] It should be noted that all the foregoing embodiments use planar structure transistors merely as illustrative examples. In other embodiments, the transistor structure may adopt three-dimensional architectures such as fin field effect transistors (FinFETs). Particularly for three-dimensional transistors, the fabrication method disclosed in these embodiments demonstrates superior effectiveness, enabling formation of three-dimensional transistors with excellent performance and stability. For specific processes, please refer to the relevant descriptions above, which will not be repeated here.

[0087] Although the present invention has been disclosed above with reference to preferred embodiments, it is not intended to limit the scope of the invention. Any person skilled in the art may, without departing from the spirit and scope of the invention, make possible alterations and modifications to the technical solution of the present invention based on the methods and techniques disclosed above. Therefore, any simple modifications, equivalent variations, or modifications made to the above embodiments in accordance with the technical essence of the present invention, without deviating from the technical solution of the invention, shall fall within the scope of protection of the present invention.

**FIG. 1****FIG. 2****FIG. 3**

**FIG. 4****FIG. 5****FIG. 6**

**FIG. 7****FIG. 8****FIG. 9**



March 28, 2025

**Certification**

**Welocalize Translations**

**TRANSLATOR'S DECLARATION:**

I, Cinthia Wang, am fluent in both the Chinese and English languages. I have translated the application CN103915384B from Chinese to English. I hereby certify that the translation is accurate and complete to the best of my judgment and ability. I understand that willful false statements and the like are punishable by fine or imprisonment, or both, pursuant to 18 U.S.C. § 1001.

I certify under penalty of perjury under the laws of the United States that the foregoing is true and correct.

A handwritten signature in black ink that reads "Cinthia Wang".

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Cinthia Wang

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