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Chi

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(54) **METHODS OF FORMING SELF-ALIGNED CONTACTS FOR A SEMICONDUCTOR DEVICE**

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H01L 21/3115 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 21/3115*** (2013.01)
USPC **438/299**

(58) **Field of Classification Search**
USPC 438/299, 229, 230, 514, 525, 533; 257/E21.085
See application file for complete search history.

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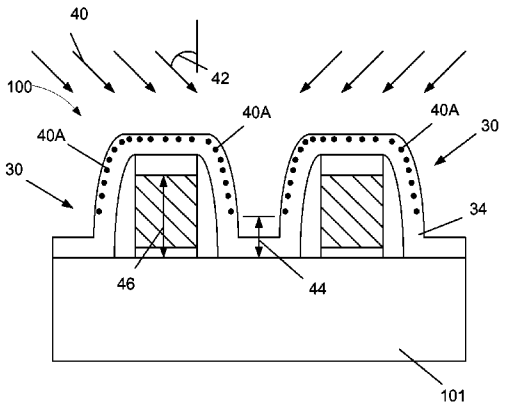
(74) *Attorney, Agent, or Firm* — Amerson Law Firm, PLLC

(57) **ABSTRACT**

One illustrative method disclosed herein involves forming gate structures for first and second spaced-apart transistors above a semiconducting substrate, forming an etch stop layer above the substrate and the gate structures, performing at least one angled ion implant process to implant at least one etch-inhibiting species into less than an entirety of the etch stop layer, after performing at least one angled ion implant process, forming a layer of insulating material above the etch stop layer, performing at least one first etching process to define an opening in the layer of insulating material and thereby expose a portion of the etch stop layer, performing at least one etching process on the exposed portion of the etch stop layer to define a contact opening therethrough that exposes a doped region formed in the substrate, and forming a conductive contact in the opening that is conductively coupled to the doped region.

25 Claims, 12 Drawing Sheets



TSMC EXHIBIT 1018

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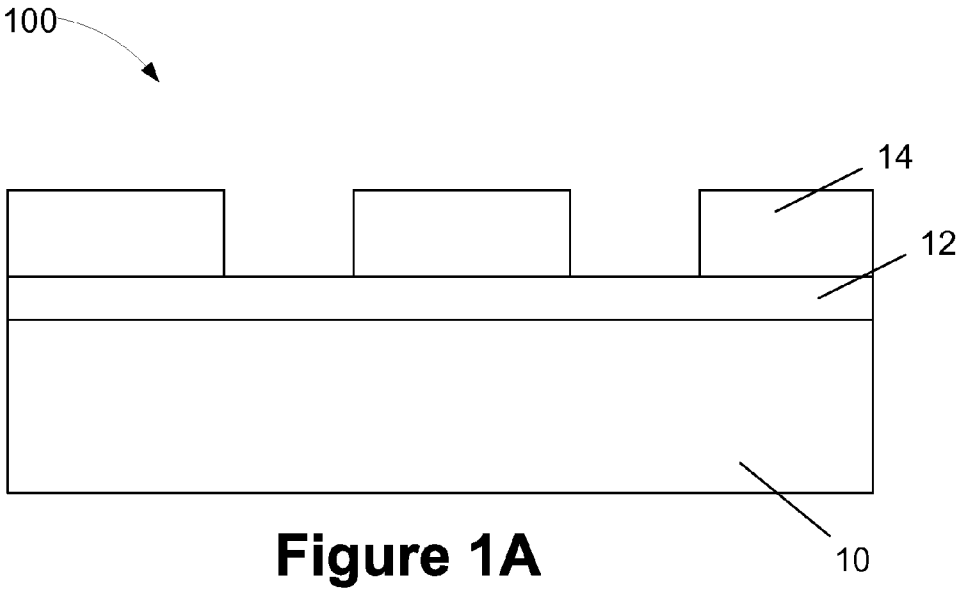


Figure 1A

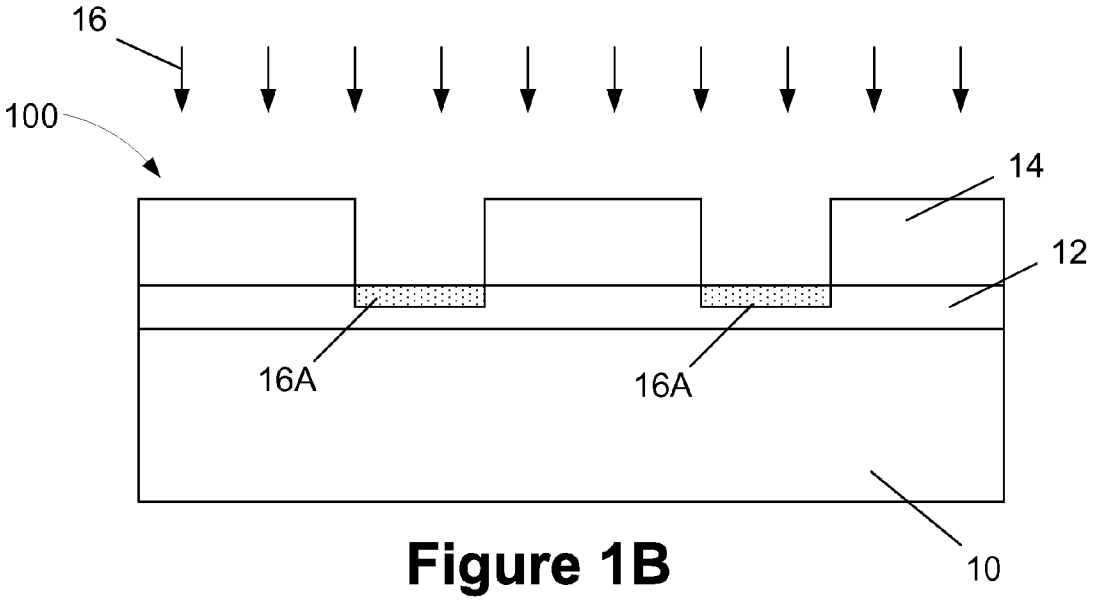


Figure 1B

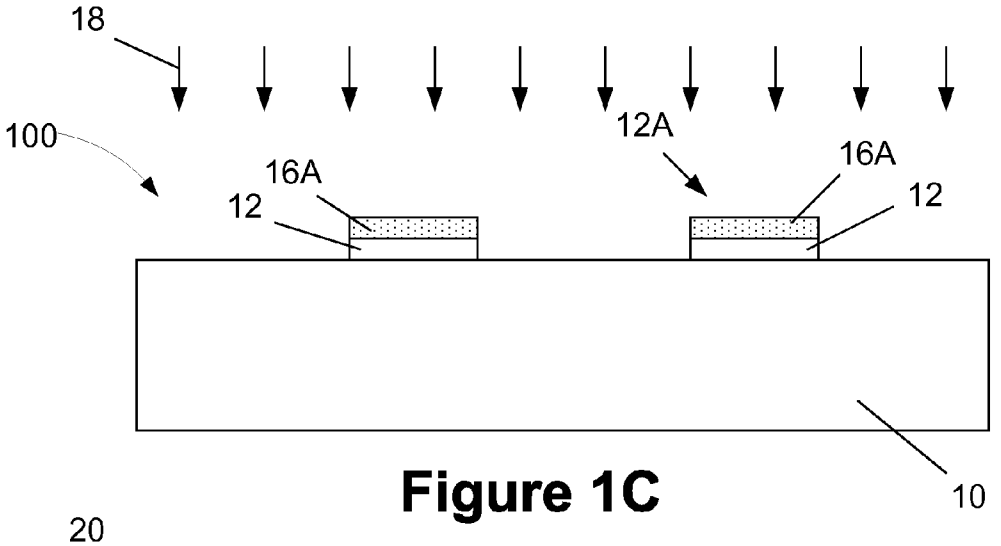


Figure 1C

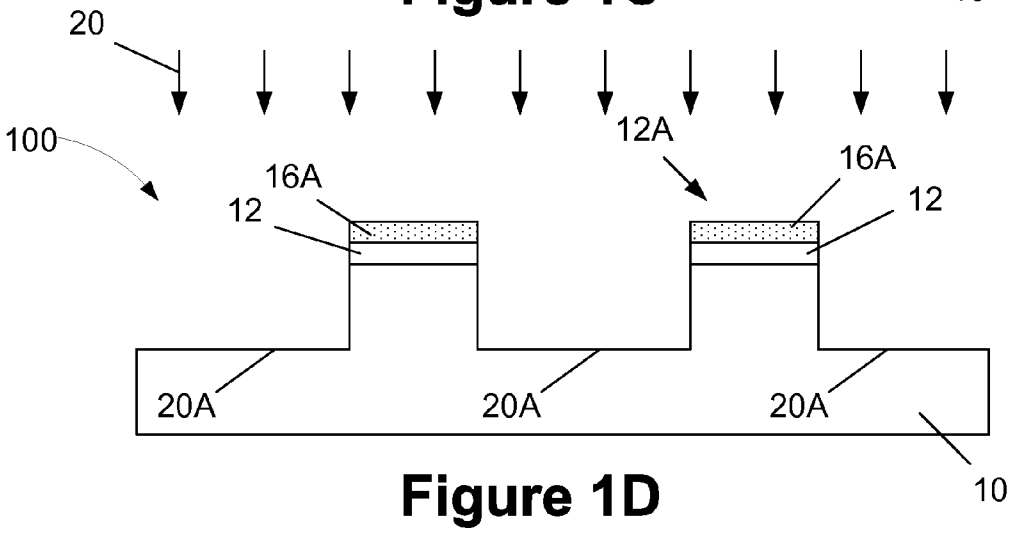


Figure 1D

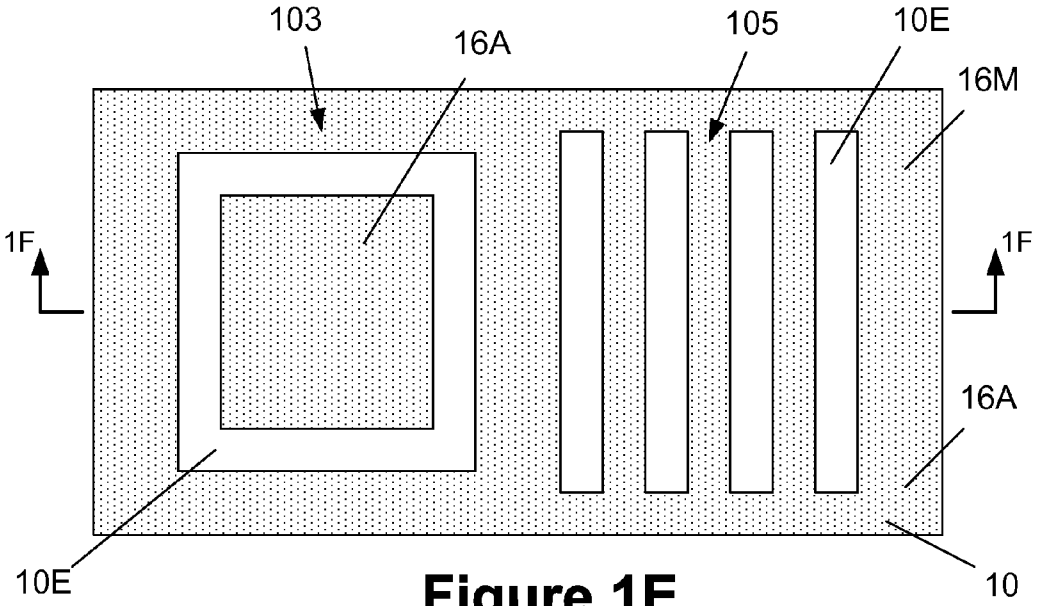
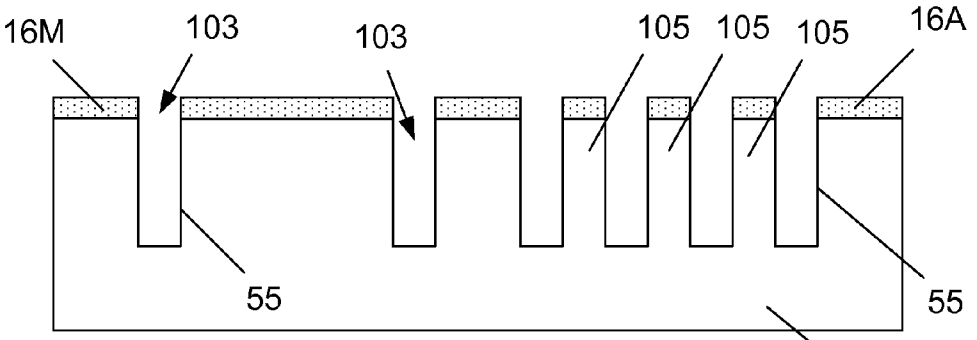


Figure 1E



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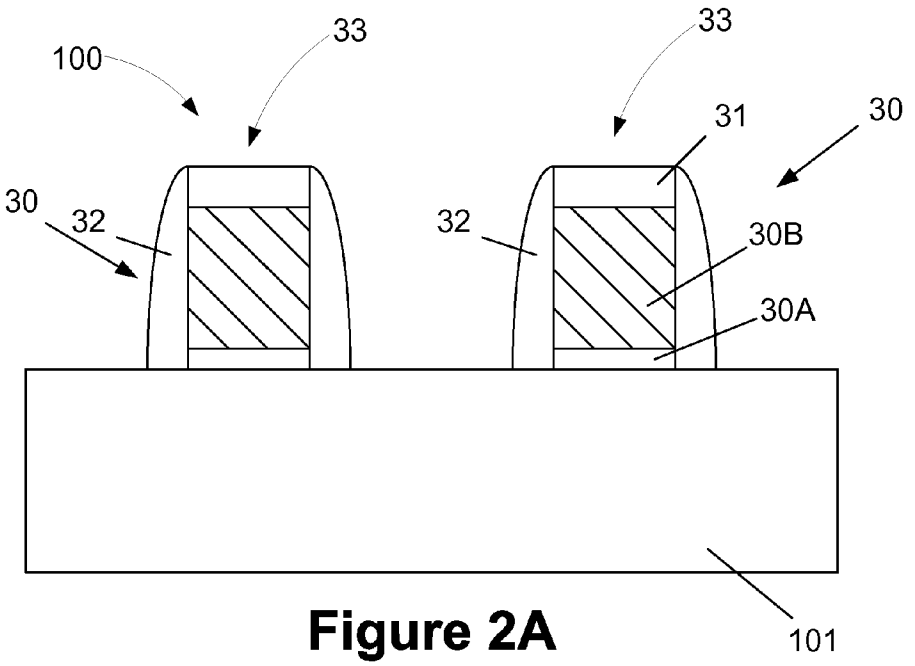

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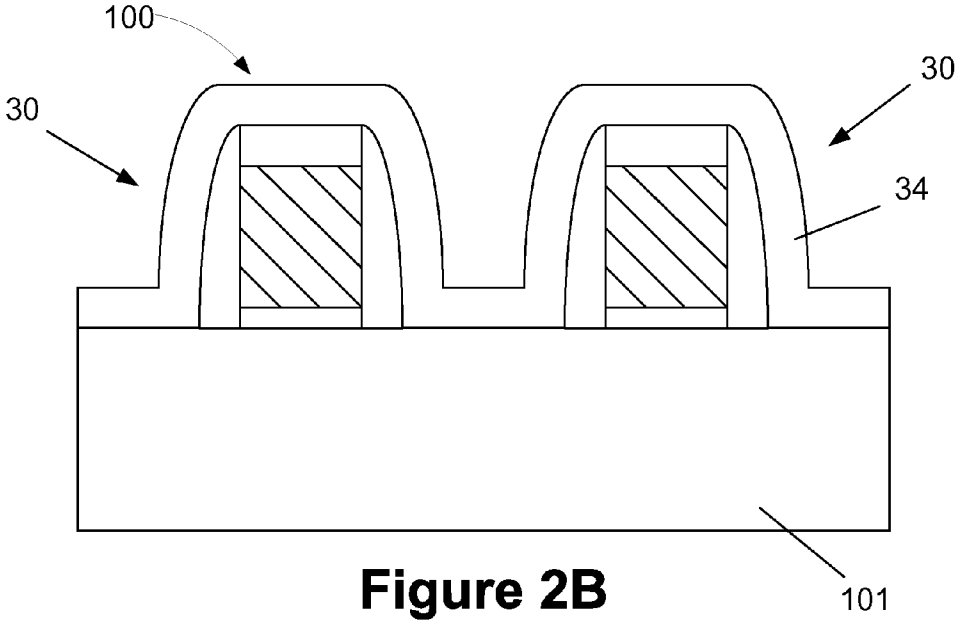

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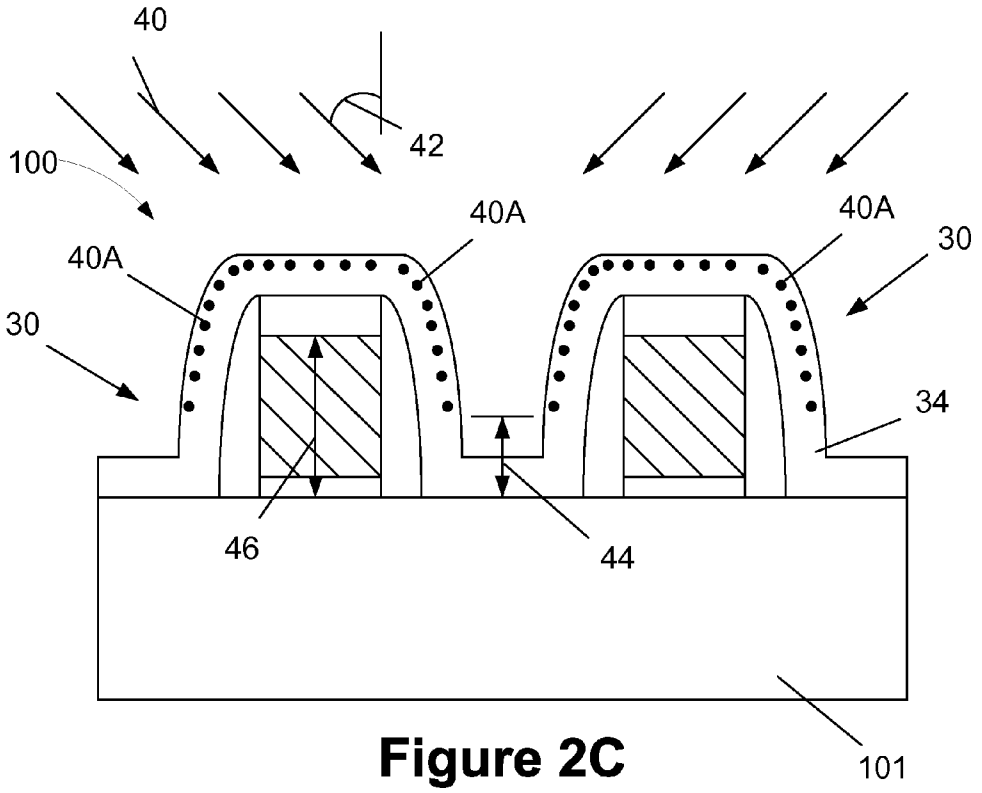

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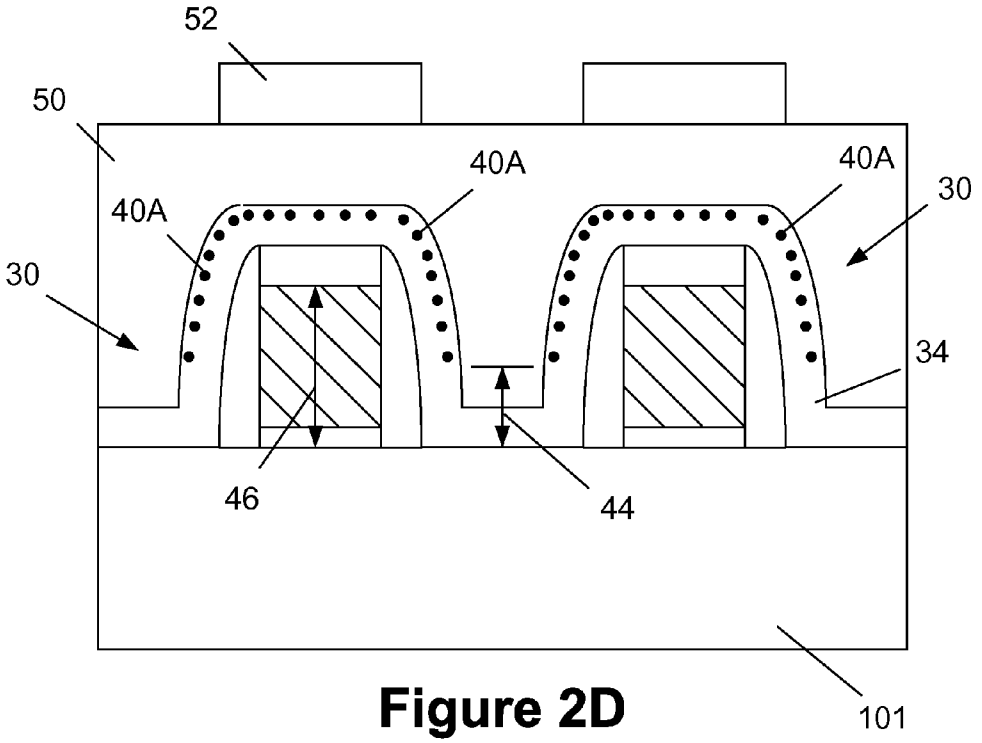

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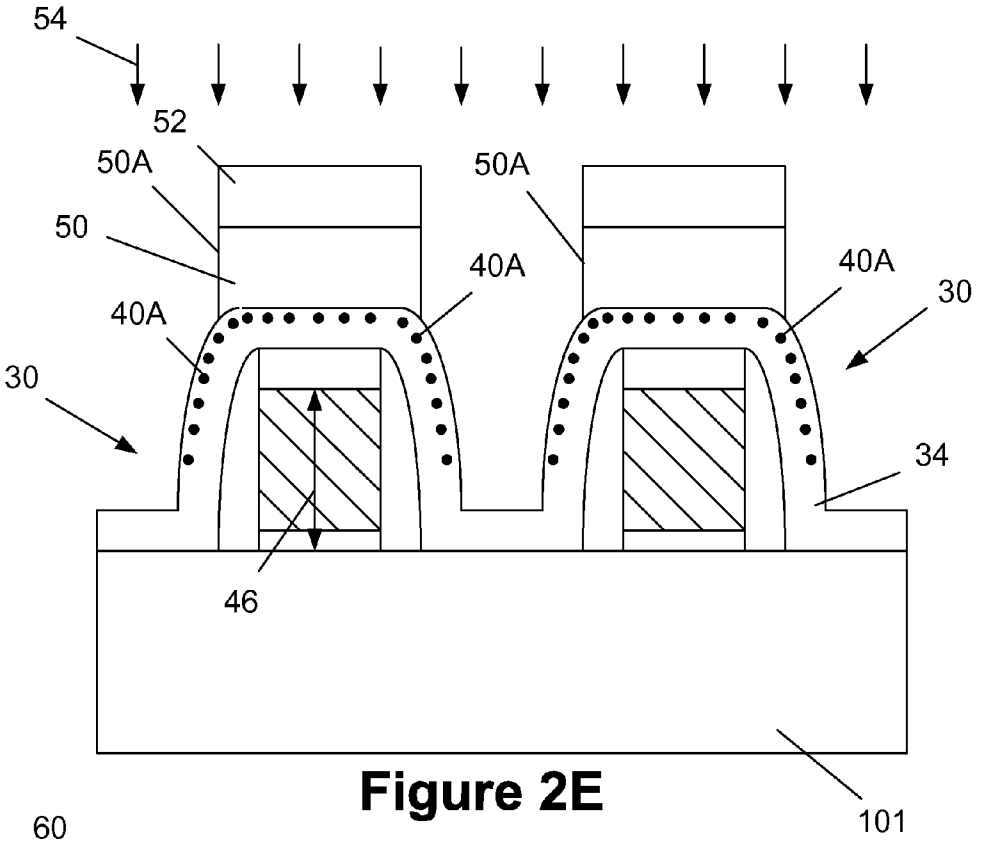

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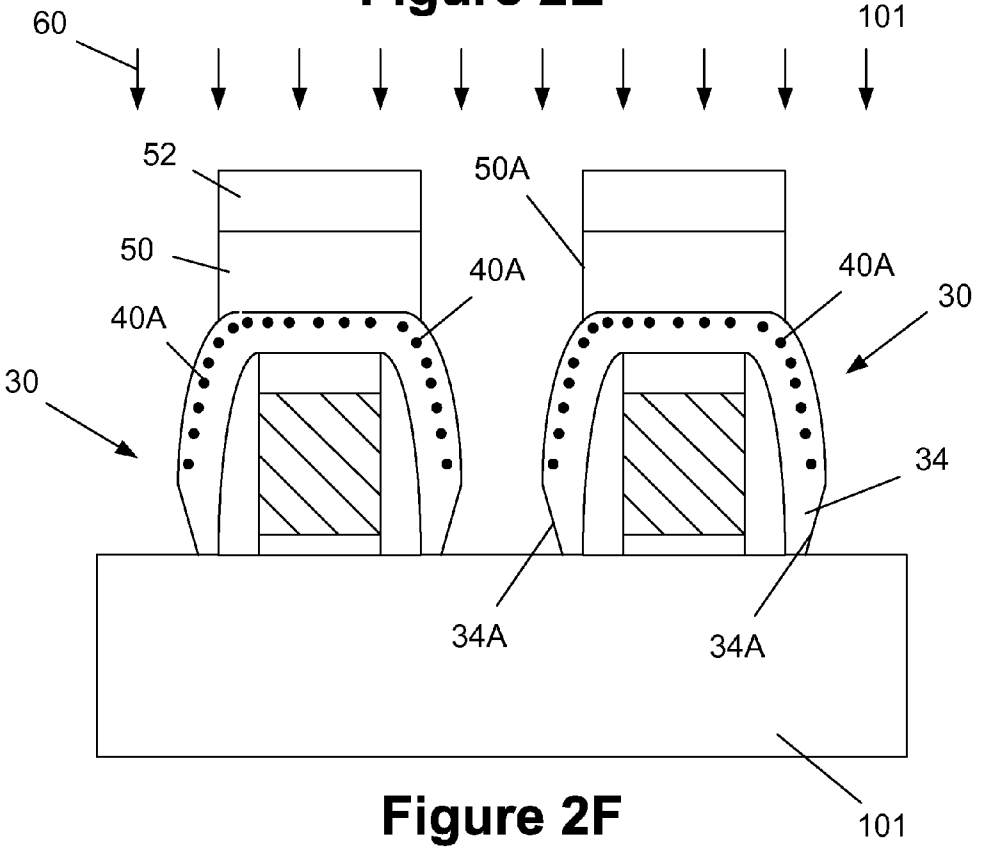

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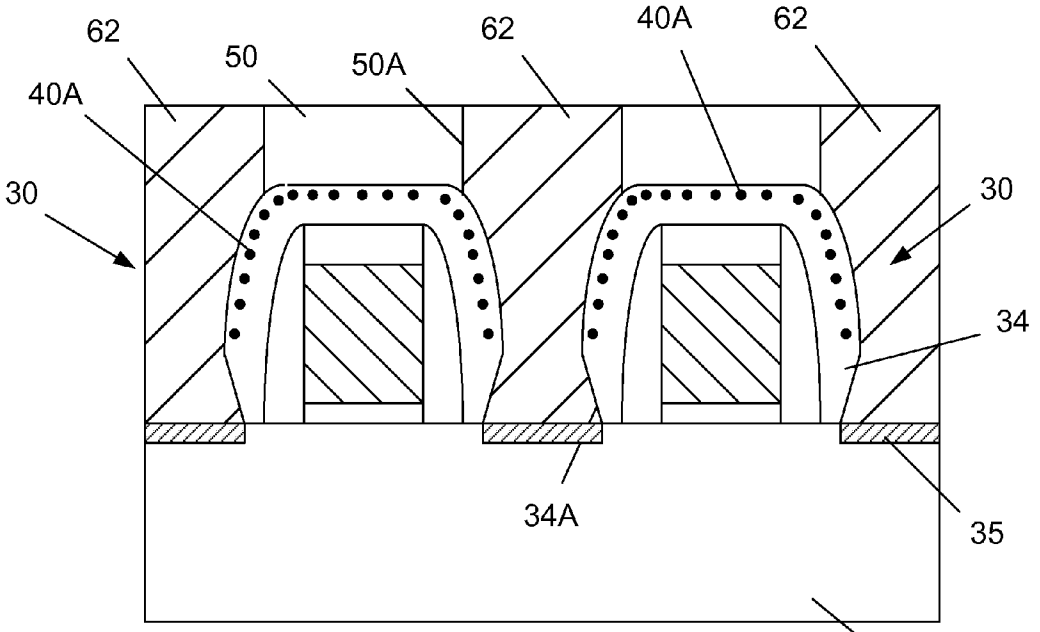

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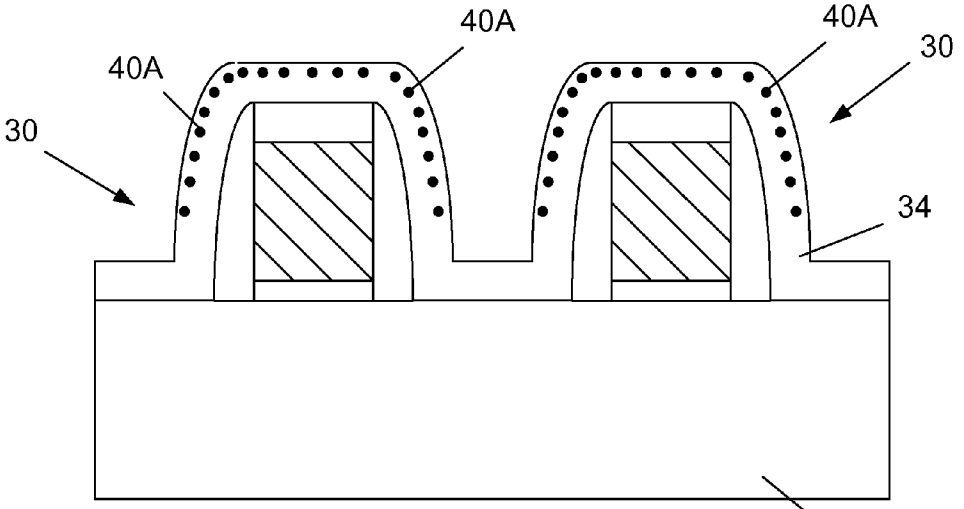
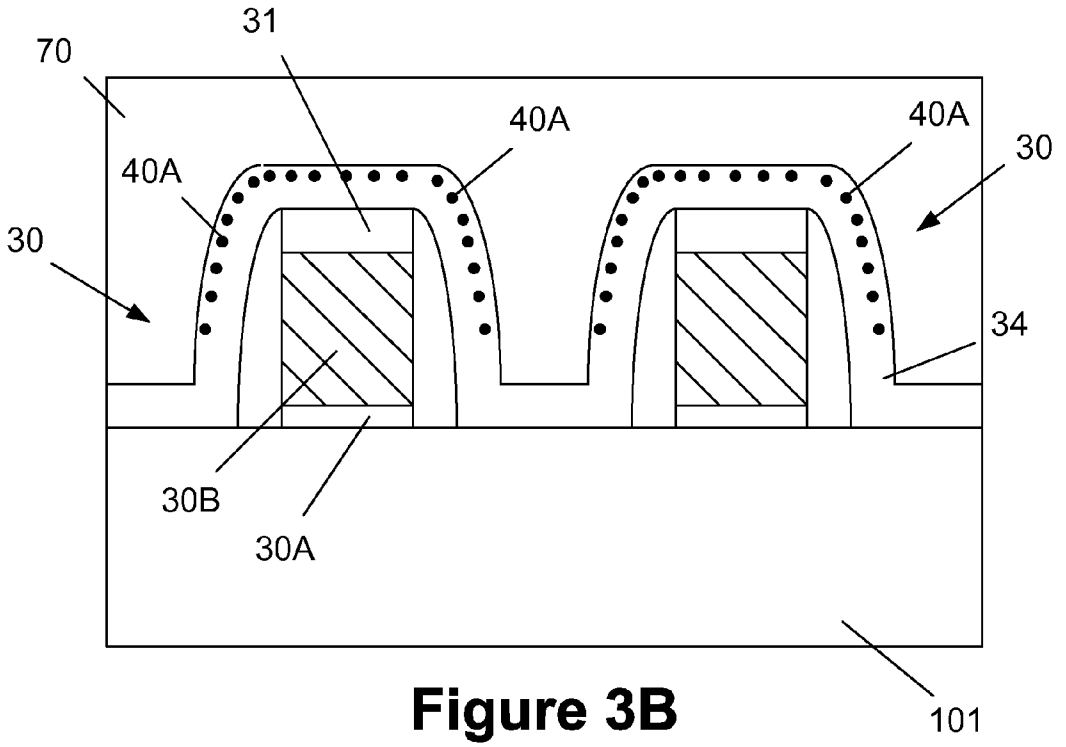


Figure 3A



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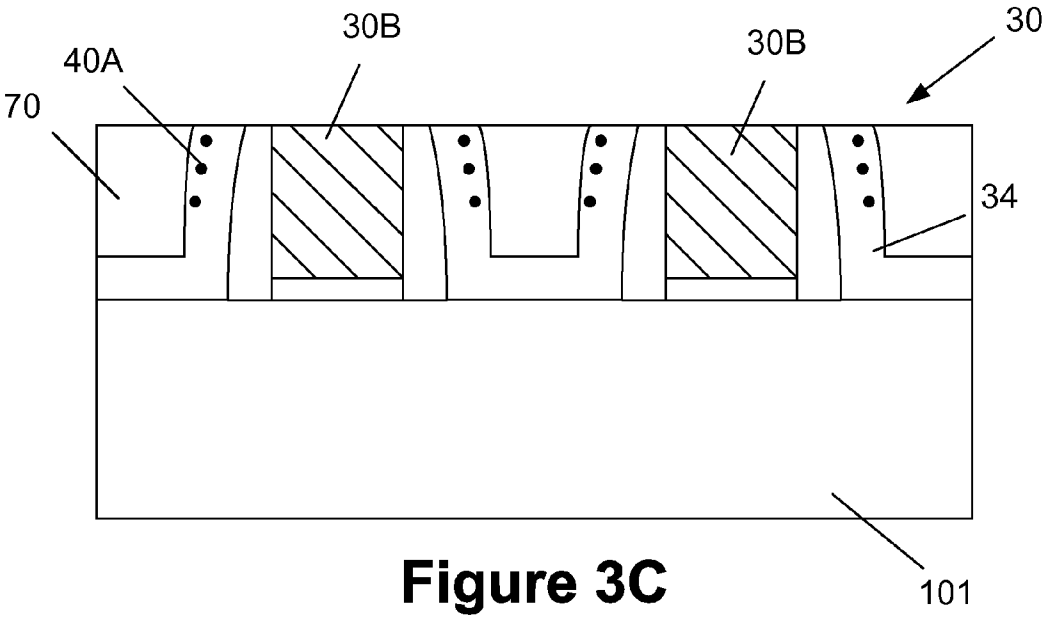

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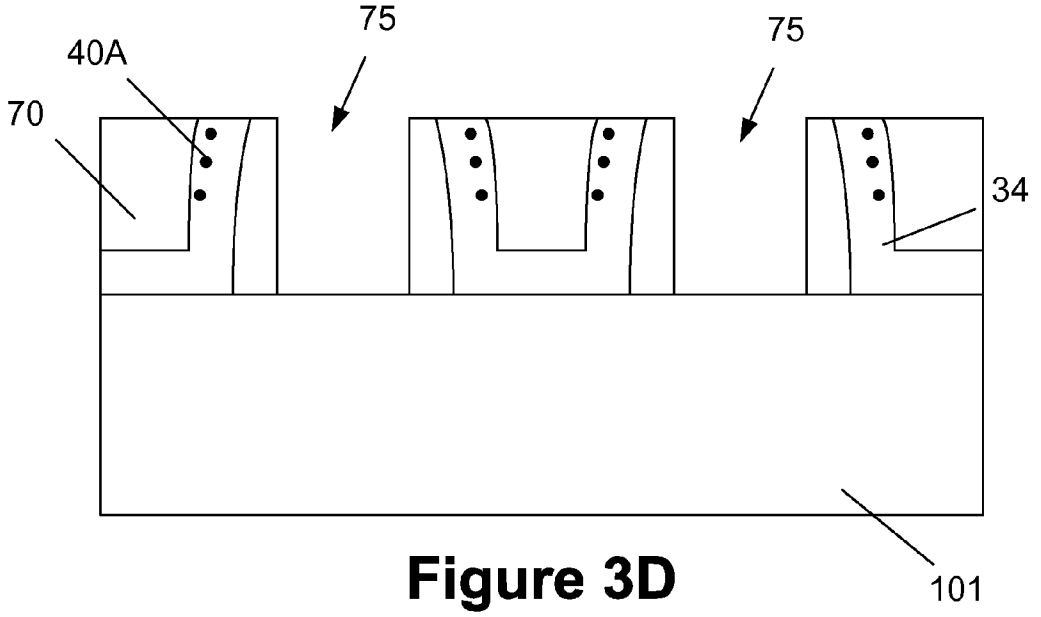

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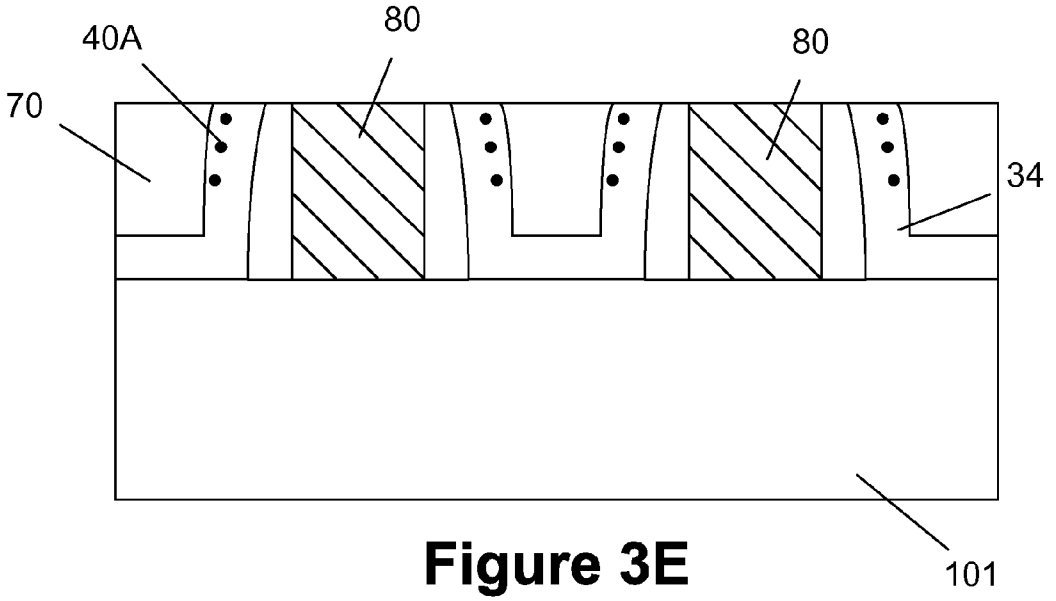

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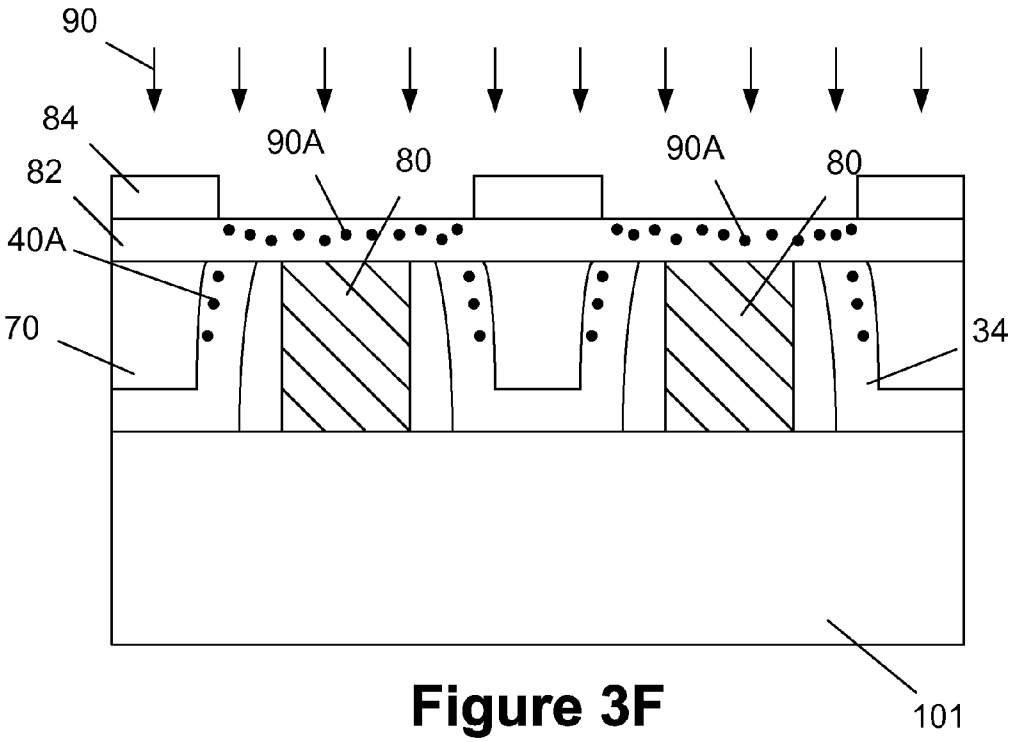

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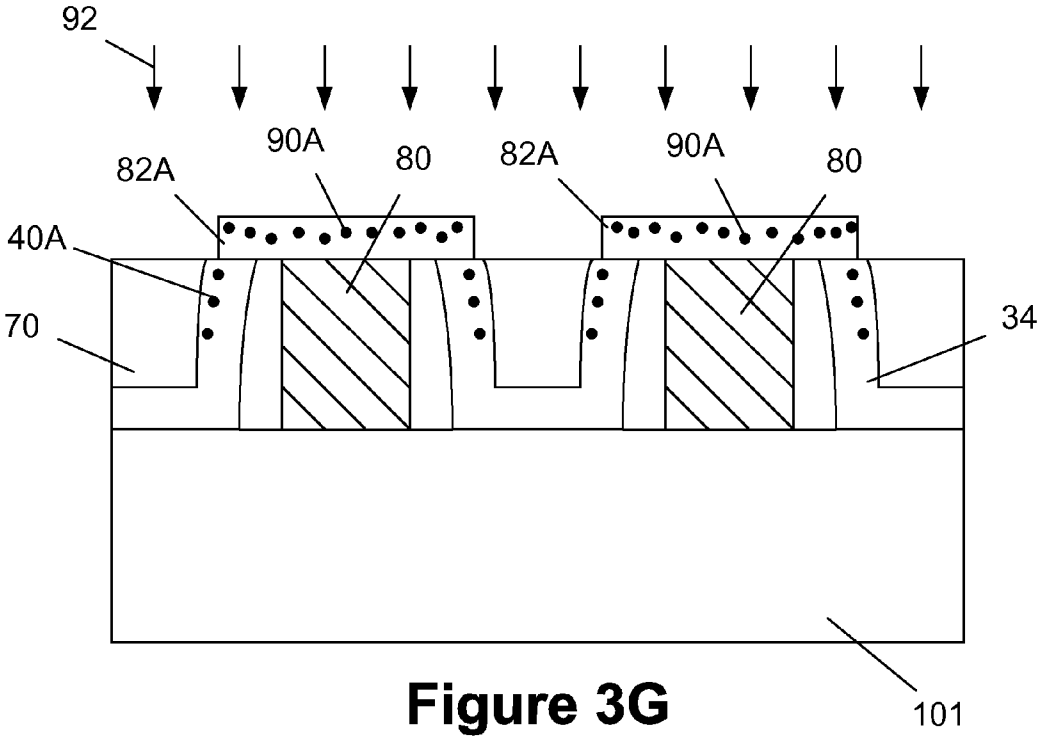

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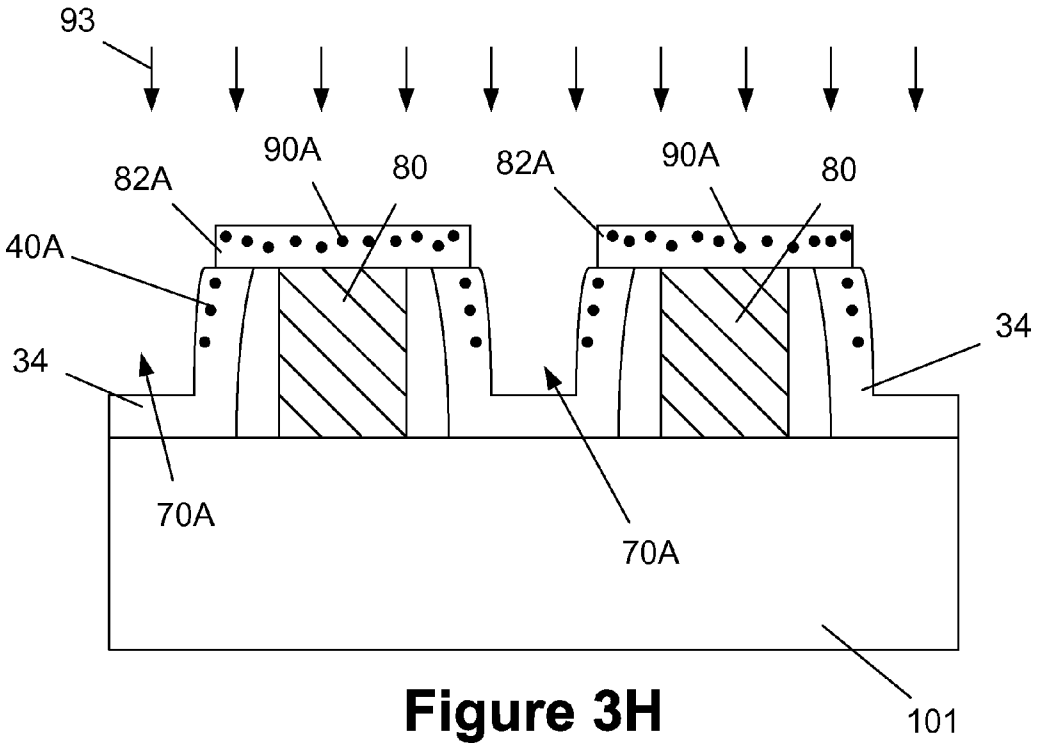

Figure 3H

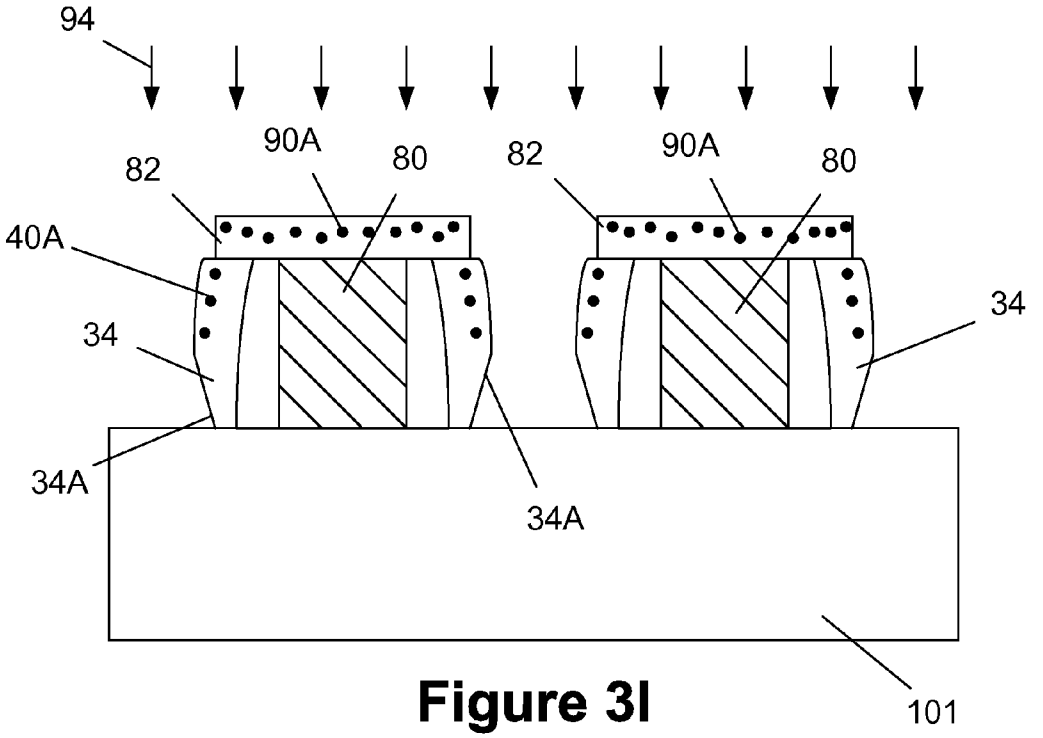

Figure 3I

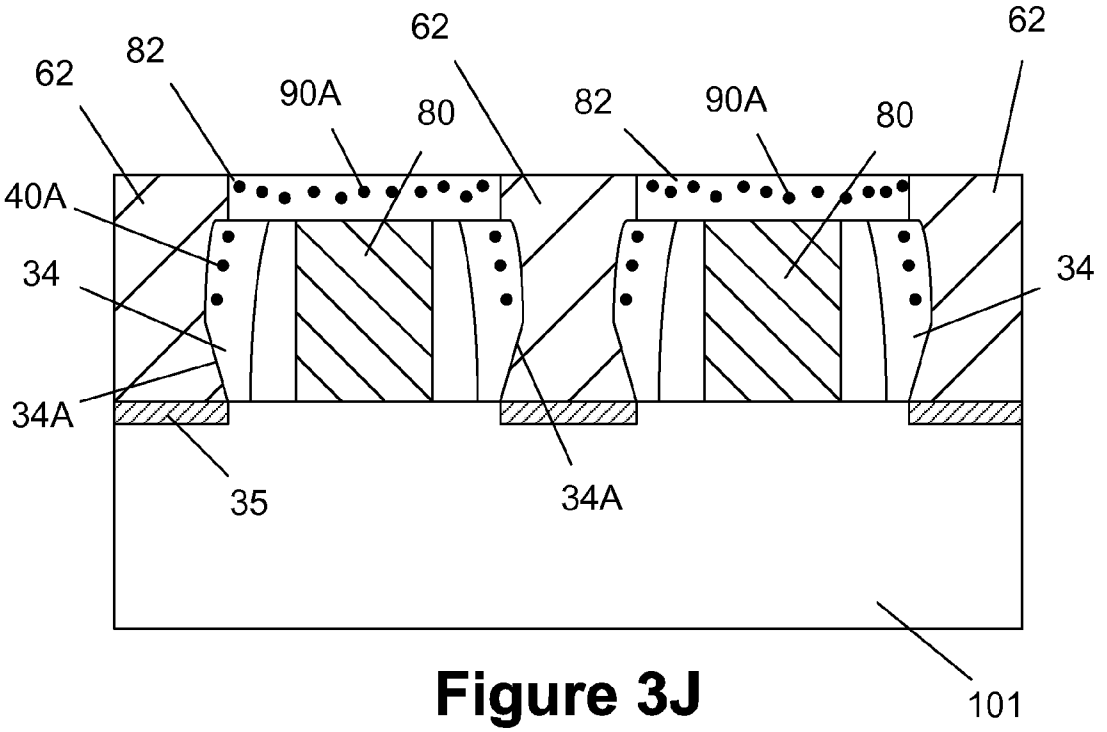

Figure 3J

METHODS OF FORMING SELF-ALIGNED CONTACTS FOR A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

Generally, the present disclosure relates to the manufacture of sophisticated semiconductor devices, and, more specifically, to various methods of forming self-aligned contacts (SAC) for semiconductor devices such as transistors.

2. Description of the Related Art

The fabrication of advanced integrated circuits, such as CPU's, memory devices, ASIC's (application specific integrated circuits) and the like, requires the formation of a large number of circuit elements in a given chip area according to a specified circuit layout. Metal-Oxide-Field-Effect-Transistors (MOSFETs) represent one dominant type of circuit element that substantially determines performance of the integrated circuits. MOSFETs are typically either an N-type (NFET) device or a P-type (PFET) device and they are complementary to each other (thus, when both types are used in an integrated circuit product, the technology is referred to as C-MOSFET or CMOS technology). During the fabrication of complex integrated circuits, millions of CMOS transistors, e.g., NFETs and/or PFETs, are formed on a substrate including a crystalline semiconductor layer. A field effect transistor, irrespective of whether an NFET or a PFET is considered, typically comprises so-called PN junctions that are formed by an interface of highly doped regions, referred to as drain and source regions, with a slightly doped or non-doped region, referred to as a channel region, disposed between the highly doped source/drain regions in the substrate. The channel length of a MOS transistor is generally considered to be the lateral distance between the source/drain regions.

In modern semiconductor devices, the gate structures are very small and have a very small distance or pitch between adjacent gate structures. As CMOS device dimensions continue to be reduced in size, e.g., 20-30 nm gate lengths and gate pitches on the order of 60-90 nm at the 20 nm CMOS technology node, the formation of conductive contacts to the source/drain regions of a transistor has become very challenging. Such contacts are typically formed by direct patterning techniques using traditional photolithography and etching techniques. Given the decrease in device dimension, device designers have resorted to making the conductive contacts very small so as to have some tolerance or "process margin" for positioning the contact between adjacent gate structures. If the process margin is not large enough with contact holes that are aligned poorly and near the spacer shoulder of gate structures, the spacers on the sidewall of gate structures can be damaged by the plasma oxide etching during contact formation and result in circuit failures due to the "short" between the contact and the gate electrode. However, when using such techniques, the accuracy in forming such contact openings is very critical. Errors in pattern alignment can ultimately result in the formation of conductive contacts that are even smaller than intended by the device designer. As a result, such excessively small conductive contacts, and the resulting underlying metal silicide regions, can increase the resistance of the contact structure and thereby reduce the performance of the resulting transistors and integrated circuit products incorporating such devices. In a worst case scenario, such misalignment can lead to short circuits and total device failure as described.

Another technique that device designers have developed in an effort to meet the challenge of making contact to the

source/drain regions of such very small devices involves the formation of so-called self-aligned contacts (SAC). In general, in a self-aligned contact, the configuration of the opening for the contact is essentially defined by the configuration of adjacent structures, e.g., sidewall spacers on adjacent gate structures. The contact opening and the resulting conductive contact are "self-aligned" in the sense that the location and even the configuration of the final opening is not directly defined by traditional patterning and etching techniques. Rather, a "self-aligned" contact is essentially formed in the opening that is defined by selectively etching one material, e.g., silicon dioxide, relative to other materials, such as silicon nitride sidewall spacers on adjacent gate structures. One typical self-aligned contact (SAC) process involves performing a first plasma etching process on a layer of insulating material, e.g., silicon dioxide, to define the contact opening. This first etching process is performed until the underlying etch stop layer, e.g., silicon nitride, is exposed. Thereafter, a second plasma etching process is performed on the exposed etch stop layer until such time as the underlying source/drain region that is formed in the substrate is exposed. The silicon nitride etch stop layer (which was also deposited on the upper portion of the gate structures and the sidewall spacers) needs to be highly resistant to the etch chemistry employed in the first plasma etching process performed on the insulating material, e.g., silicon dioxide, to insure the integrity of the gate encapsulation is not jeopardized. The silicon nitride etch stop layer should also be of sufficient thickness along the side of the gate structures to withstand the second plasma etch process that etches through the silicon nitride etch stop layer and exposes the source/drain region.

The first plasma etching process, which is typically performed to etch a layer of silicon dioxide, is performed using a plasma based etch process with an etch chemistry that is a combination of carbon and fluorine containing gases (e.g., $C_4F_8/CH_2F_2/Ar$, or $C_4F_6/Co/Ar$, etc.). Polymer formation during the first plasma etching process is a key factor in maintaining an anisotropic and vertical profile for the contact opening and in protecting the upper portion of the silicon nitride etch stop layer on the gate structures as well as the etch stop layer positioned on the sidewall spacer of the gate structure. If there is no polymer production during the first plasma etching process (the etching of the silicon dioxide insulating layer) and the second plasma etching process (the etching of the silicon nitride etch stop layer), then the upper shoulder of the silicon nitride etch stop layer may be completely consumed, which can lead to the formation of a short circuit between the gate electrode and the contact. If there is too much polymer formation during the first plasma etching process, then it may be difficult to break through the etch stop layer during the second plasma etching process that is performed to expose the source/drain region. Such a condition may result in an "open" contact which can lead to device failure.

The use of self-aligned contacts (SAC) in memory devices has been employed for several years. In a memory array, to the extent that there are defects in the formation of such self-aligned contacts (SAC) in the memory array, e.g., a short circuit was created between the conductive contact and the cells, such a problem could be readily addressed in such a memory array by using well-known redundancy schemes, i.e., redundant memory cells and repair control circuits. However, when logic circuits, such as microprocessor circuits, are involved, it is much more difficult to locate where such an error or defective contact is located, and there is limited and costly capability for fixing such problems in a logic circuit and then only when such defective contacts happen to be

located in a redundant circuit block. As a result, in some cases, even one defect in forming conductive contacts to the source/drain regions of a transistor device can result in complete circuit failure with the attendant loss of yield and increased production costs. Even when repairs are possible, there is a very low success rate on such repairs. Thus, for logic circuits, the formation of self-aligned contacts (SAC) must be much more accurate and defect-free than the self-aligned contact (SAC) formation processes used in memory devices.

There have been attempts to improve the accuracy and reliability of the processes used to form self-aligned contacts (SAC). For example, current improvement methods focus on enhancing the etch selectivity between a silicon dioxide insulating layer and a silicon nitride etch stop layer by fine-tuning the plasma etch chemistry for such materials, e.g., using C_4F_6 or C_5F_8 gases with better control of the ratio of carbon to fluorine for controlling polymer generation. Another technique that has been employed to improve self-aligned contact (SAC) formation processes involves using different materials for the etch stop layer, such as silicon or carbon doped materials, silicon-rich silicon oxynitride, aluminum dioxide, etc. One other technique involves carbon doping of the silicon nitride etch stop layer to reduce the nominal etch rate of the original silicon nitride material, but this process is not effective at solving the problems mentioned above as there is still a chance of consuming the etch stop layer in problematic areas identified above. Another technique that has been employed is to try to locally increase the thickness of the etch stop layer near the upper corner of the gate structure. However, this latter approach greatly increases processing complexities and costs by requiring the performance of additional steps such as thin-film deposition, lithography, etching, etc.

The present disclosure is directed to various methods of forming self-aligned contacts (SAC) for semiconductor devices such as transistors that may avoid, or at least reduce, the effects of one or more of the problems identified above.

SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

Generally, the present disclosure is directed to various methods of forming self-aligned contacts (SAC) on semiconductor devices such as transistor devices. As will be appreciated by those skilled in the art after a complete reading of the present application, the present techniques may be employed when manufacturing transistor devices using either so-called "gate-first" or "replacement gate" (RMG) techniques, and the techniques disclosed herein may be employed to form planar field effect transistor devices, as well as on three dimensional devices such as FinFET devices.

One illustrative method disclosed herein involves forming gate structures for first and second spaced-apart transistors above a semiconducting substrate, forming an etch stop layer above the substrate and the gate structures, performing at least one angled ion implant process to implant at least one etch-inhibiting species into less than an entirety of the etch stop layer, after performing at least one angled ion implant process, forming a layer of insulating material above the etch stop layer, performing at least one first etching process to define an opening in the layer of insulating material and thereby expose a portion of the etch stop layer, performing at least one etching process on the exposed portion of the etch stop layer to define a contact opening therethrough that exposes a doped region formed in the substrate, and forming a conductive contact in the opening that is conductively coupled to the doped region.

Another illustrative method disclosed herein involves forming gate structures for first and second spaced-apart transistors above a semiconducting substrate, forming an etch stop layer above the substrate and the gate structures, performing at least one angled ion implant process to implant at least one polymer-forming species into less than an entirety of the etch stop layer, after performing at least one angled ion implant process, forming a layer of insulating material above the etch stop layer, performing at least one first etching process to define an opening in the layer of insulating material and thereby expose a portion of the etch stop layer, performing at least one plasma-based etching process on the exposed portion of the etch stop layer to define a contact opening therethrough that exposes a doped region formed in the substrate, and forming a conductive contact in the opening that is conductively coupled to the doped region.

Yet another illustrative method disclosed herein involves forming gate structures for first and second spaced-apart transistors above a semiconducting substrate, forming an etch stop layer above the substrate and the gate structures, performing at least one angled ion implant process to implant at least one etch-inhibiting species into less than an entirety of the etch stop layer, after performing at least one angled ion implant process, forming a layer of insulating material above the etch stop layer, performing at least one first etching process to define an opening in the layer of insulating material and thereby expose a portion of the etch stop layer, performing at least one wet etching process on the exposed portion of the etch stop layer to define a contact opening therethrough that exposes a doped region formed in the substrate, and forming a conductive contact in the opening that is conductively coupled to the doped region.

BRIEF DESCRIPTION OF THE DRAWINGS

The disclosure may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

FIGS. **1**A-**1**D depict various illustrative methods disclosed herein for forming a generic hard mask layer that may be employed in a variety of applications as it relates to the fabrication of, for example, integrated circuit products;

FIGS. **1**E-**1**F depict a particular embodiment disclosed herein wherein an etch mask comprised of a plurality of implant regions may be formed and used to etch various features in a substrate;

FIGS. **2**A-**2**G depict various illustrative methods disclosed herein for forming self-aligned contacts for an integrated circuit product; and

FIGS. **3**A-**3**J depict various illustrative methods disclosed herein for forming self-aligned contacts for an integrated circuit product wherein a "gate-last" or a replacement metal gate technique is employed.

While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is

to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION

Various illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present subject matter will now be described with reference to the attached figures. Various structures, systems and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present disclosure with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present disclosure. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, i.e., a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, i.e., a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

The present disclosure is directed to various methods of forming hard mask layers for use in manufacturing semiconductor devices and to the formation of self-aligned contacts (SAC) on semiconductor devices. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of devices (e.g., planar devices and non-planar devices such as FinFETs) and technologies, e.g., NFET, PFET, CMOS, etc., and is readily applicable to a variety of integrated circuit products, including, but not limited to, ASIC's, logic devices, memory devices, etc. With reference to the attached drawings, various illustrative embodiments of the methods disclosed herein will now be described in more detail.

FIGS. **1**A-**1**D depict various illustrative methods disclosed herein for forming a generic hard mask layer that may be employed in a variety of applications as it relates to the fabrication of, for example, integrated circuit products. As shown in FIG. **1**A, a layer of hard mask material **12** is formed above a structure **10**. The structure **10** is intended to be representative of any type of structure or layer of material, such as those that may be employed in manufacturing integrated circuit products. For example, the structure **10** may be a semiconducting substrate, a layer of metal (or its nitride or oxide), a layer of insulating material, a layer of polysilicon, a layer of gate electrode material, etc. The layer of hard mask material **12** may comprised of a variety of different materials, e.g., silicon nitride, silicon dioxide, a metal, oxides or nitrides of metals, such as titanium, tantalum, aluminum, tungsten, etc., its thickness may vary depending upon the particular application, e.g., less than 100 nm, and it may be formed by a variety of techniques, e.g., chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), etc. In one illustrative embodiment, the layer of hard mask material **12** may be a layer of silicon nitride that has a thickness of about 30 nm that was formed by performing a CVD process.

Also depicted in FIG. **1**A is an illustrative patterned implant mask **14** that is patterned to expose portions of the layer of hard mask material **12** for further processing. In one illustrative embodiment, the patterned implant mask **14** is a patterned layer of photoresist material that was formed using traditional photolithography tools and techniques.

Next, as shown in FIG. **1**B, an ion implant process **16** is performed through the patterned implant mask **14** to form implant regions **16**A in the layer of hard mask material **12**. In one illustrative example, the ion implant process may be performed to implant an "etch-inhibiting" species such as fluorine (F), carbon (C), nitrogen (N) or a combination of such materials with various implant dosages and implant energy levels. As described more fully below, the implanted etch-inhibiting species may be employed to effectively increase the etch resistance of the hard mask layer **12** during the performance of either wet or dry (plasma-based) etching processes. In the case of a dry plasma-based etching process, the implanted etch-inhibiting species act with radicals in the plasma process to form polymers that inhibit the etching of the portions of the hard mask layer **12** that have the implant regions **16**A formed therein during the dry etching process as compared to other portions of the hard mask layer **12** where the etch-inhibiting species was not implanted. In the case of a wet etching process, the ions in the etch solution bath tend to act with the implanted etch-inhibiting species to form a protective "interfacial" layer between the surface of the hard mask layer **12** and the solution to thereby locally reduce the etch rate of the hard mask material by the wet etching solution. This technique is effective especially for "buffered" wet etching solutions where significant amounts of carbon (C), fluorine (F), and nitrogen (N) radicals are added to the etching solution. The protective interfacial layer formed between the implanted surface of the hard mask layer and the wet etching solution effectively reduces the etching rate in the region where the protective interfacial layer is formed. The magnitude of the reduction of the etching rate using this wet etching technique is similar to the reduction in etch rate that is obtained when the protective polymer material is formed in the case where plasma etching is employed.

The parameters of the ion implant process **16** may vary depending upon the particular application. For example, the ion implant process **16** may be performed using an implant dose in the range of 10^{14}-10^{16} ions/cm^2 and at multiple energy levels in the range of 1-500 keV. In one particularly illustrative example, where a dry plasma etching process is to be performed, if the expected polymer chain is based upon CF_2 radicals, then the ion implant process **16** may be performed using carbon and fluorine (in a ratio of about 1:2 (for matching the ratio of carbon and fluorine in the polymer material)) with an implant dose of about 10^{15} ions/cm^2 and at an energy level of about 1-10 keV such that the polymer material is formed near the surface of the hard mask layer **12**. The depth of the implant regions **16**A may vary depending upon the particular application and it may be controlled by controlling the implant energy of the implant process. In one illustrative example, where the layer of hard mask material **12** has an as-formed thickness of about 30 nm, the implant regions **16**A may have a target depth of about 10-15 nm. As mentioned

above and as will be described more fully below, in some embodiments disclosed herein, the etch-inhibiting species (C, F, N, etc.) in the implant regions **16**A are essentially polymer forming species that will serve as seeding sites for polymerization, e.g., C—F polymerization, during a subsequent plasma etching process that is performed on the layer of hard mask material **12** and on the substrate materials **10** below the hard mask material **12**. In one embodiment, the nitrogen atoms serve as a catalyst for nucleation in the polymerization process. Other species can also be easily added by implantation techniques for particular applications. The relative amount of polymer formation species in the implanted hard mask layer **12** may typically match those expected polymers formed in the subsequent plasma etching of the hard mask layer **12** and the substrate material **10** for most efficient polymer formation. In the case of a wet etching process, the parameters of the ion implant process may be similarly optimized as those described immediately above to obtain the most efficient reduction of the etch rate for various etchants that are used in such wet etching process. As mentioned above, during the wet etching process, the etch-inhibiting species (C, F, N, etc.) in the implant regions **16**A will tend to act with the radicals in the chemical bath to form a thin protective interfacial layer on the surface of the implant regions **16**A that will tend to reduce the etch rate of the hard mask layer **12** that contain or are very near the implant regions **16**A. As the chemistry, science and plasma etching technology progresses, the etch-inhibiting species will likely not be limited to the illustrative one specifically discussed herein (e.g., C, F, and N). Rather, additional etch-inhibiting species, such as Cl, B, P, As, O, S, H, etc., may be employed depending upon a variety of factors, such as, for example, the specific materials involved, the specific radicals or ions present in the wet or plasma etch chemistry, etc.

FIG. **1**C depicts the device **100** after several process operations have been performed. First, the patterned implant mask **14** was removed by performing, for example, an oxygen-plasma ashing process. Next, the layer of hard mask material **12** is exposed to an etching process **18** to thereby define a patterned layer of hard mask material **12**A. As noted above, the etching process **18** may be either a wet etching process or a dry, plasma-based etching process. In one illustrative embodiment, where the etching process **18** is a dry, plasma-based etching process, the process gases used in the dry, plasma-based etching process **18** may include $C_4F_8/CH_2F_2/Ar$, $C_4F_6/Co/Ar$, C_4F_6, or C_SF_B based, etc., and an additive gas of nitrogen (N_2). The process parameters of such an illustrative dry, plasma-based etching process **18** (i.e., gas flow ratio, N_2 additive, chamber pressure, temperature, RF power, etc.) determine the sidewall profile, etching rate at vertical/horizontal (isotropic vs anisotropic) directions, the rate of polymer formation and removal rates. Typical operating parameters of such a dry plasma-based etching process **18** may be pressures in the range of 20 mTorr-10 Torr, gas flow rates in the range of 1-100 sccm, chamber temperatures in the range of 20-200° C., and RF power settings in the range of 100-1 kW with multiple frequencies. As noted above, during the dry plasma-based etching process **18**, the "polymer-forming" species in the implant regions **16**A serve as seeding sites for adsorption (or deposition) of polymer radicals (not shown), e.g., C—F polymer material on the surface of the implant regions **16**A. The larger chemical bond formation energy of C—F bonding (e.g., about 525 kJ/mol) favors the formation of C—F bonds than other chemical bonds during the illustrative dry plasma-based etching process **18**. Once the surface of the implant regions **16**A is covered with the polymer material, the carbon (C) and fluorine (F) radicals in the plasma will perform both adsorption (deposition) or de-sorption (etching) actions dynamically. If deposition rate is faster than the de-sorption rate, then polymer will accumulate on the surface; if the deposition rate is less than the adsorption rate, no polymer material will form on the surface of the hard mask layer **12** and such regions are thus exposed to the plasma etching process. The presence of the polymer material effectively reduces the etch rate of those portions of the hard mask material **12** where the implant regions **16**A are formed. As a result, the portions of the layer of hard mask material **12** that do not have the implant regions **16**A formed therein, i.e., the portions of the layer of hard mask material **12** that are not "covered" by the implant regions **16**A, may be readily removed during the etching process **18**.

In the case, where the etching process **18** is a wet etching process and the hard mask layer is made of silicon nitride, the wet etching process may be performed using phosphorous acid (H_3PO_4) with additives for etching silicon nitride. As is well-known, the additives (or "buffer" agents) added to a wet etching bath are primarily used to stabilize the active etchants and to achieve an approximately constant etch rate. The additives for stabilizing H_3PO_4 are usually HF, acetic acid, (thus containing F and C radicals in solution) with a concentration of a few percent (in volume). The parameters of the wet etching process **18**, such as temperature, chemical concentration, buffer agents, and duration, may vary depending upon the particular application. In one illustrative embodiment, where the hard mask layer **12** is comprised of silicon nitride, the wet etching process **18** may be performed using buffered phosphorous acid (H_3PO_4) as the etchants and the wet etching process **18** may be performed at a temperature of about 25-150° C. If the hard mask layer **12** is comprised of silicon dioxide, then the wet etching process **18** may performed by using HF solutions (diluted and/or buffered).

After the patterned hard mask layer **12**A is formed, as shown in FIG. **1**D, an etching process **20**, e.g., a wet or dry (plasma-based) etching process may be performed on the structure layer **10** through the patterned hard mask layer **12**A. In the example depicted in FIG. **1**D, the etching process **20** defines a plurality of trench-type features **20**A in the structure layer **10**. Of course, the patterned hard mask layer **12**A may be employed to define any type of feature, e.g., line-type features, hole-type features, vias, etc. In the case where the etching process **18** is a dry plasma-based etching process, the polymer material that was formed during the dry plasma-based etching process **18** may be left in place during the etching process **20** or it may be removed prior to performing the etching process **20**. For example, prior to performing the etching process **20**, the polymer material may be removed by subjecting the device to a wet HF acid cleaning process. Similarly, in the case where the etching process **18** is a wet etching process, the protective interfacial layer that is formed on the certain surface portions of the hard mask layer **12**, i.e., in the areas near the implant regions **16**A, it may be left in place during the etching process **20** or it may be removed prior to performing the etching process **20**. For example, prior to performing the etching process **20**, the protective interfacial layer may be removed by subjecting the device to a DI water rinse or diluted acid cleaning process at elevated temperatures. Note that etching processes **18** and **20** can be performed sequentially in one chamber by using both dry (plasma) etching or both wet etching steps. Also, the profile of the feature etched in the structure **10** is entirely determined by the nature of etching process **20** (e.g., an isotropic or anisotropic etching process), while the etch-inhibiting species in implant regions **16**A only protects the hard mask material **16** from consumption.

Interestingly, in the case where the etching process **18** is a dry plasma-based etching process, the substantially continuous generation of polymer material during the dry plasma-based etching process **18** prevents any substantial consumption of the hard mask layer **12**. That is, unlike prior art hard mask layers and photoresist masking layers that would be consumed to a substantial degree, if not entirely, the polymer formation described herein effectively prevents or reduces a substantial consumption of the hard mask layer **12** where the polymer material is formed. Thus, if desired, the hard mask layer **12** can be very thin (or simply skipped) and still can serve as an effective etch mask.

Moreover, with reference to FIGS. **1**E (plan view) and **1**F (cross-sectional view), in some cases, an ion implantation etch mask **16**M comprised of one or more implant regions **16**A may be formed in the structure **10** so as to define non-implant regions **10**E of the structure **10** that are desired to be etched. Thereafter, an etching process may be performed to define various features in the structure **10**. That is, using the methods disclosed herein, various features may be directly formed in the structure **10**, e.g., a plurality of trenches, without having to form a separate etch mask, such as a patterned hard mask or an etch mask made of photoresist material above the structure **10**. For example, as shown in FIG. **1**E, the ion implant process **16** may be performed to form various implant regions **16**A, i.e., the ion implantation mask **16**M, in the structure **10**. The implantation mask **16**M (that is comprised of one or more implant regions **16**A) effectively defines the non-implant regions **10**E of the structure **10** that are to be etched. In the example depicted in FIG. **1**E, where the structure **10** is a semiconducting substrate, the etch mask **16**M may define a portion of the non-implant regions **10**E of the substrate where a shallow trench isolation (STI) region **103** will be formed as well as non-implant regions **10**E of the substrate that will be etched to thereby form a plurality of fins **105** for a FinFET device. As shown in FIG. **1**F, one or more etching processes may be performed through the implant etch mask **16**M to define various trenches **55** in the substrate that define in whole or part the isolation structure **103** and the fins **105**. Of course, those skilled in the art will recognize that additional operations need to be performed to complete the fabrication of the isolation structure **103** (e.g., fill with insulating material and polish) and the rest of steps to complete the FinFET device. Due to the formation of the polymer material during a dry plasma-based etching process, the portions of the substrate where the implant regions **16**A are formed are effectively protected from the etching process. Stated another way, if the implant regions **16**A are formed directly in the structure **10**, then the polymer will also be formed on the surface of the structure **10** where those implant regions **16**A are located and thereby act as a patterned etch mask comprised of a plurality of spaced-apart implant regions **16**A (that contain the implanted etch-inhibiting species) during the subsequent etching of structure material **10**. In effect, the processes described herein result in a patterned etch mask comprised of a plurality of spaced-apart implant regions **16**A, and the structure **10** may be patterned without requiring the formation of a separate patterned layer of hard mask material that acts as an etch mask above the structure **10**. Rather, in the case where a patterned etch mask comprised of a plurality of spaced-apart implant regions **16**A is formed in the structure **10**, the structure **10** may be patterned by subjecting the entirety of the structure **10** to the etching process and without the need of going through the process complexity and expense of forming a separate patterned etch mask layer above the structure **10**. Of course, as noted above, the structure **10** is generic in nature, as it may be, for example, a semiconducting substrate, a layer of insulating material, etc., and a variety of different features may be defined in the structure **10**, such as the aforementioned isolation structure **103**, fins **105**, trenches for metal wiring lines, etc. Similarly, due to the formation of the protective interfacial layer during a wet etching process, the regions of the structure **10** where the implant regions **16**A are formed are effectively protected from the wet etching process.

FIGS. **2**A-**2**G depict various illustrative methods disclosed herein for forming self-aligned contacts for an integrated circuit product. FIG. **2**A is a schematic depiction of a device **100** that includes a plurality of illustrative transistors **33**. Each of the transistors **33** is formed in an active area of a semiconducting substrate **101**. Of course, in a real-world product, there may be millions or thousands of such transistors **33** on the device **100**. The substrate **101** may have a variety of configurations, such as the depicted bulk silicon configuration. The substrate **101** may also have a silicon-on-insulator (SOI) configuration that includes a bulk silicon layer, a buried insulation layer and an active layer, wherein semiconductor devices are formed in and above the active layer. Thus, the terms substrate or semiconductor substrate should be understood to cover all forms of semiconductor structures. The substrate **101** may also be made of materials other than silicon.

FIG. **2**A depicts the device **100** at a point in fabrication wherein source/drain regions (not shown) have been formed in the substrate **101** between the transistors **33** and the next major activity to be performed involves the formation of conductive contact structures and metal silicide regions in the source/drain regions of the device **100**. Each of the transistors **33** may be N-type transistors or P-type transistors, or one may be an N-type transistor and a P-type transistor. In one example, the transistors may have basically the same configuration. The transistors **33** each comprise a schematically depicted gate structure **30** (comprised of a gate insulation layer **30**A, one or more conductive gate electrode layers **30**B) and a gate cap layer **31**, made of a material such as silicon nitride, and sidewall spacers **32**, made of a material such as silicon nitride.

The gate structures **30** depicted herein are intended to be schematic and representative in nature, as the materials of construction used in the gate structures for one of the transistors **33**, e.g., an N-type transistor, may be different than the gate structure **30** for the other transistor, e.g., a P-type transistor, which may have multiple layers of conductive metal, etc. However, in some applications, the gate structures **30** may be comprised of the same basic materials, e.g., both of the gate structures **30** may comprise a silicon dioxide gate insulation layer **30**A and a polysilicon gate electrode **30**B. In general, the gate insulation layer **30**A may be comprised of a variety of materials, such as silicon dioxide, silicon oxynitride, a high-k (k value greater than 10) insulating material. The gate electrode **30**B may be comprised of one or more layers of conductive materials, such as polysilicon, a metal (aluminum or tungsten), a metal nitride or carbide (e.g., TaN, TaC, TiC, TiN), etc. The gate structures **30** depicted in FIG. **2**A may be formed by performing a variety of known techniques. For example, the layers of material that make up the illustrative gate insulation layer **30**A, the gate electrode **30**B and the gate cap layer **31** may be blanket-deposited above the substrate **101** and, thereafter, one or more etching process are performed through a patterned mask layer (not shown) to define the basic gate structures **30** and the gate cap layer **31** depicted in FIG. **2**A. Moreover, the gate insulation layers and gate electrodes in the gate structures **30** may be the final gate insulation layers and gate electrodes to be used on the pro-

duction device or they may be sacrificial structures that may be later removed and replaced with final gate insulation layers and gate electrodes for the finished device using well-known "replacement gate" (RMG) formation techniques. That is, the gate structures **30** may be sacrificial gate structures or final gate structures as it relates to the formation of the finished device. The sidewall spacers **32** may be formed by performing a conformable deposition process to form a layer of spacer material above the device **100** and thereafter performing an anisotropic etching process. Moreover, as will be appreciated by one skilled in the art after having read the present application, the methods disclosed in FIGS. **2**A-**2**G may be employed on planar field effect transistor devices as well as on three dimensional devices such as FinFET devices.

Next, as shown in FIG. **2**B, an etch stop layer **34** is conformably deposited above the device **100**. The etch stop layer **34** may be comprised of a variety of different materials, e.g., silicon nitride, silicon oxynitride, etc., its thickness may vary depending upon the particular application, e.g., 20-100 nm, and it may be formed by a variety of techniques, e.g., chemical vapor deposition (CVD), atomic layer deposition (ALD), etc. In one illustrative embodiment, the etch stop layer **34** may be a layer of silicon nitride that has a thickness of about 30 nm that was formed by performing a CVD process.

Then, as shown in FIG. **2**C, a plurality of angle implant processes **40** is performed to implant schematically depicted etch-inhibiting species **40**A into portions of the etch stop layer **34**. The etch-inhibiting species employed and parameters of the implant process **40** may be the same as those described previously for the implant process **16**. The implant process **40** is performed at a relatively high implant angle **42** to insure that the etch-inhibiting species **40**A are not implanted into the entirety of the etch stop layer **34**. More specifically, the implant angle **42** is selected such that, due to the shadowing effects of the adjacent transistor, the etch-inhibiting species **40**A will not be implanted into the etch stop layer **34** in the level or region defined by the vertical height **44**. The magnitude of the dimension **44** may vary depending upon the particular application and the thickness of the etch stop layer **34** in the device under construction. For example, the gate pitch, the height **46** of the gate structure **30**, and the selection of the implant angle **42** will have an impact on the amount of shadowing from adjacent structures during the implant process **40**. In one illustrative embodiment, the implant angle **42** may fall within the range of about 20-60° (relative to the vertical), and the distance **44** may be about 30% of the height **46** of the gate structure **30** of the transistors **33** or slightly thicker than the etch stop layer **34**. In one illustrative example, the dimension **44** may be about 20 nm above the etch stop layer **34**, e.g., the dimension **44** may fall within the range of about 20 to 50 nm.

Stated another way, the angled implant process **40** is performed at an angle **42** such that one of the transistors prevents the implantation of the etch-inhibiting species **40**A into the entirety of the etch stop layer **34** positioned proximate a side of the other of the transistors **33**. Stated yet another way, the angled implant process **40** is performed at an angle **42** such that a portion of the etch stop layer **34** between the two transistors is not implanted with the etch-inhibiting species **40**A. In another embodiment, the angled implant process **40** is performed at an angle **42** such that portions of the etch stop layer **34** within the vertical distance **44** of the surface of the substrate **101** that corresponds to approximately 30% of a gate height **46** of one of the gate structures of the transistors **33** is not implanted with the "etch-inhibiting" species **40**A. In yet another embodiment, the angled implant process **40** is performed at an angle **42** such that only portions of the etch stop layer **34** that are positioned a vertical distance above the surface of the substrate **101** that is greater than a distance that corresponds to approximately 30% of a gate height **46** of one of the gate structures **30** is implanted with the etch-inhibiting species **40**A.

Of course, as will be appreciated by those skilled in the art, the angled implant process **40** can be a two-twist implantation process wherein a first part of the implant process **40** is performed to implant the etch-inhibiting species **40**A into the etch stop layer **34** on a first side of the transistors **33** and, thereafter, the substrate **101** is rotated 180° and a second part of the implant process **40** is performed to introduce the etch-inhibiting species **40**A into the etch stop layer **34** on the other side of the transistors **33**. As it relates to implantation angles discussed and claimed herein, all angles are described relative to a vertical axis. Depending upon the specific application, the angled implant process **40** can be performed with multiple twists, e.g., 3, 4 or more, with corresponding substrate rotation angles of 120°, 90°, etc.

The next sequence of process operations involves the formation of self-aligned contacts to the source/drain regions of the transistors **33**. In one illustrative process flow, as shown in FIG. **2**D, the process begins with the formation of a layer of insulating material **50** above the device **100** and the formation of a patterned etch mask **52** above the layer of insulation material **50**. In general, the layer of insulating material **50** may be comprised of a variety of materials, such as silicon dioxide, a low-k (k value less than 3.5) insulating material, and it may be formed by a variety of techniques, e.g., CVD, ALD, etc. In one illustrative embodiment, the layer of insulating material **50** may be a layer of silicon dioxide that was formed by performing a CVD process. The layer of insulation material **50** may be deposited by performing a conformal deposition process, and it is often planarized by performing a chemical-mechanical-polishing (CMP) process (as shown in FIG. **2**D). The patterned etch mask **52** exposes portions of the layer of insulating material **50** for further processing. In one illustrative embodiment, the patterned etch mask **52** is a patterned layer of photoresist material that was formed using traditional photolithography tools and techniques. The patterned etch mask **52** may also be a hard mask layer, e.g., a layer of metal.

Next, as shown in FIG. **2**E, an etching process **54**, e.g., a wet or dry etching process, may be performed on the layer of insulating material **50** through the patterned etch mask **52**. The etching process **54** is typically performed with an etch chemistry that is selective relative to the etch stop layer **34**. In the example depicted in FIG. **2**E, the etching process **54** defines a plurality of trench-type or hole-type features **50**A in the layer of insulating material **50** which exposes portions of the etch stop layer **34** for further processing.

Then, as shown in FIG. **2**F, an etching process **60**, e.g., a wet or dry (plasma-based) etching process, may be performed on the portions of the etch stop layer **34** that are exposed by the openings **50**A in the layer of insulating material **50**. In one embodiment, the etching process **60** may be either a wet or dry etching process that is performed using the same parameters as discussed above with respect to the etching process **18**. If desired, the etch mask **52** may be left in place during the etching process **60** or it may be removed prior to performing the etching process **60**. The etching process **60** is typically performed with an etch chemistry that is selective relative to the substrate material. In the example depicted in FIG. **2**F, the etching process **60** defines a plurality of trench-type or hole-type features **34**A in the etch stop layer **34** that exposes portion of the source/drain regions (not shown) that are formed in the substrate **101**. As discussed above with respect

to the discussion of polymer formation during the case where the etching process **18** was a dry plasma-based etching process, during the dry plasma-based etching process **60**, the implanted etch-inhibiting species **40**A serve as seeding sites for forming polymer material (not shown), e.g., C—F polymer material, on the surface of the etch stop layer **34** where the implanted etch-inhibiting species **40**A are located. As noted previously, once the surfaces of the etch stop layer **34** where the implanted etch-inhibiting species **40**A are located is covered with the polymer material, the carbon (C) and fluorine (F) radicals in the plasma during the dry, plasma-based etch process **60** will perform both adsorption (deposition) or de-sorption (etching) dynamically. The presence of the polymer material effectively reduces the etch rate of those portions of the etch stop layer **34** where the polymer material is present. However, since the etch-inhibiting species **40**A were not implanted into the lower regions of the etch stop layer **34**, e.g., the region within the vertical dimension **44** shown in FIG. **2**C, the portions of the etch stop layer **34** where such etch-inhibiting species **40**A are not present will etch at a faster rate. Thus, the openings **34**A may be formed in the lower portion of etch stop layer **34** while the polymer material formed on the portions of the etch stop layer **34** where the etch-inhibiting species **40**A are present insures that the gate structures of the device are protected during the contact formation process. The statements above regarding the situation where the etching process **18** is a wet etching process apply equally to this situation where the etching process **60** is a wet etching process.

Next, as shown in FIG. **2**G, metal silicide regions **35** are formed in the source/drain regions of the device **100** and a plurality of conductive self-aligned contacts **62** are formed in the openings **50**A in the layer of insulating material **50**. In general, the metal silicide regions **35** are typically formed in the source/drain regions of a transistor to reduce the resistance when a conductive contact is formed to establish electrical connection to the source/drain regions. The metal silicide regions **35** depicted herein may be made using a variety of different refractory metals, e.g., nickel, platinum, cobalt, titanium, etc., or combinations thereof, and they may be formed using techniques that are well known to those skilled in the art. The typical steps performed to form metal silicide regions are: (1) depositing a layer of refractory metal; (2) performing an initial heating process causing the refractory metal to react with underlying silicon containing material; (3) performing an etching process to remove unreacted portions of the layer of refractory metal; and (4) performing an additional heating process to form the final phase of the metal silicide. The details of such silicidation processes are well known to those skilled in the art. Next, the self-aligned contacts **62** are formed in the openings **50**A using traditional techniques. In some cases, a relatively thin layer of barrier material (e.g., TaN, TiN) may be formed in the openings **50**A, although such a barrier layer is not depicted in the drawings. The self-aligned contact **62** may be comprised of a variety of conductive materials, e.g., Ti, TiN, tungsten, aluminum, copper, etc., and it may be form by depositing the material in the contact opening **50**A using, for example, a PVD process, a CVD process, an electroplating process (ECP) and thereafter performing one or more CMP processes to remove excess portions of the conductive material positioned outside of the contact opening **50**A.

FIGS. **3**A-**3**J depict various specific methods disclosed herein for forming self-aligned contacts for an integrated circuit product wherein a "gate-last" or a replacement metal gate technique (RMG) is employed. FIG. **3**A depicts the device at a point wherein the etch-inhibiting species **40**A have been implanted into the etch stop layer **34** as previously described. In this illustrative embodiment, the gate structures **30** of the transistors **33** are sacrificial in nature as they will ultimately be replaced with final gate structures using a so-called "gate-last" technique. Moreover, as will be appreciated by one skilled in the art after having read the present application, the methods disclosed in FIGS. **3**A-**3**J may be employed on planar field effect transistor devices as well as on three dimensional devices such as FinFET devices.

As shown in FIG. **3**B, a layer of insulating material **70** is formed above the device **100**. If desired or necessary, a CMP process may be performed on the layer of insulating material **70** to planarize its upper surface. The layer of insulating material **70** may be comprised of a variety of materials, such as silicon dioxide, a low-k (k value less than 3.5) insulating material, and it may be formed by a variety of techniques, e.g., CVD, ALD, etc. In one illustrative embodiment, the layer of insulating material **70** may be a layer of silicon dioxide that was formed by performing a CVD process.

Next, as shown in FIG. **3**C one or more CMP processes are performed to remove portions of the layer of insulating material **70**, the etch stop layer **34** and the gate cap layer **31**. The process results in the exposure of the gate structure **30** (more specifically the gate electrode **30**B) for further processing.

Then, as shown in FIG. **3**D, one or more etching processes are performed to remove the sacrificial gate electrode **30**B and the sacrificial gate insulation layer **30**A to thereby define a gate cavity **75** where a replacement gate structure will subsequently be formed. Typically, the sacrificial gate insulation layer **30**A is removed as part of the replacement gate technique, as depicted herein. However, the sacrificial gate insulation layer **30**A may also be left in place in some applications.

Next, as shown in FIG. **3**E, schematically depicted replacement gate structures **80** are formed in the gate cavities **75**. In one illustrative example, the replacement gate structure **80** is comprised of a high-k gate insulation layer (not shown) having a work-function adjusting layer (not shown) comprised of a metal (e.g., a layer of titanium nitride) and a bulk metal layer (not shown) (e.g., aluminum). Ultimately, as shown in FIG. **3**E, one or more CMP processes are performed to remove excess portions of the gate insulation layer, the work-function adjusting layer and the bulk metal layer positioned outside of the gate cavity **75** to define the replacement gate structure **80**. The replacement gate structure **80** depicted herein is intended to be representative in nature. That is, the replacement gate structure may be comprised of a variety of different materials. For example, the replacement gate structure **80** may include a high-k gate insulation layer that is made of tantalum oxide (Ta_2O_5), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), titanium oxide (TiO_2), aluminum oxide (Al_2O_3), hafnium silicates ($HfSiO_x$), or the like. Furthermore, one or more non-polysilicon metal gate electrode materials may be part of the replacement gate structure. These metal gate electrode materials may include, for example, one or more layers of titanium (Ti), titanium nitride (TiN), titanium-aluminum (TiAl), titanium carbide (TiC), aluminum (Al), aluminum nitride (AlN), tantalum (Ta), tantalum nitride (TaN), tantalum carbide (TaC), tantalum carbonitride (TaCN), tantalum silicon nitride (TaSiN), tantalum silicide (TaSi), and the like.

Next, as shown in FIG. **3**F, a layer of hard mask material **82** is formed above the device **100** and the replacement gate structures **80**. The layer of hard mask material **82** may comprised of a variety of different materials, e.g., silicon nitride, silicon dioxide, etc., its thickness may vary depending upon the particular application, e.g., less than 100 nm, and it may be formed by a variety of techniques, e.g., CVD, ALD, etc. In

one illustrative embodiment, the layer of hard mask material **82** may be a layer of silicon nitride that has a thickness of about 30 nm that was formed by performing a CVD process. Also depicted in FIG. **3**F is an illustrative patterned implant mask **84** that is patterned to expose portions of the layer of hard mask material **82** for further processing. In one illustrative embodiment, the patterned implant mask **84** is a patterned layer of photoresist material that was formed using traditional photolithography tools and techniques.

With continuing reference to FIG. **3**F, an ion implant process **90** is performed through the patterned implant mask **84** to implant schematically depicted etch-inhibiting species **90**A into portions of the layer of hard mask material **82**. The species employed and parameters of the implant process **90** may be the same as those described previously for the implant process **16** or the implant process **40** (using a zero implant angle).

Next, as shown in FIG. **3**G, the patterned implant mask **84** is removed and a wet or dry (plasma-based) etching process **92**, e.g., a fluorine (F) based plasma etching process, may be performed on the entirety of the layer of hard mask material **82** to thereby define a patterned layer of hard mask material **82**A. In one embodiment, the etching process **92** may be performed using the same parameters as discussed above with respect to the etching processes **18** or **60**. As noted above, in the case where the etching process **92** is a dry plasma-based process, the etch-inhibiting species **90**A in the implant regions of the hard mask layer **82** serve as seeding sites for forming polymer material (not shown), e.g., C—F polymer material, on the surface of the hard mask layer **82**. As a result, the portions of the layer of hard mask material **82** that do not have the implanted etch-inhibiting species **90**A may be readily removed during the etching process **92**. In effect, the processes described herein result in the creation of an in situ patterned hard mask layer **82**A in the sense that the patterned hard mask layer **82**A is formed by exposing all of the layer of hard mask material **82** to the etching process **92**. The statements above regarding the situation where the etching process **18** is a wet etching process apply equally to this situation where the etching process **92** is a wet etching process.

With reference to FIGS. **3**H-**3**J, the next sequence of operations involves the formation of the conductive self-aligned contacts **62** and metal silicide regions **35** for the device **100**. More specifically, in FIG. **3**H, an etching process **93**, e.g., a wet or dry etching process, may be performed on the layer of insulating material **70** through the patterned hard mask **82**A. The etching process **93** is typically performed with an etch chemistry that is selective relative to the etch stop layer **34** and the patterned hard mask **82**A. The etching process **93** results in the structure depicted in FIG. **3**H wherein a plurality of trench-type or hole-type features **70**A in the layer of insulating material **70** which exposes portions of the etch stop layer **34** for further processing.

Then, as shown in FIG. **3**I, a wet or dry (plasma-based) etching process **94**, e.g., a dry fluorine based plasma etching process, may be performed on the portions of the etch stop layer **34** that are exposed by the openings **70**A. In one embodiment, the etching process **94** may be performed using the same parameters as discussed above with respect to the etching processes **18** or **60**. The etching process **94** is typically performed with an etch chemistry that is selective relative to the substrate material. In the example depicted in FIG. **3**I, the etching process **94** defines a plurality of trench-type or hole-type features **34**A in the etch stop layer **34** that exposes portions of the source/drain regions (not shown) that are formed in the substrate **101**. As discussed above with respect to the discussion of polymer formation, in the case where the etching process **94** is a dry plasma-based etching process, the implanted "etch-inhibiting" species **40**A, **90**A serve as seeding sites for forming polymer material (not shown), e.g., C—F polymer material, on the surface of the etch stop layer **34** and the patterned hard mask **82**A where the implanted etch-inhibiting species **40**A, **90**A are located. As noted previously, once the surfaces of the etch stop layer **34** and the patterned hard mask layer **82**A where the implanted etch-inhibiting species **40**A, **90**A are located are covered with the polymer material, the carbon (C) and fluorine (F) radicals in the plasma during the dry, plasma-based etching process **94** will perform both adsorption (deposition) or de-sorption (etching) dynamically. The presence of the polymer material effectively reduces the etch rate of those portions of the etch stop layer **34** and the patterned hard mask layer **82**A where the polymer material is present. However, since the etch-inhibiting species **40**A were not implanted into the lower regions of the etch stop layer **34**, e.g., the region within the vertical dimension **44** shown in FIG. **2**C, the portions of the etch stop layer **34** where such etch-inhibiting species **40**A are not present will etch at a faster rate. Thus, the openings **34**A may be formed in the lower portion of etch stop layer **34** while the polymer material formed on the portions of the etch stop layer **34** where the etch-inhibiting species **40**A are present (and where the etch-inhibiting species **90**A are present in the patterned hard mask layer **82**) insures that the gate structure of the device will be protected during the contact formation process. The statements above regarding the situation where the etching process **18** is a wet etching process apply equally to this situation where the etching process **94** is a wet etching process.

In one illustrative embodiment, where the etching processes **92**, **93**, and **94** are all dry plasma-based etching process, they may be performed in a sequential manner (with some tuning of the process parameters, such as gas flows, process time, RF power, etc.) in a chamber without breaking the vacuum. In one particularly extreme example, the thickness of hard mask material **82** may be reduced to approximately zero, and the etch-inhibiting species can be implanted to the top surface of the replacement gate electrode, and the etching process **92** may be omitted. Then, during the etching processes **93** and **94**, polymer material can still be formed on the top of replacement gate electrode as well as the upper portion of the spacer where the etch-inhibiting species are positioned. Such an etch mask that is defined by spaced-apart implant regions may be useful during the SAC formation process illustrated in FIG. **3**F to **3**I. Similarly, in case of all wet etching processes for etching processes **92**, **93**, and **94**, they may be performed in a sequential manner (with some tuning of the process parameters, such as gas flows, process time, RF power, etc.) in a wet etching chamber without exposing the wafers to the ambient environment. Similarly, the thickness of hard mask material **82** may be reduced to approximately zero, and the etch-inhibiting species may be implanted to the top surface of the replacement gate electrode, and the wet etching process **92** may be omitted.

Next, as shown in FIG. **3**J, metal silicide regions **35** are formed in the source/drain regions of the device **100** and a plurality of conductive self-aligned contacts **62** are formed in the openings **70**A as previously described.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than

as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

What is claimed:

1. A method, comprising:

forming gate structures for first and second spaced-apart transistors above a semiconducting substrate;

forming an etch stop layer above said substrate and said gate structures for said transistors;

performing at least one angled ion implant process to implant at least one etch-inhibiting species into less than an entirety of said etch stop layer, wherein performing said at least one angled ion implant process to implant said at least one etch-inhibiting species comprises performing a first ion implant process using one of carbon or fluorine and performing a second ion implant process using the other of said carbon or fluorine;

after performing said at least one angled ion implant process, forming a layer of insulating material above said etch stop layer;

performing at least one first etching process to define an opening in said layer of insulating material and thereby expose a portion of said etch stop layer;

performing a second etching process on said exposed portion of said etch stop layer to define a contact opening therethrough that exposes a doped region formed in said substrate; and

forming a conductive contact in said opening that is conductively coupled to said doped region.

2. The method of claim **1**, wherein performing said second etching process comprises performing a wet etching process or a dry plasma-based etching process.

3. The method of claim **1**, wherein said etch-inhibiting species is a polymer forming species and wherein performing said second etching process comprises performing a dry plasma-based etching process that causes formation of a polymer material proximate said at least one implant region.

4. The method of claim **1**, wherein performing said second etching process comprises performing a wet etching process that causes formation of a protective interfacial layer proximate said at least one implant region.

5. The method of claim **1**, wherein each of said first and second angled implant processes is performed at an angle such that said first transistor prevents the implantation of said at least one etch-inhibiting species into the entirety of the etch stop layer positioned proximate a side of said second transistor.

6. The method of claim **1**, wherein each of said first and second angled implant processes is performed at an angle such that a portion of said etch stop layer between said first and second transistors is not implanted with said etch-inhibiting species.

7. The method of claim **1**, wherein each of said first and second angled implant processes is performed at an angle such that portions of said etch stop layer within a vertical distance above a surface of said substrate that corresponds to approximately 30% of a gate height of one of said gate structures is not implanted with said etch-inhibiting species.

8. The method of claim **7**, wherein said vertical distance is about 40 nm or less.

9. The method of claim **1**, wherein each of said first and second angled implant processes is performed at an angle such that only portions of said etch stop layer that are positioned a vertical distance above a surface of said substrate that is greater than a distance that corresponds to approximately 30% of a gate height of one of said gate structures is implanted with said etch-inhibiting species.

10. The method of claim **1**, wherein each of said first and second angled ion implant processes is performed at an angle within the range of about 20-60 degrees relative to a vertical.

11. The method of claim **1**, wherein said gate structures are sacrificial gate structures.

12. The method of claim **1**, wherein said gate structures are final gate structures for said transistors.

13. The method of claim **1**, wherein said transistors are planar transistor devices.

14. The method of claim **1**, wherein said transistors are FinFET transistor devices.

15. A method, comprising:

forming gate structures for first and second spaced-apart transistors above a semiconducting substrate;

forming an etch stop layer above said substrate and said gate structures for said transistors;

performing at least one angled ion implant process to implant at least one polymer-forming species into less than an entirety of said etch stop layer, wherein performing said at least one angled ion implant process to implant said at least one polymer-forming species comprises performing a first ion implant process using one of carbon or fluorine and performing a second ion implant process using the other of said carbon or fluorine;

after performing said at least one angled ion implant process, forming a layer of insulating material above said etch stop layer;

performing at least one first etching process to define an opening in said layer of insulating material and thereby expose a portion of said etch stop layer;

performing at least one dry plasma-based etching process on said exposed portion of said etch stop layer to define a contact opening therethrough that exposes a doped region formed in said substrate; and

forming a conductive contact in said opening that is conductively coupled to said doped region.

16. The method of claim **15**, wherein forming said etch stop layer comprises performing a deposition process to form said etch stop layer comprised of silicon nitride or silicon dioxide.

17. The method of claim **15**, wherein the ratio of carbon to fluorine is about 1:2.

18. The method of claim **15**, wherein performing said dry plasma-based etching process on said etch stop layer comprises performing a carbon-fluorine based dry plasma etching process on said etch stop layer.

19. The method of claim **15**, wherein performing said dry plasma-based etching process comprises performing said dry plasma-based etching process using at least one of the following process gases: $C_4F_8/CH_2F_2/Ar$ or C_5F_8 and nitrogen.

20. The method of claim **15**, wherein each of said first and second angled implant processes is performed at an angle such that said first transistor prevents the implantation of said at least one polymer-forming species into the entirety of the etch stop layer positioned proximate a side of said second transistor.

21. The method of claim **15**, wherein each of said first and second angled implant processes is performed at an angle such that a portion of said etch stop layer between said first and second transistors is not implanted with said polymer-forming species.

22. The method of claim **15**, wherein each of said first and second angled implant processes is performed at an angle such that portions of said etch stop layer within a vertical distance above a surface of said substrate that corresponds to

approximately 30% of a gate height of one of said gate structures is not implanted with said polymer-forming species.

23. The method of claim **22**, wherein said vertical distance is about 40 nm or less.

24. The method of claim **15**, wherein each of said first and second angled implant processes is performed at an angle such that only portions of said etch stop layer that are positioned a vertical distance above a surface of said substrate that is greater than a distance that corresponds to approximately 30% of a gate height of one of said gate structures is implanted with said polymer-forming species.

25. The method of claim **22**, wherein each of said first and second angled ion implant processes is performed at an angle within the range of about 20-60 degrees relative to a vertical.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,741,723 B2
APPLICATION NO. : 13/455579
DATED : June 3, 2014
INVENTOR(S) : Min-Hwa Chi

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In claim 25, column 19, line 12, delete "claim 22" and insert therefor -- claim 24 --.

Signed and Sealed this
Fifth Day of August, 2014

Michelle K. Lee

Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office