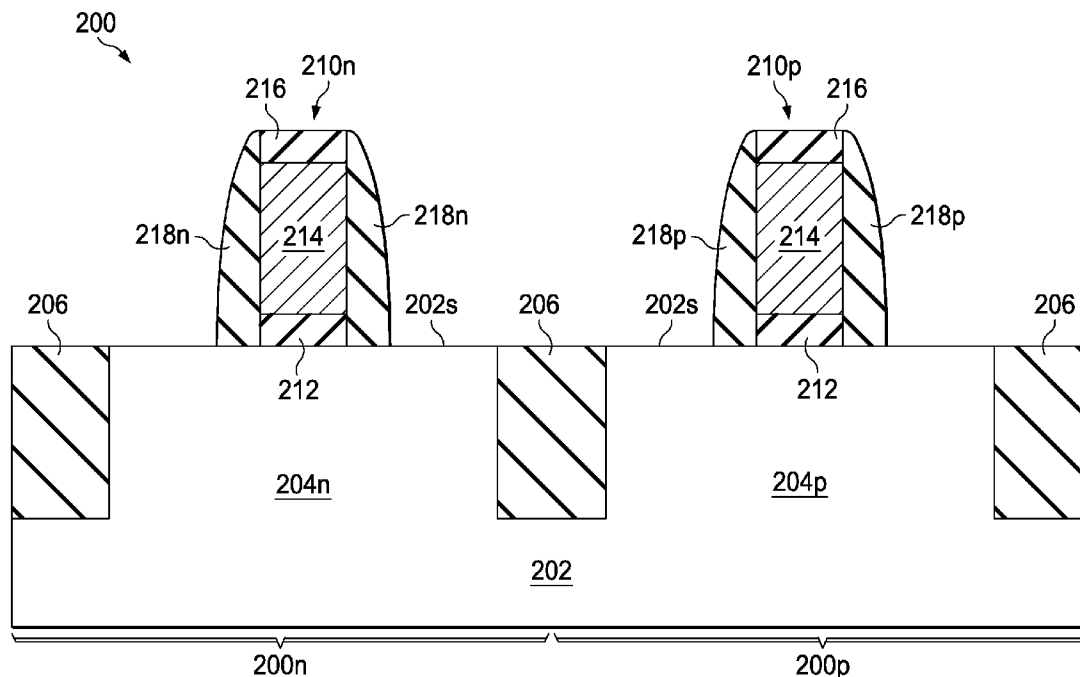




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USPC 257/369; 438/478; 257/E21.09; 257/E27.062



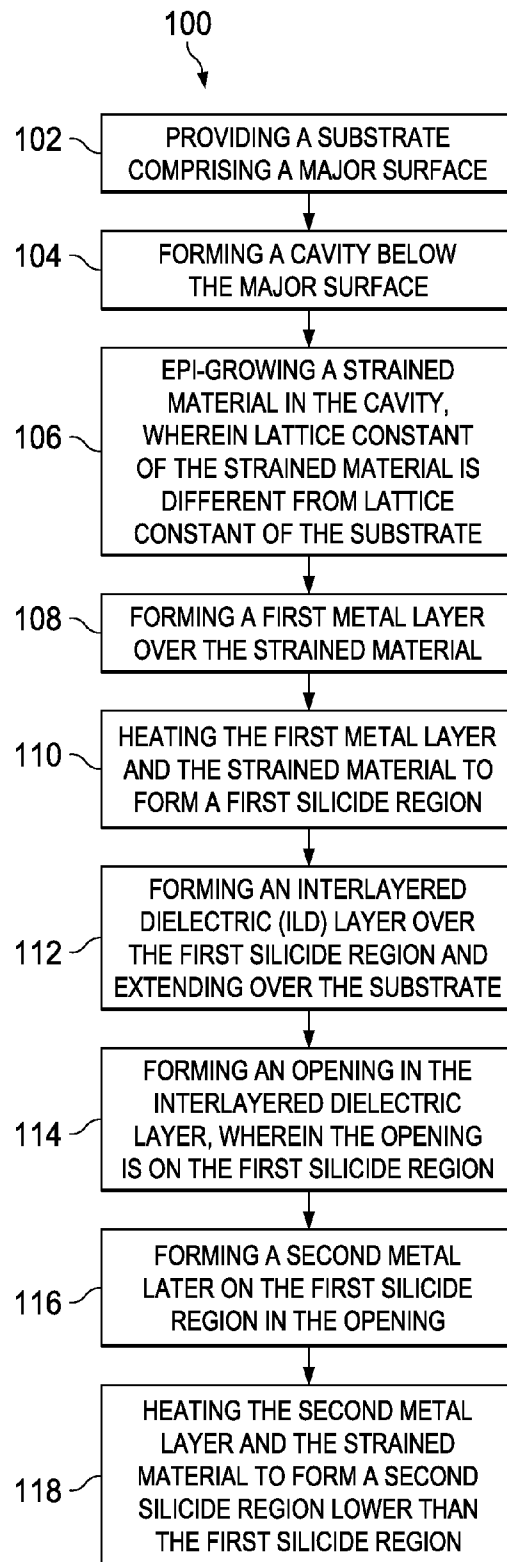


FIG. 1

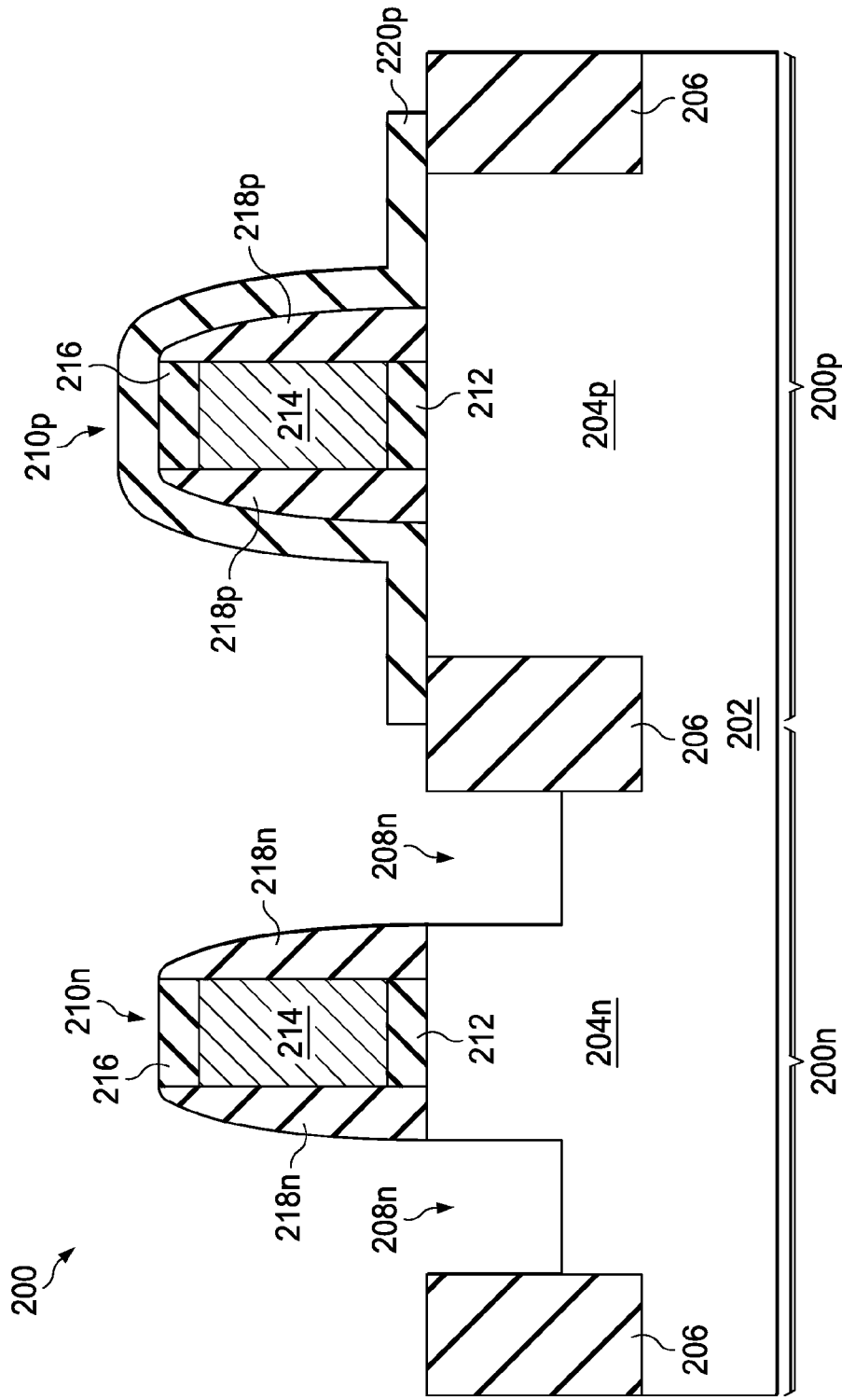


FIG. 3

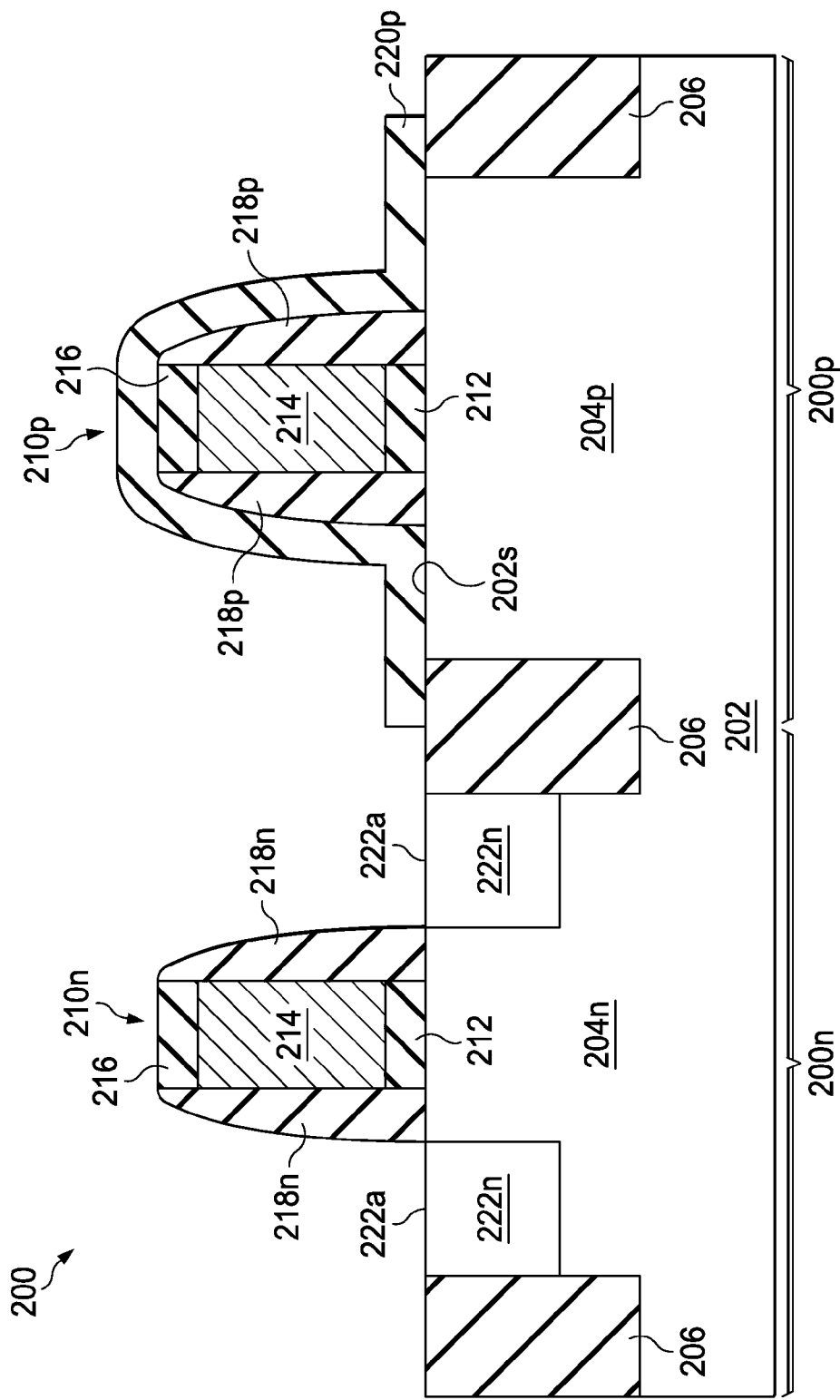


FIG. 4

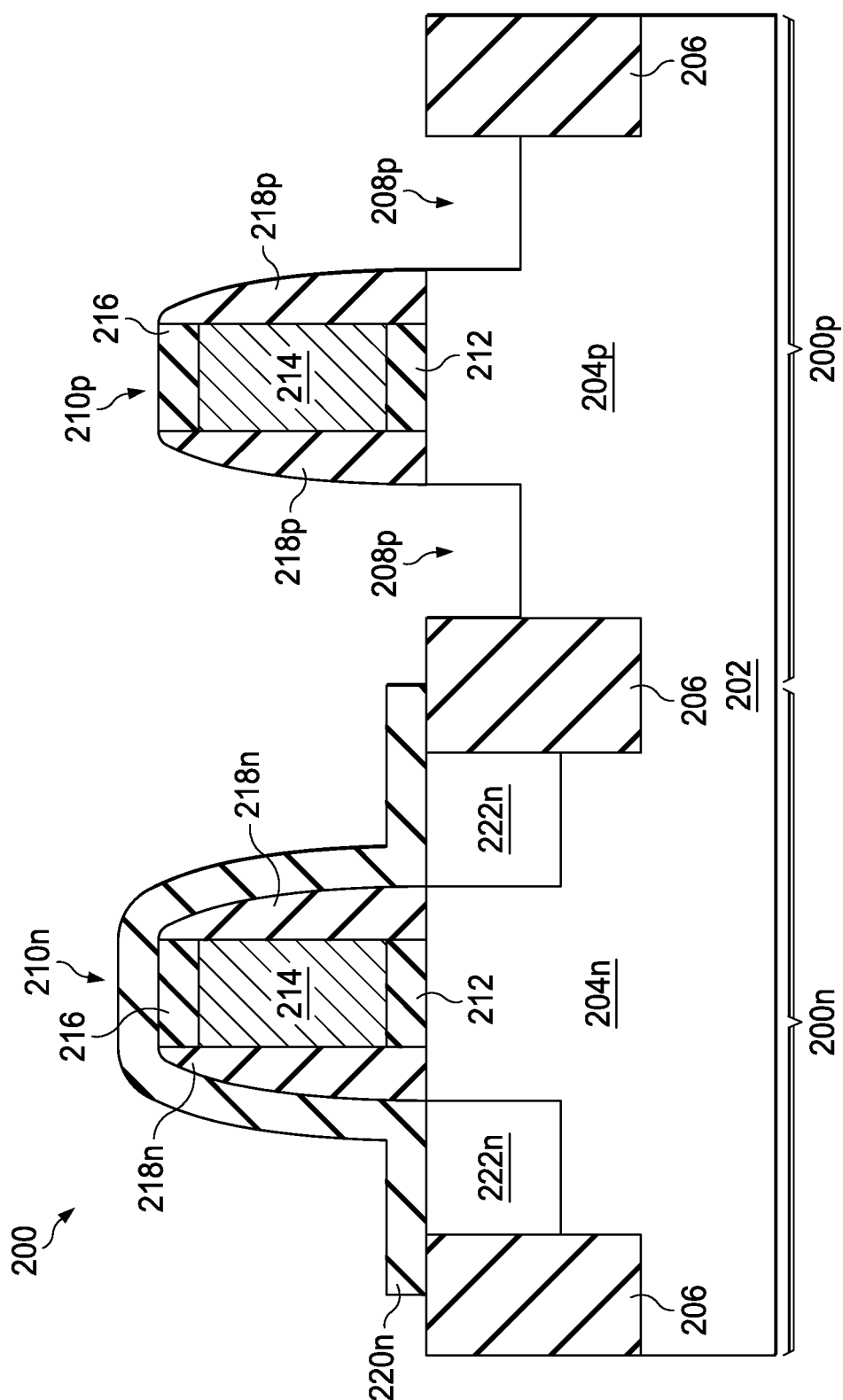


FIG. 5

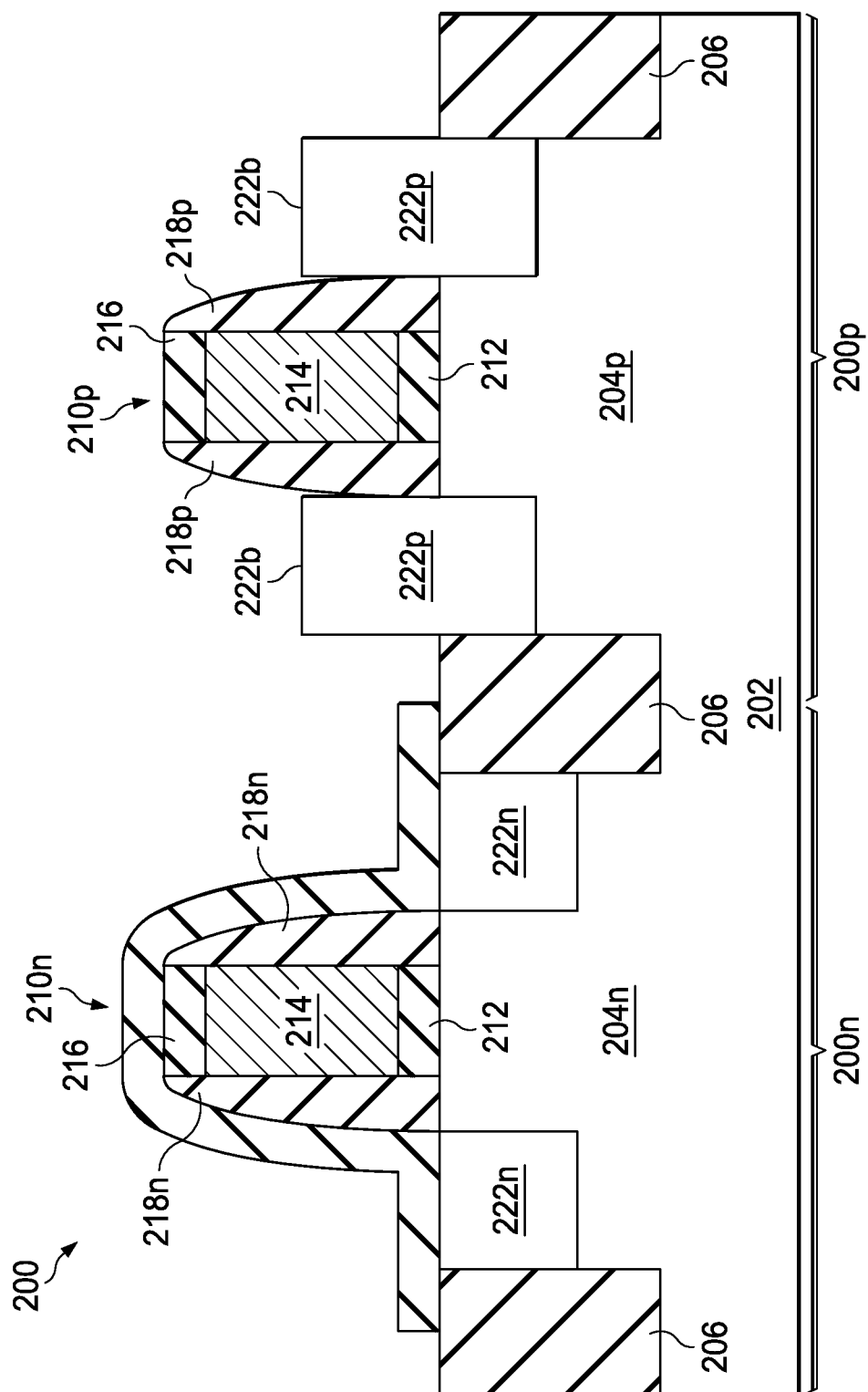


FIG. 6

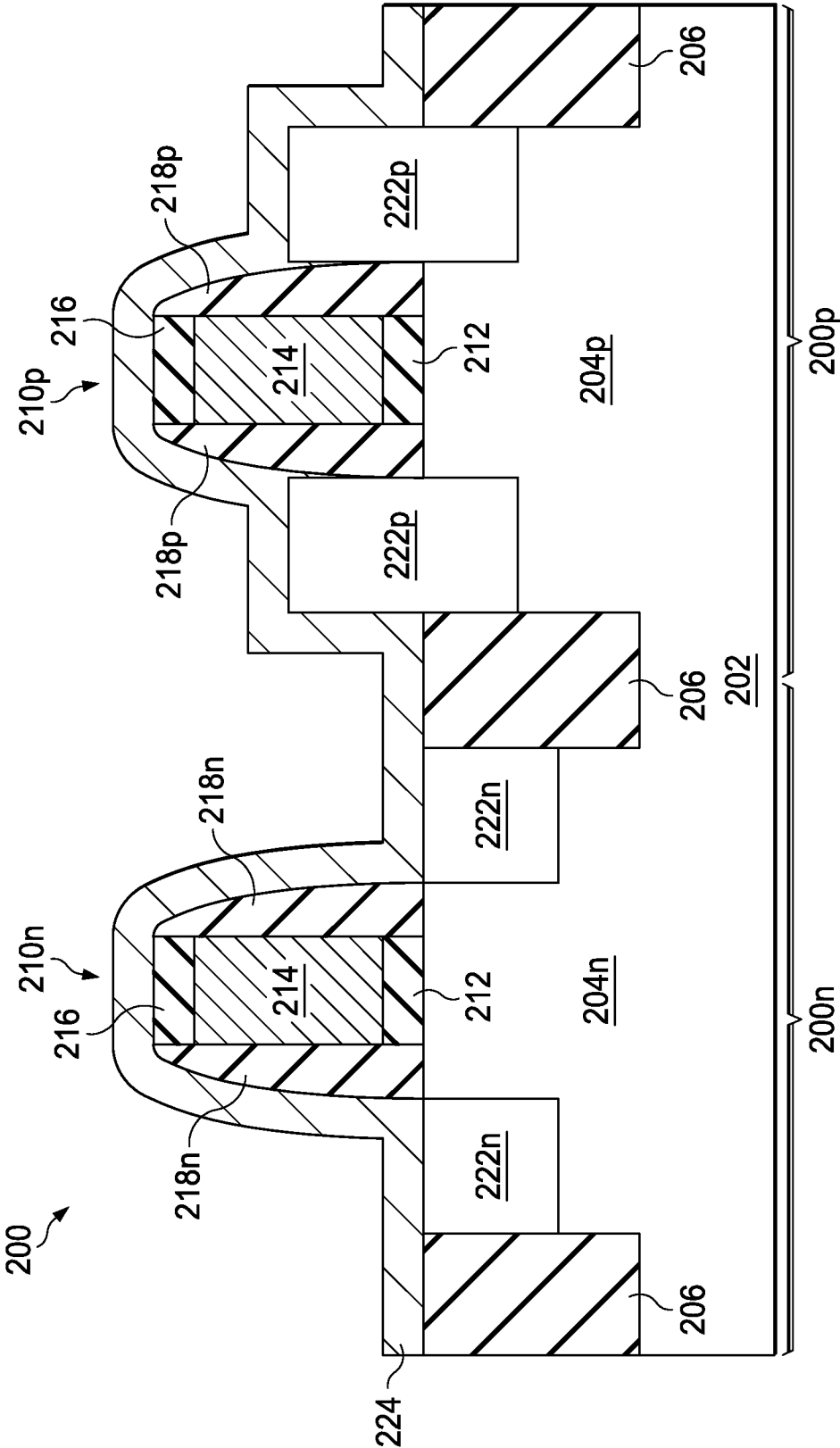


FIG. 7

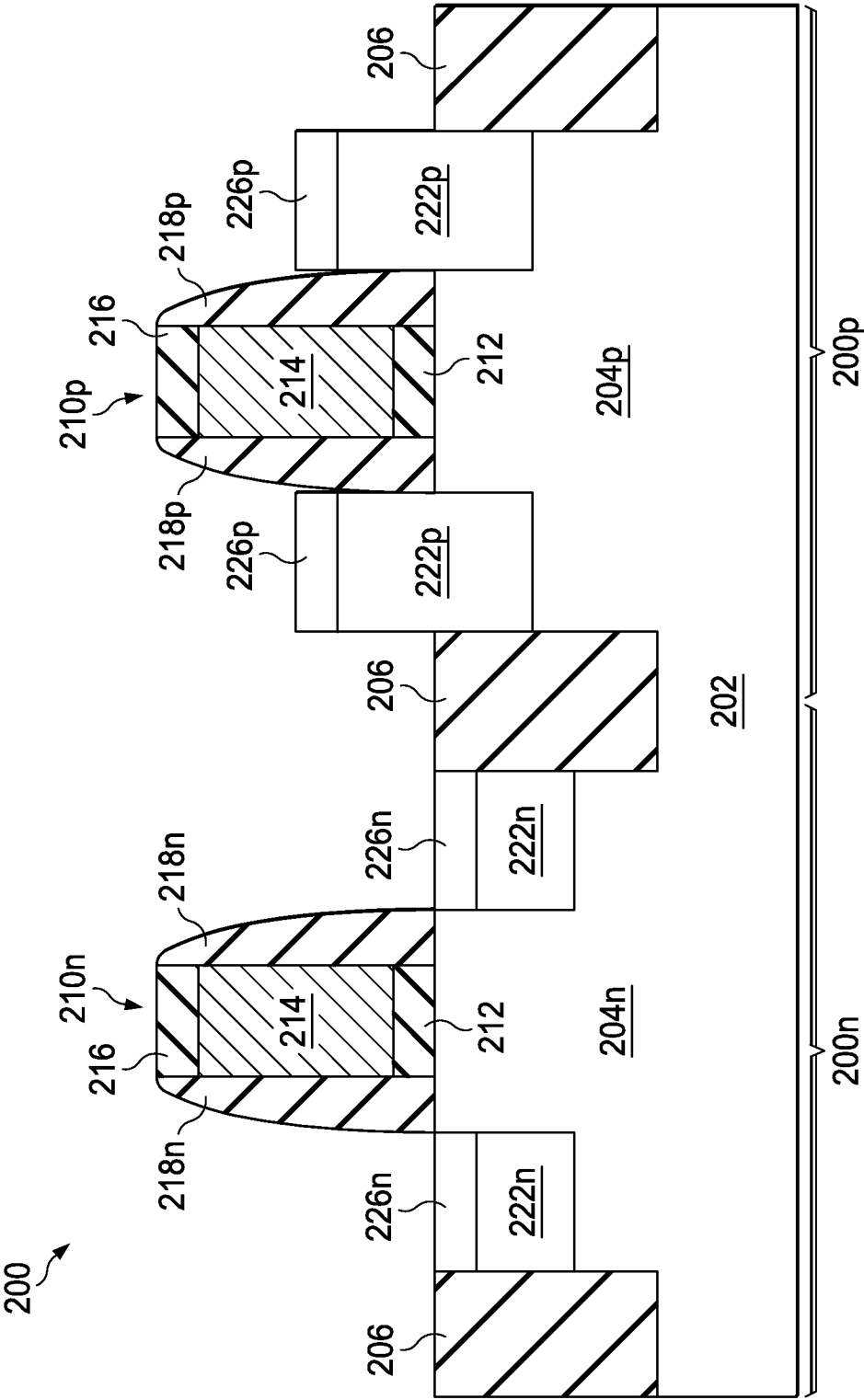


FIG. 8

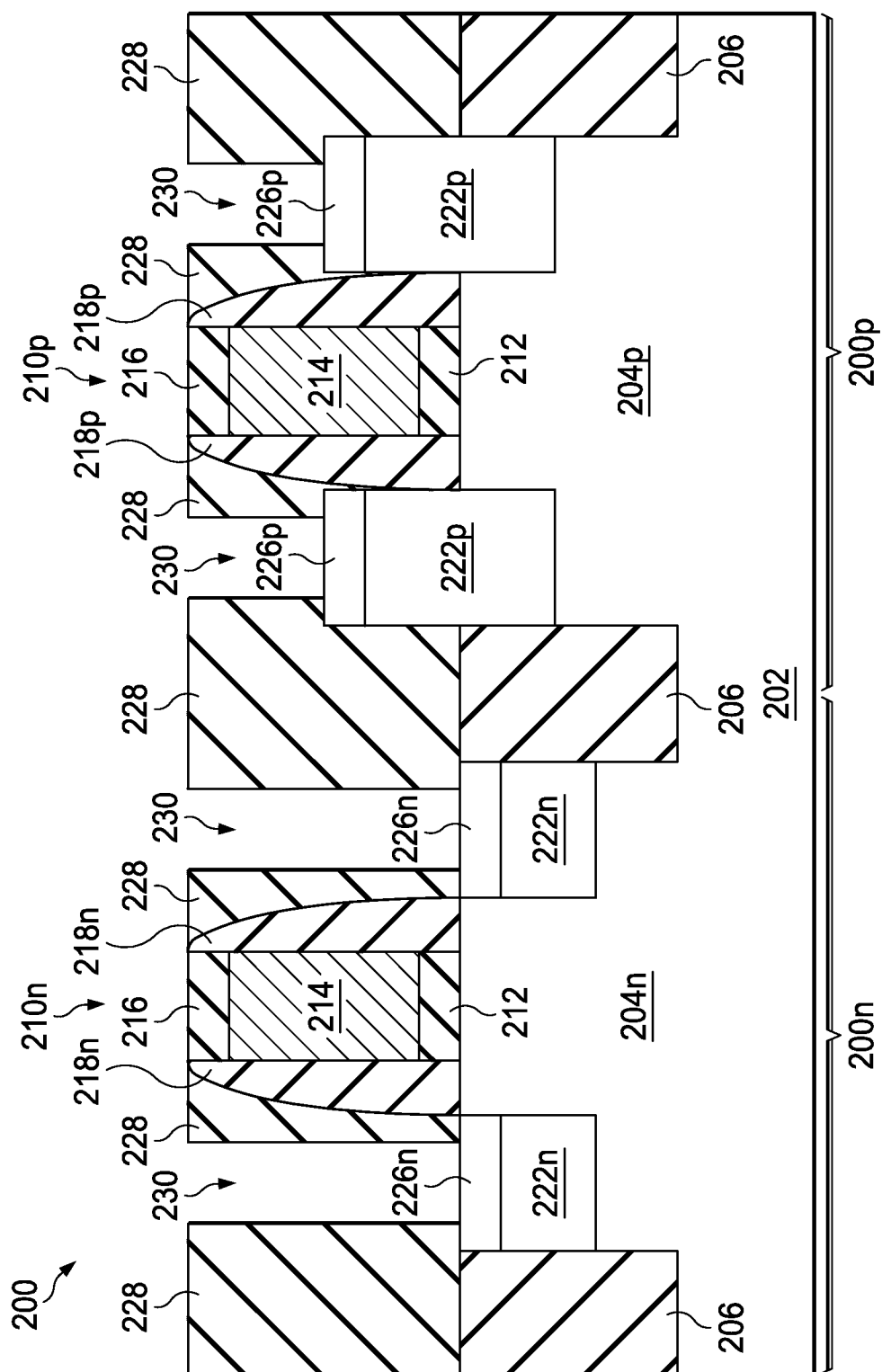


FIG. 10

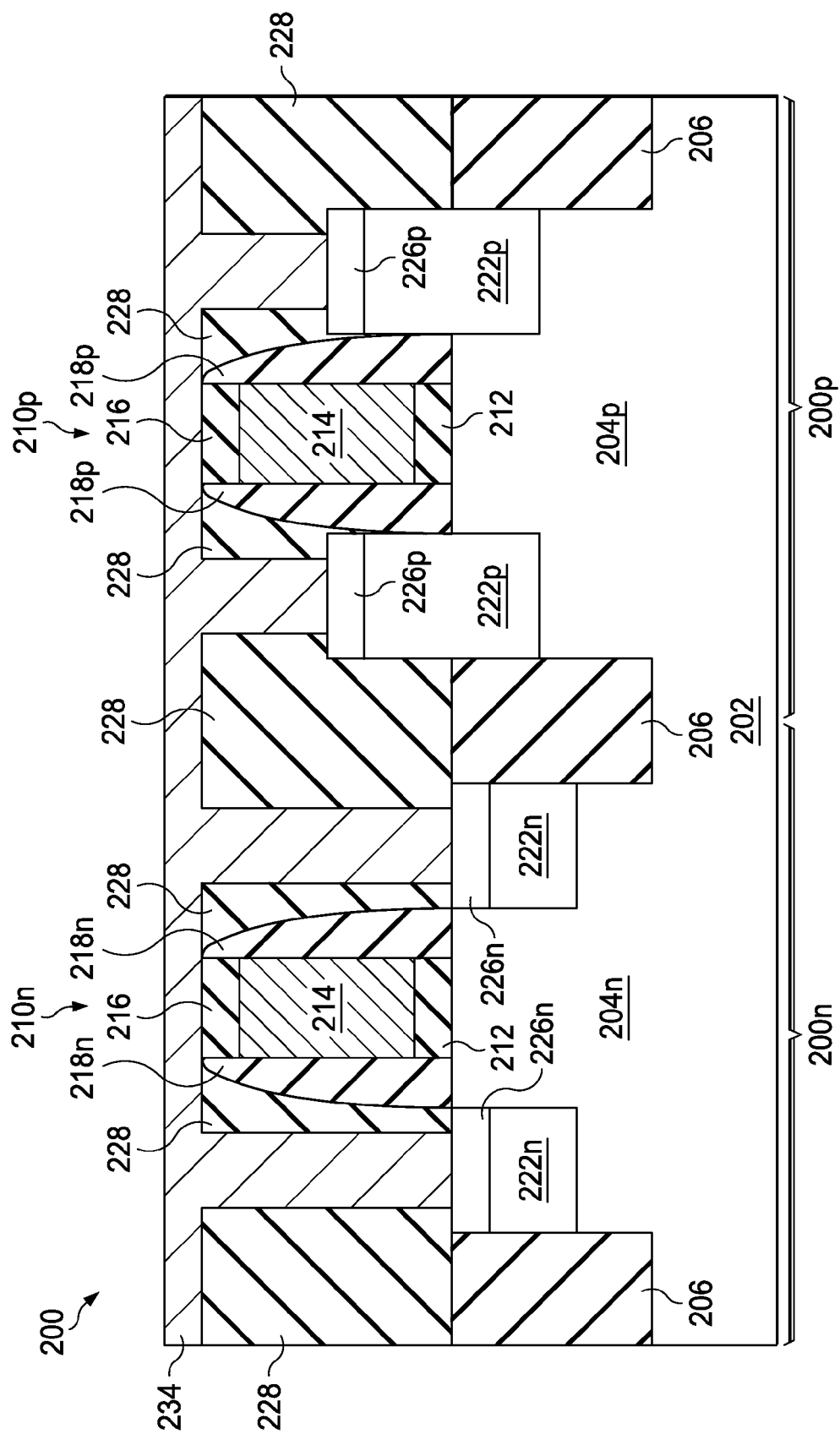
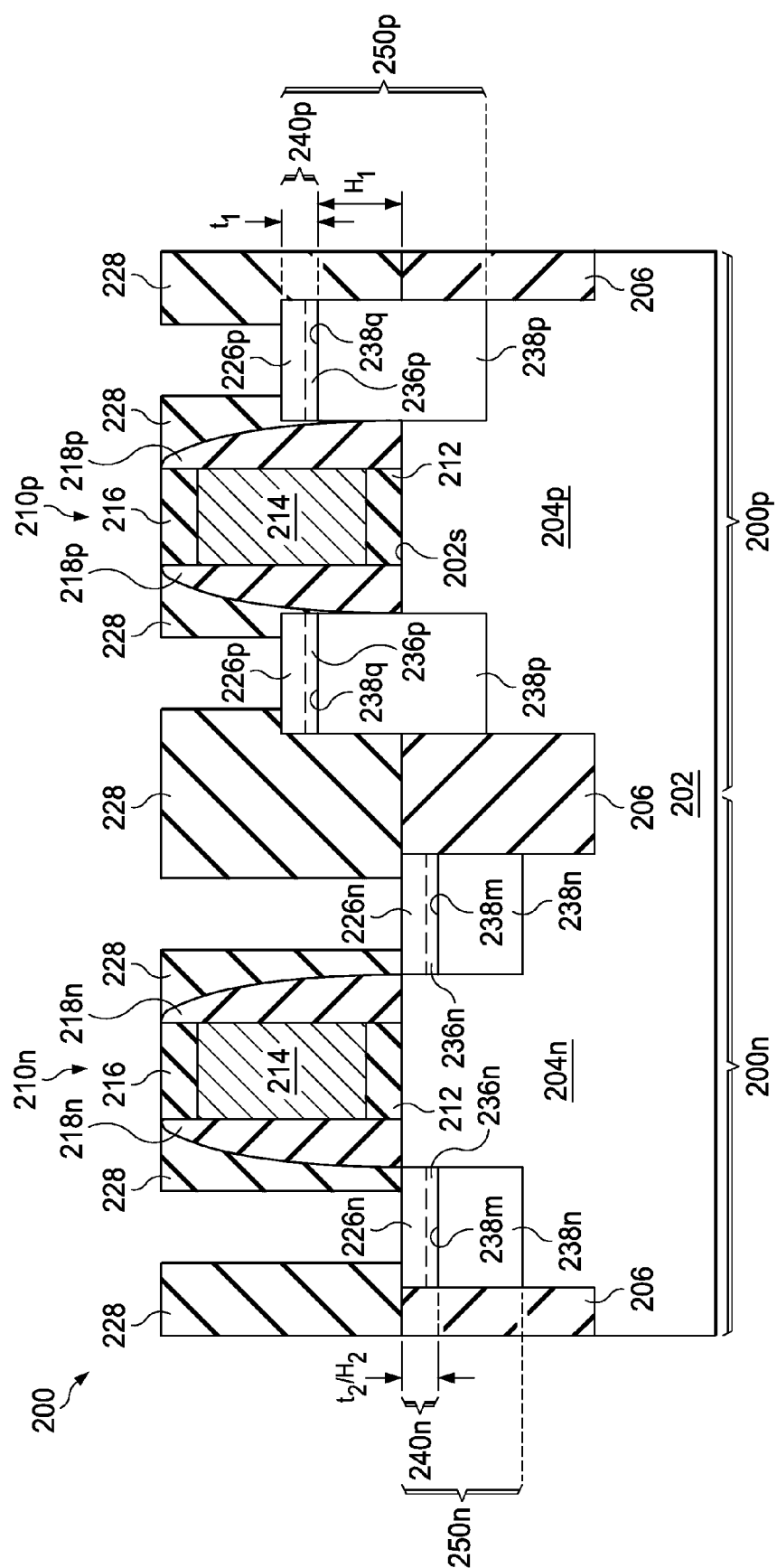


FIG. 11



STRAINED STRUCTURE OF A SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001] The disclosure relates to integrated circuit fabrication, and more particularly to a semiconductor device with a strained structure.

BACKGROUND

[0002] When a semiconductor device, such as a metal-oxide-semiconductor field-effect transistor (MOSFET), is scaled down through various technology nodes, a high-k gate dielectric layer and metal gate electrode layer are incorporated into the gate stack of the MOSFET to improve device performance with the decreased feature sizes. In addition, strained structures in source and drain (S/D) recess cavities of the MOSFET utilizing selectively grown silicon germanium (SiGe) may be used to enhance carrier mobility.

[0003] However, there are challenges to implement such features and processes in complementary metal-oxide-semiconductor (CMOS) fabrication. For example, it is difficult to achieve enhanced carrier mobility for a field-effect transistor (FET) because strained materials can not deliver a given amount of strain into channel region of the FET, thereby increasing the likelihood of device instability and/or device failure. As the gate length and spacing between devices decrease, these problems are exacerbated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features in the drawings may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIG. 1 is a flowchart illustrating a method of fabricating a strained structure of a semiconductor device according to various aspects of the present disclosure; and

[0006] FIGS. 2-12 show schematic cross-sectional views of a semiconductor device comprising a strained structure at various stages of fabrication according to various aspects of the present disclosure.

DESCRIPTION

[0007] It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. Various features may be arbitrarily drawn in different scales for simplicity and clarity. Further, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of sim-

plicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0008] Referring to FIG. 1, illustrated is a flowchart of a method 100 of fabricating a strained structure of a semiconductor device according to various aspects of the present disclosure. The method 100 begins with step 102 in which a substrate comprising a major surface is provided. The method 100 continues with step 104 in which a cavity is formed below the major surface. The method 100 continues with step 106 in which a strained material is epi-grown in the cavity, wherein a lattice constant of the strained material is different from a lattice constant of the substrate. The method 100 continues with step 108 in which a first metal layer is formed over the strained material. The method 100 continues with step 110 in which the first metal layer and the strained material are heated to form a first silicide region. The method 100 continues with step 112 in which an interlayer dielectric (ILD) layer is formed over the first silicide region and extending over the substrate. The method 100 continues with step 114 in which an opening is formed in the ILD layer, wherein the opening is on the first silicide region (i.e. the opening at least partially exposes the first silicide region). The method 100 continues with step 116 in which a second metal layer is formed on the first silicide region in the opening. The method 100 continues with step 118 in which the second metal layer and the strained material are heated to form a second silicide region lower than the first silicide region. The discussion that follows illustrates embodiments of semiconductor devices that can be fabricated according to the method 100 of FIG. 1.

[0009] FIGS. 2-12 show schematic cross-sectional views of a semiconductor device 200 comprising a strained structure 250 (see FIG. 12) at various stages of fabrication according to various aspects of the present disclosure. As employed in the present disclosure, the term semiconductor device 200 refers to a planar field effect transistor (FET). Alternatively, the term semiconductor device 200 refers to a fin field effect transistor (FinFET). The FinFET refers to any fin-based, multi-gate transistor. Other transistor structures and analogous structures are within the contemplated scope of this disclosure. The semiconductor device 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC). It is noted that the method of FIG. 1 does not produce a completed semiconductor device 200. Completed semiconductor device 200 may be fabricated using complementary metal-oxide-semiconductor (CMOS) technology processing. Accordingly, it is understood that additional processes may be provided before, during, and after the method 100 of FIG. 1, and that some other processes may only be briefly described herein. Also, FIGS. 2 through 12 are simplified for a better understanding of the concepts of the present disclosure. For example, although only the semiconductor device 200 is depicted in FIGS. 2-12, it is understood the IC may comprise a number of other devices comprising resistors, capacitors, inductors, fuses, etc.

[0010] Referring to FIG. 2 and step 102 in FIG. 1, a substrate 202 is provided. The substrate 202 may comprise a silicon substrate. In some embodiments, the substrate 202 may alternatively comprise silicon germanium, gallium arsenic, or other suitable semiconductor materials. The substrate 202 may further comprise other features such as various doped regions, a buried layer, and/or an epitaxy layer. Furthermore, the substrate 202 may be a semiconductor on insulator such as silicon on insulator (SOI). In other embodi-

ments, the semiconductor substrate **202** may comprise a doped epi layer, a gradient semiconductor layer, and/or may further include a semiconductor layer overlying another semiconductor layer of a different type such as a silicon layer on a silicon germanium layer. In other examples, a compound semiconductor substrate may comprise a multilayer silicon structure or a silicon substrate may include a multilayer compound semiconductor structure. In the depicted embodiment, the substrate **202** comprises a major surface **202s**.

[0011] In some embodiments, the semiconductor substrate **202** comprises a P-active region **204p** and an N-active region **204n** separated by an isolation region **206**. The active regions **204p**, **204n** may include various doping configurations depending on design requirements. For example, the P-active region **204p** is doped with n-type dopants, such as phosphorus or arsenic; the N-active region **204n** is doped with p-type dopants, such as boron or BF₂. As such, the P-active region **204p** may be usable for forming a p-type Field Effect Transistor (pFET) **200p**, while the N-active region **204n** may be usable for forming an n-type Field Effect Transistor (nFET) **200n**. Thus, the semiconductor device **200** comprises both the pFET **200p** and the nFET **200n**.

[0012] Isolation regions **206** may be formed on the substrate **202** to isolate the various active regions **204p**, **204n** from each other. The isolation regions **206** may utilize isolation technology, such as local oxidation of silicon (LOCOS) or shallow trench isolation (STI), to define and electrically isolate the various active regions **204p**, **204n**. In the present embodiment, the isolation regions **206** comprise an STI. The isolation regions **206** may comprise materials such as silicon oxide, silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), a low-k dielectric material, and/or combinations thereof. The isolation regions **206**, and in the present embodiment, the STI, may be formed by any suitable process. As one example, the formation of the STI may include patterning the semiconductor substrate **202** by a photolithography process, etching a trench in the substrate **202** (for example, by using a dry etching, wet etching, and/or plasma etching process), and filling the trench (for example, by using a chemical vapor deposition process) with a dielectric material. In some embodiments, the filled trench may have a multi-layer structure such as a thermal oxide liner layer filled with silicon nitride or silicon oxide.

[0013] Still referring to FIG. 2, a P-gate stack **210p** is formed over one portion of the major surface **202s** (i.e. channel portion of the P-active region **204p**), while an N-gate stack **210n** is formed over another portion of the major surface **202s** (i.e., channel portion of the N-active region **204n**). In some embodiments, each of the P-gate stack **210p** and the N-gate stack **210n** comprises a gate dielectric layer **212** and a gate electrode layer **214** over the gate dielectric layer **212**. The P-gate stacks **210p** and the N-gate stacks **210n** may be formed using any suitable process, including the processes described herein.

[0014] In one example, the gate dielectric layer **212** and gate electrode layer **214** are sequentially deposited over the substrate **202**. In some embodiments, the gate dielectric layer **212** may include silicon oxide, silicon nitride, silicon oxynitride, or high-k dielectric. High-k dielectrics comprise metal oxides. Examples of metal oxides used for high-k dielectrics include oxides of Li, Be, Mg, Ca, Sr, Sc, Y, Zr, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof. In the present embodiment, the gate dielectric layer **212** is a high-k dielectric layer with a thick-

ness in the range of about 10 to 30 angstroms. The gate dielectric layer **212** may be formed using a suitable process such as atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), thermal oxidation, UV-ozone oxidation, or combinations thereof. The gate dielectric layer **212** may further comprise an interfacial layer (not shown) to reduce damage between the gate dielectric layer **212** and the substrate **202**. The interfacial layer may comprise silicon oxide.

[0015] In some embodiments, the gate electrode layer **214** may comprise a single layer or multilayer structure. In the present embodiment, the gate electrode layer **214** may comprise poly-silicon. Further, the gate electrode layer **214** may be doped poly-silicon with uniform or non-uniform doping. In some embodiments, the gate electrode layer **214** may include an N-work-function metal for the N-gate stack **210n**. The N-work-function metal comprises Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, or Zr. In some embodiments, the gate electrode layer **214** may include a P-work-function metal for the P-gate stack **210p**. The P-work-function metal comprises TiN, WN, TaN, and Ru. In the present embodiment, the gate electrode layer **214** comprises a thickness in the range of about 30 nm to about 60 nm. The gate electrode layer **214** may be formed using a suitable process such as ALD, CVD, PVD, plating, or combinations thereof.

[0016] Then, a layer of photoresist (not shown) is formed over the gate electrode layer **214** by a suitable process, such as spin-on coating, and patterned to form a patterned photoresist feature by a proper lithography patterning method. In at least one embodiment, a width of the patterned photoresist feature is in the range of about 5 to 45 nm. The patterned photoresist feature can then be transferred using a dry etching process to the underlying layers (i.e., the gate electrode layer **214** and the gate dielectric layer **212**) to form the P-gate stack **210p** and the N-gate stacks **210n**. The photoresist layer may be stripped thereafter.

[0017] In another example, a hard mask layer **216** is formed over the gate electrode layer **214**; a patterned photoresist layer (not shown) is formed on the hard mask layer **216**; and the pattern of the photoresist layer is transferred to the hard mask layer **216** and then transferred to the gate electrode layer **214** and the gate dielectric layer **212** to form the P-gate stack **210p** and the N-gate stack **210n**. The hard mask layer **216** comprises silicon oxide. In some alternative embodiments, the hard mask layer **216** may comprise silicon nitride, silicon oxynitride, and/or other suitable dielectric materials, and may be formed using a method such as CVD or PVD. The hard mask layer **216** has a thickness in the range from about 100 to 800 angstroms. The photoresist layer may be stripped thereafter.

[0018] Still referring to FIG. 2, the semiconductor device **200** further comprises a pair of sidewall spacers **218p** on two sides of the P-gate stack **210p** and a pair of sidewall spacers **218n** on two sides of the N-gate stack **210n**. In some embodiments, the sidewall spacers **218p**, **218n** are formed by first forming a dielectric layer formed over the P-gate stack **210p**, the N-gate stacks **210n**, and the substrate **202** and covering sidewalls of the P-gate stack **210p** and sidewalls of the N-gate stack **210n**. The dielectric layer may include silicon oxide, silicon nitride, silicon oxy-nitride, or other suitable material. The dielectric layer may comprise a single layer or multilayer structure. The dielectric layer may be formed by CVD, PVD, ALD, or other suitable technique. The dielectric layer has a thickness ranging from about 5 to 15 nm. Then, an anisotropic

etching is performed on the dielectric layer to form the pair of sidewall spacers **218p** on two sides of the P-gate stack **210p** and the pair of sidewall spacers **218n** on two sides of the N-gate stack **210n**.

[0019] The process steps up to this point have provided the substrate **202** having the P-gate stack **210p** over channel portion of the P-active region **204p** and the N-gate stack **210n** over channel portion of the N-active region **204n**. Conventionally, portions of the N-active region (other than where the N-gate stack **210n** and the pair of sidewall spacers **218n** are formed thereover) are recessed to form N-source and drain (S/D) cavities in the N-active region **204n**. Then an N-strained material is epi-grown in the N-S/D cavities to form N-S/D regions to strain or stress the channel region of the nFET **200n** to enhance carrier mobility of the nFET **200n**. Further, portions of the P-active region **204p** (other than where the P-gate stack **210p** and the pair of sidewall spacers **218p** are formed thereover) are recessed to form P-source and drain (S/D) cavities in the P-active region **204p**. Then a P-strained material is epi-grown in the P-SD cavities to form P-S/D regions to strain or stress the channel region of the pFET **200p** to enhance carrier mobility of the pFET **200p**. However, the strained material (i.e., the N-strained material or P-strained material) may not deliver a given amount of strain into channel region of the semiconductor device, resulting in an insufficient on-current of the semiconductor device.

[0020] Accordingly, the processing discussed below with reference to FIGS. 3-12 may fabricate a strained structure in the S/D regions of the semiconductor device, thereby delivering a given amount of strain into channel region of the semiconductor device. Problems associated with insufficient on-current of a semiconductor device may be avoided, thereby enhancing the device performance.

[0021] For fabricating one embodiment of the strained structure **250** (shown in FIG. 12) of the semiconductor device **200**, the structure in FIG. 3 is produced by recessing portions of the N-active region **204n** (other than where the N-gate stack **210n** and the pair of sidewall spacers **218n** are formed thereover) to form N-source and drain (S/D) cavities **208n** in the N-active region **204n** (step **104** in FIG. 1). Each of the N-S/D cavities **208n** is below the major surface **202s** and adjacent to one side of the N-gate stack **210n**.

[0022] In the depicted embodiment, a dummy dielectric layer comprising a material such as silicon oxide is formed over the substrate **202** by a CVD process, and patterned to form a dummy dielectric feature **220p** by proper lithography and etch methods. The dummy dielectric feature **220p** covers the P-active region **204p** and exposes portions of the N-active region **204n** (other than where the N-gate stack **210n** and the pair of sidewall spacers **218n** are formed thereover). Then, using the dummy dielectric feature **220p** and the pair of sidewall spacers **218n** as hard masks, a biased etching process is performed to recess the major surface **202s** of the substrate **202** that are unprotected or exposed to form the N-S/D cavities **208n** in the N-active region **204n**. In one embodiment, the etching process may be performed using a chemical selected from NF_3 , CF_4 , and SF_6 as an etching gas. In an alternative embodiment, the etching process may be performed using a solution comprising NH_4OH and H_2O_2 .

[0023] Referring to FIG. 4 and step **106** in FIG. 1, subsequent to the formation of the N-S/D cavities **208n** in the N-active region **204n**, the structure in FIG. 4 is produced by epi-growing an N-strained material **222n** in the N-S/D cavities **208n**, wherein a lattice constant of the N-strained material

222n is different from a lattice constant of the substrate **202**. In the depicted embodiment, a top surface **222a** of the N-strained material **222n** is coplanar with the major surface **202s**, although it may be higher or lower than the major surface **202s**. In some embodiments, the N-strained material **222n** comprises SiCP or SiP.

[0024] In the depicted embodiment, a pre-cleaning process may be performed to clean the N-S/D cavities **208n** with HF or other suitable solution. Then, the N-strained material **222n** such as SiCP is selectively grown by an LPCVD process to fill the N-SD cavities **208n**. In the depicted embodiment, the LPCVD process is performed at a temperature of about 400 to 800° C. and under a pressure of about 1 to 15 Torr, using SiH_4 , CH_4 , and H_2 as reaction gases. Then the dummy dielectric feature **220p** is removed using HF solution.

[0025] Referring to FIG. 5 and step **104** in FIG. 1, after the formation of the N-strained material **222n** in the N-S/D cavities **208n**, portions of the P-active region **204p** (other than where the P-gate stack **210p** and the pair of sidewall spacers **218p** are formed thereover) are recessed to form P-source and drain (S/D) cavities **208p** in the P-active region **204p**. Each of the P-S/D cavities **208p** is below the major surface **202s** and adjacent to one side of the P-gate stack **210p**. In the depicted embodiment, a dummy dielectric layer such as silicon oxide is formed over the substrate **202** by a CVD process, and patterned to form a dummy dielectric feature **220n** by proper lithography and etch methods. The dummy dielectric feature **220n** covers the N-active region **204n** and exposes portions of the P-active region **204p** (other than where the P-gate stack **210p** and the pair of sidewall spacers **218p** are formed thereover). Then, using the dummy dielectric feature **220n** and the pair of sidewall spacers **218p** as hard masks, a biased etching process is performed to recess the major surface **202s** of the substrate **202** that are unprotected or exposed to form the P-S/D cavities **208p**. In at least one embodiment, the etching process may be performed using a chemical selected from NF_3 , CF_4 , and SF_6 as an etching gas. In an alternative embodiment, the etching process may be performed using a solution comprising NH_4OH and/or H_2O_2 .

[0026] Referring to FIG. 6 and step **106** in FIG. 1, after the formation of the P-S/D cavities **208p** in the P-active region **204p**, the structure in FIG. 6 is produced by epi-growing a P-strained material **222p** in the P-S/D cavities **208p**, wherein a lattice constant of the P-strained material **222p** is different from a lattice constant of the substrate **202**. In the depicted embodiment, a top surface **222b** of the P-strained material **222p** is higher than the major surface **202s**. In some embodiments, the P-strained material **222p** comprises SiGe or SiGeB.

[0027] In the depicted embodiment, a pre-cleaning process may be performed to clean the P-S/D cavities **208p** with HF or other suitable solution. Then, the P-strained material **222p** such as silicon germanium (SiGe) is selectively grown by an LPCVD process to fill the P-S/D cavities **208p**. In one embodiment, the LPCVD process is performed at a temperature of about 660 to 700° C. and under a pressure of about 13 to 50 Torr, using SiH_2Cl_2 , HCl , GeH_4 , B_2H_6 , and H_2 as reaction gases. Then the dummy dielectric feature **220n** is removed using HF solution.

[0028] Referring to FIG. 7 and step **108** in FIG. 1, subsequent to the formation of the strained materials **222** (i.e., the P-strained material **222p** and the N-strained material **222n**), a first metal layer **224** is formed over the strained materials **222** to a thickness of between about 15 and 60 angstroms. In the

depicted embodiment, the first metal layer **224** comprises titanium, cobalt, nickel, platinum, erbium, or palladium. The first metal layer **224** may be formed by CVD, PVD, plating, ALD, or other suitable technique.

[0029] Then, the structure depicted in FIG. **8** is produced by heating the first metal layer **224** and the strained materials **222** to form first silicide regions **226** (step **110** in FIG. **1**). In other words, the first metal layer **224** in contact with the strained materials **222** is then transformed into the first silicide regions **226** by a thermal process, such as a rapid thermal anneal (RTA) process. In the depicted embodiment, the first silicide regions **226** comprise first N-silicide regions **226_n** and first P-silicide regions **226_p**. In some embodiments, the first silicide regions **226** comprise titanium silicide, cobalt silicide, nickel silicide, platinum silicide, erbium silicide, palladium silicide, and combinations thereof.

[0030] In the depicted embodiment, a first RTA process is applied to heat the substrate **202** at a temperature of about 230° C. to 260° C. The first metal layer **224** in contact with the strained materials **222** will form a high-resistance silicide. Then, the remaining un-reacted first metal layer **224** is removed using, for example, a solution comprising NH₄OH, H₂O₂, and deionized water. In order to transform the high-resistance silicide to a low-resistance silicide, a second RTA process is applied to heat the substrate **202** at a temperature of about 650° C. to 750° C., thereby forming the first silicide regions **226**.

[0031] Referring to FIG. **9** and step **112** in FIG. **1**, after the formation of the first silicide regions **226**, the structure in FIG. **9** is produced by forming an interlayer dielectric (ILD) layer **228** over the first silicide regions **226** and extending over the substrate **202**. In some embodiments, the ILD layer **228** may comprise a dielectric material. The dielectric material may comprise silicon oxide, silicon nitride, silicon oxynitride, or a low-k material. It is understood that the ILD layer **228** may comprise one or more dielectric materials and/or one or more dielectric layers. In some embodiments, the ILD layer **228** may be deposited over the first silicide region **226** to a suitable thickness by CVD, high density plasma (HDP) CVD, sub-atmospheric CVD (SACVD), spin-on, sputtering, or other suitable methods. In the present embodiment, the ILD layer **228** has a thickness of about 3000 to 4500 Å. Then, the ILD layer **228** is planarized using a chemical mechanical polishing (CMP) process until a top surface of the hard mask (i.e., the sidewall spacer) **218** is exposed or reached.

[0032] Subsequent CMOS processing steps applied to the semiconductor device **200** of FIG. **9** comprise forming openings **230** in the ILD layer **228**, wherein the openings **230** are on the first silicide regions **226** (step **114** in FIG. **1**). Referring to FIG. **10**, the openings **230** may be formed by any suitable process. As one example, the formation of the openings **230** may comprise patterning the ILD layer **228** by a conventional photolithography process, and etching the exposed ILD layer **228** (for example, by using a dry etching, wet etching, and/or plasma etching process) to remove portions of the ILD layer **228** over portions of the first silicide regions **226** to expose top portions of the first silicide regions **226**.

[0033] Referring to FIG. **11** and step **116** in FIG. **1**, subsequent to the formation of the openings **230** in the ILD layer **228**, a second metal layer **234** is formed on the first silicide regions **226** in the openings **230** to a thickness of between about 15 and 60 angstroms. In the depicted embodiment, the second metal layer **234** comprises titanium, cobalt, nickel, platinum, erbium, and palladium. The second metal layer **234**

may be formed by CVD, PVD, plating, ALD, or other suitable technique. Although second metal layer **234** is shown as over-filling openings **230**, it is not necessary that second metal layer **234** over-fill the trench or even completely fill the trench, because excess portions of second metal layer **234** are subsequently removed, as described more fully below.

[0034] Then, the structure depicted in FIG. **12** is produced by heating the second metal layer **234** and the strained materials **222** to form second silicide regions **236** lower than the first silicide regions **226** (step **118** in FIG. **1**). In other words, the second metal layer **234** will penetrate through the first silicide regions **226** to meet the remaining strained material **222**, and then will be transformed into the second silicide regions **236** by a thermal process, such as a rapid thermal anneal (RTA) process. In the depicted embodiment, the second silicide regions **236** comprise second N-silicide regions **236_n** and second P-silicide regions **236_p**. In some embodiments, the second silicide regions **236** comprise titanium silicide, cobalt silicide, nickel silicide, platinum silicide, erbium silicide, and palladium silicide.

[0035] In the depicted embodiment, a third RTA process is applied to heat the substrate **202** at a temperature of about 230° C. to 260° C. The second metal layer **234** meeting the strained material **222** will form a high-resistance silicide. Then, the remaining un-reacted second metal layer **234** is removed using, for example, a solution comprising NH₄OH, H₂O₂, and deionized water. In order to transform the high-resistance silicide to a low-resistance silicide, a fourth RTA process is applied to heat the substrate **202** at a temperature of about 650° C. to 750° C., thereby forming the second silicide regions **236**. In the depicted embodiment, the second N-silicide regions **236_n** are on the remaining N-strained material **222_n** (referred to as N-strained regions **238_n** hereafter), while the second P-silicide regions **236_p** are on the remaining P-strained material **222_p** (referred to as P-strained regions **238_p** hereafter).

[0036] In some embodiments, the P-strained region **238_p** has a first top surface **238_q** higher than the major surface **202_s**. In some embodiments, a distance H₁ between the first top surface **238_q** and the major surface **202_s** is in the range of about 5 to 15 nm.

[0037] In some embodiments, the N-strained region **238_n** has a second top surface **238_m** lower than the major surface **202_s**. In some embodiments, a distance H₂ between the second top surface **238_m** and the major surface **202_s** is in the range of about 10 to 25 nm.

[0038] In some embodiments, the first N-silicide regions **226_n** and the second N-silicide regions **236_n** are combined and referred to as N-silicide regions **240_n**. As such, a volume of the N-silicide regions **240_n** is a summation of a volume of the first N-silicide regions **226_n** and a volume of the second N-silicide regions **236_n**, which is greater than each of the volume of the first N-silicide regions **226_n** and the volume of the second N-silicide regions **236_n**. In some embodiment, a maximum thickness t₂ of the N-silicide region **240_n** is in the range of about 10 to 25 nm. In the depicted embodiment, the N-silicide regions **240_n** are on the N-strained region **238_n**. Further, the N-silicide regions **240_n** are used to strain or stress the channel region of the nFET **200_n** to enhance carrier mobility of the nFET **200_n**.

[0039] In some embodiments, the first P-silicide regions **226_p** and the second P-silicide regions **236_p** are combined and referred to as P-silicide regions **240_p**. As such, a volume of the P-silicide regions **240_p** is a summation of a volume of

the first P-silicide regions **226p** and a volume of the second P-silicide regions **236p**, which is greater than each of the volume of the first P-silicide regions **226p** and the volume of the second P-silicide regions **236p**. In some embodiments, a maximum thickness t_1 of the P-silicide region **240p** is in the range of about 10 to 25 nm. It should be noted that the P-silicide regions **240p** (with similar stress as the N-silicide regions **240n**) will degrade carrier mobility of the pFET **200p** if the P-silicide regions **240p** strain or stress the channel region of the pFET **200p**. In the depicted embodiment, the P-silicide regions **240p** are on the P-strained regions **238p**. Further, the P-silicide regions **240p** is used to strain or stress the P-gate stack **210p** to enhance work-function of the P-gate stack **210p**. Thus, the P-silicide regions **240p** are adjacent to the P-gate stack **210p**, but far from the channel region of the pFET **200p**.

[0040] In some embodiments, the P-silicide regions **240p** and P-strained regions **238p** are combined and referred to as a P-strained structure **250p**. In some embodiments, the N-silicide regions **240n** and N-strained regions **238n** are combined and referred to as an N-strained structure **250n**. In some embodiments, the P-strained structure **250p** and N-strained structure **250n** are combined and referred to as a strained structure **250**.

[0041] Accordingly, Applicant's method may fabricate large-volume N-silicide regions **240n** in the S/D regions of the nFET **200n** of the semiconductor device **200**, thereby delivering a given amount of strain into channel region of the semiconductor device **200**. Further, Applicant's method may fabricate large-volume P-silicide regions **240p** in the S/D regions of the pFET **200p** of the semiconductor device **200**, thereby delivering a given amount of strain into P-gate stack **210p** of the semiconductor device **200**. Problems associated with insufficient on-current of the semiconductor device **200** may be avoided, thereby enhancing the device performance.

[0042] It is understood that the semiconductor device **200** may undergo further CMOS processes to form various features such as contacts/vias, interconnect metal layers, dielectric layers, passivation layers, etc.

[0043] In accordance with embodiments, a semiconductor device comprises a substrate comprising a major surface; a p-type Field Effect Transistor (pFET) comprising: a P-gate stack over the major surface, a P-strained region in the substrate adjacent to one side of the P-gate stack, wherein a lattice constant of the P-strained region is different from a lattice constant of the substrate, wherein the P-strained region has a first top surface higher than the major surface; and a P-silicide region on the P-strained region; and an n-type Field Effect Transistor (nFET) comprising: an N-gate stack over the major surface, an N-strained region in the substrate adjacent to one side of the N-gate stack, wherein a lattice constant of the N-strained region is different from a lattice constant of the substrate, wherein the N-strained region has a second top surface lower than the major surface and a N-silicide region on the N-strained region.

[0044] In accordance with another embodiments, a method for fabricating a semiconductor device comprises providing a substrate comprising a major surface; forming a cavity below the major surface; epi-growing a strained material in the cavity, wherein a lattice constant of the strained material is different from a lattice constant of the substrate; forming a first metal layer over the strained material; heating the first metal layer and the strained material to form a first silicide region; forming an interlayer dielectric (ILD) layer over the

first silicide region and extending over the substrate; forming an opening in the ILD layer, wherein the opening is on the first silicide region; forming a second metal layer on the first silicide region in the opening; and heating the second metal layer and the strained material to form a second silicide region lower than the first silicide region.

[0045] While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A semiconductor device, comprising:
 - a substrate comprising a major surface;
 - a p-type Field Effect Transistor (pFET) comprising:
 - a P-gate stack over the major surface,
 - a P-strained region in the substrate adjacent to one side of the P-gate stack, wherein a lattice constant of the P-strained region is different from a lattice constant of the substrate, wherein the P-strained region has a first top surface higher than the major surface; and
 - a P-silicide region on the P-strained region; and
 - an n-type Field Effect Transistor (nFET) comprising:
 - an N-gate stack over the major surface,
 - an N-strained region in the substrate adjacent to one side of the N-gate stack, wherein a lattice constant of the N-strained region is different from a lattice constant of the substrate, wherein the N-strained region has a second top surface lower than the major surface and
 - a N-silicide region on the N-strained region.
2. The semiconductor device of claim 1, wherein a distance between the first top surface and the major surface is in the range of about 5 to 15 nm.
3. The semiconductor device of claim 1, wherein a maximum thickness of the P-silicide region is in the range of about 10 to 25 nm.
4. The semiconductor device of claim 1, wherein the P-silicide region comprises titanium silicide, cobalt silicide, nickel silicide, platinum silicide, erbium silicide, or palladium silicide.
5. The semiconductor device of claim 1, wherein the P-strained region comprises SiGe or SiGe:B.
6. The semiconductor device of claim 1, wherein the P-gate stack comprises a P-work-function metal.
7. The semiconductor device of claim 6, wherein the P-work-function metal comprises TiN, WN, TaN, and Ru.
8. The semiconductor device of claim 1, wherein the P-gate stack comprises a gate dielectric, wherein the gate dielectric the gate dielectric comprises silicon oxide, silicon nitride, silicon oxy-nitride, or high-k dielectric.
9. The semiconductor device of claim 1, wherein a distance between the second top surface and the major surface is in the range of about 10 to 25 nm.
10. The semiconductor device of claim 1, wherein a maximum thickness of the N-silicide region is in the range of about 10 to 25 nm.
11. The semiconductor device of claim 1, wherein the N-silicide region comprises titanium silicide, cobalt silicide, nickel silicide, platinum silicide, erbium silicide, or palladium silicide.

12. The semiconductor device of claim **1**, wherein the N-strained region comprises SiCP or SiP.

13. The semiconductor device of claim **1**, wherein the N-gate stack comprises an N-work-function metal.

14. The semiconductor device of claim **13**, wherein the N-work-function metal comprises Ti, Ag, Al, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, or Zr.

15. The semiconductor device of claim **1**, wherein the N-gate stack comprises a gate dielectric, wherein the gate dielectric the gate dielectric comprises silicon oxide, silicon nitride, silicon oxy-nitride, or high-k dielectric.

16. A method for fabricating a semiconductor device, comprising:

- providing a substrate comprising a major surface;
- forming a cavity below the major surface;
- epi-growing a strained material in the cavity, wherein a lattice constant of the strained material is different from a lattice constant of the substrate;
- forming a first metal layer over the strained material;
- heating the first metal layer and the strained material to form a first silicide region;
- forming an interlayer dielectric (ILD) layer over the first silicide region and extending over the substrate;
- forming an opening in the ILD layer, wherein the opening is on the first silicide region;

forming a second metal layer on the first silicide region in the opening; and

heating the second metal layer and the strained material to form a second silicide region lower than the first silicide region.

17. The method of claim **16**, wherein the step of heating the first metal layer and the strained material comprises heating the substrate at a temperature of about 230 to 260° C.;

removing remaining first metal layer; and heating the substrate at a temperature of about 650 to 750° C.

18. The method of claim **16**, wherein the step of heating the second metal layer and the strained material comprises: heating the substrate at a temperature of about 230 to 260° C.;

removing remaining second metal layer; and heating the substrate at a temperature of about 650 to 750° C.

19. The method of claim **16**, wherein the step of forming a first metal layer over the strained material is performed by a physical vapor deposition process.

20. The method of claim **16**, wherein the cavity is adjacent to one side of a gate stack.

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