UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.

AND

APPLE INC.,

Petitioners

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

IPR2025-00865

Patent No. 9,147,747

DECLARATION OF R. JACOB BAKER, PH.D., P.E. IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,147,747

TABLE OF CONTENTS

I. INTRODUCTION 1

II. BACKGROUND AND QUALIFICATIONS 2

A. Industry Experience 3

B. Academic Experience 6

C. Other Relevant Experience 7

III. MATERIALS REVIEWED 9

IV. PERSON OF ORDINARY SKILL IN THE ART AT THE TIME OF THE ALLEGED INVENTION 11

V. TECHNICAL BACKGROUND 12

A. Field-Effect-Transistors (FETs) 13

B. Self-Aligned/Shared Contacts 20

C. Planarization 22

D. Metal Interconnect (BEOL) 25

VI. THE '747 PATENT 27

A. Description 27

B. The Prosecution History 29

VII. OVERVIEW OF THE PRIOR ART 29

A. Pethe 29

B. Chang 37

VIII. CLAIM CONSTUCTION 38

IX. THE PRIOR ART DISCLOSES AND/OR SUGGESTS ALL THE RECITED FEATURES OF CLAIMS 1-9 OF THE '747 PATENT 39

A. Ground 1: Pethe Discloses (Ground 1A) and Suggests (Ground 1B) Claims 1-5, and 8 39

1. Claim 1 40

2. Claim 2 91

3. Claim 3 94

4. Claim 4 99

5. Claim 5 103

6. Claim 8 108

7. Combination of Pethe's Embodiments 111

B. Ground 2: Pethe Discloses and/or Suggests Claims 6-7 114

1. Claim 6 114

2. Claim 7 122

C. Ground 3: Pethe in View of Bohr Discloses and/or Suggests Claim 7 128

1. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact. 128

D. Ground 4: Pethe in View of Huang Discloses and/or Suggests Claims 8-9 141

1. Claims 8-9 141

E. Ground 5: Chang Discloses (Ground 5A) and Suggests (Ground 5B) Claims 1 and 2 166

1. Claim 1 166

2. Claim 2 193

3. Combination of Chang's Embodiments 194

F. Ground 6: Chang Discloses and/or Suggests Claims 4-6 196

1. Claims 4-5 197

2. Claim 6 200

G. Ground 7: Chang in View of Huang Discloses and/or Suggests Claims 3 and 8-9.....203

1. Claim 3 203

2. Claims 8-9 215

H. Ground 8: Chang in View of Hong Discloses and/or Suggests Claims 4-5 237

1. Claim 4 237

2. Claim 5 243

I. Ground 9: Chang in View of Bohr Discloses and/or Suggests Claim 7 244

1. Claim 7 244

CONCLUSION 250

I, Dr. R. Jacob Baker declare as follows:

I. INTRODUCTION

1. I have been retained as an independent expert consultant in this proceeding before the United States Patent and Trademark Office ("PTO") regarding U.S. Patent No. 9,147,747 ("the '747 patent") (EX1001).[1] I have been asked to consider whether prior art references disclose or suggest the features recited in claims 1-9 ("the challenged claims") of the '747 patent.

2. My opinions are set forth below.

3. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study and analysis, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or in any litigation involving the '747 patent.

[1] In this Declaration, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the '747 patent.

II. BACKGROUND AND QUALIFICATIONS

4. My qualifications generally are set forth in my Curriculum Vitae, which is attached as EX1003 and also includes a list of the publications I have authored and a list of the other cases in which I have testified during the last four years.

5. I have been working as an Engineer since 1985 and I have been teaching Electrical and Computer Engineering courses since 1991. I am currently a Professor Emeritus of Electrical and Computer Engineering at the University of Nevada, Las Vegas ("UNLV").

6. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

7. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices," published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

A. Industry Experience

8. I have done technical and expert witness consulting for over 200 companies and their subsidiaries since I started working as an engineer in 1985. From 1985 to 1993, I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the fabrication of, over 30 electronic and electro-optic instruments, including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

9. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry.

10. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at

Micron Technology, Inc. ("MTI") in Boise, Idaho from 1994 to 2008. I worked on the circuit design and process integration of 3D transistors, that is, transistors where the gate was surrounded by semiconductor material to minimize the transistor leakage. I spent considerable time working on the development of flash memory chips while at MTI, again both circuit design and process development. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics, including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical-to-physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM, which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via

interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI's acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology.

11. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics.

12. My most recent research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics, and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory.

B. Academic Experience

13. I was an adjunct faculty member in the Electrical Engineering departments of UNLV and UNR from 1991-1993. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University ("BSU"), where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university's second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised more than 100 masters and doctoral students.

14. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011, I received the IEEE Circuits and Systems Education Award. I received the

Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

15. I have authored several books and papers in the electrical and computer engineering area. My published books include CMOS Circuit Design, Layout, and Simulation (Baker, R.J., Wiley-IEEE, ISBN: 9781119481515 (4th ed., 2019)) and CMOS Mixed-Signal Circuit Design (Baker, R.J., Wiley-IEEE, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I coauthored DRAM Circuit Design: Fundamental and High-Speed Topics (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., Wiley-IEEE, ISBN: 9780470184752 (2008)), DRAM Circuit Design: A Tutorial (Keeth, B. and Baker, R.J., Wiley-IEEE, ISBN: 0-7803-6014-1 (2001)), and CMOS Circuit Design, Layout and Simulation (Baker, R.J., Li, H.W., and Boyce, D.E., Wiley - IEEE, ISBN: 9780780334168 (1998)). My CMOS books, for example, teach the design, layout, and process integration of 3D transistors, those transistors where the gate is surrounded by semiconductor, such as FinFETs. I contributed as an editor and co-author on several other electrical and computer engineering books.

C. Other Relevant Experience

16. I have performed technical and expert witness consulting for more than 200 companies and their subsidiaries and given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of

more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication, and packaging.

17. I currently serve, or have served, as a volunteer on the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for IEEE Solid-State Circuits Magazine; IEEE Kirchhoff Award Committee (2020-2023); and advisor for the student branch of the IEEE at UNLV (2013-2024). These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

18. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

III. MATERIALS REVIEWED

19. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding semiconductor structures and manufacturing processes.

20. In forming my opinions expressed in this Declaration, I reviewed the following materials:

EX1001	U.S. Patent No. 9,147,747
EX1004	Prosecution History of U.S. Patent No. 9,147,747
EX1005	U.S. Patent No. 9,461,143 ("**Pethe**")
EX1006	PCT/US 2011/066989 ("**Golonzka**")
EX1007	U.S. Patent App. Pub. No. 2006/0223302 ("**Chang**")
EX1008	U.S. Patent App. Pub. No. 2013/0161707 ("**Huang**")
EX1009	U.S. Patent No. 8,436,404 ("**Bohr**")
EX1010	U.S. Patent No. 8,895,389 ("**Hong**")
EX1011	CN 2013 1 0006390 ("**Hong Foreign Priority**") and Certified Translation of Hong with Certification of Translation
EX1012	D. Neamen, *Semiconductor Physics and Devices – Basic Principles*, 4th Ed. (2011)
EX1013	U.S. Patent No. 8,258,057 ("**Kuhn**")
EX1014	Wolf, Stanley. *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology*. Lattice Press, 2002 ("**Wolf**")
EX1015	May, Gary S., and Simon M. Sze. *Fundamentals of Semiconductor Fabrication*. John Wiley & Sons, 2004 ("**May**")

EX1016	U.S. Patent App. Pub. No. 2012/0252180 ("**Tomimatsu**")
EX1017	U.S. Patent App. Pub. 2008/0142975 ("**Ning**")
EX1018	U.S. Patent No. 8,741,723 ("**Chi**")
EX1019	U.S. Patent App. Pub. 2014/0048888 ("**Chen**")
EX1020	Xiao, H. (2012). *Introduction to Semiconductor Manufacturing Technology* (2nd ed.). Prentice Hall ("**Xiao**")
EX1021	U.S. Patent No. 8,835,245 ("**Baars**")
EX1022	U.S. Patent No. 8,455,314 ("**Griebenow**")
EX1023	**Sze**, S.M. *Physics of Semiconductor Devices*. 2nd ed., John Wiley & Sons, 1981 ("**Sze**")
EX1024	U.S. Patent App. Pub. No. 2009/0155991 ("**Lee**")
EX1025	U.S. Patent App. Pub. No. 2009/0014796 ("**Liaw**")
EX1026	Banerjee, G. and R. Rhoades, *Chemical Mechanical Planarization*, ECS Trans., 13 (4) 1-19 (2008)
EX1027	U.S. Patent No. 5,536,962 ("**Pfiester**")
EX1028	U.S. Patent No. 8,928,048 ("**Xie**")
EX1029	U.S. Patent No. 8,906,754 ("**Pham**")

21. I also considered any other documents and materials I refer to in this Declaration.

22. My opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would

have understood the state of the art, the prior art, and the claims and the specification of the ’747 patent at the time of the alleged invention, which I discuss below.

23. I have been asked to consider that the time of the alleged invention of the ’747 patent was around 2013 (including and up to May 2, 2013), which corresponds to the filing date of the application that led to the ’747 patent.

24. Based on my experience and expertise, it is my opinion that certain references disclose and/or suggest all the features recited in the challenged claims of the ’747 patent, as I discuss in detail below.

IV. PERSON OF ORDINARY SKILL IN THE ART AT THE TIME OF THE ALLEGED INVENTION

25. I am familiar with the level of ordinary skill in the art regarding the ’747 patent as of around May 2, 2013. Considering the ’747 patent, the technology, the educational level and experience of workers in the field relating to the patent, and problems and solutions in that field, and drawing on my own experience, I believe a person of ordinary skill in the art at the time of the alleged invention (around May 2, 2013) (which I refer herein as “POSITA”) would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as for example, integrated circuit device (or transistor) design and/or manufacturing. Additional relevant education could substitute for professional

experience, and significant work experience or training could substitute for less formal education.

26. My opinions in this Declaration regarding the ’747 patent and the prior art (including the state of the art) are from the perspective of one of ordinary skill in the art as I defined above, during the relevant timeframe (the time of the alleged invention), which I discussed above as being around May 2, 2013.

V. TECHNICAL BACKGROUND

27. Below, I present a brief overview of certain features relating to those discussed and claimed in the ’747 patent that were known to a person of ordinary skill in the art prior to and at the time of the alleged invention of the ’747 patent. The features, techniques, and concepts I describe below in this technical background section reflect the state of the art knowledge that a person of ordinary skill in the art would have had prior to and at the time of the alleged invention of the ’747 patent. I rely on, and incorporate as applicable (even if not expressly mentioned below in §IX), the following disclosures and opinions to support my opinions in this Declaration, including those opinions relating to how the prior art discloses and/or suggests the challenged claims of the ’747 patent and how and why a person of ordinary skill in the art would have been motivated to consider and combine the disclosures and suggestions from one or more prior art references as I explain below in §IX.

A. Field-Effect-Transistors (FETs)

28. The field-effect transistor (FET) has, for many decades, been the foundational device for very-large-scale integrated circuits (ICs) such as microprocessors and semiconductor memories. (EX1023, 431.) FETs, such as MOSFETs, function essentially as a switch controlled by voltage applied to a "gate" (G) between "source" (S) and "drain" (D) regions.

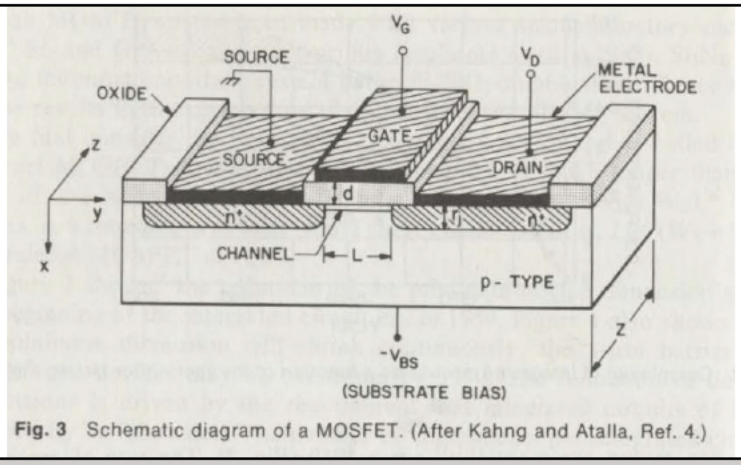


Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

EX1023, Figure 3

(EX1023, 433-34, Figs. 3, 6.)

29. As shown above, the channel is disposed below the gate, and the source and drain semiconductor regions are disposed on each side of the gate. When the FET is turned on, current flows between the source and drain regions through the "channel" formed under the gate of the FET. (EX1023, 433-34, 438, Figs. 3, 6.) The element that provides the source of electrical carriers that will flow along the channel during operation is generally termed the "source," and the element that acts as a sink or drain for the electrical carriers to flow to during operation is generally

termed the "drain." A source or drain element is commonly referred to as a "source/drain" because whether the element operates as a "source" of electrical carriers or a "drain" for electrical carriers in a FET is interchangeable depending on the voltage applied to the element. A POSITA would have understood that source/drain regions are conventionally formed by diffusion of dopants, and in such instances, were commonly referred to as diffusion regions. (EX1012, xxiii, Figure 0.5; EX1014, 3, 6.)

30. The textbook *Semiconductor Physics and Devices – Basic Principles*, explains this conventional operation, including explanation of both "n-type" and "p-type" options:

> There are four basic MOSFET device types. Figure 10.34 shows an n-channel enhancement mode MOSFET. Implicit in the enhancement mode notation is the idea that the semiconductor substrate is not inverted directly under the oxide with zero gate voltage. **A positive gate voltage induces the electron inversion layer, which then "connects" the n-type source and the n-type drain regions**. The source terminal is the source of carriers that flow through the channel to the drain terminal. For this n-channel device, electrons flow from the source to the drain so the conventional current will enter the drain and leave the source. **The conventional circuit symbol for this n-channel enhancement mode device is also shown in the figure**.
>
> Figure 10.35 shows an n-channel depletion mode MOSFET. An n-channel region exists under the oxide with 0 V applied to the gate.

However, we have shown that the threshold voltage of a MOS device with a p-type substrate may be negative; this means that an electron inversion layer already exists with zero gate voltage applied. Such a device is also considered to be a depletion mode device. The n-channel shown in the figure can be an electron inversion layer or an intentionally doped n region. **The conventional circuit symbol for the n-channel depletion mode MOSFET is also shown in the figure**.

Figures 10.36a, b show a p-channel enhancement mode MOSFET and a p channel depletion mode MOSFET. In the p-channel enhancement mode device, **a negative gate voltage must be applied to create an inversion layer of holes that will "connect" the p-type source and drain regions**. Holes flow from the source to the drain, so the conventional current will enter the source and leave the drain. A p-channel region exists in the depletion mode device even with zero gate voltage. **The conventional circuit symbols are shown in the figure.**

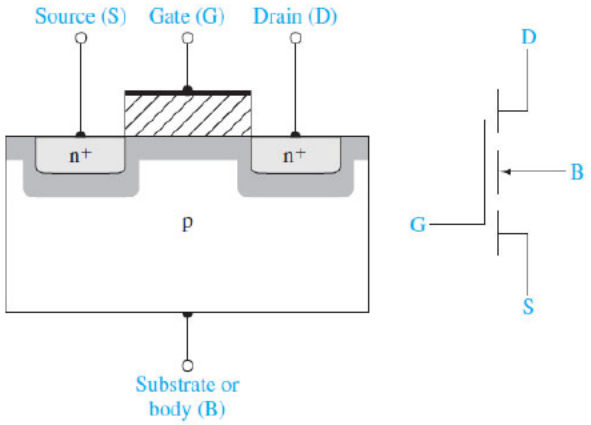


Figure 10.34 | Cross section and circuit symbol for an n-channel enhancement mode MOSFET.

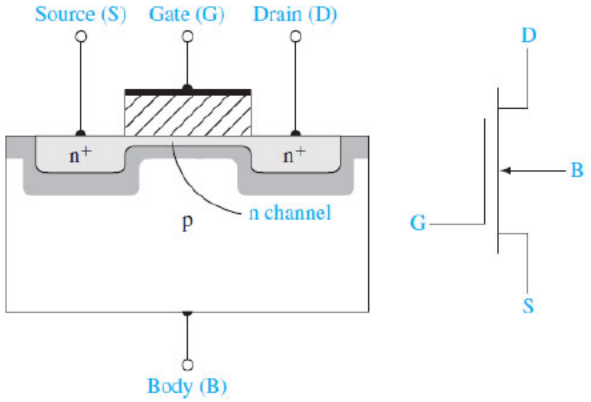


Figure 10.35 | Cross section and circuit symbol for an n-channel depletion mode MOSFET.

EX1012, Figures 10.34 and 10.35

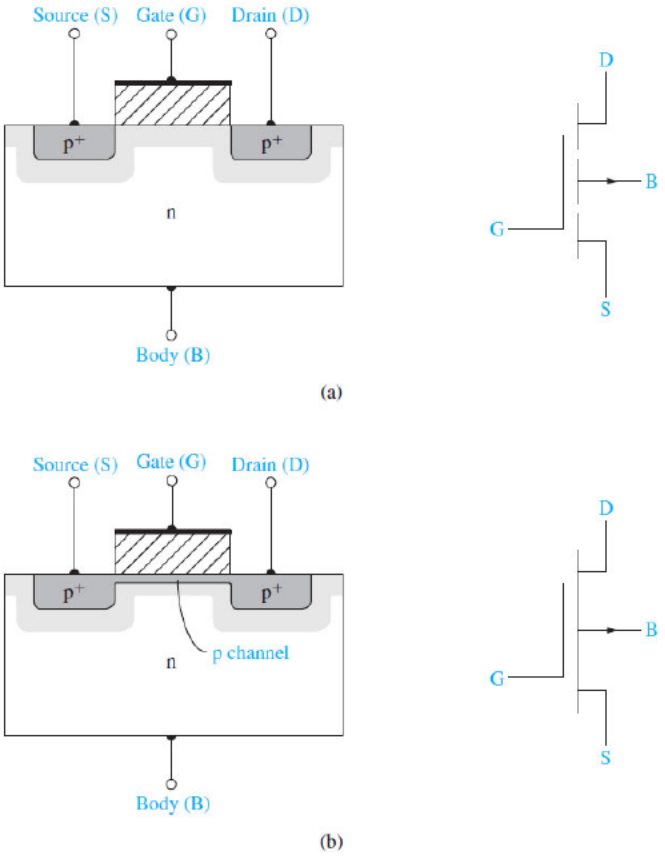
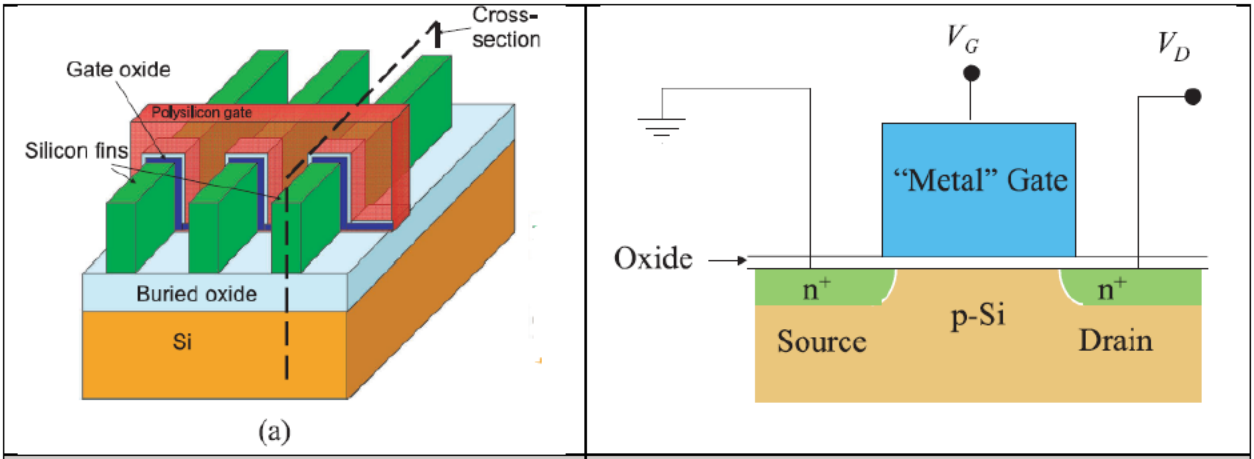


Figure 10.36 | Cross section and circuit symbol for (a) a p-channel enhancement mode MOSFET and (b) a p-channel depletion mode MOSFET.

EX1012, Figure 10.36

EX1012 (*Semiconductor Physics and Devices – Basic Principles*, 4th Ed. (2011)), pp. 403-05.

31. Two types of FETs known in the art at the relevant time include a planar FET (for example, a planar MOSFET) and a non-planar three-dimensional (3D) FET (for example, a FinFET, tri-gate transistor). FinFETs and tri-gate transistors are examples of non-planar MOSFETs.



EX1020, Figure 9.41 (FinFET) | **EX1020, Figure 3.20 (planar MOSFET)**

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 351, 72-74.)

32. Further, inter-layer dielectric layers (ILDs) were known features of IC structures that were typically disposed on the wafer/substrate between features (for example, metal gates) in the IC structure. EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 370-71.

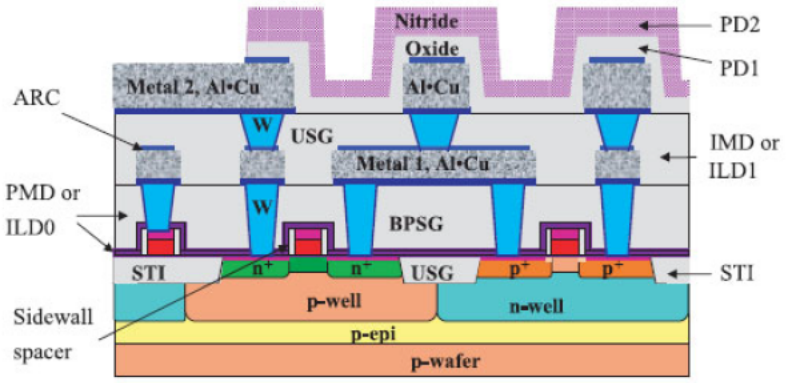


Figure 10.2 Applications of dielectric thin film in a CMOS circuit with Al–Cu interconnection.

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 371, FIG. 10.2 (showing ILD filling space between features); *see also* EX1005 (Pethe), FIG. 2C, 5:7-10 (inter-layer dielectric layers 270)).

33. Likewise, it was known that FET structures were formed with a source/drain region, typically disposed between respective metal gates of the structure. *Above*; EX1023, 433-34, FIG. 3; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 351, 72-74.

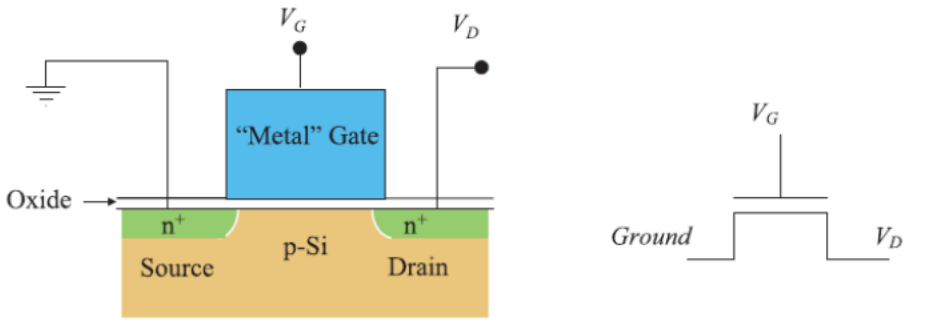


Figure 3.20 An nMOS transistor.

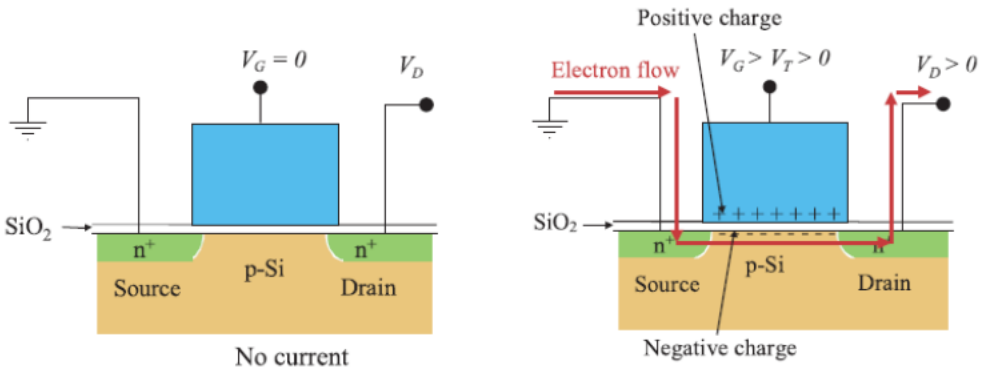


Figure 3.21 Switching process of the nMOS.

EX1020, Figures 3.20 and 3.21

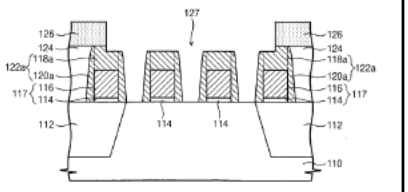
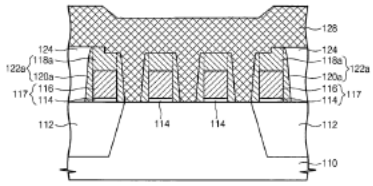
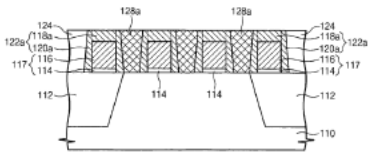
34. EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 72-73 ("In a CMOS circuit, both nMOS and pMOS are used"); *see also* EX1005

(Pethe), 3:19-20 (diffusion region), 3:25-28 (source or drain contacts disposed over source and drain regions), 3:31-46 and 3:60-64 (diffusion region), 4:27-32 (diffusion region), 4:33-36 ("source and drain regions").

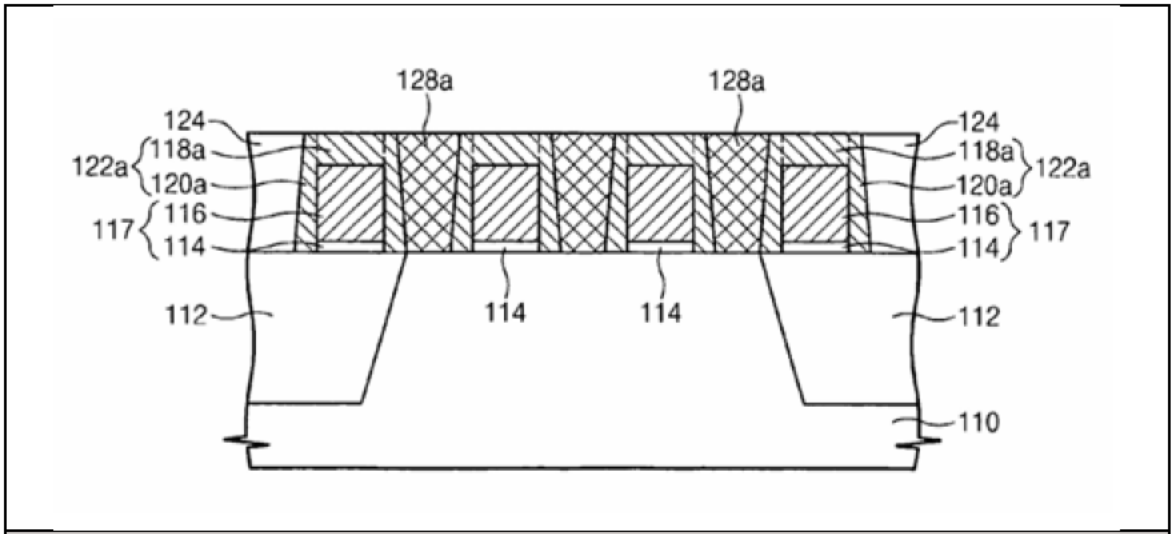
B. Self-Aligned/Shared Contacts

35. In ICs, transistors are interconnected in various arrangements through contact plugs and interconnection structures. (EX1001, 1:17-21 (Description of Prior Art).) With "the continuous miniaturization of… IC[s], the line width of interconnections and the feature sizes of semiconductor devices… continuously shrunk." (*Id*., 1:14-17.) Making electrical contacts to such miniaturized devices was a known challenge. (EX1018, 1:36-65.)

36. Before the '747 patent's filing, self-aligned contacts (SAC) was a conventional and well understood technique to form contacts to such miniaturized devices. (*Id.*, 1:66-2:13, 2:55-56; EX1024 (US2009/0155991 (Lee)), ¶¶5, 64-68, FIGs. 3D-3F (showing formation of SAC 128a).) In SAC, "after forming an opening that simultaneously exposes gates of a region requiring a contact plug and a semiconductor substrate between the gates, a conductive layer is deposited to fill the opening," and the conductive layer (for example, metal) is then planarized. (EX1024, ¶6.)

Fig. 3D	Fig. 3E	Fig. 3F
		
Lee, Figure 3D (showing formation of openings)	Lee, Figure 3E (showing filling of openings with conductive layer)	Lee, Figure 3F (showing planarization of conductive layer)

37. SACs were known to use cap layers, otherwise known as hard masks, to cover and protect the gate during formation of the contact opening to features such as the source/drain. (EX1024 (US2009/0155991 (Lee)), ¶7.)



EX1024 (Lee), FIG. 3F

38. For some IC structures, such as static random-access memory (SRAM), for example, it was known to implement shared contacts, which are single contacts connecting together two transistor features, such as a source/drain and a gate.

(EX1025 (US20090014796 (Liaw)), ¶3, 42-43, FIG. 1 (butted contact 10), FIG. 8C (contact B).)

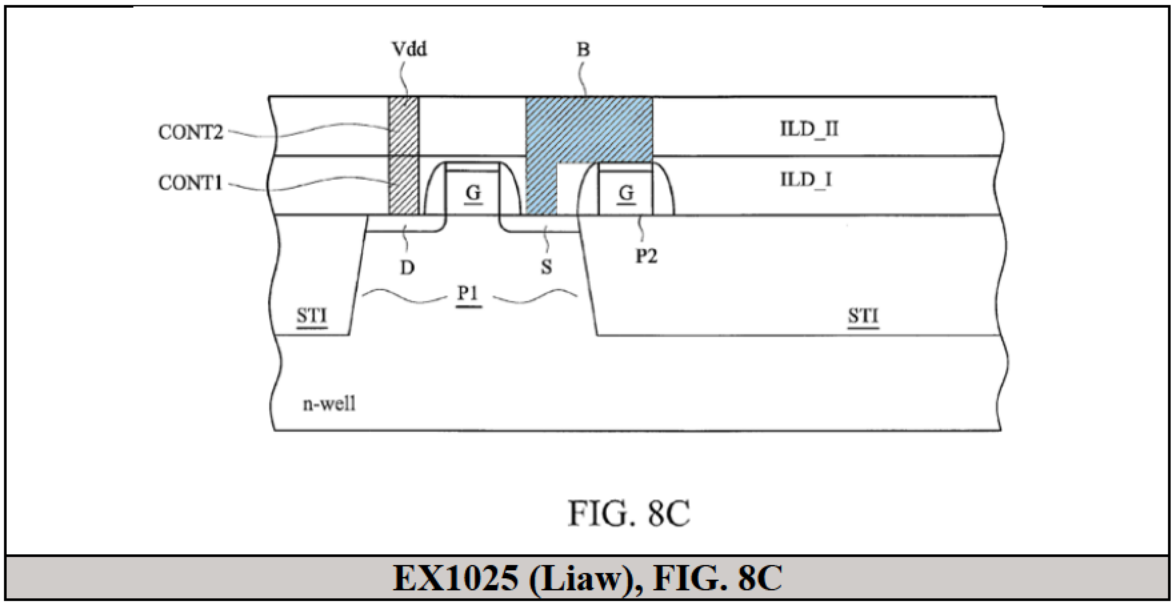


FIG. 8C

EX1025 (Liaw), FIG. 8C

39. Such shared contacts (for example, as shown in EX1025 at FIGs. 1, 8C) were a known way to "mak[e] electrical connection… where high device density is desired, such as an embedded SRAM and DRAM cell area, thus, reducing the [IC] die area and enhancing device reliability." (EX1025, ¶3; *see also* EX1027, 5:59-6:18 (disclosing use of shared contact in SRAM), FIG. 4 (shared contact 82).)

C. Planarization

40. Before and around the time of the alleged invention, and still today, semiconductor device processing, including semiconductor device contacting, was known to include a planarization step. Such planarization steps could, for example, include etching steps and/or chemical mechanical planarization (CMP) steps.

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 511-514.) In fact, before the '747 patent's filing, CMP had been long-established in the IC industry for planarizing the surface of semiconductor structures. (EX1026, 1-2 (explaining that "CMP became a mainstream process at and below the 0.35um technology node" in "1995"). CMP, consistent with its name, is a removal process that employs chemical and mechanical means to planarize the surface of a semiconductor structure/wafer.

41. Planarizing etchback processes for recessing transistor gates/spacers in ILD was also known. EX1028, 4:37-60, 7:4-53, Figs. 1A, 2A-2C; EX1029, 4:37-5:6, 7:48-8:37, Figs. 1B, 2A-2C.

42. Chapter 12 of EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 507-48) summarizes CMP as follows:

> CMP is a removal process that strips small portions of film deposited on a wafer by a combination of chemical reaction and mechanical polishing, thus making the surface smoother and more planarized. It is also used to remove bulk dielectric film on the surface to form STI on the silicon substrate, and remove bulk metal film from the wafer surface to form metal interconnection lines or plugs in the dielectric film. This chapter covers CMP processes.

43. The following provides a high-level overview of CMP:

> After the 1980s, more than two metal layers were required to connect the increasing number of transistors in IC chips. One of the great

challenges was planarization of the dielectric layers between the metal layers. It is very difficult to achieve high-resolution photolithography on a rough surface due to the DOF requirements of optical systems. A rough dielectric surface can also cause problems in metallization because metal PVD processes usually do not have good sidewall step coverage. Thinner metal lines on the sidewall have a higher current density and are more vulnerable to electromigration issues.

Figure 12.1 shows a brief summary of the IC manufacturing flow and makes it clear that CMP is a very important part of the process. Wafers come to CMP from a thin-film process, either dielectric or metal thin-film deposition. In most cases, wafers are transported out of the CMP bay into a photo bay or thin-film bay. Dielectric CMP is followed by either photolithography or metal thin-film deposition, and metal CMP is only followed by dielectric thin-film deposition.

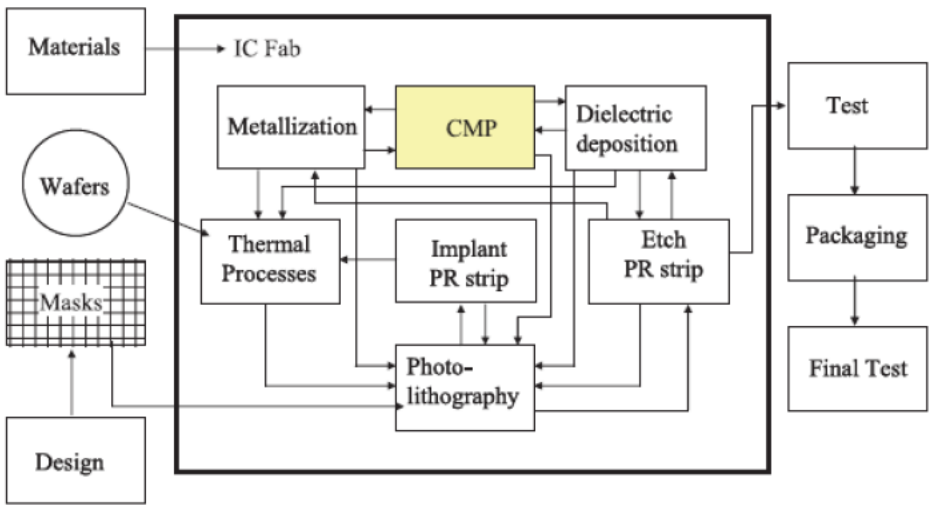


Figure 12.1 CMP applications in IC manufacturing flow.

EX1020, Figure 12.1

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), p. 508.)

D. Metal Interconnect (BEOL)

44. After individual transistors are fabricated and contacted, through a SAC, for example, BEOL (Back-End-of-Line) processes are used to interconnect the transistors to form an IC. Such interconnection has conventionally (including long before the '747 patent's filing), been performed using a "dual-damascene" process where metal lines and vias are formed simultaneously in order to connect to a lower level. (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 19, 345-49, 453, 464, 517-18; EX1014, pp. 696-98; EX1015, pp. 55-56.) This process involves depositing metal in an etched geometry representing the shape of the metal lines and vias, and then removing the excess metal using CMP.

45. In order to interconnect the up to billions of transistors on modern ICs, by the relevant time it became necessary to provide multiple metal layers. (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), p. 570; EX1014, 559.) It was well known that to provide such metals layers, a "dual damascene process is repeated multiple times, depending on how many metal layers there are" (i.e., M2/V1, M3/V2, etc.). (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 19, 345-49, 570; EX1014, pp. 696-98.) As explained in EX1020 (*Introduction to Semiconductor Manufacturing Technology*, pp. 570), back-end process transitioned to copper interconnections around the turn of the century:

> After MOS transistors are formed on the wafer surface, the wafer process is approximately half done. The front-end process is finished, while the back-end process has just begun. For an advanced IC chip, **multiple metal layers with dielectric material in between are required to route millions or billions of transistors**. Silicide is commonly used to improve conductivity of local interconnections and reduce contact resistance. For many devices that do not require more than a gigahertz (GHz) of clock frequency (such as most DRAM and flash memory devices), tungsten and aluminum alloys are still widely used in metallization processes, along with undoped silicate glass (USG) as the dielectric. At the turn of the century, interconnection technology made a transition from traditional tungsten and aluminum alloy interconnections to copper interconnections for high-speed (clock frequency >1 GHz) CMOS logic devices.

46. As I explain further in Grounds 4 and 7, the advantages of the dual-damascene process, including in large part the avoiding of any metal etch, helped drive the transition to copper interconnections:

> "In the **back-end of the line (BEoL) process**, all photolithography processes are followed by etch processes. **In copper metallization, this dual damascene process is repeated multiple times, depending on how many metal layers there are**: dielectric CVD, photolithography, dielectric etch, photoresist strip and clean, photolithography, dielectric etch, photoresist strip and clean, deposition of metal layers, metal anneal, and CMP. After all of the metal layers are formed, CVD silicon oxide and silicon nitride are deposited as the

> passivation layer, and the last photolithography process defines the pads for wire bonding or bump formation. After that, the chips are tested, die sawed, sorted, packaged, burned-in, and shipped to customers."

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), p. 19).

VI. THE '747 PATENT

A. Description

47. The '747 patent relates to a semiconductor manufacturing process and resulting semiconductor structure. (EX1001, Abstract, 1:7-11.) The '747 patent purports to address alleged drawbacks of prior structures where a barrier layer is formed between an upper contact structure (i.e., metal level zero M0) and a lower contact structure that are formed in different steps. (*Id.*, 1:22-41.) Namely, the '747 patent describes a semiconductor device 1 formed through manufacturing process described in the patent like that shown in Figure 9 below. (*Id.*, 5:66-6:37.)

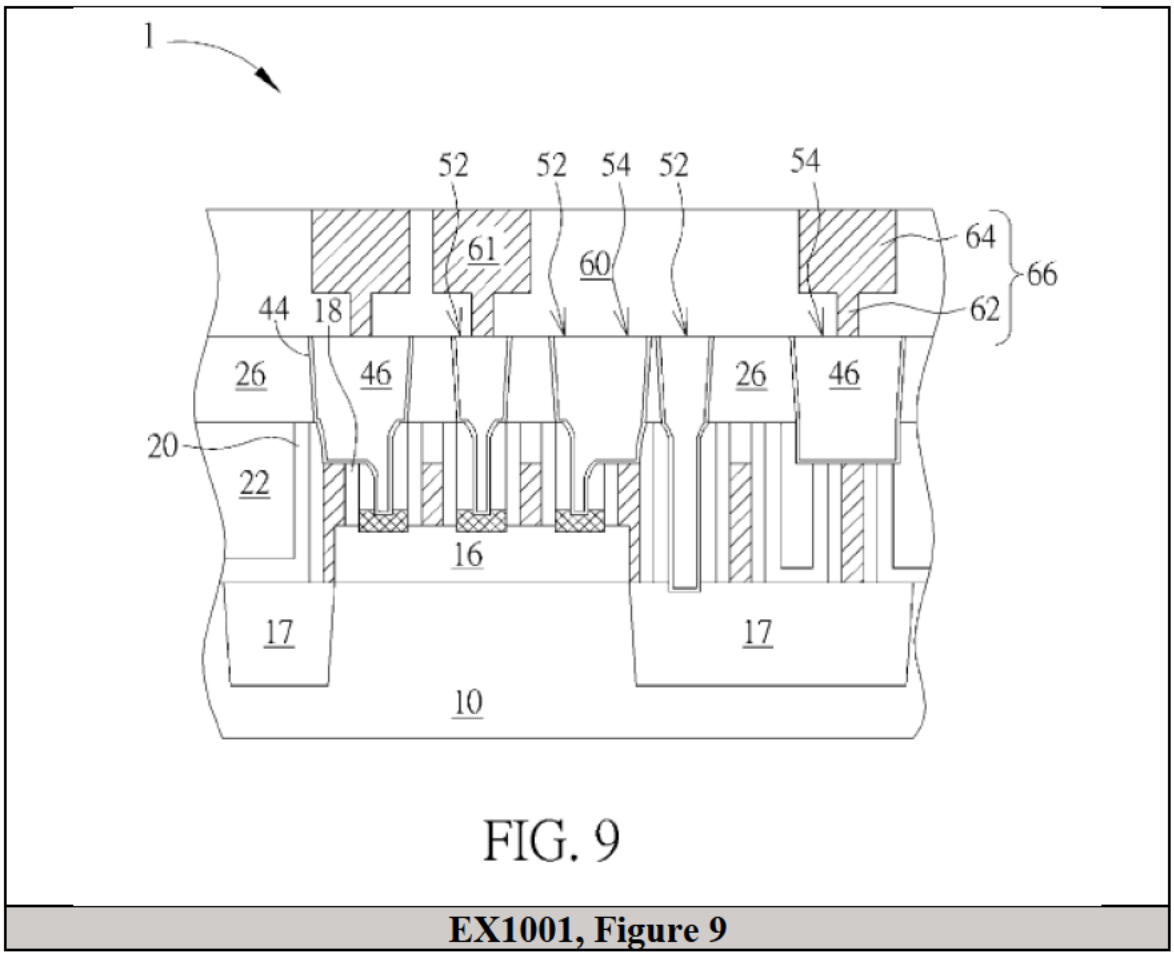


FIG. 9

EX1001, Figure 9

(*Id.*, FIG. 9.)

48. Device 1 includes a substrate 10, first dielectric layer 22 disposed on substrate 10, metal gate 12 disposed in the first dielectric layer 22, a source/drain (S/D) region 14 disposed on two sides of the metal gate 12, and a hard mask 24 disposed on the metal gate 12, where the top surface of the hard mask 24 and the top of the first dielectric layer 22 are on the same level, a second dielectric layer 26 disposed on the first dielectric layer 22. The device 1 further comprises a plurality of first contacts 52 disposed in the first dielectric layer 22 and in the second dielectric layer 26 electrically connected to parts of the S/D region 14, where each first contact

52 is a monolithically formed structure, and a plurality of second contacts 54 disposed in the first dielectric layer 22 and in the second dielectric layer 26 electrically connected to parts of the metal gate 12, wherein each second contact 54 is a monolithically formed structure. (*Id.*, 6:2-18.)

B. The Prosecution History

49. I reviewed the prosecution history of the '747 patent (EX1004). It is my understanding that during prosecution before the U.S. Patent and Trademark Office (Office), there were several amendments presented by the applicant in response to rejections by the Office. (*See generally* EX1004.) For example, during prosecution of the application that issued as the '747 patent, in response to prior art rejections by the Examiner, the pending claims were first amended to include the now claimed spacer with a truncated top surface features (*id.*, 93-110), and later amended to include what is now features claimed in the challenged claims, such as the claimed first and second contacts, metal gate, and S/D features (*id.*, 134-144.) I understand that following another amendment (*id.*, 146-159), the pending claims of the application were allowed (*id.*, 169-171) and later the '747 patent issued.

VII. OVERVIEW OF THE PRIOR ART

A. Pethe

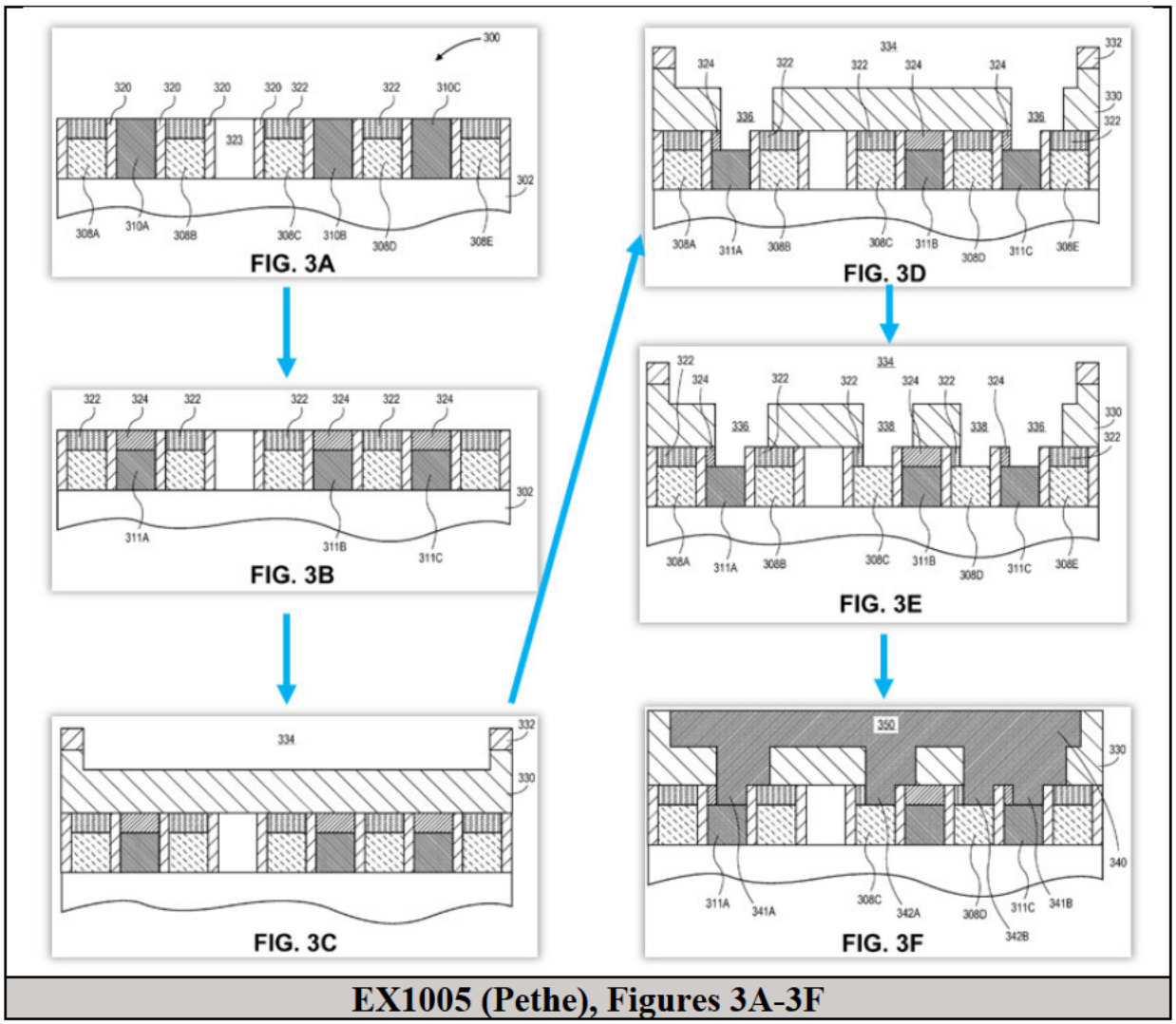
50. Pethe discloses semiconductor devices, including MOS transistors (MOSFETs) having gate contact structures disposed over active portions of gates

and methods of forming such structures. (EX1005 (Pethe), 2:50-52, 2:50-3:10, 7:9-11:42, 12:22-13:12, 14:4-11.) A POSITA would have understood that Pethe is in the same field (MOSFETs) and reasonably pertinent to a problem the '747 patent purports to address (e.g., MOSFET fabrication). (EX1001, 1:9-2:9, 2:39-42, 5:31-6:37; EX1005, 2:50-3:10, 7:9-11:42, 12:22-13:12, 14:4-11.)

51. As Pethe explains, "well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention." (*Id*., 2:55-62.)

52. Pethe discloses a semiconductor structure in FIG. 3F. The fabrication steps that result in the structure of Figure 3F are shown in Figures 3A-3F. (EX1005 (Pethe), 7:9-16).

53. I sometimes refer to this semiconductor structure as the "Figure 3 Embodiment."



EX1005 (Pethe), Figures 3A-3F

(EX1005 (Pethe), FIGs. 3A-3F, 2:8-27, 7:9-11:42.)

54. According to one feature of Pethe, as shown in Figure 3E, Pethe performs etching processes to create openings 336, 338, and metal (0) trench 334. (EX1005 (Pethe), 9:1-11:42, FIGs. 3D-3F.)

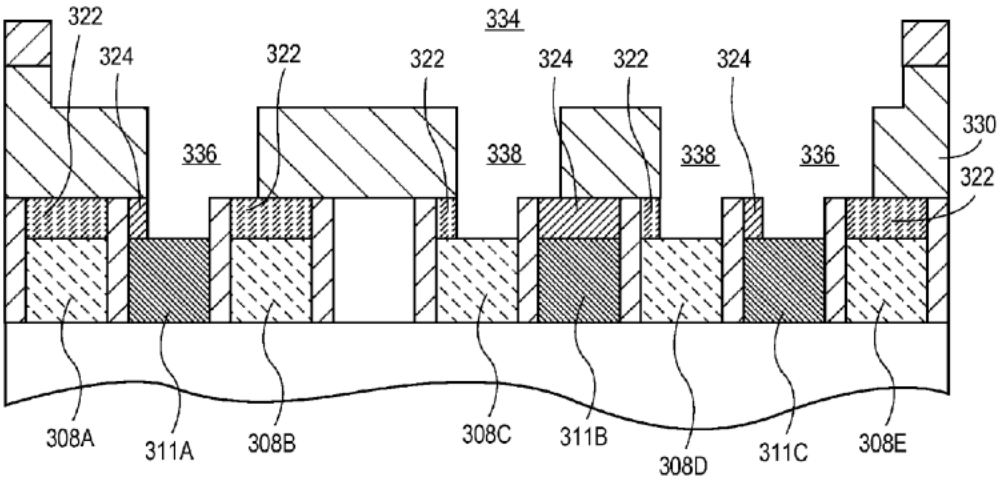


FIG. 3E

EX1005 (Pethe), Figure 3E

55. Pethe then performs a single metal fill process to fill the entire region of openings 336, 338, and metal (0) trench 334 to form the metal contact structure 340, including a metal (0) portion 350 along with trench contact vias (trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively) and gate contact vias (gate contact vias 342A and 342B to gate stack structures 308C and 308D, respectively). (EX1005 (Pethe), 11:23-42.)

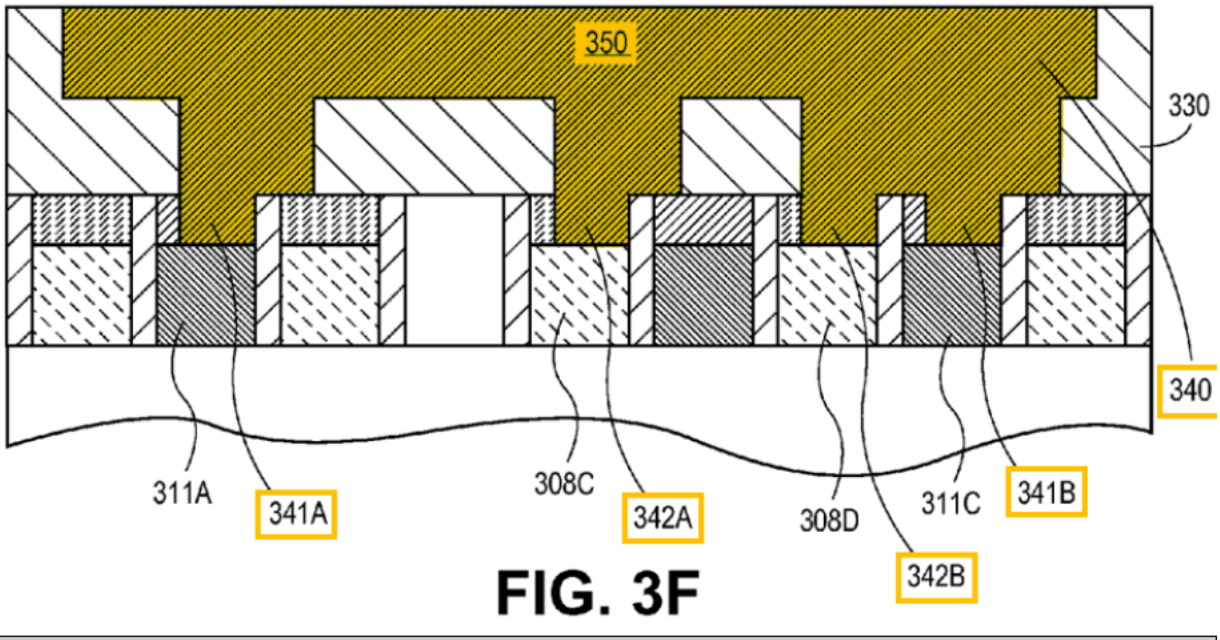


FIG. 3F

EX1005 (Pethe), Figure 3F

56. Pethe also discloses a semiconductor structure as shown in Figure 5B, the fabrication of which is shown collectively in FIGs. 5A-5B. (EX1005 (Pethe), 2:32-36, 12:32-33.)

57. I refer to this semiconductor structure as the "Figure 5 Embodiment."[2]

[2] As I explain below in §IX, my opinions concerning how Pethe discloses or suggests the limitations of the challenged claims is based on this Figure 5 embodiment. As I also explain below, Pethe does not repeat discussions of certain features in the Figure 5 embodiment that overlap with the Figure 3 embodiment shown in Figures 3A-3F, but a POSITA would have understood those features as described are likewise disclosed in the Figure 5 embodiment disclosures.

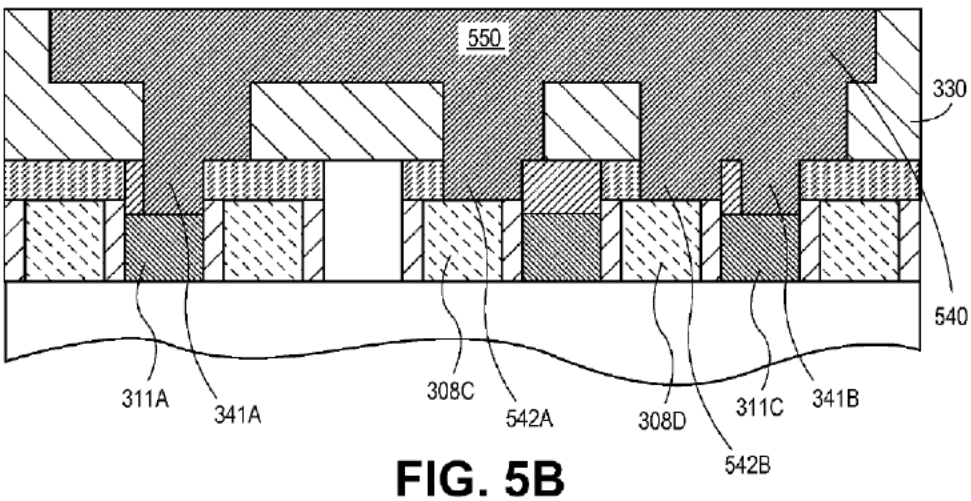


FIG. 5B

EX1005 (Pethe), Figure 5B

58. Pethe's-Figure-5-Embodiment is similar to Pethe's-Figure-3-Embodiment, except, Pethe's-Figure-5-Embodiment's spacers are "recessed" unlike in Pethe's-Figure-3-Embodiment. For instance, Pethe explains that unlike the Figure-3-Embodiment, in the Figure-5-Embodiment "the spacer may be **recessed** to be essentially **planar** with the gate structures." (*Id.*, 12:22-26, 12:48-53 ("**in contrast to the structure 300** described in associated with FIG. 3A, **the spacers 520 have been recessed** to approximately the same height as the gate stack structures 308A-308E,").)

59. Pethe's Figure 5B structure also includes a cap layer 522 (the same as the cap layer 322 but wider because of the recessed spacers 520). Pethe's Figure 5B structure also includes gate contact vias 542 and metal portion 550 (the same as the

gate contact vias 342 and the metal portion 350 but extending deeper because of the recessed spacers 520).

60. Both Figure 3 and 5 embodiments starting structures 300 and 500 respectively are "provided following trench contact (TCN) formation." (EX1005 (Pethe), 7:15-16, 12:32-33.) Pethe's-Figure-5-Embodiment also relies on earlier disclosures from Pethe's-Figure-3-Embodiment (*id.*, 12:37-48 (referring to gate stack structures 308A-308E, substrate 302, gate dielectric layer and gate electrode (in connection with Figure 2), and trench contacts 310A-310C, coupled with similar features associated with Figure 5A (structure 500, spacers 520, cap layer 522).)

61. In other words, Pethe teaches forming contact structures to form the structures of Figures 3F and 5B from 3A and 5A, respectively. (for example, EX1005 (Pethe), 7:9-14, 12:26-31.) In order to "arrive at" the structures of Figures 3A and 5A, Pethe teaches a "a dummy and replacement gate process in combination with a dummy and replacement contact process," and incorporates Golonzka for such teachings. (for example, EX1005 (Pethe), 7:15-8:23, 12:32-39.)

62. Given Pethe's reliance on many features associated with Pethe's-Figure-3-Embodiment in describing Pethe's-Figure-5-Embodiment, my opinions and analysis below relies on disclosures from Pethe's-Figure-3-Embodiment that overlap with the features disclosed in Pethe's-Figure-5-Embodiment to demonstrate how, in my opinion, Pethe's-Figure-5-Embodiment meets claim 1-9 in Grounds 1-

4. (*Id.*, ¶IX.) It is also apparent that the fabrication process of 3A to 3F is the same as that of 5A to 5B, as shown below. However, because the differences in the Pethe Figure 3 and 5 Embodiments are confined to a particular feature (the spacers, discussed below), Pethe does not repeat its Figures 3B-3E and related discussion for the Pethe-Figure-5-Embodiment. Accordingly, a POSITA would have understood that these teachings disclosed with the Pethe-Figure-5-Embodiment.

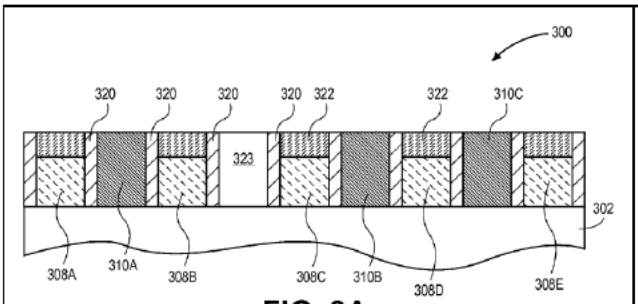


FIG. 3A

Pethe, Figure 3A

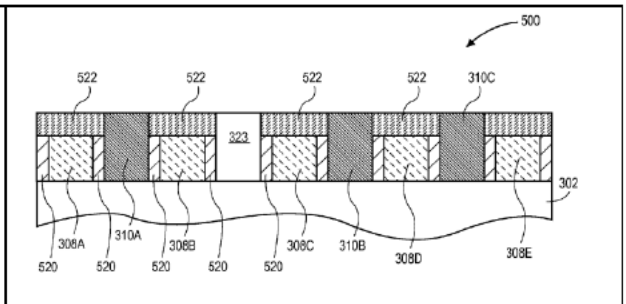


FIG. 5A

Pethe, Figure 5A

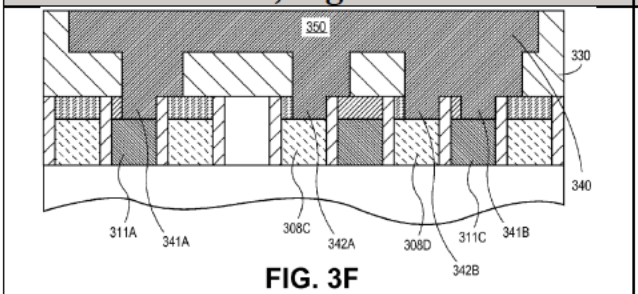


FIG. 3F

Pethe, Figure 3F

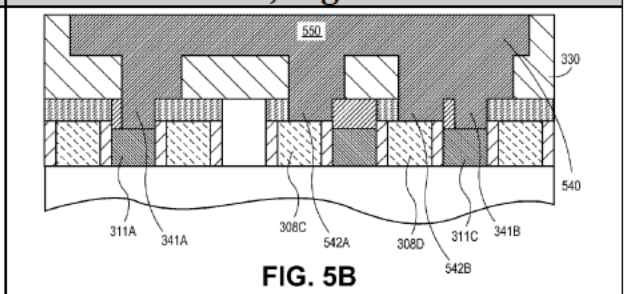


FIG. 5B

Pethe, Figure 5B

63. Both Pethe's-Figure-3-Embodiment and Pethe's-Figure-5-Embodiment rely on disclosures from Figure 2's Embodiment to describe the Figure 3 and 5 Embodiment's structure. (EX1005 (Pethe), 7:22-25, 12:39-41.)

B. Chang

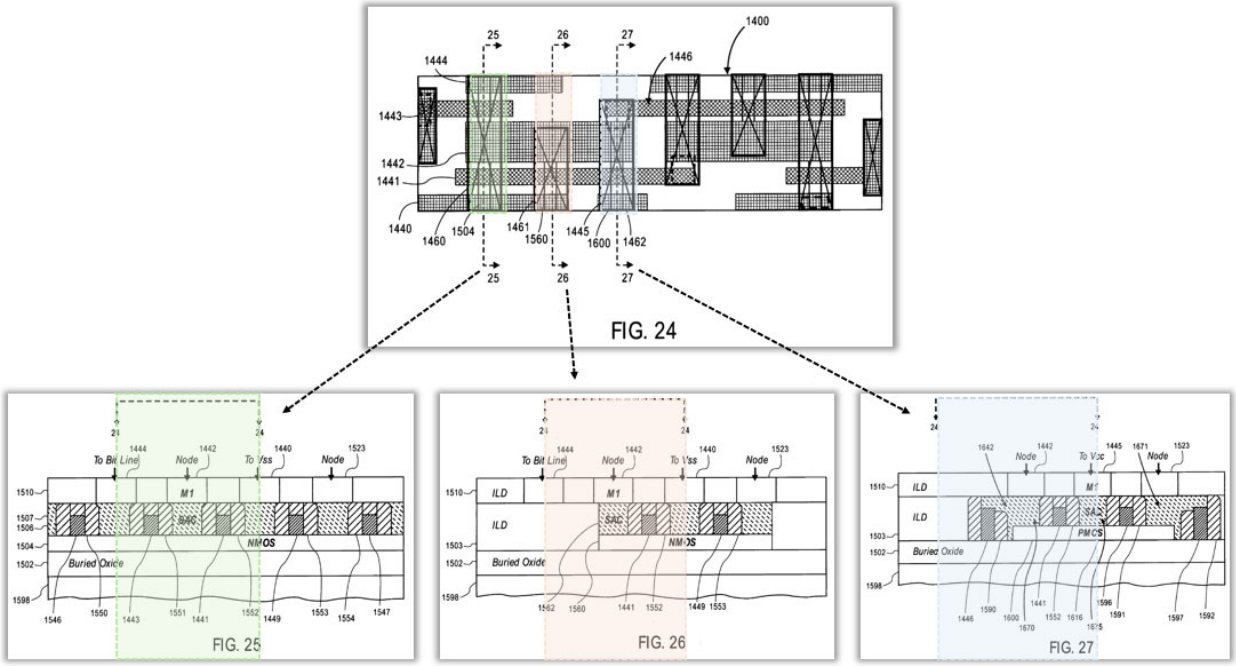
64. Chang teaches an "SRAM containing transistor structures with gate-protected self-aligned contacts" in Figures 24-27. (EX1007 (Chang), ¶107.) The transistor structures in Chang's SRAM include MOSFETs. (*Id*., ¶1, 27-35, 46-49, 52, 89-92, 107-114.) A POSITA would have understood that Chang is in the same field (MOSFETs) and reasonably pertinent to a problem the '747 patent purports to address (e.g., MOSFET fabrication). EX1001, 1:9-2:9, 2:39-42, 5:31-6:37; EX1007, ¶¶27-35, 46-49, 52, 89-92, 107, 111-114.

65. The SRAM of Figures 24-27 is disclosed in the context of Chang's "self-aligned contacts" with a "gate-protection option," which Chang explains "is described with respect to FIGS. 17-27." (EX1007 (Chang), ¶[0052].)[3] Specifically, "FIGS. 17 through 23 show wafer cross sections that illustrate operations in connection with the gate-protect option with respect to forming self-aligned contacts" (*Id*., ¶89) and "FIG. 24 is a top view of a layout 1400 of an SRAM containing transistor structures with gate-protected self-aligned contacts… cross sections of the SRAM layout 1400 are shown in FIGS. 25, 26, and 27." (*Id*., ¶107.)

[3] Chang discloses an alternative "no gate-protect option … in reference to FIGS. 6 through 16." (EX1007 (Chang), ¶0051.)

66. A POSITA would have thus understood that the teachings of Figure 17-23 are methods and operations for the SRAM of Figures 24-27. Specifically, Figures 17-23 illustrate forming the self-aligned contacts, and Figures 24-27 show an SRAM with those contacts.

67. Figures 25-27 show three cross-sections of the SRAM structure in Figure 24, as I have depicted below:



VIII. CLAIM CONSTUCTION

68. I understand that when considering the meaning of patent claims, one must consider the language of the claims, the specification, and the prosecution history of the patent. I also understand that claim terms are typically given their ordinary and customary meanings as would have been understood by a person of ordinary skill in the art at the time of the invention for the patent. For the '747 patent,

as I explained above in Section IV, the relevant time that I have been asked to consider is around May 2, 2013. For purposes of my opinions in this declaration, I have been asked to consider the challenged claims under their plain and ordinary meanings as understood by a person of ordinary skill in the art at the time of the alleged invention in context of the '747 patent as I discussed above, and I have applied such understandings in my analysis of the '747 patent and the prior art.

IX. THE PRIOR ART DISCLOSES AND/OR SUGGESTS ALL THE RECITED FEATURES OF CLAIMS 1-9 OF THE '747 PATENT

A. Ground 1: Pethe Discloses (Ground 1A) and Suggests (Ground 1B) Claims 1-5, and 8

69. My opinions below in Grounds 1-4 explain and show how Pethe's Figure 5B structure discussed in the embodiment in connection with FIGs. 5A-5B discloses and/or suggests limitations of the identified challenged claims.

70. As I previously noted, because Pethe relies on many features disclosed with respect to Pethe's-Figure-3-Embodiment to describe Pethe's-Figure-5-Embodiment, my analysis below relies on disclosures from Pethe's-Figure-3-Embodiment that overlap with the features disclosed in Pethe's-Figure-5-Embodiment to demonstrate how Pethe's-Figure-5-Embodiment meets claim 1-9 in Grounds 1-4.

71. It would have also been apparent to a POSITA that the fabrication process of 3A to 3F is the same as that of 5A to 5B, as shown below. However,

because the differences in the Pethe-Figure-3 and 5 Embodiments are confined to a particular feature (the spacers, discussed below), Pethe does not repeat its Figures 3B-3E and related discussion for the Pethe's-Figure-5-Embodiment. Accordingly, a POSITA would have understood that these teachings are also disclosed in connection with the Pethe's-Figure-5-Embodiment (in particular the Figure 5B structure).

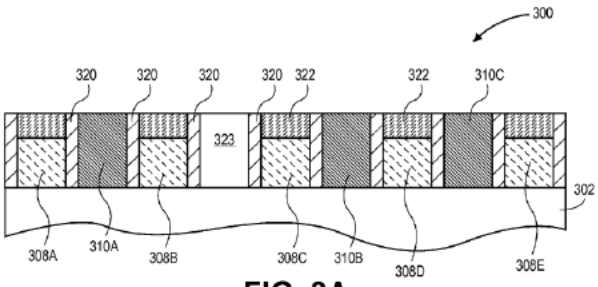


FIG. 3A

Pethe, Figure 3A

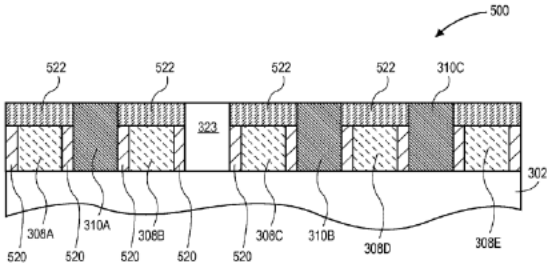


FIG. 5A

Pethe, Figure 5A

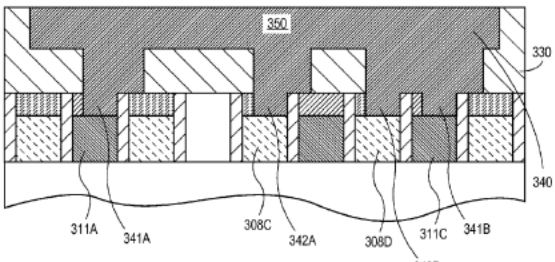


FIG. 3F

Pethe, Figure 3F

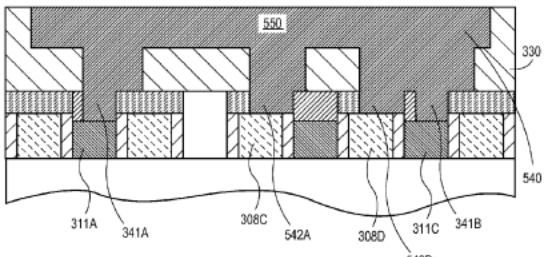


FIG. 5B

Pethe, Figure 5B

1. Claim 1

a) A semiconductor structure, comprising:

72. In my opinion, Pethe's Figures 5A-5B embodiment ("Pethe's-Figure-5-Embodiment") discloses **[a] semiconductor structure**, as shown in the following limitations [1.b] through [1.i].

73. In particular, Pethe discloses **[a] semiconductor structure** in the FIG. 5B structure, and in the fabrication steps that result in the structure of Figure 5B as shown in FIGs. 5A-5B. (EX1005 (Pethe), 2:32-36, 12:32-33.)

74. I sometimes refer herein to this **semiconductor structure** (namely the Figure 5B structure) in Grounds 1-4 in context of the "Figure 5 Embodiment."

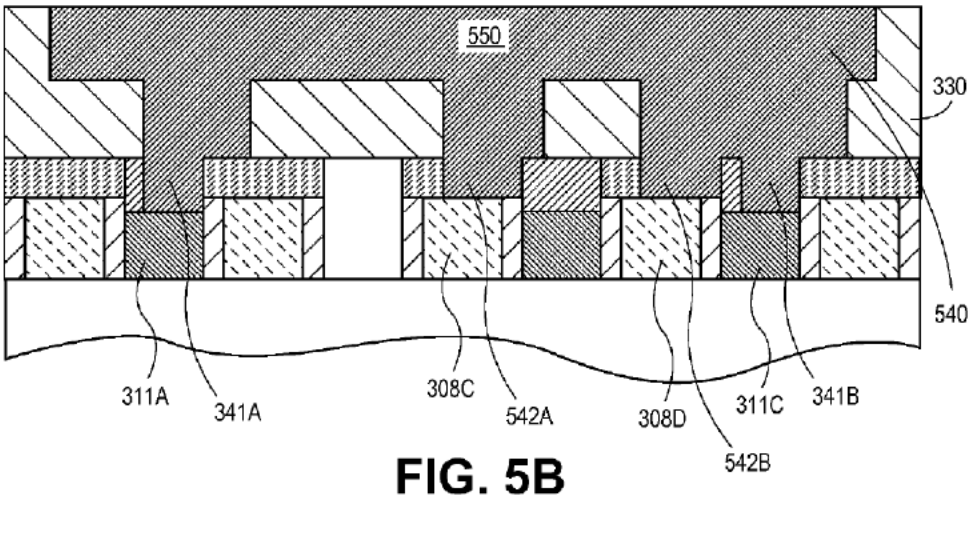


FIG. 5B

EX1005 (Pethe), Figure 5B

75. As discussed above and shown below, the Figure 5B structure has undergone the fabrication steps of Figures 3B-3E.

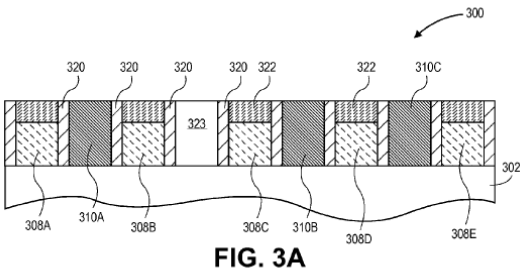


FIG. 3A

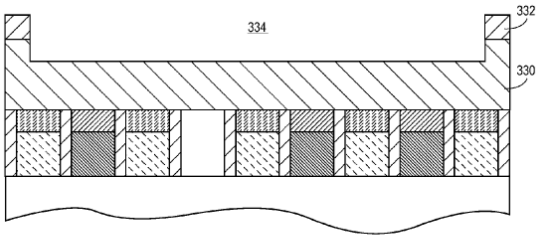


FIG. 3C

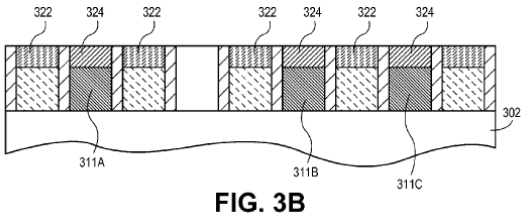


FIG. 3B

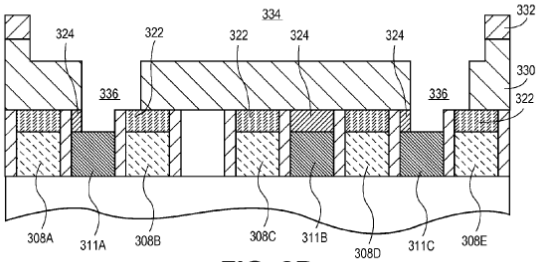


FIG. 3D

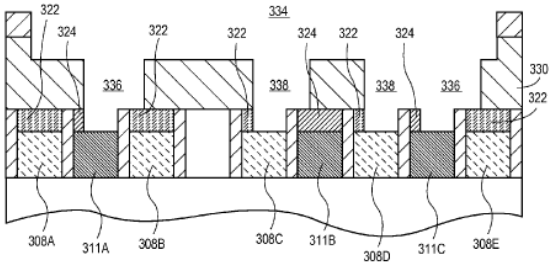


FIG. 3E

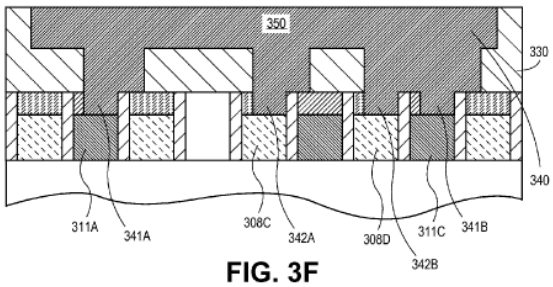


FIG. 3F

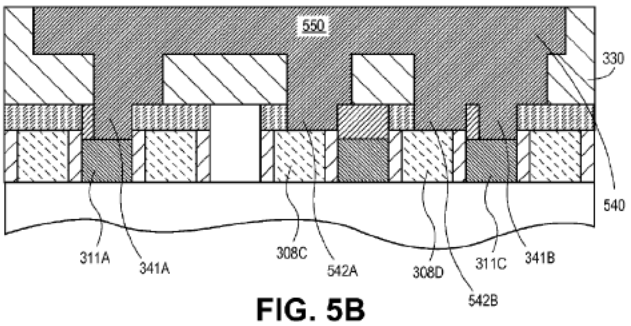


FIG. 5B

(EX1005 (Pethe), FIGs. 3A-3F, 5B, 2:8-27, 7:9-11:42, 12:15-67.)

b) a substrate;

76. In my opinion, Pethe discloses this limitation.

77. For example, Pethe's substrate 302 in the Figure 5B structure is **a substrate**.

78. The following annotated Figures 5A and 5B that show how Pethe discloses a substrate, which is labeled 302 in Figure 5A, and would be understood to likewise associate to the structure in Figure 5B (colored in blue):

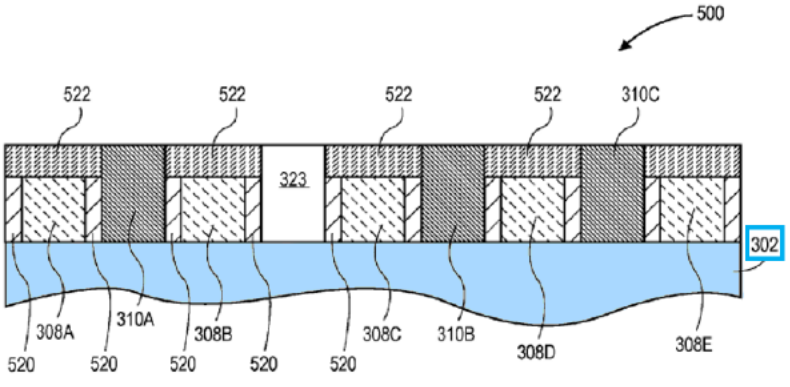


FIG. 5A

EX1005 (Pethe), Figure 5A

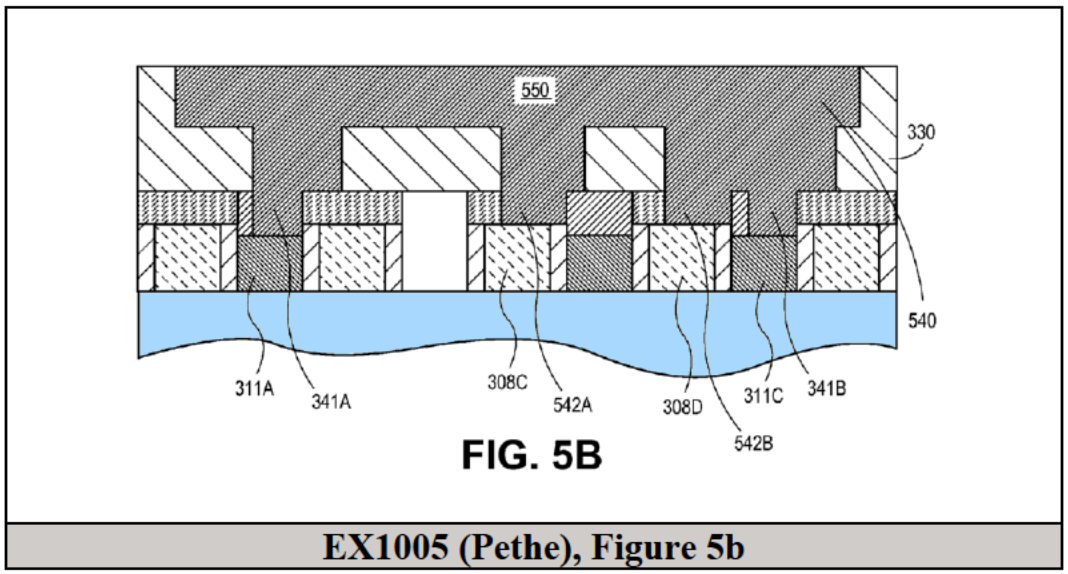


FIG. 5B

EX1005 (Pethe), Figure 5b

(EX1005 (Pethe), 12:37-45; *see also* for FIG. 3 embodiment 7:20-27; FIGs. 3B-3E.)

c) a first dielectric layer disposed on the substrate;

79. In my opinion, Pethe discloses this limitation.

80. Pethe discloses an inter-layer dielectric layer that includes a region 323 shown in the Figure 5B structure. The inter-layer dielectric layer is the first dielectric layer. (EX1005 (Pethe), FIGs. 5B, 3F, *see also id.*, FIGs. 5A, 3A-3E.)

81. Pethe discloses "contact blocking **regions**…, such as region 323 fabricated from ***an inter-layer dielectric material***, may be included in **regions** where contact formation is to be blocked." (in other words, fills spaces where no gate structure or source/drain contact). (EX1005 (Pethe), 7:31-34.)

82. Thus, in my opinion, Pethe's Figure 5B structure includes contact blocking regions (of which region 323 is a part and fabricated with inter-layer

dielectric material (*See above*)) is a **dielectric layer** (hereinafter "Pethe's first dielectric layer").

83. The following annotations of Figures 5A and 5B show how Pethe discloses this limitation (where I identify region 323 in red in both structures of Figures 5A and 5B):

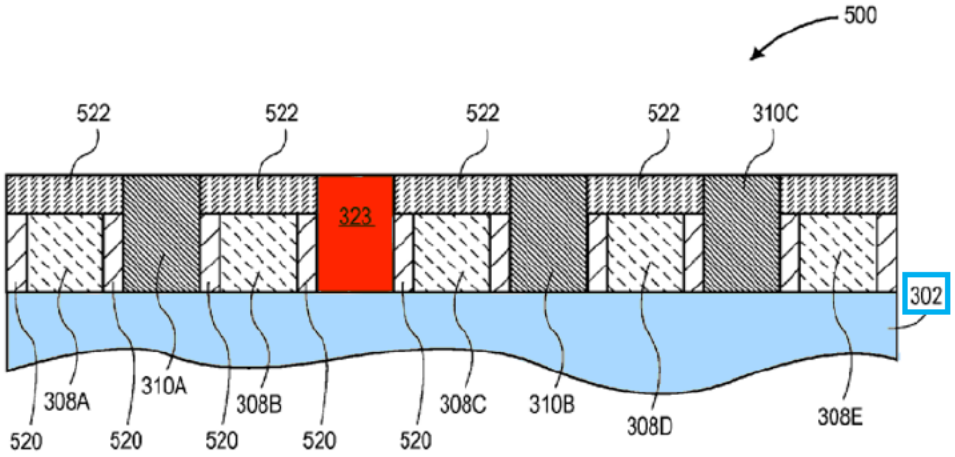


FIG. 5A

Pethe, Figure 5A

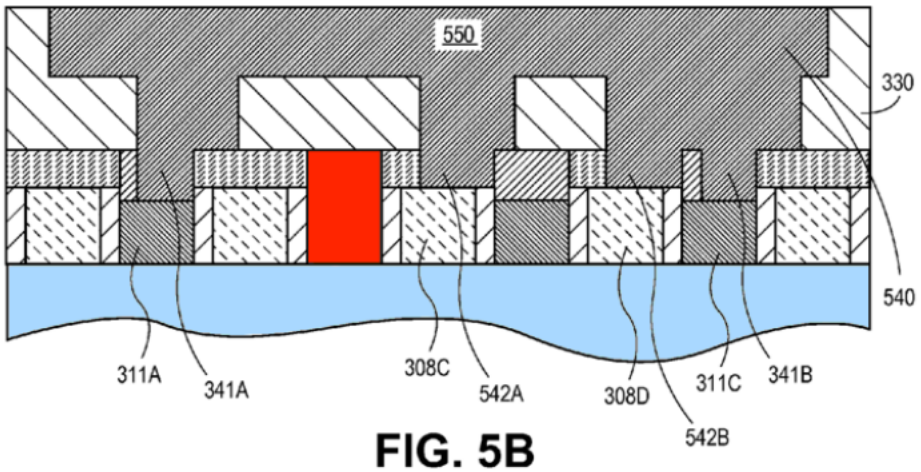


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 12:32-53, 7:31-34.)

84. Region 323 is a **layer**. Region 323 (which is not labeled in Figure 5B, but a POSITA would have understood to be the same layer) is described by Pethe as "an inter-layer dielectric" (also known as an "ILD"), which were known by a POSITA to be a layer. (EX1005 (Pethe), 7:31-34.)

85. A POSITA understood that ILDs were well-known well before the time of the '747 patent to be an insulating (dielectric) material that is deposited as a **layer**. This understanding is consistent with Pethe's disclosures, which likewise explains that this layer is "included in regions where contact formation is to be blocked," which a POSITA would have understood that it fills the spaces where there is no gate or source/drain contact. (EX1005 (Pethe), 7:31-34.)

86. Pethe first introduces ILD region 323 in Figure 3A, as part of structure 300, and describes subsequent fabrication steps, moving next to Figure 3B and ending with the structure shown in Figure 3F. (See for example, EX1005 (Pethe), 7:11-14.) In describing structure 300 of Figure 3A and an exemplary fabrication thereof (the process to "arrive at" structure 300 in Figure 3A, and ultimately the "structure" of Figure 3F), Pethe incorporates by reference PCT/US 2011/066989 ("Golonzka".) (EX1005 (Pethe), 7:35-8:23.)

87. Golonzka's "first permanent interlayer dielectric portion" 128/ "second permanent interlayer dielectric portion" 132 are formed by "deposition and

planarization," which a POSITA would have understood to mean it is a deposited and planarized **layer**. (EX1006, ¶¶0042-0045, 0047, 0050.)

88. Accordingly, in my opinion, Pethe's first dielectric layer (of which inter-layer dielectric material of region 323 is a part) in the Figure 5B structure is **disposed on the substrate** (substrate 302). Further, Pethe explains that "gate stack structures 308A-308E [are] **disposed above a substrate 302**,"[4] and, region 323 and gate stack structures 308A-308E are identically positioned with respect to substrate 302. (EX1005 (Pethe), 12:37-39, 7:20-34, 12:39-13:12; FIG. 3A.) For similar reasons, the structure of Figure 5B also includes gate stack structures 308A-308E that are **disposed above a substrate 302**, which are identically positioned with respect to substrate 302.

89. Pethe's region 323 in Pethe's-Figure-5-Embodiment and Pethe's-Figure-3-Embodiment are the same for purposes of this limitation, as I show below in connection with the intermediate FIGs. 3A and 5A structures to the final FIGs. 3F and 5B "structure[s]").

90. Pethe identifies ILD region 323 in Figures 5A and 5B in the same manner (in other words, same location and same numerical reference number) as in Figure 3 (shown below).

[4] I provide emphasis in this declaration unless I note otherwise.

91. In my opinion and experience, when a patent uses the same name and reference number in different Figures for an element, the text disclosures describing the element for one Figure apply to the element on the other Figures, as they are the same element (unless otherwise noted). In my opinion, a POSITA would have understood the same in Pethe's discussion of the Figure 5B structure in the Figure 5 embodiment, which references same elements discussed for the Figure 3 embodiment.

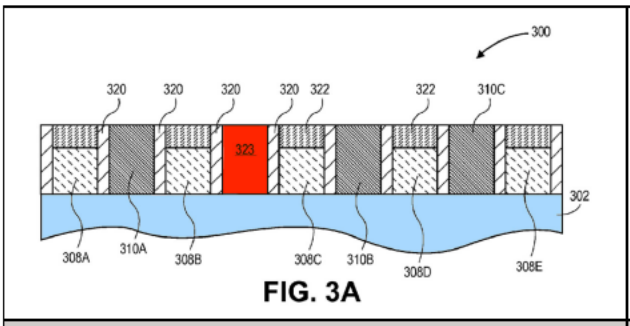


FIG. 3A

EX1005 (Pethe), Figure 3A

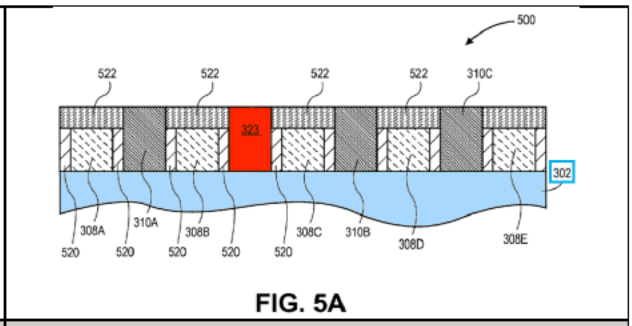


FIG. 5A

EX1005 (Pethe), Figure 5A

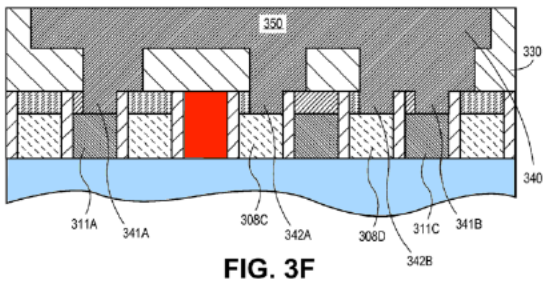


FIG. 3F

EX1005 (Pethe), Figure 3F

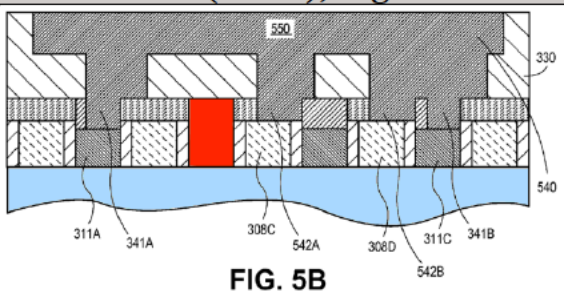


FIG. 5B

EX1005 (Pethe), Figure 5B

92. Pethe's inter-layer dielectric (of which region 323 is a part of) in Pethe's-Figure-5-Embodiment, like in Pethe's-Figure-3-Embodiment, is disposed on the substrate (302). (EX1005 (Pethe), 12:37-39, 7:20-34, 12:39-13:12; FIG. 3A.)

d) at least two metal gates disposed in the first dielectric

layer;

93. In my opinion, Pethe discloses this limitation.

94. For example, Pethe's "gate stack structures 308A-308E" in the Figure 5B structure comprise five **metal gates** (which is **at least two**), as I show in the following annotated versions of Figures 5A and 5B.

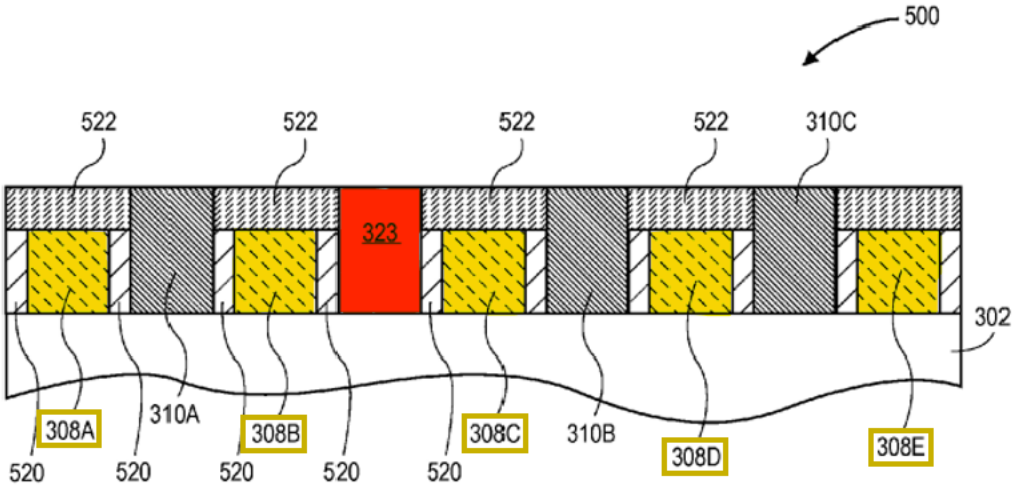


FIG. 5A

Pethe, Figure 5A

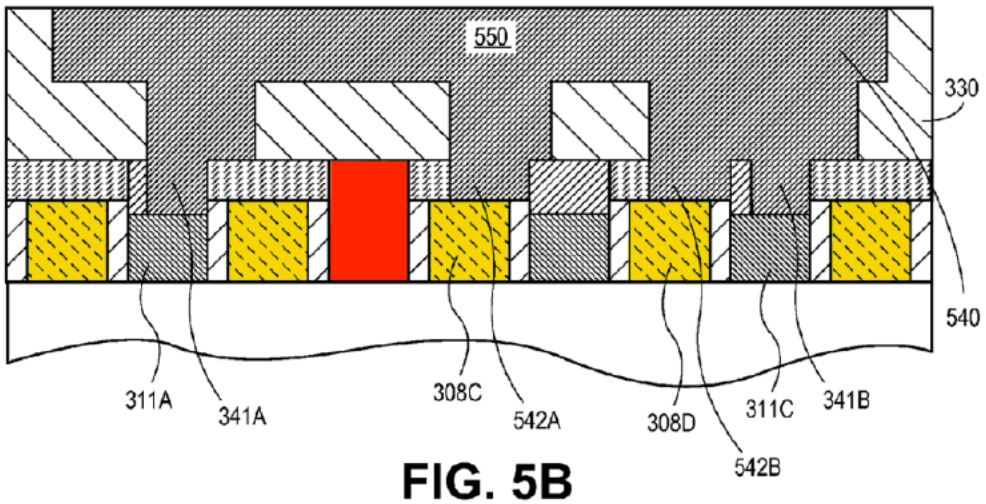


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 12:32-53, also for the Figure 3 embodiment, 7:20-34.)

95. Gate stack structures 308A-308E are **metal**. Pethe in the Figure 5 Embodiment explains that "[t]he gate stack structures may include a gate dielectric layer and a **gate electrode**, as described above in association with FIG. 2." (EX1005 (Pethe), 12:39-42.)

96. In the above statement, Pethe incorporates Figure 2 for its discussion of the gate dielectric layer and gate electrode. In Figure 2, as directed in Figure 5, Pethe explicitly states that "the gate electrode is composed of a **metal** layer." (EX1005 (Pethe), 6:37-44.)

97. Additionally, Figure 5A's "structure 500, which has its gate stack structures fully formed, "is provided following trench contact (TCN) formation." (EX1005 (Pethe), 12:32-53.) The TCN process is used to form both structure 500 in Figure 5A (*Id*.) and structure 300 in Figure 3A (*Id.*, 7:15-34) and is described by Pethe's incorporated Golonzka (EX1005, 7:35-8:11), which further confirms that the "gate electrode… is composed of a **metal** gate." (EX1006, ¶0049.)

98. Pethe's gate stack structures 308A-308E in FIG. 5B's structure **are disposed in the first dielectric layer (of which region 323 is a part)**. As shown in the annotated Figure 5A above, gate stack structures 308A-308E (also in the structure of Figure 5B) are **disposed in the first dielectric layer (of which region 323 is a part)**. A POSITA would have understood that Pethe's teachings on the

relationship of metal gates and first dielectric layer is similar to how such features are described in the '747 patent (on the right), as I show below in relation to Pethe's Figure 5B (on the left):

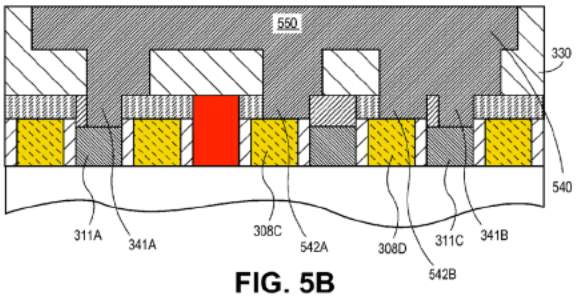


FIG. 5B

Pethe, Figure 5B

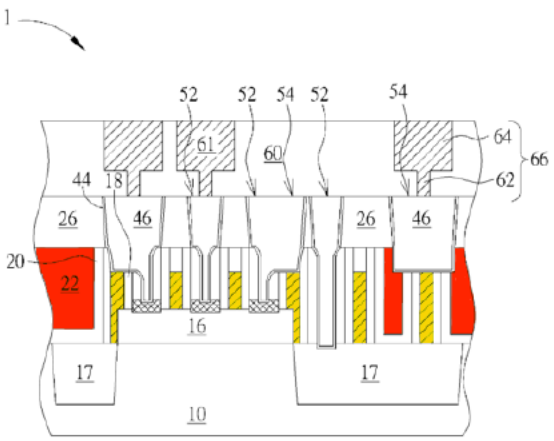


FIG. 9

'747 Patent, Figure 9

(EX1001, 5:66-6:5.)

99. As explained, the first dielectric layer (of which region 323 is a part) (Pethe's first dielectric layer) is blanket deposited on the substrate and fills the spaces where there is no gate structure and no contact (i.e., "regions where contact formation is to be blocked"), meaning the metal gates are disposed in the first dielectric layer. EX1005 (Pethe), 7:31-34; §IX.A.1.c.

100. The disclosure of incorporated Golonzka, which describes the TCN process used to form Figure 5A's 500 structure including fully formed gate structures, further confirms the disposition of the metal gates in the ILD. (*See* EX1005 (Pethe), 12:32-37, 7:15-41; *See above* §IX.A.1.c; EX1006, ¶¶0044-0049

(explaining the gate is formed disposed in the layer comprising interlayer dielectric 132), FIG. 1J (annotated below showing metal gates 138 within dielectric 132), FIGs. 1I, 1K, 2.) Accordingly, the resulting Figure 5B structure includes at least two metal gates disposed in the first dielectric layer as claimed.

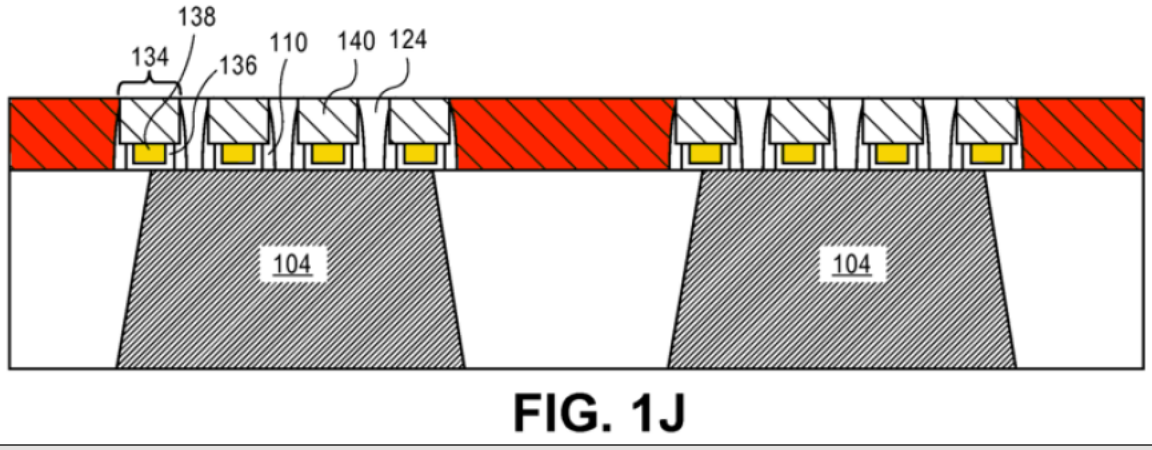


FIG. 1J

Golonzka, Figure 1J

101. As I explained above for element [1c] (*section* § IX.A.1.c), Pethe's first dielectric layer (of which region 323 is a part) fills the spaces where there is no contact formation (*i.e.*, is "included in regions where contact formation is to be blocked"), which a POSITA would have understood to mean that the **metal gates** are **disposed in** the first dielectric layer (**of which region 323 is a part)** including in the Figure 5B structure. (EX1005 (Pethe), 7:31-34.)

102. In addition, Pethe's teachings are consistent with the knowledge of a POSITA at the time that ILDs are dielectric layers providing insulation.

e) a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

103. In my opinion, Pethe discloses this limitation.

104. For example, Pethe's spacers 520 (**a spacer**) in the Figure 5B structure, (*see also* Figure 5A), are **disposed on two sides of** each gate stack structure 308A-308E of Figure 5B's structure (any one or more being **the metal gate**).

105. The following annotations of Figures 5A and 5B exemplify how Pethe discloses this limitation:

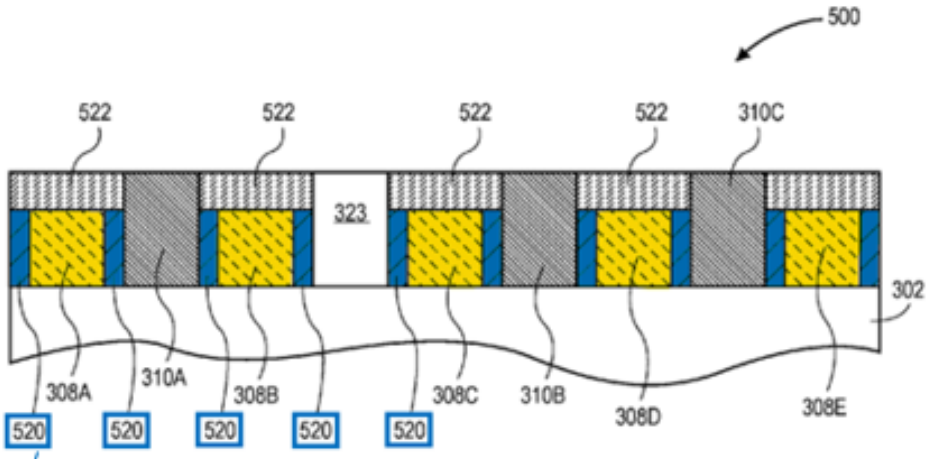


FIG. 5A

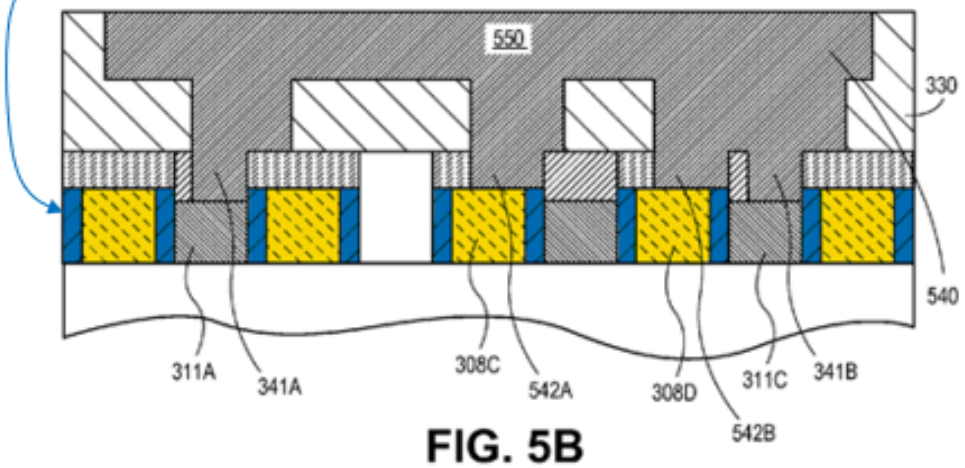


FIG. 5B

(EX1005 (Pethe), 12:42-53, 12:22-31, FIGs. 5A-5B.)

106. Pethe explains that the trench contacts 310A-310C (in Figure 5A) and 311A-311C (in Figure 5B) are "spaced apart from gate stack structures 308A-308E by dielectric spacers 520." (EX1005 (Pethe), 12:42-45.)

107. A POSITA would have understood Pethe discloses that trench contacts 310A-310C (shown in annotated Figure 5A) "are recessed" to become recessed trench contacts 311A-311C (shown in annotated Figure 5B below). (EX1005 (Pethe), 13:1-12.)

108. In my opinion, and as I explain further below, Pethe's spacer 520 in Figure 5B's structure **has a truncated top surface**.

109. Pethe describes spacers 520 in its Figure 5 Embodiment, in relation to spacers 320 in its Figure 3 Embodiment. Specifically, Pethe explains that "in contrast to the structure 300 described in associated with FIG. 3A, the spacers 520 have been **recessed** to approximately the same height as the gate stack structures 308A-308E." (EX1005 (Pethe), 12:48-53, 12:22-31.) Pethe shows these "**recessed**" spacers 520, in the annotated Figures 5A/5B in relation to Figures 3A/3F below, as shortened with the spacers' top portions (i.e., portions depicted above gate electrodes 308A-308E) removed from the spacers 520 in the Figure 5 Embodiment but not removed from the spacers in the Figure 3 Embodiment.

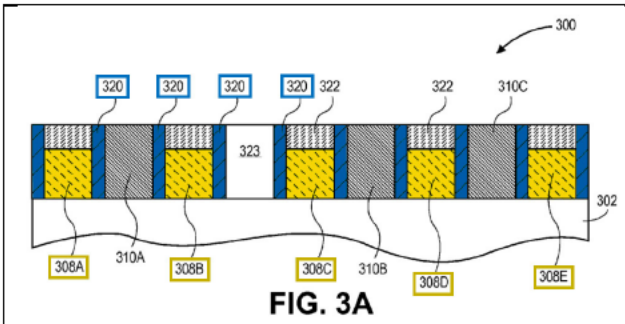


FIG. 3A

Pethe, Figure 3A

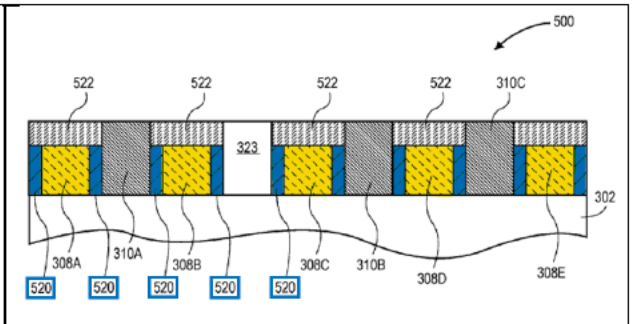


FIG. 5A

Pethe, Figure 5A

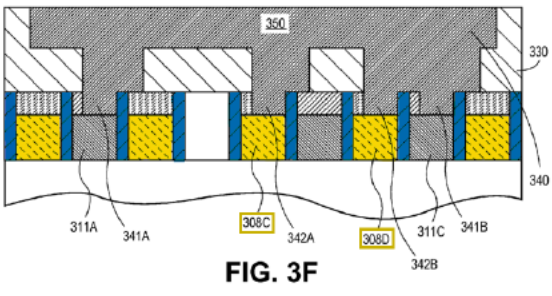


FIG. 3F

Pethe, Figure 3F

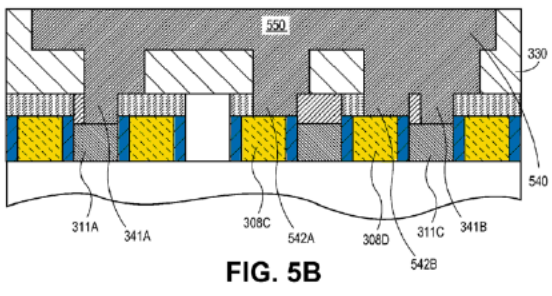


FIG. 5B

Pethe, Figure 5B

110. Pethe's explanation that "spacers 520 have been **recessed**" further confirms that the spacer 520's top surface has been **truncated** by etching or other processes. (EX1005 (Pethe), 12:15-31.)

111. Pethe generally uses the terminology "recessed" to connote that a given feature has been truncated by etching (or another process) to remove material from the feature's top surface. For example, trench contacts 310A-310C (annotated Figure 5A) "are recessed" to become recessed trench contacts 311A-311C (annotated Figure 5B below). (EX1005 (Pethe), 13:1-12.) These contacts "may be recessed by... **an etch process** such as a wet etch process or dry etch process," to remove trench contact material from the trench contacts' top surface. (EX1005 (Pethe), 8:24-51, 13:1-12.) It was well known to use planarizing etch processes to recess gates/spacers in ILD. §V.C.

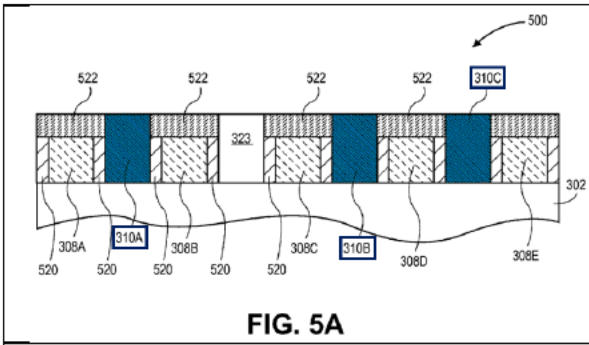


FIG. 5A

Pethe, Figure 5A

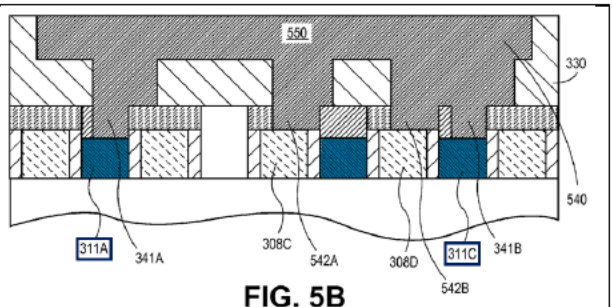
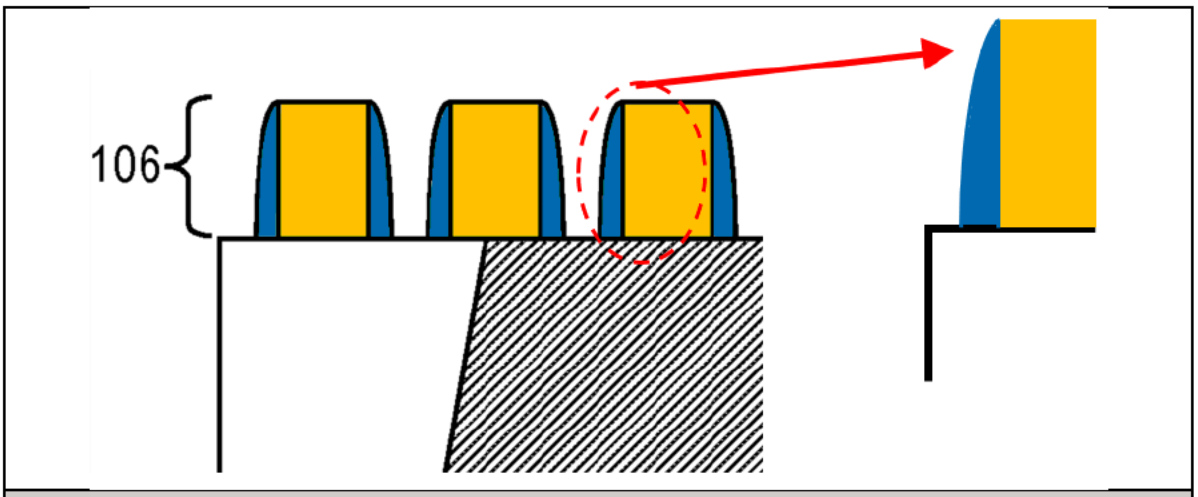


FIG. 5B

Pethe, Figure 5B

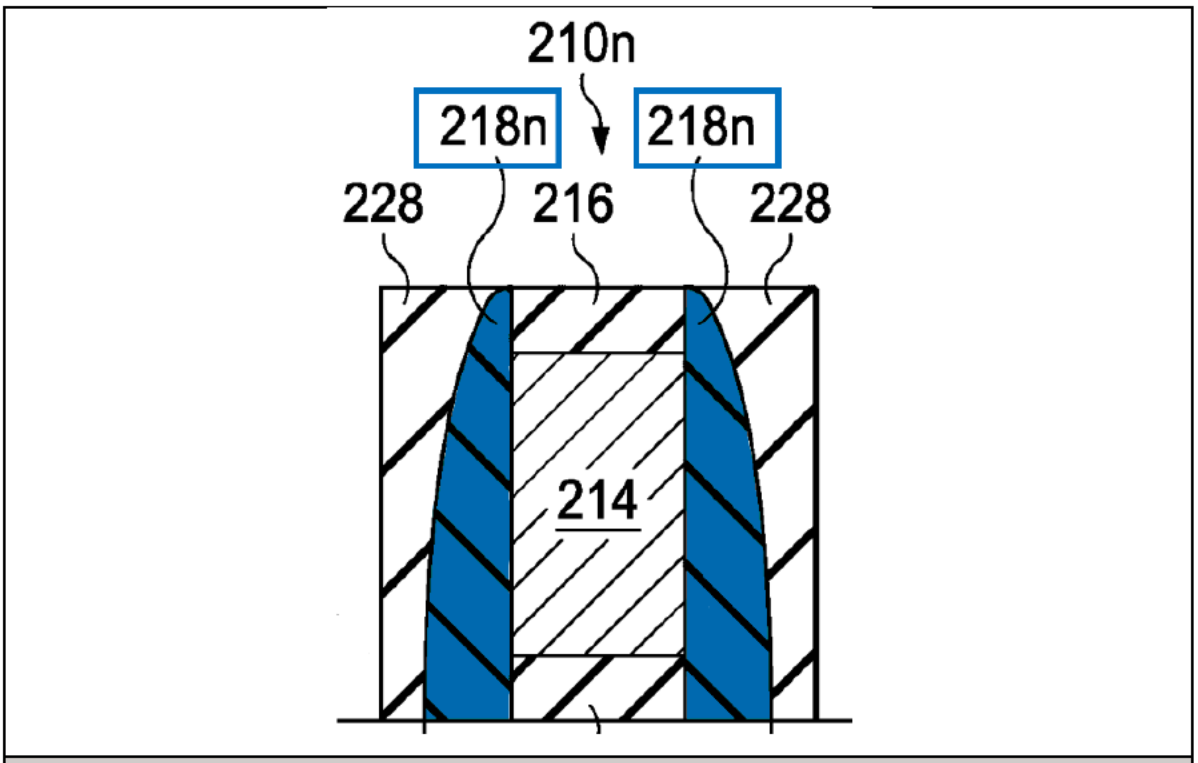
112. Pethe's spacers have been "recessed to be essentially **planar**," meaning that the recessing is a planarizing process. (EX1005 (Pethe), 12:22-31.) Figures 5A-5B depicts spacers 520 as planar, further consistent with Pethe's-Figure-5-Embodiment's disclosure of spacer 520 having a **truncated top surface**. A POSITA would have understood where the **top surface** of each spacer 520 is "recessed" to a lower height (same height as gate stack structures 308A-308E) and "planar," it is **truncated**.

113. My opinion that the spacer(s) in Pethe's Figure 5 structure in the Figure 5 Embodiment has a truncated top surface is further confirmed by the disclosure of incorporated Golonzka, which discloses the spacers do not have a planar top surface, as initially formed. (EX1006, ¶0030.) Instead, they are formed with their top surface sloping downward from the gate edge, as shown in annotated Golonzka FIG. 1A below. (EX1006, FIGs. 1A-1K, 2.) As shown below, the spacer top surface is rounded, not planarized:



EX1006 at Fig. 1A (annotated.)

114. I have reviewed the file history of the '747 patent (EX1004). In doing so, I understand that the Patent Office applied a rejection to claims under examination at that time based on a prior art reference to Chen (EX1019). I understand that the applicant for the application for the '747 patent presented arguments in an attempt to distinguish Chen from the truncated top surface features that was under consideration at that time. (EX1004, 93-108.) Golonzka's rounded (untruncated) spacer top surfaces shown above (Fig. 1A) are similar to spacers described in the prior art (218n) of Chen that applicant said "do[] not have a truncated top surface" when it amended the claims to include this limitation. (EX1019, pp. 106-07; EX1004, 106-107.) The spacer top surface in Chen is rounded (as I show below), not planarized, just like Golonzka's:



Chen (EX1019) at Fig. 10 (annotated.)

115. In my opinion, A POSITA would have understood, to achieve Pethe's 500 structure, spacers 520's top surfaces are planarized, so spacer 520 also **has a truncated top surface** by virtue of the processing that is performed between its initial formation and its state as disclosed with reference to Figure 5A in Pethe. The last step in Golonzka's process (forming trench contacts 142) involves "planarization" "by CMP" of metal down to the spacers' surface. (EX1006, ¶0051.)

116. Pethe's corresponding trench contacts are adjacent to the flat-topped spacer and "spaced apart from gate stack structures 303A-308E by [these] spacers." (EX1005 (Pethe), 12:42-45; FIGs. 5A/5B.) No trench contact metal remains over the spacer after the aforementioned planarization, and thus the resulting Figure 5A

(and likewise FIG. 5B structure) including the spacer's top surface is planar, and thus truncated. (*id.*, FIGs. 5A/5B.)

f) a source/drain region (S/D region) disposed between two metal gates;

117. In my opinion, Pethe discloses this limitation.

118. Pethe teaches that trench contacts (310A-310C in Figure 5A and 311A-311C in Figure 5B) contact "diffusion regions" that include **a source/drain region (S/D region)**, which is **disposed between** gate stack structure 308A-308E (any two being **two metal gates**), as shown below in annotated Figure 5B structure.

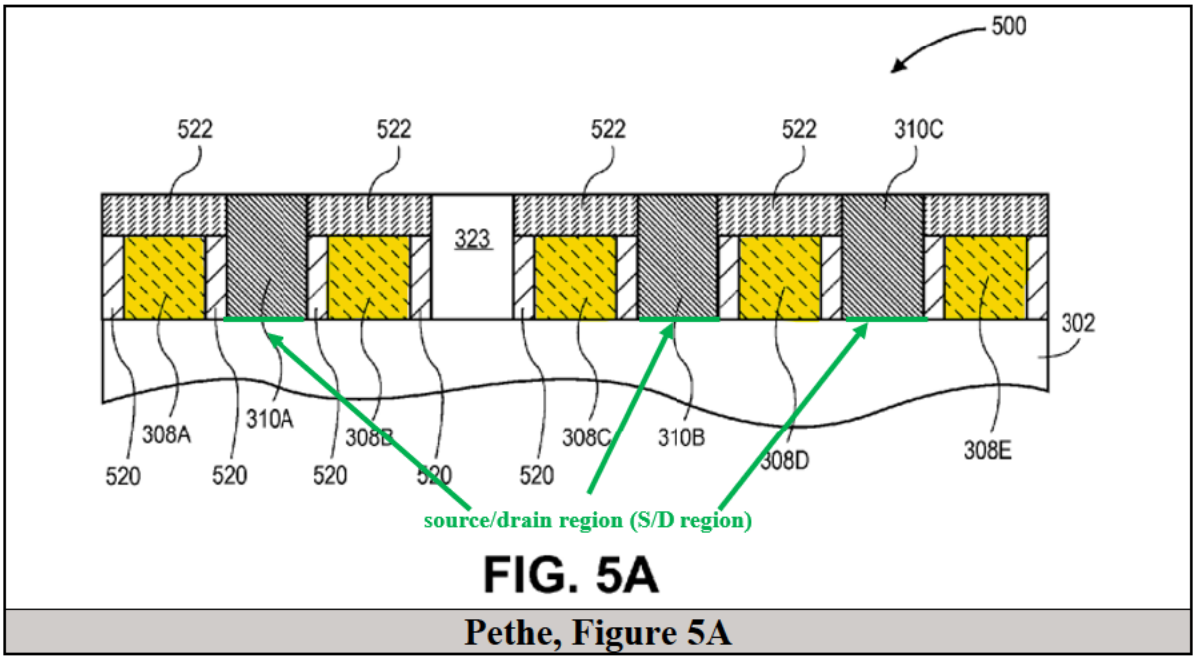
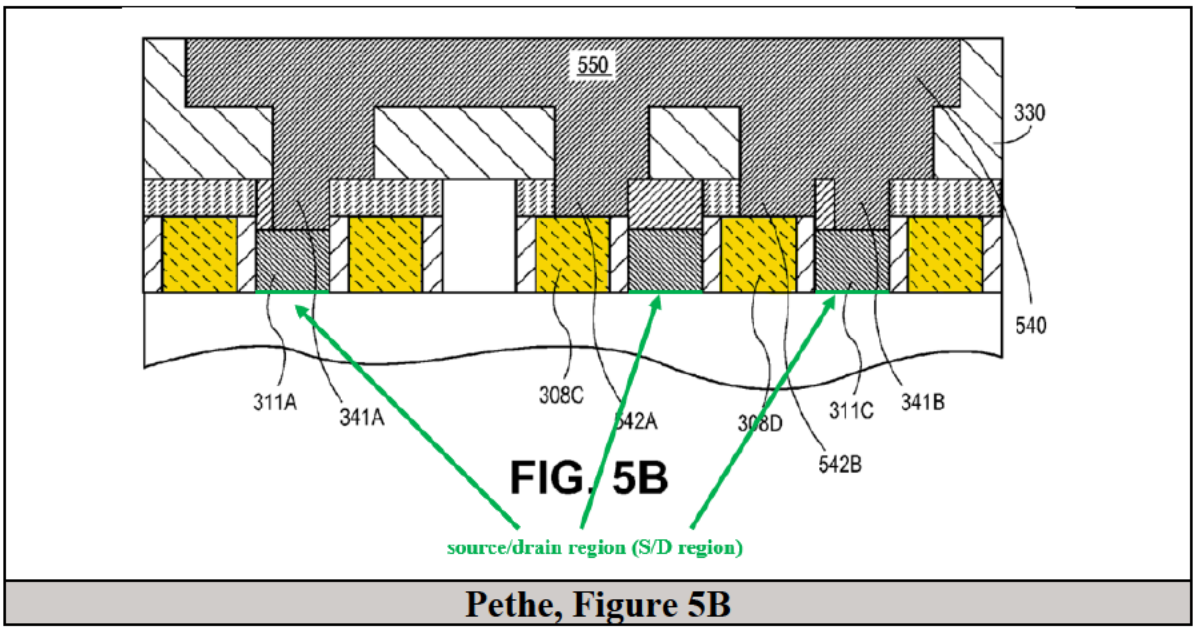


FIG. 5A

Pethe, Figure 5A



Pethe, Figure 5B

(EX1005 (Pethe), 12:32-53.)

119. As Pethe explains, "[t]rench contacts, *e.g.*, **contacts to diffusion regions** of substrate 302, such as trench contacts 310A-310C are also included in structure 500 and are **spaced apart from gate stack structures 308A-308E** by dielectric spacers 520." (EX1005 (Pethe), 12:32-53.)

120. The trench contacts... to diffusion regions" are to source/drain region (S/D region). In Pethe, the term "trench contacts" means source/drain contacts.

- "Referring to FIG. 1A, a semiconductor structure or device 100A includes a diffusion or active region 104 disposed in a substrate 102, and within an isolation region 106. One or more gate lines (also known as poly lines). Such as gate lines 108A, 108B and 108C are disposed over the diffusion or active region 104 as well as over a portion of the isolation region 106. ***Source or***

drain contacts (also known as trench contacts), such as contacts 110A and 110B, are disposed over **source and drain regions** of the semiconductor structure or device 100A. Trench contact vias 112A and 112B provide contact to trench contacts 110A and 110B, respectively. A separate gate contact 114, and overlying gate contact via 116, provides contact to gate line 108B. In contrast to the **source or drain trench contacts 110A or 110B**, the gate contact 114 is disposed, from a plan view perspective, over isolation region 106, but not over diffusion or active region 104. Furthermore, neither the gate contact 114 nor gate contact via 116 is disposed between the source or drain trench contacts 110A an 110B." (EX1005 (Pethe), 3:19-37.)

- "As an example, FIG. 2A illustrates a plan view of a semiconductor device having a gate contact via disposed over an active portion of a gate electrode, in accordance with an embodiment of the present invention. Referring to FIG. 2A, a semiconductor structure or device 200A includes a diffusion or active region 204 disposed in a substrate 202, and within an isolation region 206. One or more gate lines, such as gate lines 208A, 208B and 208C are disposed over the diffusion or active region 204 as well as over a portion of the isolation region 206. ***Source or drain trench contacts***, **such as trench contacts 210A and 210B**, are disposed over **source and drain regions** of the semiconductor structure or device 200A. Trench contact vias 212A and 212B provide contact

to trench contacts 210A and 210B, respectively. A gate contact via 216, with no intervening separate gate contact layer, provides contact to gate line 208B. In contrast to FIG. 1A, the gate contact 216 is disposed, from a plan view perspective, over the diffusion or active region 204 and between the source or drain contacts 210A and 210B." (EX1005 (Pethe), 4:33-36.)

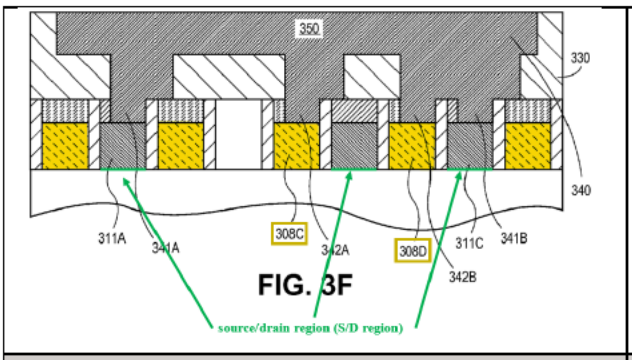
121. As another example, Pethe describes trench contact vias 341A/341B (formed by filling openings 336 with metal) to recessed trench contacts 311A-311C as "form[ing] contacts to the **source[/]drain regions of the transistor**." (EX1005 (Pethe), FIGS. 3D-3F, 10:35-36, 9:29-10:36, 11:21-22, 12:54-59 (referring to "trench contact vias 341A and 341B to trench contacts 311A and 311C" in "Fig. 5B.")

122. Also, Pethe describes similar features in connection with Pethe's-Figure-5-Embodiment, including by referencing Pethe's-Figure-3-Embodiment's features. (EX1005 (Pethe), 12:32-13:21, *e.g.*, 12:42-45 (describing same trench contacts 310A-310C).) Pethe's-Figure-3-Embodiment teaches trench contact vias 341A/341B (formed by filling openings 336 with metal) to recessed trench contacts 311A-311C as "form[ing] contacts to the **source[/]drain regions of the transistor**" (see EX1005 (Pethe), FIGS. 3D-3F, 10:35-36, 9:29-10:36, 11:21-22), and these teachings are also for the corresponding features of Pethe's-Figure-5-Embodiment, including the Figure 5B structure.

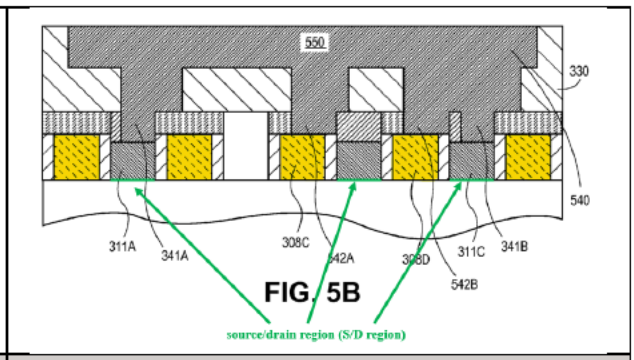
123. Pethe's trench contact vias 341A/341B, trench contacts 311A/311C, and source[/]drain regions in Pethe's-Figure-3-Embodiment and in Pethe's-Figure-5-Embodiment are the same for purposes of this limitation.

124. I have shown this below with respect to the Figures 3F and 5B structures. Pethe's trench contact vias 341A/341B, trench contacts 311A/311C, and source[/]drain regions teachings related to the Figure-3-Embodiment are also teachings are also for the corresponding features of Pethe's Figure-5-Embodiment. Pethe does not repeat its discussion of 341A/341B, 311A/311C, and S/D regions in the Pethe's-Figure-3-Embodiment to describe the Figure-5-Embodiment, and instead uses the same numerical reference number (341A/341B and 311A/311C) to describe the same elements.

125. As I explained above, in my opinion and experience, when a patent uses the same name and reference number in different Figures for an element, the text disclosures describing the element for one Figure apply to the element on the other Figures, as they are the same element (unless otherwise noted). It is my opinion that a POSITA would have understood the same in context of Pethe's disclosures, which discusses the same elements for the Figure 5B structure in the Figure 5 embodiment and for the Figure 3 embodiment, as exemplified below.

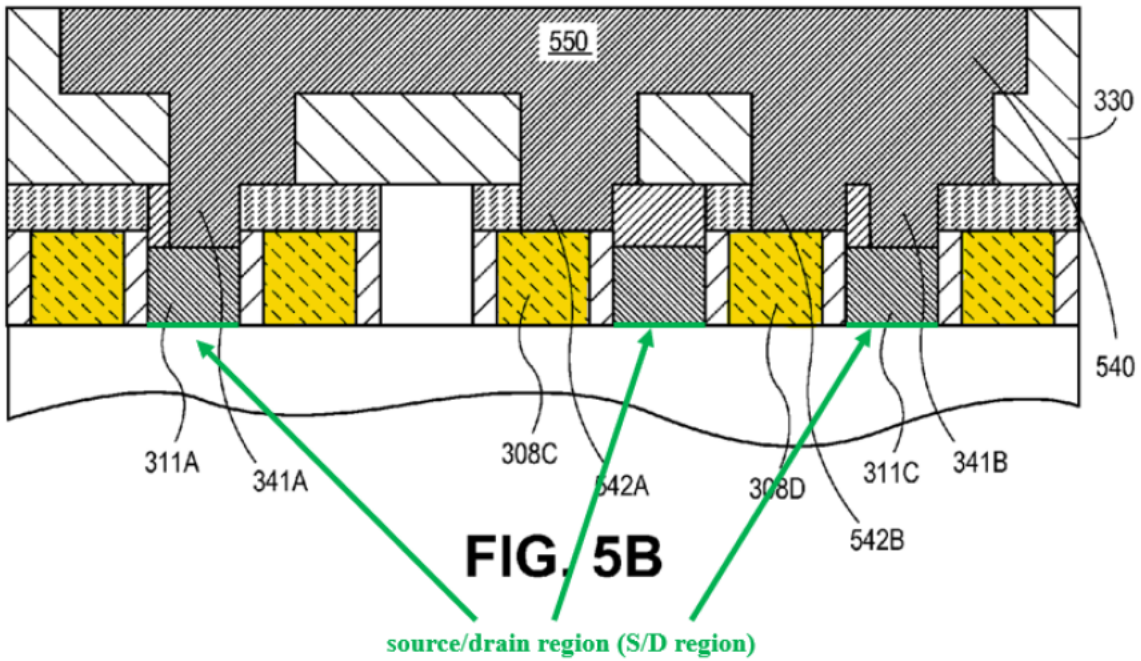


Pethe, Figure 3F



Pethe, Figure 5B

126. A POSITA would have understood in context of Pethe's teachings, diffusion regions of substrate 302 that contact **trench contacts 311A-311C** in Figure 5B's structure of Pethe's-Figure-5-Embodiment include **a source/drain region (S/D region)**, which is **"disposed between two metal gates**," like that shown below in annotated Figures 5B structure, and also shown in Figures 3A and 5A and consistent with element [1.f].



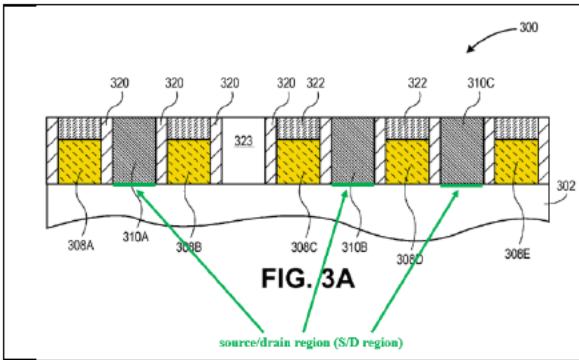


FIG. 3A

Pethe, Figure 3A

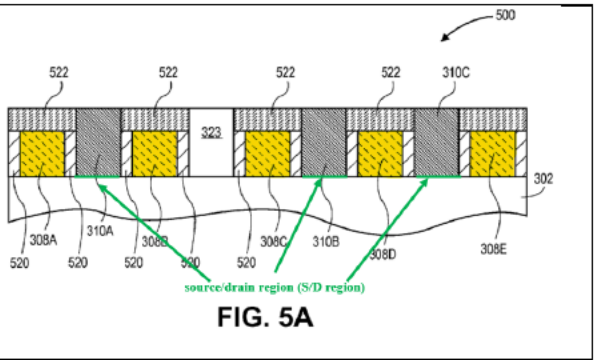


FIG. 5A

Pethe, Figure 5A

127. With respect to **Ground 1B**, in addition to Pethe disclosing element [1.f], it suggests it as well.

128. As I discussed above (*see* §IX.A.1.f Ground 1A, incorporated herein by reference), Pethe's "trench contacts... to diffusion regions" are to source/drain region (S/D region). (EX1005 (Pethe), 3:25-28 ("**Source or drain contacts (also known as trench contacts)**... are disposed over source and drain regions."), 3:31-35 ("source or drain trench contacts"), 4:33-36 ("**Source or drain trench contacts, such as trench contacts**... are disposed over source and drain regions."), 10:35-36).

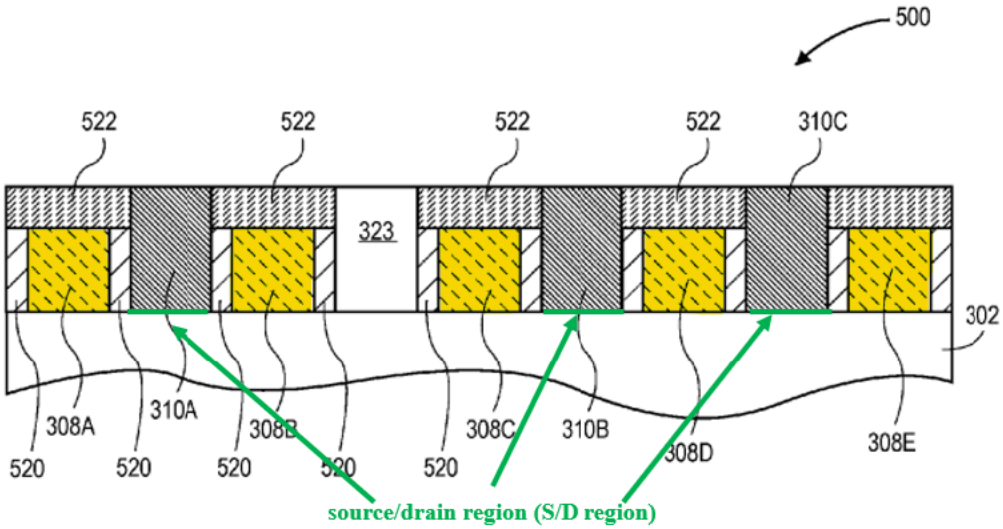


FIG. 5A

Pethe, Figure 5A

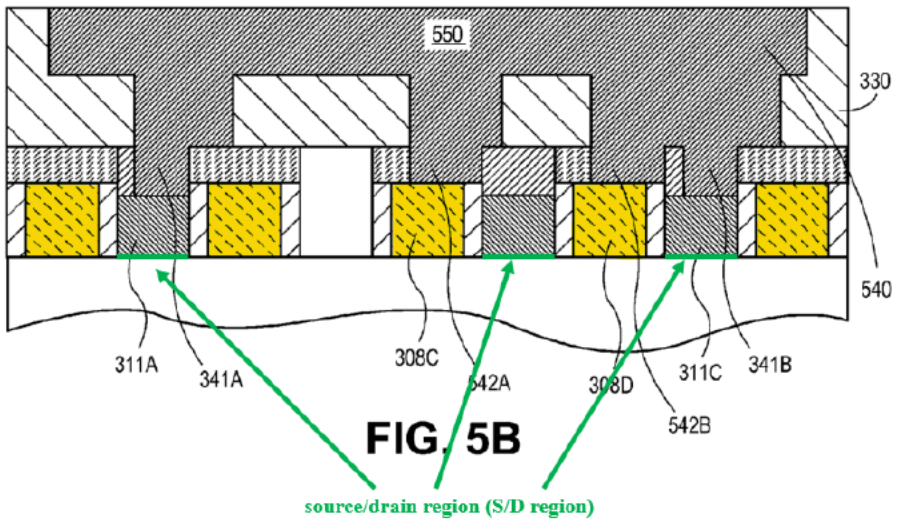


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 7:25-28; 10:33-36; 14:1-13.)

129. Thus, in my opinion a POSITA would have been motivated to include a S/D region disposed between two metal gates in the Figure 5B structure based on

the teachings and suggestions in Pethe, and would have had a reasonable expectation of such implementation would have been successfully achieved.

130. A POSITA would have appreciated that Pethe consistently describes its invention in the context of transistors. For instance, in its Background, Pethe describes the desire to "shrink[] transistor size" and "scal[e]" the "dimensions" of "multi-gate transistors." (EX1005 (Pethe), 1:14-45.)

131. Building from that background, Pethe describes structures having known transistor features. (for example, 5:23-26 (referring to "transistor gates"), 3:25-28 ("source and drain regions"), 4:33-36, 5:19-23, 6:60-64, 10:32-36.) In fact, Pethe notes that the described semiconductor devices "may be transistors or like devices" including MOS transistors and "FIN-FET" transistors, which were known to include gate and source/drain features. (*Id*., 14:1-13.)

132. Figure-5-Embodiment also describes transistors having "gate stack structures," including a gate electrode and a gate dielectric layer (EX1005 (Pethe), 12:37-53), which a POSITA would have understood concerns a field-effect transistor (FET).

133. A POSITA would have recognized and appreciated Pethe's numerous references to transistor features, including features consistent with source/drain regions of a transistor. (*See* citations and discussions of Pethe immediately above; for example, EX1005 (Pethe), 13:63-14:13.) Pethe's-Figure-3-Embodiment (which

provides disclosures of features relating to features disclosed in Pethe's-Figure-5-Embodiment), describes a transistor's source/drain regions, stating that trench contact vias 341A/341B (formed by filling openings 336 with metal) to recessed trench contacts 311A-311C "form contacts to the **source drain regions** **of the transistor**." (EX1005 (Pethe), FIGS. 3D-3E, 3A, 10:35-36, 9:29-10:36, 11:21-22, 7:25-28, 3:25-28, 3:32-37, 4:33-36, 4:42.)

134. A POSITA was well aware of the term "diffusion regions" at the time, and thus understood that diffusion regions was used to describe source/drain regions, which were conventionally formed by a diffusion process involving introducing dopants (impurities) into the substrate. (EX1012, xxiii, Figure 0.5; EX1014, 3, 6.)

135. A POSITA would have also understood and appreciated that to make a FET, such as a MOSFET, FIN-FET, or tri-gate transistor, as contemplated by Pethe (*see for example*, EX1005 (Pethe), 13:63-14:13), a source/drain region on each side of the gate (i.e., next to the channel) was needed in order for the structure to operate as a MOS transistor or field-effect transistor (for example, MOSFET, FIN-FET, trigate transistor)-based semiconductor device.

136. As I discussed in Section V.A (which I incorporate by reference here), FETs are fundamentally structured as shown below, with a channel beneath a "gate" (G), and "source" (S) and "drain" (D) regions on each side of the gate such that

current flows between the source and drain regions through the channel formed under the gate.

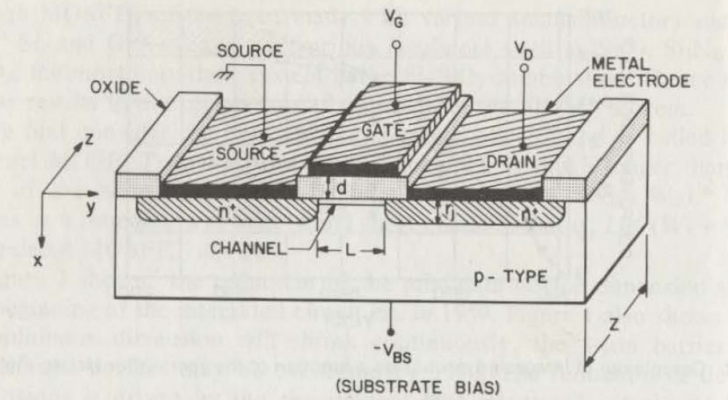


Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

(EX1023, 433-34, 438, Figs. 3, 6.)

137. Thus, in my opinion, a POSITA would have been motivated to include in context of Pethe's teachings, to include a source/drain region (S/D region), which is "disposed between two metal gates" 308.

138. A POSITA would have thus been motivated to include a S/D region between two metal gates, in particular, underneath the trench contacts 311A-311C shown above in annotated Figure 5B (and 310A-310C shown above in annotated Figure 5A), which are all between two metal gates in the Figure 5B structure's semiconductor region. (EX1005 (Pethe), FIGs. 5A/5B.) A POSITA would have been motivated to implement, and had a reasonable expectation of success of implementing, such a modification, especially given it would have involved the

application of known semiconductor device structure and process technologies that were well within a POSITA's capabilities and knowledge at the time.

139. Pethe's discussions of a "gate" would have led a POSITA to understand that a field-effect transistor (FET) transistor was contemplated by Pethe in connection with its disclosed semiconductor structure / device features. Thus, in order to have a FET, a POSITA would have been motivated to include a S/D region, for example, on both sides of the gate 308D (in the substrate 302 underneath where the trench contacts 311B and 311C in the Figure 5 embodiment as shown above in annotated FIG. 5B (and shown in FIGs. 5A and 3A-3F)). Accordingly, the S/D region under trench contact 311B is between gates 308C and 308D, and the S/D region under trench contact 311C is between gates 308D and 308E.

140. A POSITA would have understood that implement the modification discussed above would have involved the application of known semiconductor device structure and process technologies that were well within the capabilities and knowledge of a POSITA at the time, consistent with the teachings of Pethe. In my opinion, a POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of Pethe Figure 5 embodiment structure of Figure 5B having **a source/drain region (S/D region)** in

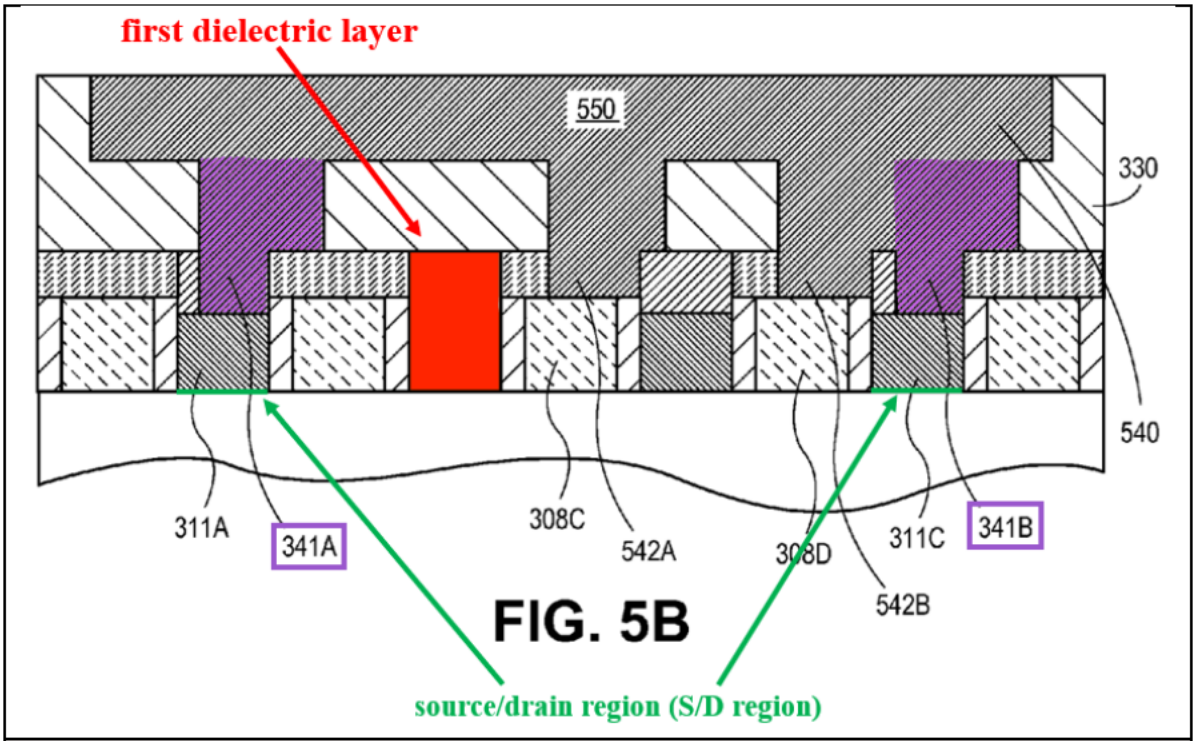
substrate 302 directly beneath, for example, trench contact 311C that is **disposed between two metal gates 308D** and **308E**, like that recited in element [1.f].

g) a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;

141. In my opinion, Pethe discloses this limitation.

142. Pethe teaches trench contact vias 341A and 341B that are **a plurality of first contacts**, as shown in annotated Figure 5B's structure below.

143. The following annotations of the structure of Figure 5B shows how Pethe discloses this limitation:



Pethe, Figure 5B

(EX1005 (Pethe), 12:54-67, see also for Figure 3 embodiment 11:23-31.)

144. As also shown in Figure 5B, the trench contact vias 341A and 341B are **disposed** in Pethe's first dielectric layer (of which region 323 is a part of) (**the first dielectric layer**.) This is also apparent for the same reasons discussed above for claim element [1.d], which is incorporated by reference here for further explanation. (*See Section* § IX.A.1.d.)

145. Trench contact vias 341 correspond to the structures comprising metal that fill in the openings 336.

146. Pethe first introduces trench contact vias 341 in relation to Figure 3 and explains:

> Referring to FIG. 3F, **a metal contact structure 340 is formed in** the metal (0) trench 334 and **via openings 336** and 338 **of the structure described in association with FIG. 3E**. **The metal contact structure 340 includes** a metal (0) portion 350 along with **trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively)** and gate contact vias (e.g., gate contact vias 342A and 342B to gate stack structures 308C and 308D, respectively).

(EX1005 (Pethe), 11:23-31.)

147. The following annotations show openings 336:

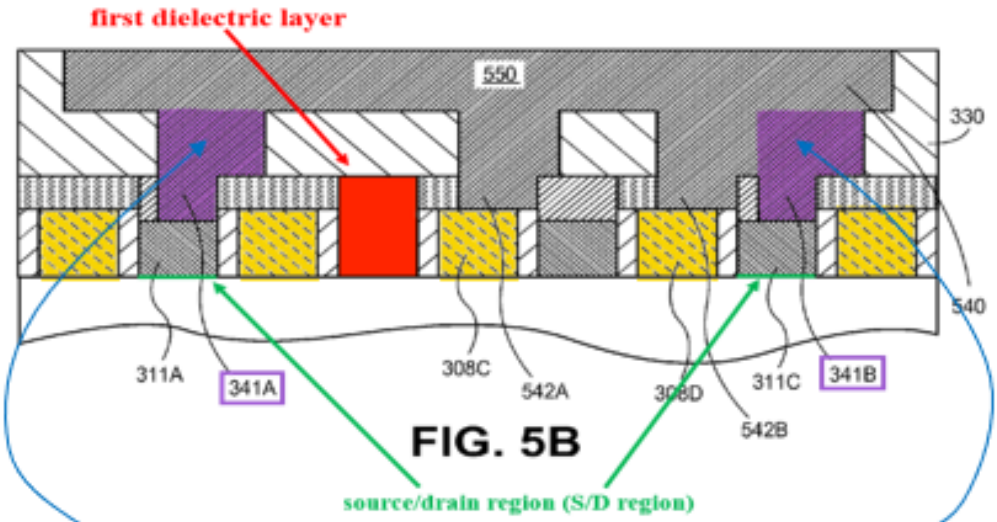


FIG. 5B

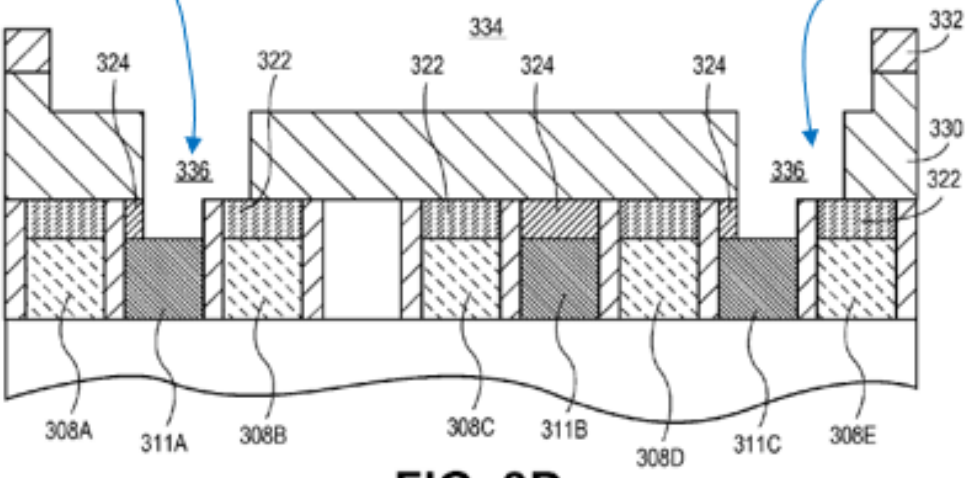


FIG. 3D

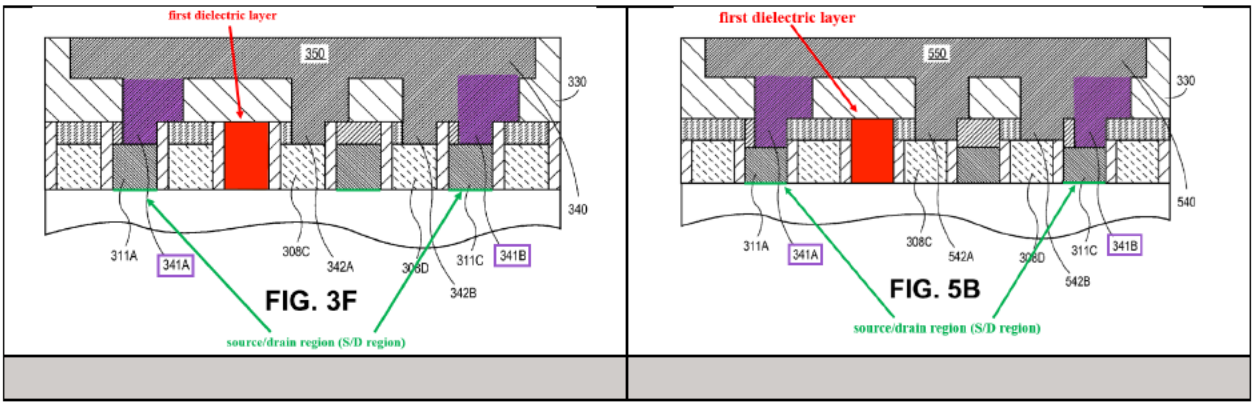
(EX1005 (Pethe), 11:23-31, 11:32-42, 9:29-10:36.)

148. Pethe identifies trench contact vias 341 in the Figure-5 Embodiment in the same manner.

> Referring to FIG. 5B, **a metal contact structure 540** is formed in a metal (0) trench and **via openings** formed in a dielectric layer 330. **The metal contact structure 540 includes** a metal (0) portion 550 along

with **trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively)**. The metal contact structure 540 also includes gate contact vias (e.g., gate contact vias 542A and 542B to gate stack structures 308C and 308D, respectively). (EX1005 (Pethe), 12:54-62)

149. Trench contact vias 341A, 341B in Pethe's-Figure-3-Embodiment and Pethe's-Figure-5-Embodiment are the same for purposes of this limitation, as shown in annotated figures below.



150. As I discussed in the Overview of Pethe (VII.A), the introduction to Ground 1 (IX.A), and the preamble of claim 1 (IX.A.1.a), Pethe's Figure 5B structure has undergone the fabrication steps of Figures 3B-3E.

151. The "trench contact vias 341A and 341B" are "to trench contacts 311A and 311C," meaning that the trench contact vias 341A and 341B are **electrically connected to** trench contacts 311A and 311C. (EX1005 (Pethe), 12:54-67; *see also id.*, 11:23-29.)

152. And as explained above for element [1.f] (§IX.A.1.f incorporated by reference here), in Pethe, the term "trench contacts" means source/drain contacts. The openings 336 (when filled with metal to form trench contact vias 341A and 341B) to recessed trench contacts 311A-311C "form contacts to the source drain regions of the transistor," meaning the trench contact vias 341A and 341B **are electrically connected to parts of the S/D region** in the Figure 3F structure (EX1005 (Pethe), 10:35-36, 9:29-10:36.)

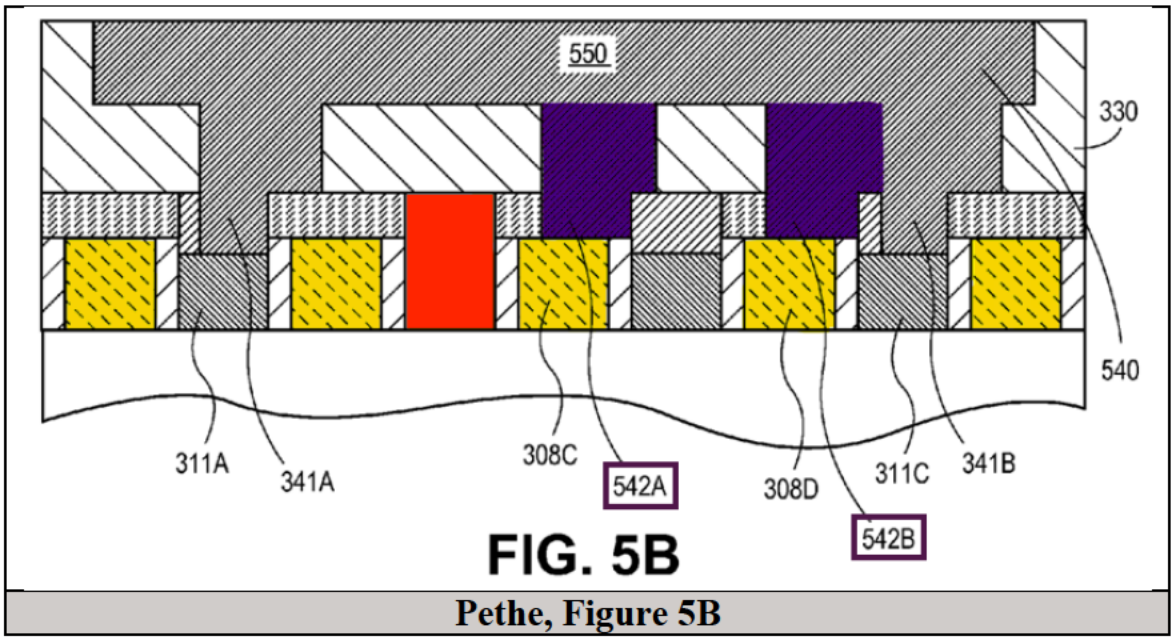
153. Thus, trench contact vias 341A and 341B **are electrically connected to** trench contacts 311A-311C, and trench contacts 311A-311C **are electrically connected to** the source/drain regions, meaning that trench contact vias 341A and 341B **(a plurality of first contacts) are electrically connected to parts of** the source/drain regions.

154. Thus, trench contact vias 341A, 341B in Pethe's-Figure-5-Embodiment Figure 5B structure **are electrically connected to parts of the S/D region** as shown above. (EX1005 (Pethe), 10:35-36, 9:29-10:36; 12:54-59.) The purpose of trench contact vias 341A and 341B is in fact to provide electrical connection to the source/drain regions in the Figure 5B structure.

h) a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts; and

155. In my opinion, Pethe discloses this limitation.

156. Pethe's gate contact vias 542A, 542B in Figure 5B's structure are **a plurality of second contacts**, as shown annotated Figure 5B below:



Pethe, Figure 5B

(EX1005 (Pethe), 12:54-67, see also Figure 3 embodiment 11:23-31.)

157. As also shown in Figure 5B, the gate contact vias 542A, 542B are **disposed in** Pethe's first dielectric layer (of which region 323 is a part of) (**the first dielectric layer**.) This is apparent for the same reasons that I discussed above for element [1.d], which I incorporate by reference here for further explanation.

158. Pethe also explains, and as shown in Figure 5B, that "gate contact vias 542A and 542B" (**a plurality of second contacts**) are "to gate stack structures 308C and 308D, respectively" (**are electrically connected to one of the metal gates**). (EX1005 (Pethe), 12:54-67.)

159. In other words, gate contact via 542A **is electrically connected to** 308C (**one of the metal gates**), and gate contact via 542B is **electrically connected to** 308D (**one of the metal gates**), meaning the **plurality of second contacts**...**are electrically connected to one of the metal gates**. (EX1005 (Pethe), 12:54-67.)

160. Pethe first introduces gate contact vias in relation to Figure 3 and explains:

> Referring to FIG. 3F, **a metal contact structure 340 is formed in** the metal (0) trench 334 and **via openings** 336 and **338 of the structure described in association with FIG. 3E**. **The metal contact structure 340 includes** a metal (0) portion 350 along with trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively) and **gate contact vias (e.g., gate contact vias 342A and 342B to gate stack structures 308C and 308D, respectively).**

(EX1005 (Pethe), 11:23-31.)

161. Gate contact vias 342A, 342B in the Figure-3-Embodiment comprise metal that fill openings 338 shown in annotated Figure 3E below:

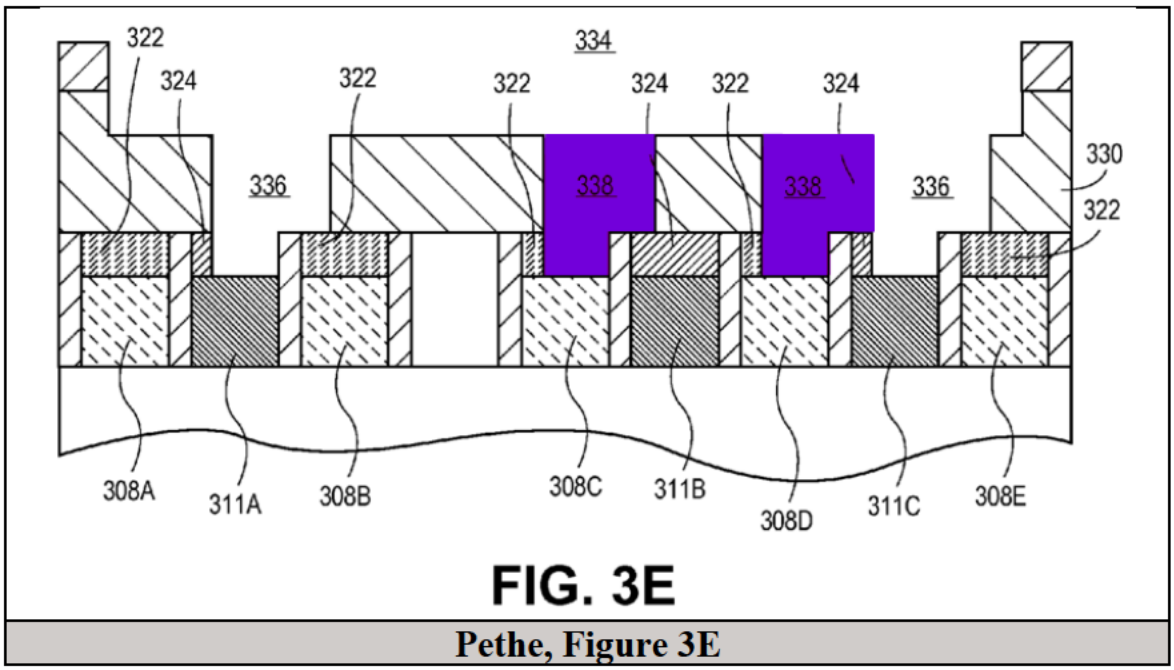


FIG. 3E

Pethe, Figure 3E

(EX1005 (Pethe), 11:23-31, 10:37-11:22.)

162. The openings 338 (when filled with metal to form gate contact vias 342A and 342B) to gate stack structures 308C and 308D "form the gate contact on active regions of the transistor," meaning the gate contact vias 342A and 342B are **electrically connected to one of the metal gates**. (EX1005 (Pethe), 11:21-22, 11:23-31, 10:52-11:22.) The purpose of gate contact vias 342A and 342B is to provide electrical connection to the metal gates within gate structures 308C and 308D.

163. Gate contact via 342A **is electrically connected to** gate stack structure 308C (**one of the metal gates**), and gate contact via 342B is **electrically connected to** gate stack structure 308D (**one of the metal gates**), meaning the **plurality of**

second contacts... are electrically connected to one of the metal gates. (EX1005 (Pethe), 11:23-31.)

164. As shown in the annotated Figure 3F below, trench contact via 341B (**at least one of the first contacts**) **directly connects** gate contact via 342B (**at least one of the second contacts**).

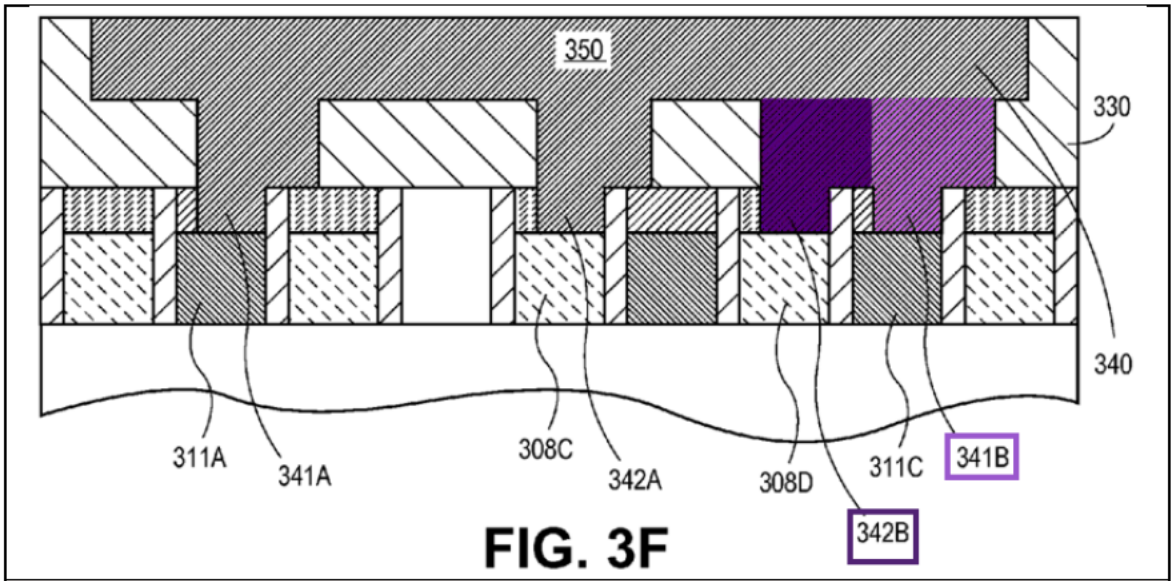


FIG. 3F

Pethe, Figure 3F

(EX1005 (Pethe), 11:23-42.)

165. In addition, the etching steps described by Pethe in connection with Figures 3C, 3D, and 3E result in metal (0) trench 334, via openings 338, and via openings 336 being formed. (EX1005 (Pethe), 9:1-11:22.) In Figure 3F, a single metal deposition (i.e., "a deposition of a fill metal layer") fills the space of all three regions, by which metal (0) trench 334 is filled with metal (0) portion 350, gate contact vias 342 fills via openings 338, and trench contact vias 341 fills via openings

336. (EX1005 (Pethe), 11:23-42.) Thus, trench contact via 341B (**at least one of the first contacts**) **directly connects** gate contact via 342B (**at least one of the second contacts**) with no intervening layers or other barriers in the Figure 3F structure.

166. Pethe identifies gate contact vias 542 in Figure 5's Embodiment in the same manner as gate contact vias 342 in Figure 3's Embodiment.

> Referring to FIG. 5B, **a metal contact structure 540** is formed in a metal (0) trench and **via openings** formed in a dielectric layer 330. The metal contact structure 540 includes a metal (0) portion 550 along with trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively). **The metal contact structure 540 also includes gate contact vias (e.g., gate contact vias 542A and 542B to gate stack structures 308C and 308D, respectively)**.

(EX1005 (Pethe), 12:54-62.)

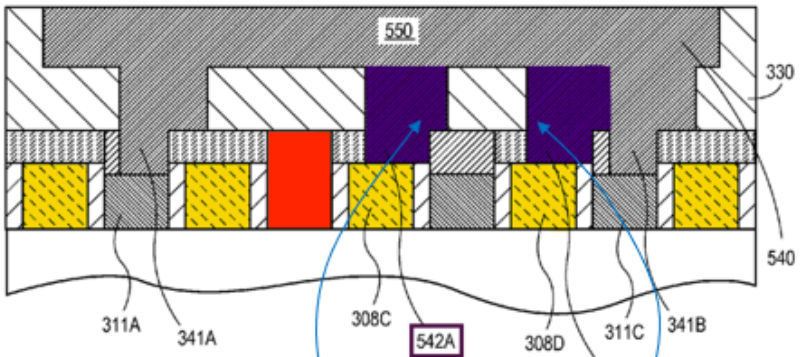


FIG. 5B

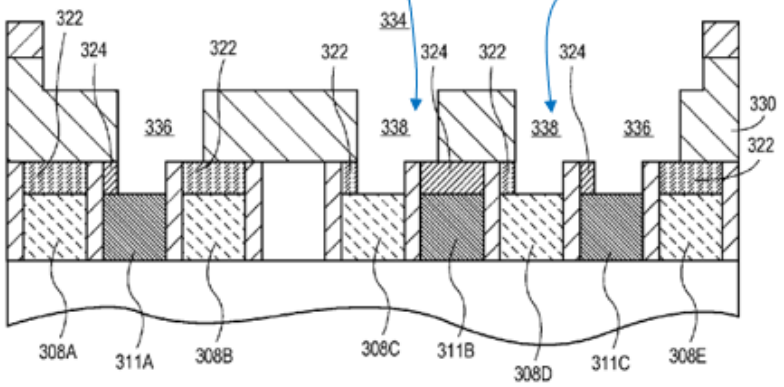


FIG. 3E

167. Gate contact vias 342A, 342B in Pethe's-Figure-3-Embodiment and gate contact vias 542A, 542B in Pethe's-Figure-5-Embodiment are the same for purposes of this limitation. I have shown this in annotated figures below.

168. As I discussed in the Overview of Pethe (VII.A), the introduction to Ground 1 (IX.A), and the preamble of claim 1 (IX.A.1.a), Pethe's Figure 5B structure has undergone the fabrication steps of Figures 3B-3E.

169. The formation of the gate contact vias 542 share the same processes of formation as gate contact via 342 (same feature but deeper only because of recessed

spacers 520). EX1005 (Pethe), 12:54-67 (explaining that the Figure 5B structure "[i]n comparison to the structure described in association with FIG. 3F" is just "slightly different since the spacers 522 are not exposed, yet coverage of the insulating cap layers 522 is extended, during etch formation of the via openings leading to gate contact vias 542A and 542B").

170. The only difference between the gate contact vias in Pethe's-Figure-3-Embodiment and in Pethe's-Figure-5-Embodiment are that gate contact vias 542A, 542B in Pethe's-Figure-5-Embodiment occupy the space that the spacers did before being recessed, which does not affect whether the gate contact via discloses this limitation. (EX1005 (Pethe), 12:62-67.)

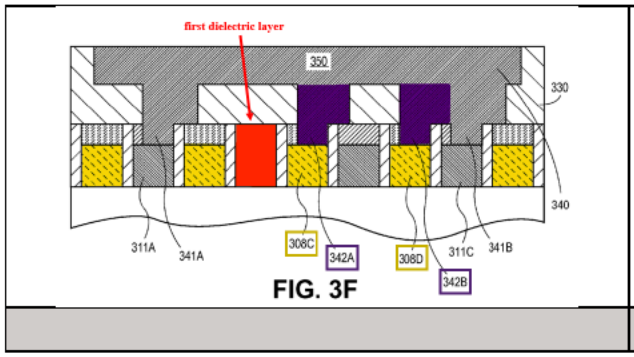


FIG. 3F

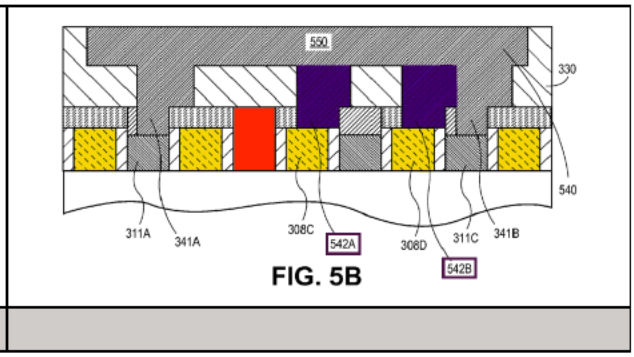


FIG. 5B

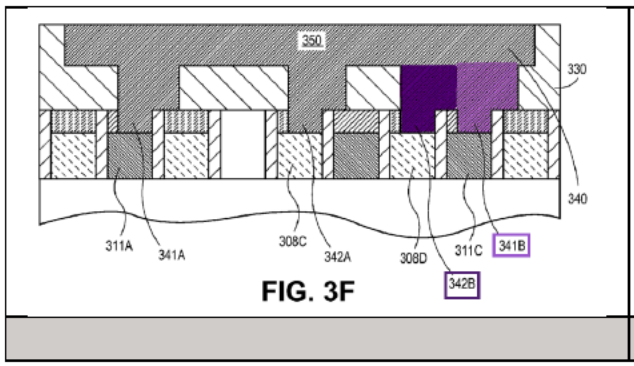


FIG. 3F

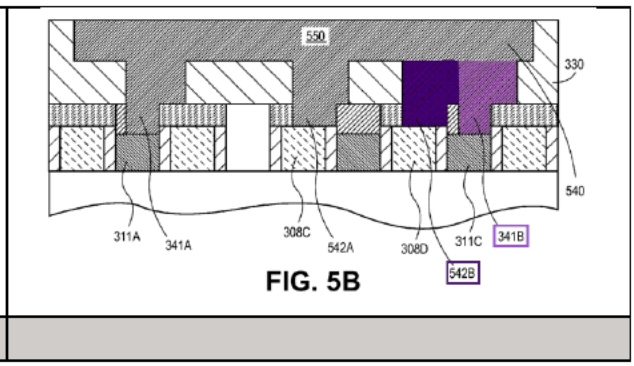


FIG. 5B

171. Pethe's Figure 5B structure meets the identified challenged claims for reasons explained. The discussion of features from Figures 3C-3F provides disclosures of the same features in the Figure 5B structure given, as noted, the formation of the gate contact vias 542 share the same processes of formation as gate contact vias 342. EX1005 (Pethe), 12:54-67.

172. Further, as I previously discussed, the etching steps described by Figures 3C-3E to create openings 336 and 338 (*see* 9:1-11:22) to be filled with metal to create the vias and metal (0) portion in Figures 3F and 5B (discussed in [1.f], [1.g], and [1.h]) are also teachings for the corresponding features of Pethe's-Figure-5-Embodiment. While these steps in Figures 3C-3E arrive at the Figure 3F structure in Pethe's-Figure-3-Embodiment, the Figure 5B structure includes the same relevant features. Pethe did not reproduce Figures 3C-3E in any Figures 5C-5E, as a POSITA would have understood that the Figure-3-Embodiment teachings apply to the Figure-5-Embodiment.

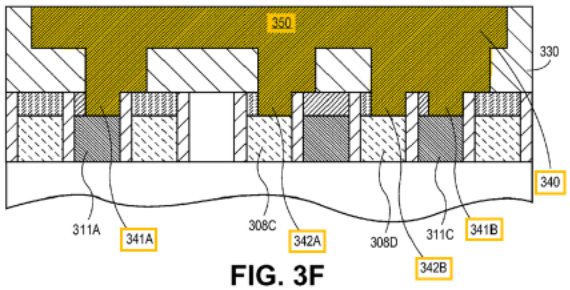


FIG. 3F

EX1005 (Pethe), Figure 3F

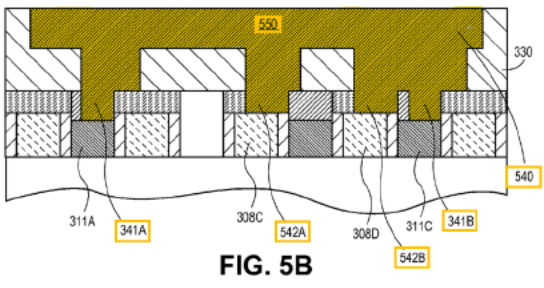
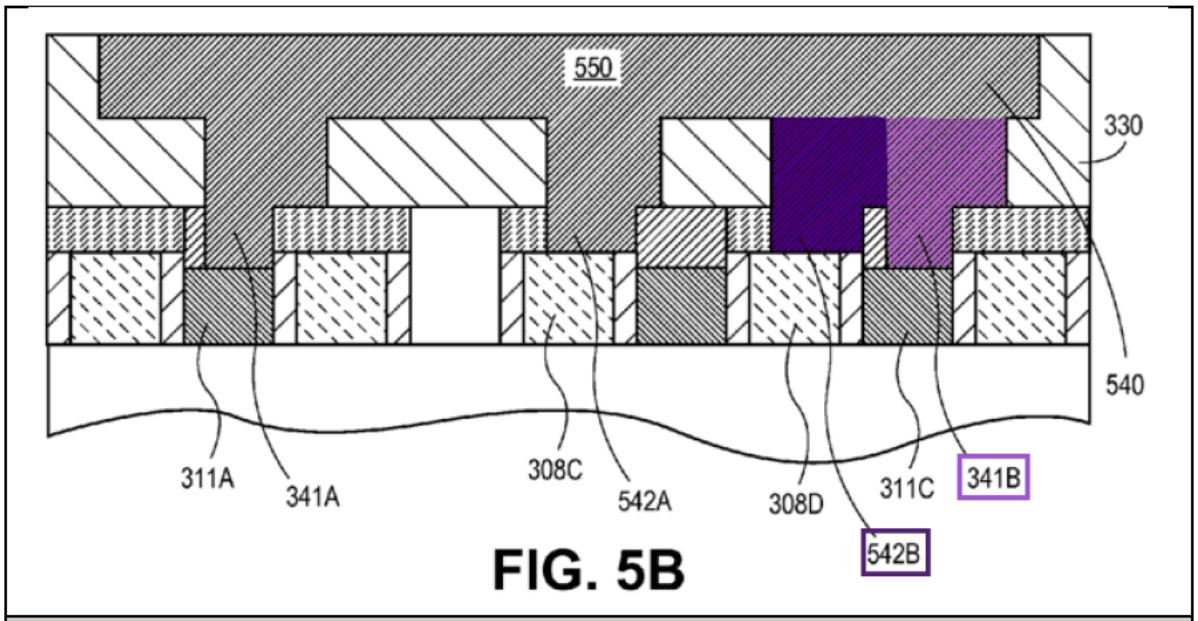


FIG. 5B

EX1005 (Pethe), Figure 5B

173. Accordingly, for reasons explained, Pethe's-Figure-5-Embodiment discloses a "plurality of second contacts" (gate contact vias 542A, 542B) "disposed in the first dielectric layer" (of which region 323 is a part of) "that are electrically connected to one of the metal gates" (gate stack structures 308A-308E, e.g., 308C-308D). (EX1005 (Pethe), FIG. 5B.)

174. As explained above and further shown in the annotated Figure 5B below, trench contact via 341B (**at least one of the first contacts**) **directly connects** gate contact via 542B (**at least one of the second contacts**).



Pethe, Figure 5B

(EX1005 (Pethe), 12:54-67.)

175. In my opinion, Pethe's teachings are consistent with the '747 patent's descriptions of first and second contacts formed next to each other. (EX1001, FIG. 9 (elements 52/54); *see also* EX1004, 135.)

i) a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

176. In my opinion, Pethe discloses this limitation.

177. For example, Pethe's Figure 5B structure includes insulating cap layer 522 that is **a hard mask** that is **disposed on** the gate stack structures 308A-308E, *e.g.*, 308B (**one of the metal gates**), as shown in annotated Figures 5A-5B. For example, an insulating cap layer 522 (**hard mask**) is disposed on gate structure 308B (one of the metal gates), as shown below in annotated Figures 5A-5B.

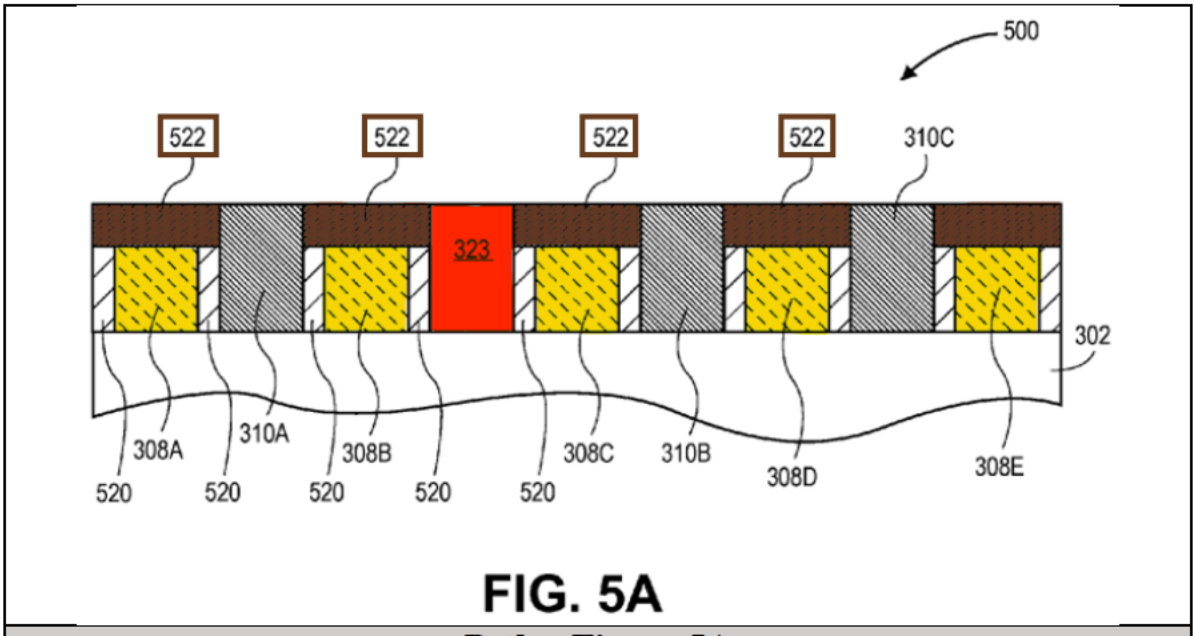


FIG. 5A

Pethe, Figure 5A

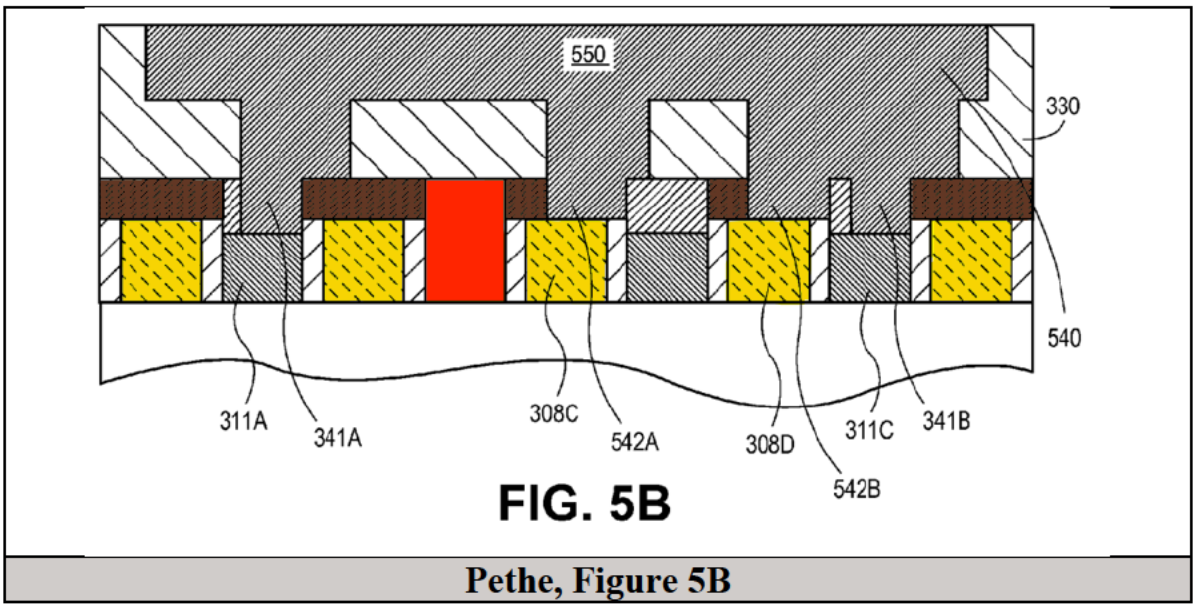


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 12:45-67, *see also* Figure 3 embodiment 7:15-34.)

178. Pethe also notes that "insulating cap layers 522... cover[] the gate stack." (*Id.*) With it covering the gate stack, Pethe's insulating cap layer disposed on the gates is "for protecting a metal gate electrode." (EX1005 (Pethe), 3:48-50, 4:54-56.) Cap layer 522 is a **hard mask**, as 522 is an insulating layer that provides protection for gate regions directly covered by 522.

179. As shown in Figure 5B structure above, the **top surface of** insulating cap layer 522 **and the top surface of** Pethe's first dielectric layer (of which region 323 is a part of) **(the first dielectric layer) are on the same level**. This understanding is consistent with the incorporated teachings of Golonzka, which describes the formation of the first dielectric layer as a CVD process, after which the dielectric is "planarized to expose the top portions of all dummy gates" by a CMP, as shown in Figures 1G and 1H. (EX1006, ¶¶41-42; EX1005 (Pethe), 7:35-39.) The

dummy gates are replaced by permanent gates, and "a top portion of the permanent gate structures 134 are removed, e.g., by an etch process, and replaced with a dielectric cap layer." (EX1006, ¶¶45-47.) Thus, the top surface of the caps 140 shown in Golonzka's Figure 1J (which correspond to insulating cap layer 322 in Pethe's Figure 3) are at the same planarized level as the top surface of the first dielectric layer.

180. This **same level** is further confirmed by the CMP planarization described in Figure 3B and discussed in claim 3. (*See below* IX.A.3, which I incorporate by reference herein.) Pethe explains that the conformal deposition of cap layer 324 and subsequent planarization by CMP occurs over "the entire structure," meaning that Pethe's first dielectric layer (of which region 323 is a part of) (**the first dielectric layer**) and insulating cap layers 322 (and 522) and 324 would all become planarized with the top surfaces **on the same level**. (EX1005 (Pethe), 8:44-51.) The CMP over the entire structure provides layer 324 "**only** above 310A-310C," and "**re-expos[es]** spacers 320 and insulating cap layer 322" (EX1005 (Pethe), 8:37-51.) The CMP of Figure 3B is also performed in the Figure-5-Embodiment. (*See* above §IX.A; *below* §IX.A.3.)

181. Further confirmation of Pethe's insulating cap layer 522 in Figure 5B's structure being **a hard mask** that "is **disposed on** the gate stack structures 308A-

308E," *e.g.*, 308B (**one of the metal gates**) is provided by Pethe's-Figure-3-Embodiment teachings.

182. Also, as Pethe explains, insulating cap layer 322 is "**disposed on** the gate stack structures 308A-308E." (EX1005 (Pethe), 7:15-34.) Pethe further explains that insulating cap layer 322 and insulating cap layer 324 are etch selective with each other, meaning that an etch may be selected that etches only one of 322/324, and another etch that etches the inverse. (EX1005 (Pethe), 8:34-36, 8:52-67.) This etch selectivity is relied on etch the openings 336 in Figure 3D (by etching 324 but not 322), and the openings in Figure 3E (by etching 322 but not 324.) (EX1005 (Pethe), 9:29-11:22.)

183. Pethe also discloses that "insulating cap layer 324 is etched to form via openings 336 **selective to (i.e., without significantly etching or impacting) insulating cap layer 322**," which is shown in Figure 3D. (EX1005 (Pethe), 9:36-43, FIG. 3D.) Accordingly, insulating cap layer 322 in the Figure 3F structure (and therefore insulating cap layer 522 in the Figure 5B structure) is a **hard mask** for the etching of openings 336, as layer 322 is an insulating layer that blocks or provides protection for regions directly covered by 322 so these regions do not etch. Cap layer 322 in the Figure 3F structure is also disposed on one of the metal gates, as it is situated on and not part of the metal gate. (EX1005 (Pethe), 8:33 ("insulating cap layer 322 on gate stack structures 308A-308E"), 9:39-40.)

184. Pethe's-Figure-3-Embodiment discloses similar features, which are also teachings for the corresponding features of to Pethe's-Figure-5-Embodiment. For example, Pethe's FIG. 3F structure also includes insulating cap layer 322 that is **a hard mask disposed on** gate stack structures 308A-308E, *e.g.*, 308B (**one of the metal gates**). (EX1005 (Pethe), FIGs. 3A, 3F.)

185. It can be seen that layer 322 (hard mask) is disposed on gate structure 308B (one of the metal gates), as shown in annotated Figures 3A/3F below.

186. Pethe's insulating cap layer 322 in Pethe's-Figure-3-Embodiment and insulating cap layer 522 in Pethe's-Figure-5-Embodiment are the same for purposes of this limitation, for example, as shown below (in connection with the Figures 3F and 5B structures), and its teachings related to the Figure-3-Embodiment are also teachings for the corresponding features of to the Figure-5-Embodiment. The only difference between the insulating cap layer in Pethe's-Figure-3-Embodiment and in Pethe's-Figure-5-Embodiment is that insulating cap layer 522 in Pethe's-Figure-5-Embodiment occupies the space that the spacers did before being recessed. (EX1005 (Pethe), 12:62-67.) Such difference does not detract from the analysis and rationale for Pethe's-Figure-3-Embodiment applying to the analysis here for Pethe's-Figure-5-Embodiment.

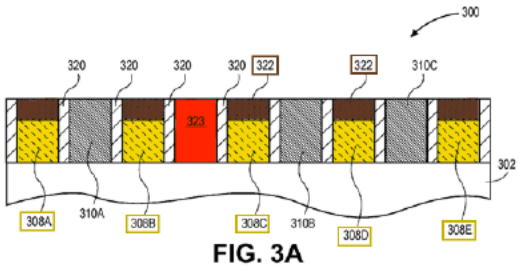


FIG. 3A

Pethe, Figure 3A

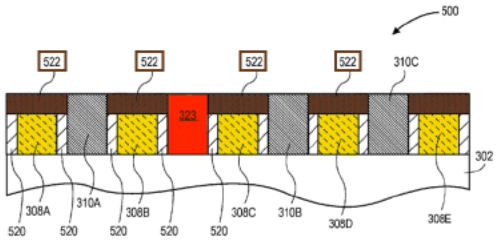


FIG. 5A

Pethe, Figure 5A

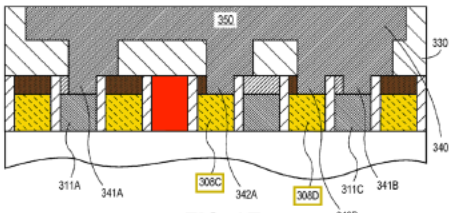


FIG. 3F

Pethe, Figure 3F

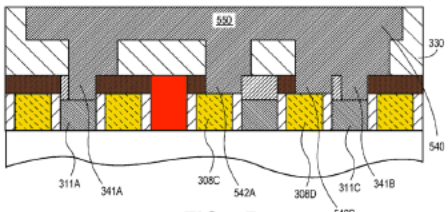


FIG. 5B

Pethe, Figure 5B

2. Claim 2

a) The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.[5]

187. In my opinion, Pethe discloses these limitations.

[5] Claim 1 does not recite a "semiconductor device." However, for purposes of my opinions, I have been asked to assume claims 2-9 refer to the semiconductor "structure" recited in claim 1.

188. For example, Pethe's Figure 5B structure includes an inter-layer dielectric 330 that is **a second dielectric layer disposed on the first dielectric layer** (of which ILD region 323 is a part).

189. The following annotations of Figure 5B shows how Pethe discloses this limitation:

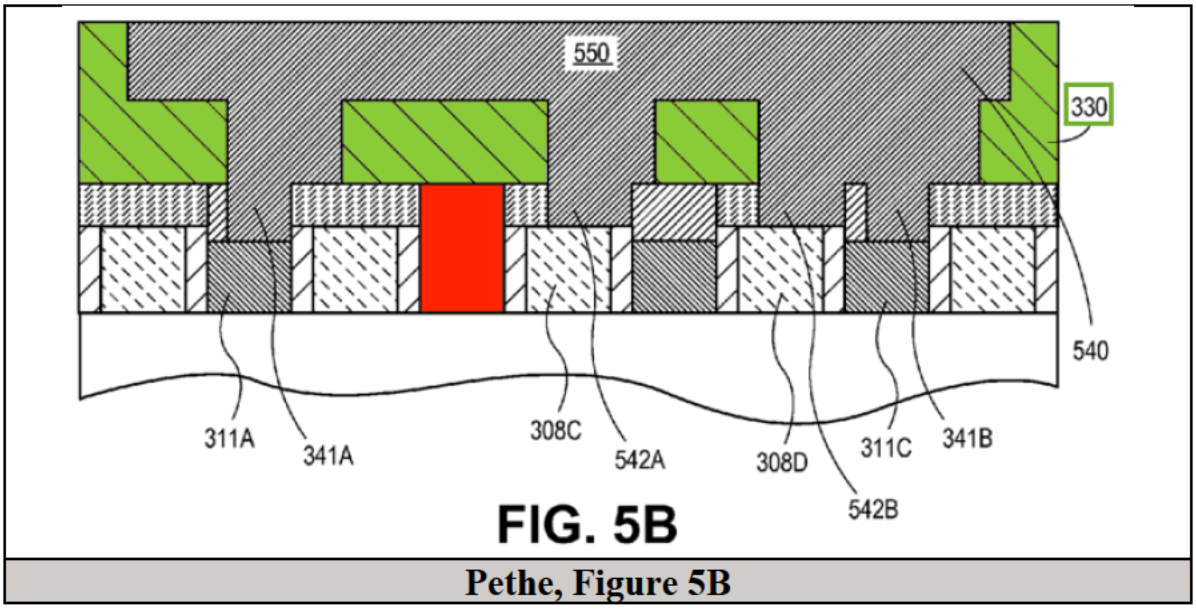


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 12:54-67, see also for Figure 3 embodiment 9:1-43, 10:47-51.)

190. Pethe explains that "inter-layer dielectric (ILD) 330 may be composed of a material suitable to electrically isolate metal features ultimately formed therein while maintaining a robust structure between front end and back end processing." (EX1005 (Pethe), 9:1-43, 10:47-51.)

191. Pethe's disclosures of its Figure 3 embodiment support that Pethe's-Figure-5-Embodiment discloses claim 2. For example, Pethe's Figure 3F structure also includes inter-layer dielectric 330 that is **a second dielectric layer disposed on**

Pethe's first dielectric layer (of which region 323 is a part of) (**the first dielectric layer**), as shown in annotated Figure 3F below:

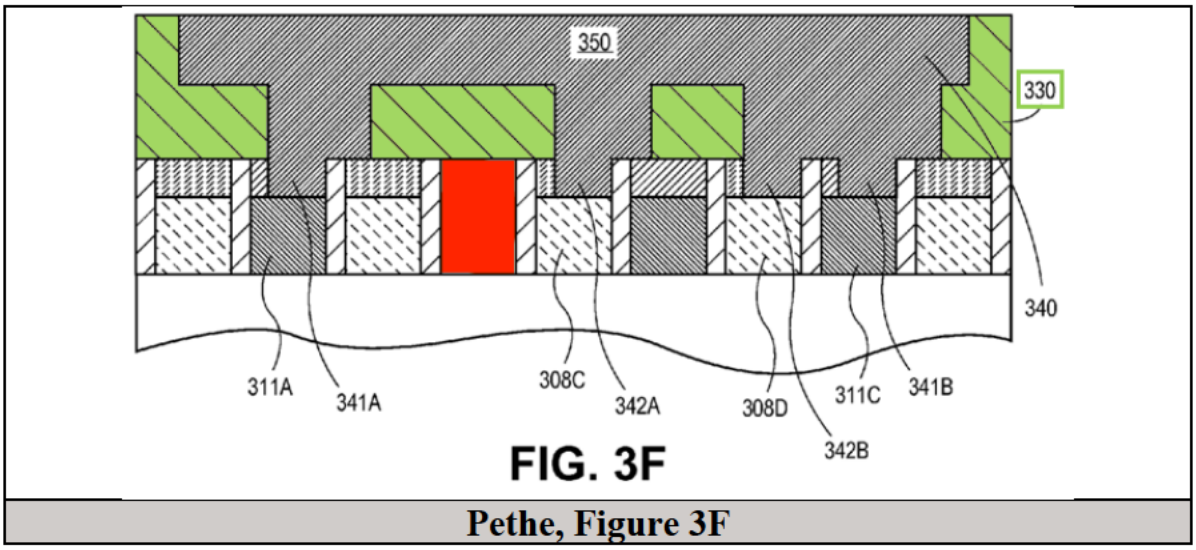


FIG. 3F

Pethe, Figure 3F

(EX1005 (Pethe), 9:1-43, 10:47-51.)

192. Thus, Pethe's disclosures of inter-layer dielectric 330 in Pethe's-Figure-3-Embodiment and Pethe's-Figure-5-Embodiment are the same for purposes of this limitation, for example, as shown below.

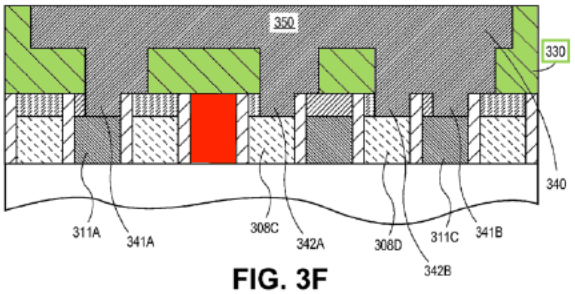


FIG. 3F

Pethe, Figure 3F

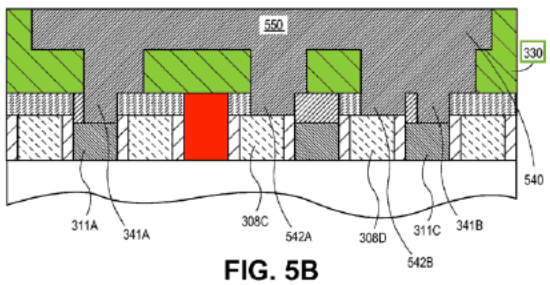


FIG. 5B

Pethe, Figure 5B

193. Accordingly, Pethe discloses the structure in Figure 5B discussed above for claim 1 (*See* §IX.A.1) includes a "**second dielectric layer …**" as recited in claim 2.

3. Claim 3

a) The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

194. In my opinion, Pethe discloses these limitations.

195. Pethe's Figure 5B structure includes insulating cap layer 324 that is **an etching stop layer disposed on two sides of** the gate stack structures 308A-308E, e.g., 308D (**the metal gate**).

196. The following annotations of Figure 5B that shows how Pethe discloses this limitation:

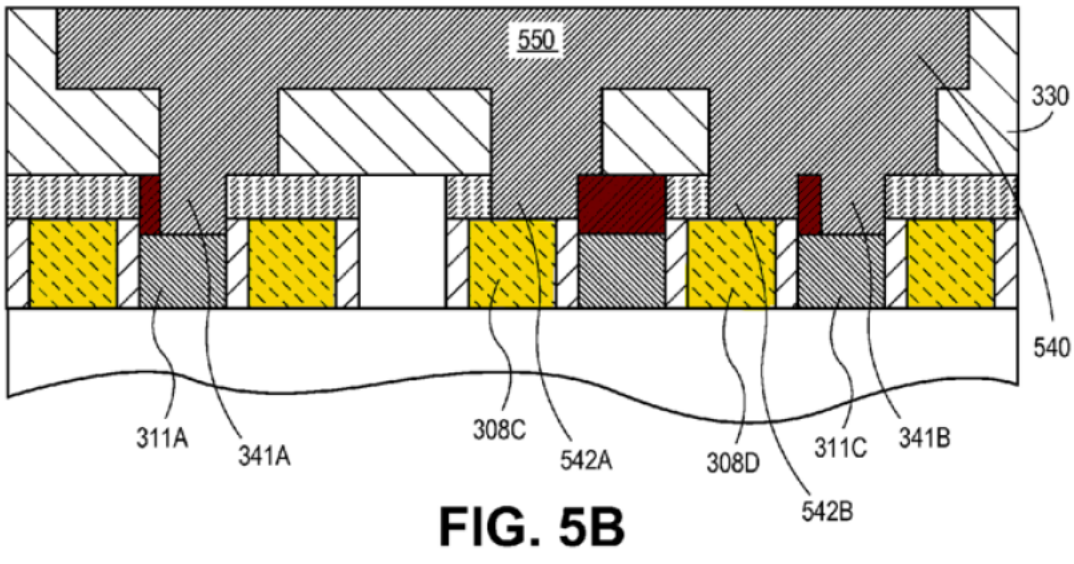


FIG. 5B

Pethe, Figure 5B

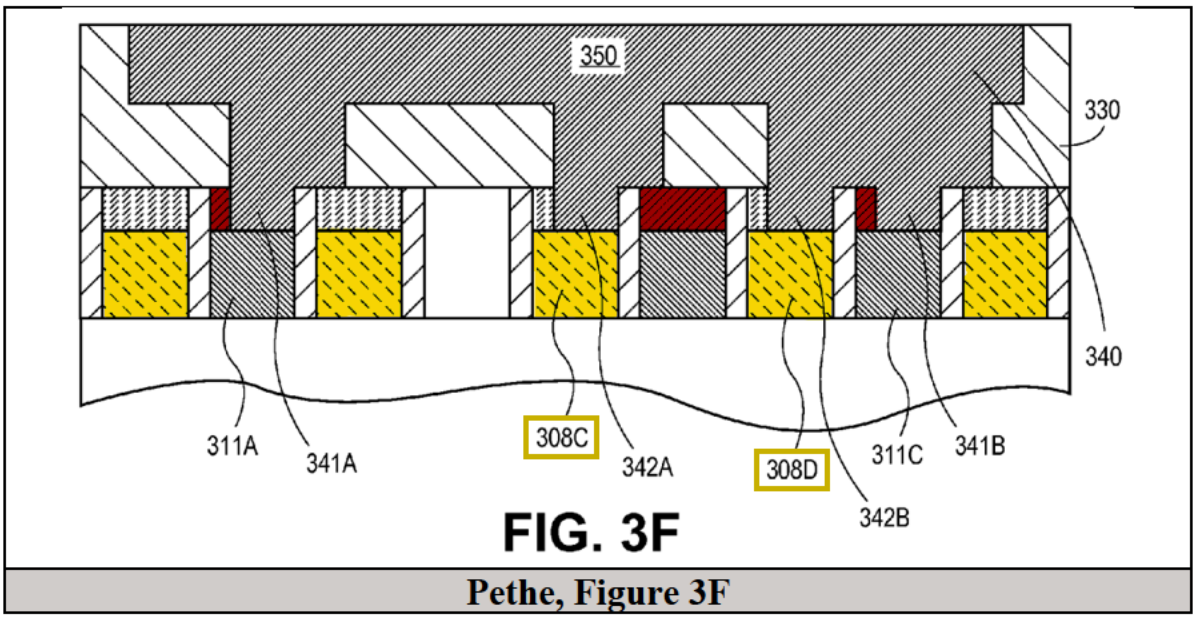


FIG. 3F

Pethe, Figure 3F

(EX1005 (Pethe), 12:32-13:12, 8:28-36, 8:41-51, 10:42-51.)

197. Pethe's disclosures of its Figure 3 embodiment support that Pethe's-Figure-5-Embodiment discloses claim 3. For instance, Pethe's FIG. 3F structure describes insulating cap layer 324 that is **an etching stop layer disposed on two sides of** the gate stack structures 308A-308E, e.g., 308D (**metal gate**).

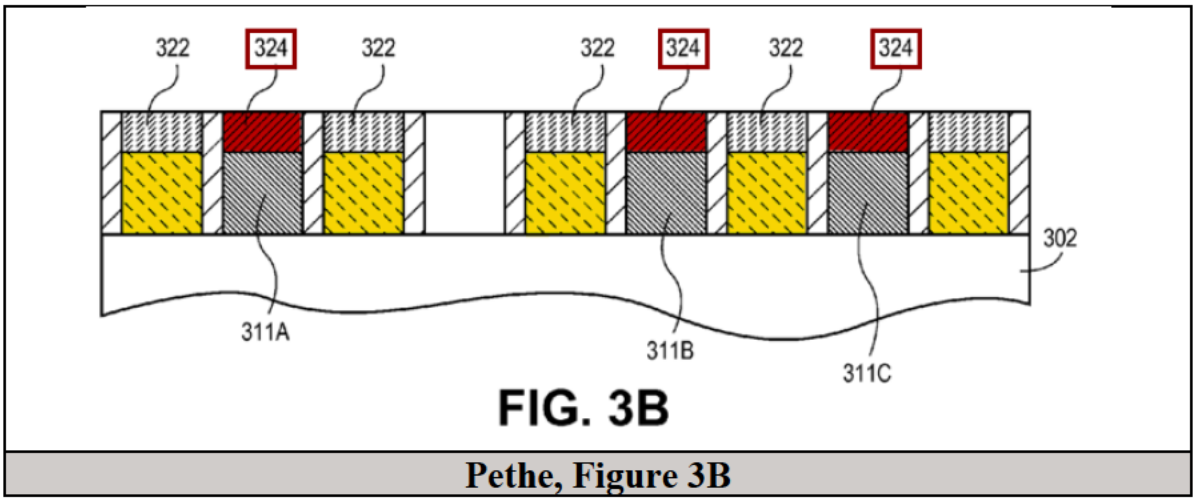


FIG. 3B

Pethe, Figure 3B

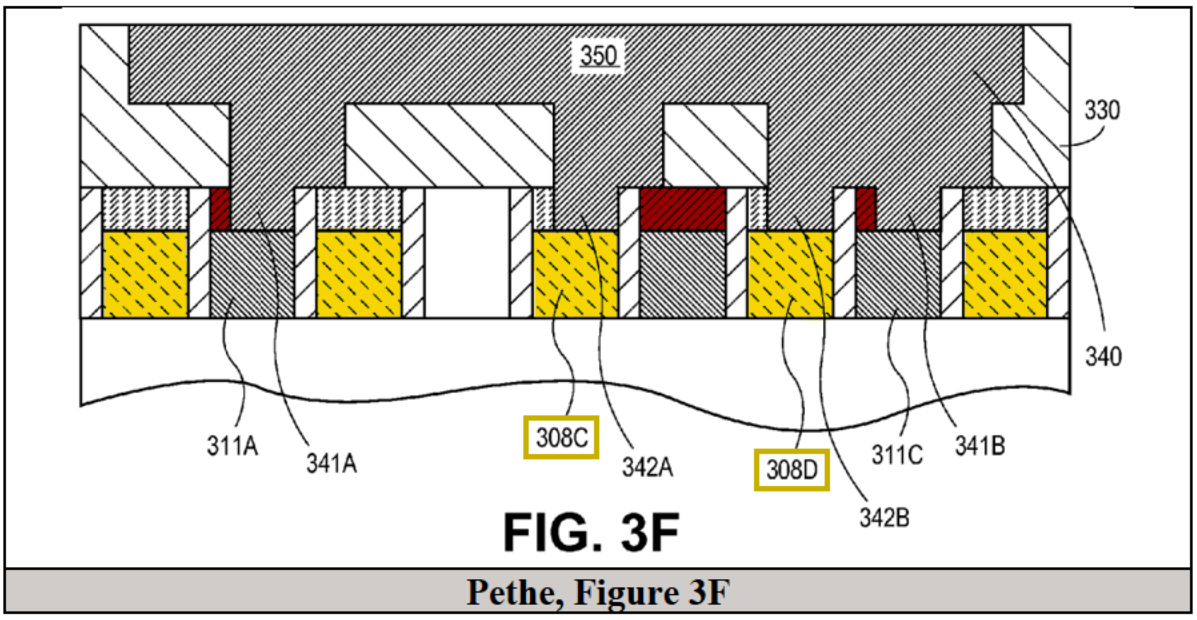


FIG. 3F

Pethe, Figure 3F

(EX1005 (Pethe), 8:28-36, 8:41-51, 10:42-51.)

198. During the etching step of Figure 3E, the "insulating cap layer 322 is etched to form via openings 338 **selective to (i.e., without significantly etching or impacting) insulating cap layer 324**," meaning that insulating cap layer 324 is an **etching stop layer**. (EX1005 (Pethe), 10:44-51, 10:62-64 ("an etch process without etching the insulating cap layer 324 (i.e., the trench contact insulating cap layers)").)

199. The following annotations of Figure 3E show insulating cap layer 324 during the etching step of Figure 3E:

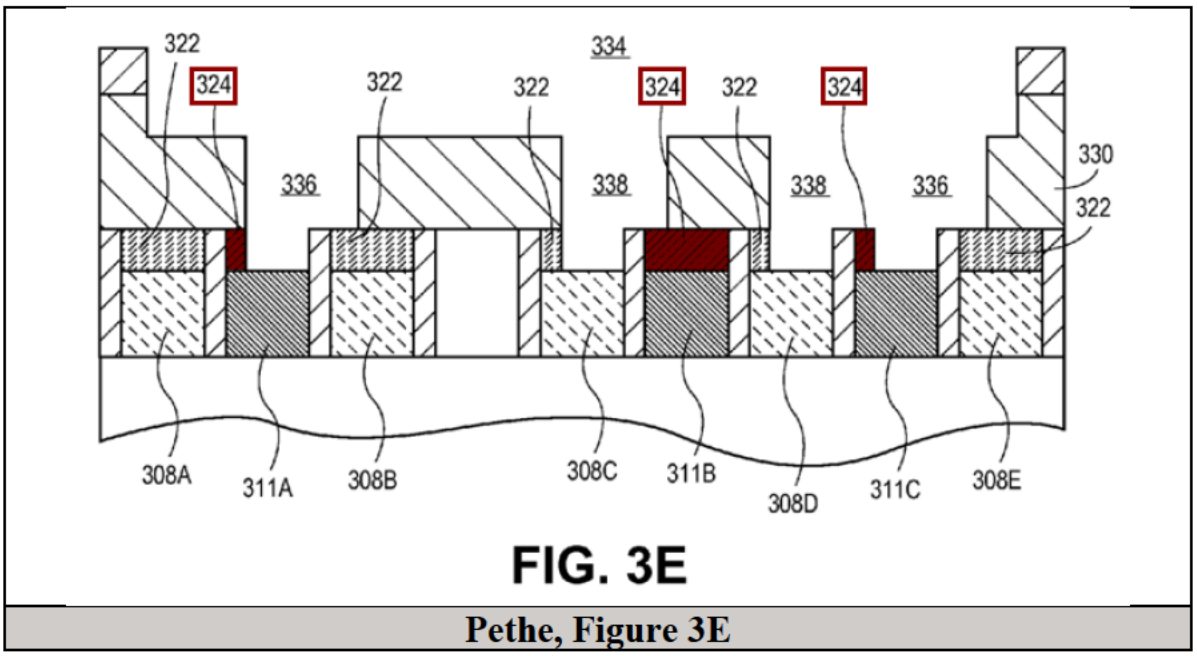


FIG. 3E

Pethe, Figure 3E

200. As shown in Figure 3E, insulating cap layer 324 is exposed during the etch, but is not removed. The insulating cap layer 324 is also shown in Figure 3F's structure (shown in dark red).

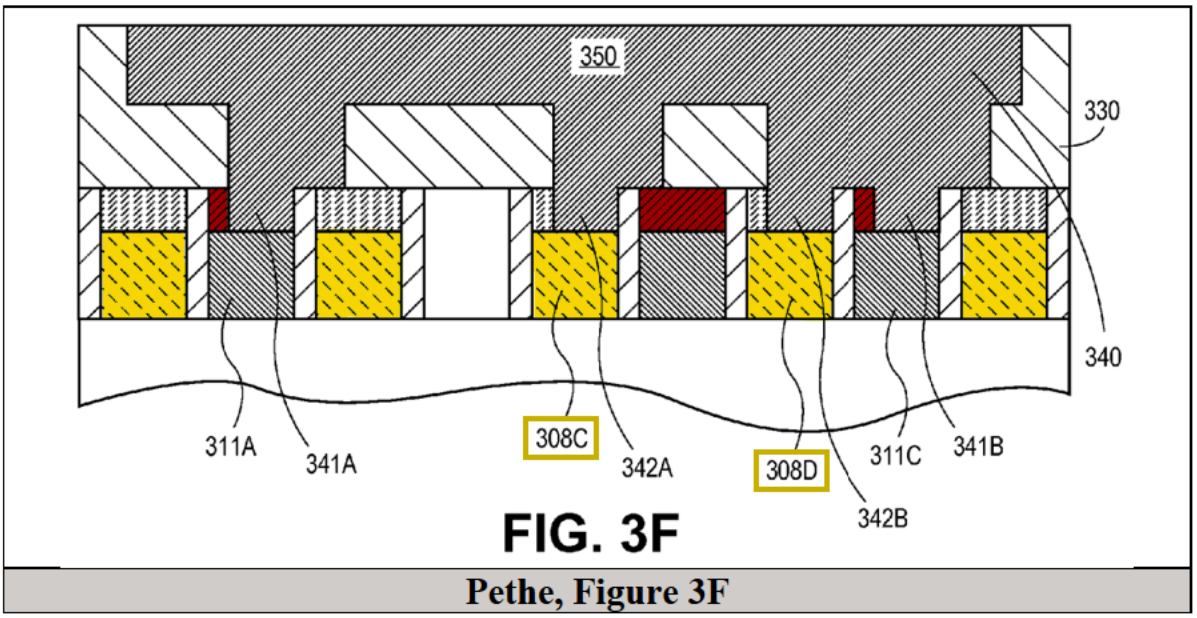


FIG. 3F

Pethe, Figure 3F

201. Insulating cap layer 324 **has a truncated top surface** because it is "planarized... by chemical mechanical polishing (CMP.)" (EX1005 (Pethe), 8:37-97

51.) The insulating cap layer 324 is formed as a conformal layer above the exposed portions of trench contacts 310A-310C, for example by chemical vapor deposition (CVD.) (EX1005 (Pethe), 8:41-44.) Afterwards, "[t]he conformal layer is then planarized, e.g., by chemical mechanical polishing (CMP), to provide insulating cap layer 324 material only above trench contacts 310A-310C, and re-exposing spacers 320 and insulating cap layer 322." (EX1005 (Pethe), 8:47-51.) This removal of the top portion of insulating cap layer 324 by polishing results in **a truncated top surface**.

202. As I discussed in the Overview of Pethe (VII.A), the introduction to Ground 1 (§IX.A), and the preamble of claim 1 (§IX.A.1.a), Pethe's Figure 5B structure has undergone the fabrication steps of Figures 3B-3E.

203. Thus, insulating cap layer 324 in Pethe's-Figure-3-Embodiment and Pethe's-Figure-5-Embodiment are the same for purposes of this limitation, as shown below.

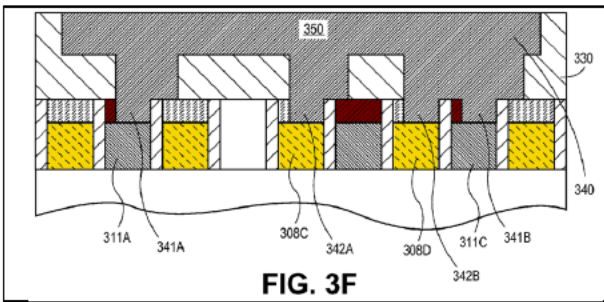


FIG. 3F

Pethe, Figure 3F

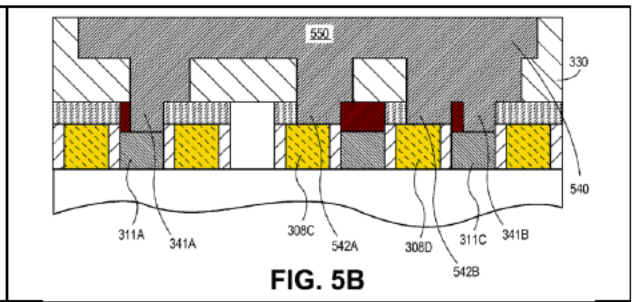


FIG. 5B

Pethe, Figure 5B

204. Accordingly, in my opinion, the structure of Figure 5B includes an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface, like that claimed in claim 3.

4. Claim 4

a) The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

205. In my opinion, Pethe discloses these limitations.

206. For example, Pether's Figure 3F structure includes trench contact vias 341A and 341B (**the first contacts**) are **disposed in** Pethe's first dielectric layer (of which region 323 is a part of) (**the first dielectric layer**) and inter-layer dielectric 330 (**the second dielectric layer**), as shown in annotated Figure 5B below.

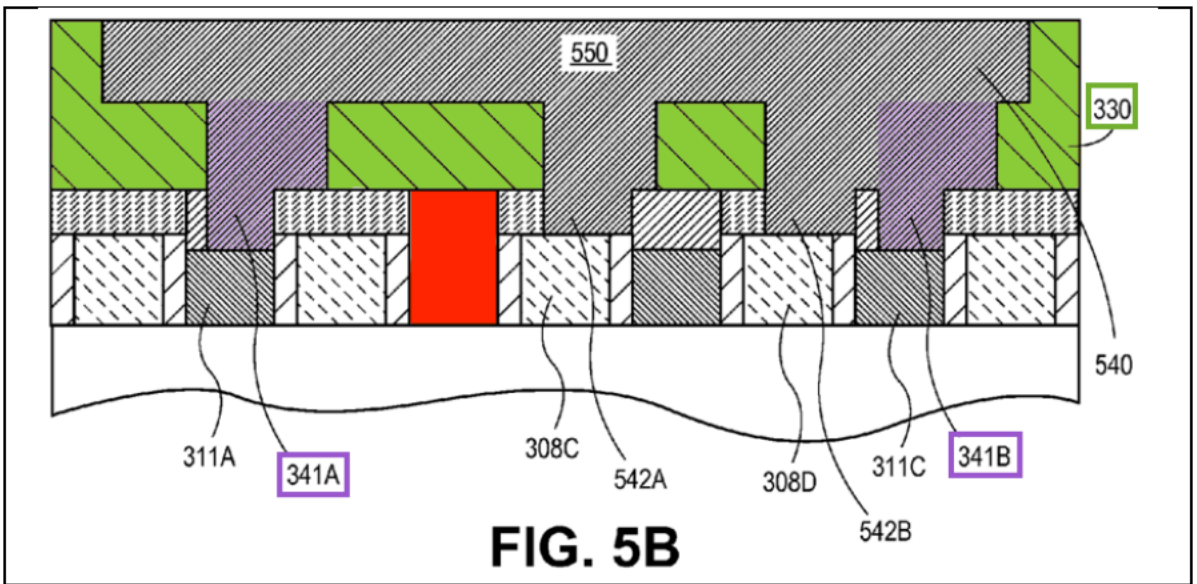


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 12:32-13:12, 11:23-31, 9:1-43, 7:15-34.)

207. Pethe explains in reference to FIG. 5B that "a metal contact structure 540 is formed in a metal (0) trench and via openings formed in a **dielectric layer 330**" (**second dielectric layer**). (EX1005 (Pethe), 12:54-56.) Pethe further explains that "contact structure 540 includes… trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively)" (EX1005 (Pethe), 12:56-58), confirming trench contact vias 341 (**first contacts**) are disposed in ILD 323 (**first dielectric layer**) and dielectric layer 330 (**second dielectric layer**), and are monolithically formed.

208. Pethe's disclosures of its Figure 3 embodiment support that Pethe's-Figure-5-Embodiment discloses claim 4. For example, Pethe explains trench contact vias 341A, 341B (**first contacts**) are **disposed in** Pethe's first dielectric layer (of which region 323 is a part of) (**the first dielectric layer**) and inter-layer dielectric 330 (**second dielectric layer**), as shown in annotated Figure 3F below.

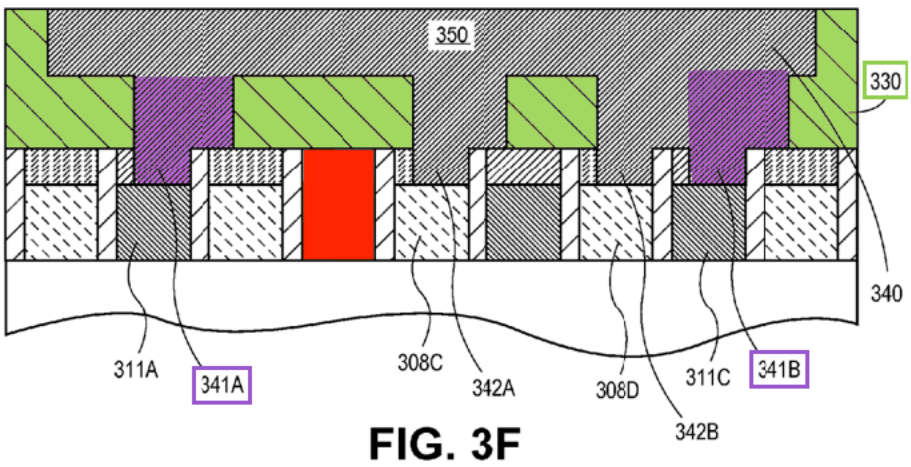


FIG. 3F

Pethe, Figure 3F

(EX1005 (Pethe), 11:23-31, 9:1-43, 7:15-34.)

209. Each trench contact vias 341A and 341B **(first contact) is a monolithically formed structure** because each is formed from an opening 336 being filled by a single metal contact structure 340. As shown in the annotated Figure 3D below, trench contact vias 341A and 341B are formed in openings 336.

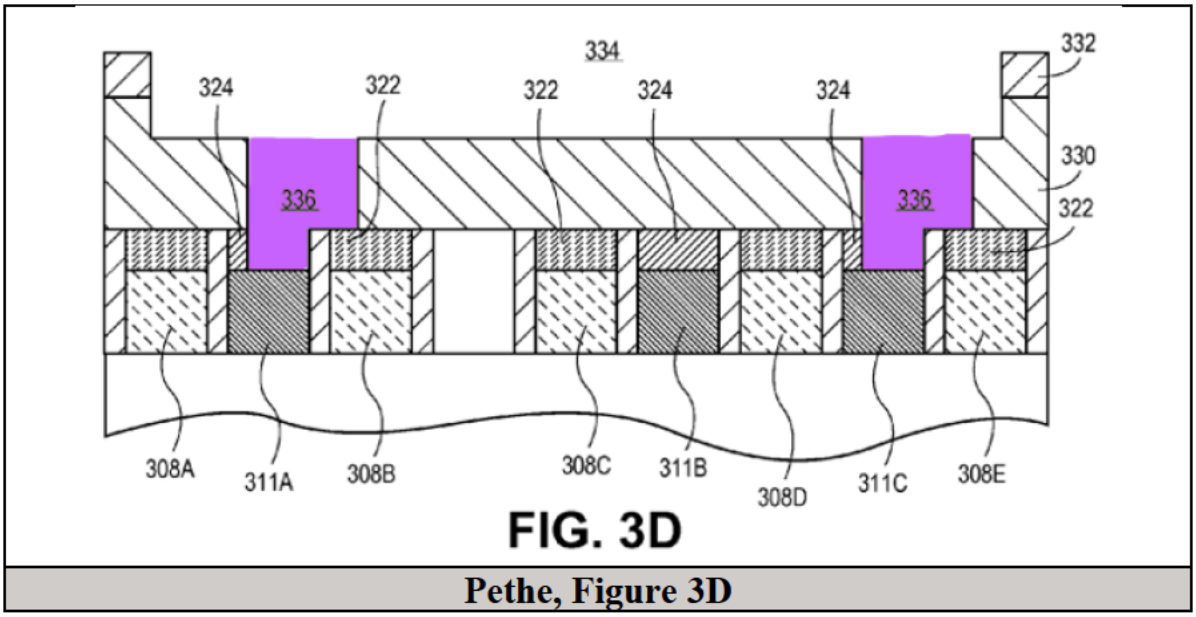


FIG. 3D

Pethe, Figure 3D

(EX1005 (Pethe), 9:29-10:36.)

210. A POSITA would have understood that in Figure 3F, a single metal deposition (*i.e.*, "a deposition of **a fill metal layer**") fills the space of openings 336 to form trench contact vias 341A and 341B each as a **monolithically formed structure**.

> Referring to FIG. 3F, a metal contact structure 340 is formed in the metal (0) trench 334 and via openings 336 and 338 of the structure described in association with FIG. 3E. **The metal contact structure**

> **340 includes** a metal (0) portion 350 along with **trench contact vias** (e.g., **trench contact vias 341A and 341B** to trench contacts 311A and 311C, respectively) and gate contact vias (e.g., gate contact vias 342A and 342B to gate stack structures 308C and 308D, respectively).
>
> In an embodiment, **the metal contact structure is formed by a metal deposition** and subsequent chemical mechanical polishing operation. The metal deposition may involve first deposition of an adhesion layer followed by **deposition of a fill metal layer**. Thus, the metal structure 340 may be composed of a conductive material. In an embodiment, the metal structure 340 is composed of a metal species. The metal species may be a pure metal. Such as copper, tungsten, nickel or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., Such as a silicide material).

(EX1005 (Pethe), 11:23-42.)

211. As I discussed in the Overview of Pethe (§VII.A), the introduction to Ground 1 (§IX.A), and the preamble of claim 1 (§IX.A.1.a), Pethe's Figure 5B structure has undergone the fabrication steps of Figures 3B-3E.

212. Thus, Pethe's-Figure-5-Embodiment discloses claim 4 for reasons explained by Pethe for its Figure-3-Embodiment. Pethe's formation of trench contact vias 341A, 341B, and positioning of 341A, 341B with respect to Pethe's first dielectric layer (of which region 323 is a part of) and inter-layer dielectric 330 in

these embodiments are the same for purposes of this limitation, for example, as shown below.

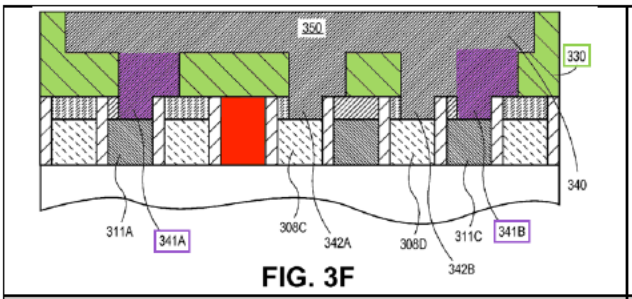


FIG. 3F

Pethe, Figure 3F

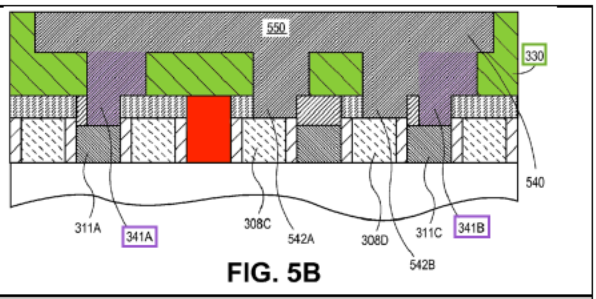


FIG. 5B

Pethe, Figure 5B

5. Claim 5

a) The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

213. In my opinion, Pethe discloses these limitations.

214. For example, the Figure 5B structure includes gate contact vias 542A and 542B (**second contacts**) that are **disposed in the first dielectric layer** (of which ILD region 323 is a part) and inter-layer dielectric 330 (**the second dielectric layer**), as shown in Figure 5B.

215. The following annotations of Figure 5B show how Pethe discloses this limitation:

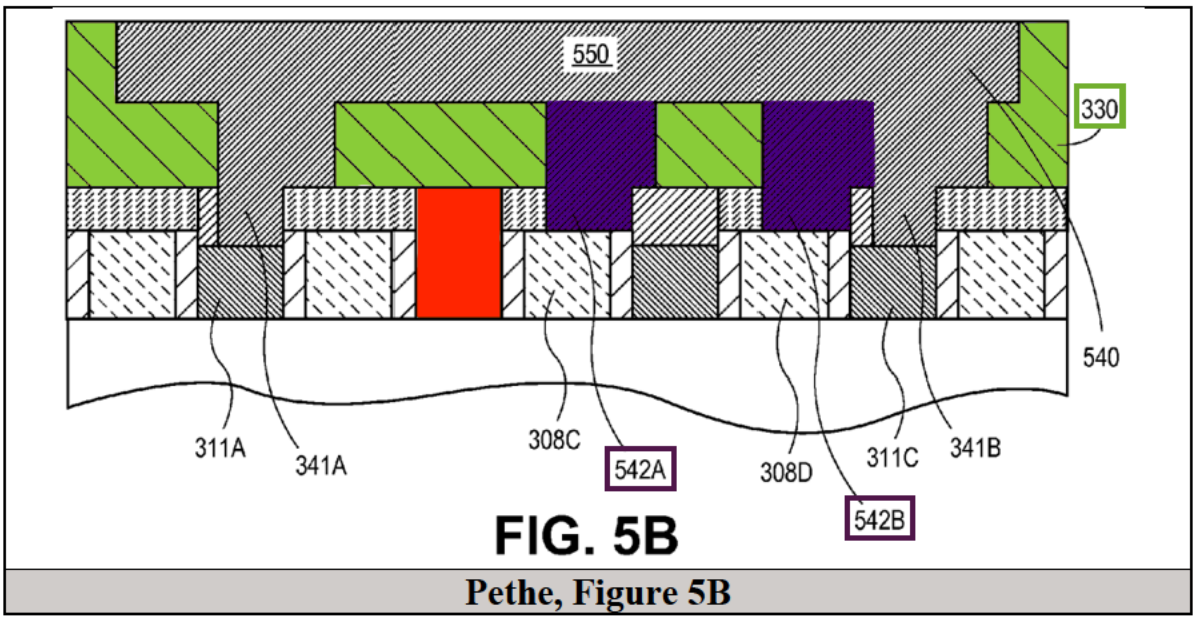


FIG. 5B

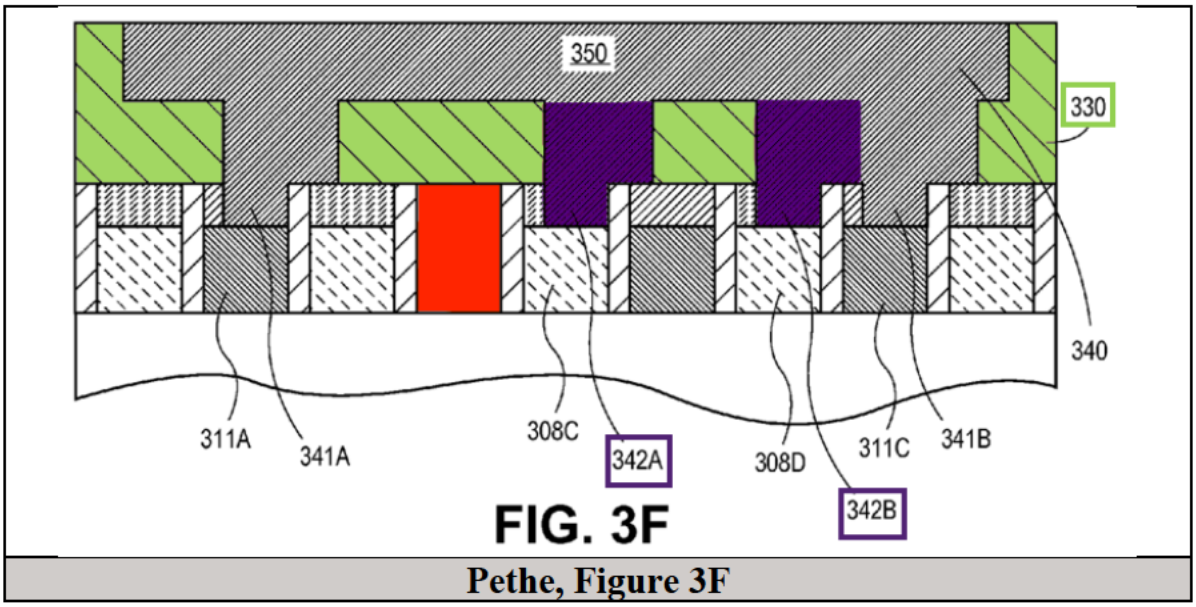
Pethe, Figure 5B

(EX1005 (Pethe), 12:54-13:12, 11:23-31, 9:1-43, 7:15-34)

216. Pethe explains, with reference to Figure 5B, that "a metal contact structure 540 is formed in a metal (0) trench and via openings formed in a **dielectric layer 330**" (**second dielectric layer**). (EX1005 (Pethe), 12:54-56.) Pethe further explains that "contact structure 540 includes… gate contact vias (e.g., gate contact vias 542A and 542B to gate structures 308C and 308D, respectively)" (EX1005 (Pethe), 12:59-62), confirming gate contact vias 542 (**second contacts**) are disposed in ILD 323 (**first dielectric layer**) and dielectric layer 330 (**second dielectric layer**), and are monolithically formed.

217. Pethe's disclosures of its Figure 3 embodiment support that Pethe's-Figure-5-Embodiment discloses claim 5. For example, Pethe discloses gate contact vias 342A and 342B (**second contacts**) are **disposed the first dielectric layer** (of

which ILD region 323 is a part) (**first dielectric layer**) and inter-layer dielectric 330 (**second dielectric layer**), as shown in annotated Figure 3F below.



Pethe, Figure 3F

(EX1005 (Pethe), 11:23-42, 9:1-43, 7:15-34.)

218. In my opinion, each of gate contact vias 342A and 342B (**second contact**) in the Figure 3F structure **is a monolithically** formed **structure** because each is formed from an opening 338 filled by a single metal contact structure 340. This is shown below via annotated Figure 3E, where gate contact vias 342A and 342B are formed in openings 338.

219. I have prepared the following annotations of Figure 3E that show openings 338:

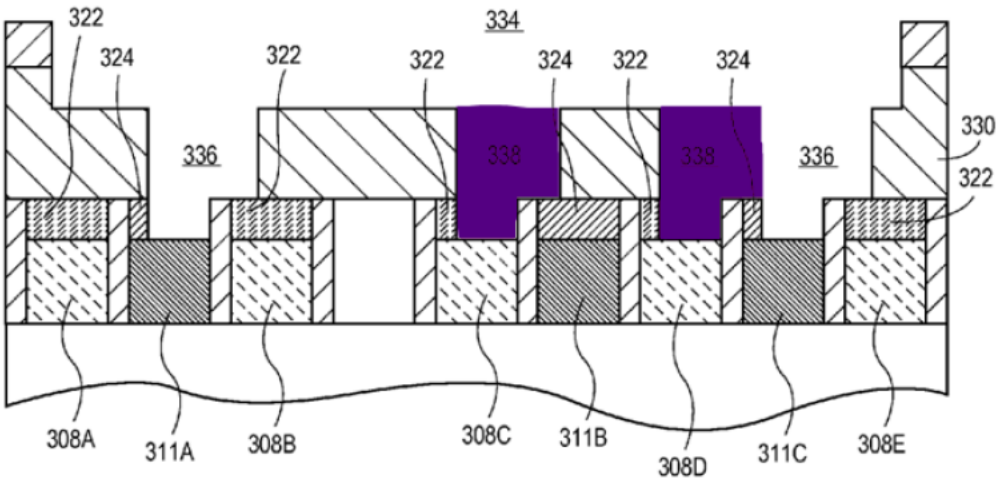


FIG. 3E

Pethe, Figure 3E

(EX1005 (Pethe), 10:37-11:22.)

220. In Figure 3F, a single metal deposition (*i.e.*, "a deposition of **a fill metal layer**") fills the space of openings 338 to form gate contact vias 342A and 342B each as a **monolithically formed structure**. (EX1005 (Pethe), 11:23-42.)

> Referring to FIG. 3F, a metal contact structure 340 is formed in the metal (0) trench 334 and via openings 336 and 338 of the structure described in association with FIG. 3E. **The metal contact structure 340 includes** a metal (0) portion 350 along with trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively) **and gate contact vias** (e.g., gate contact vias 342A and 342B to gate stack structures 308C and 308D, respectively).
>
> In an embodiment, **the metal contact structure is formed by a metal deposition** and subsequent chemical mechanical polishing operation. The metal deposition may involve first deposition of an

> adhesion layer followed by **deposition of a fill metal layer**. Thus, the metal structure 340 may be composed of a conductive material. In an embodiment, the metal structure 340 is composed of a metal species. The metal species may be a pure metal. Such as copper, tungsten, nickel or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., Such as a silicide material).

(EX1005 (Pethe), 11:23-42.)

221. As I discussed in the Overview of Pethe (§VII.A), the introduction to Ground 1 (§IX.A), and the preamble of claim 1 (§IX.A.1.a), Pethe's Figure 5B structure has undergone the fabrication steps of Figures 3B-3E.

222. Thus, Pethe's-Figure-5-Embodiment discloses claim 5 for reasons similar to those described by Pethe's-Figure-3-Embodiment. Pethe's formation of gate contact vias 542A, 542B and gate contact vias 342A, 342B, and their positioning with respect to Pethe's first dielectric layer (of which region 323 is a part of) and inter-layer dielectric 330 in Pethe's-Figure-3-Embodiment and Pethe's-Figure-5-Embodiment are the same for purposes of this limitation, as shown below.

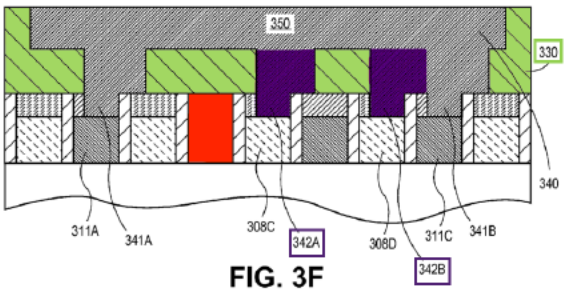


FIG. 3F

Pethe, Figure 3F

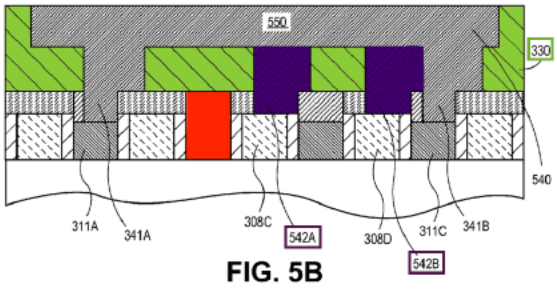


FIG. 5B

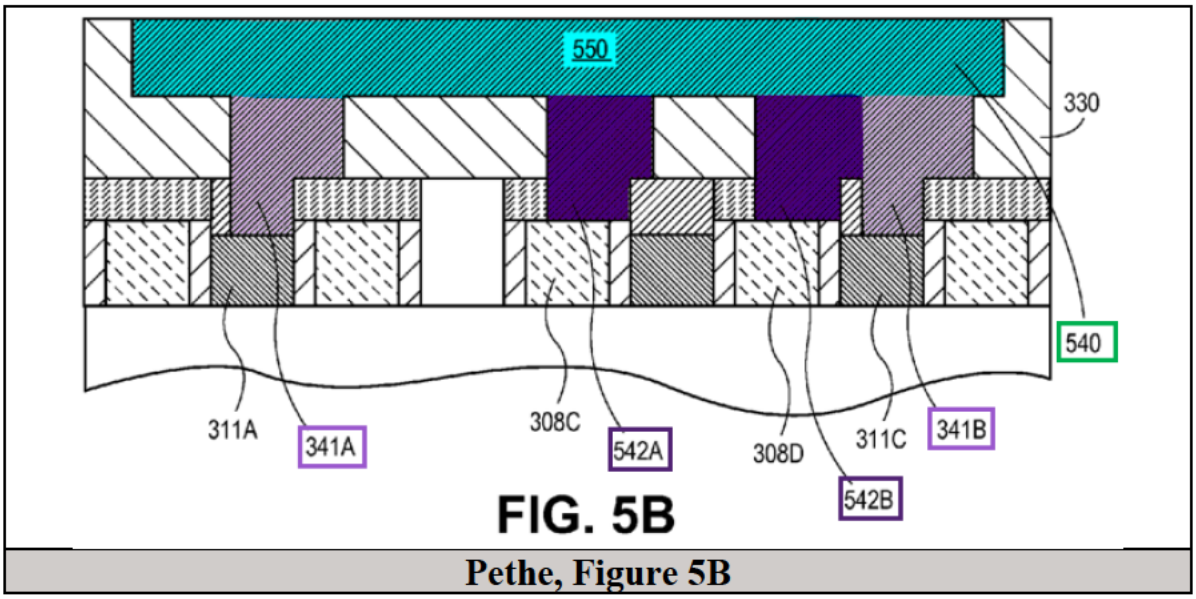
Pethe, Figure 5B

6. Claim 8

a) The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

223. In my opinion, Pethe discloses these limitations.

224. For example, Pethe's Figure 5B structure includes a metal (0) portion 350 that includes **a plurality of third contacts**. (EX1005 (Pethe), 11:23-31.) As shown in Figure 5B, the metal (0) portion 350 is **disposed on** trench contact vias 341A and 341B (**parts of the first contacts**) and on gate contact vias 542A and 542B (**parts of the second contacts**.)



Pethe, Figure 5B

(EX1005 (Pethe), 12:54-13:12, 11:23-31.)

225. Pethe explains, with reference to Figure 5B, that "metal contact structure 540 **is formed in a metal (0) trench and via openings**." (EX1005 (Pethe),

12:54-56.) Pethe also explains that "metal (0) portion" is "550," and 540 also comprises "trench contact vias" (341) and "gate contact vias" (542), which contact trench contacts (311) and gate stack structures (308) respectively. (EX1005 (Pethe), 12:56-62.) Consistent with this disclosure, 550 is monolithically formed (as part of 540) and shown in Figure 5 **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and gate contact vias 542A, 542B (**parts of the second contacts**).

226. Pethe's disclosures of its Figure 3 embodiment support that Pethe's-Figure-5-Embodiment discloses claim 8. For example, Pethe teaches metal (0) portion 350 ("350") including **a plurality of third contacts**. (EX1005 (Pethe), 11:23-31.) As shown in annotated Figure 3F below, 350 is **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and gate contact vias 342A, 342B (**parts of the second contacts**.)

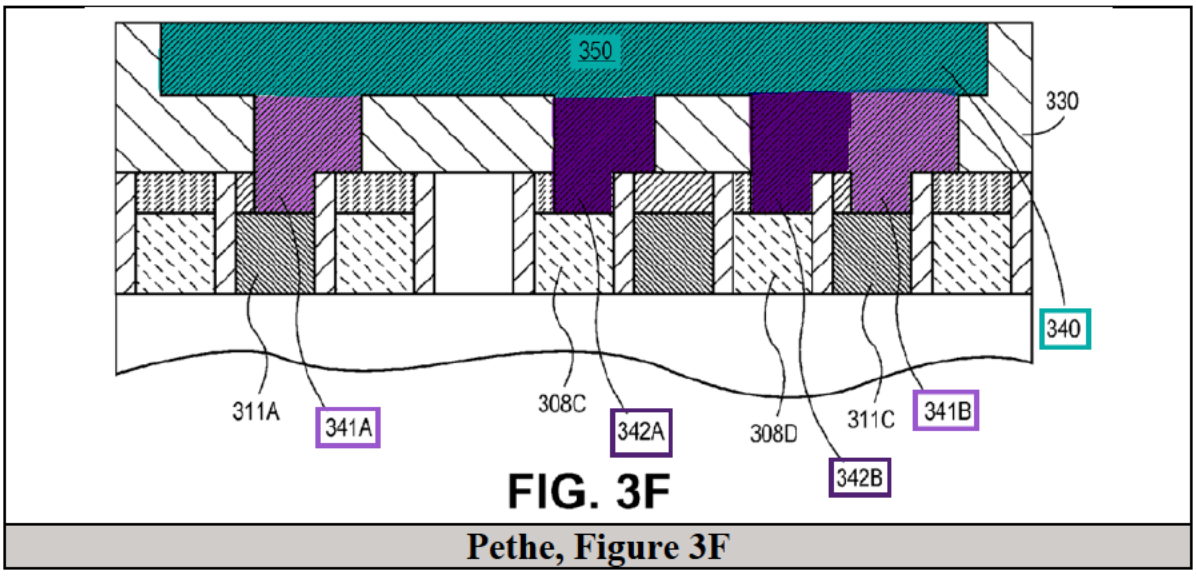


FIG. 3F

Pethe, Figure 3F

227. A POSITA would have understood that metal (0) portion 550/350 would comprise a metal line interconnect structure with **a plurality of contacts** (e.g., metal lines) each connecting to **parts of the first and second contacts**.

228. For example, Pethe discloses "a metal (0) portion" 550/350 and "trench contact via (e.g., trench contact vias 341A and 341B … and gate contact vias (e.g., gate contact vias" 542A/342A and 542B/342B. (Ex. 1005, 11:26-31). Metal (0) portion 550/350 is formed in metal (0) trench. Metal (0) is a known term for an interconnect structure of metal lines on the metal (0) layer. Further, Pethe refers to the structures above the vias (i.e., the trench contact vias and gate contact vias) as a "metal interconnect" structure. (EX1005 (Pethe), 3:50-4:8 (discussing "overlying metal interconnect 160"), 4:56-5:10 (discussing "overlying metal interconnect 260"), 11:59-64 (discussing "overlying metal interconnect 460").)

229. A "metal interconnect" at the metal (0) layer would have been understood by a POSITA to include a networks of metal lines.

230. Thus, Pethe's-Figure-5-Embodiment discloses claim 8 for reasons similar to that described by Pethe's-Figure-3-Embodiment. Pethe's-Figure-3-Embodiment's metal (0) portion 350 and Pethe's-Figure-5-Embodiment's metal (0) portion 550 are the same for purposes of this limitation, for example, as shown below.

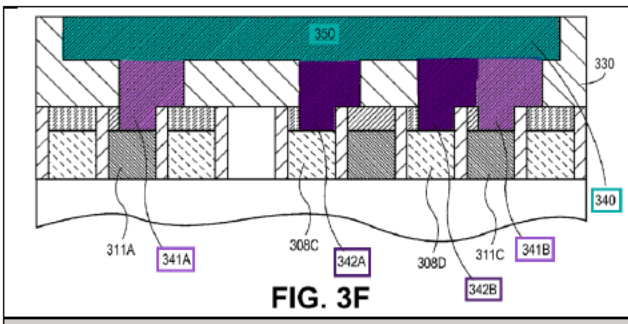


FIG. 3F

Pethe, Figure 3F

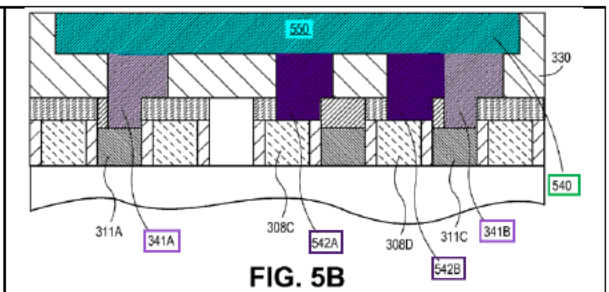


FIG. 5B

Pethe, Figure 5B

7. Combination of Pethe's Embodiments

231. Pethe discloses various aspects regarding the formation of and resulting semiconductor structures. EX1005 (Pethe), 1:49-2:46, 2:64-7:14 (Figures 1-2C), 7:9-11:42 (Figures 3A-3F), 11:43-12:14 (Figure 4), 12:15-13:12 (Figures 5A-5B), 13:13-21, 13:23-43 (Figure 6), 13:44-14:38 (Figure 7), 14:29-15:38 (Figure 8), 14:39-17:18. While as I explained, Pethe's disclosures of Figures 5A-5B describe features common to those described for Figures 3A-3F (*see* discussion in Overview of Pethe (§VII.A), the introduction to Ground 1 (§IX.A), and the preamble of claim 1 (§IX.A.1.a)), Pethe does not expressly incorporate other teachings. However, a POSITA would have been motivated to combine teachings from other aspects of Pethe when considering and implementing the Figure 5B structure addressed above in Ground 1.

232. As explained above, in discussing Figures 5A-5B, Pethe does not repeat details/discussions related to features common to Figures 3A-3F, such as for example, substrate 302, ILD region 323, dielectric layer 330, trench contact vias

341A/341B, trench contacts 311A/311C (all similarly labeled in Figures 3A-3F and 5A-5B), and cap layer 522 (same as cap layer 322 but wider because of recessed spacers 520), gate via contacts 542A/542B (same as gate contact vias 342A/342B), and metal (0) portion 550 (same as metal (0) portion 350). EX1005 (Pethe), FIGs. 3A-3F, 5A-5B, 2:3-63, 7:9-11:42, 12:22-13:12.

233. As I noted above, in my opinion and experience, when a patent uses the same name and reference number in different Figures for an element (for example, trench contacts 311A/311C in Figure 3F and Figure 5B), the text disclosures describing the element for one Figure apply to the element on the other Figures, as they are the same element (unless otherwise noted). This is similarly true when the patent updates the first number of the reference number in accordance with the Figure number (for example, gate contact vias **3**42A/**3**42B in Figure **3**F and gate via contacts **5**42A/**5**42B in **F**igure 5B). It is my opinion that a POSITA would have understood the same understanding in context of Pethe's disclosures, which discusses the same elements for the Figure 5B structure in the Figure 5 embodiment and for the Figure 3 embodiment, as exemplified below

234. A POSITA would have been motivated to incorporate such teachings, as Pethe relates the various aspects of its disclosed invention. *See for example*, EX1005 (Pethe), 15:39-41 (explaining after discussing Figures 1-8, "[t]hus, embodiments of the present invention include gate contact structures disposed over

active portions of gates and methods of forming such gate contact structures"), 2:50-63. In reviewing Pethe, it is clear that Pethe references discussions from other figures and/or aspects of the invention when describing a given embodiment. *See e.g. id.*, 4:39-42, 5:15-34, 7:22-25, 9:15-20, 11:23-25, 12:15-31, 12:39-42, 12:48-53.

235. With such teachings/suggestions, a POSITA would have been motivated to consider and implement from teachings related to other aspects of Pethe's invention when forming/configuring the Figure 5B structure, and would have had a reasonable expectation of success in achieving such implementations. This is true especially considering the fact that the implementation of combined features would have involved techniques and technologies already contemplated by the teachings of Pethe. *Id*. Thus, for these reasons, and those further discussed below, a POSITA would have been motivated to combine certain teachings from the various disclosed aspects of Pethe to Pethe's Figure 5B structure, and would predictably have resulted in a structure meeting the identified challenged claims as explained below. *Id*.

236. In addition to Pethe's discussions of features related to Figures 3A-3F being included in the teachings for the Figure 5B structure, a POSITA would also have been motivated to consider and implement them when forming/configuring the Figure 5B structure (as discussed above in §§IX.A.1-7), and would have had a

reasonable expectation of success in doing so. In my opinion, a POSITA would have recognized and appreciated that Pethe relates/references features between embodiments in describing the disclosed invention (for example, EX1005 (Pethe), 2:50-63, 4:39-42, 5:15-34, 7:22-25, 9:15-20, 11:23-25, 12:15-31, 12:39-42, 12:48-53., 15:39-41), and thus been motivated to incorporate such combined teachings to yield the predictable result of a structure as discussed above for claims 1-5 and 8. §§IX.A.1-7.

B. Ground 2: Pethe Discloses and/or Suggests Claims 6-7

237. For my Ground 2 analysis, I incorporate my Ground 1 analysis, which demonstrates how Pethe's-Figure-5-Embodiment discloses and/or suggests **claims 1-5 and 8**. (*See section* §IX.A incorporated herein by reference.)

238. For instance, claims 6 and 7 depend from claim 1. My opinions above for Ground 1 demonstrates how Pethe's Figure 5B structure discloses claim 1. *Above* §IX.A.1, which I incorporate herein. Pethe further discloses/suggests claims 6-7 for the reasons below.

1. Claim 6

a) The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

239. In my opinion, Pethe discloses and/or suggests this limitation.

240. For example, Pethe describes the formation of fin structures in context of its disclosed semiconductor structures. Pethe explains that the disclosed semiconductor devices may be transistors or like devices, including a "TRI-GATE" and "FIN-FET," which were both known to include fins. (EX1005 (Pethe), 5:35-39, 14:8-11, 1:27-35.) Consistent with this understanding, Pethe refers to forming "fins in a bulk semiconductor substrate" (*id.*, 17:17-18), refers to a non-planar diffusion or active region in the Figure 1C, Figure 2A, and Figure 4 structures as "a fin structure" (*id.*, 3:60-67, 4:65-5:3, 11:49-52) and contemplates the Figure 2B structure 200 as a "fin-FET" or "tri-gate" transistor device (*id.*, 5:35-39). (*See also id.*, 6:7-12 ("fin active regions").)

241. Notwithstanding Pethe's teachings, it is my opinion that a POSITA would have been motivated in light of Pethe's teachings and suggestions to configure Figure 5B's structure (discussed above for claim 1 in § IX.A.1) with at least one fin structure disposed on the substrate. A POSITA would have been motivated to consider and implement fin structure features similar to those discussed above for the FIGs. 1, 2, 4 and other embodiments described by Pethe (*see* fin structure citations to Pethe above) in the Figure 5 embodiment structure to apply Pethe's Figure 5B structure to multi-gate transistors (for example, FinFET, TRI-GATE transistor) configurations, consistent with a POSITA's knowledge of the use of fin structures at the time. (*See* §V.)

242. In my opinion, Pethe recognized that "multi-gate transistors" are "fundamental building blocks of microelectronic circuitry," "fabricated by conventional processes," and "prevalent as device dimensions continue to scale down." (EX1005 (Pethe), 1:27-45.) As Pethe further explains, such "multi-gate transistors" are "consequent[ial]" to address "scaling of features in integrated circuits"—the "driving force behind an ever-growing semiconductor industry." (EX1005 (Pethe), 1:14-19, 1:36-42.).

243. Consistent with this disclosure, Pethe explains that Figure 5 embodiment's gate structure "may include a gate dielectric layer and a gate electrode, **as described above in FIG. 2**," which discloses a multi-gate transistor having a fin structure. (EX1005 (Pethe), 12:39-42.) Pethe's Figure 2 embodiment's gate structure is for use with and "disposed over the non-planar diffusion or active region 204C," which Pethe identifies as a "fin structure." (EX1005 (Pethe), 4:62-5:5; FIG. 2C (showing "tri-gate transistor" including gate structure comprising gate electrode 205/ gate dielectric layer 252 disposed over fin structure 204C).)

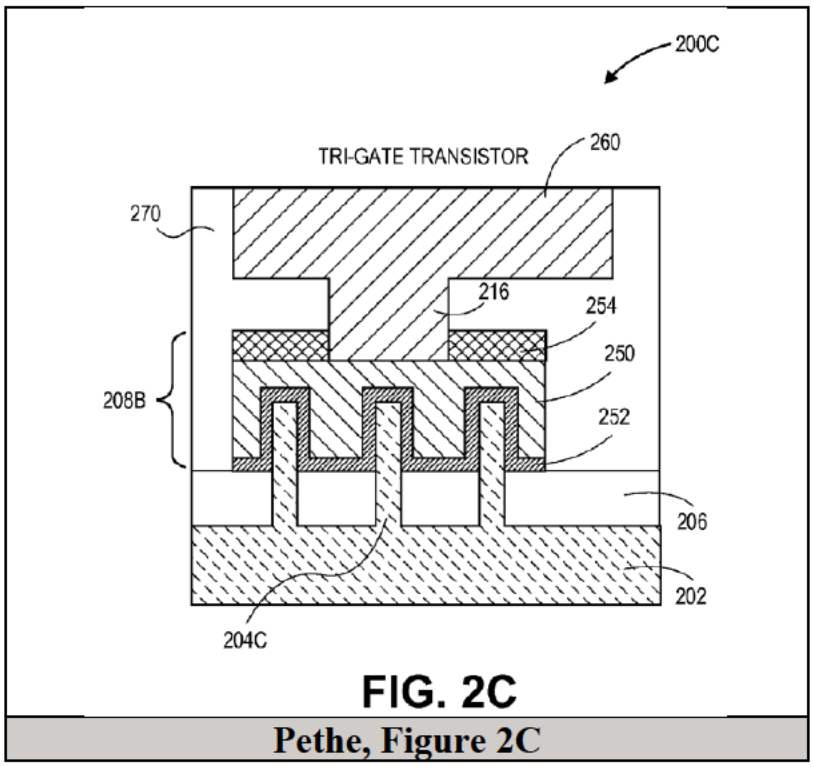
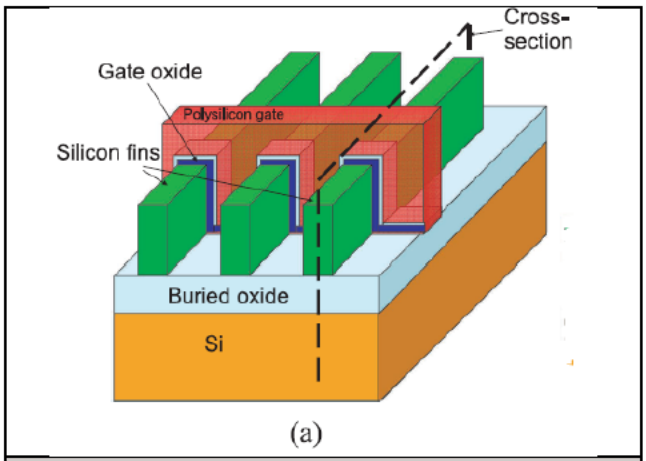


FIG. 2C

Pethe, Figure 2C

244. A POSITA would have understood that the use of fin structures in transistor semiconductor devices was well known at the time, as evidenced by Pethe's repeated disclosures of such devices.

245. FETs were known in the art at the relevant time to include non-planar three-dimensional (3D) FETs, such as FinFETs and tri-gate transistors.



EX1020, Figure 9.41 (FinFET)

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 351, 72-74.)

246. For example, Pethe explicitly describes non-planar FETs, such as "tri-gate transistors" (which were known to include fins, see below), as "prevalent" and "conventional":

> For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, **shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity**. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.
>
> In the manufacture of integrated circuit devices, multi-gate transistors, such as **tri-gate transistors, have become more prevalent as device**

> **dimensions continue to scale down**. In **conventional processes**, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and because they enable a less complicated tri-gate fabrication process.

(EX1005 (Pethe), 1:14-35.)

247. Pethe also recognizes the benefits of non-planar structures with fins – by exploiting the vertical dimension, non-planar structures allow for more transistors "on the limited real estate of semiconductor chips." (*Id*.) It would have been widely recognized by a POSITA that non-planar structures with fins were advantageous due to their small footprint, as the "scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry." (*Id*.) It was conventionally recognized that "shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity." (*Id*.)

248. As explained below, non-planar structures with fins (such as tri-gate and FinFet structures) were known to provide reduced feature size: "[b]y folding the active area (AA) of a planar MOSFET into a thin strip like **a fin**, **device dimensions can be dramatically reduced without feature size shrinkage**." (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 650-51.)

249. Non-planar structures such as tri-gate and FinFet structures described by Pethe were known to include fins. As explained in *Introduction to Semiconductor Manufacturing Technology*:

> Planar MOSFETs have been used as basic IC building blocks for more than half a century. Because traditional scaling is rapidly approaching its physical limit, and the cost to scale technology nodes in the deep nanometer range has skyrocketed, fabs are actively looking for other approaches to extend technology development. One promising technology is the **3D multiple-gate field effect transistor, or MuGFET**. Figure 15.1 shows a MuGFET on a SOI substrate. By folding the active area (AA) of a planar MOSFET into a thin strip like **a fin, device dimensions can be dramatically reduced without feature size shrinkage**. This is shown in Fig. 15.1(b), which folds the AA with channel width Z from Fig. 15.1(a) into a fin, with 2h+w = Z. **Because the MuGFET shown in Fig. 15.1(b) has gate electrodes on three sides of the fin, it is called a triple-gate FET, or simply a trigate**. **The trigate device illustrated in Fig. 15.1(b)** could perform similarly to the planar MOSFET shown in Fig. 15.1(a). **By using a trigate, fabs can use the same lithographic technology to reduce transistor dimensions while maintaining the same performance, or to improve device performance without increasing device density**. With trigates, IC manufacturers can further improve device performance by making the fin taller; however, that will pose great challenges for etch processing development, polysilicon deposition, polysilicon dummy gate etch, SEG, dummy gate removal, trench cleaning, HKMG deposition, etc.
>
> Silicon fin etching has a nitride hard mask with a pad oxide underneath. By keeping this hard mask while forming the MuGFET, the gate electrode is only on two sides of the fin, not on the top or bottom. **Fabs usually call this double-gate FET a finFET**. For finFET devices, channel length only relates to the height of the fin (2h) and is no longer related to the fin CD (w), which is the smallest CD of the device. **From a processing point of view, a finFET is easier to build than a trigate. Intel's 22-nm IC chips are built with trigate devices**.

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 650-51.)

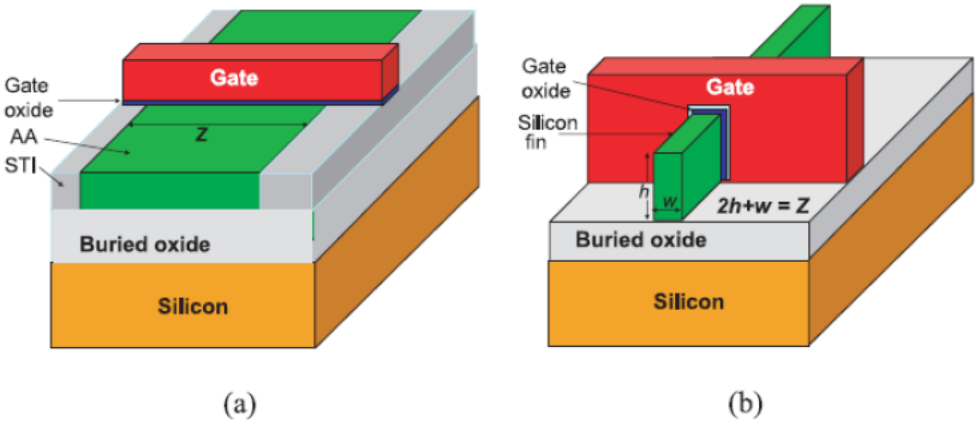


Figure 15.1 (a) A 3D illustration of a planar MOSFET with SOI substrate, and (b) an equivalent trigate FET with SOI substrate.

EX1020, Figure 15.1 (Planar MOSFET (left) vs. Tri-gate (right))

250. As shown above, tri-gate FETs were conventionally known to include fin structures.

251. Tri-gate structures with fins, which Pethe (assigned to Intel) recognizes that were "prevalent" and "conventional", were mature technology that were already included in "Intel's 22-nm IC chips" before the relevant time. (*Id.*)

252. Thus, based on their knowledge in the art, and the guidance and suggestions offered by Pethe, a POSITA would have had sufficient rationale to configure the Figure 5 embodiment Figure 5B structure with a fin structure disposed on top of substrate 302, consistent with known Fin-FET and tri-gate transistor semiconductor structure configurations at the time. A POSITA would have been motivated to implement such a modification, and would have reasonably expected such an implementation to be successful.

253. In my opinion, a POSITA would have understood that implementing the modification discussed above would have involved the application of known semiconductor device structure and process technologies that were well within the capabilities and knowledge of a POSITA at the time, consistent with the teachings of Pethe. In my opinion, a POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of the Pethe Figure 5 embodiment Figure 5B structure (as I discussed above for claim 1) including a fin structure like that recited in claim 6.

2. Claim 7

a) The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

254. In my opinion, Pethe discloses and/or suggests these limitations.

255. As shown in annotated Figure 5B below, Pethe's Figure 5B structure includes trench contacts 311A and 311C that are **disposed between each S/D region and each first contact** (discussed above for elements [1.f] (§ IX.A.1.f) and [1.g] (§ IX.A.1.g)).

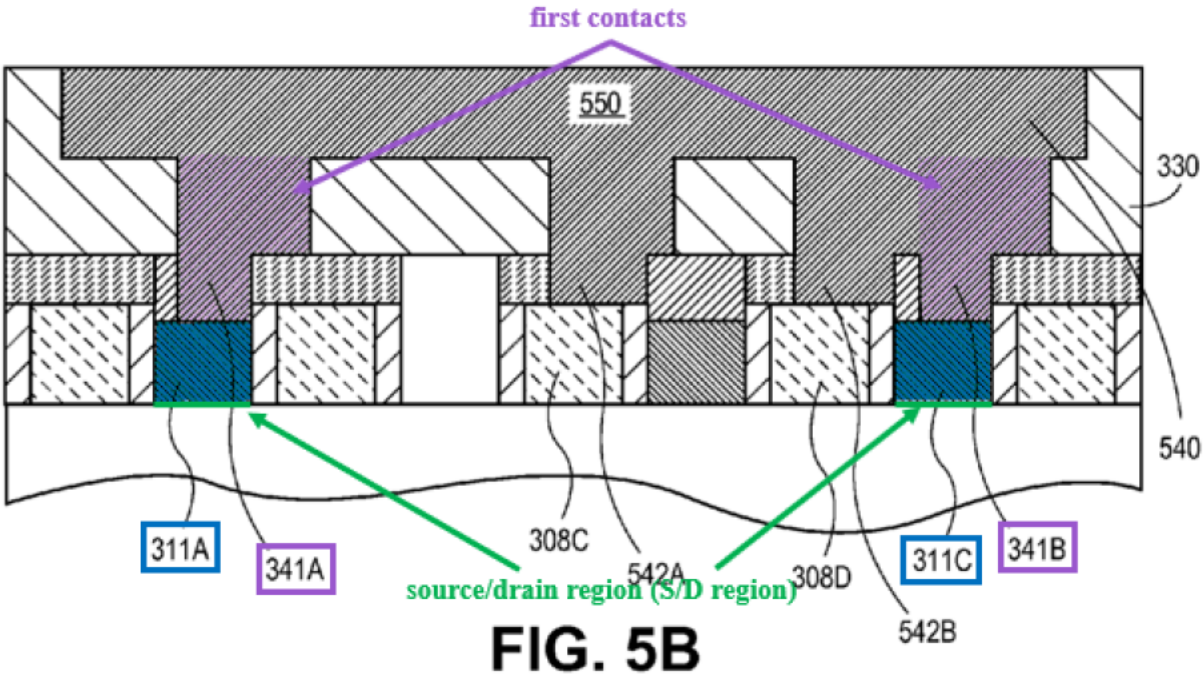


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 7:39-41, 8:24-28.)

256. Trench contact vias 341A, 341B (first contacts) are electrically conductive vias to trench contacts 311A, 311C, which are electrically conductive contacts to the source/drain regions. (EX1005 (Pethe), 11:23-31, 9:29-10:36 (describing Figure 3 embodiment, which are also teachings for the similar labeled features in the Figure 5 embodiment).) 341A, 341B are formed in the same process as metal (0) portion 550, which is electrically connected to the structure. (*Id.*) Thus, electrical connection to the source/drain regions relies on a conductive path through trench contact vias 341A, 341B, and trench contacts 311A, 311C, which are self-aligned contacts.

257. Pethe explains in connection with Figure 3's embodiment (which are also teachings for the corresponding features of similarly labeled features in Figure 5's embodiment) that these trench contacts are "self-aligned contacts" and recessed. (EX1005 (Pethe), 7:39-41, 8:24-28, 12:42-45, 12:56-59, 7:15-16 (disclosing Figure 3 embodiment's starting structure 300 is "provided following trench contact (TCN) formation" process; 12:32-33 (disclosing same regarding Figure 5's starting structure 500).)

258. In my opinion and experience, as I mentioned above, when a patent uses the same name and reference number in different Figures for an element (for example, trench contacts 311A/311C in Figure 3F and Figure 5B), the text disclosures describing the element for one Figure apply to the element on the other Figures, as they are the same element (unless otherwise noted). A POSITA would have had a similar understanding in connection with Pethe's Figure 5B structure, which refers to the same elements discussed for the Figure 3 embodiment.

259. A POSITA understood at the time that "salicide" generally refers to a self-aligned "silicide," which is a silicide formed in a particular region without the use of photolithography (implemented in trench contacts 311A-311C).

260. Notwithstanding Pethe's teachings, it is my opinion that a POSITA would have been motivated to implement in Pethe's Figure 5 embodiment structure

of Figure 5B a salicide layer disposed between each S/D region and each first contact.

261. For example, in connection with Figure 2's structure, Pethe teaches that "all of [trench] contacts 210A and 210B" may be composed of "a silicide material," and incorporated Golonzka teaches the same of its trench contacts. (EX1005 (Pethe), 6:53-59, 4:33-36, 11:26-31, 7:39-41; EX1006, [0051].) Pethe also directs a POSITA to Figure 2 and incorporates features from Figure 2's embodiment into Pethe's-Figure-5-Embodiment and Pethe's-Figure-3-Embodiment. (EX1005 (Pethe), 12:39-41; 7:22-25.)

262. Incorporated Golonzka further teaches that its trench contacts may be "a silicide material." (EX1006, [0051].) Pethe also recognizes that silicides may be formed as a layer (i.e., "the gate electrode is composed of a metal **layer** such as... metal **silicides**." (EX1005 (Pethe), 6:37-44, 7:22-25, 12:39-41.)

263. Thus, being directed to and otherwise having reasons to look to Figure 2's embodiment, a POSITA would have been motivated to configure trench contacts 311A-311C (above source/drain region) in Pethe's-Figure-5-Embodiment to include a salicide layer. (EX1005 (Pethe), 7:39-41.) A POSITA would have appreciated that such configuration would have reduced electrical resistance. (EX1009, 13:8-10; EX1013, 4:63-67, 3:56-58; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 585 (salicide helps reduce contact resistance).)

264. Thus, a POSITA would have been motivated to configure the Pethe Figure 5B structure (see §§IX.A.1, IX.A.7) with a salicide layer disposed in trench contacts between each source/drain region and trench contact vias 341, when implementing Pethe's Figure 5B structure. (*Id*.) A POSITA would have had a reasonable expectation of success in implementing such a modification given the direction by Pethe to Figure 2's structure, which itself discloses such structure, and especially given it would have involved application of known semiconductor device structure materials/processes, which would have predictably led to Pethe's-Figure-5-Embodiment's Figure 5B structure including a salicide layer disposed between each S/D region and each first contact, as claimed.

265. In my opinion, a POSITA would have had reason to look to the teachings in the Figure 2 embodiment and in turn been motivated to configure the trench contacts 311A-311C to include a salicide layer. (EX1005 (Pethe), 7:39-41.) Also, a POSITA was aware of known advantages to implementing a salicide layer similar to that described by Pethe, including to create a lower resistance contact. (EX1009, 13:8-10 ("The silicide layer 802 reduces the electrical resistance between the later formed trench contact 200 and the diffusion region 106."); EX1013, 4:63-67 ("Often, a layer of silicide material 212 is formed over the source and drain regions 206 and optionally, the gate electrode 208 **to enhance the contact**."), 3:56-58 ("silicide layers or regions are also formed to **enhance or establish conductive**

surfaces to the device".); EX1020 (*Introduction to Semiconductor Manufacturing Technology*), p. 585 (explaining how salicide helps reduce contact resistance).

266. Thus, a POSITA considering the semiconductor structure taught by Pethe (including Pethe's-Figure-5-embodiment) would have been motivated to consider teachings in Pethe (for example, Figure 2 structure) and the knowledge of such technologies in the art for options in ways to improve the Figure 5B embodiment semiconductor device structure to create a contact with reduced resistance.

267. Given such teachings and knowledge, it is my opinion that a POSITA would have appreciated that use of a salicide layer in the Figure 5 embodiment would have created a lower resistance source/drain contact, including by providing a more conductive interface. (EX1013, 4:63-67, 3:56-58.) A POSITA considering the semiconductor structure taught by Pethe would have been motivated to look to teachings in the art for options in ways to improve the semiconductor device structure to create a more conductive (less resistive) contact.

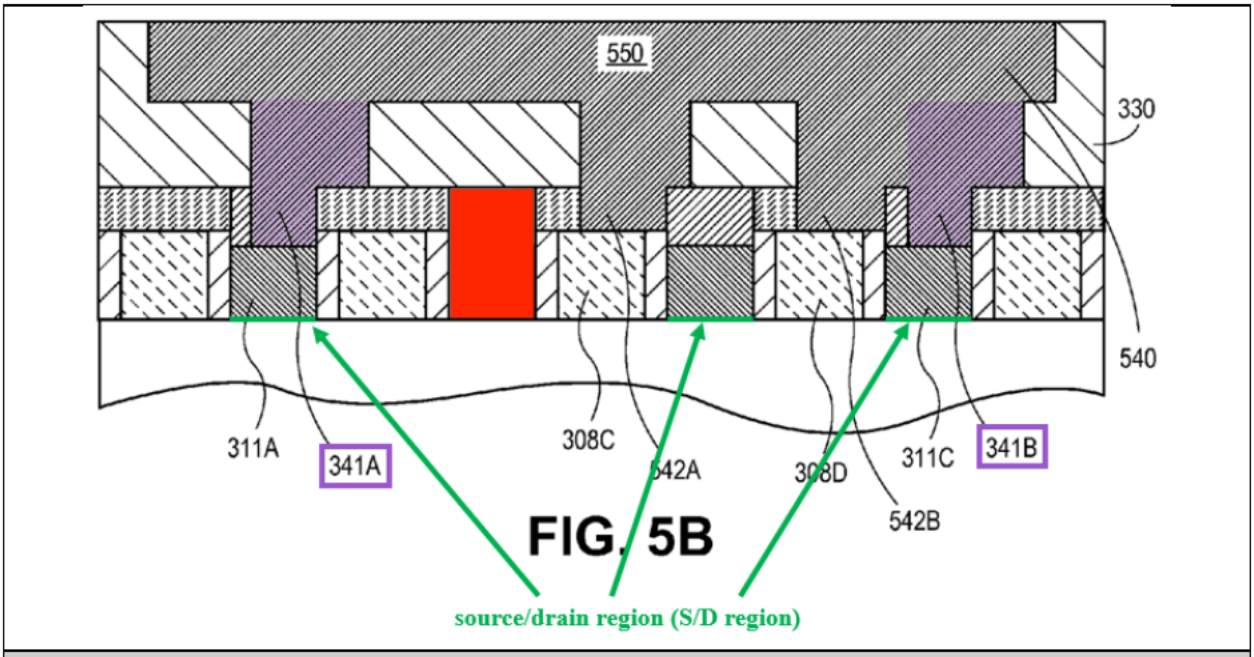
268. A POSITA would have found such a modification a predictable application of known semiconductor device structure materials and processes, which would have predictably led to the Figure 5 embodiment Figure 5B structure including **a salicide layer disposed between** each **S/D region** **and each** **first contact**, as claimed in claim 7.

C. Ground 3: Pethe in View of Bohr Discloses and/or Suggests Claim 7

1. Claim 7: The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

269. In my opinion, Pethe in view of Bohr discloses and/or suggests these limitations.

270. As explained for Ground 1, claim 1, Pethe's Figure 5B structure includes trench contact vias 341A and 341B (**first contacts**) and source/drain regions, as shown in annotated Figure 5B below:



Pethe, Figure 5B

(EX1005 (Pethe), 11:23-31, 10:29-36; §§ IX.A.1.f (S/D region), IX.A.1.g (first contacts).)

271. A POSITA would have understood that trench contact vias 341A and 341B are electrically conductive vias to trench contacts 311A and 311C, which are electrically conductive contacts to the source/drain regions. (EX1005 (Pethe), 12:54-67, 13:1-12, 11:23-31, 10:29-36, 9:29-10:36.) The trench contact vias 341A and 341B is also formed in the same process as the metal (0) portion 550, which a POSITA would have understood is electrically connected to the source/drain regions. Thus, electrical connection to the source/drain regions—which a POSITA would have understood would have been crucial to operation of the semiconductor structure of Figure 5B—relies on a conductive path through the trench contact vias 341A and 341B, and trench contacts 311A and 311C.

272. As I explained for Ground 2, for claim 7 (§IX.B.2.), Pethe's-Figure-5-Embodiment's self-aligned trench contacts are present in Figure 5B's 500 structure, which incorporated Golonzka teaches how to form and that such contacts may be "a silicide material." Pethe also teaches that silicides may be implemented as a **layer** (*see* EX1005 (Pethe), 6:37-44), and further teaches that trench contacts 210A and 210B may "a silicide material" (*see* EX1005 (Pethe), 6:53-59.)

273. A POSITA would have been motivated to implement **a salicide layer disposed between each S/D region and each first contact** in the Figure 5B structure in view of Bohr's teachings.

274. Consistent with a POSITA's understanding, it was known to include a salicide layer above a source/drain and/or below a contact, such as a trench contact (which is itself below the first contact) at the time of the alleged invention. State of art references confirm such an understanding. For example, before the date of the alleged invention, conventional self-aligned silicide (salicide) processes used deposition of silicide material and annealing to form alloys over source drain regions. For example, "[f]ormation of cobalt silicide (CoSi2) in a self-aligned silicide (salicide) process is one of the most common" for the technology nodes from 0.25 μm to 90 nm, while nickel silicide (NiSi) became common after the 65-nm node. (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 157-58.) A well-known self-aligned cobalt silicide is shown below.

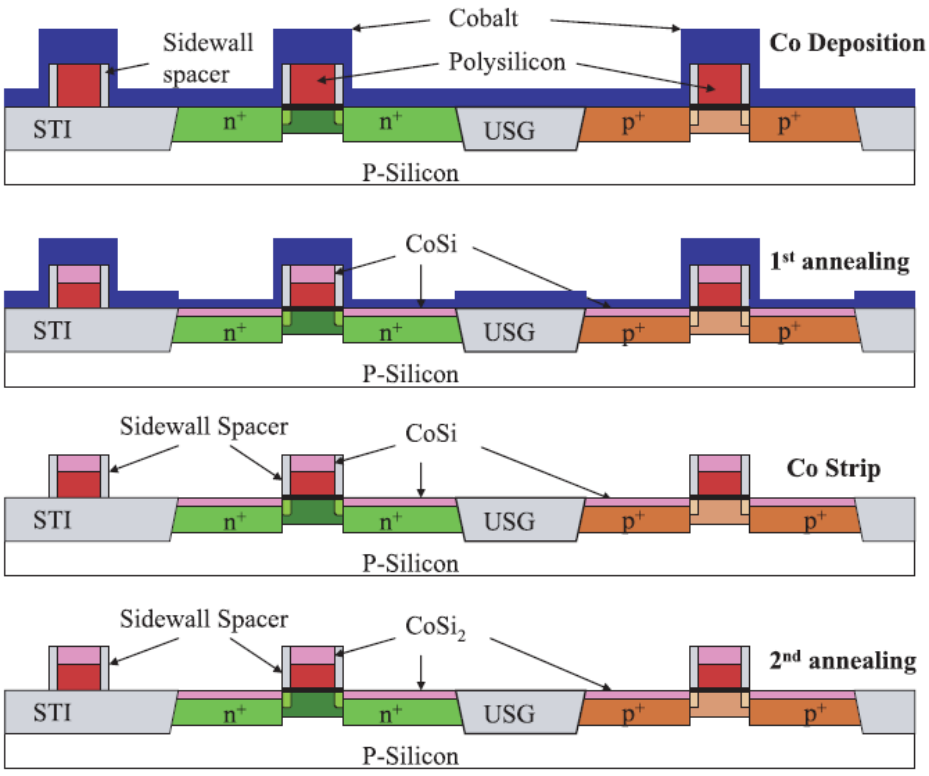


Figure 5.39 Self-aligned cobalt silicide process.

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 157-58.)

275. As another example, state of art teachings from Kuhn (EX1013), which has a common assignee (Intel) and overlapping inventorship with Pethe, confirms it was known to form a semiconductor structure that "[o]ften" includes: "a layer of silicide material 212 is formed over the source and drain regions 206" and contacts 220 "on top of the silicide layer 212." (*See* EX1013, 4:63-5:30.) (*See also id.*, FIG. 2 (depicting layer of silicide material 212 on top of source and drain regions 206 and below.)

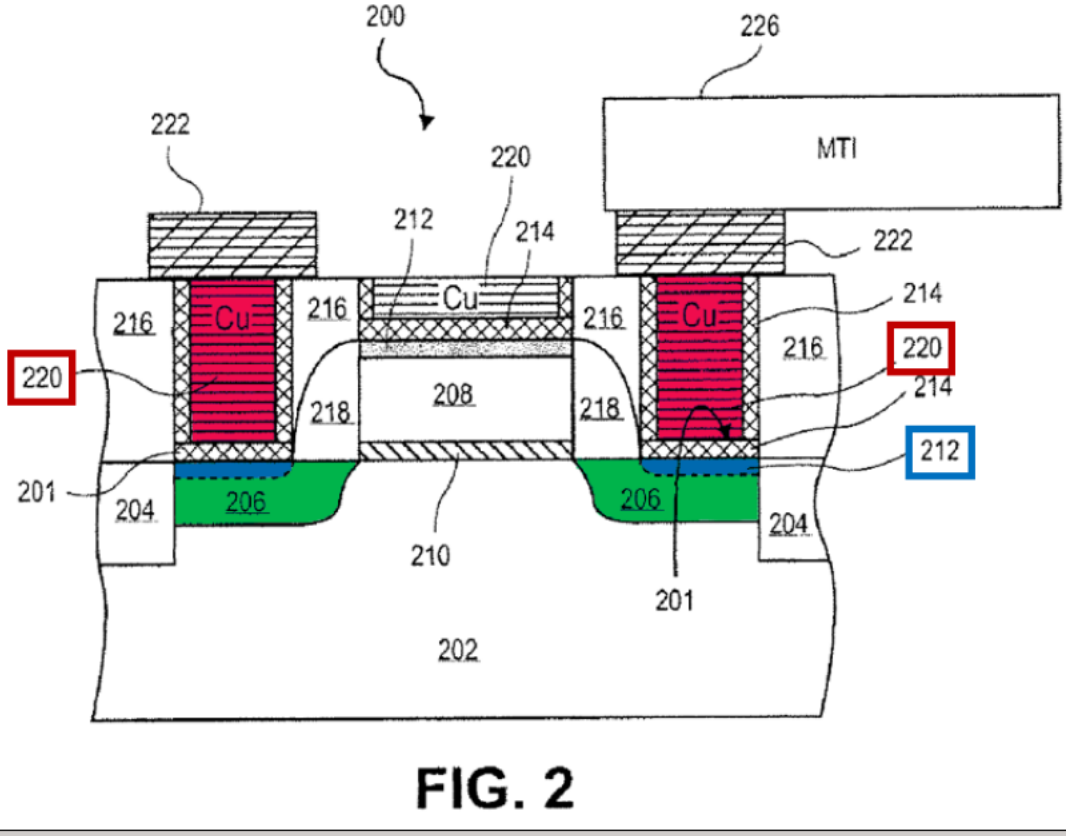


FIG. 2

Kuhn, Figure 2

(*See* EX1013, 4:63-5:30.)

276. A POSITA was also aware of known advantages to implementing a salicide layer between a source/drain and a contact, including to create a more conductive contact (for example, to "reduce[] the electrical resistance between the later formed trench contact… and the diffusion region…"). (EX1009, 13:8-10; EX1013, 4:63-67 ("Often, a layer of silicide material 212 is formed over the source and drain regions 206 and optionally, the gate electrode 208 **to enhance the contact**."), 3:56-58 ("silicide layers or regions are also formed to **enhance or establish conductive surfaces** to the device").)

277. Accordingly, in my opinion, a POSITA considering semiconductor structure taught by Pethe would have been motivated to look to teachings in the art for options in ways to improve the semiconductor device structure to create a more conductive contact.

278. Bohr is an example of such relevant teachings that a POSITA would have considered. Bohr has a common assignee (Intel) and multiple overlapping inventors with Pethe.

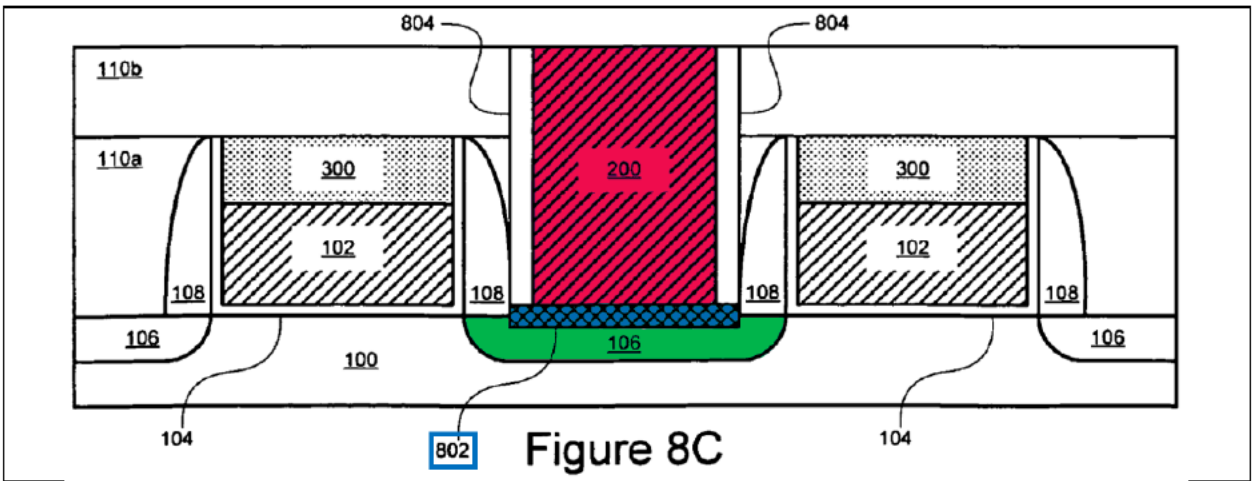
279. Like Pethe, Bohr discloses features related to the formation and configuration of semiconductor structures, including FETs. EX1005 (Pethe), 12:32-13:12, 13:63-14:11, id., 9:29-10:36, 11:23-31; EX1009, 1:5-36, 4:5-11, 12:61-14:3; EX1001, 1:9-13, 5:66-6:37. Thus, a POSITA would have considered Bohr's teachings when implementing the Figure 5B structure discussed in Pethe.

280. A POSITA would have been motivated to combine teachings of Pethe (for example, use of trench contacts and source/drain regions,) and Bohr (for example, use of a self-aligned silicide (i.e., salicide layer) disposed between a source/drain region and trench contact) to improve Pethe's structure by, for example, reducing the electrical resistance between the S/D region and trench contact.

281. Bohr describes systems/methods of reducing likelihood of contact-to-gate shorts during fabrication of MOS (for example, MOSFET) transistors. EX1009, 2:16-18, Abstract, 1:5-2:37. In particular, Bohr teaches self-aligned contacts for a

field-effect transistor (FET) utilizing a salicide layer between a source/drain and contact. An example of this contact is shown below and comprises silicide layer 802 formed between trench contact 200 and source/drain diffusion region 106.

282. Consistent with the POSITA's knowledge discussed above, Bohr (EX1009) teaches the use of a salicide layer between a source/drain and a contact. (EX1009, 12:61-13:10, FIGs. 8A-8C.) In particular, Bohr teaches diffusion region 106, upon which a silicide layer 802 is formed beneath trench contact 200, as shown in annotated Figure 8C below.



Bohr, Figure 8C

(EX1009, 12:61-13:10, FIG. 8C.)

283. In Bohr, before the trench contact 200 is formed, silicide layer 802 is formed at the bottom of the contact trench opening 800 (which is later filled in to become trench contact 200.) (EX1009, 12:61-66, 8A.)

284. As discussed above, a conventional salicide processes involved metal deposition/annealing over source/drain regions (see EX1020 (*Introduction to*

Semiconductor Manufacturing Technology), 157-58, FIG. 5.39 (above)), and Bohr teaches forming the silicide layer in the same manner (EX1009, 12:61-13:10 ("deposition process…annealing process…")) and use of a salicide layer between a source/drain and contact (id., FIGs. 8A-8B). See also EX1001, 4:22-33.

285. A POSITA would have understood that Bohr's silicide is a self-aligned silicide, and thus a salicide. (EX1009, 12:61-13:8.) Bohr expressly teaches this because it explains that the silicide layer is formed without using a photolithography step, and is instead formed by "a conventional metal deposition process" and "anneal[ed] … to cause the metal to react" with the silicon "diffusion region **…** and form a silicide layer" with "[a]ny unreacted metal may be selectively removed using known processes." (EX1009, 12:61-13:8.) Accordingly, and as taught in Figure 8C, the salicide layer is disposed between source drain region and trench contact.

286. Thus, a POSITA would have had reasons to consider Bohr in context of Pethe given they each disclose features relating to semiconductor devices/structures and/or parts thereof. For example, Pethe, Bohr describes semiconductor structures with trench contacts to source/drain regions. (*See for example*, EX1005 (Pethe), 11:23-31, 10:29-36, 9:29-10:36; EX1009, 12:61-14:3; EX1001, 1:9-13, 5:66-6:37.) Thus, a POSITA would have had reasons to consult Bohr when looking to implement a semiconductor structure like in Pethe's-Figure-5-Embodiment's Figure 5B structure, and in doing so, would have been motivated

to modify Pethe's structure to achieve a salicide layer disposed between its source/drain region and trench contact consistent with Bohr's teachings. (EX1005 (Pethe), 12:32-13:12; *see also id*., 9:29-10:36, 11:23-31 (Figure 3 embodiment teaching which are also teachings for the corresponding/overlapping features of the Figure 5 embodiment); EX1009, 12:61-14:3, FIG. 8C; EX1001, 1:9-13, 5:66-6:37.)

287. Such a rationale and resulting modification would have been applicable to both Pethe's-Figure-5-Embodiment's structure discussed for claim 1 in §IX.A.1 and to the modified Pethe's-Figure-5-Embodiment's structure that I discussed for claim 1 in connection with §IX.A.7.

288. A POSITA would have been motivated to combine the teachings of Pethe with those of Bohr to achieve a salicide layer disposed between its source drain region and trench contact in Pethe's Figure 5B structure. (EX1009, 12:61-14:3, FIG. 8C.)

289. A POSITA would have been motivated to implement such a salicide layer disposed between a source/drain region and trench contact in Pethe's structure. Also, a POSITA would have reasonably expected such an implementation to be successful. In my opinion, a POSITA would have understood that implementing the modification discussed above would have involved the application of known semiconductor device structure and process technologies that were well within the capabilities and knowledge of a POSITA at the time, consistent with the teachings

of Pethe. For example, a POSITA would have appreciated that the implementation of a salicide layer disposed between a source/drain region and trench contact was known in the art well before the alleged invention of the '747 patent, as Bohr expressly acknowledges (*see for example*, Ex.1009, 12:61-13:10) and as demonstrated by the state of art teachings that I discussed above (*see above* regarding Exhibits EX1009, EX1013, EX1020 (*Introduction to Semiconductor Manufacturing Technology*)). A POSITA would have appreciated the possibility of a salicide layer residing above Pethe's source drain region and underneath its trench contact 311A and 311C, as disclosed by Bohr. Pethe contemplates a number of implementations of salicide layers. *See* Ground 2, claim 7 (§IX.B.2.).

290. As I explained above, a POSITA would have had a reasonable expectation of success of implementing such features, and would have appreciated that the implementation of a salicide layer disposed between a source/drain region and trench contact in semiconductor structures was known at the time, as were conventional methods to produce such implementations, as demonstrated by Bohr. (*See above* Ex.1009, 12:61-13:10; EX1013, 4:63-5:30, 5:48-64, 9:5-30, 10:7-35; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 157-58.)

291. For example, in my opinion, a POSITA would have leveraged their state of art knowledge in context of the teachings of Pethe and Bohr to understand that such a structure would have been produced by "a conventional metal deposition

process" followed by an "annealing process... to cause the metal to react with the diffusion region 106 and form a silicide layer 802," with "[a]ny unreacted metal … selectively removed using known processes" and finally a metal deposition process to produce a trench contact. (EX1009, 12:61-13:10; EX1013, 5:48-64.) Therefore, in my opinion, a POSITA would have been able to readily apply the conventional methods of salicide layers disposed between source/drain regions and trench contacts, such as those taught by Bohr, to Pethe with high predictability.

292. Thus, a POSITA would have been able to readily apply such conventional features (for example, salicide layers between source/drain regions and trench contacts) to Pethe's structure with high predictability, and considered different silicide layer materials/thicknesses, deposition/annealing processes, and parameters to facilitate such a modification, resulting in the source/drain region and trench contact 311A-C structures in Pethe's FIG. 5B structure having a salicide layer disposed between.

293. Bohr teaches advantages to implementing a salicide layer between a source/drain and contact (for example, to "reduce[] the electrical resistance between the later formed trench contact…and the diffusion region…"), which is consistent with a POSITA's knowledge and understanding. EX1009, 13:8-10; EX1013, 4:63-67, 3:56-58. Thus, a POSITA would have looked to achieve similar benefits by

using a salicide layer between Pethe's S/D region and trench contacts in Pethe's Figure 5B structure.

294. A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Pethe-Bohr combination. As explained, Bohr teaches the known advantages of using a salicide layer between a diffusion region and trench contact in a semiconductor structure similar to those contemplated by Pethe (for example, FET structures). Ex.1009, 1:5-36, 4:5-11, 12:61-13:10; EX1005 (Pethe), 12:32-13:12, 13:63-14:11.

295. The combination of Pethe and Bohr would have involved application of known technologies (for example, known use of salicide layers between source/drain regions and trench contacts) (*see for example*, EX1013, 4:63-5:30, 5:48-64, 9:5-30, 10:7-35; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 157-58) according to known methods (for example, known deposition/annealing processes) to yield the predictable result of a semiconductor structure (Pethe's Figure 5B) including a salicide layer formed over the source/drain region and between trench contacts 311A/311C (and thus trench contact vias 341A/341B (**first contacts**)) so the resistance between the source/drain region and (trench contacts 311A/311C (and thus "**first contacts**" 341A/341B) can be reduced.

296. Therefore, in light of such teachings, guidance, and knowledge at the time, a POSITA would have been motivated to modify the Pethe Figure-5-

Embodiment's structure such that a salicide layer was disposed between source/drain region and trench contact 311A-C structures. A POSITA would have considered different materials and thicknesses for the salicide layer and different deposition and annealing processes and parameters to facilitate such a modification in a successful manner while keeping with the objectives and desired goals of Pethe.

297. A POSITA would have appreciated that such a modification would have involved applying known technologies/techniques (for example, use of salicide layer as taught/suggested by Bohr) to a known device/structure (Pethe's source drain regions and trench contacts). Accordingly, such a skilled person at the time would have had the motivation and reasonable expectation of success in implementing such a modification to Pethe. Considering and implementing such knowledge, techniques, and teachings would have resulted in providing a salicide layer disposed between Pethe's source drain region and trench contacts 311A-C to achieve improved operation of Pethe's source drain region and trench contacts 311A-C when integrated into the semiconductor device (improved contact to the source drain by), in a manner consistent with that taught by Pethe and Bohr, and as also known in the art by a POSITA at the time. (EX1005 (Pethe), 11:23-31, 10:29-36, 9:29-10:36; EX1009, 12:61-14:3.)

D. Ground 4: Pethe in View of Huang Discloses and/or Suggests Claims 8-9

1. Claims 8-9

8. The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

9. The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.

298. In my opinion, Pethe in view of Huang discloses and/or suggests these limitations.

299. Ground 2's (and as incorporated, Ground 1's) analysis (incorporated by reference herein) explains how Pethe's-Figure-5-Embodiment discloses/suggests claims 1-8. (§IX.B.)

300. As explained for Ground 1, claims 1 and 8, Pethe teaches the metal (0) portion 550 includes **a plurality of third contacts** and is **disposed on** trench contact vias 341A and 341B (**parts of the first contacts**) and on gate contact vias 542A and 542B (**parts of the second contacts**).

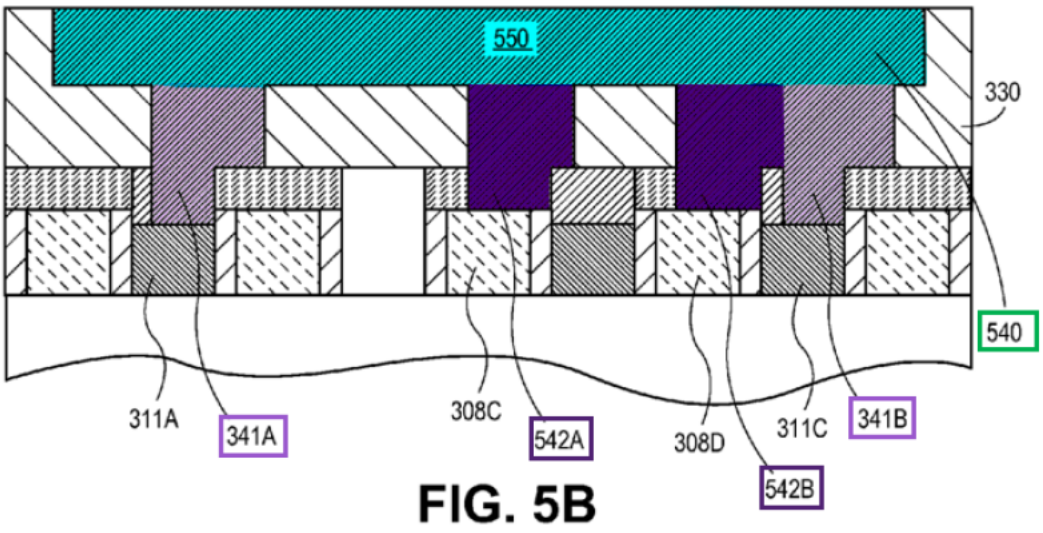


FIG. 5B

Pethe, Figure 5B

(EX1005 (Pethe), 12:54-13:12, 11:23-31.)

301. In addition to Pethe's-Figure-5-Embodiment Figure 5B structure discussed above for claim 3 in §§IX.A.1, IX.A.3 or as modified as discussed above for claim 3 in §IX.A.7 disclosing a plurality of third contacts as claimed, a POSITA would have been motivated to implement such features in view of Huang.

302. It was well-known and conventional to form metal (1) ("M1") metal lines and metal (0) vias (above the metal (0) lines and device contacts) using a dual-damascene process. By the time of the alleged invention, the dual-damascene process was an established technique in semiconductor manufacturing, particularly in the back-end-of-line (BEOL) processing, which is the "formation of the M1 wiring layer to formation of a pad opening to a final passivation... in a wafer level package process." (EX1016, ¶89.)

303. A number of state of art references confirm such an understanding and provide teachings consistent with a POSITA knowledge of the art at the time of the '747 patent.

304. For example, using a dual-damascene process to provide M1 metal lines and metal (0) vias was conventional and ubiquitous, as discussed in *Introduction to Semiconductor Manufacturing Technology* (EX1020, pp. 345-49):

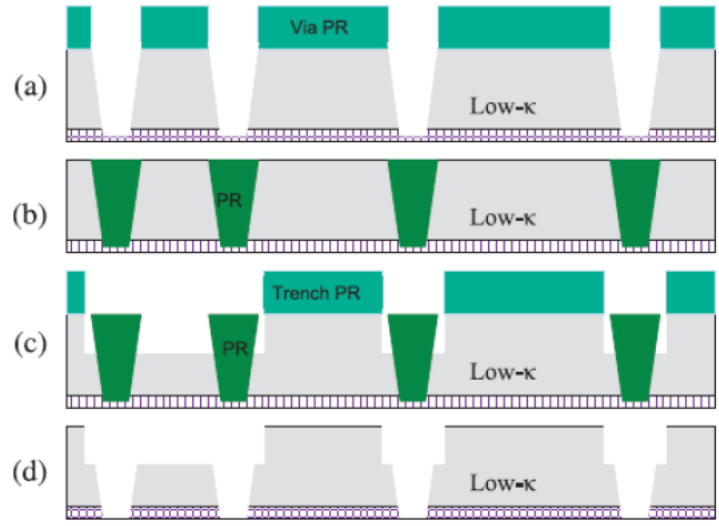


Figure 9.35 A via-first dual damascene process: (a) via etch, (b) photoresist fill and etchback, (c) trench etch, and (d) ESL breakthrough.

EX1020, p. 346 (a via-first dual damascene process)

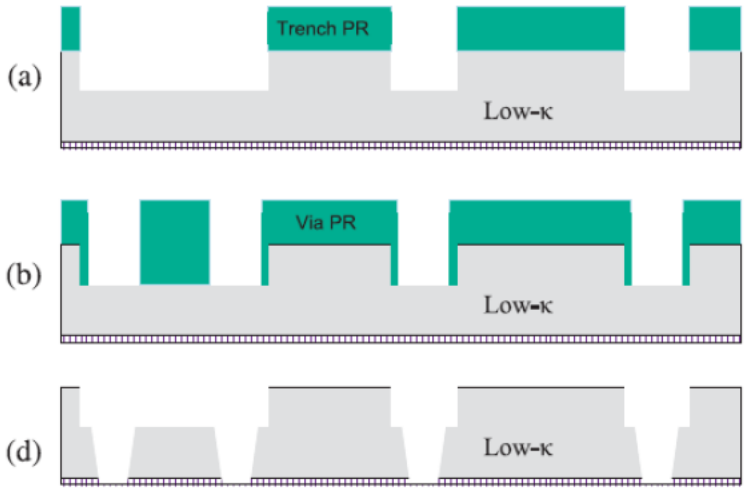


Figure 9.36 A trench-first dual damascene process: (a) trench etch, (b) via mask lithography, (c) via etch, and (d) ESL breakthrough.

EX1020, p. 346 (a trench-first dual damascene process)

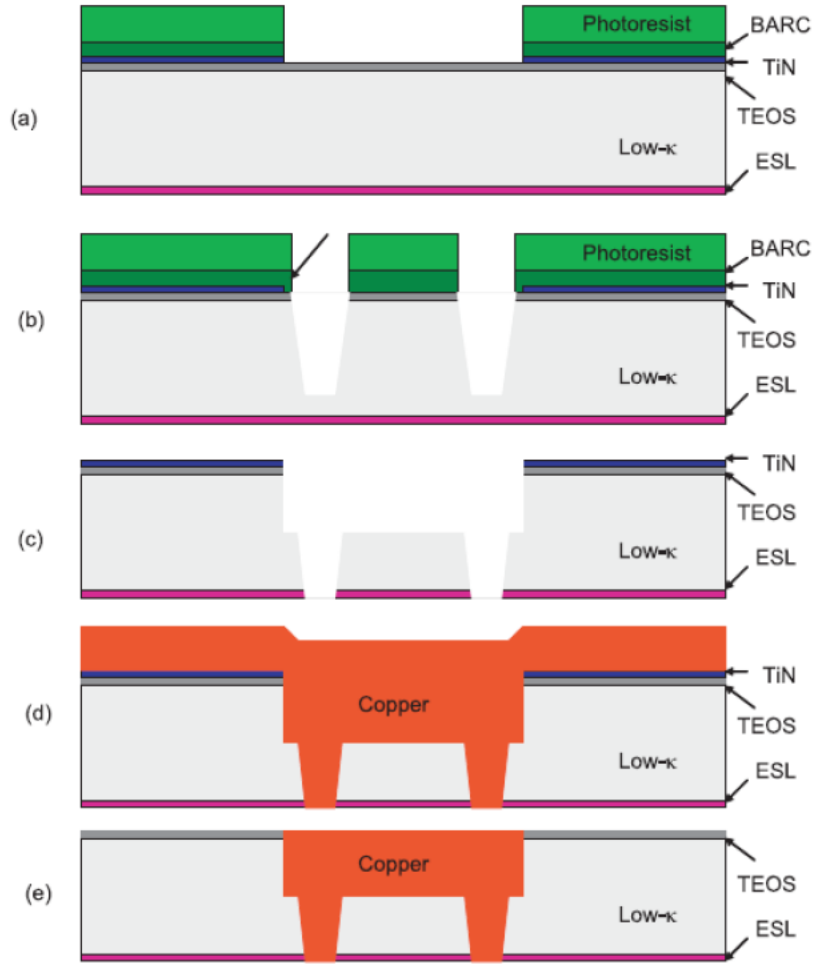


Figure 9.37 Copper metallization with a metal hard mask: (a) etch bottom antireflective coating (BARC) and metal hard mask with trench mask, (b) via etch halfway with a via mask, (c) trench and via etch with metal hard mask and ESL breakthrough, (d) copper deposition, and (e) metal CMP to remove the metal hard mask.

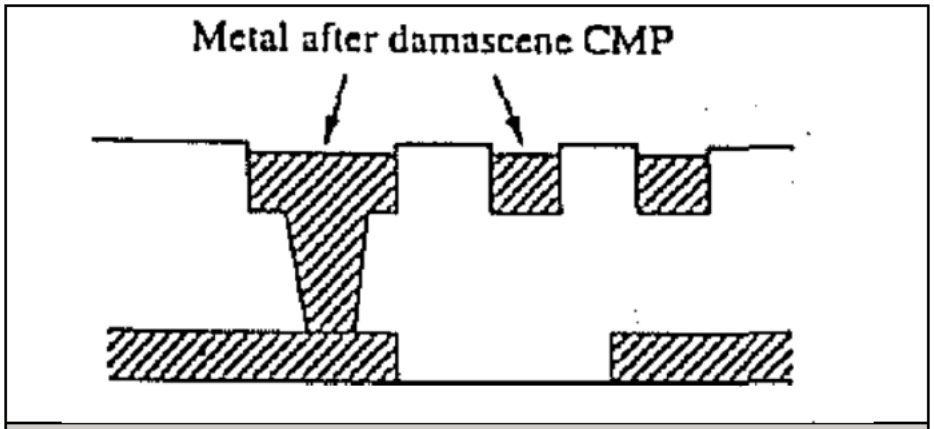
EX1020, p. 346 (a via-first dual damascene process)

"In the **back-end of the line (BEoL) process**, all photolithography processes are followed by etch processes. **In copper metallization, this dual damascene process is repeated multiple times, depending on how many metal layers there are**: dielectric CVD, photolithography, dielectric etch, photoresist strip and clean, photolithography, dielectric etch, photoresist strip and clean, deposition of metal layers, metal anneal, and CMP. After all of the metal layers are formed, CVD silicon oxide and silicon nitride are deposited as the passivation layer, and the last photolithography process defines the

> pads for wire bonding or bump formation. After that, the chips are tested, die sawed, sorted, packaged, burned-in, and shipped to customers."

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), p. 19):

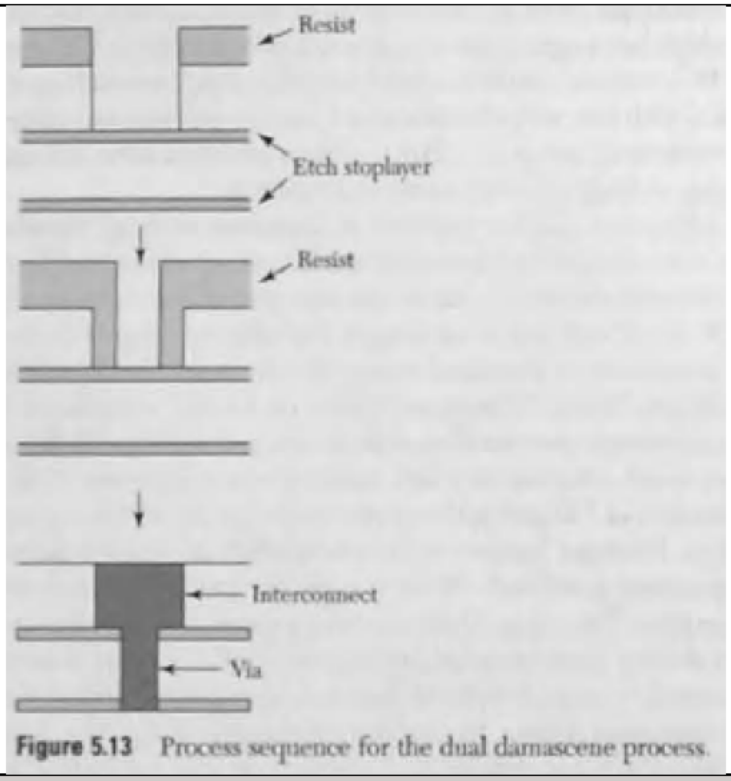
305. As another example, state of art teachings from *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology* ("Wolf")(EX1014), explain that in a dual-damascene process, "only a single metal deposition step is used to simultaneously form the main metal lines and the metal in the vias," after which "CMP is used to remove excess metal." (EX1014, pp. 696-98.) This "sequence is repeated for the next level of metal" (i.e., M2, M3... M8).



Wolf, Figure 15-3

306. As another example, *Fundamentals of Semiconductor Fabrication* ("May")(EX1015) explains that "[d]amascene processing involves the creation of interconnect lines by first etching a trench or canal in a planar dielectric layer and then filling that trench metal," and [i]n dual damascene processing (Figure 5.13). a

second level is involved where a series of holes (i.e., contacts or vias) are etched and filled in addition to the trench."



Wolf, Figure 15-3

(EX1015, pp. 55-56.)

307. As further examples, using a dual-damascene process to provide M1 metal lines and metal (0) vias is referred to in *Introduction to Semiconductor Manufacturing Technology* (EX1020, pp. 345-49) at the time of the alleged invention to be "mainstream" (pp. 345-49), well developed "[i]n the late 1990s" (p. 453), having "maturity" (p. 464), "dual damascene has **become the process of choice** for copper metallization in IC chip manufacturing" (pp. 517-18), "Copper interconnections have become a **mainstream technology in CMOS logic IC** since

the development of the 130-nm technology node. Copper CMP processes have been **widely used in** dual damascene processes to form copper interconnections in **advanced IC fabs**" (p. 543), "The dual damascene process, which combines via and trench etching before metal deposition, is **the most commonly used method for copper metallization**" (pp. 574-79).

308. A POSITA was also aware of known advantages to implementing a dual-damascene process to provide M1 metal lines and M0 vias, including:

- **simplified fabrication**: "The dual damascene process can eliminate some metal deposition and CMP processes, unlike two single damascene processes." (EX1020, pp. 574-79); "The dual-damascene process offers the advantage of reducing the number of process steps" (EX1014, pp. 695); "The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes" (EX1014, pp. 698).
- **no requirement for metal etching**: "the dual damascene process does not need to etch metal" (EX1020, pp. 345-49, 497-98), "[t]he fact that the dual damascene process does not require a metal etch step paved the way for copper metallization of IC interconnections in the late 1990s" (EX1020, p. 464), "[b]ecause copper is very difficult to dry etch, dual damascene has become the process of choice for copper metallization in IC chip

manufacturing" (EX1020, pp. 517-18), "The advantage of damascene processing is that it eliminates the need for metal etch" (EX1015, pp. 56).

- **reduced risk of electromigration failure**: "One special benefit of the dual damascene technique is that the via plug is now of the same material as the metal line and the risk of via electromigration failure is reduced." (EX1015, pp. 92.)

309. As these state of the art sources further explain:

310. *Introduction to Semiconductor Manufacturing Technology* (EX1020, pp. 345-49) explains:

> "The most significant difference between the dual damascene Cu process and the Al–Cu process (Fig. 10.70) is that the **dual damascene process does not need to etch metal**. Because copper is very difficult to dry etch, **dual damascene has become the process of choice for copper metallization**. In advanced CMOS ICs, copper interconnects have already replaced Al–Cu interconnects and **become mainstream**. Even in memory chips, such as DRAM and NAND flash, copper interconnects are being applied in high-speed products. For Cu interconnects, ILD and passivation dielectric thin-film depositions have become relatively simple, with no more gaps to fill and no more planarization issues. Requirements for those thin-film depositions are high deposition rate, good uniformity, stable low-k value, and capability of process integration. Of course, for STI and ILD0, there are still the great challenges of filling even narrower gaps and planarizing dielectric layer surfaces."

(EX1020, pp. 345-49.)

> "In the late 1990s, development of the CMP process paved the way for using copper in IC interconnection applications with damascene or dual damascene processes. Tantalum (Ta) or tantalum nitride

(TaN) is used as the barrier layer, and silicon nitride (SiN) or silicon carbon nitride (SiCN) has been used as barrier and cap layers to isolate the copper layer and prevent it from diffusing through the low-k dielectric layer into the silicon substrate, causing interference with the normal operations of the transistors. Silicon nitride is also used as an etch-stop layer for the dual damascene dielectric etching process. Figure 11.2 illustrates a CMOS chip cross section with a copper interconnection. Figure 11.3 illustrates the position of metallization in IC manufacturing processes. This chapter covers the metals used in IC chip manufacturing, their applications, and their deposition processes."

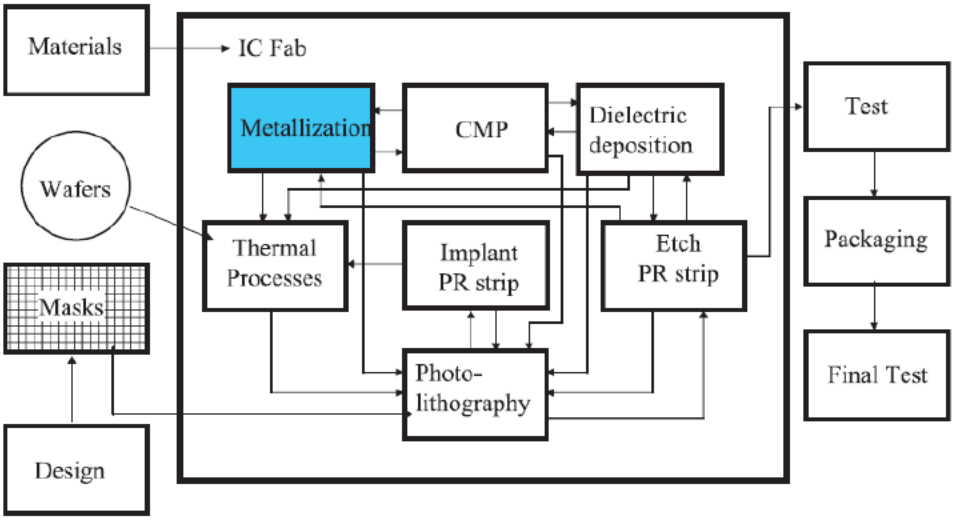


Figure 11.3 Metallization in an IC fabrication process flow.

EX1020, Figure 11-3

(EX1020, p. 453.)

"Technology developments, including high-aspect-ratio dielectric contact/via and trench etch processes, barrier layer deposition, copper deposition, and more importantly copper chemical mechanical polishing (CMP), led to the **maturity of dual damascene metallization technology**. The fact that the dual damascene process does not require a metal etch step paved the way for **copper metallization of IC interconnections in the late 1990s**.

> Copper deposition requires two steps: deposition of barrier and seed layers that cover the sidewall and bottom of the trenches and via holes, and bulk layer deposition by electrochemical plating (ECP) that **completely fills the via holes and trenches**. An annealing process follows bulk copper deposition to increase grain size and improve electrical conductivity before the metal CMP process, which removes copper and the barrier metal layer from the wafer surface, **leaving the copper inside the trenches and via holes to form metal interconnects**."

(EX1020, p. 464.)

> "**In the 1990s, development of the CMP process paved the way for copper interconnections by applying the dual damascene process**, which does not require a metal etching step. There are several other applications for the dual damascene copper interconnection process. A barrier layer of copper can be deposited into highaspect-ratio via holes to prevent copper diffusion. This barrier layer provides good sidewall and bottom step coverage, good adhesion to dielectrics, and low contact resistance. Other applications are the deposition of copper film with high-quality, low-resistivity, and void-free filling of high-aspect-ratio **trench and via holes**. Finally, there are defect-free copper polishing and post-CMP cleaning processes. **A copper interconnection processing sequence is illustrated in Fig. 11.38**."

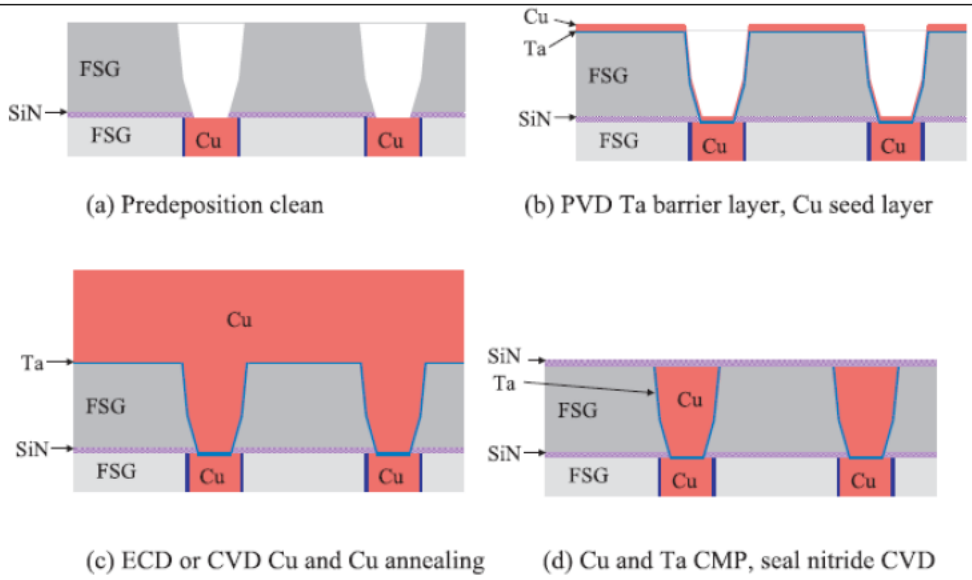


Figure 11.38 Dual damascene copper interconnection process.

EX1020, Figure 11-38 (Dual damascene copper interconnection process)

(EX1020, pp. 497-98.)

> "One of the most important applications of CMP processes are copper interconnections. Because copper is very difficult to dry etch, **dual damascene has become the process of choice for copper metallization in IC chip manufacturing**. The term damascene originates from the ancient Middle East in today's Damascus, capital of Syria. People there invented a process to decorate sword surfaces with gold inscriptions by using diamond to cut trenches into the steel sword surface, polishing gold into the trenches, washing away the gold on the surface, and leaving gold in the trenches. After this process, the sword was decorated with inscriptions on its surface. This technique has been used in the jewelry industry to place gold inscriptions on gemstone surfaces and is called a damascene process. In fact, the tungsten plug formation process is a damascene process.
>
> For copper applications, the dual damascene process is used. It uses two dielectric etch processes, **one for via etch and one for trench etch**. **After dielectric etches, metal layers (PVD Ta/PVD Cu/ECP Cu) are deposited into via holes and trenches. After metal annealing, a metal CMP process removes the copper and**

tantalum barrier layer from the wafer surface and leaves copper lines and plugs embedded inside the dielectric layer. Figure 12.15 illustrates the dual damascene copper metallization process."

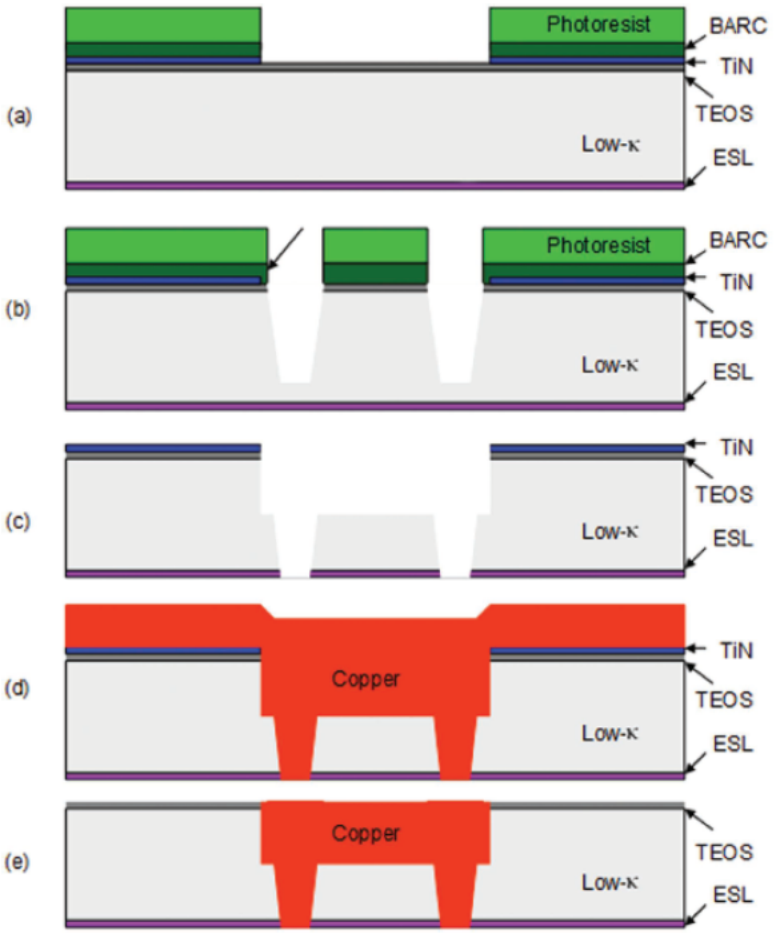


Figure 12.15 Copper metallization with a metal hard mask: (a) etch BARC and metal hard mask with trench mask, (b) etch via halfway with via mask, (c) etch trench and via with metal hard mask and ESL breakthrough, (d) metal deposition, and (e) metal CMP.

EX1020, Figure 12-15

(EX1020, pp. 517-18.)

"The CMP process is one of the fundamental processes in IC chip manufacturing, along with etch and CVD. Multilayer Al–Cu interconnections need oxide and tungsten CMP processes to planarize ILD layers and form tungsten plugs, respectively. Copper interconnections have become a mainstream technology in CMOS logic IC since the development of the 130-nm technology node.

> Copper CMP processes have been widely used in dual damascene processes to form copper interconnections in advanced IC fabs."

(EX1020, p. 543.)

> "In the 1990s, CMP technology developed and matured quickly. It is still widely used in bulk tungsten removal processes to form tungsten plugs. The copper interconnection process is very similar to a tungsten plug formation process. Instead of via holes, trenches are etched on the dielectric surface. Then copper is deposited into the trenches, and a subsequent copper CMP process removes the bulk copper layer on the wafer surface, leaving the copper lines embedded in the dielectric layers. **By using this damascene process, a metal etch process becomes unnecessary. The dual damascene process, which combines via and trench etching before metal deposition, is the most commonly used method for copper metallization. The dual damascene process can eliminate some metal deposition and CMP processes, unlike two single damascene processes**."

(EX1020, pp. 574-79.)

311. Many other references recognized these advantages. (EX1014, pp. 695 ("The dual-damascene process offers the advantage of reducing the number of process steps"), 698 ("The reduction in the number of processing steps is another of the benefits that have driven the development of dual-damascene processes."); EX1015, pp. 56 ("The advantage of damascene processing is that it eliminates the need for metal etch"), 92 ("One special benefit of the dual damascene technique is that the via plug is now of the same material as the metal line and the risk of via electromigration failure is reduced.").

312. Accordingly, a POSITA considering Pethe's semiconductor structure would have been motivated to look to teachings in the art for ways to provide a connection of the semiconductor structure to the M1 layer with simplified fabrication, no requirement for metal etching, and reduced risk of electromigration failure.

313. In doing so, a POSITA would have recognized Huang as an example of such relevant teachings. Consistent with the POSITA's knowledge discussed above, Huang (EX1008) teaches the use of a dual-damascene process to provide M1 metal lines and M0 vias. (EX1008, ¶17, FIG. 8A.) Huang teaches metal layer M1 metal lines 74 and M0 vias 72 for "for connecting to contact plugs 60 and 62," as shown in annotated Figure 8A below.

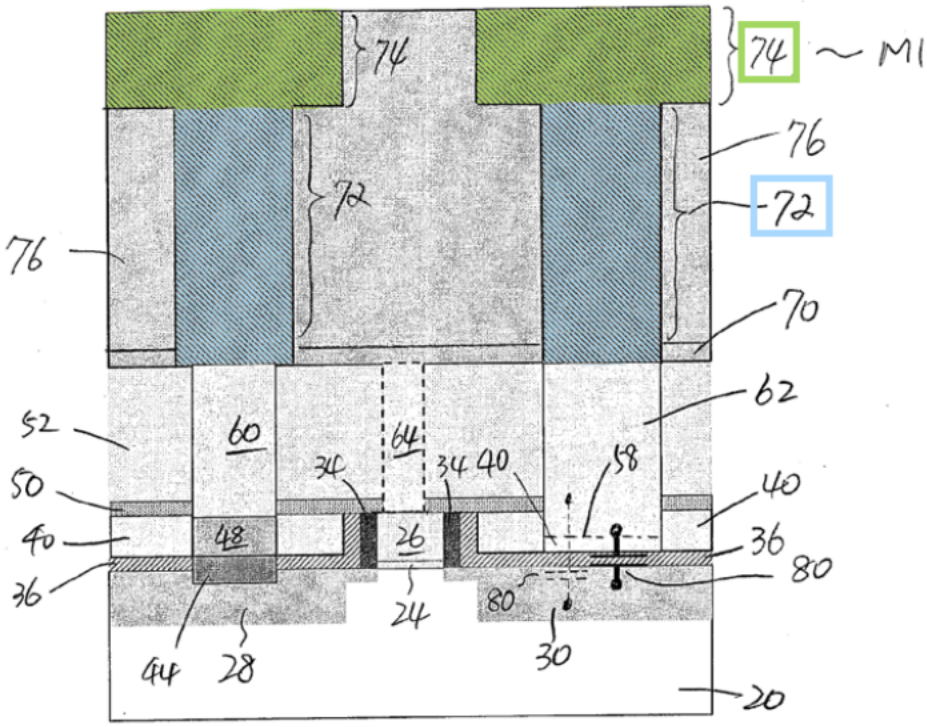


Fig. 8A

Huang, Figure 8A

(EX1008, ¶17, FIG. 8A.)

314. In Huang, "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces are formed between M0 vias 72 and the respective overlying metal lines 74. (EX1008, ¶17.)

315. Huang's aforementioned structure also corresponds to **a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly**. For example, Huang's M0 vias 72 structure corresponds to a "via hole structure" and metal lines 74 structure corresponds to the third contact's "trace structure."

316. Given that the "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces being formed between M0 vias 72 and respective overlying metal lines 74" (EX1008, ¶17), the via hole structure and the trace structure comprises the same material and contact each other directly.

317. Huang and Pethe each disclose features relating to semiconductor devices/structures and/or parts thereof. For example, Pethe and Huang describe semiconductor structures with metal layers to contacts (i.e., gate and source/drain contacts). (*See*, *e.g.*, EX1005 (Pethe), 8:24-51, 9:29-43, 11:23-42; EX1008, ¶17; EX1001, 5:31-6:37.) Thus, in my opinion, a POSITA would have had reasons to consult Huang when looking to implement a semiconductor structure like that discussed in Pethe.

318. In considering Huang in context of Pethe, a POSITA would have been motivated to consider the collective teachings of Pethe with those of Huang to achieve a dual-damascene process to provide M1 metal lines and M0 vias in Pethe's Figure 5B structure. (EX1008, ¶17, FIG. 8A.)

319. In my opinion, a POSITA would have been motivated to implement such a dual-damascene process in Pethe's structure and would have reasonably expected such an implementation to be successful in context of Pethe's disclosed structure. The implementation of a achieve a dual-damascene process to provide

M1 metal lines and M0 vias was known in the art by a POSITA before the alleged invention of the '747 patent, as I demonstrated by the above-mentioned state of art teachings (*see* my discussions above regarding Exhibits 1014, 1015, 1020). A POSITA would have readily appreciated the possibility of using a dual-damascene process to provide M1 metal lines and M0 vias, as disclosed by Huang. Pethe provides a metal (0) portion, but does not provide any BEOL interconnection, which a POSITA would have understood is critical to create an integrated circuit with ever-more capacity, as is the driving force of the semiconductor industry and of Pethe. (EX1005 (Pethe), 1:14-26.)

320. As I explained above, a POSITA would have appreciated that the implementation of a dual-damascene process to provide M1 metal lines and M0 vias was at the time, a conventional method to produce such implementations. (*See above and for example*, (EX1014, pp. 696-98; EX1015, pp. 55-56; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79.) A POSITA would have understood that the combined teachings of Pethe and Huang would merely amount to determining a suitable dual-damascene process to modify the Figure 5B structure as I explained above.

321. Whether a POSITA considers Pethe's "metal (0)" layer and vias to be what is known in the art as an M1 layer would not change my analysis or opinions. A POSITA would have understood and appreciated that there was no universal

convention as to what such skilled artisans considered the "M1" or "M0" layer in semiconductor structures/devices. In Pethe, the "metal (0)" layer is what connects to the trench contacts and the gate contacts:

> Referring to FIG. 5B, a metal contact structure 540 is formed in a metal (0) trench and via openings formed in a dielectric layer 330. **The metal contact structure 540 includes a metal (0) portion 550 along with trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively). The metal contact structure 540 also includes gate contact vias (e.g., gate contact vias 542A and 542B to gate stack structures 308C and 308D, respectively)**.

(EX1005 (Pethe), 12:54-67).

322. Accordingly, a POSITA would have been reasonable in considering the "M0" process to be an "M1" process because it is the first metalized trench/via process. As I discussed, the dual damascene process was known to be generally repeated a number of times. (EX1014, pp. 696-98; EX1020, p. 19.)

323. Fig. 13.30 and other Figures (for example, 14.17-20) below illustrate a via-first dual damascene copper low-k interconnection process for an M2 metal layer and M1 via over an M1 metal layer (EX1020, pp. 578, 611-14)

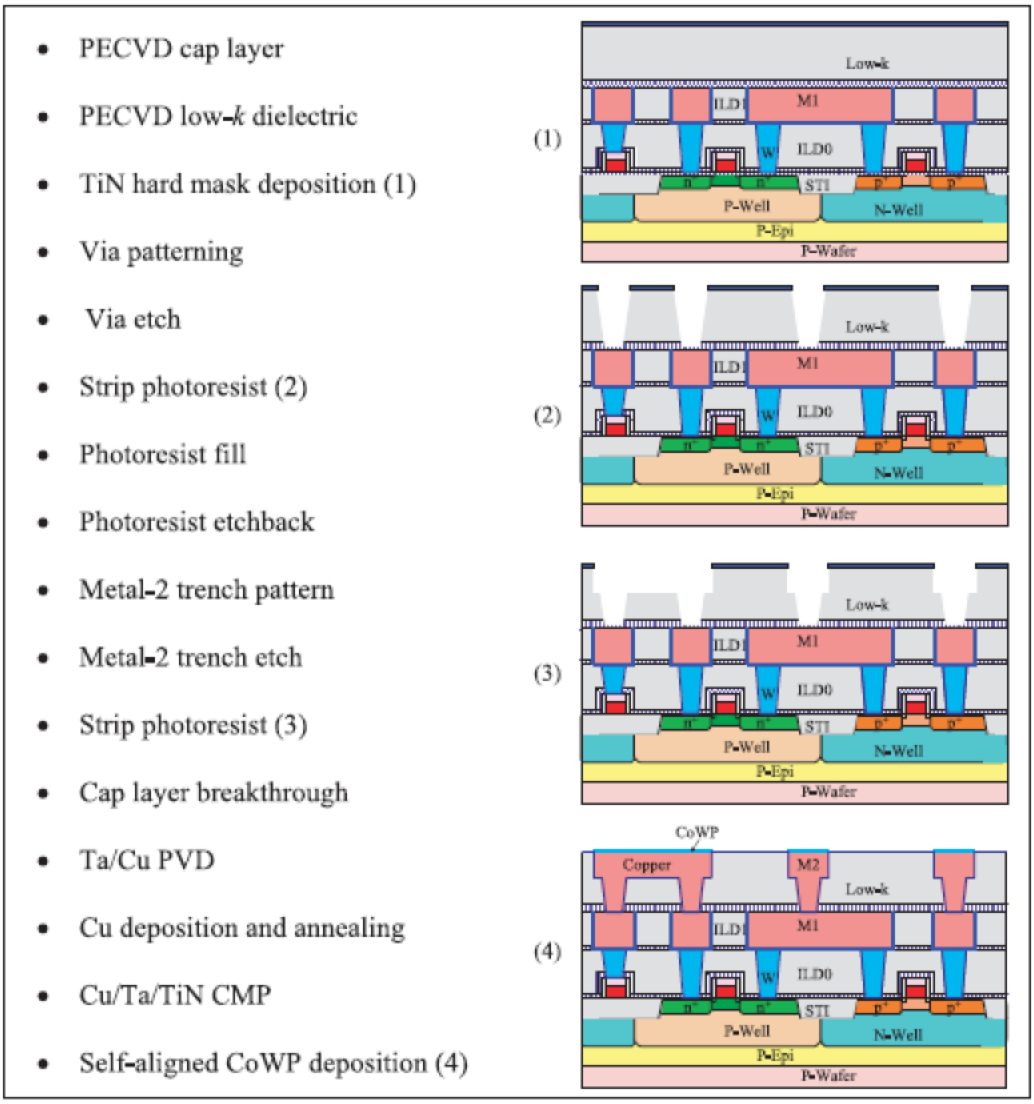


Figure 13.30 Via-first copper interconnection processing steps.

EX1020, Figure Figure 13.30

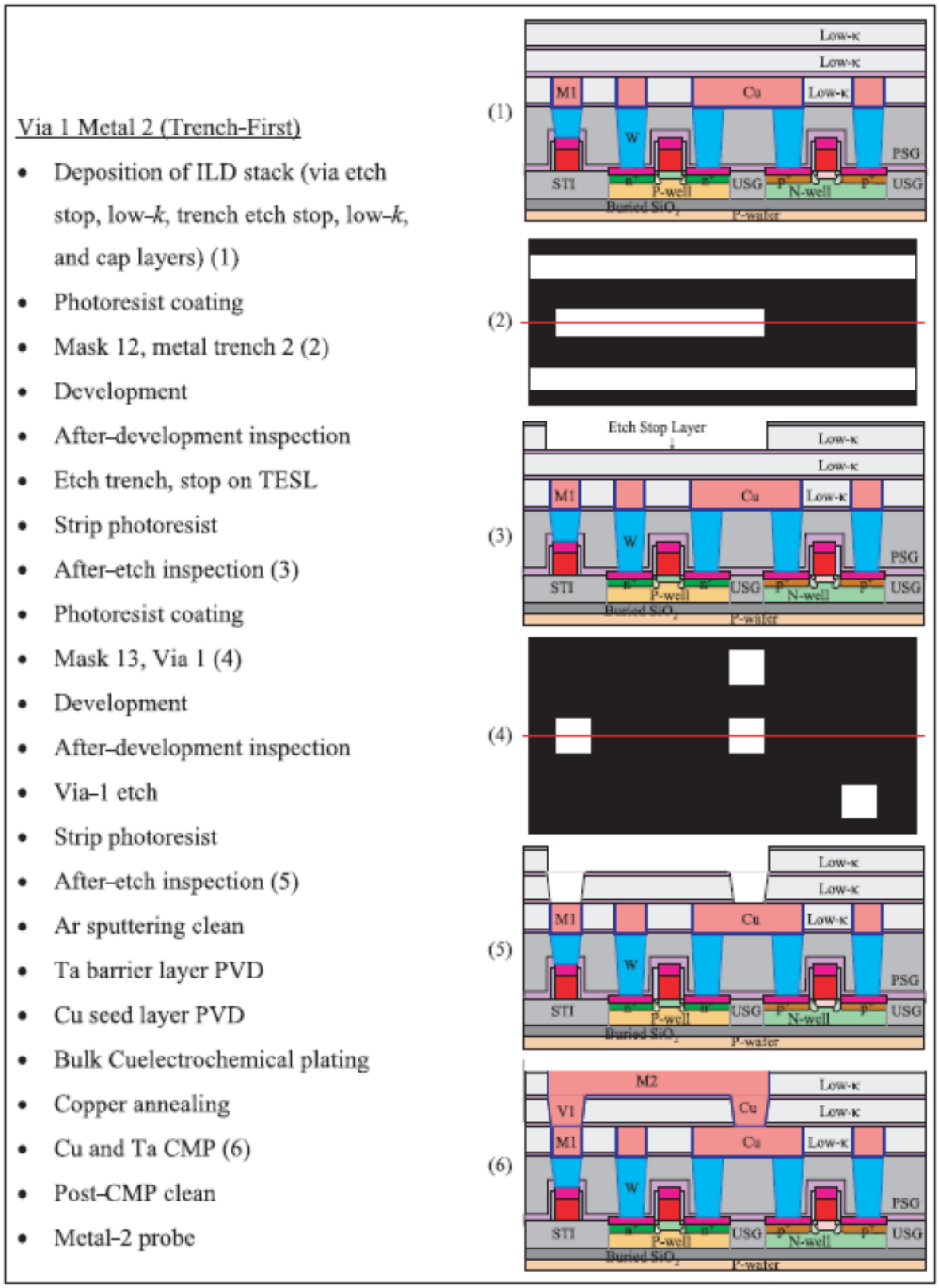


Figure 14.17 Trench-first dual damascene copper metallization.

EX1020, Figure Figure 14.17

324. Under any convention, a POSITA would have understood a dual-damascene process generally involved the conventional steps of patterning and

etching the via and trench definition, depositing metal to fill the space of both via and trench, and CMP. (*See above and for example*, EX1014, pp. 696-98; EX1015, pp. 55-56; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 19, 345-49, 453, 464, 497-98, 517-18, 543, 574-79.) A POSITA would have been able to readily apply conventional methods of dual-damascene processes, such as those taught by Huang, to Pethe with high predictability and success.

325. Accordingly, it is my opinion that a POSITA would have been motivated to modify Pethe's metal interconnection to include, above its metal (0) portion 350, Huang's M1 metal lines and M0 vias. In fact, Huang explicitly contemplates placing upper metal lines and vias over lower metal lines, such as metal (0) portion 350 in explaining that "In subsequent process steps, more metal layers (not shown) may be formed over metal layer M1." (EX1008, ¶17.)

326. The above motivation rationale discussed above for claims 8 and 9 would have been applicable to both Pethe's-Figure-5-Embodiment's structure discussed for claims 1 and 3 in §IX.A.1, IX.A.3 and to the modified Pethe's-Figure-5-Embodiment's discussed for claims 1 and 3 in §IX.A.3, 7.

327. My opinions in Grounds 1-2 explain how Pethe discloses and/or suggests claims 1-8. (§§IX.A-IX.B, incorporated herein.) However, in addition to Pethe's Figure 5B structure discussed above (claim 3 in § IX.A.3) or as modified

(claims 1 and 3 in §§IX.A.1, IX.A.7) a POSITA would have been motivated to implement **a plurality of third contacts** as claimed in claims 8-9 in view of Huang.

328. In light of Huang's teachings and a POSITA's state of art knowledge as discussed above, Pethe's Figure 5B structure would have been predictably modified to include, above its metal (0) portion 550, M1 lines and M0 vias, consistent with the teachings of Huang using the dual-damascene processes known in the art and as taught by Huang. *See Above*.

329. As a result, the modified Figure 5B structure would have included a **plurality of third contacts** (for example, parts of the newly formed M1 lines above Pethe's M0 line (550) and the associated M0 vias interconnecting the M1 and M0 lines formed based on Huang's teachings) **disposed on parts of the first contacts** (for example, parts of 341A/341B) **and on parts of the second contacts** (for example, parts of 542A/542B), as in claim 8. *Id.*

330. In addition, **each third contact** (in the modified Figure 5B structure) would have comprised **a via hole structure (M0 vias) and a trace structure (**parts of the newly formed M1 lines (*see* EX1001, 5:48-53 (trace structure may be "lines")), which would **comprise the same material and contact each other directly** (as in claim 9) given they are formed using the dual-damascene process like that taught by Huang, which would also result in **each third contact** (above) being a **monolithically formed structure (**as in claim 8).

331. In my opinion, a POSITA would have understood and appreciated that such a modification would have involved the application of known technologies/techniques (for example, dual-damascene process to provide M1 metal lines and M0 vias) to a known device/structure (like Pethe's Figure 5 embodiment with metal (0) portion 550). Accordingly, such a skilled person would have been motivated to implement such a modification, and would have reasonably expected such an implementation to be successful. A POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of providing M1 metal lines and M0 vias to a known device/structure (Pethe's Figure 5B structure with metal (0) portion 550) with operability to the M1 layer in the structure of Figure 5B.

332. In the combined structure of Pethe and Huang, M0 vias 72 (**a via hole structure**) and metal layer M1 metal lines 74 (**a trace structure**) form **a third contact**. This would have been consistent with the teachings shown in annotated Figure 8A of Huang below.

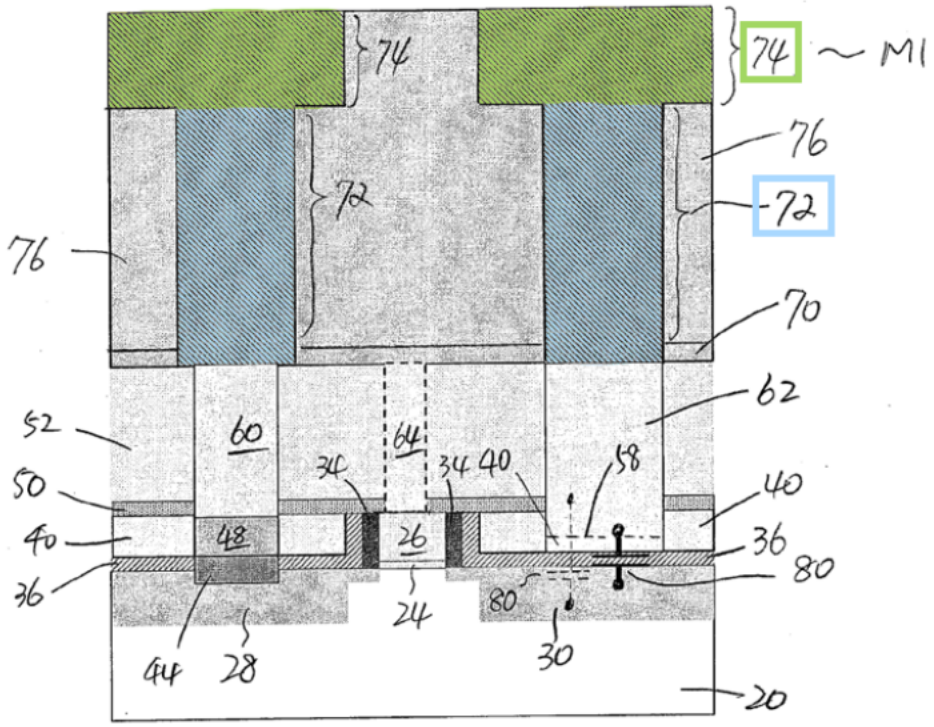


Fig. 8A

Huang, Figure 8A

(EX1008, ¶17, FIG. 8A.).

333. As I discussed in claim 8, a dual-damascene process is used to form M0 vias 72 and metal layer M1 metal lines 74 together in a single deposition, which a POSITA would have understood to mean **the via hole structure and the trace structure comprise the same material and contact each other directly**. (EX1008, ¶17 ("no noticeable interfaces are formed between MO vias 72 and the respective overlying metal lines 74."), FIG. 8A.)

E. Ground 5: Chang Discloses (Ground 5A) and Suggests (Ground 5B) Claims 1 and 2

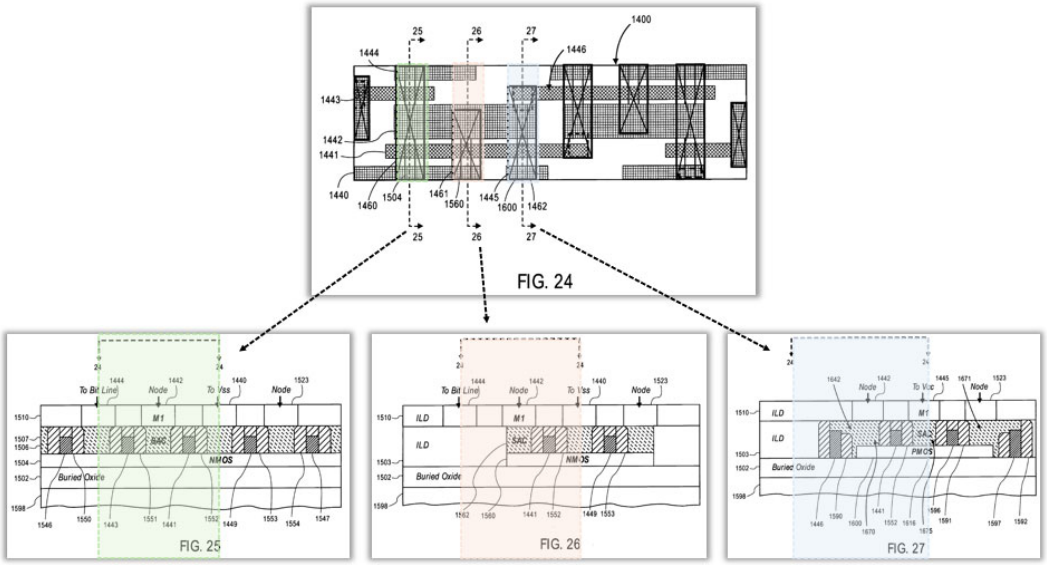
1. Claim 1

a) A semiconductor structure, comprising:

334. In my opinion, Chang discloses **[a] semiconductor structure**. (*See also* §§IX.E.1.b-IX.E.1.i.)

335. Chang's "SRAM containing transistor structures with gate-protected self-aligned contacts" in Figures 24-27 is **[a] semiconductor structure**. (EX1007 (Chang), ¶107.)

336. Figures 24-27 show different views of the same "structure." (*Id.*)



b) a substrate;

337. In my opinion, Chang discloses this limitation.

338. For example, Chang's silicon substrate 1598 is **a substrate**, as shown in the annotated Figure 27 below:

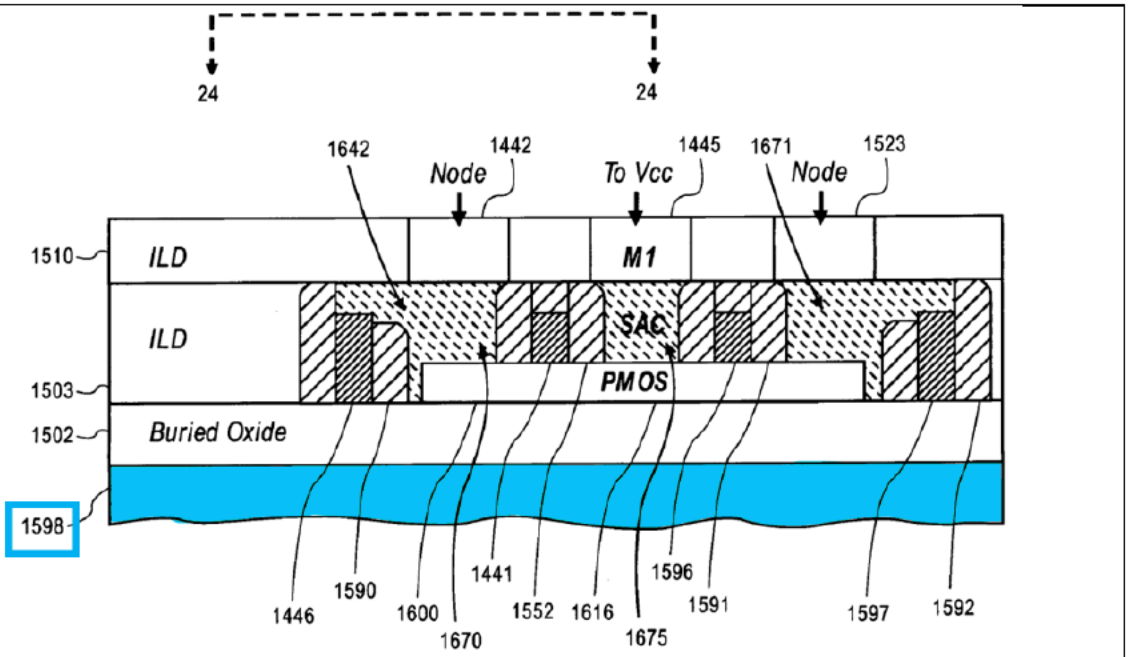


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶110.)

339. Additionally, the combination of silicon substrate 1598 and buried oxide 1502 is also a "substrate" on which the transistor structures of the SRAM is formed or built on. Further, the combination of silicon substrate 1598, buried oxide 1502, and PMOS diffusion layer 1600 is also a "substrate" on which the SRAM is formed.

340. Chang, in fact, refers to such a silicon substrate/buried oxide/diffusion layer structure as an SOI substrate, consistent with a POSITA's understanding at the time. (EX1007 (Chang), ¶46, Fig. 5.)

c) a first dielectric layer disposed on the substrate;

341. In my opinion, Chang discloses this limitation.

342. For example, Chang's "interlayer dielectric layer 1503" (**a first dielectric layer**) is **disposed on the substrate**, as shown in Figure 27:

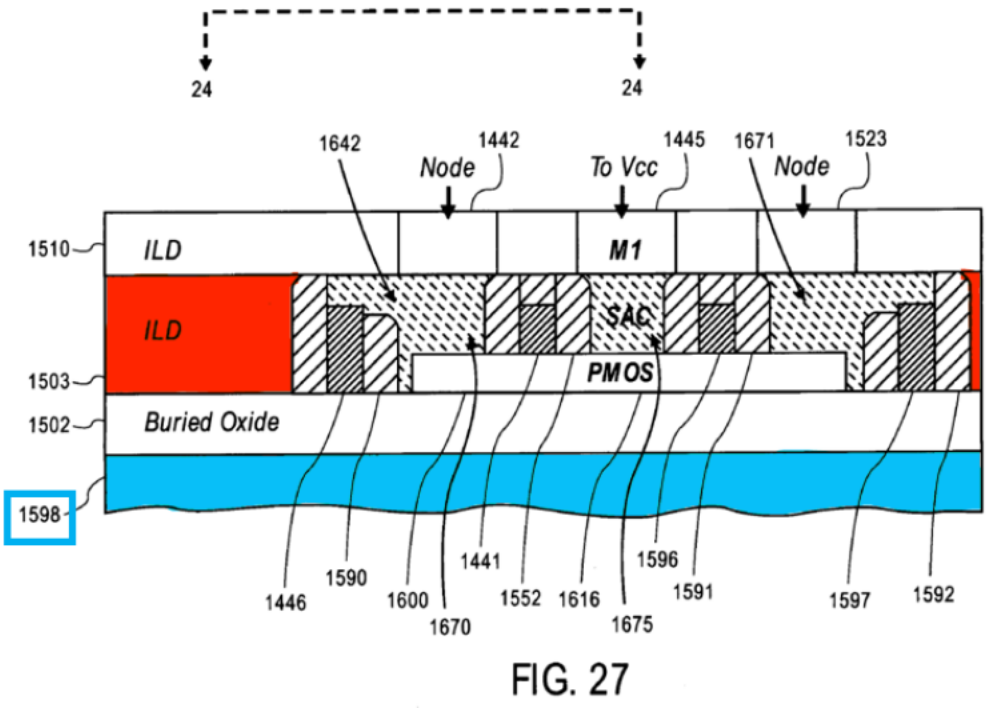


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶112.)

343. For example, ILD 1503 is disposed on the silicon substrate 1598. It is also disposed on the substrate comprising the combination of silicon substrate 1598 and buried oxide 1502. (*See* §IX.E.1.b.)

344. If **a first dielectric layer disposed on the substrate** in element [1.b] were interpreted to require the first dielectric layer be disposed *directly* on the substrate, that is disclosed by ILD 1503 being directly disposed on the substrate comprising the combination of silicon substrate 1598 and buried oxide 1502.

345. Chang further discloses that "transistors on bulk substrates" may be used with the invention instead of substrates with a buried oxide (for example, SOI substrates). (EX1007 (Chang) ¶¶ 114 ("Embodiments of the invention have been described in detail with respect to transistors on SOI with metal gates. A metal gate can be fabricated from various types of metals, including copper, aluminum, titanium, etc. Alternative embodiments of the invention can be used with other types of transistors with metal gates, such as trigate transistors and transistors on bulk silicon substrates."); 46 ("Although a silicon-on-insulator ('SOI') substrate is illustrated, the process is applicable to transistors on bulk substrates.").)

d) at least two metal gates disposed in the first dielectric layer;

346. In my opinion, Chang discloses and/or suggests this limitation.

347. For example, Chang's gates 1441, 1443, 1446, 1449, 1546-47, and 1596-97 are eight **metal gates**, which is **at least two**, as shown in the annotated Figures 24 and 27 below:

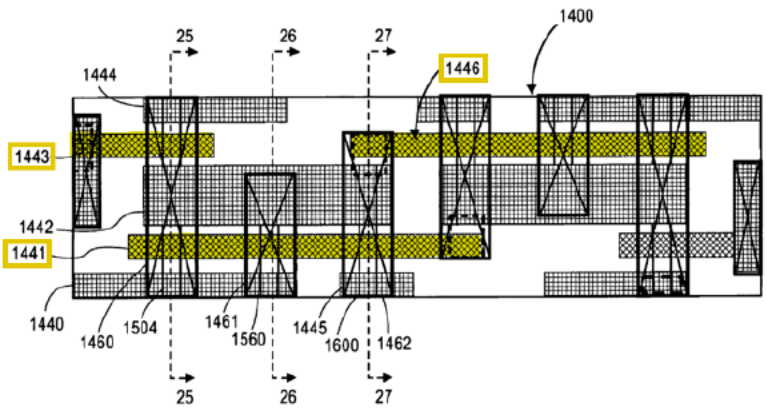


FIG. 24

Chang, Figure 24

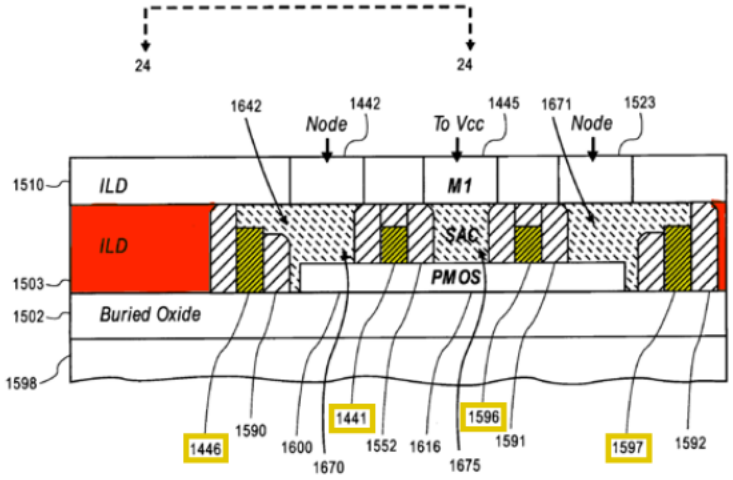


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶¶111-12, 108, 114, 47.)

348. Chang's gates are all **metal**.

349. Chang teaches "metal gates 1441 and 1449," and a POSITA would have understood the other gates to likewise be metal. (EX1007 (Chang), ¶111.) Chang also states its invention is "applicable to transistors with **metal** gates" in the plural

sense, and that the invention "is not restricted to a particular way the metal gates are formed." (EX1007 (Chang), ¶¶ 47, 114.)

350. For example, Chang discusses in its process for creating its gates with respect to Figure 5, which is "a metal gate process" for creating "metal gates." (EX1007 (Chang), ¶¶46-49.) Figures 17-23 further discuss steps related to the "metal gates" (see ¶¶89-90), which discloses operations to form the structure shown in Figures 24-27 (*id.*, ¶¶27-35, 52, 89, 107), and Chang does not describe using different materials for the gates in Figures 24-27's structure (*generally id.*).

351. A POSITA would have understood the teachings of Figures 5 and 17-23 disclose operations and methods to form the SRAM of Figures 24-27. Specifically, a POSITA would have understood that the teachings regarding the metal gates in Figures 19-20 are operations and methods to form the gates in the SRAM of Figures 24-27. Chang's "self-aligned contacts" with a "gate-protection option" "is described with respect to FIGS. 17-27." (EX1007 (Chang), ¶52.) Specifically, "FIGS. 17 through 23 show... forming self-aligned contacts" with the gate-protect option (*Id*., ¶89) and FIGS. 24-27 show "an SRAM containing transistor structures with gate-protected self-aligned contacts." (*Id*., ¶107.) In other words, Figures 17-23 illustrate forming the self-aligned contacts, and Figures 24-27 show an SRAM with those contacts, and a POSITA would have appreciated that the

teaching regarding the metal gates in Figures 17-23 would have been applied to the metal gates in the SRAM of Figures 24-27.

352. For example, Chang's teachings in Figures 17-23 (see ¶¶89-92) show forming of features related to the gates, such forming silicon nitride caps by a "recess etch" of the top of the gates, and the structure of Figures 24-27 shows an SRAM with those features, as shown below:

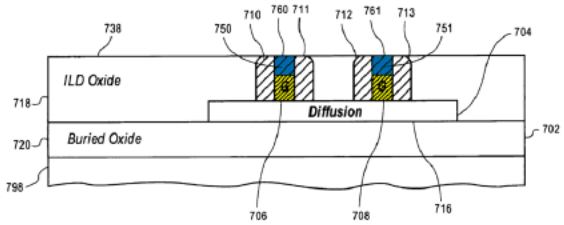


FIG. 18

Chang, Figure 18

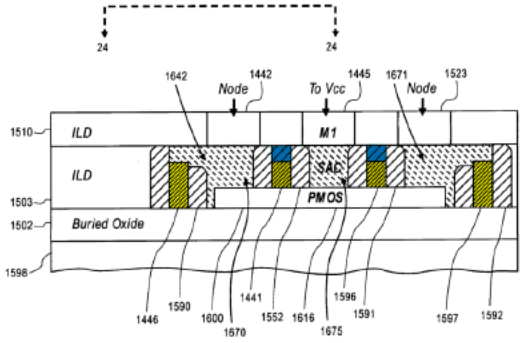


FIG. 27

Chang, Figure 27

353. Similarly, Chang's Figure 5 teachings (see ¶¶46-49) discuss forming gates with a "replacement metal gate process," and a POSITA would have understood that structure of Figures 24-27 shows an SRAM with gates produced according to that process, as shown below (of course, gates 1441 and 1596 in FIG. 27 have undergone the "recess etch" to form the silicon nitride caps per the process of Figures 17-23):

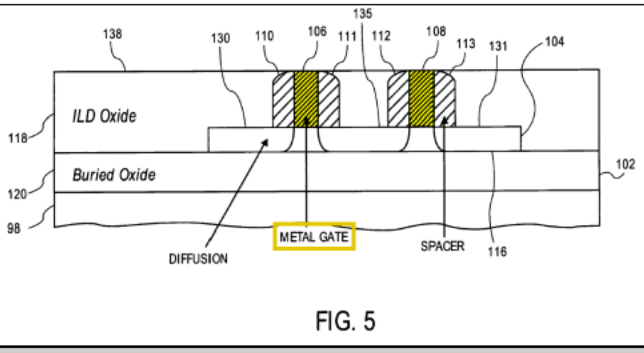


FIG. 5

Chang, Figure 5

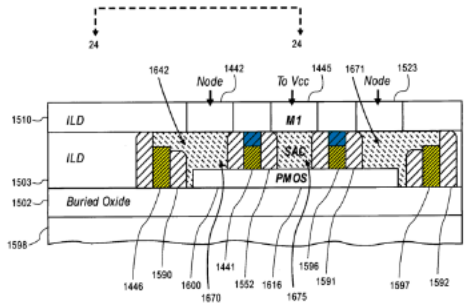


FIG. 27

Chang, Figure 27

354. As shown below, the gate structures of the SRAM of Figures 24-27 are structurally substantially the same, and are consistent with the metal gate teachings of Figures 5 and 17-23.

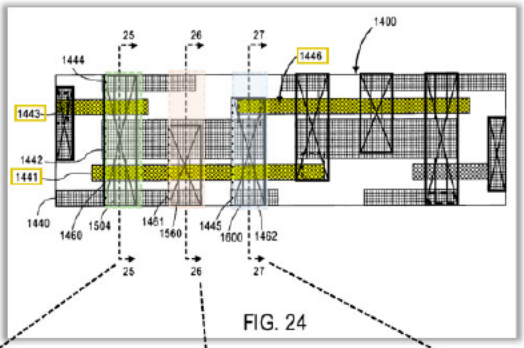


FIG. 24

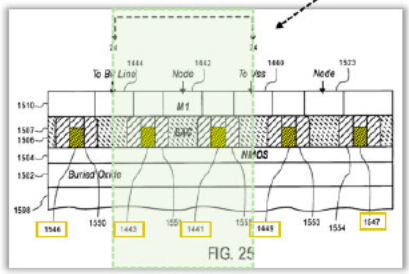


FIG. 25

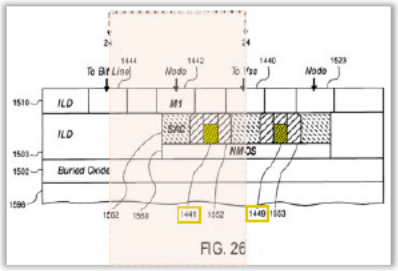


FIG. 26

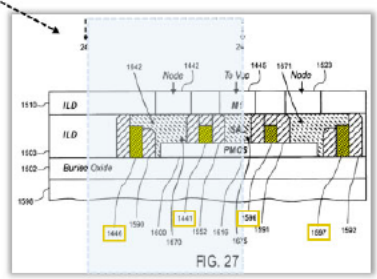


FIG. 27

Chang, Figures 24-27

355. The gates are **disposed in the first dielectric layer**, as shown in Figure 27. As Chang explains:

> The interlayer dielectric layer 1503 includes the transistor structure 1616. The transistor structure 1616 includes gate structures 1552 and 1590-1592... The gate structures 1552 and 1591 include spacers along with silicon nitride caps for the respective gates 1441 and 1596.

(EX1007 (Chang), ¶112).

356. Chang's teachings are consistent with a POSITA's knowledge of ILDs at the time, which is that they are dielectric layers providing insulation between two layers (for example, a layer below and a layer above the ILD) in a device structure and through which electrical contacts or vias are made between the layers. The relationship of metal gates and first dielectric layer in Figure is consistent with what is depicted in the '747 patent:

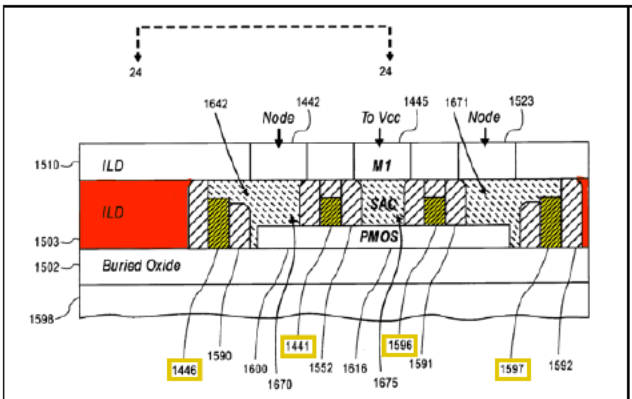


FIG. 27

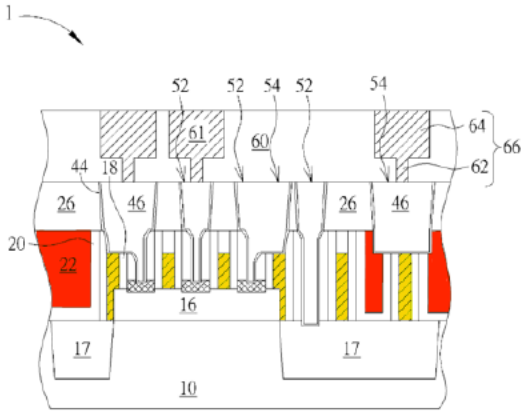


FIG. 9

Chang, Figure 27	'747 Patent, Figure 9

357. With respect to **Ground 5B,** regarding **limitation [1.d]**, notwithstanding (and in addition to the disclosures above), a POSITA would have been motivated in view of Chang's disclosures above to configure Chang's gates to

be metal. (EX1007 (Chang), ¶111.) A POSITA would have been motivated to implement, and had a reasonable expectation of success of implementing, such features since it would have involved application of known metal gates structures well within a POSITA's capabilities and knowledge at the time, consistent with Chang's teachings. (*See above*.)

358. For example, a POSITA would have appreciated that Chang explicitly teaches metal gates 1441 and 1449 in the SRAM of Figures 24-27, and teaches other substantially similar gate structures in the SRAM, in addition to teaching how to fabricate metal gates (see FIG. 5) and adapt metal gates to the SRAM of Figures 24-27 (see FIGS. 17-23.) (*See above* §IX.E.1.d, incorporated herein.) Based on such teachings/guidance and state of art knowledge, it is my opinion that a POSITA would have been motivated to simplify the fabrication process of the SRAM of Figures 24-27 by conforming its other gates to be also metal, instead of introducing unnecessary complexity and cost by providing different gates of different materials. A POSITA would have recognized the benefits and advantages of such an implementation (including e.g., simplifying the fabrication process, conserving resources such as materials and related costs), and thus had reasons to consider such a modification, which would have been consistent with Chang's teachings of using metal gates 1441 and 1449 in the SRAM of Figures 24-27.

359. Considering and implementing such knowledge, techniques, and teachings, including those explicitly taught by Chang in Figures 5 and 17-27, would have yielded the predictable result of Figure 27's structure having at least two metal gates, as claimed in limitation [1.d]. (*Id*.)

e) a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

360. In my opinion, Chang discloses this limitation.

361. For example, Chang's "gate structures 1552 and 1591 include spacers along with silicon nitride caps for the respective gates 1441 and 1596." (EX1007 (Chang), ¶112.) As shown in Figure 27, spacers 1552 are **disposed on two sides of** gate 1441 (the metal gate).[6]

[6] **[T]he metal gate** has antecedent basis to **at least two metal gates**, meaning that **the metal gate** can be any one of the **at least two metal gates**. Gate 1441 is one of the **at least two metal gates**.

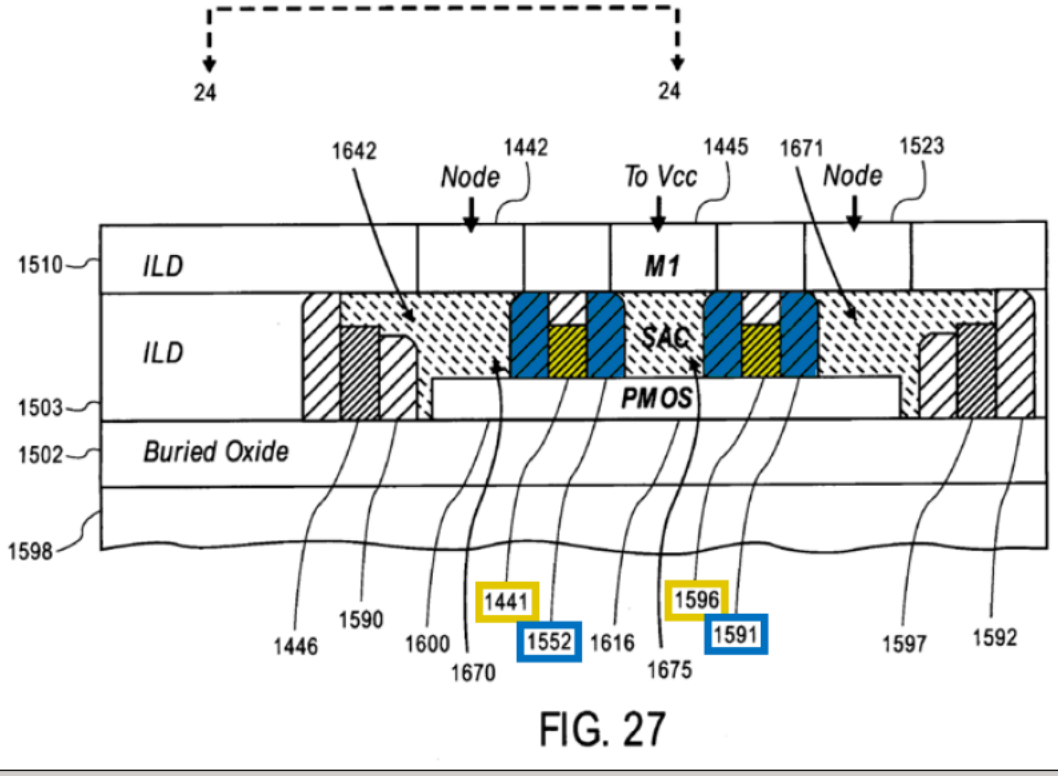


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶112).

362. Chang's gate structures 1552 and 1591 that include spacers having **a truncated top surface**.

363. With reference to FIGS. 19 and 20, Chang explains the deposition and planarization of its self-aligned contacts. (EX1007 (Chang), ¶¶94-95.) This process entails depositing a metal to fill the open areas (for example, elements 780-82) as shown in Figure 19. Afterwards:

> A polishing operation—or, alternatively, an etch operation—is then performed to **planarize the contact metal down to level 737** in order to form contact areas 820, 821, and 822. **Level 737 is a level slightly below the original top level 738**. The tops of **spacers 710 through 713** and silicon

nitride gate caps 760 and 761 are **not covered by the contact metal after the planarization step is completed**. Thus, the contact metal areas 820, 821, and 822 are not electrically interconnected with each other.

(EX1007 (Chang), ¶¶94-95.)

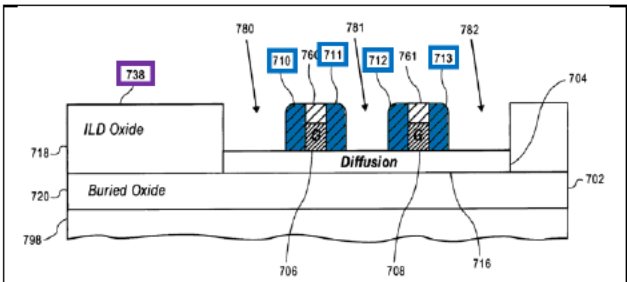


FIG. 19

Chang, Figure 19

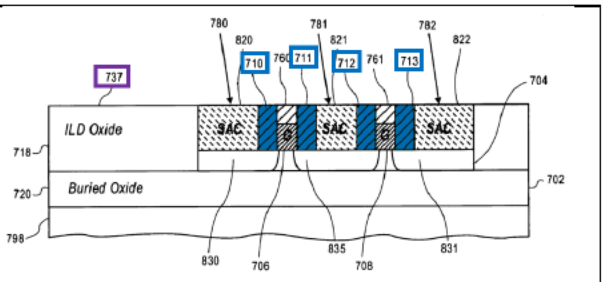


FIG. 20

Chang, Figure 20

364. Thus, as shown in Figures 19-20, the polishing lowers the level of the top of the wafer from 738 (Figure 19) to 737 (Figure 20). (EX1007 (Chang), ¶¶95 ("Level 737 is a level slightly below the original top level 738."), 94.). As shown, the spacers are at these respective levels 738 (before the deposition and polish) and 737 (after the deposition and polish is completed), meaning the polishing removed spacer material, providing **a truncated top surface**.

365. A POSITA would have understood that the teachings regarding the spacers in Figures 19-20 involve operations and methods to form to the gate structures 1552 and 1591 including spacers in the SRAM of Figures 24-27. These gate structures, shown in the SRAM of Figures 24-27, are disclosed in the context of Chang's "self-aligned contacts" with a "gate-protection option," which Chang

explains "is described with respect to FIGS. 17-27." (EX1007 (Chang), ¶[0052].)[7] Specifically, "FIGS. 17 through 23 show wafer cross sections that illustrate operations in connection with the gate-protect option with respect to forming self-aligned contacts" (*Id.*, ¶89) and "FIG. 24 is a top view of a layout 1400 of an SRAM containing transistor structures *with* **gate-protected self-aligned contacts**… cross sections of the SRAM layout 1400 are shown in FIGS. 25, 26, and 27." (*Id.*, ¶107.) A POSITA would have understood that the teachings of Figure 17-23 are operations and methods to form to the SRAM of Figures 24-27. Specifically, Figures 17-23 illustrate forming the self-aligned contacts, and Figures 24-27 show an SRAM with those contacts.

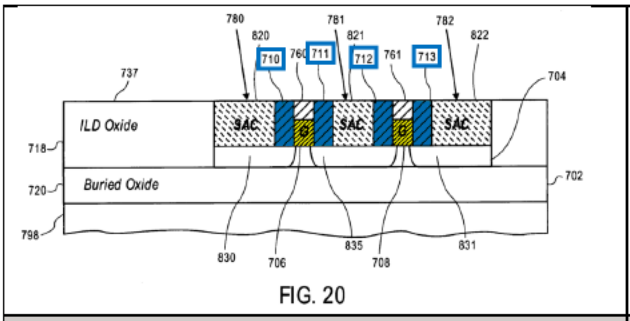


FIG. 20

Chang, Figure 20

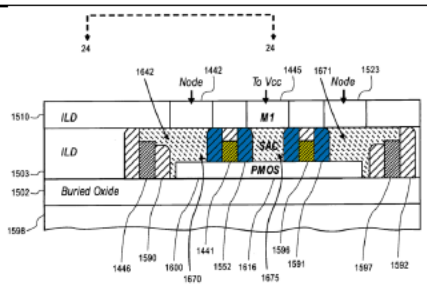


FIG. 27

Chang, Figure 27

366. Chang provides good reason to truncate its spacers: so that the contact metal areas "are not electrically interconnected with each other." (EX1007 (Chang),

[7] Chang discloses an alternative "no gate-protect option … in reference to FIGS. 6 through 16." (EX1007 (Chang), ¶0051.)

¶¶94-95.) A POSITA would have understood that electrical isolation between separate contacts on the same or different transistors must be maintained to ensure the desired functionality and operation of the respective transistor and that of the integrated circuit, such as the SRAM (as discussed in Chang).

367. If a contact metallization is not removed fully between respective contacts, the contacts will not be electrically isolated. Consistent with this ordinary understanding of a POSITA, Chang itself expresses a desire to maintain such isolation between its separate contacts. A POSITA would have understood that without truncating the spacers, the device would be susceptible to electrical shorting.

f) a source/drain region (S/D region) disposed between two metal gates;

368. In my opinion, Chang discloses this limitation.

369. Chang discloses its embodiments in the context of "transistors." (*See*, *e.g.*, EX1007 (Chang), Title; Abstract; [0001], [0039, [0041], [0045]-[0048],[0089], [0090].) Further, Chang discloses its "transistors" as having features such as "gate structures" and "drain and source regions," known to be associated with field effect transistors. (*See*, *e.g.*, id., Abstract; [0039], [0041], [0048], [0063], [0071], [0089], [0096], [0098].)

370. These transistor structures, shown in Figure 27, are disclosed in the context of Chang's "self-aligned contacts" with a "gate-protection option," which Chang explains "is described with respect to FIGS. 17-27." (EX1007 (Chang),

¶[0052].) Figures 17-23 illustrate forming the self-aligned contacts in such transistor structures, and Figures 24-27 show multiple transistors with those contacts in an SRAM circuit configuration.

371. Regarding Figure 27's transistor structures, Chang teaches that these structures include "gate structures," as well as a "diffusion region" (or "PMOS region" or "PMOS layer") 1600. (EX1007 (Chang), ¶¶ [0112, [0113].) A POSITA would have understood that layer 1600 contains source and drain regions, as shown in the annotated Figures 24 and 27 below. (EX1007 (Chang), ¶¶112-13, 96-98.) Each source and drain region would have been understood by a POSITA to be a source/drain region. As further shown in the annotated Figures 24 and 27 of Chang, each source/drain region (S/D region) is **disposed between two metal gates**:

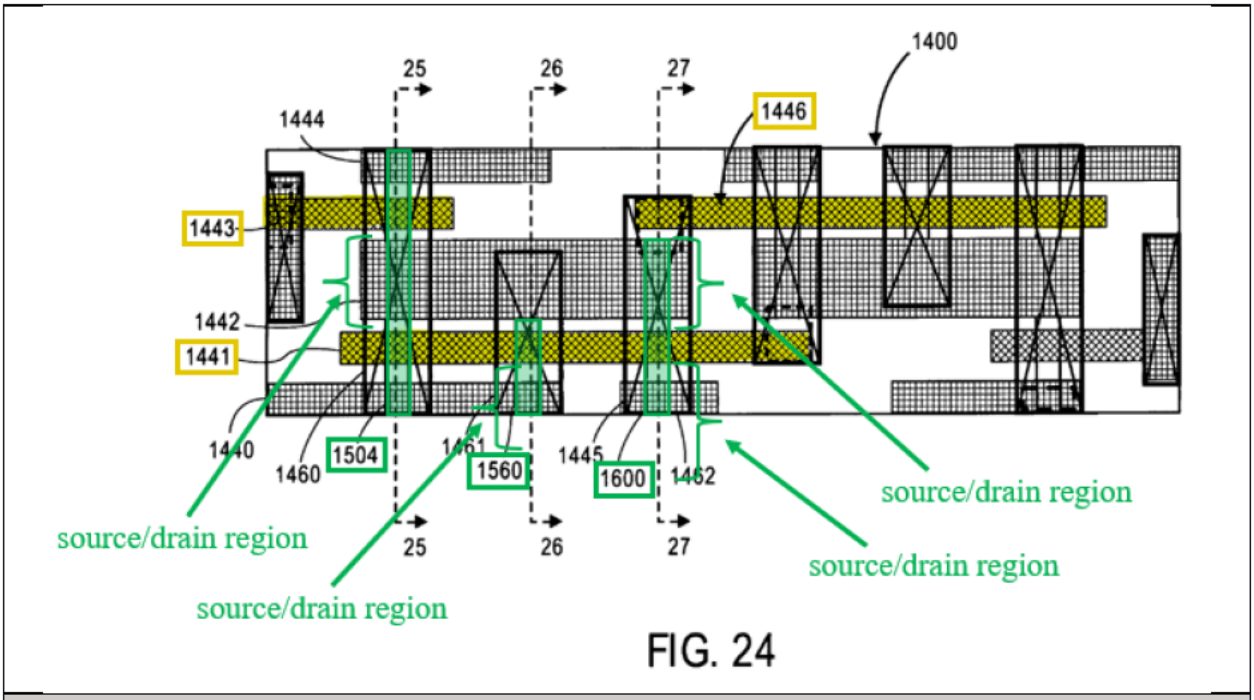
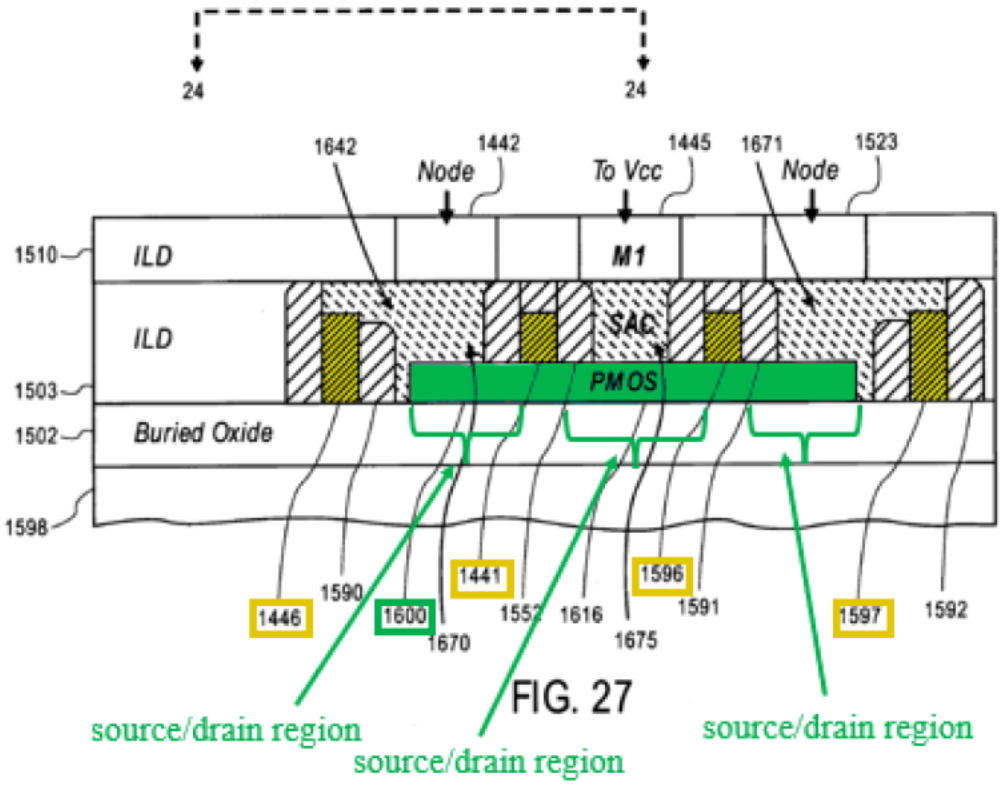


FIG. 24

Chang, Figure 24



Chang, Figure 27

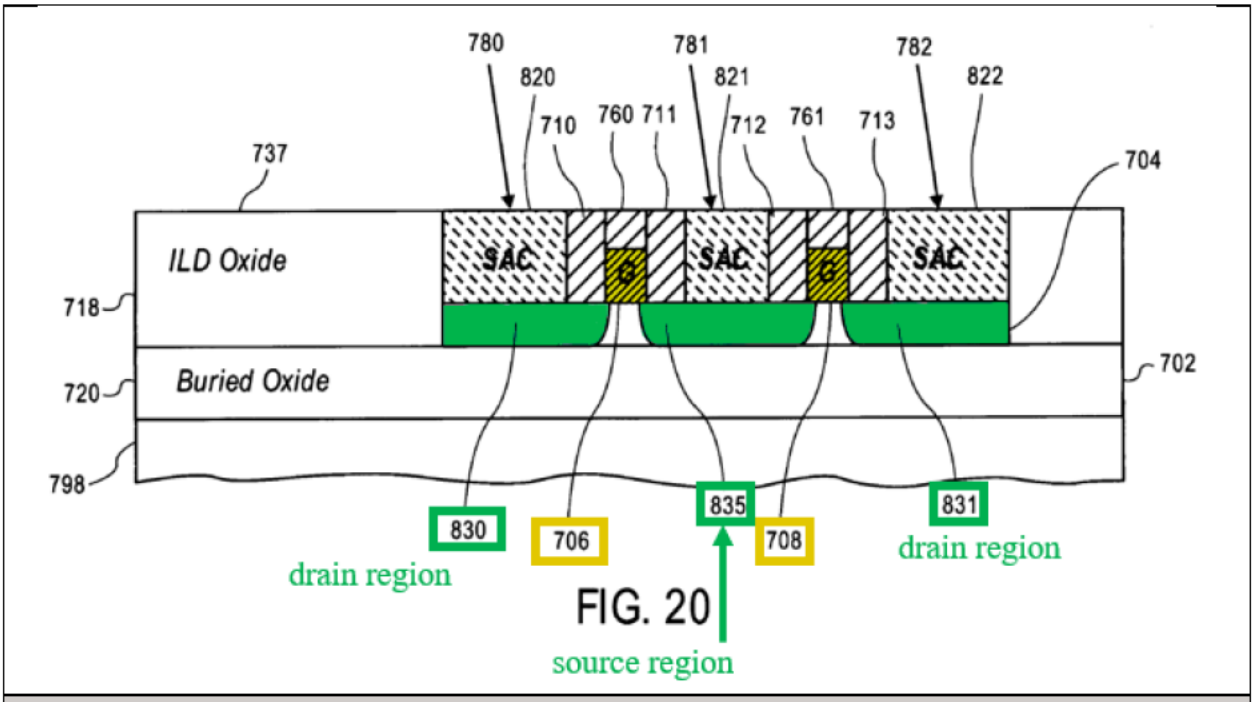
(EX1007 (Chang), ¶¶112-13, 96-98.)

372. Further, with reference to Figure 20, Chang explicitly describes a "diffusion area 704" that contains drain regions 830 and 831 and source region 835, which is **a source/drain region (S/D region) disposed between two metal gates** 706 and 708, as shown in the annotated Figure 20 below. As shown in the annotated Figures 24 and 27 above, the **source/drain region (S/D region)** of diffusion region 1600 are located in the corresponding locations.

373. As discussed in element [1.d], the teachings of FIGS. 20 and 24-27 describe Chang's "self-aligned contacts" with a "gate-protection option." (EX1007

(Chang), ¶[0052].). These teachings are methods and operations for forming the SRAM of Figures 24-27 for the same reasons discussed in element [1.e]. (*See* §IX.E.1.e.)

374. This configuration represents a conventional source, drain, and gate in a field effect transistor.



Chang, Figure 20

375. Thus, a POSITA would have understood in the context of Chang's teachings, the diffusion layer 1600 of Figure 27 include a **source/drain region (S/D region)**, as described above, including a **source/drain region (S/D region) disposed between the two metal gates 1441 and 1596**.

376. With respect to **Ground 5B**, regarding **limitation [1.f]**, notwithstanding (and in addition to) the above Chang disclosures, it is my opinion

that a POSITA would have been motivated to configure the Figure 27 structure to include **source/drain region (S/D region) disposed between the two metal gates 1441 and 1596**.

377. A POSITA would have recognized Chang's references to transistor features (including source/drain regions) (EX1007 (Chang), ¶¶112-113.) and that such features were needed on both sides of a gate for the structure/device to operate as an FET, as contemplated by Chang (*id.*).

378. In view of Chang, a POSITA would have understood that Chang's discussions of a "gate" would have led such a POSITA to understand that a FET was contemplated by Chang's structure and thus would have been motivated to include a S/D region on both sides of each gate 1441, 1596 to have functional FETs. As I discuss in Section V.A, gates are used to control current flow between a source and drain, so Chang's teaching of gates would have informed a POSITA of the need to have source and drains for which the gate is controlling the current.

379. A POSITA would have had a reasonable expectation of success implementing such a modification given it would have involved application of known transistor structure/process technologies, consistent with Chang's teachings and a POSITA's knowledge at the time, predictably resulting in Chang's Figure 24-27 embodiment structure having **a source/drain region (S/D region) disposed between two metal gates**, as claimed.

380. A POSITA would have had such motivation because such a skilled person would have recognized and appreciated Chang's numerous references to transistor features, including features consistent with source/drain regions of a transistor. (*See* citations and discussions of Chang immediately above; *for example*, EX1007 (Chang), [0112], [0113].) And as I discussed above, A POSITA would have also understood and appreciated that to make a semiconductor device with transistors, as contemplated by Chang (*see, for example*, EX1007 (Chang), [0112], [0113]), a source/drain region was needed on both sides of a gate in order for the structure/device to operate as a field effect transistor.

381. As I discussed in Section V.A (which I incorporate by reference here), FETs are fundamentally structured as shown below, with a channel beneath a "gate" (G) between, and "source" (S) and "drain" (D) regions on each side of the gate such that current flows between the source and drain regions through the channel formed under the gate of the FET.

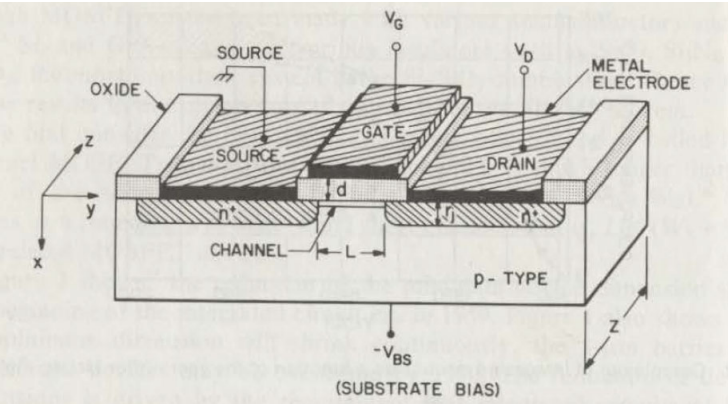


Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

(EX1023, 433-34, 438, Figs. 3, 6.)

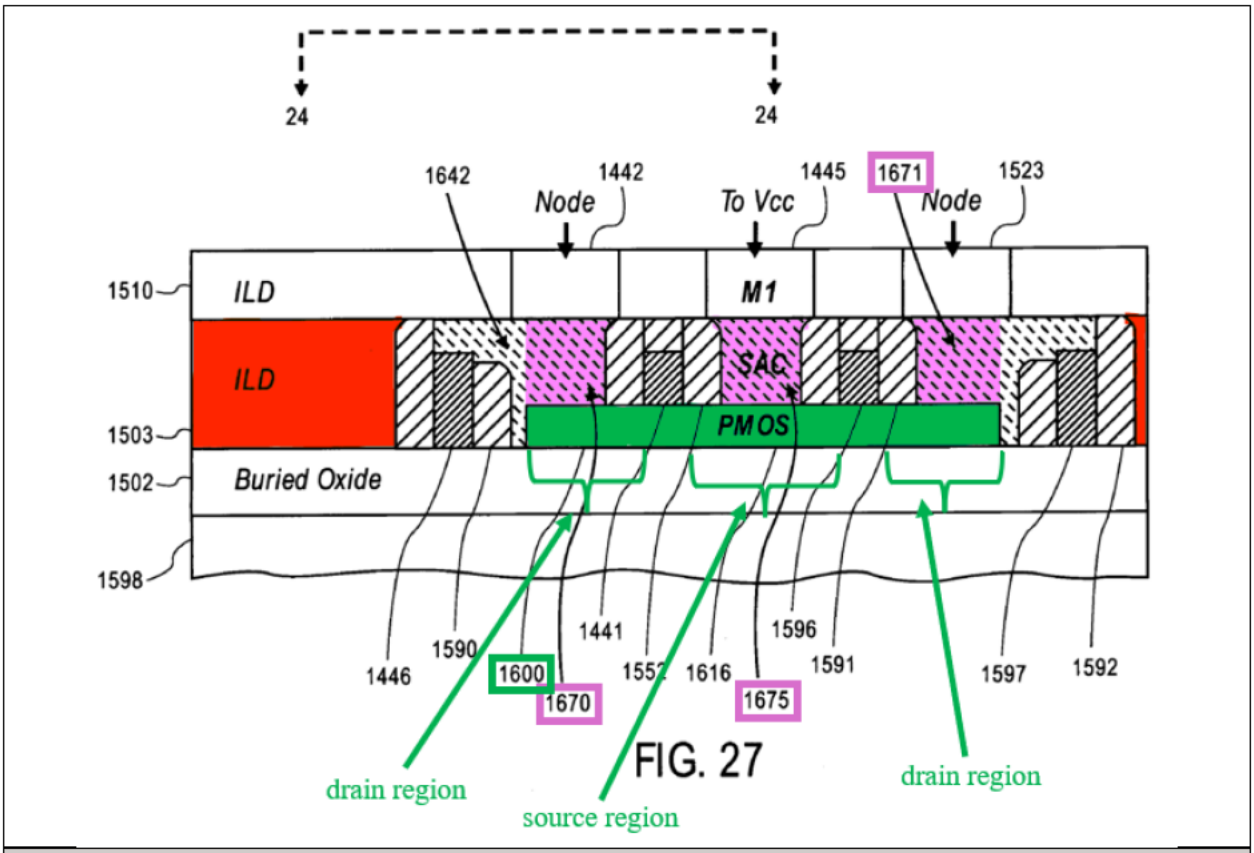
382. Chang's discussions of a "gate" would have led a POSITA to understand that a field effect transistor (FET) transistor was contemplated by Chang in connection with its disclosed transistor structure. Thus, in order to have functional FETs (For example), a POSITA would have been motivated to include a S/D region on both sides of each gates 1441 and 1596 (as shown above in annotated Figure 27).

383. A POSITA would have been motivated to implement such a modification, and would have reasonably expected such an implementation to be successful. In my opinion, a POSITA would have understood that implement the modification discussed above would have involved the application of known transistor structure and process technologies that were well within the capabilities and knowledge of a POSITA at the time, consistent with the teachings of Chang. In my opinion, a POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of Chang's Figure 27 structure having **a source/drain region (S/D region)** that is **disposed between two metal gates**, like that recited in element [1.f].

g) a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;

384. In my opinion, Chang discloses this limitation.

385. Parts of self-aligned contacts 1670 and 1671, and self-aligned contact 1675 (as indicated in the annotated Figure 27 below) are **a plurality of first contacts that are electrically connected to parts of the** S/D regions of PMOS diffusion layer 1600 and are **disposed in** interlayer dielectric layer 1503 **(the first dielectric layer)**.



Chang, Figure 27

(EX1007 (Chang), ¶¶112-13.)

386. Chang explains, "each of the respective self-aligned contacts 1670 and 1671" contacts the respective "adjacent PMOS diffusion region 1600." (*Id.*)

h) a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second

contacts; and

387. In my opinion, Chang discloses this limitation.

388. For example, Chang discloses self-aligned contacts 1670 and 1671 (as indicated in the annotated Figure 27 below) that are **a plurality of second contacts** that **are electrically connected to** gates 1446 and 1597 and are disposed in interlayer dielectric layer 1503 (**the first dielectric layer**):

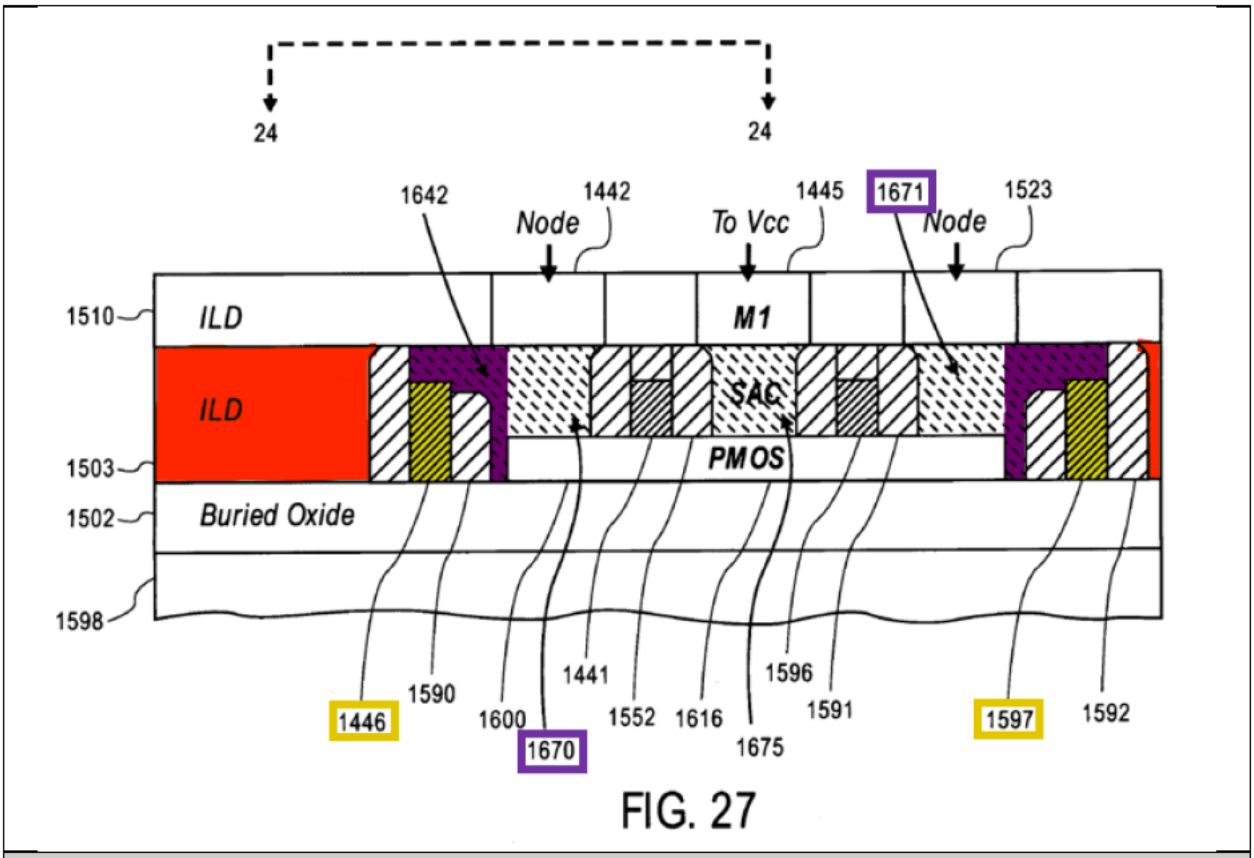


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶¶112-13.)

389. Additional examples of second contacts include metal gate contacts in notch 1105. (EX1007 (Chang), ¶105, FIG. 23.) As Chang explains, "each of the respective self-aligned contacts 1670 and 1671" "contacts the respective gate." (*Id*.)

390. Chang discloses that **at least one of the first contacts directly connects at least one of the second contacts**. Chang teaches that:

> "For gate structures 1590 and 1592, each of the respective self-aligned contacts 1670 and 1671 acts as a **merged contact** that contacts the respective gate as well as the adjacent PMOS diffusion region 1600. Thus, contact 1670 contacts gate 1446 and PMOS region 1600. Contact 1671 contacts gate 1597 and PMOS region 1600."

(EX1007 (Chang), ¶¶112).

391. In other words, each self-aligned contacts 1670 and 1671 has respective portions that serve as second contacts to the gate and first contacts to parts of PMOS region source/drain region, and are "merged" without any intervening layers or other barriers (i.e., they **directly connect[]**).

392. For example, for "merged contact" 1670, the right half (as indicated in the annotated Figure 27 below) of self-aligned contact 1670 (**at least one of the first contacts**) **directly connects** the left half (as indicated in the annotated Figure 27 below) of self-aligned contact 1670 (**at least one of the second contacts**). The same is true for merged contact 1671.

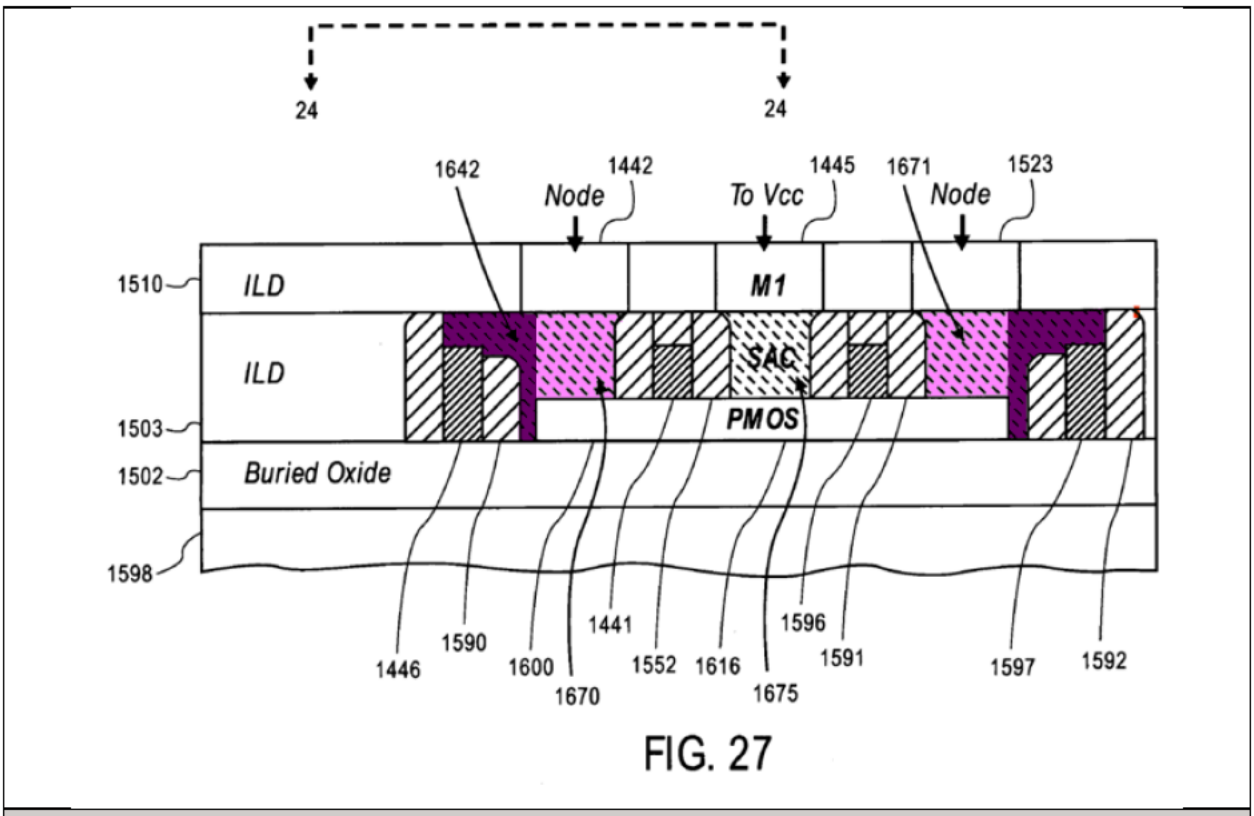


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶¶112-13)

393. A POSITA would have understood that a "merged contact" comprises multiple contacts that are merged together.

394. Further, Chang explains that the two contacts that are "merged" each serve a separate role based on what structure they contact (i.e., either the gate or the PMOS region). (*Id.*, ¶¶__.)

i) a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

395. In my opinion, Chang discloses this limitation.

396. For example, Chang's silicon nitride caps are **a hard mask** that are **disposed on** the gates 1441 and 1596.

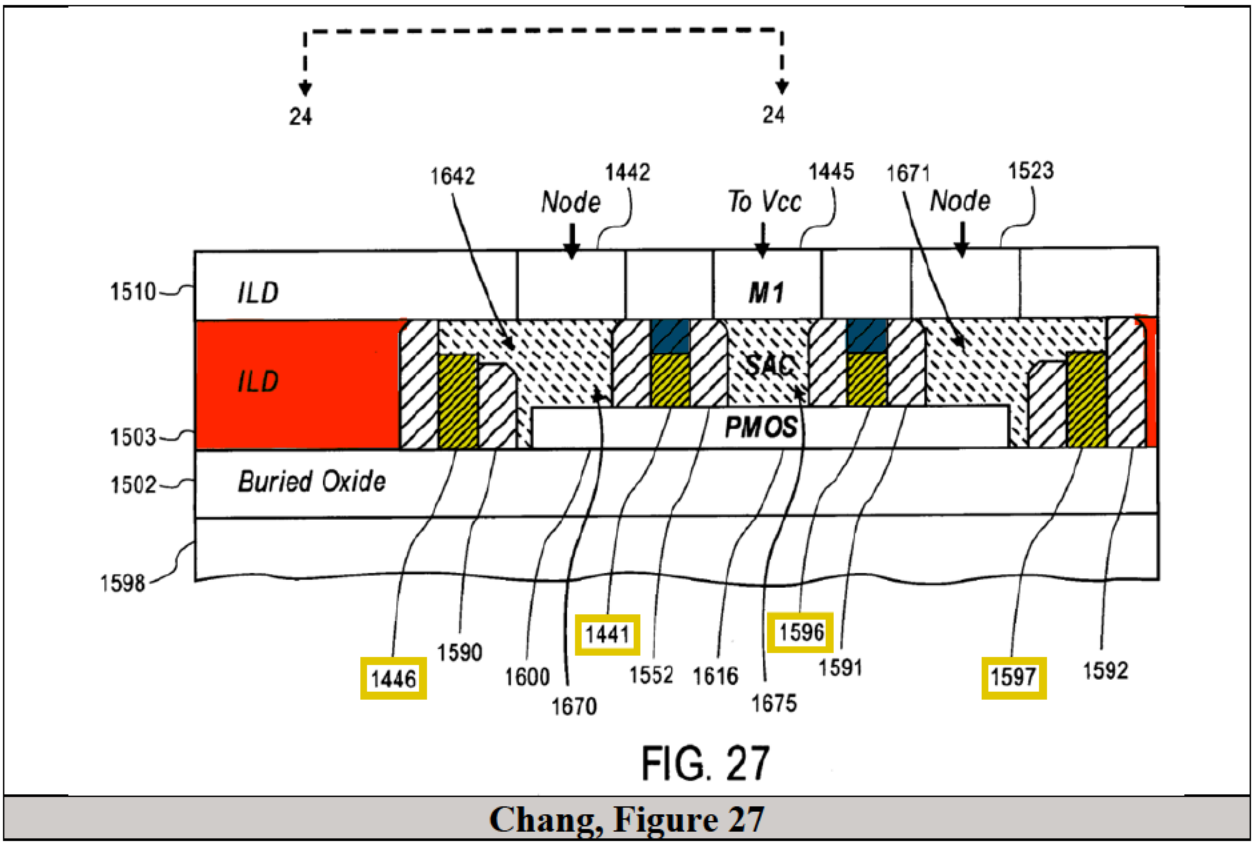


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶¶111-13)

397. Chang explains that the purpose of the silicon nitride caps is to provide protection to the below feature, which is the purpose of a **hard mask**. For example, Chang further explains that "[i]f there were alignment errors, then the metal one layer 1510 could short to the gates of gate structures 1550-1554 if those gates **were not protected by** the silicon nitride caps above those respective gates." (EX1007 (Chang), ¶111, see also ¶¶92-93 (silicon nitride caps "act as protection for" gates), ¶99 ("the metal gates 706 and 708 **are protected by** respective silicon nitride caps

760 and 761").) Silicon nitride is a known material for hard masks, which is confirmed by the '747 patent's description that "the hard mask 24 mainly comprise silicon nitride." (EX1001, 3:20-21)

398. As shown in the annotated Figure 27 above, the **top surface of** silicon nitride caps **and the top surface of** interlayer dielectric layer 1503 **are on the same level**, which is the level of the interface between ILD 1503 and 1510. This is further confirmed by Chang's disclosure of the process used to form its gate-protected self-aligned contacts whereby a "silicon nitride layer is formed over the top" of the wafer "by deposition," and "planarized by polishing the top of [the] wafer," thereby resulting in the top surface of the silicon nitride cap (hardmask) and the top surface of the ILD (first dielectric layer) on the same level. (EX1007 (Chang), ¶92, FIG. 18.) [8] As Chang explains, "[t]he polishing is done down to the top 738 of wafer 702," which is also the top surface of the first dielectric layer. (*Id*.)

[8] A POSITA would have understood that the teachings of Figure 17-23 illustrate forming the self-aligned contacts, and Figures 24-27 show an SRAM with those contacts. *See section* § IX.F.1.e. The teachings of Figure 17-23 are methods and operations for the SRAM of Figures 24-27 for the same reasons discussed in element [1.e]. (*See section* §IX.G.1.e.)

A POSITA would have understood that the subsequent deposition and planarization of its self-aligned contacts (see element [1.e]) would have polished down the entire top surface by the same amount (as discussed in element [1.e]), including the silicon nitride caps and interlayer dielectric layer 1503.

399. As discussed above, the silicon nitride caps are to provide protection to the gates below it (in ILD 1503) from the metal one layer (in ILD 1510).

2. Claim 2

a) The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

400. In my opinion, Chang discloses this limitation.

401. For example, Chang's layer 1510 includes an interlayer dielectric **(a second dielectric layer)** that is **disposed on** layer 1503 **(the first dielectric layer)**, as shown in annotated Figure 27 below:

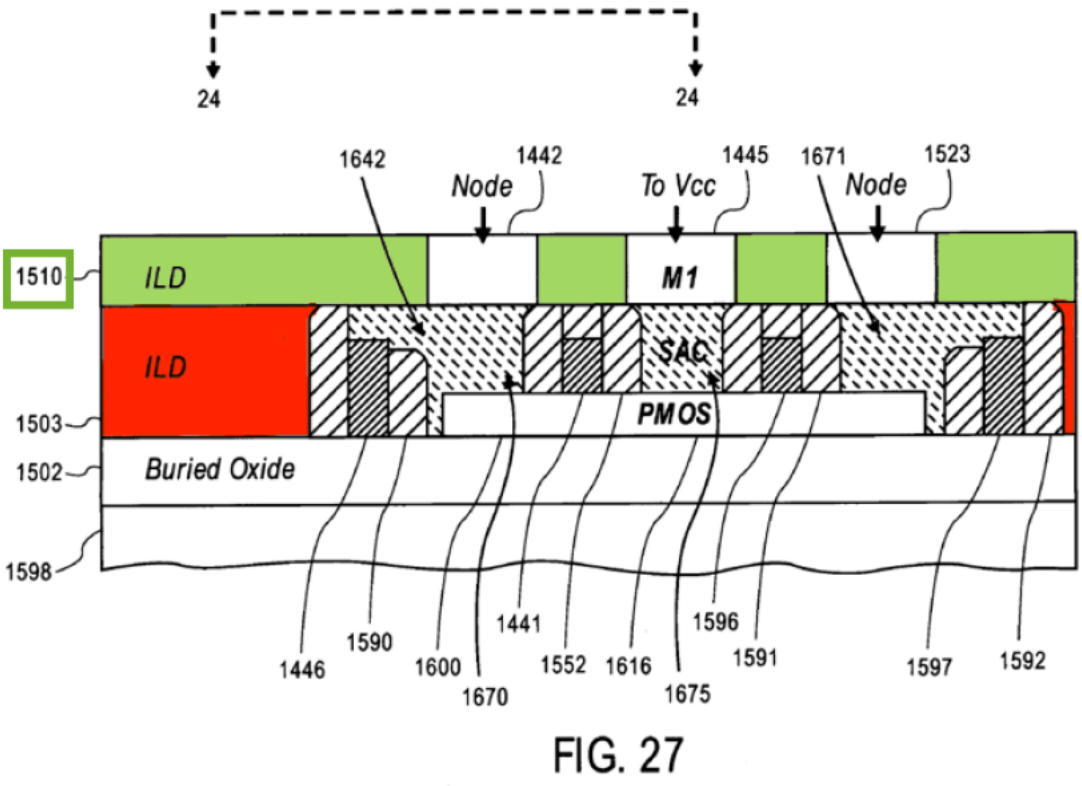


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶113)

402. Chang's "metal one layer 1510 includes an interlayer dielectric that includes openings containing the metal lines 1442, 1445, and 1523." (*Id.*)

3. Combination of Chang's Embodiments

403. Chang discloses various aspects regarding the layout and fabrication of semiconductor structures and self-aligned contacts for transistor. See EX1007 (Chang), ¶1, ¶¶17-44; id., generally ¶¶45-117. While as explained in Ground 5, Chang's discussions relating to Figures 24-27 disclose the features of claims 1-2 (§IX.E), a POSITA would have been motivated to combine teachings from other

aspects of Chang in light of a POSITA's state of art knowledge when considering and implementing the structure associated with Figures 24-27 as addressed in Ground 5.

404. A POSITA would have been motivated to incorporate various teachings/suggestions from Chang's embodiments given they all relate to various aspects of self-aligned contacts and methods of fabricating such contacts in a semiconductor structure, and do so while leveraging their state of art knowledge. EX1007 (Chang), Abstract, ¶¶36-37, 114-117.

405. Given such related teachings/suggestions, a POSITA would have been motivated to consider and implement from teachings related to other aspects of Chang's invention, and from their state of art knowledge, when forming/configuring the Figures 24-27 structure, and would have had a reasonable expectation of success in achieving such implementations.

406. A POSITA would have recognized implementing teachings/suggestions from the various aspects of Chang's disclosed invention with the Figures 24-27 structure would have involved techniques/technologies already contemplated by the collective teachings found in Chang and consistent with a POSITA's knowledge in the art. *Id*. Thus, for these reasons, and those additionally discussed below, a POSITA would have been motivated to implement a POSITA's state of art knowledge while combining certain teachings/suggestions from various

disclosed aspects of Chang to Chang's structure as described by Figures 24-27 and would predictably have resulted in a structure meeting the identified challenged claims as explained below. *Id*.

407. In addition to Chang's discussions of features discussed in other portions of Chang's disclosure (for example, those relating to Figures 5, 17-23, etc.) being incorporated in the teachings for Chang's Figure 24-27 structure, a POSITA would have been motivated to consider and implement them when forming/configuring the Figure 24-27 structure (as discussed above in §§IX.E.1-IX.E.3), and would have had a reasonable expectation of success in doing so.

408. In my opinion, a POSITA would have recognized and appreciated that Chang relates/references various features in its disclosure in describing the disclosed invention, which all relate to self-aligned contacts and methods of fabricating such contacts in a semiconductor structure (for example, EX1007 (Chang), FIGs. 5, 17-23, 24-27, Abstract, ¶¶27-35, 36-37, 45-49, 52, 89-90, 107, 114-117), and thus been motivated to incorporate such combined teachings to yield the predictable result of a structure as discussed above for claims 1-2. §§IX.E.1-IX.E.3.

F. Ground 6: Chang Discloses and/or Suggests Claims 4-6

409. The analysis in Ground 5A-5B demonstrates how Chang discloses and/or suggests **claims 1-2**. (*See above* §IX.E, which I incorporate herein by reference.)

1. Claims 4-5

4. The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

5. The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

410. Regarding **claim 5**, as I discussed above (§IX.E.1.h incorporated herein), Chang teaches **a plurality of second contacts** formed by parts of "each of the respective self-aligned contacts 1670 and 1671" (**disposed in the first dielectric layer**). Chang further explains that "the gate contact may be formed at the same time the metal one layer is formed." (EX1007 (Chang), ¶105.)

411. The metal one layer is within the ILD 1510 layer, meaning that the gate contact can be formed by a deposition step that deposits the contact material into an opening extending from the ILD 1510 to the gate. Thus, the second contact can be disposed in the first dielectric layer (ILD 1503) and the ILD 1510 (**second dielectric layer**). (EX1007 (Chang), ¶¶112-13.) This means that the identified **second contacts** are **a monolithically formed structure**, as claimed. (EX1007 (Chang), ¶¶105, 112-13; 100-06.)

412. Notwithstanding Chang's disclosure, it is my opinion that a POSITA would have been motivated to form Chang's structure's contacts (such as self-

aligned contacts 1670, 1671) during this single deposition. Chang recognizes that such a single deposition approach advantageously "result[s] in a higher aspect ratio for etch and metal deposition." (EX1007 (Chang), ¶105.) A higher aspect ratio (i.e., height divided by width) contact means the density is increased (e.g., contact is achieved with a narrower width), and thus less chip area is required for a given structure/device, and as a result, more structures/devices may be provided on a given chip area. (EX1014, 600 ("Increasing the metal line aspect-ratios... improv[e] interconnect performance and density."); EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 463-64.)

413. Thus, a POSITA would have been motivated to implement such features resulting in Chang's structure to include each second contact being a monolithically formed structure, as claimed. (*Id*.)

414. A POSITA would have a reasonable expectation of success of implementing such a modification, which would have involved application of known deposition techniques such as metal damascene, consistent with Chang's teachings. (EX1007 (Chang), ¶97.) For example, Chang teaches a damascene technique for its metal one layer formation, which was conventionally known to be able to effectively accommodate different vertical geometries of trenches and vias (for example, using a dual-damascene process. (EX1007 (Chang), ¶97; EX1008, ¶17; EX1016, ¶89; EX1015, 55-56; EX1014, 674-76 (cited for state of art

teachings/knowledge here). A POSITA would have understood that such modification would have predictably yielded Chang's Figures 24-27 structure including the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure as claimed in claim 5.

415. As to **claim 4**, as discussed above (§IX.E.1.g incorporated herein), Chang teaches **a plurality of first contacts** formed by parts of the self-aligned contacts 1670, 1671, and 1675 that reside in ILD 1503 (**disposed in the first dielectric layer**). A POSITA would have understood that forming the gate contacts extending into the second dielectric layer, as Chang teaches (see above; EX1007 (Chang), ¶105), a POSITA would have been motivated to also form source/drain contacts extending into the second dielectric layer in the modified Chang structure discussed above because doing so would allow a single deposition process to be used to form the gate contacts and source/drain contacts simultaneously. Accordingly, the processes for forming the source/drain contacts and gate contacts would therefore share same lithography process, etching processes, and/or deposition processes, which would have reduced process complexity and fabrication cost, and would have predictably led to the above modifications to structure discussed above. (*Id*.)

2. Claim 6

416. Chang discloses/suggests these limitations.

417. As discussed with respect to element [1.f], Chang teaches a "diffusion region" (or "PMOS region") 1600, which is **disposed on** silicon substrate 1598 (**the substrate**) for the same reasons the first dielectric layer is disposed on the substrate in element [1.c]. (EX1007 (Chang), ¶¶110-112; §§IX.E.1.c, IX.E.1.f (incorporated herein).)

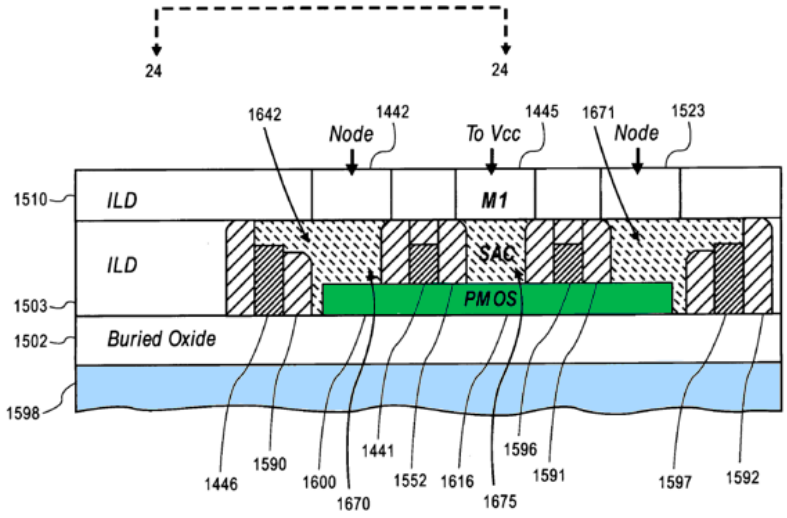


FIG. 27

418. As discussed in element [1.f], this diffusion region would have been implemented as a diffusion area 704 in Figure 20. *See* [1.f], which is incorporated by reference.

419. A POSITA would have understood this diffusion region would have been implemented as a diffusion area 704.

420. With respect to Figure 5, Chang further explains that "transistor structure 116 includes diffusion layer 104 (also called diffusion body 104 or **fin 104**)." A POSITA would have understood that diffusion area 704 could be "also called" a fin, which **compris[es] at least one fin structure**.

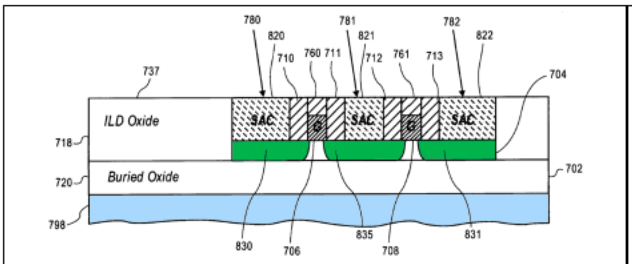


FIG. 20

Chang, Figure 20

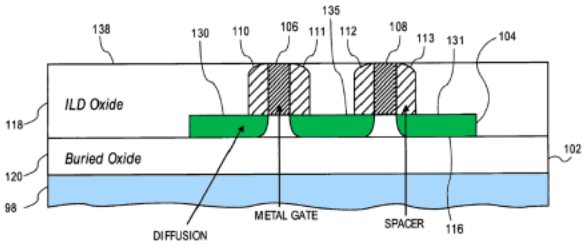


FIG. 5

Chang, Figure 5

(EX1007 (Chang), ¶48.)

421. Nonetheless, in addition to Chang's Figure 24-27 embodiment disclosing **at least one fin structure disposed on the substrate** as claimed, a POSITA would have been motivated to configure Figure 27's structure to include at least one such **fin structure** in view of Chang's teachings relating to Figure 5, which similar to Figure 27 shows a "cross section of... a transistor structure." (EX1007 (Chang), ¶¶45-46.)

422. Like Figure 24-27 embodiment, Chang's Figure 5 discloses a "transistor structure" with a "metal gate" and a "diffusion layer." (EX1007 (Chang), ¶45.) Chang also explains, in reference to Figure 5, that the "diffusion layer" is "also called" a "fin." (*Id.*)

423. Chang's Figure 5 "transistor structure" has a "metal gate" and "diffusion layer," which is "also called" a "fin." (EX1007 (Chang), ¶45.) Given the similar teachings in the same disclosure, a POSITA would have been motivated to modify Chang's Figure 27 structure with **at least one fin structure disposed on the substrate**, as recited in claim 6. A POSITA would have a reasonable expectation of success of implementing such a modification, which would have involved application of known transistor structures/techniques, consistent with Chang's teachings. (*Id*.)

424. In addition, Chang states that "[a]lternative embodiments of [Chang's] invention can be used with other types of transistors with metal gates, such as **trigate transistors**." (*Id*., ¶¶114, 2-6, 13-15, FIGS. 1-3.)

425. Chang recognizes that "[t]rigate transistors... **typically have small geometries**. For trigate transistors, the diffusion regions and the gates are typically quite thin" and that "[a] device such as a static random-access memory ("SRAM") uses numerous trigate transistors." (EX1007 (Chang), ¶¶ 2, 6.)

426. Tri-gate FETs were prevalent and mature technology, were conventionally known to include fin structures, and had known benefits to a POSITA. (*See* my discussions on this specific point in §IX.B.1 (referenced only for purposes of my opinions regarding the state of art knowledge of a POSITA)).

427. Accordingly, a POSITA would have been motivated to implement such a modification, and would have reasonably expected such an implementation to be successful. In my opinion, a POSITA would have understood that implement the modification discussed above would have involved the application of known transistor structures that were well within the capabilities and knowledge of a POSITA at the time, consistent with the teachings of Chang. In my opinion, a POSITA would have understood upon considering and implementing such knowledge, known techniques, and teachings in the prior art references, such a modification would have yielded the foreseeable result of the Figure 27 structure having **at least one fin structure disposed on the substrate**, like that recited in claim 6.

G. Ground 7: Chang in View of Huang Discloses and/or Suggests Claims 3 and 8-9

1. Claim 3

428. In my opinion, Chang in view of Huang discloses and/or suggests these limitations.

429. As explained for Ground 6, claim 1 (§IX.E.1, incorporated herein), Chang teaches **metal gates**, for example, Chang's gates 1441, 1443, 1446, 1596, and 1597 are shown in the annotated Figures 24 and 27 below:

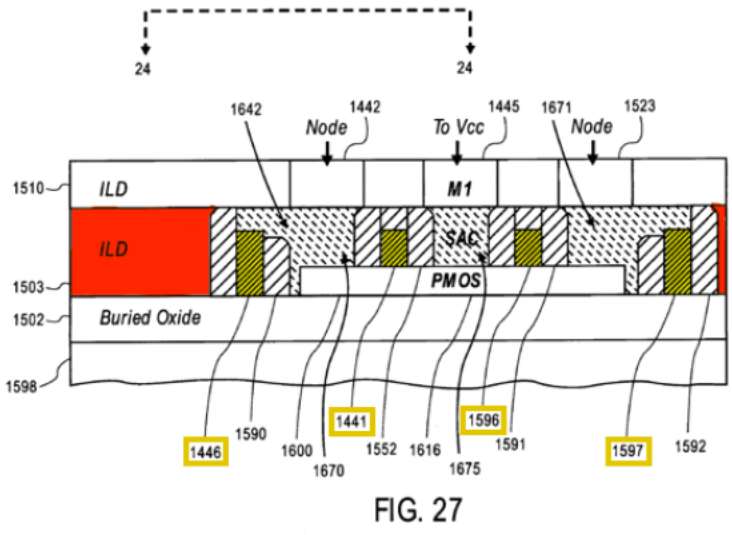


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶¶112, 108, 114, 47, 111, FIG. 24.)

430. Chang's gates include a "silicon nitride protection layer" (EX1007 (Chang), ¶114), which is a known "etch-stop layer for self-aligned contact application." (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 164-65, FIG. 5.64.)

431. Notwithstanding Chang's disclosures, it is my opinion that a POSITA would have been motivated to implement in Chang's structure **an etching stop layer having a truncated top surface and disposed on two sides of the metal gate**, in view of Huang's teachings.

432. A POSITA would have had reasons to consider Huang in context of Chang given they each disclose features relating to semiconductor devices/structures and/or parts thereof. Thus, a POSITA had reasons to consider the teachings of Huang when considering the structure and related features disclosed by Chang.

433. For instance, a POSITA would have recognized that Huang discloses the use of a conventional Contact Etch Stop Layer (CESL) 36, which is a dielectric material and acts as "an etch stop layer" (**an etching stop layer**), and is disposed on both sides of gate dielectric 24 and gate electrode 26 (**an etching stop layer disposed on two sides of the metal gate**).

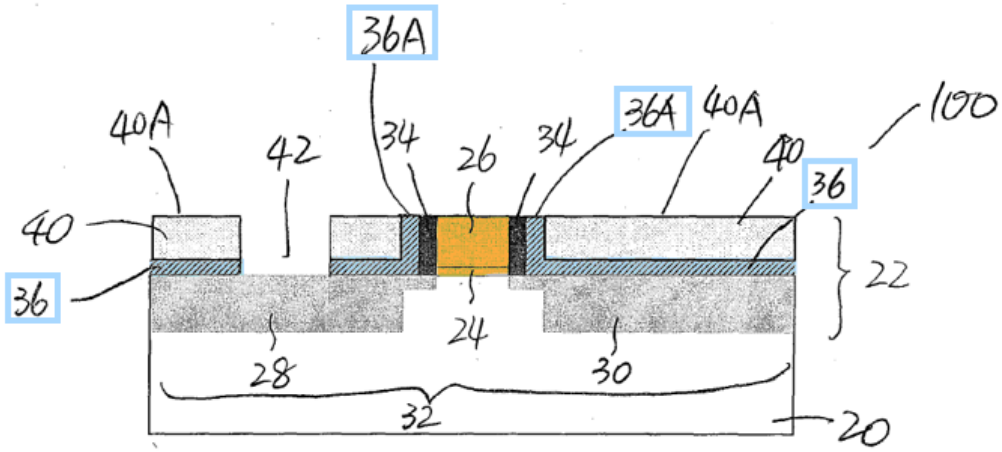


Fig. 1

(EX1008, ¶¶ 8-10, 14.)

434. As shown in Figure 6, the CESL is an etch stop layer to protect a source/drain regions (30) against etching of opening (56). (EX1008, ¶14, FIG. 6.)

435. As Huang explains:

> Referring to FIG. 6, a further etching is performed, so that opening 54 extends through CESL 50. As a result, contact plug 48 is exposed through opening 54. **Opening 56 also extends down through CESL 50, and ILD 40 may be etched. In some embodiments, the etching uses CESL 36 as an etch stop layer, Accordingly, CESL 36 is exposed**

through opening 56. Opening 56 may slightly extend into CESL 36 due to the over-etching.

(EX1008, ¶14, FIG. 6.)

436. Annotated Figure 6 below shows CESL acting as an etch stop layer to protect a source/drain regions (30) against etching of opening (56).

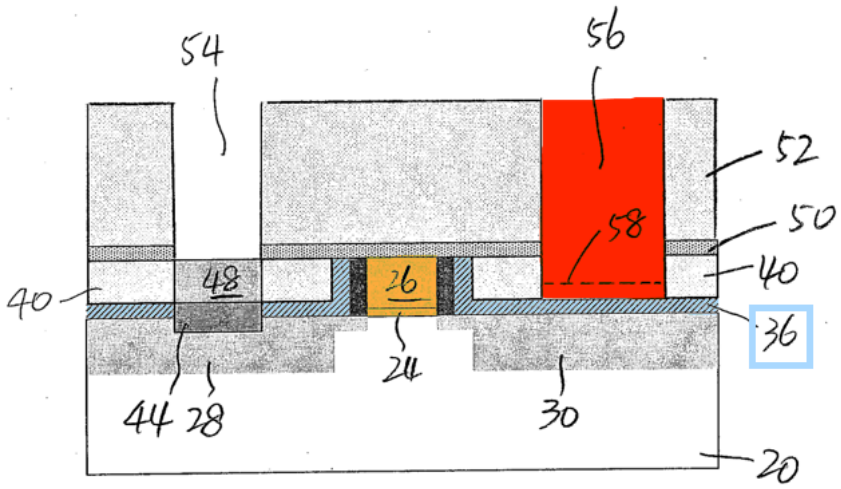


Fig. 6

"truncated top surface"

437. Huang's device shown in Figure 1 has a planarized top surface due to the "gate last approach," which conventionally involves a planarization by two CMP processes of the top surface of the structure, including top edges 36A of CESL 36 (**a truncated top surface**).

438. A POSITA would have understood that well before the relevant time of the '747 patent, it was conventional that an etch stop layer would be planarized during a gate-last process like that disclosed by Huang.

439. As an initial matter, for the gate-replacement/gate-last process, a POSITA understood that a CMP process is required in order to "open up" the dummy gate for removal, as shown in Figure 12:49 below:

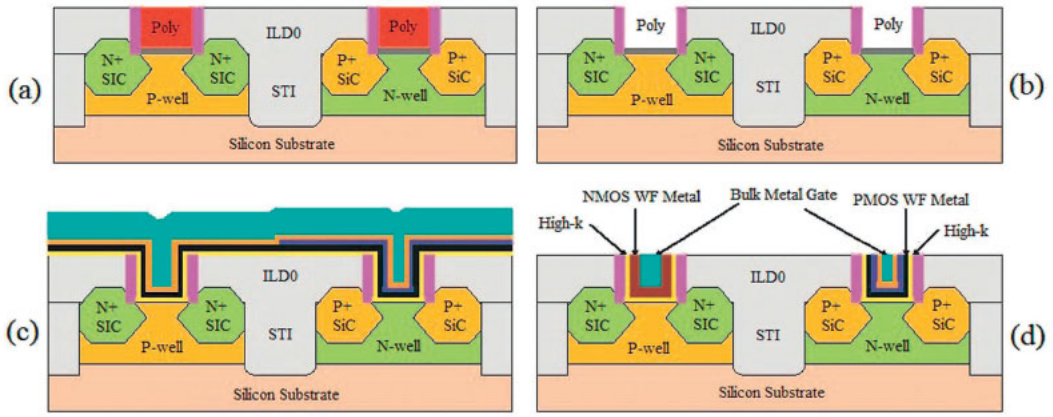


Figure 12.49 Gate-last HKMG processes: (a) ILD0 CMP or poly-open CMP, (b) polysilicon dummy gate removal, (c) high-κ and metal layer deposition, and (d) metal CMP to form HKMG MOSFETs.

(EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 544-45.)

440. EX1018 ("Chi") is another example, and further shows truncation of the etch stop layer during the CMP to open up the gates for replacement. Chi's "FIGS. 3A-3J depict various specific methods disclosed herein for forming self-aligned contacts for an integrated circuit product wherein a 'gate-last' or a replacement metal gate technique (RMG) is employed." (EX1018, 13:63-66.)

441. Figure 3A of Chi shows the initial formation of etch stop layer 34, which is previously described in the process of Figure 2:

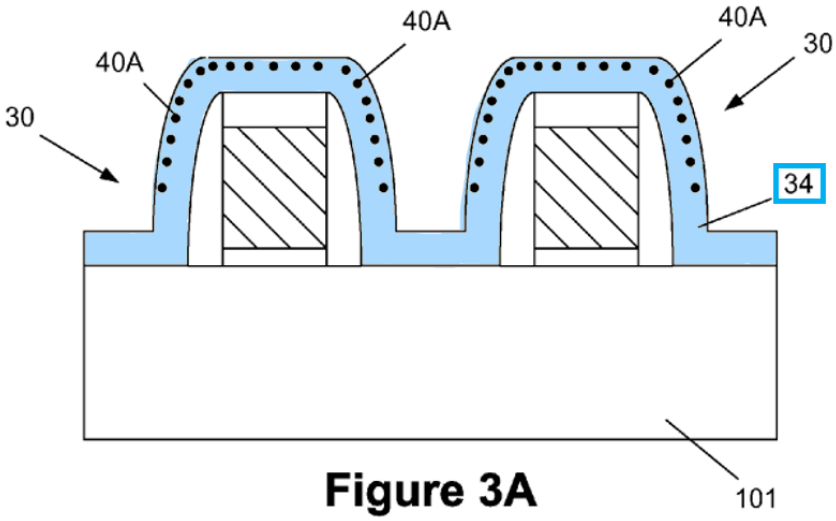


Figure 3A

(EX1018, 13:66-14:9.)

442. Afterwards, "as shown in FIG. 3C one or more CMP processes are performed to remove portions of the layer of insulating material 70, the etch stop layer 34 and the gate cap layer 31. The process results in the exposure of the gate structure 30 (more specifically the gate electrode 30B) for further processing."

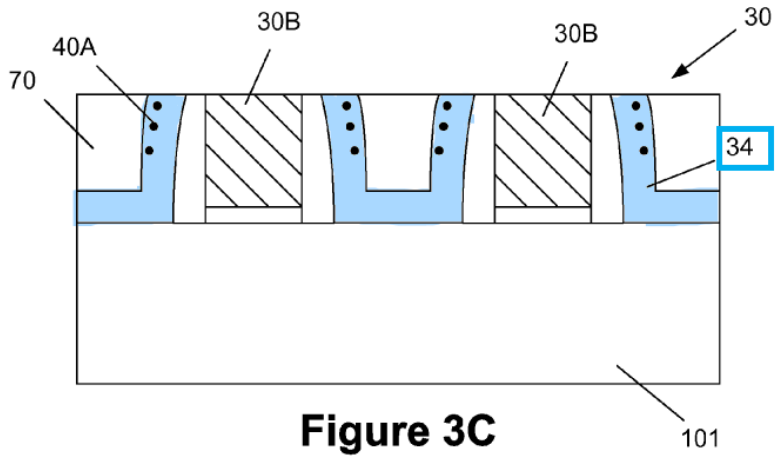


Figure 3C

(EX1018, 14:20-24.)

443. In the remaining steps of Figure 3, in particular Figures 3D through 3F, Chi then describes performing the gate replacement process (i.e., replacing the dummy gates with the permanent gates). (EX1018, 14:25-15:9.)

444. Similar conventional process are shown in EX1021 (Baars) (see Figures 2H-2J and layer 221) and EX1022 (Griebenow) at 16:30-47.

445. While Chang describes metal gates, and discusses replacement processes, it does not provide detail on how to implement such process, and a POSITA would have looked to the art on how to implement such processes.

446. As Huang explicitly acknowledges, as a result of the gate-last approach "the top surface of gate electrode 26 is level with top surface 40A of ILD 40 and top edges 36A of CESL 36." (EX1008, ¶9.)

447. In light of such knowledge in context of Huang's teachings, it is my opinion that a POSITA would have had motivation to implement features consistent with Huang's CESL 36 in Chang's structure. CESLs were well-known in the art at the time of the alleged invention, and a POSITA would have recognized numerous advantages in so implementing such layers. For example, to protect transistor gate structures, source/drain regions). (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 341-45, 164-65.)

448. A POSITA understood that well before the time of the alleged invention, it was well-known and conventional to use CESLs to protect gate structures and source drain regions. A number of state of the art references confirm such an understanding. (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 341-45.)

449. For example, Chi (EX1018) states that an effective etch stop layer is "highly resistant to the etch chemistry," which prevents an etch process (performed on the inter layer dielectric) from "expos[ing] the source/drain region" and ensures "the integrity of the gate encapsulation is not jeopardized" in the etch process. (EX1018, 2:16-31.) Chang seeks to protect transistors features (EX1007 (Chang), ¶114), a POSITA would have been motivated to look to ways to provide such protection, like that taught by Huang. These advantages of using CESLs would have been readily apparent to a POSITA.

450. As an example of ensuring integrity of the gate encapsulation, Introduction to Semiconductor Manufacturing Technology, which explains that a "Nitride liner" (i.e., silicon nitride layer) can "serve as an etch-stop layer for self-aligned contact application, as shown in Fig. 5.46." (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), pp. 164-65.) As shown in the Figure, the Nitride liner protects the gate structure during etching to form openings for self-aligned contact, which was a "common" use of silicon nitride.

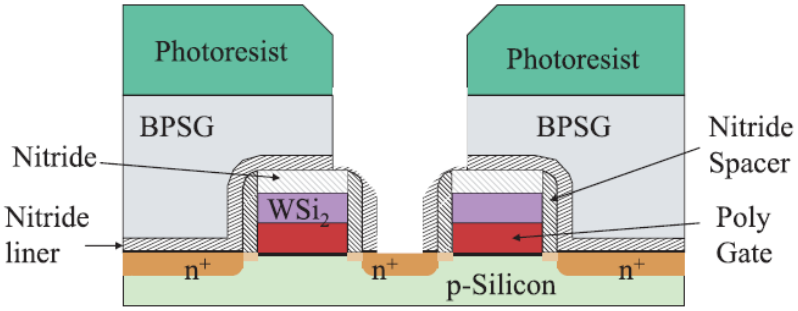


Figure 5.46 Silicon nitride sidewall spacer and self-aligned contact etch stop.

(*Id.*)

451. Accordingly, a POSITA considering semiconductor structures taught by Chang would have been motivated to look to teachings in the art for options in ways to protect its gates and source/drain regions.

452. Huang is an example of such relevant teachings that a POSITA would have considered. Huang teaches the CESL described above, and further explains that it will act as an etch stop layer to protect source/drain region 30 against etching of opening 54. (EX1008, ¶14, FIG. 6.)

453. A POSITA would have been motivated to modify Chang's structure with an etching stop layer having a truncated top surface and disposed on two sides of Chang's metal gate to provide the protective benefits of etch stop layers consistent with that taught by Huang and known in the art, for example, as discussed above.

454. A POSITA would have understood implementing features consistent with Huang's CESL 36 with Chang's structure would have predictably resulted in such a CESL being **disposed on two sides of** Chang's gates 1441 and 1596 (**the metal gate**) and would have had a truncated top surface as a result of the truncation process taught by Huang. A POSITA would have had a reasonable expectation of success in implementing such features given it would have involved known processes/techniques predictably resulting in features providing such desired protection (for example, CESL layers). (*Id.*)

455. In addition to the CMP process discussed above, a POSITA would have further understood that the proposed combination of Chang with Huang would have had a truncated top surface because Huang teaches to provide the spacer and etch stop layer to have the same top surface. (EX1008, ¶9, FIG. 1.) Accordingly, in the combined structure of Chang and Huang, the etch stop layer would have a truncated top surface as a result of the truncation process discussed in IX.E.1.e (regarding "the spacer has a truncated top surface"), which is herein incorporated by reference.

456. A POSITA would have had the rationale to implement such etching stop layer features in Chang's Figure 24-27 structure and would have had a reasonable expectation that the implementation and modification would have been successful. In fact, a POSITA would have understood and appreciated the above-described modification would have leveraged known processes to achieve CESL layers, and their protective characteristics. Such knowledge and expectations, coupled with the teachings of Huang in context of Chang's disclosures, which provides gates and source/drain regions (*see* my citations/analysis above for claim 1-Chang) that would be degraded by over etching, would have led a POSITA to consider and implement the above-discussed modifications to Chang's Figure 24-27 structure to provide such protection.

457. It is my opinion that a POSITA would have had reasons to consider Huang in context of Chang given they both disclose features relating to semiconductor structures and methods of forming such structures and/or parts thereof. Given such disclosures, it is my opinion that a POSITA would have been motivated to combine the teachings of Chang with those of Huang to provide the protective benefits of etch stop layers discussed above.

458. A POSITA would have been motivated to implement, and had a reasonable expectation of success of implementing, such etch stop features in Chang's Figure 24-27 structure. For example, the implementation to achieve CESL

layers were known in the art well before the alleged invention of the '747 patent, as demonstrated by the state of art teachings that I discuss above (*see section* regarding Exhibits EX1018, EX1020 (*Introduction to Semiconductor Manufacturing Technology*)). A POSITA would have readily appreciated the possibility of using a CESL, as disclosed by Huang. Chang provides source drain regions (*see* my discussions above in § IX.E.1.f) and gate structures (*see* § IX.E.1.d) that require protection from over etching.

459. Notwithstanding Chang's disclosure, a POSITA would have had motivation to modify Chang's Figure 24-27 structure to provide a CESL to provide protection from overetching.

460. A POSITA would have appreciated that such a modification would have involved applying known technologies/techniques (*e.g.*, CESL layer along the sides of gates and on top of source drain regions) to a known device/structure (Chang's Figures 24-27 embodiment with gates and source drain regions) and thus would have had the motivation and reasonable expectation of success in implementing such a modification to Chang. Considering and implementing such knowledge, techniques, and teachings would have yielded the predictable result of providing etch protection to a known device/structure (Chang's Figures 24-27 structure with gates and source/drain regions) by providing an etching stop layer

disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface in such structure.

2. Claims 8-9

461. Chang-Huang discloses/suggests these limitations.

462. Chang-Huang discloses/suggests the limitations of claim 3. (§IX.G.1 incorporated herein.) Chang-Huang discloses/suggests the further limitations recited in claim 8 based on the teachings of (1) Chang alone; and/or (2) Chang and Huang, and the further limitations recited in claim 9 based on the teachings of Chang and Huang.

463. As discussed, Chang teaches **first and second contacts**. (EX1007 (Chang), ¶¶112-13; §§IX.E.1.g-h (incorporated herein).)

464. *Chang:* Chang teaches metal one (M1) layer 1510 including **a plurality of** metal lines (**third contacts**) that "resides immediately above layer 1503" (**disposed on parts of the first contacts and on parts of the second contacts**) and provides contact to the self-aligned contacts and gates. (EX1007 (Chang), ¶¶112-13, 97-99, 106.) Each metal "line" or "contact" is a unitary metal structure formed from a single metal deposition, meaning **each third contact is a monolithically formed structure**. (*Id*.) For example, the metal lines/contacts may be formed by "a metal damanscene [sic] process" where a "deposited" "metal layer" "fills opening[s]" that were etched according to the desired structure of the

lines/contacts. (*Id*.) Such features would have been included in the Chang-Huang structure discussed above for claim 3 in §IX.G.1.

465. *Chang in view of Huang*: in addition to Chang-Huang disclosing/suggesting the further limitations recited in claim 8 based on the teachings of Chang alone, it also does based on the teachings of Chang and Huang. Chang does not explicitly disclose higher-level metal layers beyond metal (1) layer, a POSITA would have been motivated to implement such features in Chang in view of Huang resulting in third contacts disposed on parts of the first contacts and on parts of the second contacts of Chang's structure, where each third contact is a monolithically formed structure.

466. As I discussed in Ground 4, it was known to provide a damascene process, such as a dual-damascene process, to create metal lines and/or vias to connect to the contact level of the semiconductor structure, and a POSITA would have recognized numerous advantages in doing so. (*See* my discussions regarding this point above in §IX.D (*e.g.,* referring to EX1014 and EX1015), which I reference here only for purposes of the state of art knowledge of such features to a POSITA at the time).

467. Well before the time of the alleged invention, it was well-known and conventional to repeat the described dual-damascene process to provide higher level metal layers, with the number of layers depending on the particular application.

468. As I discuss, the advantages and necessity of implementing multiple metal layer levels and vias would have been readily apparent to a POSITA, who would have recognized that a single metal layer would be insufficient to handle the complexity of ICs comprising small geometry transistors.

469. A number of state of the art references confirm such an understanding.

470. For example, repeating the described dual-damascene process to provide higher level metal layers was known as basic textbook, conventional back-end of the line (BEoL) processing. For example, as discussed in *Introduction to Semiconductor Manufacturing Technology* (EX1020), back-end of the line (BEoL) processes conventionally provided numerous metal layers comprising vias and trench/trace structures:

> "In the **back-end of the line (BEoL) process**, all photolithography processes are followed by etch processes. **In copper metallization, this dual damascene process is repeated multiple times, depending on how many metal layers there are**: dielectric CVD, photolithography, dielectric etch, photoresist strip and clean, photolithography, dielectric etch, photoresist strip and clean, deposition of metal layers, metal anneal, and CMP. After all of the metal layers are formed, CVD silicon oxide and silicon nitride are deposited as the passivation layer, and the last photolithography process defines the pads for wire bonding or bump formation. After that, the chips are tested, die sawed, sorted, packaged, burned-in, and shipped to customers."

(EX1020, p. 19.)

471. Fig. 13.30 and other figures illustrate a via-first dual damascene copper low-k interconnection process for an M2 metal layer and M1 via over an M1 metal layer

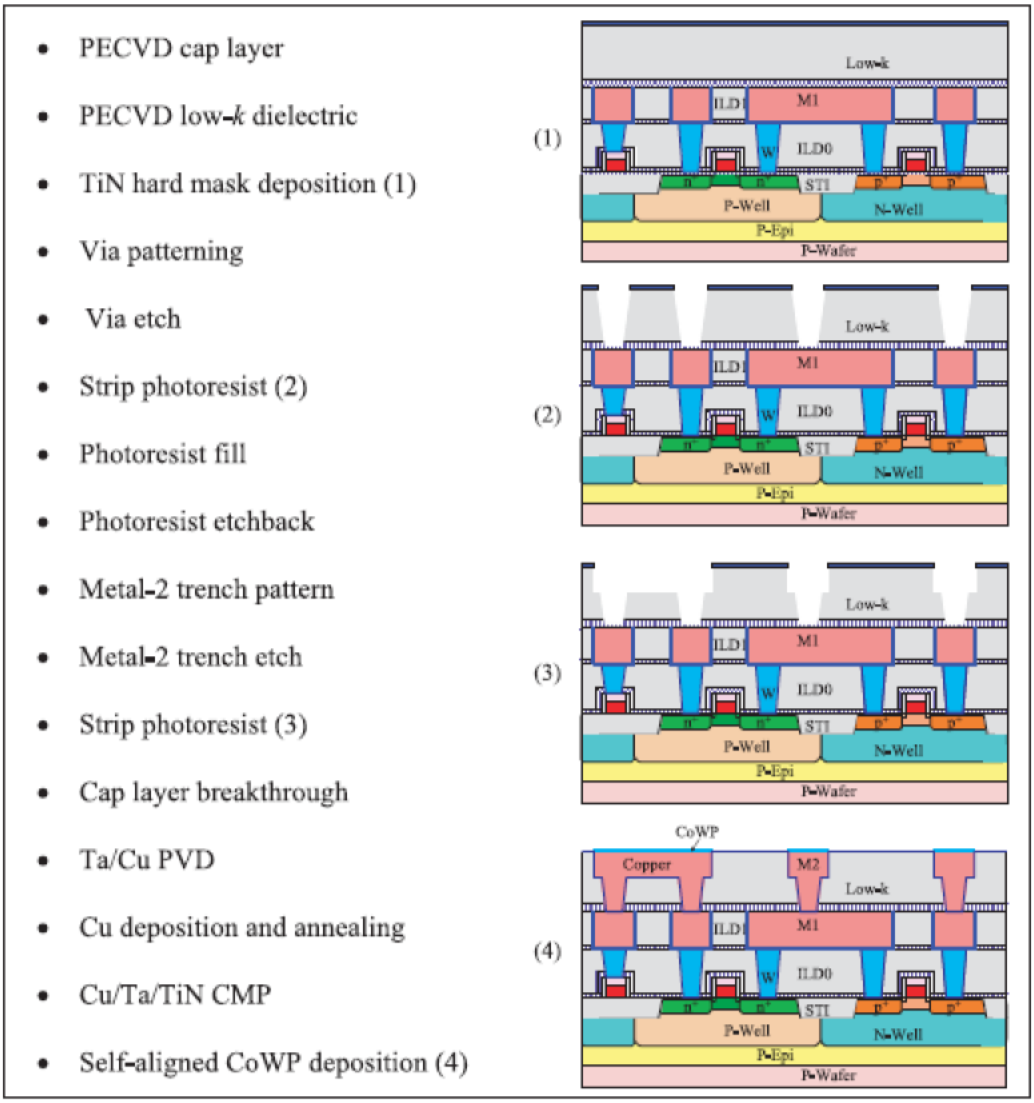


Figure 13.30 Via-first copper interconnection processing steps.

EX1020, Figure 13.30

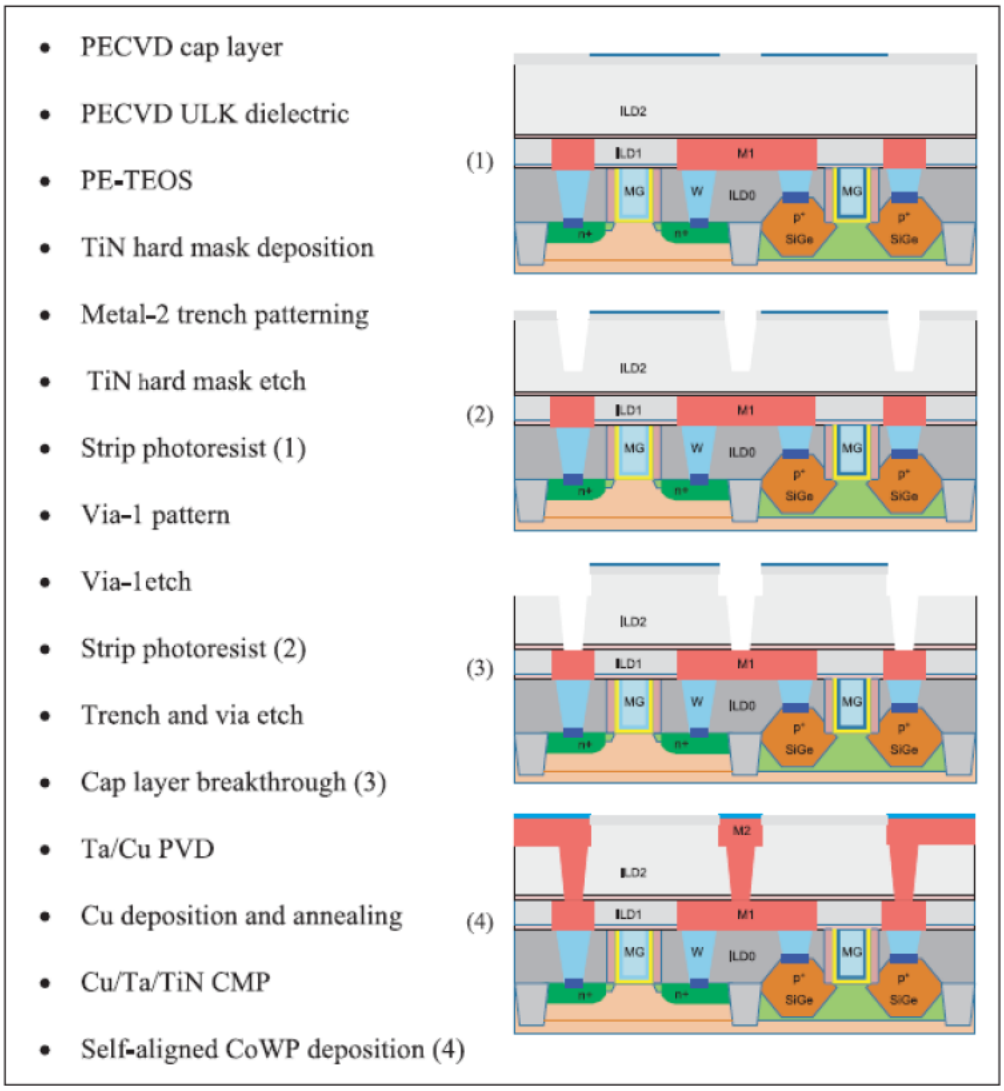


Figure 13.31 Copper/ULK interconnection with trench-first integration.

EX1020, Figure 13.31

Via 1 Metal 2 (Trench-First)

- Deposition of ILD stack (via etch stop, low-*k*, trench etch stop, low-*k*, and cap layers) (1)
- Photoresist coating
- Mask 12, metal trench 2 (2)
- Development
- After-development inspection
- Etch trench, stop on TESL
- Strip photoresist
- After-etch inspection (3)
- Photoresist coating
- Mask 13, Via 1 (4)
- Development
- After-development inspection
- Via-1 etch
- Strip photoresist
- After-etch inspection (5)
- Ar sputtering clean
- Ta barrier layer PVD
- Cu seed layer PVD
- Bulk Cuelectrochemical plating
- Copper annealing
- Cu and Ta CMP (6)
- Post-CMP clean
- Metal-2 probe

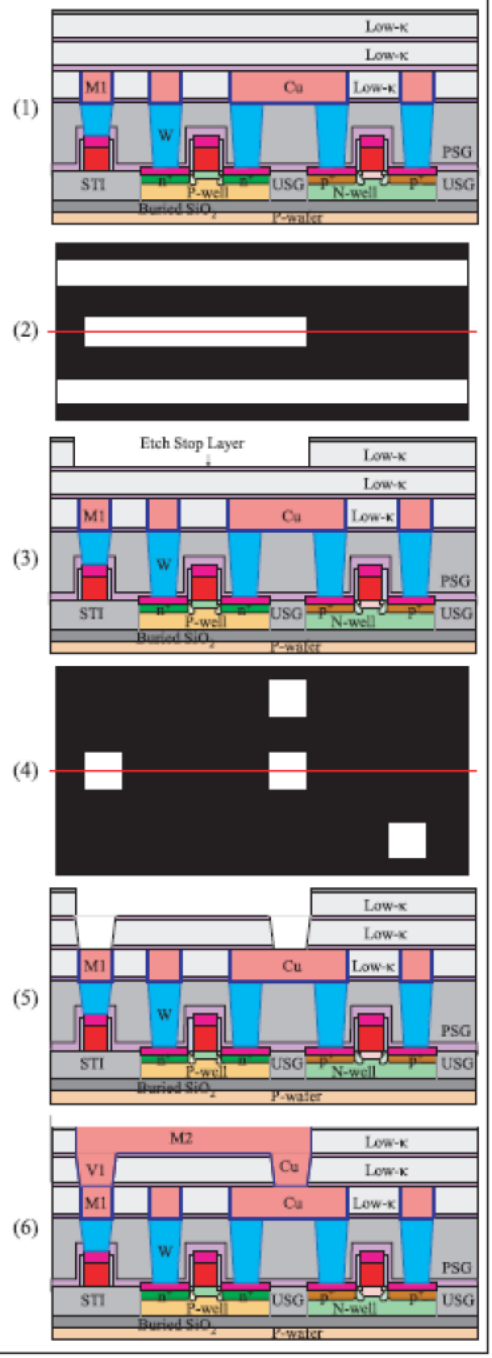


Figure 14.17 Trench-first dual damascene copper metallization.

EX1020, Figure 14.17

Via 2 and Metal 3 (Buried Hard Mask)

- Via ESL deposition
- Low-*k* dielectric deposition
- Trench ESL deposition (1)
- Photoresist coating
- Mask 14, via 2
- Development
- After-development inspection
- Etch hard mask on trench ESL
- Strip photoresist (2)
- Low-*k* deposition
- Cap layer deposition
- Photoresist coating
- Mask 15, metal trench 3 (3)
- Development
- After-development inspection
- Dielectric etch
- Strip photoresist (4)
- Ar sputtering clean
- Ta/Cu PVD
- Cuelectrochemical plating
- Cu annealing
- Cu and Ta CMP (5)
- Post-CMP clean
- Metal-3 probe

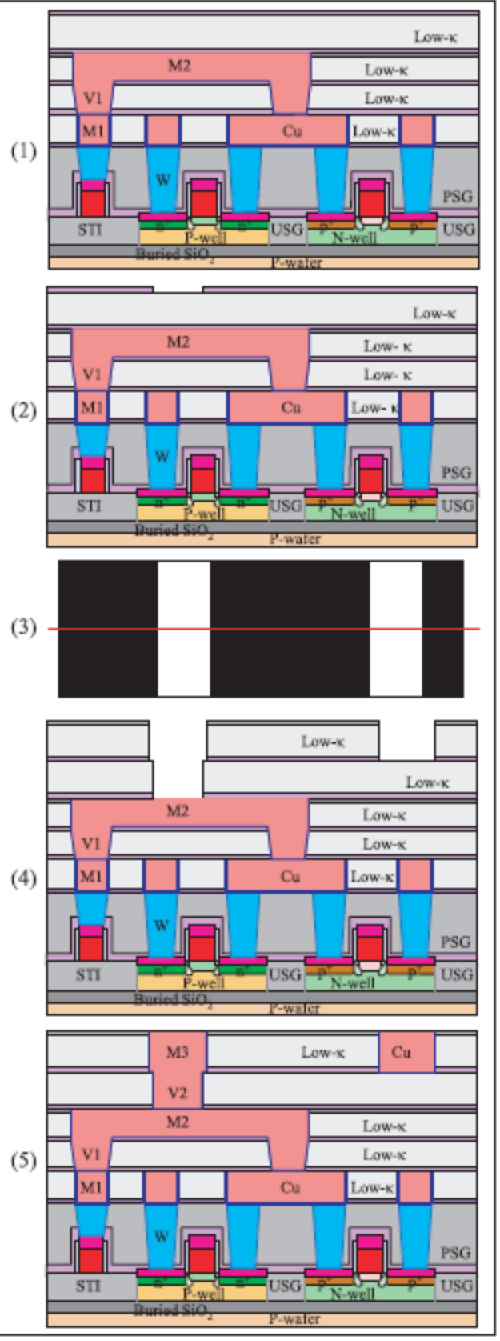


Figure 14.18 Buried-hard-mask copper metallization.

EX1020, Figure 14.18

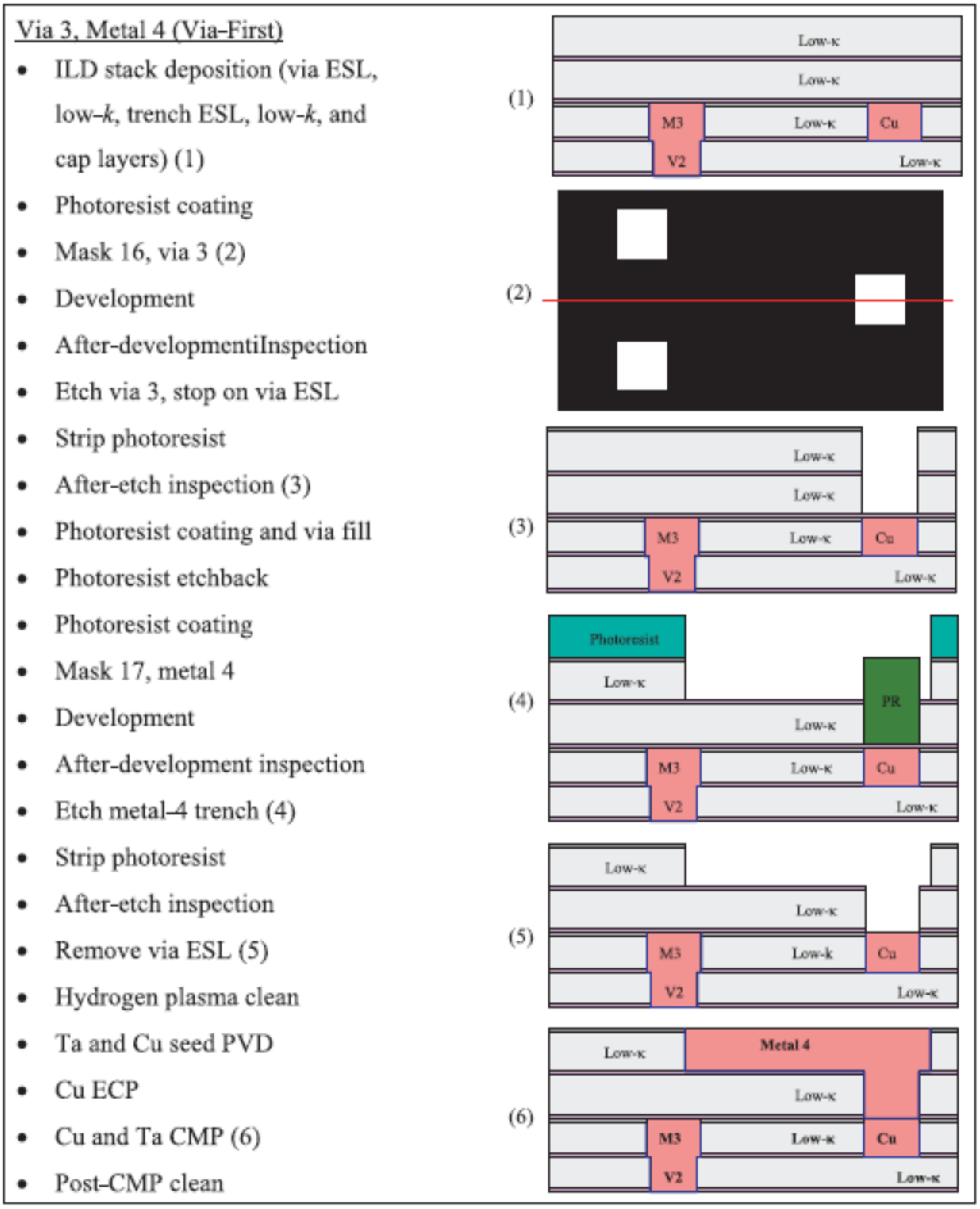


Figure 14.19 Via-first copper interconnection process.

EX1020, Figure 14.19

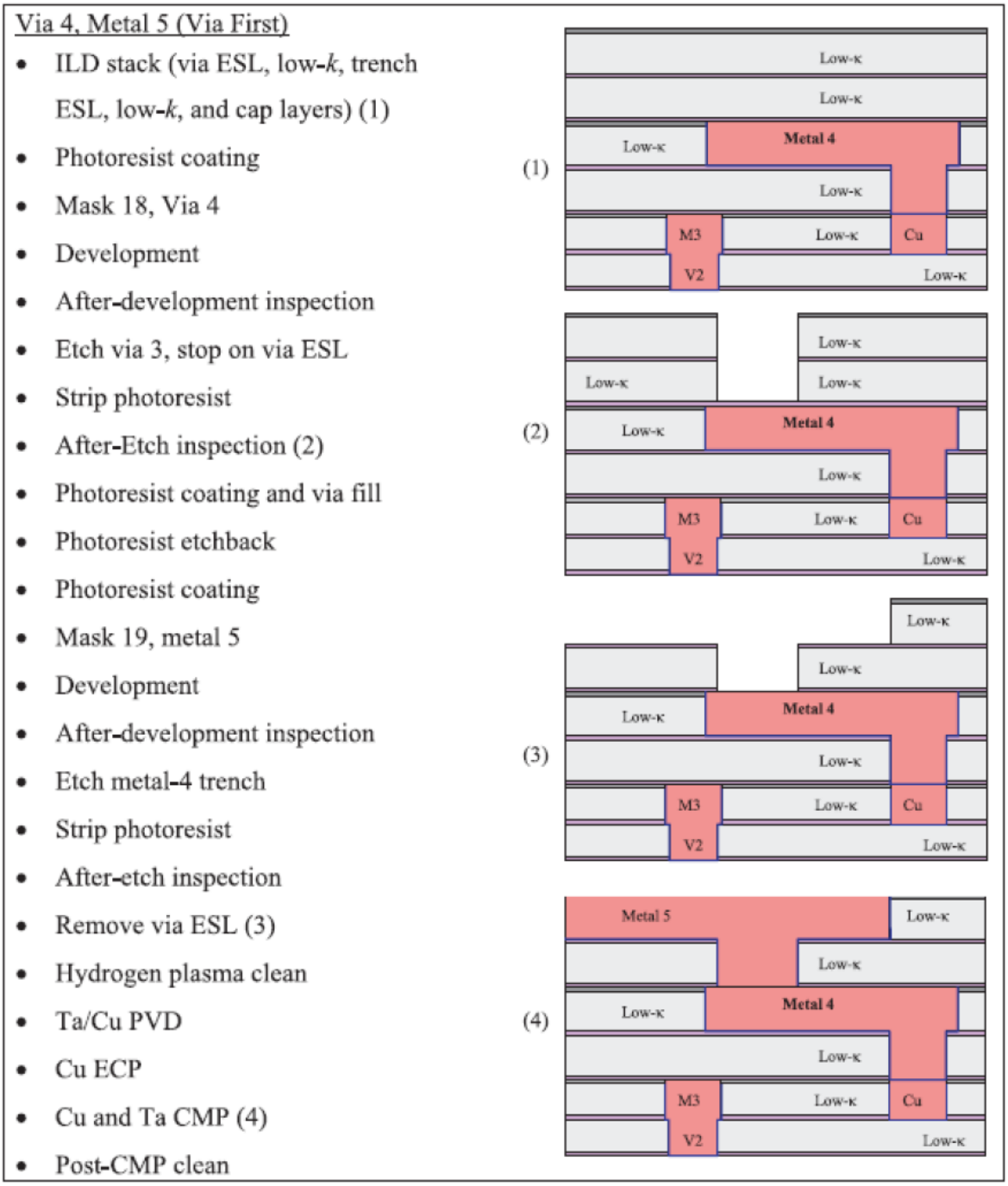


Figure 14.20 Via-first copper interconnection process.

EX1020, Figure 14.20

(EX1020, pp. 574-78, 611-14.)

"Copper interconnection technology is relatively new. After intensive research and development, IC chips with copper interconnections came to production in limited quantities for the first time in 1999. **Copper interconnections have been applied to IC chips with minimum feature sizes smaller than 0.18 µm. They have been used in logic IC chip fabrication since the 0.13-µm technology node and have also been applied in memory chip manufacturing. Because the dual damascene process simplified the interconnection process by reducing the number of steps, the cost of copper interconnections became lower than that of traditional tungsten/aluminum-copper alloy interconnections**. **Copper interconnections have become mainstream in advanced IC chip fabrication. By combining SOI substrate and copper/low-k interconnections, fabs can manufacture faster, more powerful, and more reliable IC chips with higher noise resistance and lower power consumption. Figure 14.22 shows a cross section of a CMOS IC with SOI substrate and copper/low-k dielectric interconnections**."

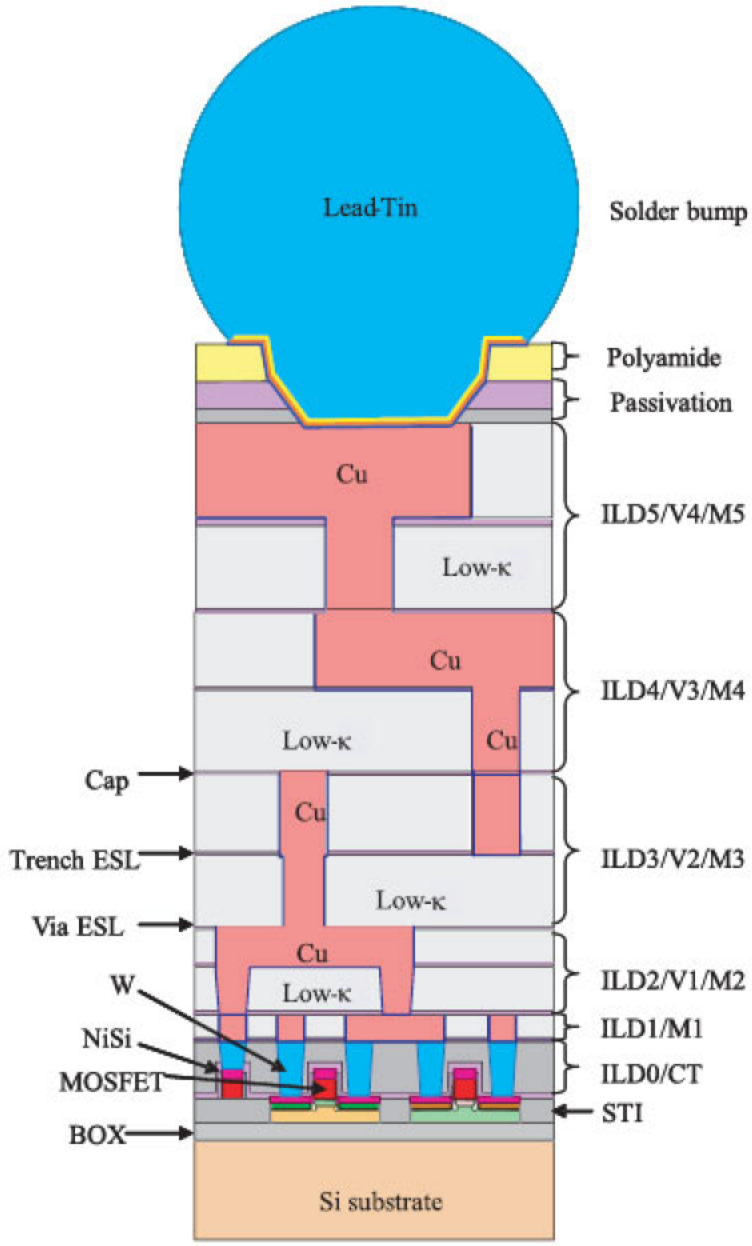


Figure 14.22 CMOS IC with SOI substrate and Cu/low-κ interconnections.

EX1020, Figure 14.22

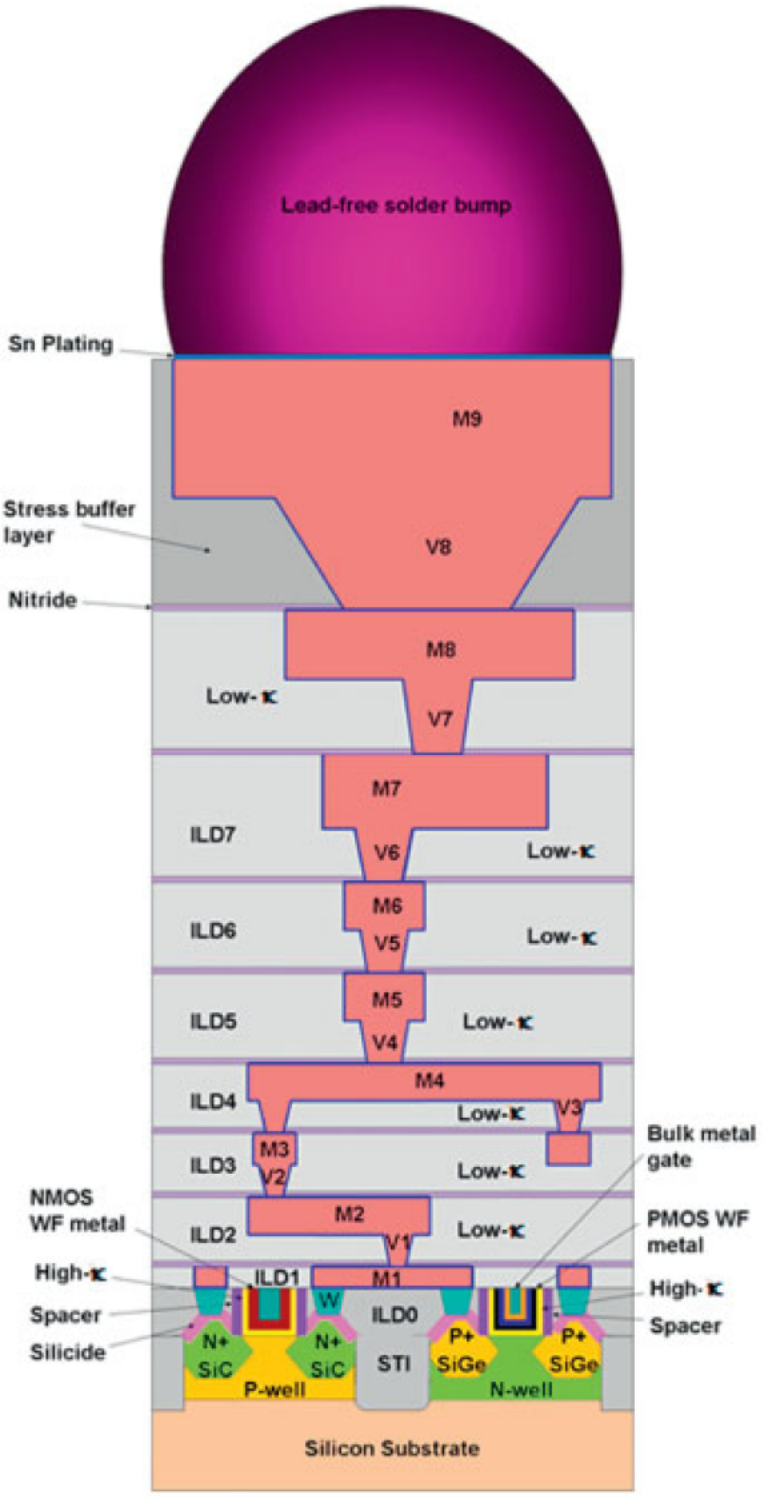


Figure 14.23 Cross section of a CMOS with HKMG, SMT, SEG SiGe S/D, copper/ultralow-κ interconnections, and lead-free solder bump.

EX1020, Figure 14.23

(EX1020, pp. 616-18)

472. As another example, after describing the dual-damascene process, Wolf states that the "sequence is repeated for the next level of metal" (*i.e.*, M2, M3...), as shown below. (EX1014, pp. 696-98).

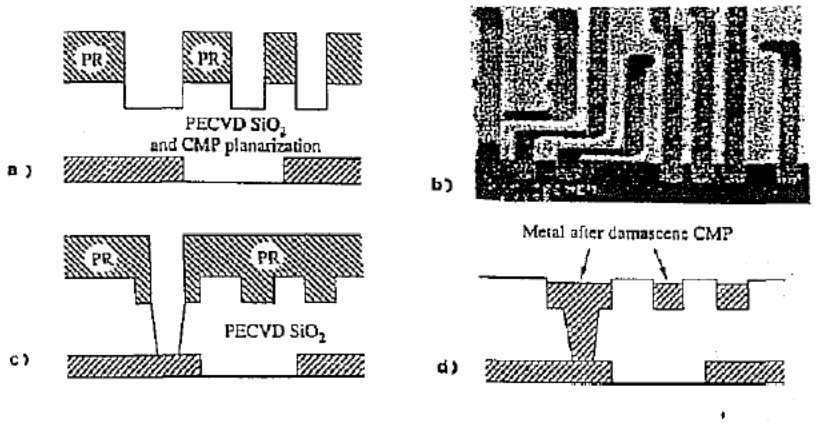


Fig. 15-3 *Dual-Damascene* process: (a) IMD is deposited by CVD and planarized by CMP. Trench is defined by PR #1 and then etched; (b) SEM of the etched trench after PR #1 has been stripped; (c) Vias are defined by PR #2 and then etched, using PR #2 to protect other regions of the IMD from etching; (d) Metal is deposited to simultaneously fill trenches and vias. CMP is used to remove excess metal. The sequence is repeated for the next level of metal.

Wolf, Figure 15-3

473. As another example, Tomimatsu explains that BEOL processes generally begins with the M1 layer, and "four-layer embedded wiring" (i.e., up to M4) or "ten-layer embedded wiring" (i.e., up to M10) may be utilized. (EX1016, ¶89.) Ning further explains how such multiple wirings are created. In Figure 3A below, Ning shows an example utilizing M1-M4 metal layers ("(e.g., via 1, via 2, via 3, M2, M3, M4)")

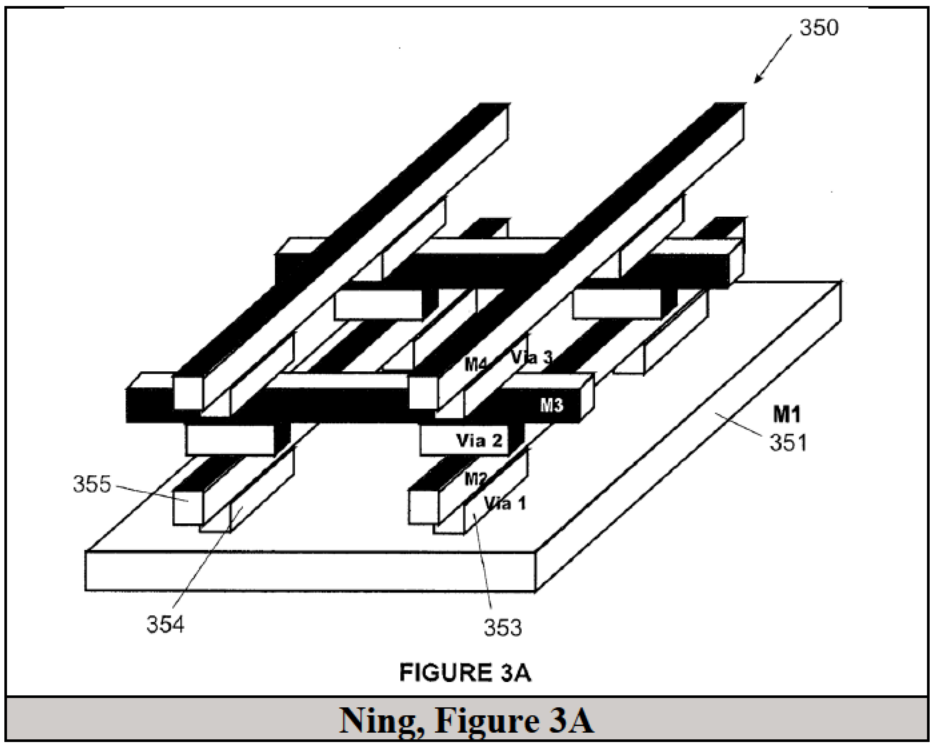


FIGURE 3A

Ning, Figure 3A

(EX1017, ¶¶37-40, FIG. 3A.)

474. As Ning explains, following M1 formation "via 1 and M2 are formed using dual damascene processes," and "repeated for via 2 and M3, and repeated again using via 3 and M4." (EX1017, ¶40.)

475. The advantages, and in fact necessity, of using multiple metal layers would have been readily apparent to a POSITA. EX1020 (*Introduction to Semiconductor Manufacturing Technology*, p. 508) ("After the 1980s, more than two metal layers were required to connect the increasing number of transistors in IC chips.") By the time of the alleged invention, "multiple metal layers with dielectric material in between are required to route millions or billions of transistors" for given integrated circuit, and a POSITA would have recognized that a single metal layer

would be insufficient to handle this complexity. (EX1020 (*Introduction to Semiconductor Manufacturing Technology*), p. 570.)

476. See also p. 573, "When the number of transistors increased, one layer of metal interconnections could not route all of the transistors on the chip; thus, multilayer metal interconnections began to be used."

477. Accordingly, a POSITA would have recognized advantages in providing a dual-damascene process to create metal lines and vias to connect to a structure's contact level, and a POSITA considering semiconductor structure taught by Chang would have been motivated to look to teachings in the art for options in ways to provide multiple metal layers.

478. Huang is an example of such relevant teachings that a POSITA would have considered. Huang (EX1008) teaches metal layer M1 metal lines 74 and M0 vias 72, as shown in annotated Figure 8A below, and further explains that "[i]n subsequent process steps, **more metal layers (not shown) may be formed over metal layer M1**."

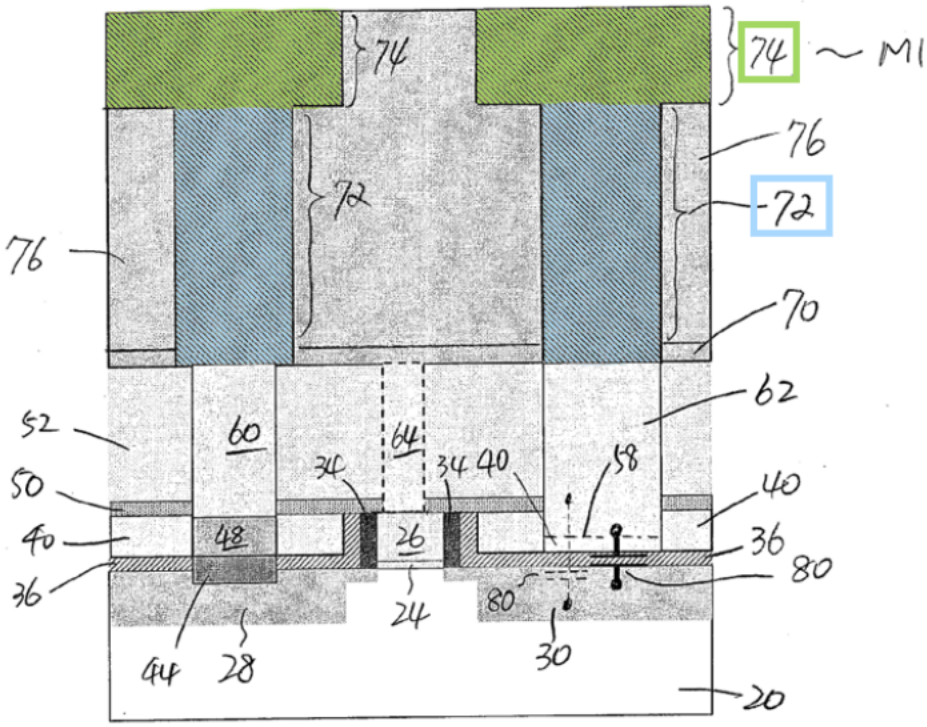


Fig. 8A

Huang, Figure 8A

(EX1008, ¶17, FIG. 8A.)

479. Consistent with a POSITA's knowledge discussed above, a POSITA would have understood Huang's teaching of "more metal layers" "formed over metal layer M1" to mean metal lines 74 implemented in the M2 layer, and vias 72 implemented in the M1 layer (together, **a plurality of third contacts**).

480. Huang's teachings, in context of Chang's disclosures, would have been motivated a POSITA to configure Chang's structure such that a plurality of third contacts (consistent with Huang) were disposed on Chang's self-aligned contacts, whether disposed only in the ILD layer 1503 or in the ILD layer 1503 and the metal

one layer within the ILD 1510 layer (parts of the first contacts and on parts of the second contacts). (*See above* §§IX.E.1.g-h.) And given Chang teaches dual-damascene (*see above*), which is a single metal deposition, each such third contact in the modified structure would have been a monolithically formed structure like that claimed.

481. Thus, a POSITA would have had reasons to consider Huang in context of Chang given they each disclose features relating to semiconductor devices/structures and/or parts thereof. For example, Chang and Huang describe semiconductor structures with metal layers to contacts (*i.e.*, gate and source/drain contacts). (*See e.g.*, EX1007 (Chang), ¶¶112-13; EX1008, ¶17; EX1001, 5:31-6:37.) Thus, a POSITA would have had reasons to consult Huang when looking to implement a semiconductor structure like that discussed in Chang.

482. In considering Huang in context of Chang, a POSITA would have recognized Chang's disclosure regarding the M1 layer, and thus would have been motivated to combine the teachings of Chang with those of Huang to achieve multiple metal layers (e.g., at least metal lines M2 and vias M1) to form a more complex IC consistent with that known in the art at the time. Further, a POSITA would have been motivated to use a dual-damascene process to provide the M2 metal lines and M1 vias.

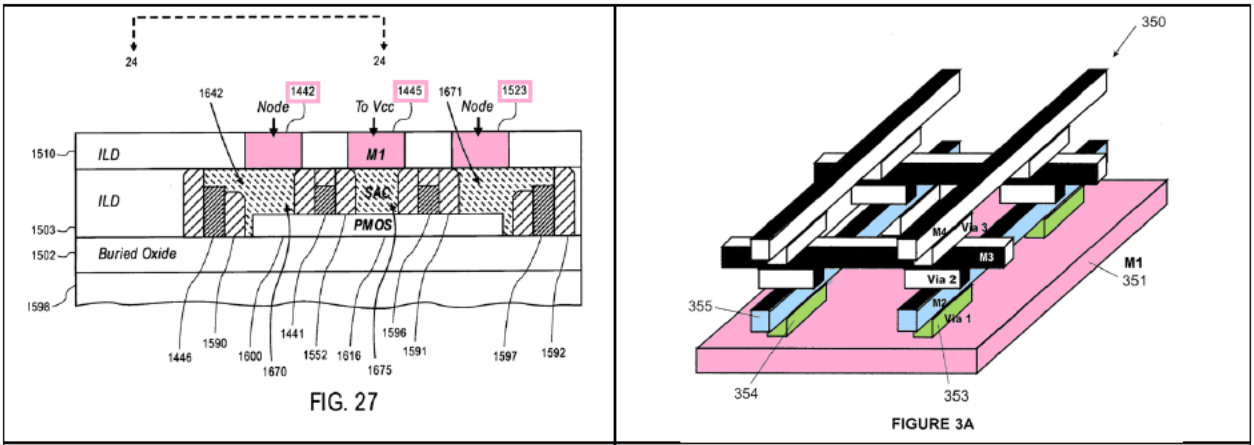
483. For example, in my opinion, a POSITA would have been motivated to implement a dual-damascene process of metal lines M2 and vias M1 in Chang's structure, and would have had a reasonable expectation that such implementation would have been successful. For example, the implementation to achieve a dual-damascene process to provide M2 metal lines and M1 vias was known in the art well before the alleged invention of the '747 patent, as demonstrated by the state of art teachings noted above (*see section* regarding Exhibits EX1014, EX1016, EX1017, EX1020). Implementation of the proposed combination would have merely involved selecting a suitable dual-damascene process.

484. A POSITA would have readily appreciated the possibility of using a dual-damascene process to provide M2 metal lines and M1 vias, as disclosed by Huang. Chang provides M1 metal lines, but does not provide any subsequent BEOL processing, and a POSITA would have understood that BEOL processing is critical to create a functioning semiconductor device.

485. Chang already recognizes its M1 layer is "formed by a metal damanscene [sic] process" (¶97), and a POSITA would have looked to damascene process to form its higher metal layers. Use of a dual-damascene process to provide M2 lines and M1 vias over M1 lines was known, and that BEOL processing (not described by Chang) was critical to create an IC. (*Id*.; EX1017, ¶¶37-40, FIG. 3A

(annotated below); EX1008, FIG. 27 (annotated below); EX1016, ¶89; EX1014, 696-98.)

486. As noted, a POSITA would have appreciated that the implementation of a dual-damascene process to provide M2 metal lines and M1 vias over M1 metal lines was known at the time, as were conventional methods to produce such implementations. (*See section* and *e.g.*, EX1017, ¶¶37-40, FIG. 3A; EX1016, ¶89; EX1014, pp. 696-98; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), p. 19, 574-78, 611-18.) For example, one such conventional method is shown by Ning:



Chang, Figure 27	Ning, Figure 3A

487. For example, as I mentioned above, such a dual-damascene process was known to a POSITA to generally involve the conventional step of a dual-damascene process to provide M2 metal lines and M1 vias (*Id.*; *see* my discussions on this point above in §IX.D (referenced only for state of art knowledge on this point at the time)

over an M1 metal line. A POSITA would have been able to readily apply the conventional methods of dual-damascene processes, such as those taught by Huang, to Chang with high predictability.

488. Accordingly, a POSITA would have been motivated to implement the modified Chang-Huang structure discussed for claim 3 to include M2 metal lines and M1 vias above Chang's M1 metal lines. A POSITA would have considered different dual-damascene processes to effectively add M2 metal lines and M1 vias to the structure shown in Chang Figures 24-27.

489. A POSITA would have appreciated that such a modification would have involved applying known technologies/techniques (dual-damascene process to provide M2 metal lines and M1 vias) to a known device/structure (Chang's Figures 24-27 structure with M1 metal lines) and thus would have had the motivation and reasonable expectation of success in implementing such a modification to Chang. Considering and implementing such knowledge, techniques, and teachings would have yielded the predictable result of providing M2 metal lines and M1 vias to a known device/structure (Chang's Figures 24-27 embodiment with M1 metal lines) with operability to the M2 metal layer and above.

490. The modification would have predictably yielded Chang's Figures 24-27 structure (*see* §IX.G.1) having third contacts (each a monolithically formed

structure) disposed on parts of the first contacts and on parts of the second contacts, like that claimed.

491. Although Chang uses different nomenclature ("M1") than Pethe ("M0") to refer to the lowest metal line/layer above its respective contact structure, both lines/layers (Chang's "M1"/Pethe's "M0") represent a metal line/layer above which additional metal lines/layers may be formed, as known in the art and taught by Huang. Thus, regardless of the label ("M0" (Pethe) or "M1" (Chang)), a POSITA would have been motivated to provide the formation of one or more metal line(s)/layer(s) and associated vias to the underlying metal line/layer for reasons respectively stated.

492. Moreover, using such a dual-damascene process to form M1 vias 72 and metal layer M2 metal lines 74 together in a single deposition in the above discussed Chang-Huang structure, would have likewise predictably resulted in M1 vias 72 and M2 layer metal lines 74 to form a plurality of contacts in the structure, where the vias and the metal lines comprise of the same material and contact each other directly (relevant to claim 9). EX1008, ¶17, FIG. 8A.

493. In the combined structure of Chang and Huang, M1 vias 72 (**a via hole structure**) and metal layer M2 metal lines 74 (**a trace structure**) form **a third contact**, as shown in annotated Figure 8A below.

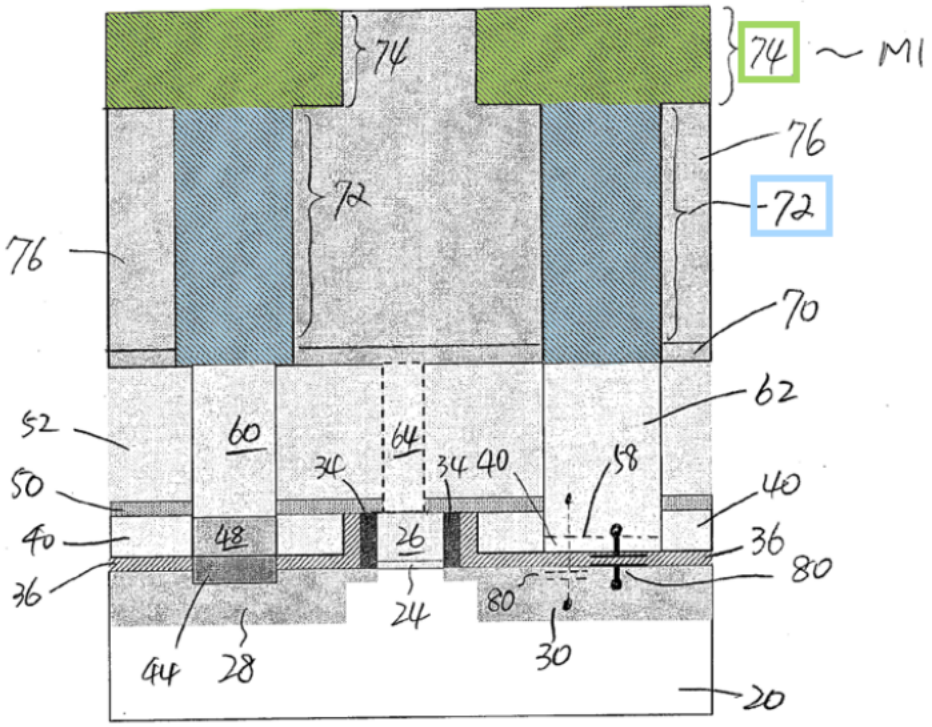


Fig. 8A

Huang, Figure 8A

(EX1008, ¶17, FIG. 8A.)

494. As discussed in claim 8, a dual-damascene process is used to form M1 vias 72 and metal layer M2 metal lines 74 together in a single deposition, meaning **the via hole structure and the trace structure comprise the same material and contact each other directly**. (EX1008, ¶17 ("no noticeable interfaces are formed between MO vias 72 and the respective overlying metal lines 74."), FIG. 8A.)

H. Ground 8: Chang in View of Hong Discloses and/or Suggests Claims 4-5

1. Claim 4

495. In my opinion, Chang in view of Hong discloses and/or suggests these limitations.

496. As discussed in §§IX.E.1.g and IX.E.2 (limitation [1.g] and claim 2), the identified parts of (as indicated in the annotated Figure 27 below) self-aligned contacts 1670 and 1671, and self-aligned contact 1675 (**first contacts**) are disposed in layer 1503 (**the first dielectric layer**), and each is a homogeneous metal fill layer is formed from a single metal deposition (see ¶¶93-94, FIGs. 19-20) and therefore is **a monolithically formed structure**. (See above §§IX.E.1.g, incorporated herein.)

497. Such features are shown annotated below:

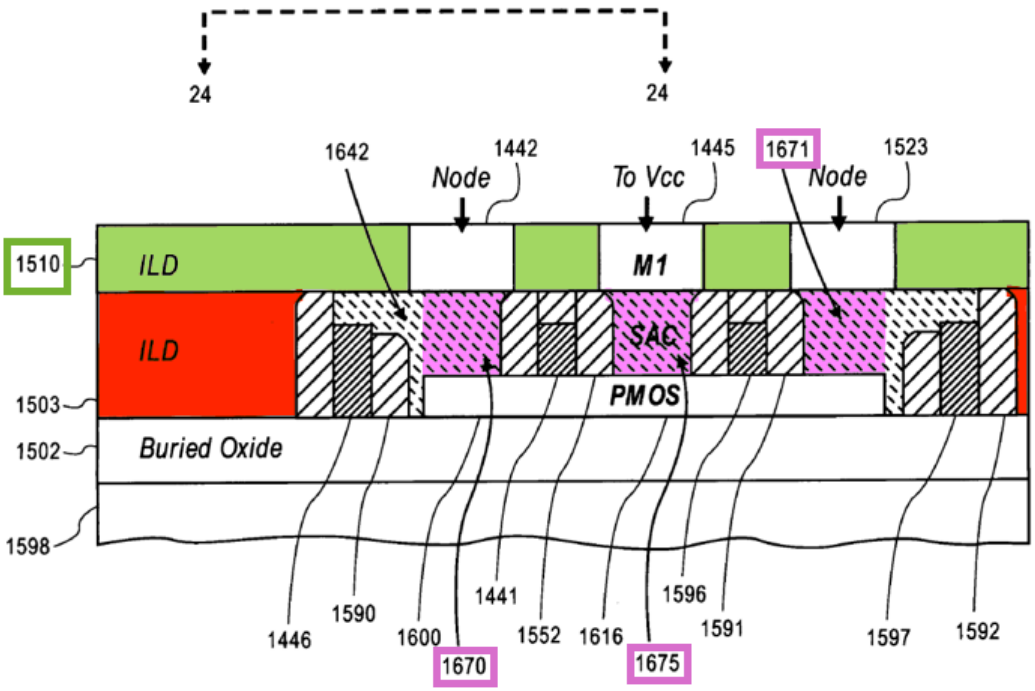


FIG. 27

(EX1007 (Chang), ¶¶113, 93-94, FIGs. 19-20.)

498. Notwithstanding Chang's disclosures, a POSITA would have had motivation to implement Chang's self-aligned contacts (**first contacts**) also **disposed in a second dielectric layer** based on Hong.

499. Hong discloses improved structures for electrically contacting semiconductor device features. (EX1010, Abstract, 2:13-58, 8:53-9:27, 10:46-67; *see also*, 2:4-10, 9:55-64, 11:1-9.) For example, Hong discloses a "share contact" for FETs that includes contact 442 formed simultaneously between a metal gate 411 and source/drain region 402, and within a plurality of dielectric layers (e.g., layer 406 on layer 401). *Id.*, 8:53-9:27, 10:46-67, FIGs. 7, 9.

500. In Hong, first contact layer 442 is formed in both a first dielectric layer 401 and a second dielectric layer 406. (EX1010, 8:54-9:27.) A third dielectric layer 409 (i.e., a capping layer) is formed on a second metal gate 421, as shown in annotated Figure 7 below.

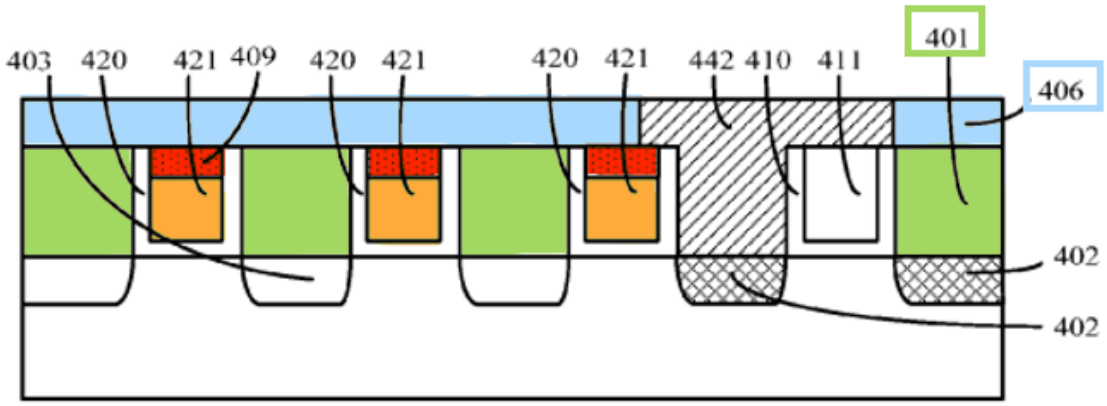


FIG. 7

501. A POSITA would have had reasons to consider Hong in context of Chang given they each disclose features relating to semiconductor devices/structures and/or parts thereof. For example, Hong, Chang, and the '747 patent are all concerned with forming contact areas over transistor structures. (*See e.g.*, EX1007 (Chang), ¶¶108-113; EX1010, 8:54-10:56; EX1001, 1:9-13, 5:66-6:37.) Thus, a POSITA would have had reasons to consult Hong when looking to implement a structure like that disclosed by Chang, including contact areas and related structures.

502. A POSITA would have been motivated to combine the teachings of Chang with those of Hong to provide a second dielectric layer beneath the metal (1)

layer of Chang. This modification of Chang would be implemented as shown below according to known techniques.

503. In my opinion, a POSITA would have been motivated to implement, and had a reasonable expectation of success of implementing, such a second dielectric layer beneath the metal (1) layer of Chang's structure.

504. For example, as previously discussed, a POSITA would have recognized that creating metal contacts typically involved depositing a metal fill layer, and polishing it back with a CMP process to remove it from outside the desired location of the contact. Hong recognizes that this CMP may damage the underlying transistor structures, and further recognizes that use of a second dielectric layer beneath the metal (1) layer protects the underlying transistor structures, resulting in "relatively less damage." (EX1010, 11:1-9, 9:55-64.) Ultimately, use of the second dielectric layer beneath the metal (1) layer will "aid to increase the stability of the transistor." (*Id*.)

505. Chang's metal (1) layer is fabricated the same way – by a "metal damanscene process" where a metal deposition "covers surface 965 and fills opening 940, 941, and 942" and then is "planarized by polishing" to remove the metal everywhere except the openings. (*See* EX1007 (Chang), ¶97.) A POSITA would have understood based on the teachings of Hong that Chang's transistor structures would be at risk of damage during such polishing, and therefore would have

recognized the benefits of Hong's second dielectric layer beneath the metal (1) layer to protect the underlying transistor structures.

506. As Hong notes, a POSITA would have also recognized the known problems caused by damage to the metal gate and spacers during the etching process to create the opening for first contact layer 442. Hong addresses this issue by providing "an etching selectivity" between the third dielectric layer 409 and the second dielectric layer 406. (EX1010, 8:54-9:27, 8:3-13, 7:43-54.)

507. As a result, the second gate dielectric layer 420 and the third dielectric layer 409 provide full protection to the second metal gate 421 during the etching process to create the opening for first contact layer 442. In other words, this solution addresses "[t]he problem of exposing the second metal gate 421 caused by technology errors during a process for exposing the first metal gate 411," "thus it may ensure the stability of the transistor." (EX1010, 8:54-64.)

508. Guided by such teachings, and by the knowledge in the art, a POSITA would have been motivated to form an additional dielectric layer (**a second dielectric layer**) in Chang beneath the metal (1) layer comprising ILD 1510, such that the identified self-aligned contacts (**first contacts**) are **disposed in** the **second dielectric layer**.

509. A POSITA would have been motivated to implement such a modification, and would have reasonably expected it to be successful. In fact, such

a skilled person would have appreciated that the above modification to Chang's structure would have involved the application of known semiconductor device structure and process technologies (i.e., dielectric deposition), including gate protection techniques for Chang's similar gate structures, that were well within the capabilities and knowledge of such a person at the time. Considering and implementing such knowledge, techniques, and teachings would have yielded the predictable and advantageous result of an enhanced protection of its gates during the etching processes to create the openings for self-aligned contacts.

510. The above motivation rationales discussed above for claim 4 would have been applicable to both Chang's structure discussed for claim 1 in §IX.E.1 and to the modified Chang structure discussed for claim 1 in §IX.E.3.

511. A POSITA would have understood that Hong's gate protection technique was applicable to Chang's gates, which have substantially the same structure and purpose. For example, both Chang and Hong have spacers provided on two sides of metal gates, a dielectric cap on the gates, and etching processes that form openings for contacts that risk damaging the gates. (EX1007 (Chang), ¶¶111-13, ¶¶93-94; EX1010, 8:53-9:45.) Implementing an additional dielectric layer with etch selectivity in such contexts were well known by those of ordinary skill at the time to have successfully worked before the time of the alleged invention, and it would have been well within the ability of a POSITA.

2. Claim 5

512. In my opinion, Chang in view of Hong discloses and/or suggests these limitations.

513. As discussed in §§IX.E.1.h and IX.E.2 (limitation [1.h] and claim 2), the identified parts of (as indicated in the annotated Figure 27 below) self-aligned contacts 1670 and 1671 (**second contacts**) are disposed in layer 1503 (**the first dielectric layer**), and each is a homogeneous metal fill layer formed from a single metal deposition (see ¶¶93-94, FIGs. 19-20) and therefore is **a monolithically formed structure**. (*Above* §§IX.E.1.h, IX.E.2, incorporated herein), as shown in annotated below:

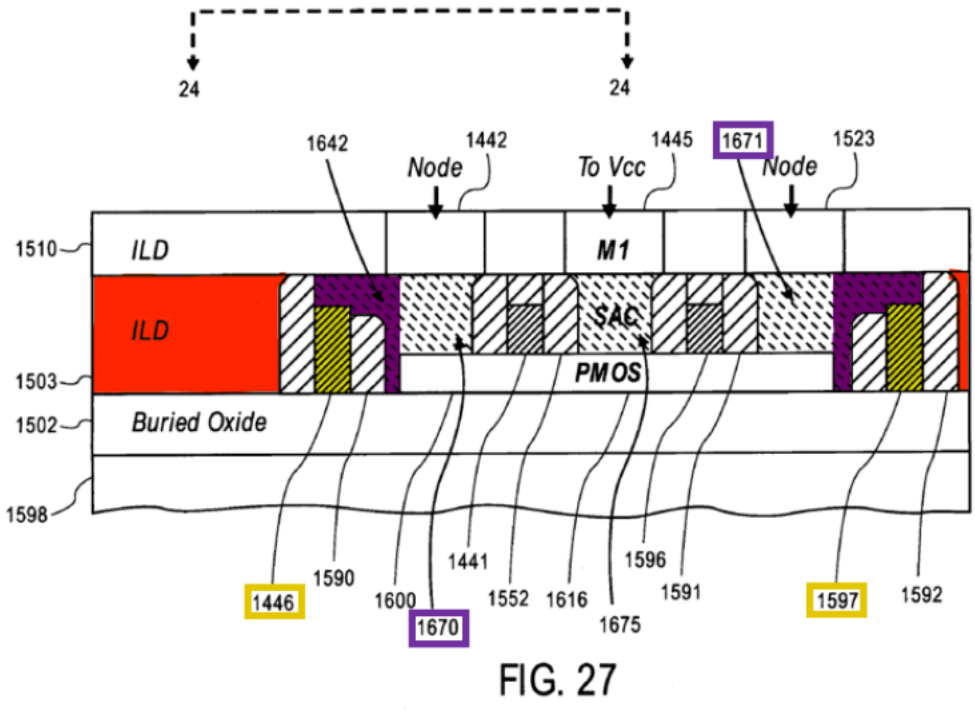


FIG. 27

Chang, Figure 27

(EX1007 (Chang), ¶¶112-13.)

514. Chang in view of Hong discloses this limitation for the same reasons as I explained in Ground 8, claim 4, which is incorporated herein by reference. (*See* § IX.H.1.)

515. Such features are consistent with the Chang's teachings in view of Hong as explained for claim 4. Thus, for similar reasons, a POSITA would have had the same motivation, rationale, and expectation of success to configure Chang's structure such that the second contacts disposed in the first dielectric layer and second dielectric layer and each second contact is a monolithically formed structure, as recited in claim 5. (Above, §IX.H.1 (incorporated herein).) The above motivation rationales discussed above for claim 5 would have been applicable to both Chang's structure discussed for claim 1 in §IX.E.1 and to the modified Chang structure discussed for claim 1 in §IX.E.3.

I. Ground 9: Chang in View of Bohr Discloses and/or Suggests Claim 7

1. Claim 7

516. In my opinion, Chang in view of Bohr discloses and/or suggests claim 7.

517. I discuss above how Chang discloses the limitations of claim 1. (*See* §IX.E.1.) Notwithstanding Chang's disclosures, a POSITA would have would have had reasons and motivation to implement in Chang's structure a self-aligned silicide

("salicide") layer disposed between each S/D region and each first contact in view of Bohr.

518. As previously discussed, it was known to include a salicide layer above a source/drain and/or below a contact, such as in a self-aligned trench contact. *See* EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 157-58; EX1013, 4:63-5:30 (semiconductor structure that "[o]ften" includes: "a layer of silicide material 212 is formed over the source and drain regions 206" and contacts 220 "on top of the silicide layer 212"), FIG. 2 (layer of silicide material 212 on top of source and drain regions 206).) A POSITA knew implementing a salicide layer between a source/drain and contact would advantageously create a more conductive contact and thus looked to likewise improve Chang's structure. (EX1013, 4:63-67, 3:56-58.)

519. Bohr teaches the use of a salicide layer between a source/drain and contact, which aligns and confirms these motivations. (EX1009, 12:61-13:10, FIGs. 8A-8B, 8C (annotated below).)

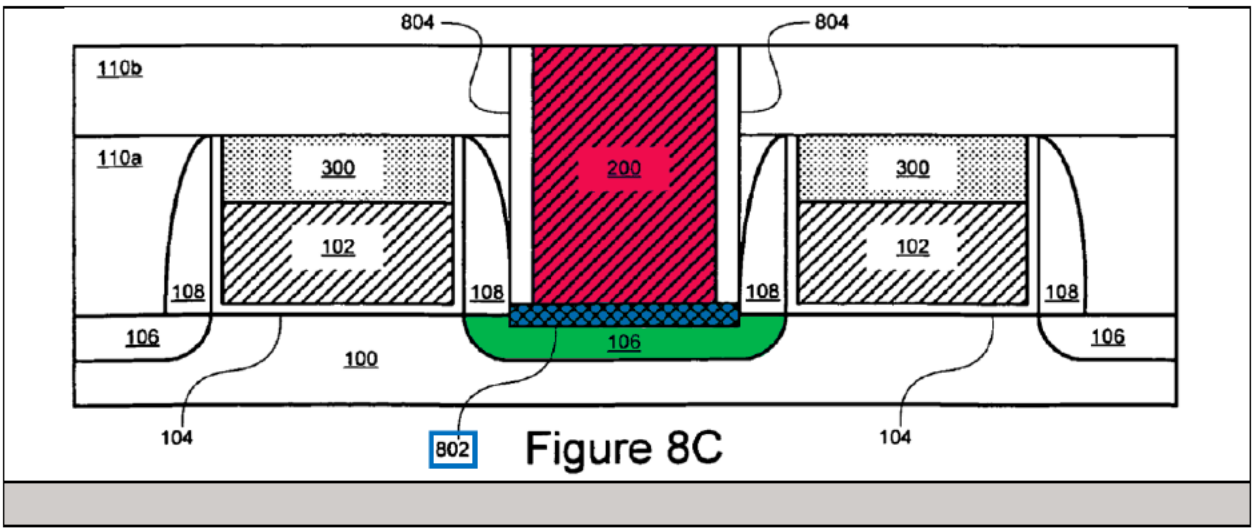


Figure 8C

(EX1009, FIG. 8A, 12:61-66.)

520. A POSITA would have understood that Bohr's silicide is a self-aligned silicide, and thus a salicide. (EX1009, 12:61-13:8.) Accordingly, Bohr teaches a salicide layer is disposed between a source/drain region and a trench contact.

521. A POSITA would have had reasons to consider Bohr in context of Chang given they each disclose features relating to semiconductor devices/structures and/or parts thereof (*See for example*, EX1007 (Chang), FIG. 27; EX1009, 12:61-14:3; *see also* EX1001, 1:9-13, 5:66-6:37.) Thus, a POSITA would have had good reason to look to Bohr when looking to implement a structure like that disclosed by Chang.

522. In light of Bohr's teachings, a POSITA would have been motivated to modify the Chang structure discussed above for claim 1 (§IX.E.1) to achieve a salicide layer disposed between its source/drain region and trench contact consistent with Bohr's teachings. (EX1009, 12:61-14:3, FIG. 8C.)

523. Bohr's teachings/guidance, in context of their state of art knowledge, would have motivated a POSITA to modify Chang's structure to achieve a salicide layer disposed between its source/drain region and trench contact consistent with Bohr's teachings. (EX1009, 12:61-14:3, FIG. 8C.) Such a rationale and resulting modification would have been applicable to both Chang's structure discussed for claim 1in §IX.E.1 and to the modified Chang structure discussed for claim 1 in §IX.E.3.

524. In my opinion, a POSITA would have been motivated to implement, and had a reasonable expectation of success of implementing, such features because such a skilled person would have understood that the use of a salicide layer was known well, as provided by Bohr and also known to those of ordinary skill in the art at the time. (Ex.1009, 12:61-13:10; EX1013, 4:63-5:30, 5:48-64, 9:5-30, 10:7-35.)

525. Knowing that implementing a salicide layer between a source/drain and contact would advantageously create a lower resistance contact, a POSITA would have had reason to look to likewise improve Chang's structure. (EX1013, 4:63-67, 3:56-58.) Thus, a POSITA would have considered Bohr's teachings when implementing a semiconductor structure/device like discussed in Chang. (EX1007 (Chang), FIG. 27; EX1009, 12:61-14:3.)

526. A POSITA would have been motivated to combine teachings of Chang (for example, contacts and source/drain regions,) and Bohr (for example, use of a

self-aligned silicide (i.e., salicide layer) disposed between a source/drain region and trench contact) to improve Chang's structure by for example, reducing the electrical resistance between the S/D region and self-aligned contacts 1670, 1671, and self-aligned contact 1675 (first contacts). (§§IX.E.1.f-IX.E.1.g.)

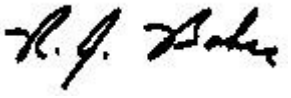
527. In fact, Bohr teaches advantages to implementing a salicide layer between a source/drain and contact (for example, to "reduce[] the electrical resistance between the later formed trench contact…and the diffusion region…"), which was consistent with a POSITA's knowledge. EX1009, 13:8-10; EX1013, 4:63-67, 3:56-58. Thus, a POSITA would have looked to achieve similar benefits by using a salicide layer between the S/D region and self-aligned contacts 1670, 1671, and self-aligned contact 1675 in Chang's structure.

528. A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Chang-Bohr combination. Bohr teaches the known advantages of using a salicide layer between a diffusion region and trench contact in a semiconductor structure similar to that contemplated by Chang. Ex.1009, 1:5-36, 4:5-11, 12:61-13:10; The combination of Chang and Bohr would have involved application of known technologies (for example, known use of salicide layers between source/drain regions and trench contacts) (*see for example*, EX1013, 4:63-5:30, 5:48-64, 9:5-30, 10:7-35; EX1020 (*Introduction to Semiconductor Manufacturing Technology*), 157-

58) according to known methods (for example, known deposition/annealing processes) to yield the predictable result of a semiconductor structure (Chang's Figure 24-27 structure) including a salicide layer disposed between the source/drain region and each self-aligned contacts 1670, 1671, 1675 ("**first contacts**") so the resistance between them can be reduced.

CONCLUSION

529. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: April 17, 2025 By: 

Dr. R. Jacob Baker