UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.

AND

APPLE INC.,

Petitioners

v.

MARLIN SEMICONDUCTOR LIMITED,
Patent Owner

IPR2025-00864

Patent No. 9,147,747

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,147,747

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EX1001	U.S. Patent No. 9,147,747
EX1002	Declaration of Dr. Jacob Baker
EX1003	Curriculum Vitae of Dr. Jacob Baker
EX1004	Prosecution History of U.S. Patent No. 9,147,747
EX1005	U.S. Patent No. 9,461,143 ("**Pethe**")
EX1006	PCT/US 2011/066989 ("**Golonzka**")
EX1007	U.S. Patent App. Pub. No. 2006/0223302 ("**Chang**")
EX1008	U.S. Patent App. Pub. No. 2013/0161707 ("**Huang**")
EX1009	U.S. Patent No. 8,436,404 ("**Bohr**")
EX1010	U.S. Patent No. 8,895,389 ("**Hong**")
EX1011	CN 2013 1 0006390 ("**Hong Foreign Priority**") and Certified Translation of Hong with Certification of Translation
EX1012	D. Neamen, *Semiconductor Physics and Devices – Basic Principles*, 4th Ed. (2011)
EX1013	U.S. Patent No. 8,258,057 ("**Kuhn**")
EX1014	Wolf, Stanley. *Silicon Processing for the VLSI Era: Deep-Submicron Process Technology*. Lattice Press, 2002 ("**Wolf**")
EX1015	May, Gary S., and Simon M. Sze. *Fundamentals of Semiconductor Fabrication*. John Wiley & Sons, 2004 ("**May**")
EX1016	U.S. Patent App. Pub. No. 2012/0252180 ("**Tomimatsu**")
EX1017	U.S. Patent App. Pub. 2008/0142975 ("**Ning**")
EX1018	U.S. Patent No. 8,741,723 ("**Chi**")
EX1019	U.S. Patent App. Pub. 2014/0048888 ("**Chen**")

EX1020	Xiao, H. (2012). *Introduction to Semiconductor Manufacturing Technology* (2nd ed.). Prentice Hall ("**Xiao**")
EX1021	U.S. Patent No. 8,835,245 ("**Baars**")
EX1022	U.S. Patent No. 8,455,314 ("**Griebenow**")
EX1023	**Sze**, S.M. *Physics of Semiconductor Devices*. 2nd ed., John Wiley & Sons, 1981 ("**Sze**")
EX1024	U.S. Patent App. Pub. No. 2009/0155991 ("**Lee**")
EX1025	U.S. Patent App. Pub. No. 2009/0014796 ("**Liaw**")
EX1026	Banerjee, G. and R. Rhoades, Chemical Mechanical Planarization, ECS Trans., 13 (4) 1-19 (2008)
EX1027	U.S. Patent No. 5,536,962 ("**Pfiester**")
EX1028	U.S. Patent No. 8,928,048 ("**Xie**")
EX1029	U.S. Patent No. 8,906,754 ("**Pham**")

I. RELIEF REQUESTED

Claims 1-9 should be canceled as unpatentable based on the following grounds:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A/1B	1-5, 8	102/103	Pethe
2	6,7	103	Pethe
3	7	103	Pethe + Bohr
4	8-9	103	Pethe + Huang
5A/5B	1-2	102/103	Chang
6	4-6	103	Chang
7	3, 8-9	103	Chang + Huang
8	4-5	103	Chang + Hong
9	7	103	Chang + Bohr

II. STATE OF THE ART

A. Field-Effect-Transistors (FETs)

The field-effect transistor (FET) has been the foundational device for very-large-scale integrated circuits (ICs) for decades. EX1023, 431. FETs (e.g., MOSFETs), function essentially as a switch controlled by voltage applied to a "gate" (G) between "source" (S) and "drain" (D) regions.

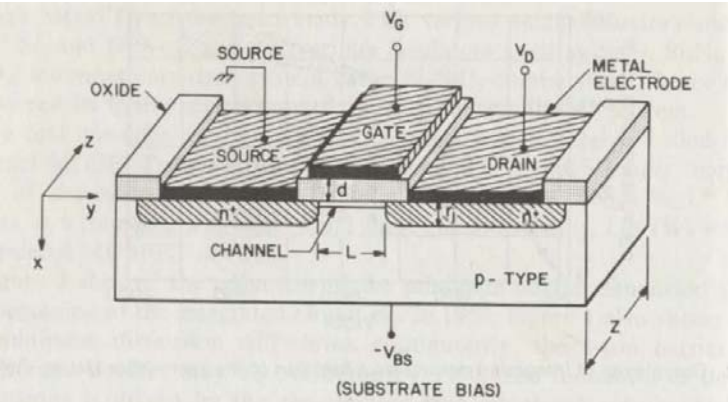


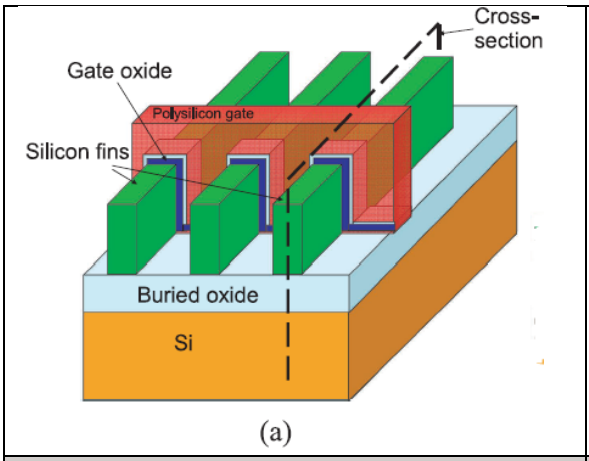
Fig. 3 Schematic diagram of a MOSFET. (After Kahng and Atalla, Ref. 4.)

EX1023, 433-34, Figs. 3, 6; EX1002, ¶¶27-30, 33-34.

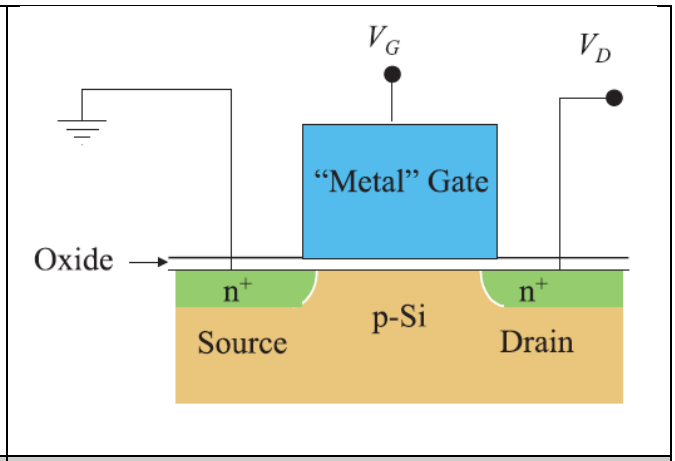
A FET has a channel disposed below the gate, and source and drain regions disposed to each side of the gate. *Id.* The "source" is the source of electrical carriers that flow along the channel during operation and the "drain" is the sink or drain where the electrical carriers flow during operation. A source or drain is commonly referred to as a "source/drain" because whether the element operates as a "source" or "drain" for electrical carriers is interchangeable depending on the voltage applied to the element. Source/drain regions were conventionally formed by diffusion of dopants, and in such instances, were commonly referred to as a diffusion regions. EX1002, ¶¶29-30, 33-34; EX1012, xxi-ii, xxii (step 6).

Two types of FETs were conventionally known at the time of the '747 patent's filing: (1) planar FETs (e.g., planar MOSFET); and (2) non-planar three-dimensional

(3D) FETs (e.g., tri-gate transistor, FinFET, both examples of non-planar MOSFETs).



EX1020, Figure 9.41 (FinFET)



EX1020, Figure 3.20 (planar MOSFET)

EX1020, 351, 72-74; EX1002, ¶31.

Inter-layer dielectric layers (ILDs) were known IC structure features typically disposed on the wafer/substrate between features (e.g., metal gates) in the structure. EX1002, ¶32; *e.g.*, EX1020, 370-71.

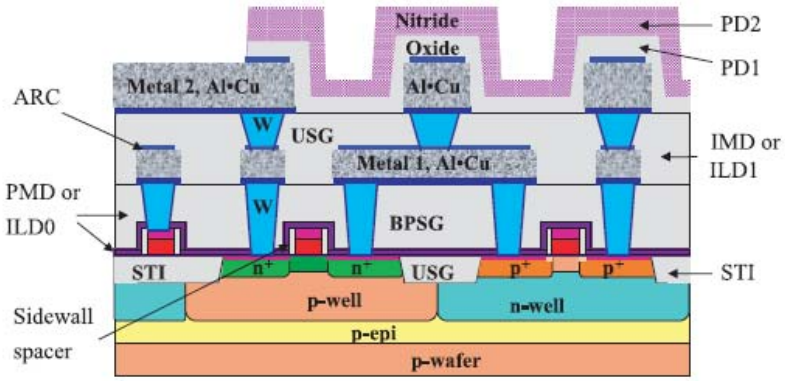


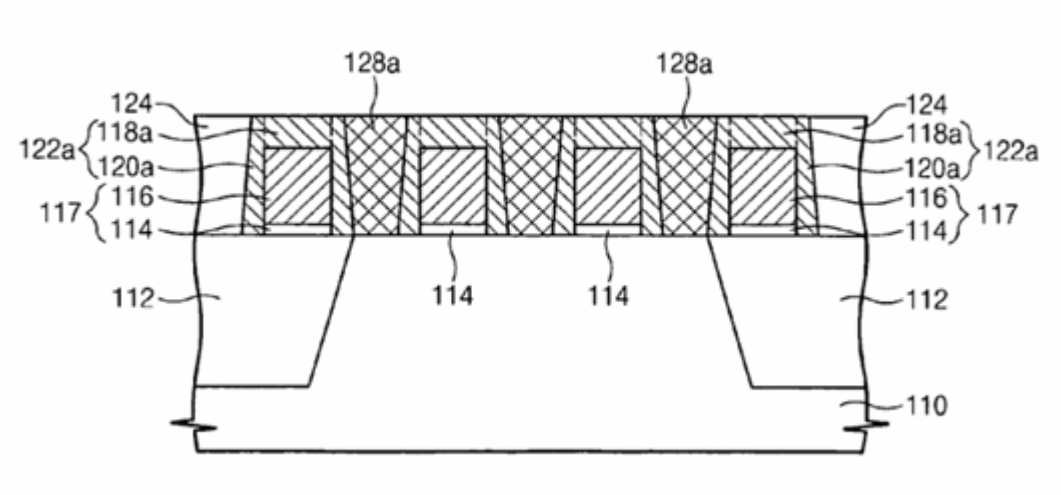
Figure 10.2 Applications of dielectric thin film in a CMOS circuit with Al–Cu interconnection.

EX1020, 371, FIG. 10.2 (ILD filling space between features); EX1005, FIG. 2C, 5:7-10 (ILDs 270).

B. Self-Aligned/Shared Contacts

In ICs, transistors are interconnected in various arrangements through contact plugs and interconnection structures. EX1001, 1:17-21. With "the continuous miniaturization of…IC[s], the line width of interconnections and the feature sizes of semiconductor devices…continuously shrunk." *Id.*, 1:14-17. Making electrical contacts to such miniaturized devices was a known challenge. EX1018, 1:36-65. A known technique to form such contacts was self-aligned contacts (SAC). *Id.*, 1:66-2:13, 2:55-56; EX1024, ¶¶5, 64-68, FIGs. 3D-3F (SAC 128a); EX1002, ¶¶27, 35-36. In SACs, "after forming an opening that simultaneously exposes gates of a region requiring a contact plug and a semiconductor substrate between the gates, a conductive layer is deposited to fill the opening," and the conductive layer (e.g., metal) is then planarized. EX1024, ¶6; EX1002, ¶¶35-36.

Implementation of SACs was known to include the use of cap layers, (hard masks) to cover and thus protect the gate during contact opening formation to features such as the source/drain. EX1024, ¶7; EX1002, ¶37.



EX1024, FIG. 3F

For some IC structures, *e.g.*, static random-access memory (SRAM), it was known to implement shared contacts, which are single contacts connecting together two transistor features, such as a source/drain and a gate. EX1025, ¶¶3, 42-43, FIG. 1 (contact 10), FIG. 8C (below, contact B); EX1002, ¶38.

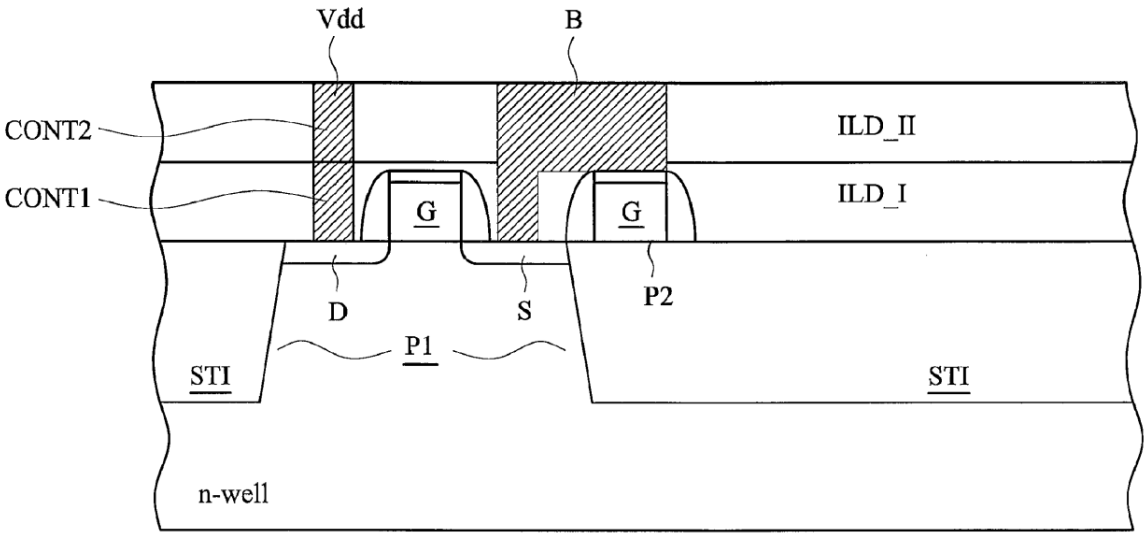


FIG. 8C

Such shared contacts (*e.g.*, EX1025, FIGs. 1, 8C) were a known way to "mak[e] electrical connection…where high device density is desired…, thus, reducing the [IC] die area and enhancing device reliability." EX1025, ¶3; EX1027, 5:59-6:18, FIG. 4 (shared contact 82). EX1002, ¶39.

C. Planarization

Semiconductor device contacting was known to include a planarization step, which was known to include etching and/or chemical mechanical planarization (CMP) for planarizing the surface of semiconductor structures. EX1020, 511-514; EX1026, 1-2 ("CMP became a mainstream process at and below the 0.35um technology node" in "1995"). CMP is a removal process employing chemical and mechanical means to planarize the surface of a semiconductor structure/wafer.

Planarizing etchback processes for recessing transistor gates/spacers in ILD was also known. EX1028, 4:37-60, 7:4-53, Figs. 1A, 2A-2C; EX1029, 4:37-5:6, 7:48-8:37, Figs. 1B, 2A-2C. EX1002, ¶¶27, 40-43.

D. Metal Interconnect (BEOL)

After individual transistors are fabricated and contacted, e.g., through a SAC, for example, BEOL (Back-End-of-Line) processes are used to interconnect the transistors to form an IC. Such interconnection has conventionally included "dual-damascene" processing where metal lines and vias are formed simultaneously to connect to a lower contact level. EX1020, 19, 345-49, 453, 464, 517-18; EX1014, 696-98; EX1015, 55-56. This process involves depositing metal in an etched geometry representing the shape of the metal lines and vias, and then removing the excess metal using CMP. *Id.*

In order to interconnect the up to billions of transistors on modern integrated circuits (ICs), it became necessary to provide multiple metal layers. EX1020, 570; EX1014, 559. To do so, "this dual damascene process is repeated multiple times, depending on how many metal layers there are" (i.e., M2/V1, M3/V2, etc.). EX1020, 19, 345-49, 570; EX1014, 696-98; EX1017, ¶¶37-40, FIG. 3A; EX1002, ¶¶27, 44-46.

III. THE ’747 PATENT

A. Overview

The ’747 patent purports to address drawbacks of prior semiconductor manufacturing process/structures where a barrier layer is formed between upper and lower contact structures formed in different steps. EX1001, Abstract, 1:7-41; *id.*, 1:45-5:66-6:37, FIG. 9.

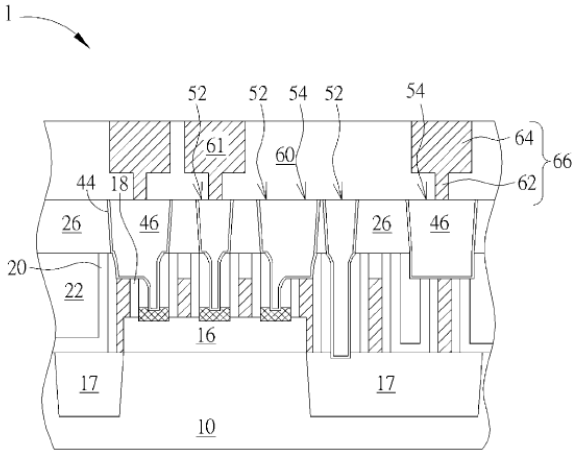


FIG. 9

EX1002, ¶¶47-48.

B. Prosecution History

The ’747 patent issued following a series of rejections/amendments, which added the now claimed truncated spacer, contacts, metal gate, and S/D features. EX1004, 93-110, 134-159; EX1002, ¶49.

C. Claim Construction

Petitioners do not believe any claims require construction to resolve the patentability disputes in this proceeding. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999.) EX1002, ¶68.[1]

IV. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") would have had a master's degree in electrical engineering, physics, chemistry, materials science, or a related field and three years of work experience in semiconductor manufacturing, such as for example, integrated circuit device (or transistor) design and/or manufacturing. Additional relevant education could substitute for professional experience, and

[1] By applying the plain meaning herein, Petitioners do not concede the claims satisfy 35 U.S.C. §112 and reserve all rights to raise claim construction and other arguments (e.g., §112, etc.), in relevant proceedings. *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 11–13 (Nov. 10, 2020). A comparison of the claims to any accused products in litigation may raise controversies that are not presented here given similarities between prior art and the patent.

significant work experience or training could substitute for less formal education. EX1002, ¶¶25-26.[2]

V. PRIOR ART

For purposes of this proceeding, Petitioners assume the May 2, 2013 filing date (EX1001, Cover) is the '747 patent's effective date without conceding to such date.

The asserted references qualify as prior art as follows:

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Pethe	9/19/2012	10/4/2016	§102(a)(2)
Chang	3/31/2005	10/5/2006	§102(a)(1)
Huang	12/22/2011	6/27/2013	§102(a)(1)
Bohr	12/30/2009	5/7/2013	§102(a)(1)
Hong	01/08/2013(CN)	07/10/2014	§102(a)(2)

[2] Petitioners submit the declaration of Dr. Jacob Baker (EX1002), an expert in the field of the '747 patent. EX1002, ¶¶4-24; EX1003.

VI. DETAILED EXPLANATION OF GROUNDS

A. Ground 1A and 1B: Pethe Anticipates (Ground 1A) and Renders Obvious (Ground 1B) Claims 1-5, 8

Because Pethe is in the same field (MOSFETs) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., MOSFET fabrication), Pethe is analogous art. EX1001, 1:9-2:9, 2:39-42, 5:31-6:37; EX1005, 2:50-3:10, 7:9-11:42, 12:22-13:12, 14:4-11; EX1002, ¶50.

Pethe discloses gate contact structures disposed over active portions of gates and methods of forming such structures. EX1005, 2:50-52, 2:50-3:10. Pethe explains "well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention." *Id.*, 2:55-62.

Pethe discloses a semiconductor structure in Figure 5B, including substrate 302, gate electrodes 308, trench contacts 311A-C, ILD region 323, dielectric layer 330, and trench contact vias 341, which are common features (same labels) with Figure 3 and discussed therein (EX1005, 12:22-13:12, FIGs. 5A-5B; *id.*, 2:3-26, 7:9-

11:42) (Pethe does not repeat the details/discussions in Figure 5B).[3] Additionally, Figure 5B's structure includes common features (similar labels) with slight difference from Figure 3 due to recess of spacers 520 (same as spacers 320). *Id.*, 12:22-26, 12:48-53. The features include a cap layer 522 (same as cap layer 322 but wider because of the recessed spacers 520) and includes gate contact vias 542 and metal portion 550 (same as gate contact vias 342 and metal portion 350 but extending deeper because of recessed spacers 520). *Id.*, 12:62-64 ("In comparison to the structure described in association with FIG. 3F, the resulting structure of FIG. 5B is **slightly different** since the spacers 522 are not exposed, yet coverage of the insulating cap layers 522 is extended, during etch formation of the via openings leading to gate contact vias 542A and 542B."); EX1002, ¶¶51-63.

[3] To be clear, Pethe's Figure 5B structure (alone or as modified/combined) discloses/suggests the claim structure in the challenged claims addressed in Grounds 1A-4 for reasons explained. §§IX.A-IX.D; EX1002, ¶¶69-71.

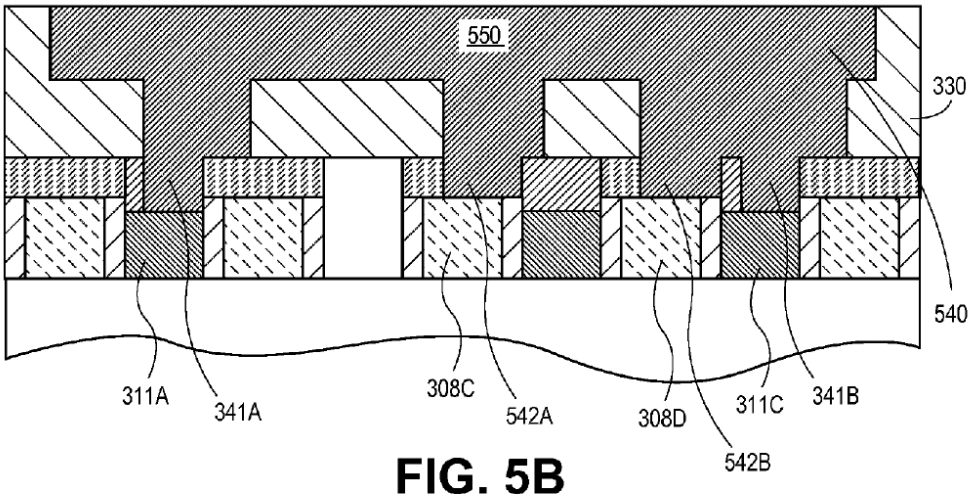


FIG. 5B

1. Claim 1[4]

a) [1.a]

To the extent limiting, Pethe discloses claim 1's preamble. EX1002, ¶¶72-75; *infra* §§VI.A.1.b-VI.A.1.i. Pethe's Figure 5B structure is **[a] semiconductor structure**, the fabrication of which is shown collectively in Figures 5A-5B (below). EX1005, 2:32-36, 12:32-33. A POSITA would have understood Figure 5B's structure has undergone the fabrication steps of Figures 3B-3E. EX1002, ¶¶75, 51-63, 70-71; EX1005, 12:22-53.

[4] *See* Appendix A for all claim language. (§XII.)

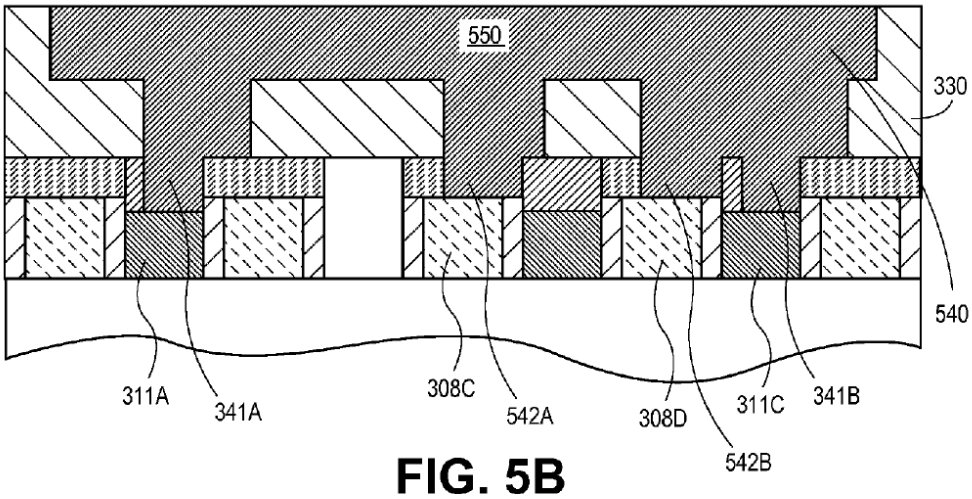


FIG. 5B

b) [1.b]

Pethe discloses this limitation. EX1002, ¶¶76-78. Pethe's substrate 302 is **a substrate**, below:

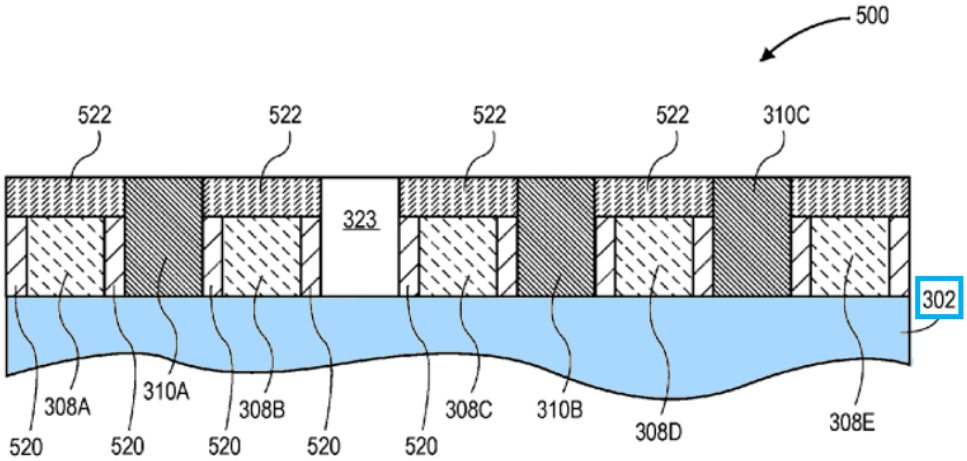


FIG. 5A

EX1005, 12:37-45, FIGs. 5A-5B.

c) [1.c]

Pethe discloses this limitation. EX1002, ¶¶79-92. Pethe discloses an inter-layer dielectric layer that includes region 323 shown in Figure 5B's structure. The inter-layer dielectric layer is the first dielectric layer.

Indeed, "contact blocking **regions**…, such as region 323 fabricated from ***an inter-layer dielectric material***, may be included in **regions** where contact formation is to be blocked" (e.g., fills spaces where no gate structure or source/drain contact). EX1005, 7:31-34; EX1002, ¶¶81-85.[5] Pethe's ILD region 323 is further described as being formed using a process as described in Golonzka (EX1006), which is incorporated in Pethe. EX1005, 7:35-8:23. *Paice LLC v. Ford Motor Co.*, 881 F.3d 894, 906-07 (Fed. Cir. 2018). Golonzka's incorporated teachings explain that corresponding first and second interlayer dielectric portions 128,132, which fill the

[5] In discussing Figures 5A-5B, Pethe does not repeat its Figure 3A discussion of ILD region 323, similarly labeled in Figure 5A. *See* Google *LLC v. Jenam Tech, LLC*, IPR2021-00630, Paper 38 at 20, n.9 (P.T.A.B. Sept. 16, 2022) (applying same disclosures where "figures refer to corresponding features using the same reference numbers").

spaces where there is no gate structures or trench contacts, are an inter-layer dielectric layer. EX1006, ¶¶0042-0050, FIGs. 1H-1J, 1K-2 (below).

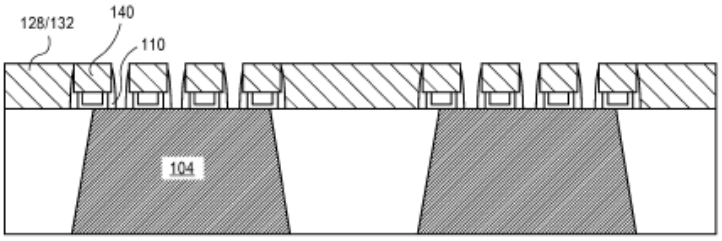


FIG. 1K

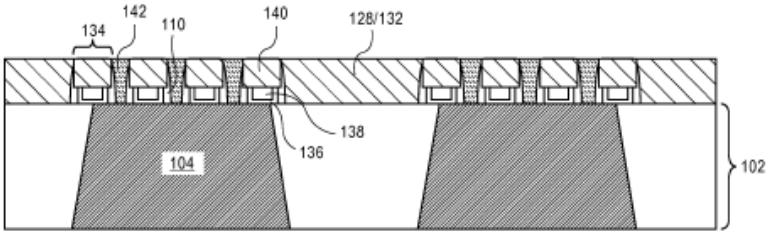


FIG. 2

EX1002, ¶¶86-87; EX1005, 7:31-34 (describing Fig. 2's ILD as a "layer").

Thus, Pethe's Figure 5B structure includes contact blocking regions (of which region 323 is a part and fabricated with inter-layer dielectric material (*supra*)) that is a **dielectric layer** (hereinafter "Pethe's first dielectric layer") that is **disposed on the substrate** (302) (EX1005, 12:32-53, 7:20-34, 12:39-13:12; FIG. 3A), as claimed and shown below:

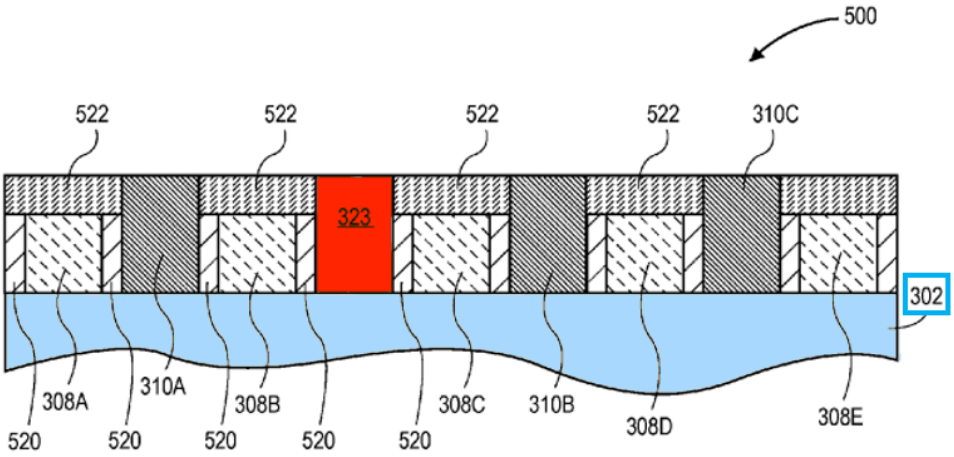


FIG. 5A

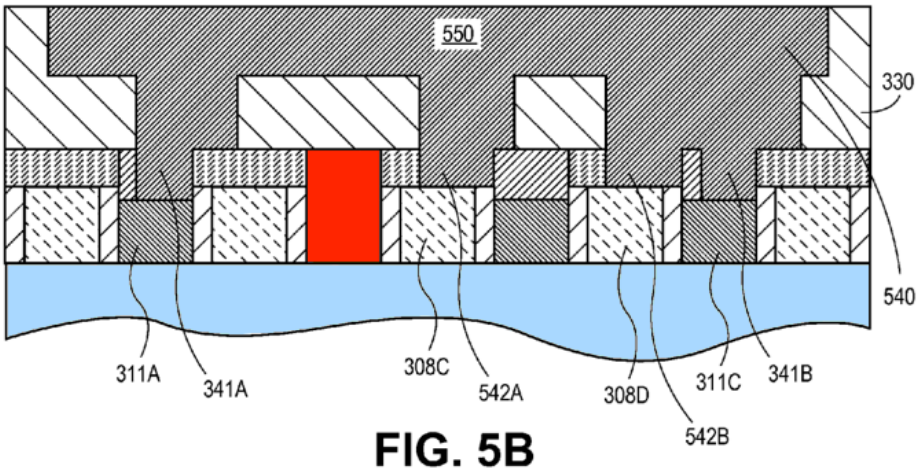


FIG. 5B

EX1002, ¶¶88-92.

d) [1.d]

Pethe discloses this limitation. EX1002, ¶¶93-102. Pethe's "gate stack structures 308A-308E" comprise five **metal gates** (which is **at least two**), as shown annotated below:

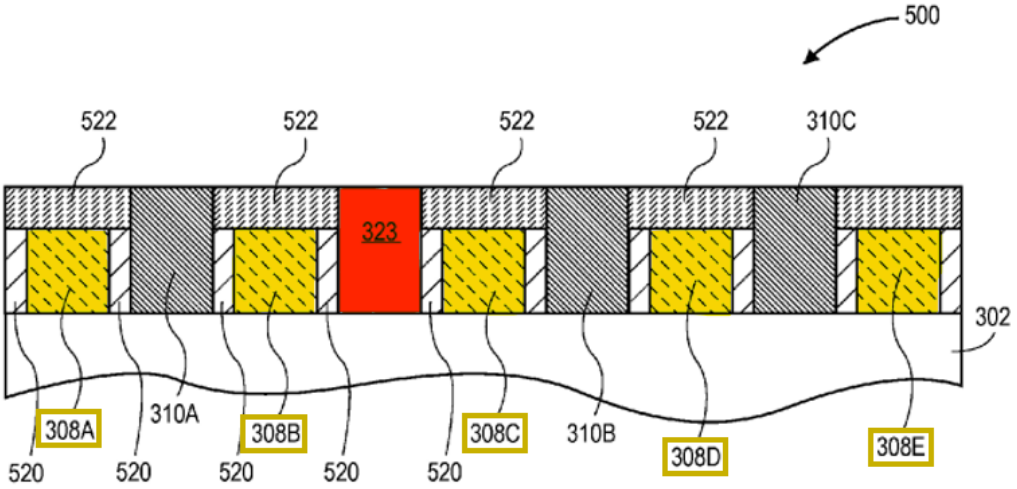


FIG. 5A

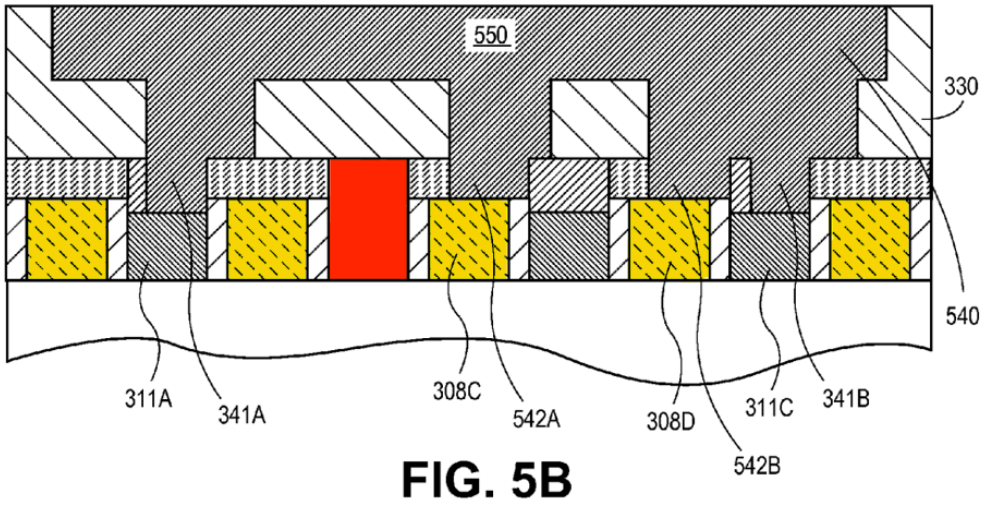


FIG. 5B

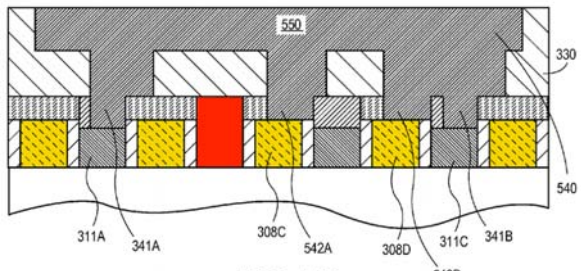
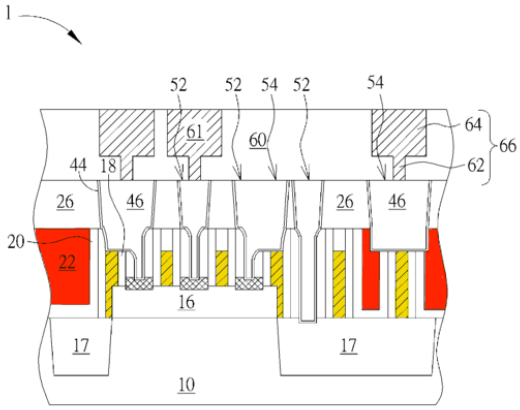
EX1005, 12:32-53; EX1002, ¶94.

Gate stack structures 308A-308E are **metal**. EX1002, ¶¶95-97. Pethe discloses that gate structures 308A-308E "may include a gate dielectric layer and a gate **electrode**, as described above in association with FIG. 2." EX1005, 12:39-42.

There, Pethe confirms "the gate electrode is composed of a **metal** layer." EX1005, 6:37-44.

Additionally, Figure 5A's structure 500, which has its gate stack structures fully formed, "is provided following trench contact (TCN) formation." EX1005, 12:32-53. The TCN process is used to form structure 500 in Figure 5A (*id.*) and structure 300 in Figure 3A (*id.*, 7:15-34) and is described by Golonzka (EX1005, 7:35-8:11), which further confirms that the "gate electrode…is composed of a **metal** gate." EX1006, ¶0049.

Gate stack structures 308A-308E are **disposed in the first dielectric layer (of which region 323 is a part)**. §VI.A.1.c; EX1005, FIGs. 5A-5B. The relationship of metal gates and first dielectric layer in Pethe's Figure 5B structure is consistent with the '747 patent disclosure of similar features:

 FIG. 5B	 FIG. 9
Pethe	**'747 Patent**

EX1002, ¶¶95-99; EX1001, 5:66-6:5.

As explained, the Pethe's **first dielectric layer (of which region 323 is a part**) is blanket deposited on the substrate and fills the spaces where there is no gate structure and no contact (*i.e.*, "regions where contact formation is to be blocked"), meaning the **metal gates** are **disposed in** the **first dielectric layer**. EX1005, 7:31-34; §VI.A.1.c; EX1002, ¶¶99-101.

Golonzka's incorporated teachings describe the TCN process used to form Figure 5A's 500 structure including fully formed gate structures, further confirming the disposition of the metal gates in the ILD. EX1005, 12:32-37, 7:15-41; §VI.A.1.c; EX1006, ¶¶0044-0049 (gate formed disposed in the layer comprising interlayer dielectric 128/132), FIG. 1J (annotated below showing metal gates 138 within dielectric 132), FIGs. 1I, 1K (128/132), 2. Accordingly, the resulting Figure 5B structure includes at least two metal gates disposed in the first dielectric layer as claimed.

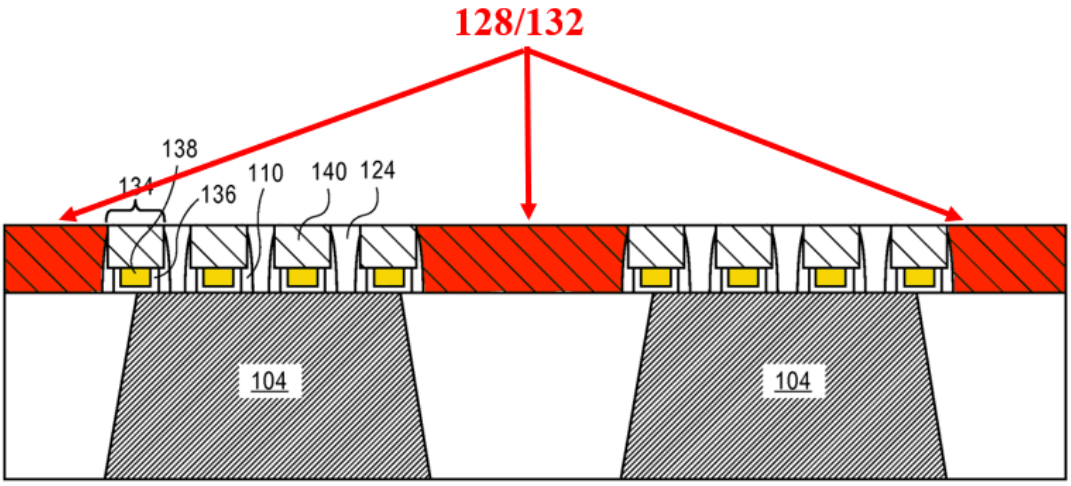
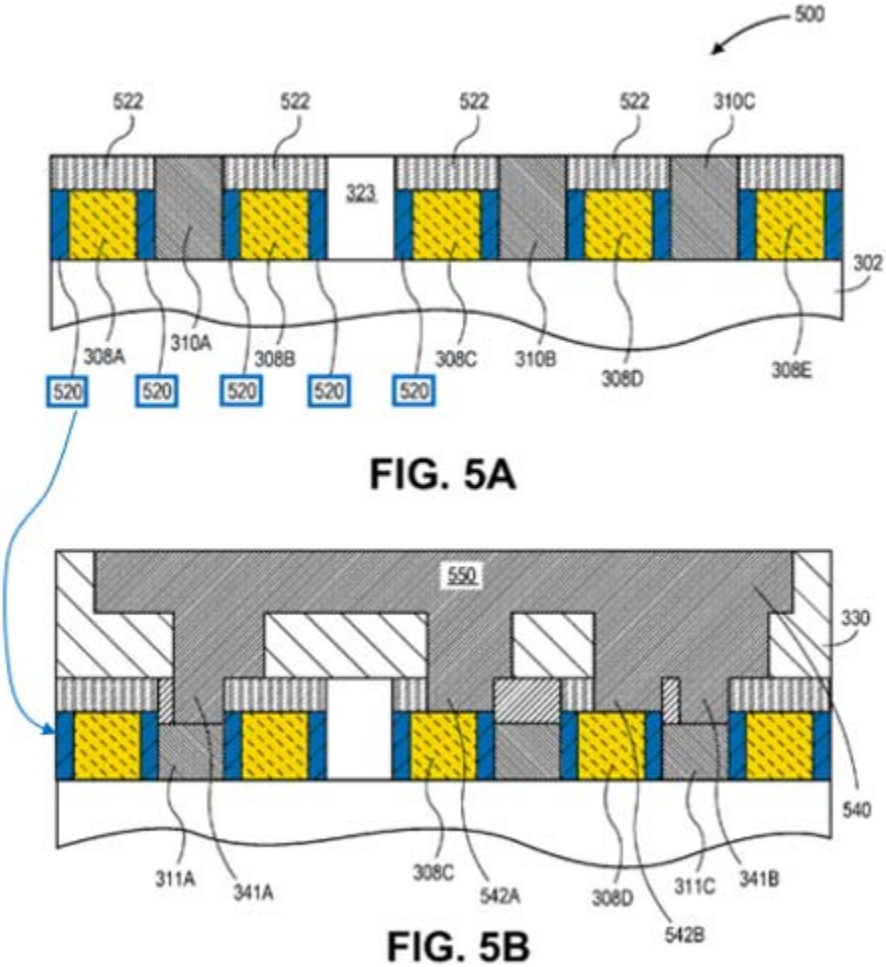


FIG. 1J

EX1006, FIG. 1J (annotated); EX1002, ¶¶100-02.

e) [1.e]

Pethe discloses this limitation. EX1002, ¶¶103-16. Pethe's spacers 520 - (**spacer**) are **disposed on two sides of** each gate stack structure 308A-308E (any one or more being **the metal gate**) of Figure 5B's structure, as annotated below:



EX1005, 12:42-53, 12:22-31, FIGs. 5A-5B; EX1002, ¶¶103-07. Trench contacts 310A-310C (in Figure 5A) and 311A-311C (in Figure 5B)[6] are "spaced apart from gate stack structures 308A-308E by dielectric spacers 520." EX1005, 12:42-45.

[6] 310A-310C (shown in annotated Figure 5A) "are recessed" to become recessed trench contacts 311A-311C (shown in annotated Figure 5B). EX1005, 13:1-12.

Pethe's spacer 520 **has a truncated top surface**. EX1002, ¶¶108-16. Pethe explains "the spacers 520 have been **recessed** to approximately the same height as the gate stack structures 308A-308E" (EX1005, 12:48-53) and "recessed to be essentially **planar**" (*id*., 12:15-31). *Id.*, FIGs. 3A, 3F, 5A-5B (below).

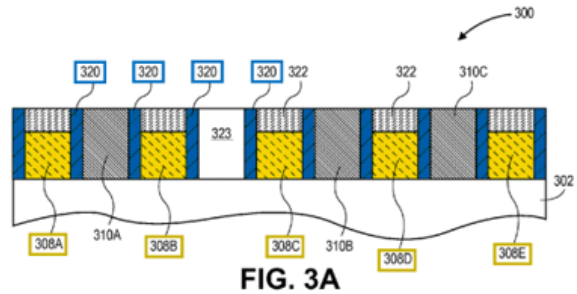


FIG. 3A

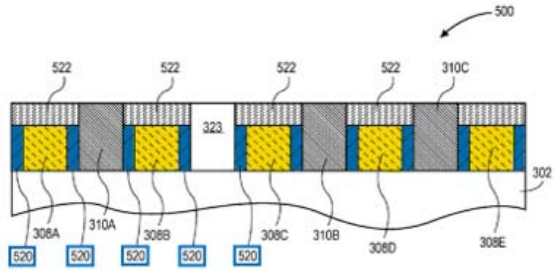


FIG. 5A

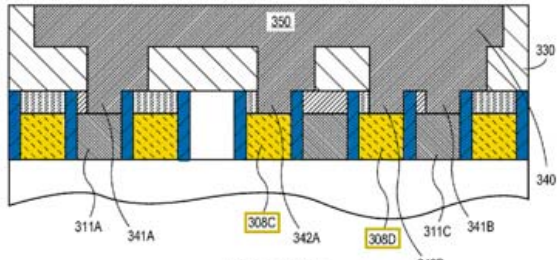


FIG. 3F

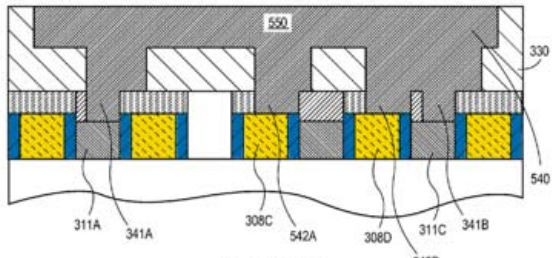


FIG. 5B

EX1002, ¶¶109-10.

Pethe generally uses the terminology "recessed" to connote that a given feature has been truncated by removing material from the feature's top surface. EX1005, 8:24-51 (explaining trench contacts "may be recessed by...**an etch process** such as a wet etch process or dry etch process"); *id*. at 13:1-12. It was known to use planarizing etch processes to recess gates/spacers in ILD. §II.C. Pethe's spacers

have been "recessed to be essentially **planar**," meaning the recessing is a planarizing process. EX1005, 12:22-31; EX1002, ¶¶111-16. Figures 5A-5B (below) depicts spacers 520 as planar, further consistent with the disclosure of spacer 520 having a **truncated top surface**. A POSITA would have understood in context of Pethe's disclosures where the **top surface** of each spacer 520 is "recessed" to a lower height (same height as gate stack structures 308A-308E) and "planar," it is **truncated**.

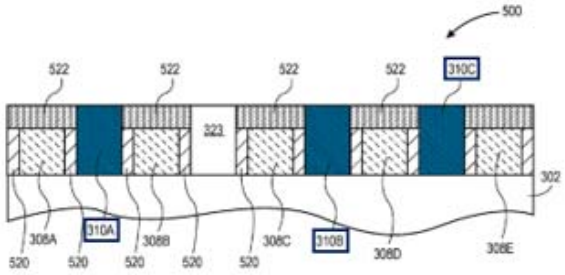


FIG. 5A

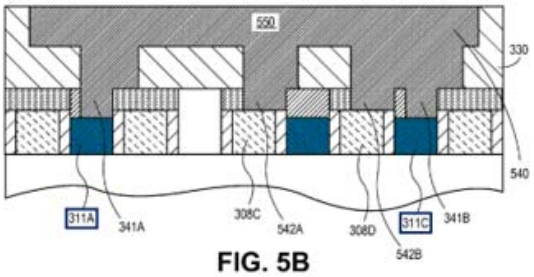


FIG. 5B

EX1002, ¶¶112-16.

f) [1.f]

Pethe discloses this limitation. EX1002, ¶¶117-40. Pethe teaches that trench contacts (310A-310C (Figure 5A) and 311A-311C (Figure 5B)) contact "diffusion regions" that include **a source/drain region (S/D region) disposed between respective two metal gates in** gate stack structures 308A-308E (any two being **two metal gates**), as annotated below.

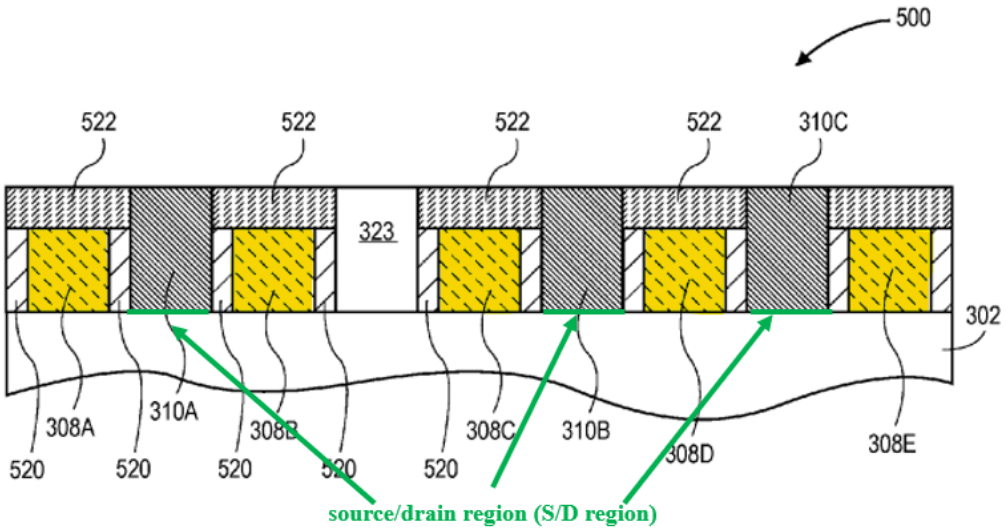


FIG. 5A

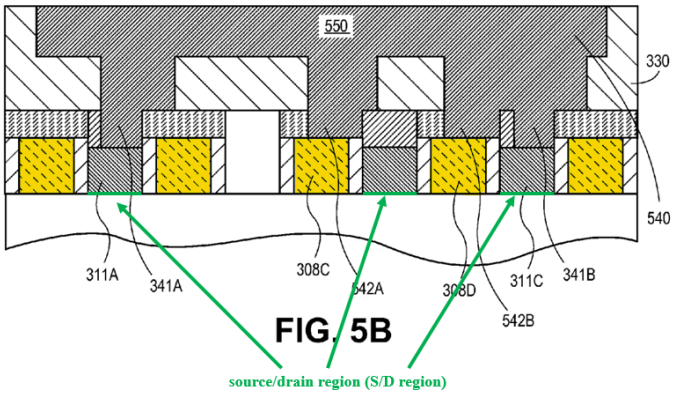
EX1005, 12:32-53; EX1002, ¶¶118-19.

Pethe explains, "[t]rench contacts, *e.g.*, **contacts to diffusion regions** of substrate 302, such as trench contacts 310A-310C are also included in structure 500 and are **spaced apart from gate stack structures 308A-308E** by dielectric spacers 520." EX1005, 12:32-53.

The "trench contacts...to diffusion regions" are contacts to source/drain regions (S/D regions). EX1002, ¶¶120-25. In Pethe, the term "trench contacts" means source/drain contacts. EX1005, 3:25-28 ("**Source or drain contacts (also known as trench contacts)**...are disposed over source and drain regions."), 3:31-35 ("source or drain trench contacts"), 4:33-36 ("**Source or drain trench contacts,**

such as trench contacts...are disposed over source and drain regions.”) ; EX1002, ¶120.

Trench contact vias 341A/341B (formed by filling openings 336 with metal) extending to recessed trench contacts 311A-311C are “contacts to the **source[/]drain regions of the transistor**.” EX1005, 10:35-36, 9:29-10:36, 12:54-13:21, FIGs 5A-B, 3A-3F.[7] A POSITA would have understood diffusion regions of substrate 302 that contact **trench contacts 311A-311C** include **a S/D region**, which is **“disposed between two metal gates**,” below. EX1002, ¶¶121-26.



[7] Pethe does not repeat its earlier discussion of 341A/341B, 311A/311C, and S/D regions for Figures 3A-3F to describe similarly labeled elements in Figure 5A-5B (341A/341B and 311A/311C). *Google LLC*, Paper 38 at 20, n.9; EX1002, ¶¶70-71, 125.

Moreover, (relevant to **Ground 1B**), a POSITA would have recognized Pethe's numerous disclosures to known FET features, including source/drain regions and gates. *Supra* above; EX1005, 13:63-14:13; *id.*, 3:25-28, 3:32-37, 4:33-36, 4:42, 7:25-28, 9:29-10:36, 10:35-36, 11:21-22; EX1002, ¶¶127-40. A POSITA would have understood to make a FET, e.g., planar FET or FIN-FET, as Pethe contemplates (EX1005, 13:63-14:13), a source/drain region was needed disposed on both sides of the gate—a typical and expected feature in forming FETs. EX1002, ¶¶128-36; §II.A. A POSITA would have thus found it obvious that Pethe's Figure 5B structure includes a S/D region between the two metal gates, which simply involves applying known semiconductor technologies/techniques with a reasonable expectation of success. EX1002, ¶¶137-40. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

g) [1.g]

Pethe discloses this limitation. EX1002, ¶¶141-54. Pethe teaches trench contact vias 341A, 341B that are **a plurality of first contacts**, below:

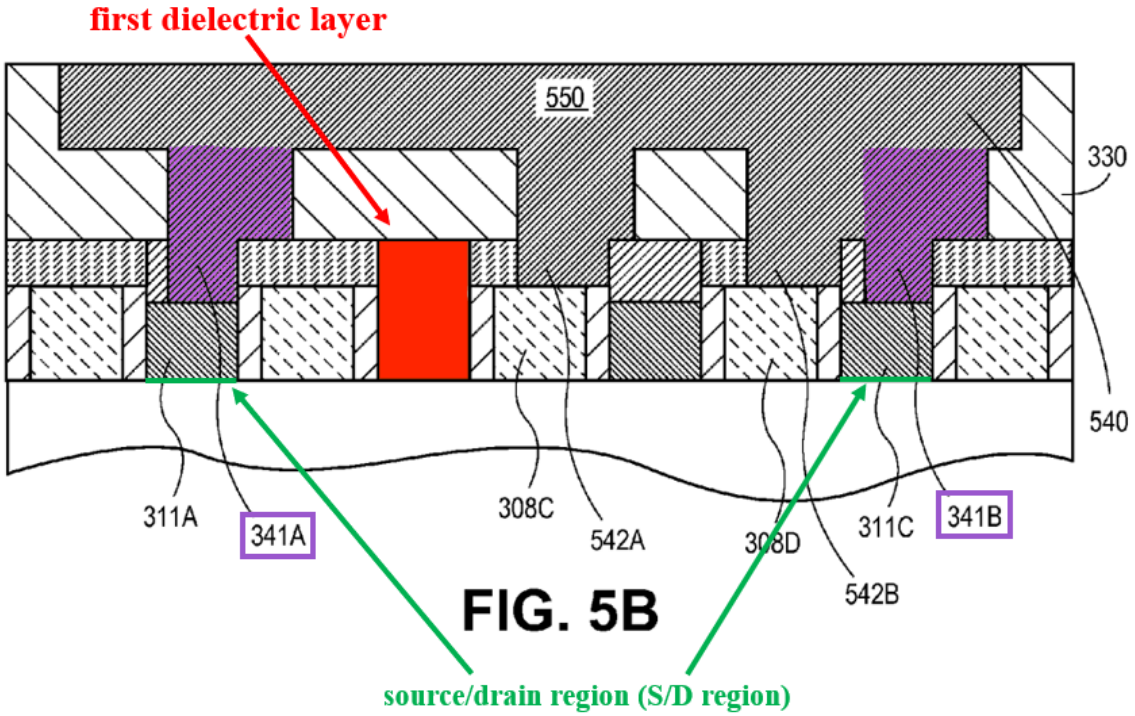


FIG. 5B

EX1005, 12:54-67; EX1002, ¶¶142-43.

As shown, trench contact vias 341A, 341B are **disposed in the first dielectric layer (of which region 323 is a part)**. *Id.*; §VI.A.1.d.

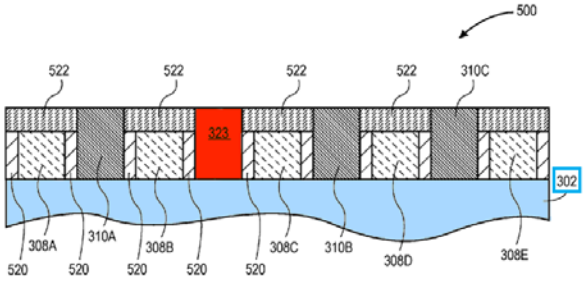


FIG. 5A

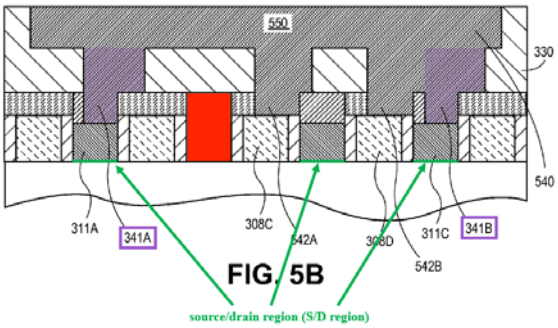
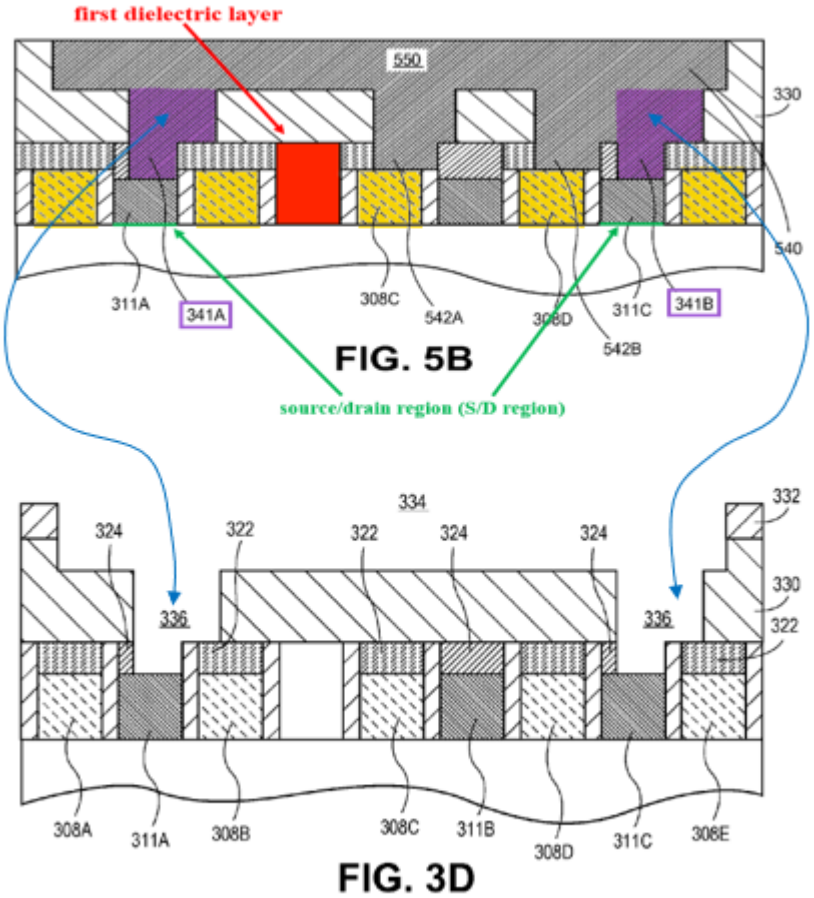


FIG. 5B

EX1002, ¶¶144-50.

Pethe's Figure 5B structure includes trench contact vias 341 that "a metal contact structure 340 is formed in…via openings 336" and the "metal contact structure 340 includes…trench contact vias (e.g., trench contact vias 341A and 341B to trench contacts 311A and 311C, respectively)…." EX1005, 11:23-31. Trench contact vias 341 comprise metal that fill openings 336 shown in Figure 3D below (blue arrows):



EX1005, 11:23-31, 11:32-42, 9:29-10:36; EX1002, ¶¶149-54.

Pethe describes "trench contact vias 341A and 341B" are contacts "to trench contacts 311A and 311C," meaning 341A/341B are **electrically connected to** 311A/311C. EX1005, 12:54-67; *id*., 11:23-29; EX1002, ¶¶151-54. And as explained (§VI.A.1.f), in Pethe, the term "trench contacts" means source/drain contacts. Thus, 341A/341B **are electrically connected to** trench contacts 311A/311C, and 311A/311C **are electrically connected to** the source/drain regions, meaning that the trench contact vias 341A/341B (**a plurality of first contacts**) **are electrically connected to parts of the S/D region** in Figure 5B's structure. EX1002, ¶¶151-54; EX1005, 10:35-36, 9:29-10:36; 12:54-59.

h) [1.h]

Pethe discloses this limitation. EX1002, ¶¶155-75. Pethe teaches gate contact vias 542A/542B that are **a plurality of second contacts**, below:

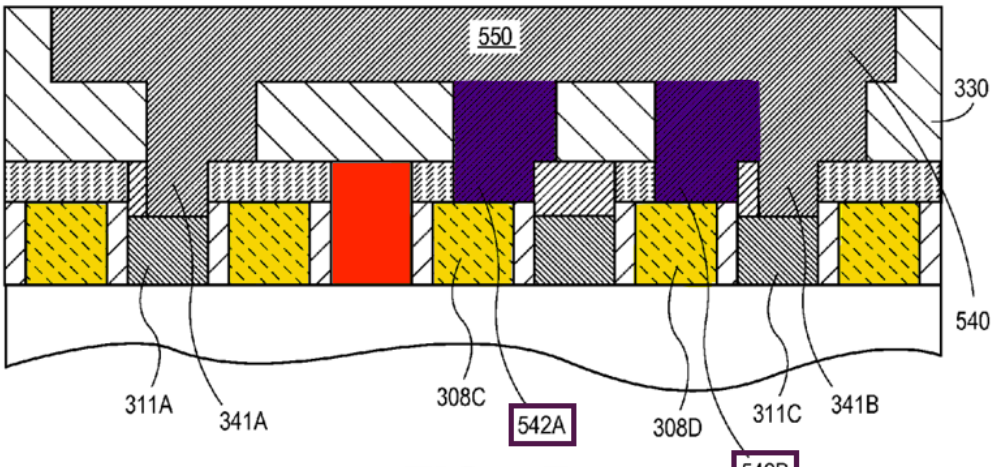


FIG. 5B

EX1005, 12:54-67; EX1002, ¶156.

As shown, gate contact vias 542A, 542B are **disposed in** [**Pethe's] first dielectric layer** (of which region 323 is a part), as discussed for limitation [1.d]. EX1002, ¶157; §VI.A.1.d. Pethe explains that "gate contact vias 542A and 542B" (**a plurality of second contacts**) are "to gate stack structures 308C and 308D, respectively" (**are electrically connected to one of the metal gates**). EX1005, 12:54-67, FIG. 5B; EX1002, ¶158.

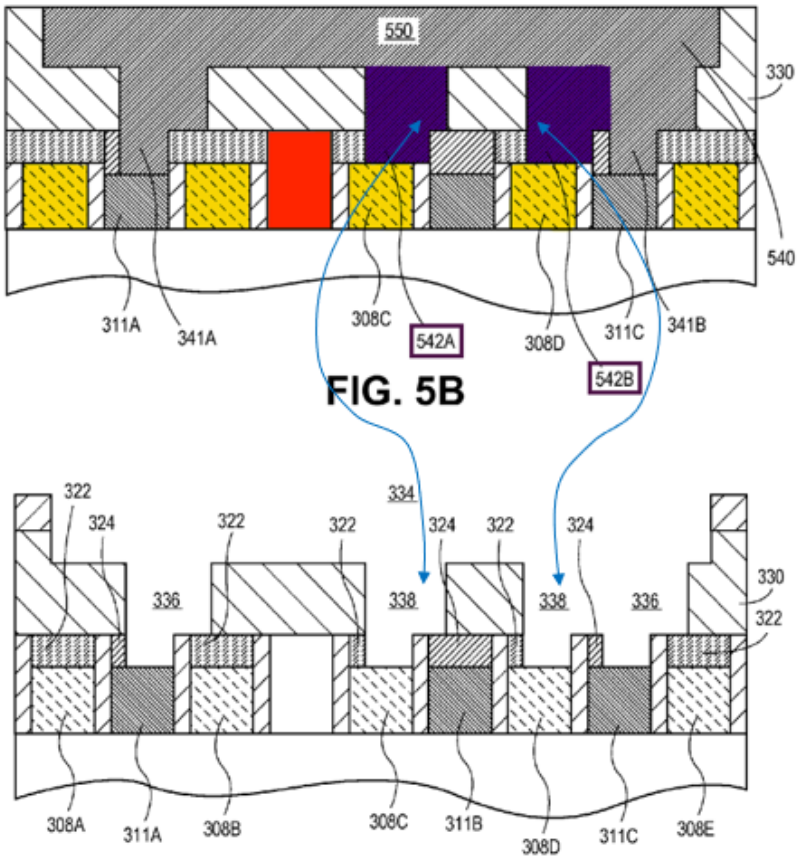
Given gate contact via 542A **is electrically connected to** 308C (**one of the metal gates**) and gate contact via 542B is **electrically connected to** 308D (**one of the metal gates**), the **plurality of second contacts**...**are electrically connected to one of the metal gates**. EX1005, 12:54-67; EX1002, ¶159.

Accordingly, Pethe's teachings concerning Figure 5B's structure discloses the "**plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts**" as claimed. *Id.*

The process of forming gate contact vias 542 further confirms Figure 5B's structure includes the features of limitation [1.h]. Namely, the formation of gate contact vias 542 share the same processes of formation as gate contact vias 342 (same feature but deeper only because of recessed spacers 520). EX1005, 12:54-67 (Figure 5B's structure "[i]n comparison to the structure described in association

with FIG. 3F" is just "slightly different since the spacers 522 are not exposed, yet coverage of the insulating cap layers 522 is extended, during etch formation of the via openings leading to gate contact vias 542A and 542B"); EX1002, ¶¶160-73.

Pethe explains "a metal contact structure 340 is formed in… via openings… 338" and that "metal contact structure 340 includes…gate contact vias (e.g., gate contact vias 342A and 342B to gate stack structures 308C and 308D, respectively)." EX1005, 11:23-31. Indeed, gate contact vias 342A/342B comprise metal that fill openings 338 shown in Figure 3E below (blue arrows):



EX1005, 11:23-31, 10:37-11:22; EX1002, ¶¶160-73.

Pethe explains metal (0) trench 334, via openings 338, and via openings 336 are formed by etching. EX1005, 9:1-11:22. A single metal deposition (i.e., "of a fill metal layer") fills all three regions, by which metal (0) trench 334 is filled with metal (0) portion 350, gate contact vias 342 fill via openings 338, and trench contact vias 341 fill via openings 336. *Id.*, 11:23-42. Thus, Pethe discloses gate contact vias 542 (**at least one of the first contacts**) directly gate contact via 342B (**at least one**

of the second contacts) with no intervening layers or other barriers in the Figure 5B structure.

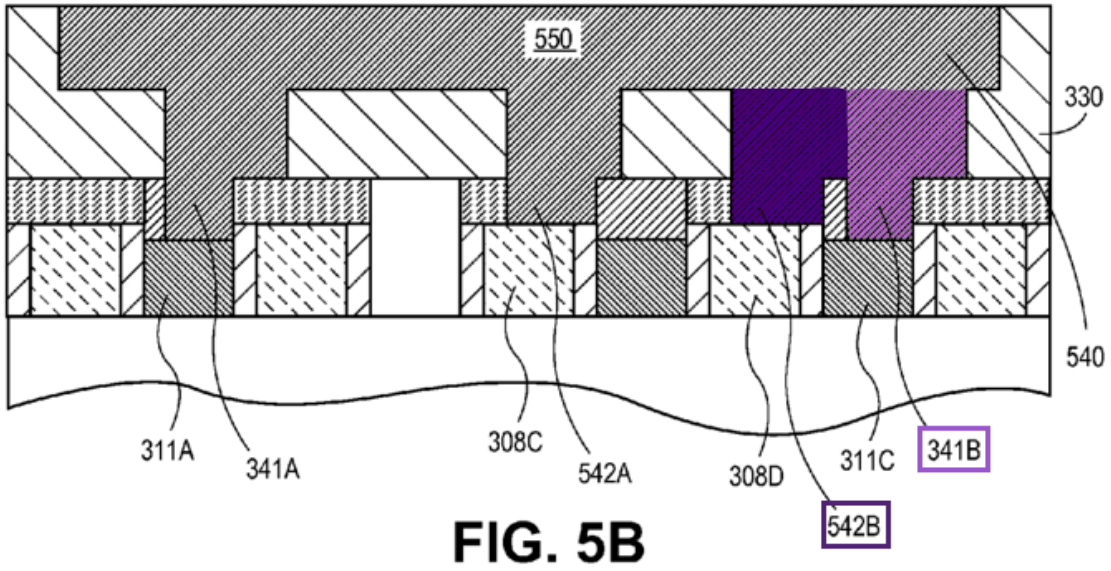


FIG. 5B

EX1005, 12:54-67; EX1002, ¶¶174, 164-65.[8]

i) [1.i]

Pethe discloses this limitation. EX1002, ¶¶176-86. Pethe's insulating cap layer 522 is **a hard mask** that "is **disposed on** the gate stack structures 308A-308E," *e.g.*, 308B (**one of the metal gates**), below:

[8] Pethe's teachings are consistent with the '747 patent's descriptions of first and second contacts formed next to each other. EX1001, FIG. 9 (elements 52/54); EX1004, 135.

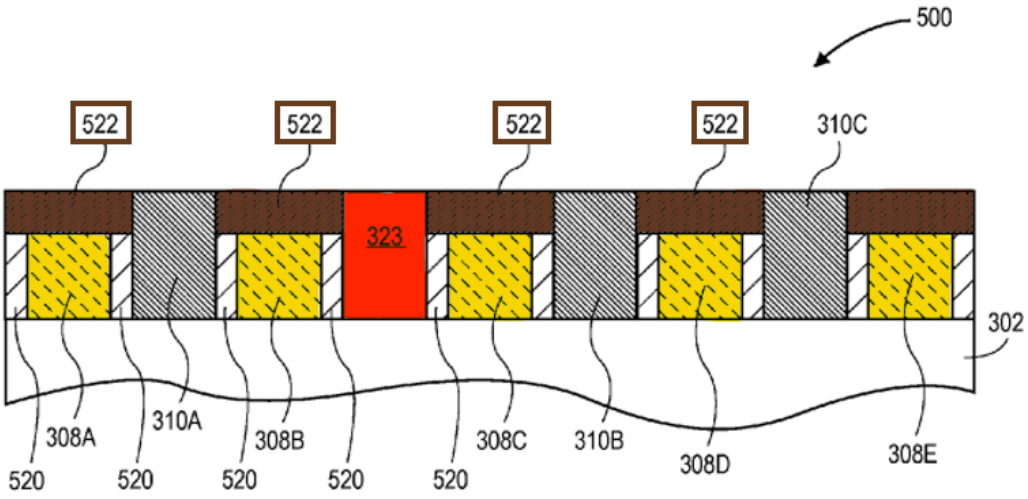


FIG. 5A

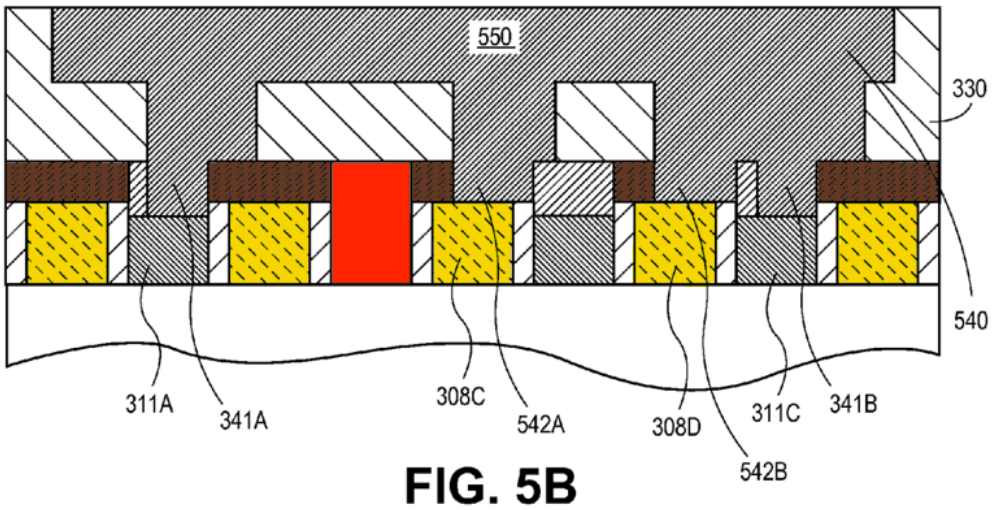


FIG. 5B

EX1005, 12:45-67; EX1002, ¶¶177-83. Indeed, "insulating cap layers 522...cover[] the gate stack" (*id.*) and is disposed on the gates "for protecting a metal gate electrode." EX1005, 3:48-50, 4:54-56. Consistent with the '747 patent's disclosure, Pethe's cap layer 522, which is an insulating layer that provides protection for gate

regions directly covered by 522 and is utilized in the contact formation process, is a **hard mask**. EX1002, ¶178, 183; EX1001, 6:2-18, FIGs. 7, 9.

The **top surface of** layer 522 (same as cap layer 322 but wider) **and the top surface of** Pethe's **first dielectric layer** (of which region 323 is a part of) **are on the same level**. EX1002, ¶¶179-80. This **same level** is further confirmed by the CMP planarization described by Pethe (EX1005, 8:24-51, Fig. 3B) and discussed below for claim 3 (§VI.A.3). Pethe explains the conformal deposition of cap layer 324 and subsequent planarization by CMP occurs over "the entire structure" to provide layer 324 "only above 310A-310C," and "re-exposing spacers 320 and insulating cap layer 322" (EX1005, 8:37-51), further confirming that Pethe's first dielectric layer (of which region 323 is a part) and insulating cap layers 322 (and 522) and 324 would all become planarized with the top surfaces **on the same level**. EX1005, 8:44-51; §II.C; EX1002, ¶180. Such features in the Figure 5B structure are comparatively shown below.

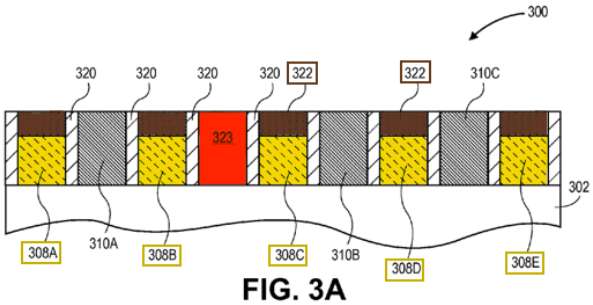


FIG. 3A

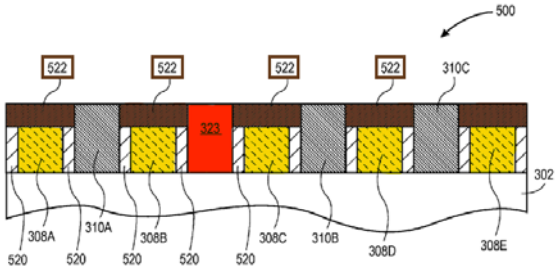


FIG. 5A

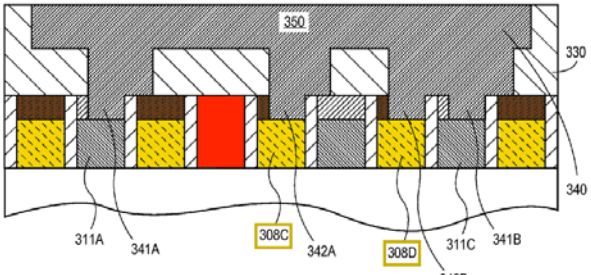


FIG. 3F

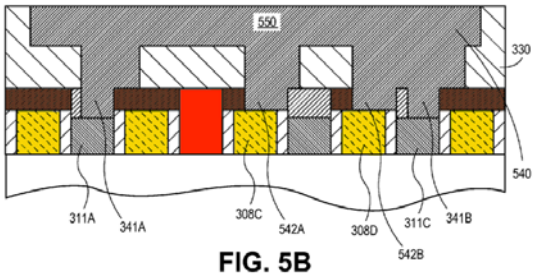


FIG. 5B

EX1002, ¶¶184-86.

2. Claim 2[9]

Pethe discloses this limitation. EX1002, ¶¶187-93. Pethe's inter-layer dielectric 330 is **a second dielectric layer disposed on** [Pethe's] **first dielectric layer** (of which region 323 is a part), below.[10]

---

[9] Claim 1 does not recite a "semiconductor device." EX1001, 6:53-7:3. Nonetheless, for purposes of this proceeding only, Petitioners assume claims 2-9 refer to the semiconductor "structure" in claim 1, without conceding claims 2-9 are definite, have specification support, etc.

[10] Pethe does not repeat its discussion of 330 for Figures 3C-3F to describe the similarly labeled element in Figure 5B. *Google LLC*, Paper 38 at 20, n.9.

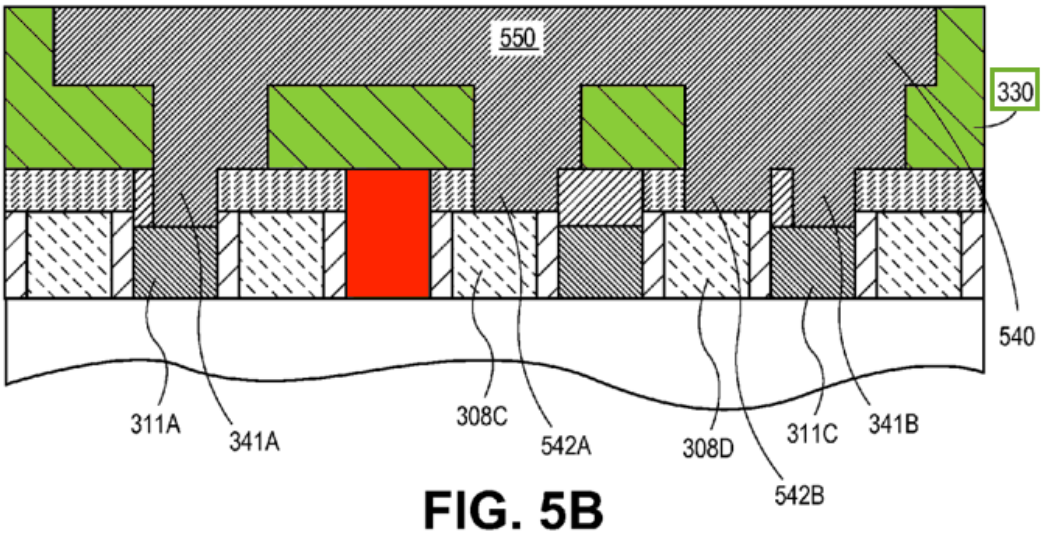


FIG. 5B

EX1005, 12:54-67; *id.*, 9:1-43 (ILD 330 "may be composed of a material suitable to electrically isolate metal features"), 10:47-51, FIGs. 3F, 5B (comparatively shown below); EX1002, ¶¶188-91.

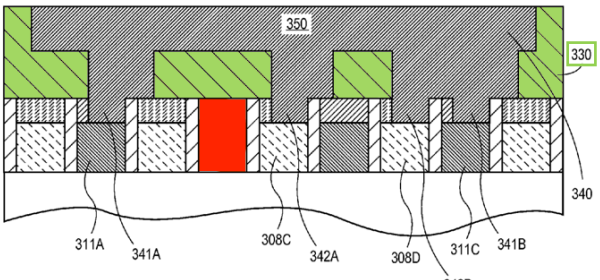


FIG. 3F

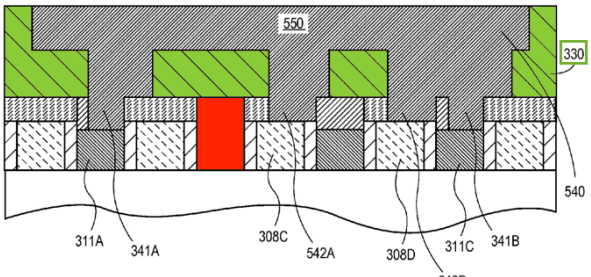


FIG. 5B

EX1002, ¶¶192-93.

3. Claim 3

Pethe discloses these limitations. EX1002, ¶¶194-204.

Pethe discloses/suggests an insulating cap layer 324 that is **an etching stop layer disposed on two sides of** the gate stack structures 308A-308E, e.g., 308D (**the metal gate**), below:

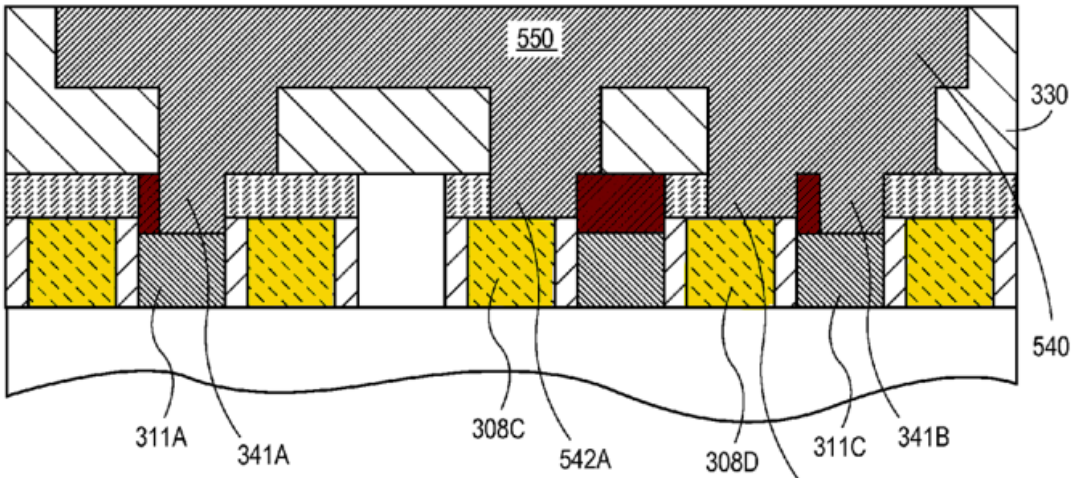


FIG. 5B

EX1005, 12:32-13:12; EX1002, ¶¶195-97.

Pethe explains "insulating cap layer 322 is etched to form via openings 338 **selective to (i.e., without significantly etching or impacting) insulating cap layer 324.**" EX1005, 10:44-51, 10:62-64. Thus, cap layer 324 in the Figure 5B structure is an **etching stop layer** as it is exposed to, but not removed by the etch.[11] EX1002, ¶¶198-200.

[11] A POSITA would have understood Figure 5B's structure has undergone the fabrication steps of Figures 3B-3E. EX1002, ¶75; EX1005, 12:22-53.

Cap layer 324 in the Figure 5B structure **has a truncated top surface** because it is planarized by a CMP. EX1005, 8:41-44 (layer 324 is formed as a conformal layer above exposed portions of trench contacts 310A-310C), 8:47-51 (conformal layer is then planarized, e.g., by CMP, to provide layer 324 only above 310A-310C, and "re-exposing spacers 320 and insulating cap layer 322"). This removal of the top portion of cap layer 324 by polishing results in **a truncated top surface**. EX1002, ¶¶201-04.

4. Claim 4

Pethe discloses these limitations. EX1002, ¶¶205-12.

As explained for claim 1, Pethe discloses first contacts (trench contact vias 341A/341B) disposed in Pethe's first dielectric layer (of which region 323 is a part) and in the second dielectric layer (inter-layer dielectric 330), below.

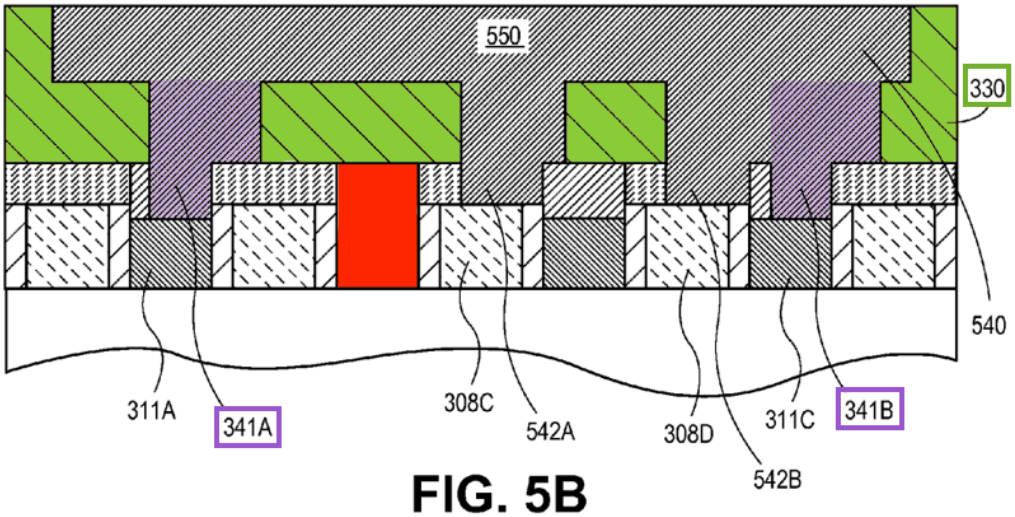


FIG. 5B

§§VI.A.1-VI.A.3; EX1005, 12:32-13:12; EX1002, ¶206-08.

As explained by Pethe (EX1005, 9:29-10:36, 12:15-67), each trench contact vias 341A and 341B **is a monolithically formed structure** because each is formed by filling an opening 336 with a single metal contact structure 340. In Figure 3F, a single metal deposition (*i.e.*, "deposition of **a fill metal layer**") fills openings 336 to form trench contact vias 341A and 341B, each as a **monolithically formed structure**. EX1005, 11:23-42, FIG. 3F; EX1002, ¶¶209-12.

Thus, trench contact vias 341A, 341B in Pethe's Figure 5B structure are each a **monolithically formed structure**, as recited in claim 4. *Id.*

5. Claim 5

Pethe discloses these limitations. EX1002, ¶¶213-22.

As explained for claim 1, Pethe discloses the second contacts (gate contact vias 542A, 542B) disposed in Pethe's first dielectric layer (of which region 323 is a part) and in the second dielectric layer (inter-layer dielectric 330).

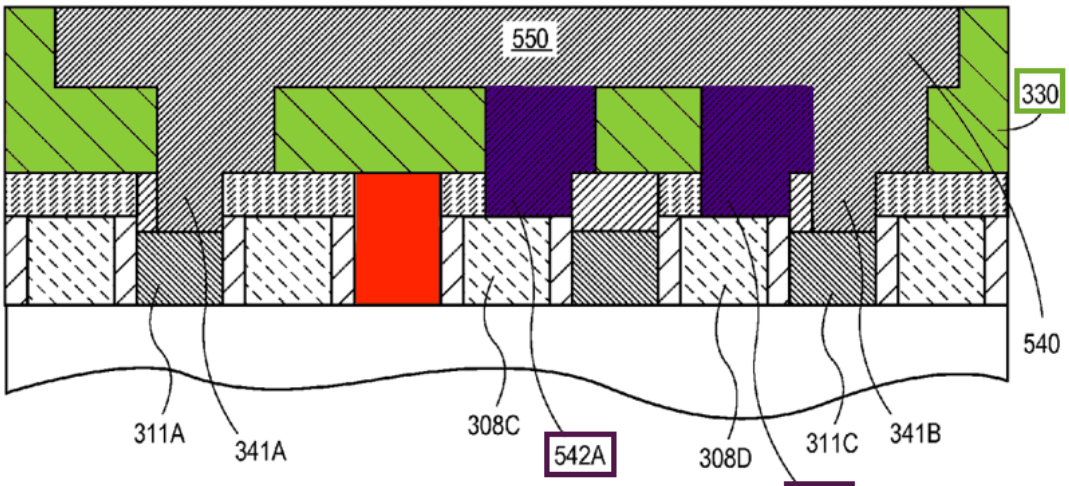


FIG. 5B

§§VI.A.1-A.3; EX1005, FIG. 5B (below), 12:54-13:12, 11:23-31, 9:1-43, 7:15-34; EX1002, ¶¶214-15.

Regarding Figure 5B, Pethe explains "a metal contact structure 540 is formed in a metal (0) trench and via openings formed in a **dielectric layer 330**" (**second dielectric layer**). EX1005, 12:54-56. Pethe also explains "contact structure 540 includes…gate contact vias (e.g., gate contact vias 542A and 542B to gate structures 308C and 308D, respectively)" (EX1005, 12:59-62), further confirming gate contact vias 542 (**second contacts**) are disposed in Pethe's **first dielectric layer** (of which region 323 is a part) and dielectric layer 330 (**second dielectric layer**), and are monolithically formed. EX1002, ¶¶216-17.

As described in §VI.A.1.h, Pethe's disclosures relating to gate contact vias 342A/342B (**second contacts**) further confirms that the gate contact vias 542A/542B

are **monolithically formed structures**. The formation of gate contact vias 542 share the same formation processes as gate contact vias 342 (same feature but deeper only because of recessed spacers 520). EX1005, 12:54-67; *id.* 11:23-42, 9:1-43, 7:15-34; EX1002, ¶¶218-22. Indeed, gate contact vias 542A/542B (**second contacts**) is each formed by filling an opening with a single metal contact structure 540. EX1005, FIG. 5B (above), 12:54-67, 10:37-11:22.

6. Claim 8

Pethe discloses these limitations. EX1002, ¶¶223-30. Metal (0) portion 550 includes **a plurality of third contacts** and **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and on gate contact vias 542A, 542B (**parts of the second contacts**).

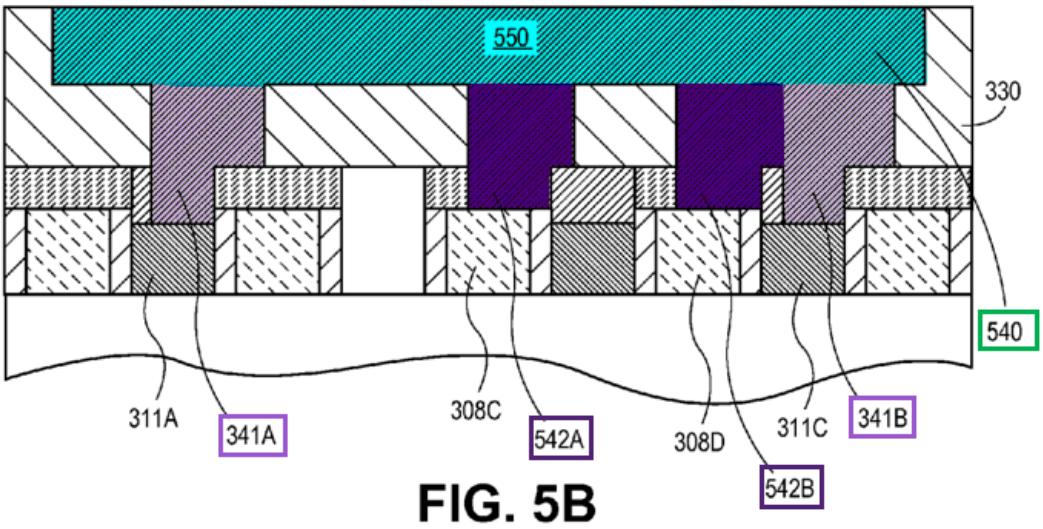


FIG. 5B

EX1005, 12:54-13:12; EX1002, ¶224.

Pethe explains that "metal contact structure 540 **is formed in a metal (0) trench and via openings**." EX1005, 12:54-56. Also that "metal (0) portion" is "550," and 540 also comprises "trench contact vias" (341) and "gate contact vias" (542), which contact trench contacts (311) and gate stack structures (308) respectively. EX1005, 12:56-62. Consistent with this disclosure, 550 is **monolithically** formed (as part of 540) and as annotated above in Figure 5B **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and gate contact vias 542A, 542B (**parts of the second contacts**). EX1002, ¶225.

A POSITA would have understood 550 comprises a metal line interconnect structure with **a plurality of third contacts** (e.g., metal lines) each connecting to **parts of the first and second contacts**. EX1002, ¶226; EX1005, 11:26-31. 550 is formed in metal (0) trench, and it was known that "metal (0)" was understood as an interconnect structure of metal lines in the metal (0) layer. EX1002, ¶¶227-30. Pethe refers to structures above trench contact vias and gate contact vias as a "metal interconnect" structure. EX1005, 3:50-4:8, 4:56-5:10, 11:59-64. Such teachings confirm that "metal interconnect" at the metal (0) layer would have been understood to include a networks of metal lines. EX1002, ¶227-30.

7. Combination of Pethe's Embodiments

As explained, in discussing Figure 5, Pethe does not repeat details/discussions related to similarly labeled features in Figure 3 (with same or similar labels), *e.g.*, substrate 302, ILD region 323, dielectric layer 330, trench contact vias 341A/341B, trench contacts 311A/311C, and cap layer 522 (same as cap layer 322 but wider because of recessed spacers 520), gate contact vias 542A/542B (same as gate contact vias 342A/342B), and metal (0) portion 550 (same as metal (0) portion 350). EX1005, FIGs. 3A-3F, 5A-5B, 2:3-63, 7:9-11:42, 12:22-13:12; EX1002, ¶¶231-33.

In addition to relying on Pethe's disclosure of Figure 5B structure including the discussions of the common features, a POSITA would also found it obvious to consider and apply the teachings of Figure 3 when forming/configuring Figure 5B's structure (as discussed in §§VI.A.1-VI.A.6), and would have had a reasonable expectation of success in doing so. EX1002, ¶¶234-35. Indeed, a POSITA would have recognized/appreciated that Pethe relates/references common features between embodiments in describing the disclosed invention (*e.g.* EX1005, 2:50-63, 4:39-42, 5:15-34, 7:22-25, 9:15-20, 11:23-25, 12:15-31, 12:39-42, 12:48-53, 15:39-41), and thus been motivated to incorporate such combined teachings to yield the predictable result of a structure as discussed above for claims 1-5 and 8. EX1002, ¶236; §§VI.A.1-VI.A.6. *KSR*, 550 U.S. at 416.

B. Ground 2: Claims 6 and 7 Are Obvious Over Pethe

1. Claim 6

Pethe discloses/suggests this limitation. EX1002, ¶¶237-53; §VI.A.1 (Claim 1).

Pethe's disclosed semiconductor devices are not limited to single-gate transistors, but can be applied to non-planar, multi-gate transistors (e.g., "TRI-GATES," "FIN-FETs") known to include fins. EX1005, 5:35-39, 14:8-11, 1:27-35; EX1002, ¶240. Pethe refers to forming "fins in a bulk semiconductor substrate" (EX1005, 17:17-18), refers to a non-planar diffusion or active region in Figures 1C, 2C, and 4 structures as "a fin structure" (*id.*, 3:60-67, 4:65-5:3, 11:49-52) and contemplates Figure 2's structure 200 as a "fin-FET" or "tri-gate" device (*id.*, 5:35-39); *id.*, 6:7-12 ("fin active regions").

Notwithstanding Pethe's teachings, it would have been obvious to a POSITA in light of Pethe's teachings/suggestions to configure Figure 5B's structure with at least one fin structure disposed on the substrate. EX1002, ¶¶241-53. A POSITA would have been motivated to consider/implement fin structure features similar to those discussed for FIG. 2 (or FIGs. 1, 4 and other embodiments) to apply Figure 5B's structure to multi-gate transistor (e.g., FinFET, TRI-GATE) configurations, consistent with the known use of fin structures. *Id.* Pethe recognizes "multi-gate

transistors" are "fundamental building blocks of microelectronic circuitry," "fabricated by conventional processes," and "prevalent as device dimensions continue to scale down." EX1005, 1:27-45; EX1002, ¶¶241-42. Such "multi-gate transistors" are "consequent[ial]" to address "scaling of features in integrated circuits"—the "driving force behind an ever-growing semiconductor industry." EX1005, 1:14-19, 1:36-42.

Pethe also explains for Figures 5A-5B, the gate structure "may include a gate dielectric layer and a gate electrode, **as described above in FIG. 2**," which discloses a multi-gate transistor having a fin structure. EX1005, 12:39-42. Figure 2's gate structure is for use with and "disposed over the non-planar diffusion or active region 204C," which is identified as a "fin structure." EX1005, 4:62-5:5; FIG. 2C (below showing "tri-gate transistor" including gate structure comprising gate electrode 250/ gate dielectric layer 252 disposed over fin structure 204C). EX1002, ¶¶243.

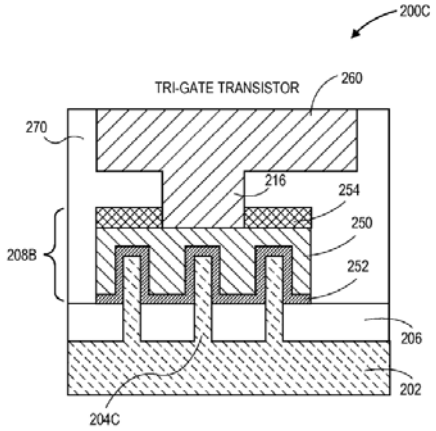


FIG. 2C

Thus, a POSITA would have been motivated, and found obvious, to configure Pethe's Figure 5B structure with a fin structure disposed on top of the substrate, consistent with Pethe's teachings. EX1002, ¶¶244-53. A POSITA would have had reasonable expectation of success in implementing such a modification, especially given it would have involved "fundamental" semiconductor device structure and "conventional" process technologies within a POSITA's capabilities and contemplated by Pethe. EX1005, 1:27-45; EX1002, ¶¶244-53. Such guidance/suggestions would have led a POSITA to configure Figure 5B's structure to include at least one fin structure disposed on the substrate as claimed. *Id.*

2. Claim 7

Pethe discloses/suggests these limitations. EX1002, ¶¶254-68. Pethe discloses trench contacts 311A, 311C **disposed between each S/D region and each first contact** (discussed above for elements [1.f] (§VI.A.1.f) and [1.g] (§VI.A.1.g)).

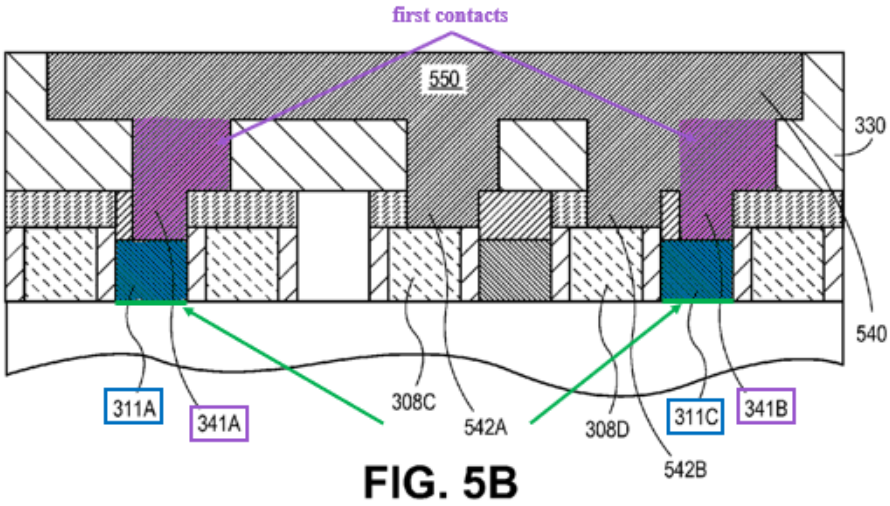


FIG. 5B

EX1002, ¶255.

Trench contact vias 341A, 341B are electrically conductive vias to trench contacts 311A, 311C, which are electrically conductive contacts to the source/drain regions. EX1005, 11:23-31, 9:29-10:36 (Figure 3D elements similarly labeled in Figures 5A-5B). Vias 341A, 341B are formed in the same process as metal (0) portion 550, which are electrically connected in the Figure 5B structure. *Id*. Thus, electrical connection to the source/drain regions relies on a conductive path through trench contact vias 341A, 341B, and trench contacts 311A, 311C, which are self-aligned contacts. EX1002, ¶256.

Notwithstanding Pethe's teachings, it would have been obvious to a POSITA at the time to include a salicide layer disposed between each S/D region and each first contact in Figure 5B's structure. EX1002, ¶¶260-68.

For example, regarding Figure 2's structure, Pethe teaches that "all of [trench] contacts 210A and 210B" may be composed of "a silicide material,"[12] and Golonzka teaches the same. EX1005, 6:53-59, 4:33-36, 11:26-31, 7:39-41; EX1006, [0051]. Pethe also incorporates features from Figure 2's embodiment into the features described for the Figure 5B structure. EX1005, 12:39-41; *id.*, 7:22-25, FIG. 3A; EX1002, ¶¶261-62.

Thus, having reasons to look to Figure 2's embodiment, a POSITA would have been motivated to configure trench contacts 311A-311C (above source/drain region) in Pethe's Figure 5B structure to include a salicide layer. EX1005, 7:39-41; EX1002, ¶263. A POSITA would have appreciated such configuration would have reduced electrical resistance. EX1002, ¶¶264-68; EX1009, 13:8-10; EX1013, 4:63-67, 3:56-58; EX1020, 585.

Thus, a POSITA would have been motivated, and found obvious, to configure the modified Figure 5B structure with a salicide layer disposed in trench contacts between each source/drain region and trench contact vias 341. EX1002, ¶¶264-68.

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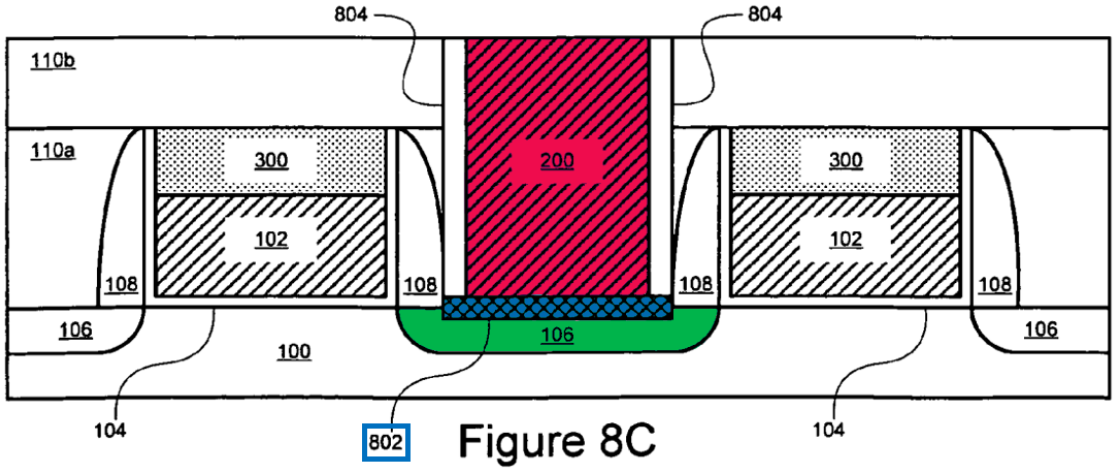
[12] "Salicide" generally refers to a self-aligned "silicide," which would be understood as a silicide formed in a region without photolithography, as implemented in trench contacts 311A-311C. (EX1005, 7:35-46; EX1002, ¶¶257, 259.)

A POSITA would have had a reasonable expectation of success in implementing such a modification given Pethe's direction to Figure 2's structure and because it would have involved application of known semiconductor structure materials/processes contemplated by Pethe, predictably leading to Pethe's Figure 5B structure including **a salicide layer disposed between each S/D region and each first contact**, as claimed. *Id.*.

C. Ground 3: Claim 7 Is Obvious Over Pethe in View of Bohr

1. Bohr

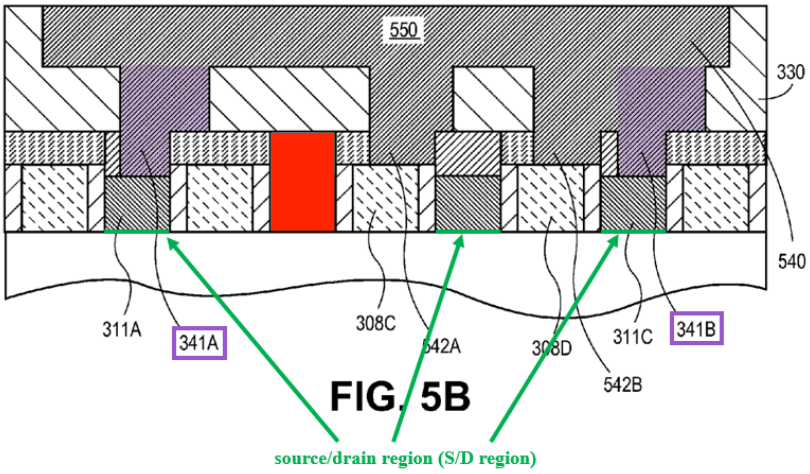
Bohr describes systems/methods of reducing likelihood of contact-to-gate shorts during fabrication of MOSFET transistors. EX1009, 2:16-18; *id.*, Abstract, 1:5-2:37. In particular, Bohr teaches self-aligned contacts for a FET utilizing a salicide layer between a source/drain and contact. An example of this contact is shown below and comprises silicide layer 802 formed between trench contact 200 and source/drain diffusion region 106.



Id., FIG. 8C (annotated); EX1002, ¶¶279-83; EX1009, FIG. 8A, 12:61-66 (before trench contact 200 formation, silicide layer 802 is formed at contact trench opening 800 bottom (later filled to become trench contact 200).

2. Combination of Pethe and Bohr

As explained (§VI.A), Pethe teaches trench contact vias 341A, 341B (**first contacts**) and source/drain regions, below:



EX1005, 12:54-67; EX1002, ¶¶269-70; §§VI.A.1.f (S/D region), VI.A.1.g (first contacts). Pethe's trench contact vias 341A, 341B are electrically conductive vias to trench contacts 311A, 311C, which are electrically conductive contacts to the source/drain regions. EX1005, 11:23-31, 9:29-10:36; EX1002, ¶¶270-72.

In addition to the express disclosure discussed in §VI.A.1, it would have been obvious to implement a **salicide layer disposed between each S/D region and each first contact** in Pethe's Figure 5B structure in view of Bohr. EX1002, ¶¶273-97.

As explained above, Bohr teaches forming a silicide layer (EX1009, 12:61-13:10 ("deposition process…annealing process…") and using a salicide layer between a source/drain and contact (*id.*, FIGs. 8A-8B). §VI.C.1. Since Bohr's silicide is a self-aligned silicide, Bohr teaches a salicide layer disposed between a source/drain region and trench contact. *Id.*; EX1009, 12:61-13:8; EX1002, ¶¶272-74.

Bohr's teachings are consistent with a POSITA's knowledge that it was known to include a salicide layer between a source/drain and contact, such as in self-aligned trench contacts. EX1002, ¶¶274-78; EX1020, 157-58 (conventional salicide processes involving metal deposition/annealing over source/drain regions), FIG. 5.39 (below); EX1001, 4:22-33.

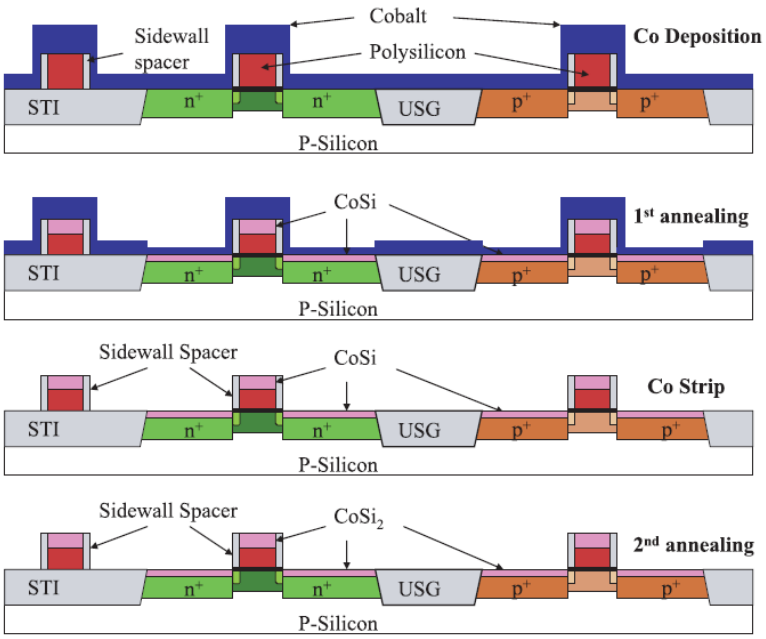


Figure 5.39 Self-aligned cobalt silicide process.

Like Pethe, Bohr discloses features related to the formation/configuration of semiconductor structures, including FETs. *E.g.*, EX1005, 12:32-13:12, 13:63-14:11, *id.*, 9:29-10:36, 11:23-31; EX1009, 1:5-36, 4:5-11, 12:61-14:3; EX1001, 1:9-13, 5:66-6:37. Thus, a POSITA would have considered Bohr's teachings when implementing Pethe's Figure 5B structure. EX1002, ¶279.

A POSITA would have been motivated to combine teachings of Pethe (*e.g.*, use of trench contacts and source/drain regions,) and Bohr (*e.g.*, use of self-aligned silicide (i.e., salicide layer) disposed between a source/drain region and trench

contact) to improve Pethe's structure by *e.g.*, reducing the electrical resistance between the S/D region and trench contact.[13] EX1002, ¶¶277-97.

Indeed, consistent with a POSITA's knowledge, Bohr teaches advantages of implementing a salicide layer between a source/drain and contact (*e.g.*, to "reduce[] the electrical resistance between the later formed trench contact…and the diffusion region…"). EX1009, 13:8-10; EX1013, 4:63-67, 3:56-58. Thus, a POSITA would have looked to achieve similar benefits by using a salicide layer between Pethe's S/D region and trench contacts in Pethe's Figure 5B structure. EX1002, ¶¶293-97.

A POSITA would have had the skill, rationale, and knowledge in implementing, and expectation of success in achieving, the above-discussed Pethe-Bohr combination. EX1002, ¶¶289-97. As explained, Bohr teaches the known advantages of using a salicide layer between a diffusion region and trench contact in a semiconductor structure similar to those contemplated by Pethe (e.g., FET

[13] Bohr has a common assignee (Intel) and multiple overlapping inventors with Pethe, which weighs in favor of finding a motivation to combine the two references. *See, e.g.*, *Abbot Vascular, Inc. v. Flexstent*, IPR2019-00882, Paper 48, 28-29 (Oct. 2, 2020); *Black v. CE Soir Lingerie Co.*, No. 2:06-CV-544, 2008 WL 3852722, at *14 (E.D. Tex. Aug. 15, 2008).

structures). Ex.1009, 1:5-36, 4:5-11, 12:61-13:10; EX1005, 12:32-13:12, 13:63-14:11; EX1002, ¶¶289-97.

The combination of Pethe and Bohr would have involved application of known technologies (e.g., known use salicide layers between source/drain regions and trench contacts) (EX1013, 4:63-5:30, 5:48-64, 9:5-30, 10:7-35; EX1020, 157-58) according to known methods (e.g., known deposition/annealing processes) to yield the predictable result of a semiconductor structure (Pethe's Figure 5B) including a salicide layer formed over the source/drain region and between trench contacts 311A/311C (and thus trench contact vias 341A/341B (**first contacts**)) so the resistance between the source/drain region and (trench contacts 311A/311C (and thus "**first contacts**" 341A/341B) can be reduced. EX1002, ¶297; *KSR*, 550 U.S. at 416.

3. Claim 7

Pethe in view of Bohr discloses/suggests these limitations. EX1002, ¶¶269-97.

As discussed in §VI.C.2, it would have been obvious to implement a **salicide layer disposed between each S/D region and each first contact** in Pethe's Figure 5B structure in view of Bohr. §§VI.C.1-VI.C.2.

For the reasons discussed in §§VI.C.1-VI.C.2, a POSITA would have been motivated, and found obvious, to modify Pethe's Figure 5B structure to achieve a salicide layer disposed between its source/drain region and trench contact consistent with Bohr's teachings and a POSITA's state of art knowledge. EX1002, ¶¶269-97; §§VI.C.1-IX.C.2. Thus, the Pethe-Bohr combination discloses and/or suggests claim 7. *Id.*

D. Ground 4: Claims 8-9 Are Obvious Over Pethe in View of Huang

1. Huang

Huang discloses methods for forming a semiconductor memory device comprising FETs. EX1008, ¶¶3-5, 7-8. Huang teaches the use of dual-damascene processing to provide M1 lines and M0 vias in forming the device. EX1008, ¶17, FIG. 8A. Huang describes M1 layer's metal lines 74 and M0 vias 72 "for connecting to contact plugs 60 and 62," shown below.

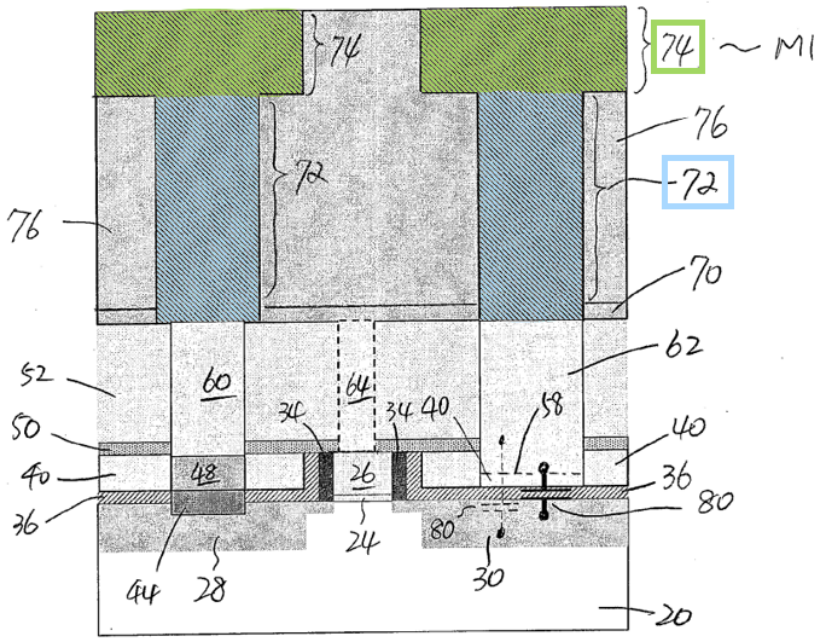


Fig. 8A

EX1002, ¶¶313-316; EX1008, ¶17. "M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces being formed between M0 vias 72 and respective overlying metal lines 74." *Id*.

2. Combination of Pethe and Huang

Pethe's metal (0) portion 550 includes **a plurality of third contacts** and **disposed on** trench contact vias 341A, 341B (**parts of the first contacts**) and on gate contact vias 542A, 542B (**parts of the second contacts**.) §VI.A.6.

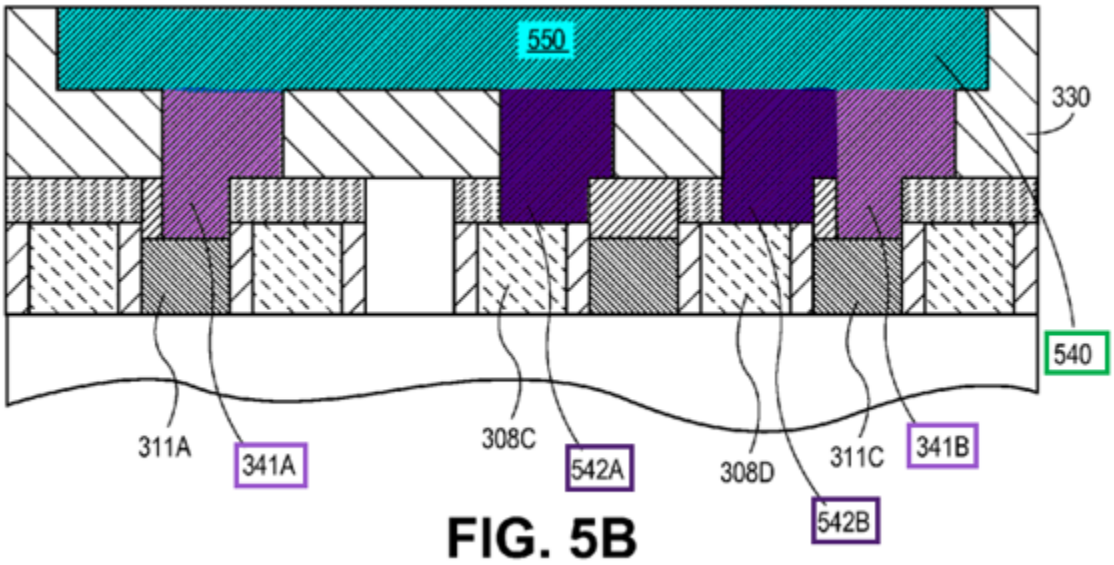


FIG. 5B

EX1005, 12:54-13:12; EX1002, ¶¶299-300.

In addition to the structure described in §§VI.A.1-VI.A.3, VI.A.6, it would have been obvious to implement "**a plurality of third contacts**…" as recited in claims 8-9 in Pethe's Figure 5B structure (§VI.A.3) in view of Huang. EX1002, ¶301.

Like Pethe, Huang discloses features related to the formation and configuration of semiconductor structures, including FETs. *E.g.*, EX1005, 8:24-51, 9:29-43, 11:23-42, 12:32-13:12, 13:63-14:11, *id.*, 9:29-10:36, 11:23-31; EX1008, ¶¶2-8, 17; EX1001, 1:9-13, 5:66-6:37; EX1002, ¶317. In particular, Huang teaches the use of dual-damascene processing to provide M1 lines and M0 vias. (§VI.D.1; EX1008, ¶17 ("M0 vias 72 and metal lines 74 may be formed using a dual-damascene process, and hence no noticeable interfaces being formed between M0

vias 72 and respective overlying metal lines 74").) *Id.*; EX1002, ¶¶313-15. Thus, Huang discloses forming via hole structures and corresponding trace structures (*e.g.*, M1 lines) comprising the same material that contact each other directly. EX1002, ¶316.

Consistent with Huang, a POSITA was aware to form metal (1) ("M1") lines and metal (0) vias (above metal (0) lines and device contacts) using a dual-damascene process, particularly in BEOL processing. EX1002, ¶¶302-07, 320-31; EX1016, ¶89; EX1015, 55-56; EX1014, FIG. 15-3, 674-76 ("sequence is repeated for the next level of metal").

Thus, a POSITA would have considered Huang's teachings when implementing Pethe's Figure 5B's structure. EX1002, ¶312-20; §II.D.

A POSITA would have been motivated, and found obvious, to modify Pethe's metal interconnection in Pethe's structure to include, above its metal (0) portions 550, M1 lines and M0 vias, consistent with Huang's teachings. EX1002, ¶¶301-31; §§VI.D.3.

Huang contemplates placing upper metal lines and vias over lower metal lines (Pethe's metal (0) portion 550)—explaining that "[i]n subsequent process steps, more metal layers (not shown) may be formed over metal layer M1." EX1008, ¶17. A POSITA would have recognized that Pethe provides a metal (0) portion, but does

not describe any BEOL interconnection, which a POSITA would have understood is critical to create an IC with ever-more capacity. EX1005, 1:14-26; EX1002, ¶319. A POSITA would have been motivated, and found it obvious, to combine Pethe's and Huang's teachings to achieve a dual-damascene process to provide M1 lines and M0 vias to form more complex and higher-capacity semiconductor devices using Pethe's structure. EX1008, ¶17, FIG. 8A; EX1005, 1:14-26; §II.D; EX1002, ¶319.

A POSITA was aware of advantages with dual-damascene to provide M1 lines and M0 vias, as taught by Huang, including simplified fabrication, no metal etching requirement, and reduced electromigration failure risk. EX1002, ¶¶308-11; EX1020, 345-49, 464, 497-98, 517-18, 574-79; EX1014, 695, 698; EX1015, 56, 92. Accordingly, a POSITA would have looked for ways to connect Figure 5B's structure to the M1 layer with similar advantages, as taught by Huang. *Id*. A POSITA thus would have found it obvious to use dual-damascene to provide M1 lines and M0 vias over Pethe's Figure 5B's M(0) portion 550. *Id.*

A POSITA would have had the skill, rationale, and knowledge in implementing, with a reasonable expectation of success, the above-discussed Pethe-Huang combination. EX1002, ¶¶319-31. Huang teaches the known use of dual-damascene to achieve additional metal line(s) and via(s) over a metal (0) portion of a semiconductor structure, like that taught by Pethe. *Supra*; EX1002, ¶¶313-15. The

Pethe-Huang combination would have involved application of known technologies/techniques (*e.g.*, dual-damascene to form M1 lines and M0 vias) to yield the predictable result of a more complex, higher-capacity semiconductor structure (Figure 5B). EX1002, ¶331; *KSR*, 550 U.S. at 416.

3. Claims 8 and 9

Pethe in view of Huang discloses/suggests these limitations. EX1002, ¶¶298-333.

Grounds 1-2 demonstrate that Pethe discloses/suggests claims 1-8. §§VI.A-VI.B. However, for reasons explained in §VI.D.2, it would have been obvious to implement "**a plurality of third contacts**…" in Pethe's Figure 5B structure (§VI.A.3) as recited in claims 8-9 in view of Huang. EX1002, ¶301-31; §§VI.D.1-VI.D.2.

In light of Huang's teachings and a POSITA's state of art knowledge as discussed in §§VI.D.1-VI.D.2, Pethe's Figure 5B structure would have been predictably modified to include, above its metal (0) portion 550, M1 lines and M0 vias, consistent with Huang's teachings using dual-damascene processes known in the art. EX1002, ¶¶327-33; §§VI.D.1-VI.D.2.

As a result, the modified Figure 5B structure would have included a **plurality of third contacts** (*e.g.*, parts of newly formed M1 lines above Pethe's M0 line (550)

and associated M0 vias interconnecting the M1 and M0 lines formed based on Huang's teachings) **disposed on parts of the first contacts** (*e.g.*, parts of 341A/341B) **and on parts of the second contacts** (*e.g.*, parts of 542A/542B), as in claim 8. *Id.* Moreover, **each third contact** (in the modified Figure 5B structure) would have comprised **a via hole structure (M0 vias) and a trace structure (**parts of the newly formed M1 lines (EX1001, 5:48-53 (trace structure may be "lines")), which would **comprise the same material and contact each other directly** (as in claim 9) given they are formed using dual-damascene processing like that taught by Huang, which would also result in **each third contact** (above) being a **monolithically formed structure** (as in claim 8). EX1002, ¶¶327-33; §VI.D.2.

E. Ground 5A and 5B: Chang anticipates (Ground 5A) and Renders Obvious (Ground 5B) Claims 1-2

Because Chang is in the same field (MOSFETs) and reasonably pertinent to a problem the '747 Patent purports to address (e.g., MOSFET fabrication), Chang is analogous art. EX1001, 1:9-2:9, 2:39-42, 5:31-6:37; EX1007, ¶¶27-35, 46-49, 52, 89-92, 107, 111-14; EX1002, ¶64.

Chang teaches two approaches in forming self-aligned contacts and SRAMs containing such contacts: (1) Figures 1-16 (no gate protection option) and (2) Figures 17-27 (with gate protection option). EX1007, ¶¶51-52. Chang teaches "SRAM containing transistor structures with gate-protected self-aligned contacts" in Figures

24-27. EX1007, ¶107. Chang discloses its SRAM in the context of "self-aligned contacts" with a "gate-protection option," which "is described with respect to FIGS. 17-27." *Id.*, ¶52.[14] Specifically, "FIGS. 17 through 23 show wafer cross sections illustrating operations in connection with the gate-protect option with respect to forming self-aligned contacts." EX1007, ¶89. Figures 24-27 show an SRAM with those contacts. *Id.*, ¶107 ("FIG. 24 is a top view of a layout 1400 of an SRAM containing transistor structures with gate-protected self-aligned contacts…cross sections of the SRAM layout 1400 are shown in FIGS. 25, 26, and 27."); EX1002, ¶¶64-67.

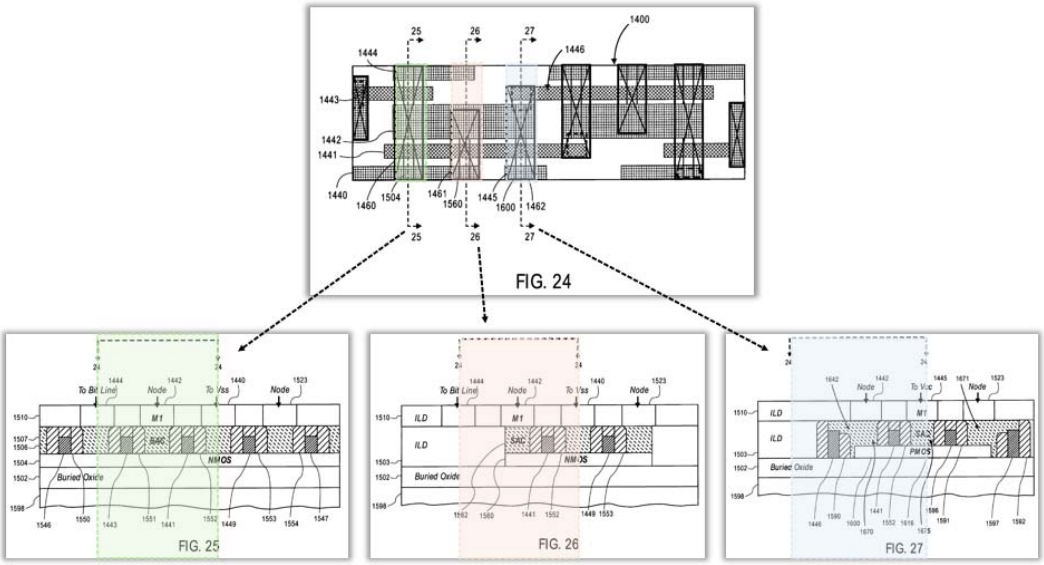
1. Claim 1

a) [1.a]

To the extent claim 1's preamble is limiting, Chang discloses it. EX1002, ¶¶334-36; §§VI.E.1.b-VI.E.1.i.

Chang's "SRAM containing transistor structures with gate-protected self-aligned contacts" in Figures 24-27 is **[a] semiconductor structure**. EX1007, ¶107, FIGs. 24-27 (showing same structure). *Id.*

[14] Chang discloses an alternative "no gate-protect option…in reference to FIGS. 6 through 16." EX1007, ¶51.



b) [1.b]

Chang discloses this limitation. EX1002, ¶¶337-40. Chang's silicon substrate 1598 is **a substrate**, below:

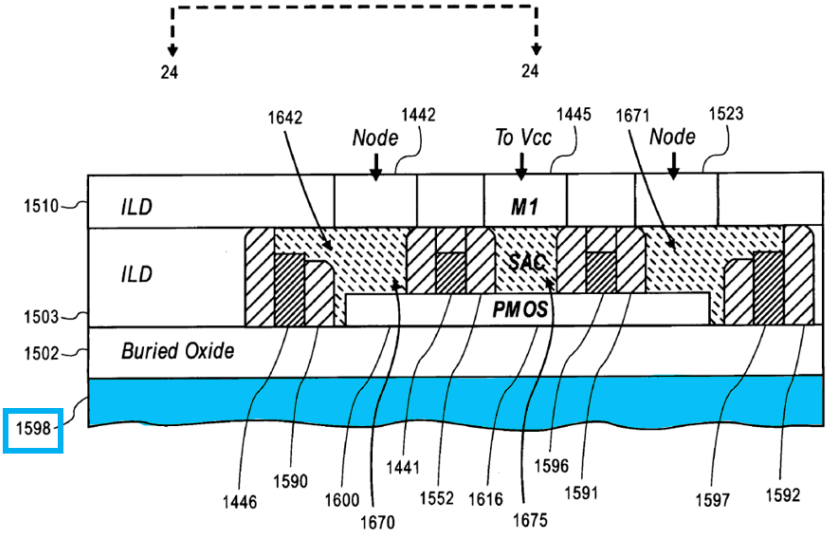


FIG. 27

EX1007, ¶110.

The combination of silicon substrate 1598 and buried oxide 1502 is also a "substrate" on which SRAM transistor structures are formed. EX1002, ¶¶338-39.

c) [1.c]

Chang discloses this limitation. EX1002, ¶¶341-45. Chang's "interlayer dielectric layer 1503" (**first dielectric layer**) is **disposed on the substrate**, below:

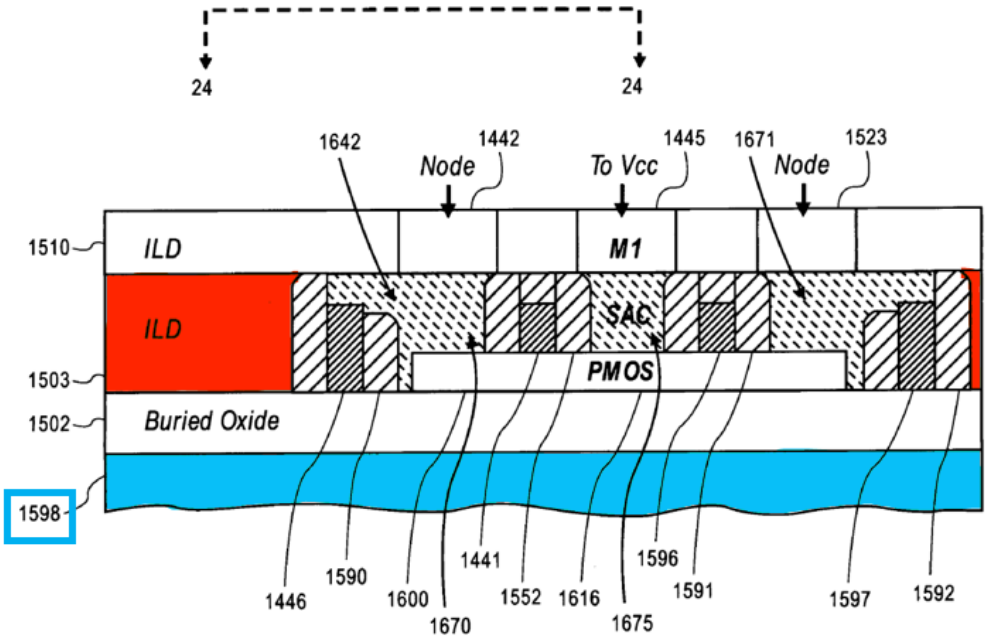


FIG. 27

EX1007, ¶112, FIG. 27; EX1002, ¶¶342-45. ILD 1503 is disposed on silicon substrate 1598 and on the substrate comprising silicon substrate 1598 and buried oxide 1502. *Id.*; §VI.E.1.b.

d) [1.d]

Chang discloses this limitation. EX1002, ¶¶346-59. Chang's gates 1441, 1443, 1446, 1449, 1546-47, and 1596-97 are eight **metal gates** (**at least two**), below:

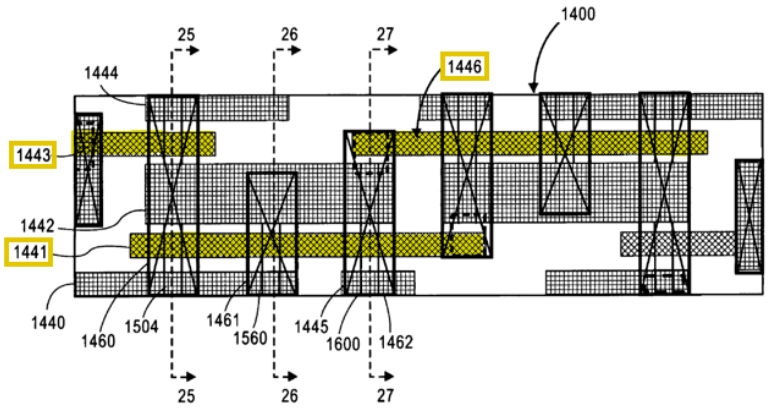


FIG. 24

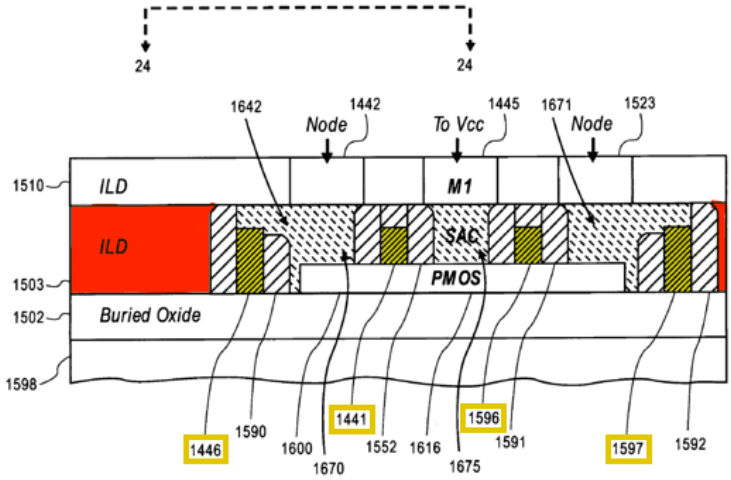


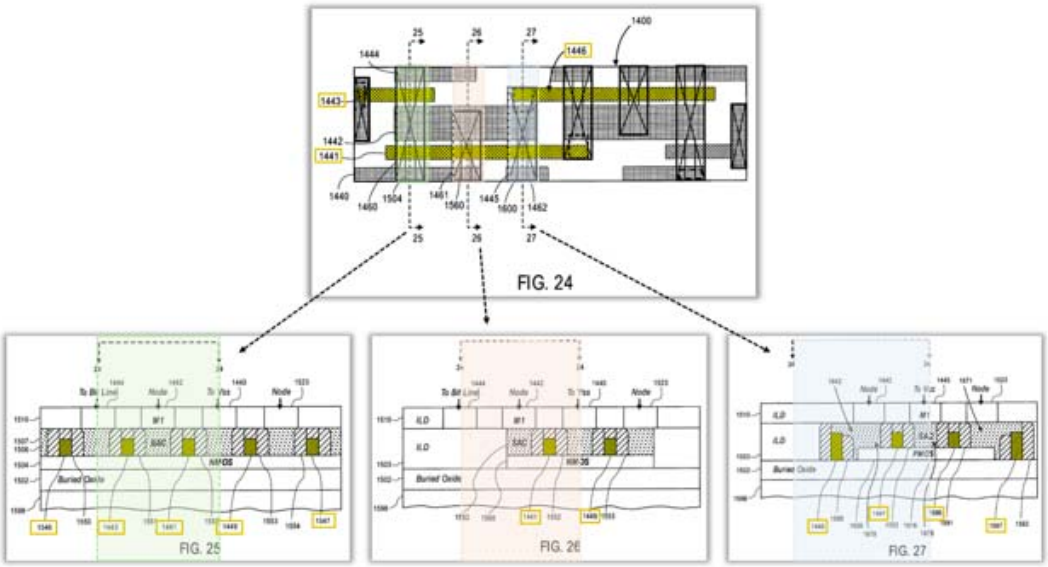
FIG. 27

EX1007, FIGs. 24, 27, ¶¶47, 111-12, 114; EX1002, ¶347.

Chang's gates are all **metal**. EX1002, ¶¶348-54. Chang's invention is "applicable to transistors with **metal** gates," and "is not restricted to a particular way

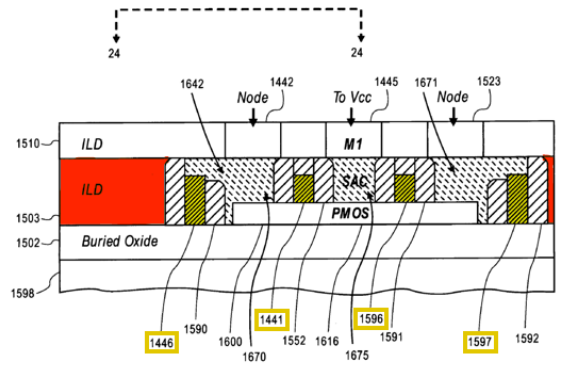
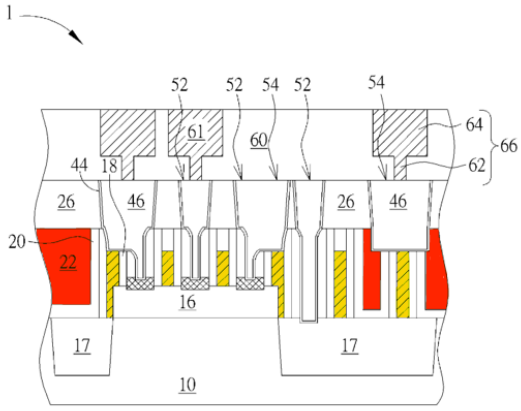
the **metal** gates are formed." EX1007, ¶¶47, 114. Chang refers to gates 1441, 1449 in Figures 24-27 as "metal gates," and a POSITA would have understood all the gates (including gates 1441, 1449) disclosed in Chang (commonly formed in the same process using the same material) are metal gates. EX1002, ¶¶349-54; EX1007, ¶111.

Figures 24-27 SRAM incorporates the self-aligned contacts formed by Figures 17-23's processes. Chang refers to all the gates in Figures 17-23 as metal gates, and process step in Figure 17 as "Metal Gate Recess Etch" (EX1007, FIG. 17, ¶90; *id.*, ¶¶27-35, 52, 89, 107, FIGs. 24-27 (below)), and Chang does not describe using different materials for the gates in the Figure 24-27 structure. Thus, the Figures 24-27 SRAM's gates are metal gates.



EX1002, ¶¶354, 64-67.

Chang's metal gates are **disposed in** interlayer dielectric layer 1503 (**first dielectric layer**), as shown in Figure 27, consistent with that described in the '747 patent (comparatively shown below). EX1007, ¶112 ("The interlayer dielectric layer 1503 includes the...gate structures.");

 FIG. 27	 FIG. 9
Chang	**EX1001**

EX1002, ¶¶355-56.

Notwithstanding (and in addition to) the above-discussed disclosures, it would have also been obvious to a POSITA in view of Chang's disclosures to configure the gates in the Figure 24-27 structure to be metal (relevant to **Ground 5B**). EX1007, ¶¶27-35, 52, 89-90, 107, 111; EX1002, ¶¶357-59. A POSITA would have understood all the gates, including gates 1441, 1449, are conventionally using the same process with the same material, just like the process described in FIG. 5, which teaches forming all the gates in a single metal gate process (EX1007, ¶46). Thus, a

POSITA would have found it obvious to form all the gates as metal gates using FIG.5's process. Such process would simplify the fabrication process of Figures 24-27 SRAM, instead of introducing unnecessary complexity and cost by providing gates of different materials. EX1002, ¶¶357-59. Considering and implementing such knowledge/techniques/teachings would have predictably yielded Chang's Figure 24-27 structure having a plurality of metal gates, as recited in limitation [1.d]. *Id*.

e) [1.e]

Chang discloses this limitation. EX1002, ¶¶360-67. Chang's "gate structures 1552 and 1591 include spacers along with silicon nitride caps for the respective gates 1441 and 1596." EX1007, ¶112. Spacers 1552 are **disposed on two sides of** gate 1441 (the metal gate). *Id.*, FIG. 27 (below).

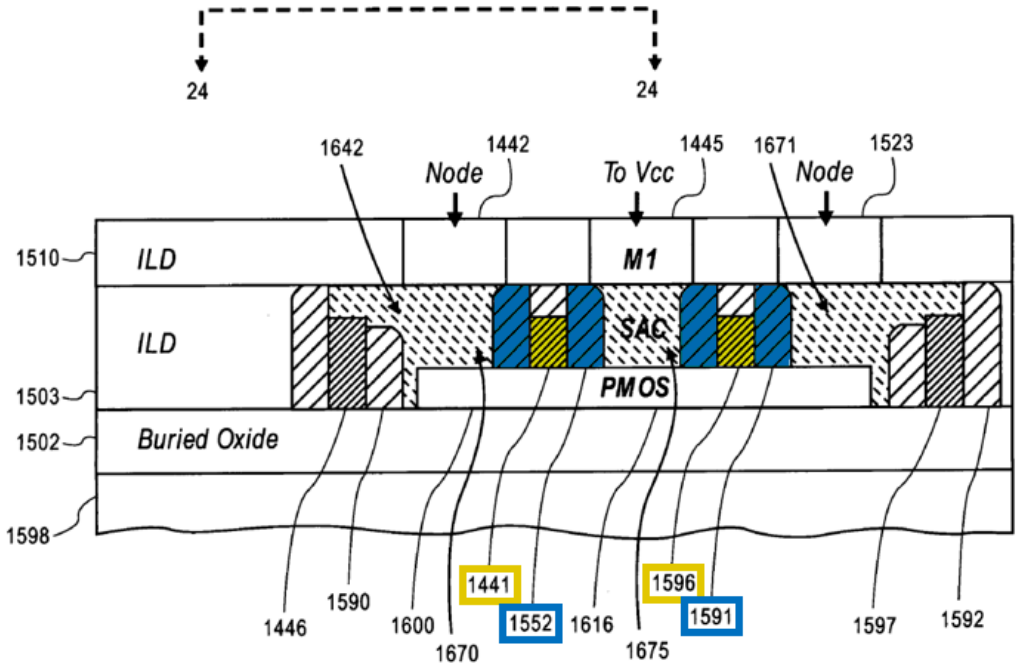


FIG. 27

EX1002, ¶361.

Gate structures 1552 and 1591 include spacers having **a truncated top surface**. EX1002, ¶¶362-67. Chang explains the deposition and planarization of its self-aligned contacts regarding FIGs. 19-20 (below), which entails depositing a metal to fill the open areas (*e.g.*, 780-82). EX1007, ¶¶94-95. Afterwards, a polishing or etch operation is performed "to **planarize the contact metal down to level 737**…to form contact areas 820, 821, and 822," where level 737 is "**slightly below the original top level 738**" and "**tops of spacers 710 through 713** and silicon nitride gate caps 760 and 761 are **not covered by the**

contact metal after the planarization…." EX1007, ¶¶94-95. Thus, contact metal areas 820/821/822 are not electrically interconnected.

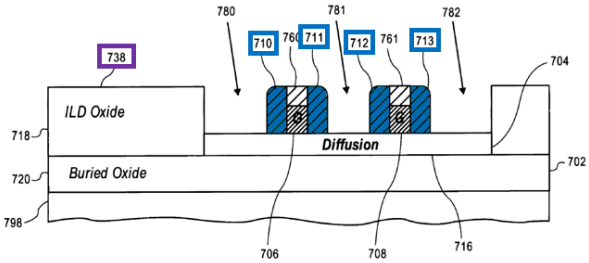


FIG. 19

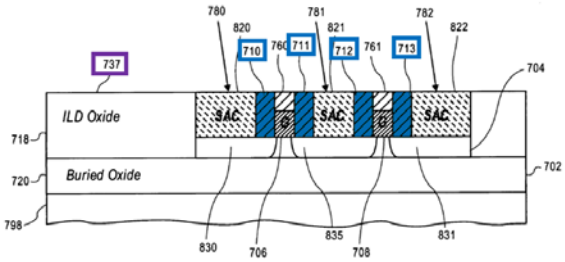


FIG. 20

EX1002, ¶363.

The polishing lowers the level of the wafer top from 738 (FIG. 19) to 737 (FIG. 20). EX1007, ¶¶94-95. The polishing removed spacer material, providing **a truncated top surface**. EX1002, ¶364.

Given Chang's teachings (including regarding Figures 17-23 illustrating forming self-aligned contacts, and Figures 24-27 showing an SRAM with those contacts), a POSITA would have understood the spacers in Figures 24-27 have a truncated top surface. §VI.E (discussing Chang); EX1002, ¶¶365-67; EX1007, ¶52 ("self-aligned contacts" with "gate-protection option" "is described with respect to FIGS. 17-27"), ¶¶89, 107, FIGS. 20, 27 (below).

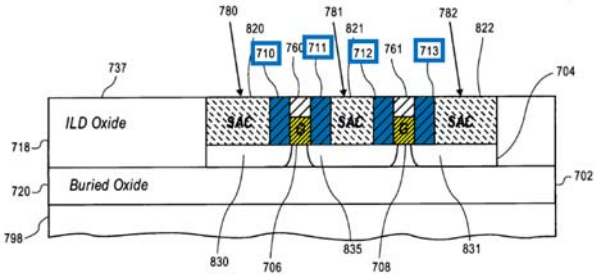


FIG. 20

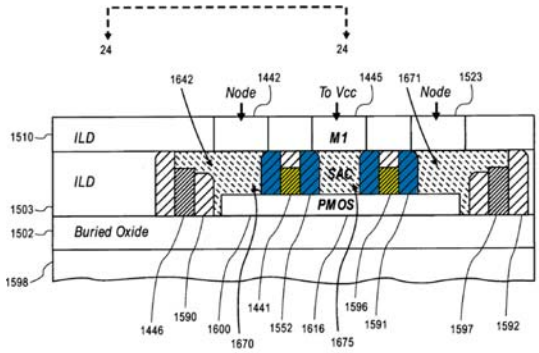


FIG. 27

f) [1.f]

Chang discloses this limitation. EX1002, ¶¶368-83. Chang's embodiments are described in context of known transistor features, e.g., "gate structures" / "drain and source regions"—known FET features, and a SRAM that includes multiple FETs. EX1007, Abstract, ¶¶39-41, 45-48, 63, 71, 89-90, 96, 98.

Figure 27's transistor structures include "gate structures" and a "diffusion region" ("PMOS region"/"PMOS layer") 1600. EX1007, ¶¶112-113. A POSITA would have understood in context of Chang's disclosures that layer 1600 contains source and drain regions (shown below), each understood as a source/drain region (S/D region). EX1007, ¶¶112-13, 96-98; EX1002, ¶¶369-71. Each such S/D region is **disposed between two metal gates**.

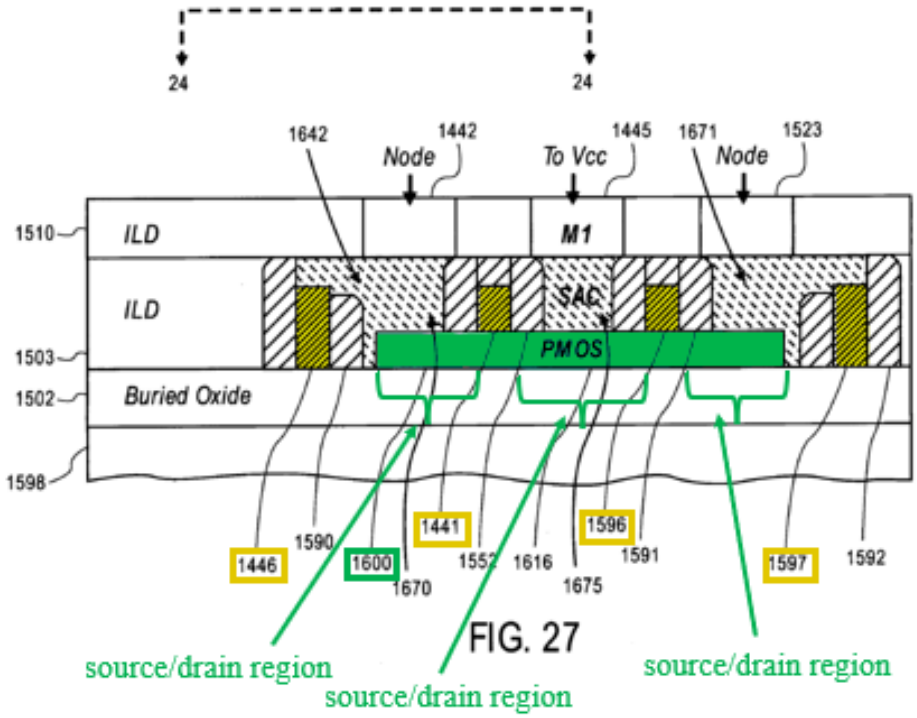


FIG. 27

EX1007, ¶¶112-13, 96-98; EX1002, ¶¶371-75.

Regarding Figure 20 (below), Chang describes "diffusion area 704" including drain regions 830, 831 and source region 835, which is **a source/drain region (S/D region) disposed between two metal gates** 706, 708. As shown above, the **source/drain region (S/D region)** of diffusion region 1600 would be in the corresponding locations.[15]

[15] The SRAM of Figures 24-27 has source/drain region (S/D region) at least for similar reasons discussed for element [1.e] (§VI.E.1.e).

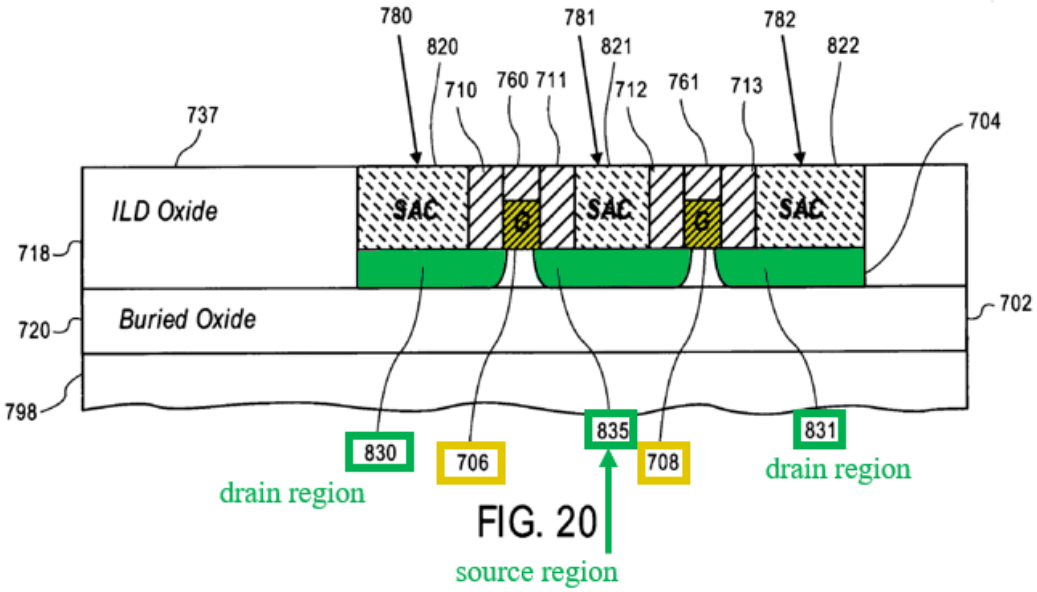


FIG. 20

EX1002, ¶¶372-74.

Thus, in context of Chang's teachings, Figure 27's diffusion layer 1600 would have included a **source/drain region (S/D region)**, as described above, including a **source/drain region (S/D region) disposed between the two metal gates 1441, 1596**. EX1002, ¶375.

Notwithstanding (and in addition to) the above-discussed disclosures, it would have been obvious to a POSITA in view of Chang's disclosures to configure Figure 24-27's structure to include an S/D region disposed between two metal gates (relevant to **Ground 5B**). A POSITA would have recognized Chang's disclosures to transistor features, including source/drain regions (*e.g.*, EX1007, ¶¶112-113;

EX1002, ¶¶376-83) and that such features were needed on both sides of the structure/device's gate for operation as an FET, consistent with the transistors contemplated by Chang (*id.*; EX1007, ¶¶2, 48). A POSITA would have thus been motivated, and found obvious, that Chang's structure includes a S/D region on both sides of each gate 1441, 1596 to have functional FETs, which simply involves applying known semiconductor technologies/techniques with a reasonable expectation of success. EX1002, ¶376-83. *See KSR*, 550 U.S. at 398, 416.

g) [1.g]

Chang discloses this limitation. EX1002, ¶¶384-86.

Parts of self-aligned contacts 1670, 1671, and self-aligned contact 1675 (as shown annotated below) are **a plurality of first contacts that are electrically connected to parts of the** S/D regions of PMOS diffusion layer 1600 and are **disposed in** interlayer dielectric layer 1503 (**first dielectric layer**).

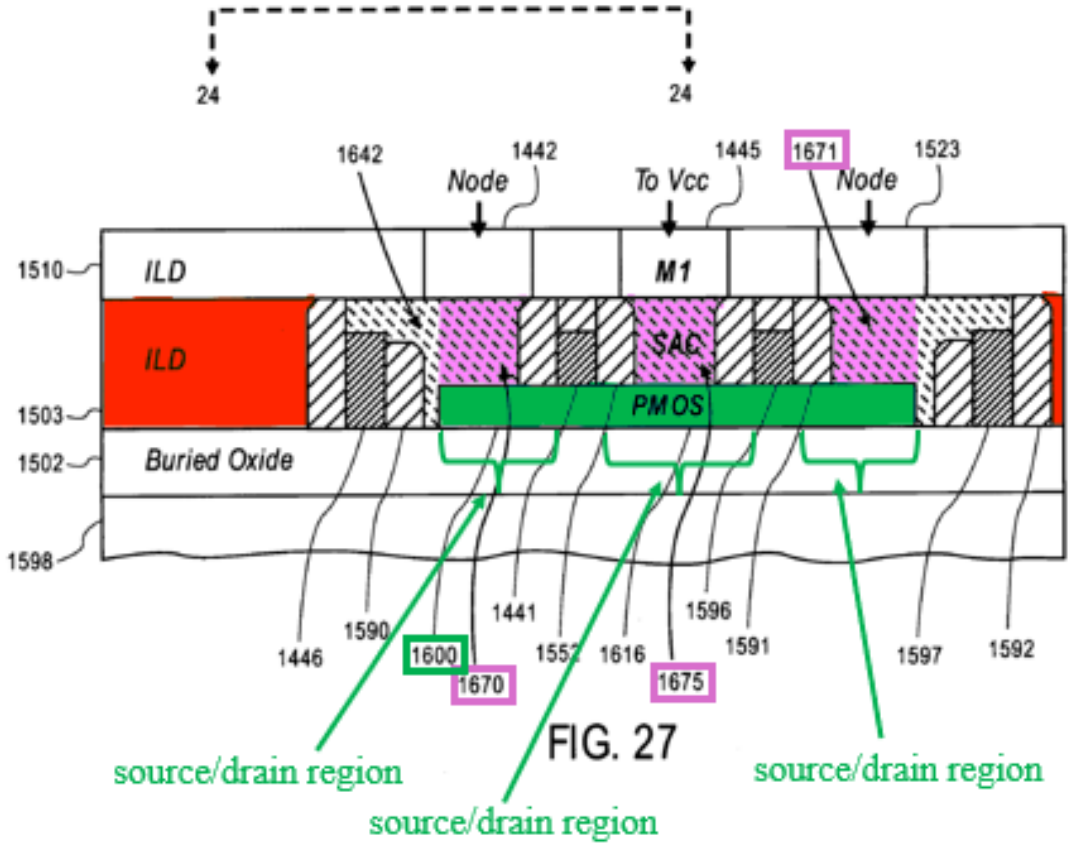


FIG. 27

EX1007, ¶¶112-13; EX1002, ¶¶385-86. "[E]ach of the respective self-aligned contacts 1670 and 1671" contacts the respective "adjacent PMOS diffusion region 1600." EX1007, ¶112.

h) [1.h]

Chang discloses this limitation. EX1002, ¶¶387-94. Chang discloses parts of self-aligned contacts 1670, 1671 (FIG. 27 below) that are **a plurality of second contacts electrically connected to** gates 1446, 1597 and disposed in interlayer dielectric layer 1503 (**first dielectric layer**).

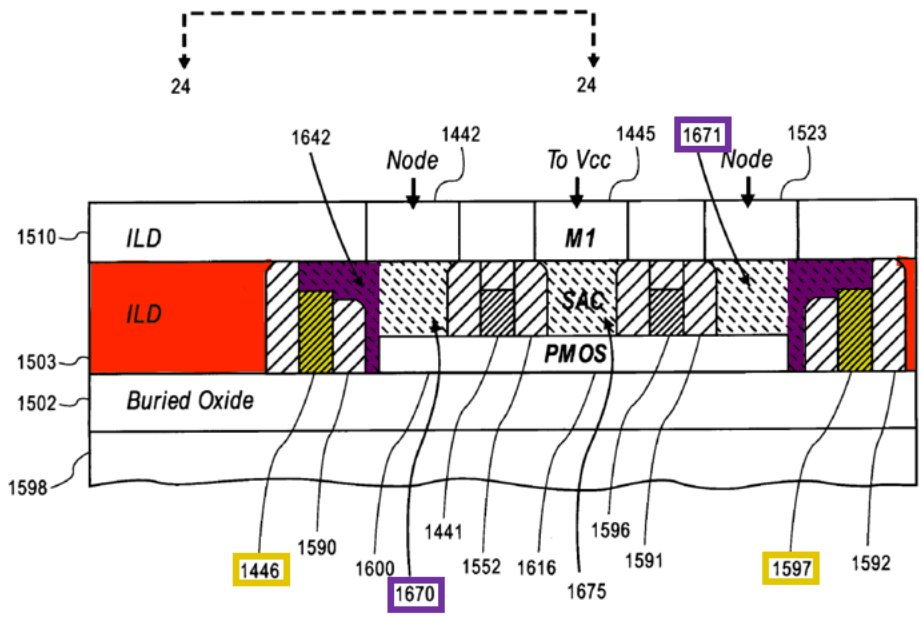


FIG. 27

EX1007, ¶¶112-13; EX1002, ¶388. Metal gate contacts in notch 1105 are also **second contacts**. EX1007, ¶105, FIG. 23.

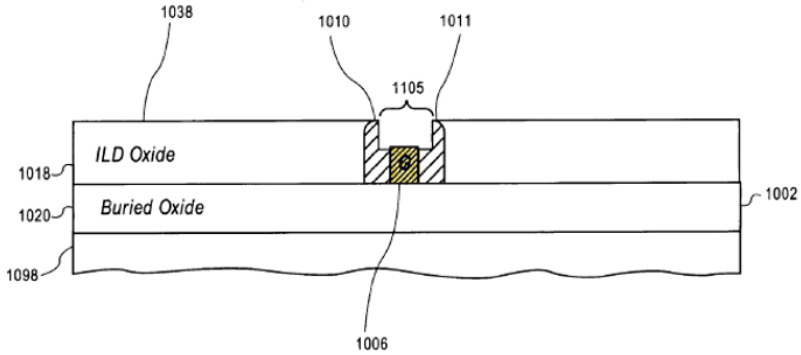


FIG. 23

Each respective self-aligned contacts (e.g., 1670/1671), and metal gate contacts in each notch 1105, contacts a respective gate. *Id.*; EX1002, ¶389.

Further, **at least one of the first contacts directly connects at least one of the second contacts**. EX1002, ¶¶390-94; EX1007, ¶112 ("contact 1670 contacts gate 1446 and PMOS region 1600" and "[c]ontact 1671 contacts gate 1597 and PMOS region 1600").

For "merged" self-aligned contact 1670, the right portion (**at least one of the first contacts**) **directly connects** the "merged" left portion (**at least one of the second contacts**) without any intervening layers or other barriers, which is likewise true for 1671. *Id*.

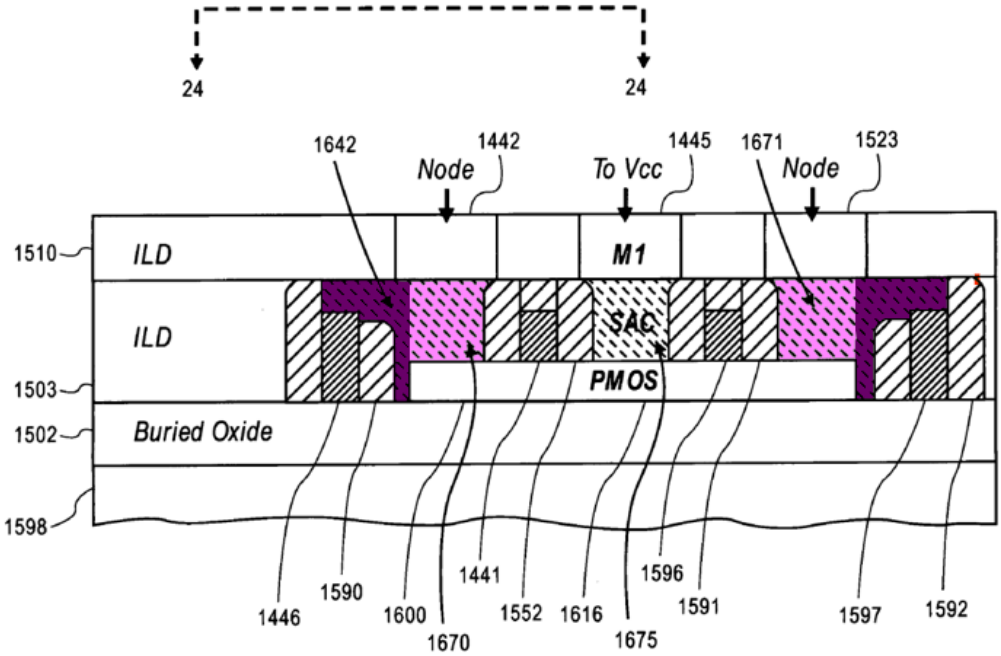


FIG. 27

EX1007, ¶¶112-13; EX1002, ¶¶390-94. The two contacts that are "merged" each serve a separate function based on what structure they contact (i.e., either gate or PMOS region). *Id*.

i) [1.i]

Chang discloses this limitation. EX1002, ¶¶395-99. Chang's silicon nitride caps are **a hard mask disposed on** gates 1441 and 1596, below.

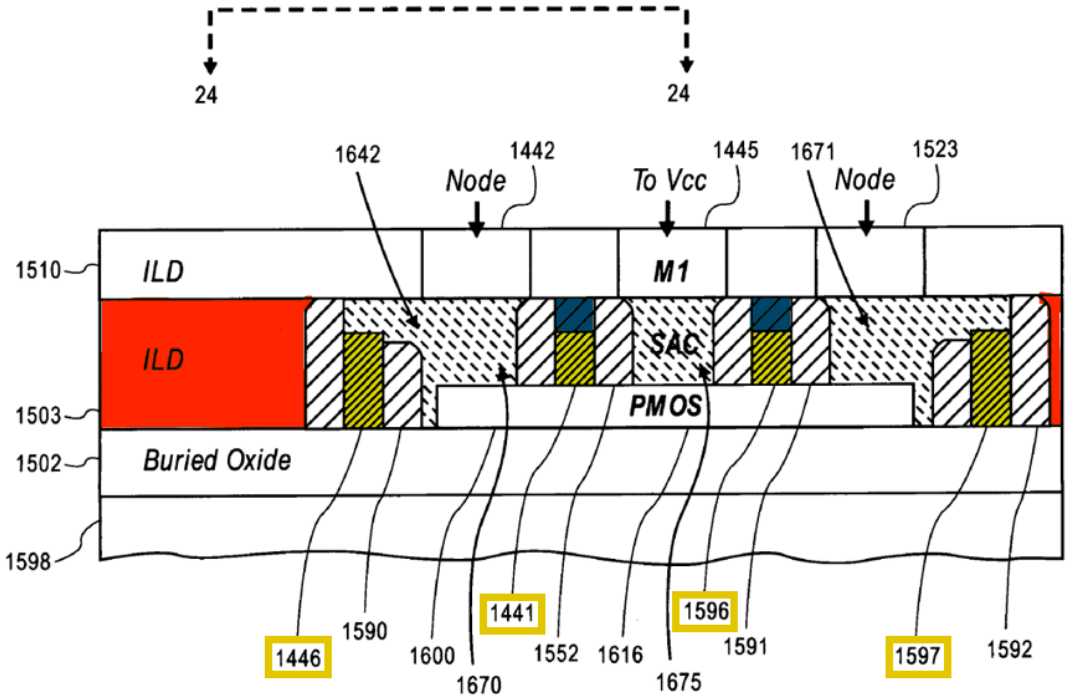


FIG. 27

EX1007, ¶¶111-13; EX1002, ¶396.

The silicon nitride caps provide protection to the feature below, which is a **hard mask** consistent with the '747 patent's disclosure. EX1007, ¶111 ("[i]f there

were alignment errors, then the metal one layer 1510 could short to the gates of gate structures 1550-1554 if those gates **were not protected by** the silicon nitride caps above those respective gates"); ¶¶92-93, 99; EX1001, FIGs. 7, 9, 6:2-18. Silicon nitride was a known hard mask material. EX1001, 3:20-21 ("hard mask 24 mainly comprise silicon nitride"); EX1002, ¶397.

As shown (FIG. 27 above), the **top surface of** silicon nitride caps **and the top surface of** interlayer dielectric layer 1503 **are on the same level** (i.e., the level of the interface between ILD 1503 and 1510). Indeed, the process to form gate-protected self-aligned contacts where a "silicon nitride layer is formed over the top" of the wafer "by deposition," and "planarized by polishing the top of [the] wafer," results in the top surfaces of silicon nitride cap (hardmask) and ILD (first dielectric layer) to be on the same level. EX1007, ¶92, FIG. 18.[16] "[P]olishing is done down to the top 738 of wafer 702," which is the first dielectric layer top surface. *Id*. As explained (§VI.E.1.e), a POSITA would have understood in context of Chang that the subsequent planarization of the self-aligned contacts would polish down the

[16] These teachings also relate to the SRAM teachings of Figures 24-27 for reasons discussed in §X.E.1.e.

entire top surface, including the silicon nitride caps and ILD 1503. EX1002, ¶¶398-99.

2. Claim 2

Chang discloses this limitation. EX1002, ¶¶400-08. Layer 1510 includes an interlayer dielectric (**second dielectric layer) disposed on** layer 1503 (**first dielectric layer**), below:

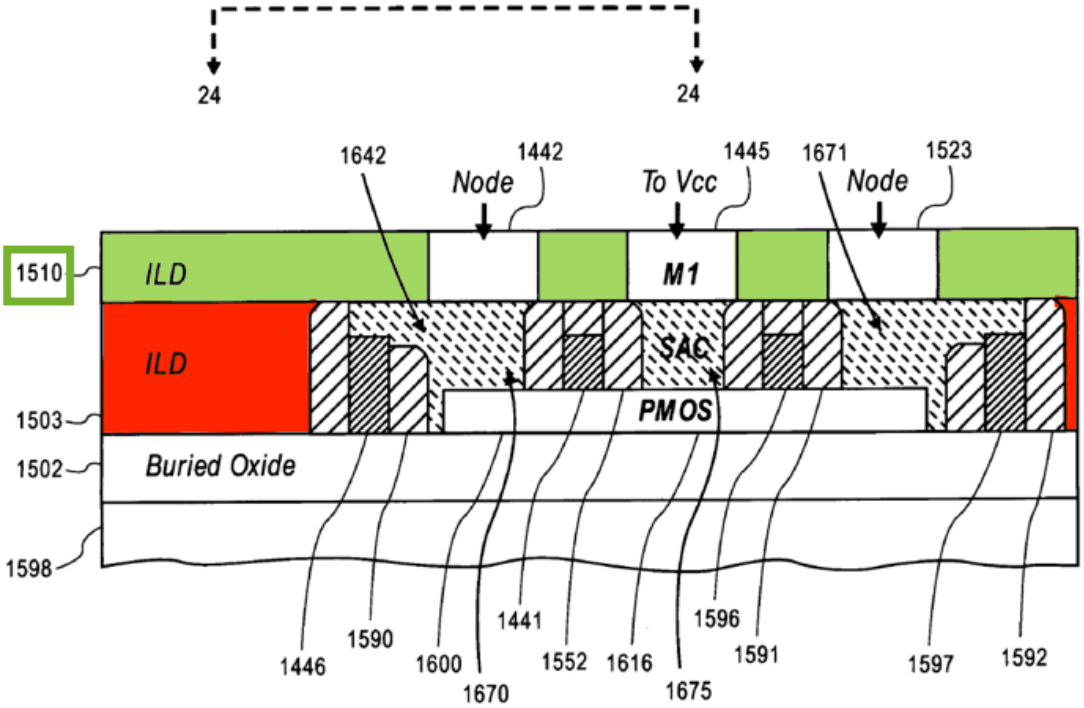


FIG. 27

EX1007, ¶113; EX1002, ¶¶401-02. Chang's "metal one layer 1510 includes an interlayer dielectric that includes openings containing the metal lines 1442, 1445, and 1523." *Id*.

3. Combination Chang's Embodiments

Chang discloses aspects regarding the layout/fabrication of semiconductor structures and self-aligned contacts for transistors. EX1007, ¶1, ¶¶17-44; *id.*, *generally* ¶¶45-117. Notwithstanding (and in addition to) Chang's Figures 24-27 related discussions, which disclose claims 1-2's features (§§VI.E.1-VI.E.2), a POSITA would have been motivated, and found obvious, to consider and implement teachings of features in other portions of Chang's disclosure (*e.g.*, relating to Figure 5, etc.) when forming/configuring Figure 24-27's above-discussed structure, and would have had a reasonable expectation of success in doing so. EX1002, ¶¶403-08.

Indeed, a POSITA would have recognized that Chang relates/references various features in its disclosure in describing the disclosed invention, which all relate to self-aligned contacts and methods of fabricating such contacts in a semiconductor structure (*e.g.*, EX1007, FIGs. 5, 17-23, 24-27, Abstract, ¶¶27-35, 36-37, 45-49, 52, 89-90, 107, 114-117). Accordingly, a POSITA would have been motivated to implement such combined teachings to yield the predictable result of a

structure as discussed above for claims 1-2. EX1002, ¶¶403-08; §§VI.E.1-VI.E.2. *KSR*, 550 U.S. at 416.

F. Ground 6: Claims 4-6 Are Obvious Over Chang

1. Claims 4-5

Chang discloses/suggests these limitations. EX1002, ¶¶409-27.

Starting with **claim 5**, as discussed (§VI.E.1.h), Chang teaches **a plurality of second contacts** formed by parts of "each of the respective self-aligned contacts 1670 and 1671" (**disposed in the first dielectric layer**). In Chang, "the gate contact may be formed at the same time the metal one layer is formed." EX1007, ¶105. The metal one layer is within ILD 1510 layer, thus the gate contact can be formed by a deposition step that deposits the contact material into an opening extending from the ILD 1510 to the gate. Thus, the second contact can be disposed in ILD 1503 (**first dielectric layer**) and ILD 1510 (**second dielectric layer**). *Id.*, ¶¶112-13. Thus Chang's **second contacts** are **a monolithically formed structure**, as claimed. *Id.*, ¶¶105, 112-13; 100-06; EX1002, ¶¶410-11.

Notwithstanding (and in addition to) the above-discussed disclosures, it would have been obvious to a POSITA to form the contacts of Chang's Figure 24-27's structure (*e.g.*, self-aligned contacts 1670, 1671) during Chang's single deposition. Chang recognizes such single deposition approach advantageously "result[s] in a

higher aspect ratio for etch and metal deposition." EX1007, ¶105; EX1002, ¶412. As was known, a higher aspect ratio (i.e., height divided by width) contact means the contact is achieved with a narrower width, and thus less chip area is required, and resultingly, more structures/devices may be provided on a given area. EX1014, 600 ("Increasing the metal line aspect-ratios...improv[e] interconnect performance and density."); EX1020, 463-64; EX1002, ¶412. Thus, a POSITA would have been motivated, and found obvious, to implement such features in Chang's structure such that each second contact is a monolithically formed structure, as claimed. EX1002, ¶413.

A POSITA would have a reasonable expectation of success of implementing such a modification, which would have involved application of known metal damascene techniques, consistent with Chang's teachings. EX1007, ¶97; EX1002, ¶414. Indeed, Chang teaches a damascene technique for its metal one layer formation, which was conventionally known to be able to effectively accommodate different vertical geometries of trenches and vias (*e.g.*, using dual-damascene processing). EX1007, ¶97; EX1002, ¶414; EX1008, ¶17; EX1016, ¶89; EX1015, 55-56; EX1014, 674-76. Such modification would have predictably yielded Chang's Figures 24-27's structure including the second contacts disposed in the first

dielectric layer and in second dielectric layer and each second contact is a monolithically formed structure as claimed. EX1002, ¶414.

Regarding **claim 4**, as discussed (§VI.E.1.g), Chang teaches **a plurality of first contacts** formed by parts of the self-aligned contacts 1670, 1671, and 1675 that reside in ILD 1503 (**disposed in the first dielectric layer**). A POSITA would have understood the gate contacts extend into ILD 1510 (second dielectric layer), as Chang teaches (*supra*; EX1007, ¶105). Further to reasons discussed above, it would have been obvious to also form source/drain contacts extending into the second dielectric layer in the Chang structure (§VI.E.2) because doing so would allow a single deposition process to form the gate contacts and source/drain contacts simultaneously. EX1002, ¶415. Consequently, the processes for forming the source/drain contacts and gate contacts would share same lithography, etching, and/or deposition processes, which reduces process complexity and/or fabrication cost, and would have predictably led to the above modifications to Chang's structure. *Id*.

A POSITA would have been motivated to implement, with a reasonable expectation of success, such a modification since it would have involved application of known technologies/techniques (*supra*, incorporated herein) that would have

predictably yielded Chang's Figures 24-27 structure including "**the first contacts…**" as recited in claim 4. EX1002, ¶415.

2. Claim 6

Chang discloses/suggests these limitations. EX1002, ¶¶416-27.

As discussed above, Chang teaches a "diffusion region" (or "PMOS region") 1600 **disposed on** silicon substrate 1598 (**substrate**) for the same reasons the first dielectric layer is disposed on the substrate in limitation [1.c]. EX1007, ¶¶110-12; §§VI.E.1.c, VI.E.1.f.

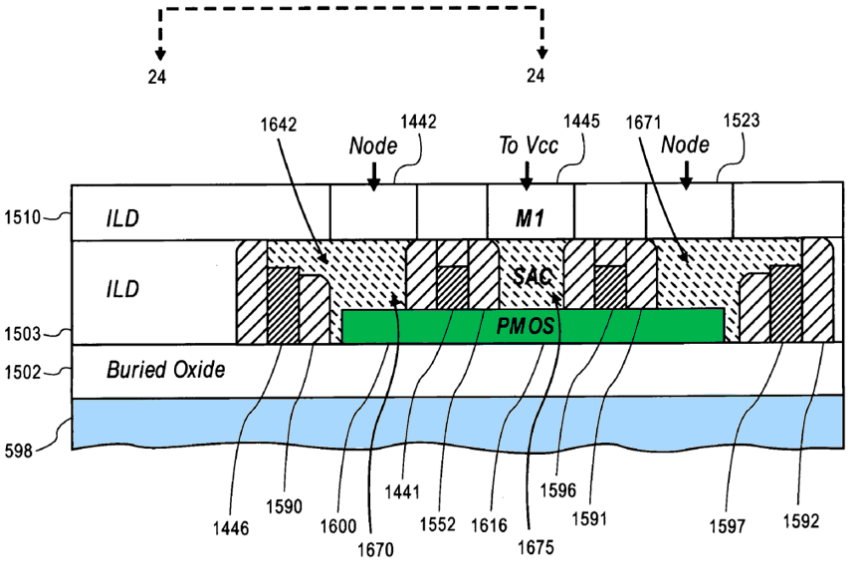


FIG. 27

EX1002, ¶417.

This diffusion region would have been implemented as a diffusion area 704. §VI.E.1.f.

Regarding Figure 5, Chang further explains that "transistor structure 116 includes diffusion layer 104 (also called diffusion body 104 or **fin 104**)." EX1007, ¶48. A POSITA would have understood diffusion area 704 would have been "also called" a fin, which **compris[es] at least one fin structure**.

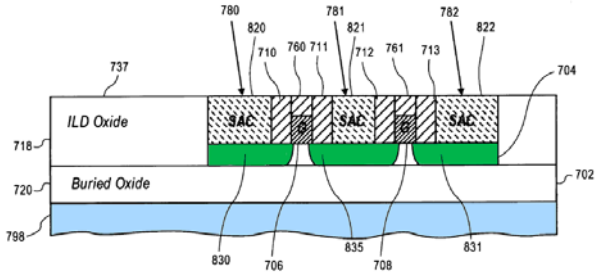


FIG. 20

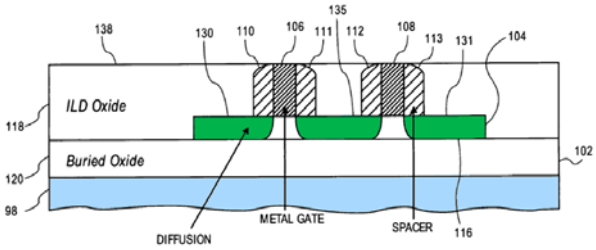


FIG. 5

EX1002, ¶¶418-20; EX1007, FIGs. 5, 20 (below).

Notwithstanding Chang's disclosures, it would have been obvious to a POSITA at the time to configure Figure 24-27's structure (§VI.E) to include **at least one fin structure disposed on the substrate** in view of Chang's Figure 5 related teachings, which similarly show a "cross section of...a transistor structure." EX1007, ¶¶45-46; EX1002, ¶¶421-23.

Additionally, Chang states that "[a]lternative embodiments of [Chang's] invention can be used with other types of transistors with metal gates, such as trigate transistors." EX1007, ¶¶114, 2-6, 13-15, FIGS. 1-3; EX1002, ¶¶424-26, 245-51 (discussing tri-gate transistors fin structure).

Chang's Figure 5 "transistor structure" has a "metal gate" and "diffusion layer," which is "also called" a "fin." EX1007, ¶45. Given the similar teachings in the same disclosure, and in addition to the reasons above (§VI.F.1), a POSITA would have been motivated, and found obvious, to modify Chang's Figure 27 structure with **at least one fin structure disposed on the substrate**, as recited in claim 6. EX1002, ¶427. A POSITA would have a reasonable expectation of success of implementing such a modification, which would have involved application of known transistor structures/techniques, consistent with Chang's teachings and a POSITA's state of art knowledge at the time. *Id*.

G. Ground 7: Claims 3 and 8-9 Are Obvious Over Chang in View of Huang

1. Combination of Chang and Huang

a) Chang-Huang (Claim 3)

As explained, Chang discloses various aspects regarding the layout and fabrication of semiconductor structures and self-aligned contacts for transistors (*e.g.*, EX1007, ¶1, ¶¶17-44; *generally* ¶¶45-117) and in particular Figures 24-27's "SRAM containing transistor structures with gate-protected self-aligned contacts" (*id.*, ¶107). §§VI.E.1-VI.E.3. Further, Chang teaches **metal gates**, *e.g.*, gates 1441, 1443, 1446, 1596, 1597 (§VI.E.1), shown below:

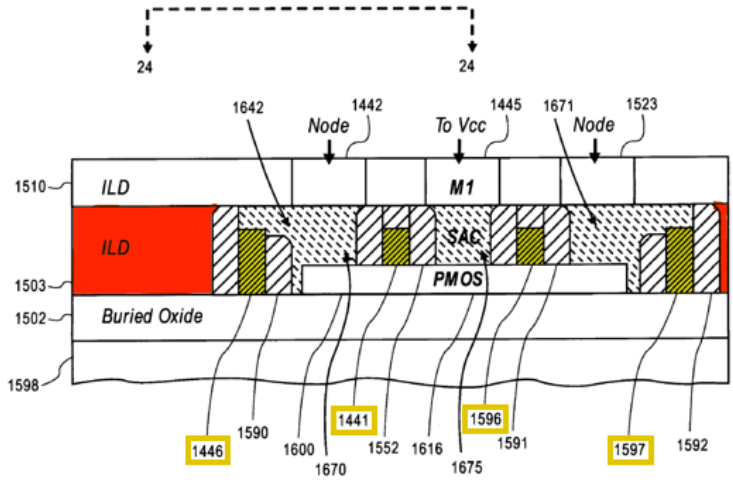


FIG. 27

EX1007, ¶¶112, 108, 114, 47, 111, FIG. 24; EX1002, ¶¶429. Chang's gates include a "silicon nitride protection layer" EX1007, ¶114, which was a known "etch-stop layer for self-aligned contact application." EX1020, 164-65, FIG. 5.64; EX1002, ¶430.

Notwithstanding Chang's disclosures, it would have been obvious to implement an etching stop layer having a truncated top surface and disposed on two sides of the metal gate (**relevant to claim 3 addressed below** (§VIG.2), in view of Huang. EX1002, ¶¶431-32.

Beyond that taught above (§VI.D.1), Huang discloses a Contact Etch Stop Layer (CESL) 36, which is a dielectric material acting as "an etch stop layer" (**an etching stop layer**) disposed on both sides of gate dielectric 24 and gate electrode

26 (**an etching stop layer disposed on two sides of the metal gate**). EX1008, ¶¶8-10, 14, FIG. 1 (annotated).

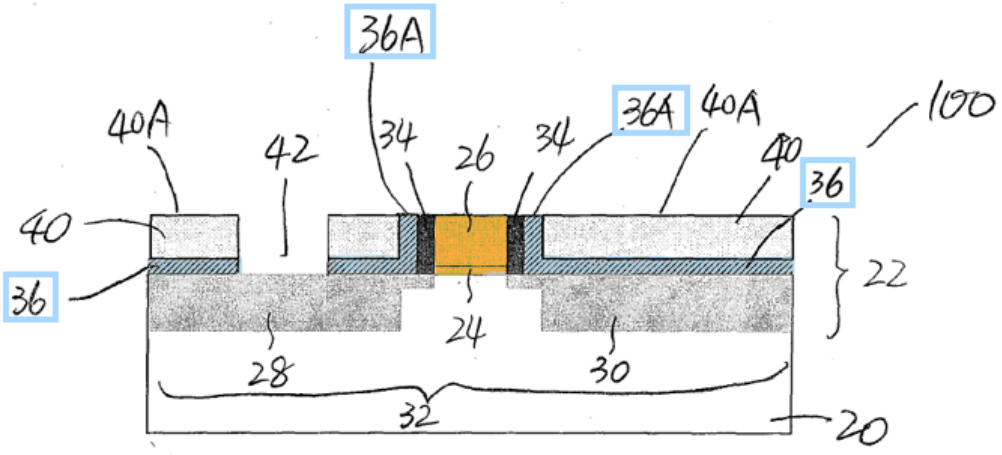


Fig. 1

EX1002, ¶433. As explained regarding Figure 6 (below), CESL 36 is an etch stop layer to protect source/drain region (30) against etching of an opening (56) so etching stops on CESL 36.

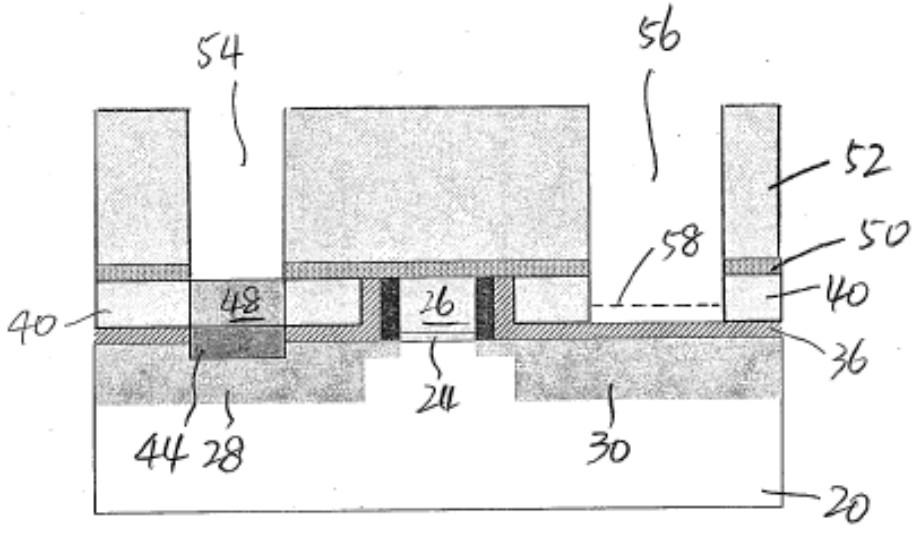


Fig. 6

EX1008, ¶14; EX1002, ¶¶434-36.

Huang's device (FIG. 1) has a planarized top surface due to the "gate last approach," which conventionally involves planarization by two CMP processes of the structure's top surface, including top edges 36A of CESL 36 (**a truncated top surface**). EX1002, ¶¶437-46; EX1020, 544-45. Consistent with Chang (EX1007, FIG. 5, ¶¶46-49 (replacement metal gate process)), Huang acknowledges the gate-last approach results in "the top surface of gate electrode 26 [being] level with top surface 40A of ILD 40 and top edges 36A of CESL 36." EX1008, ¶9.

It would have been obvious to implement a CESL consistent with Huang's teachings in Chang's structure. EX1002, ¶¶447-60. CESLs were well-known and a POSITA would have recognized advantages in implementing such layers (e.g., protect transistor gate structures, source/drain regions). EX1002, ¶447-51; EX1020, 341-45, 164-65. An effective etch stop layer is "highly resistant to the etch chemistry," which prevents an etch process (performed on the inter layer dielectric) from "expos[ing] the source/drain region" and ensures "the integrity of the gate encapsulation is not jeopardized" in this etch process. EX1018, 2:16-31. Chang seeks to protect transistors features (EX1007, ¶114), and thus a POSITA would have been motivated to look to ways to provide such protection, as taught by Huang. EX1002, ¶¶449-51. Given such guidance, a POSITA would have been motivated, and found obvious, to modify Chang's structure with an etching stop layer having a truncated top surface and disposed on two sides of Chang's metal gate to provide the protective benefits of etch stop layers consistent with Huang's teachings and known in the art. EX1002, ¶¶447-60.

b) Chang-Huang (Claims 8-9)

In considering Huang in context of Chang as explained above in §IX.G.1.a, a POSITA would have further been motivated in light of Huang to modify Chang's above modified structure with multiple metal layers (e.g., at least metal lines M2 and

vias M1) to form more complex and higher-capacity semiconductor devices using Chang's structure, and use a dual-damascene process to provide such additional lines/vias consistent with that known in the art and taught by Huang. EX1002, ¶¶461-94.

As discussed, Chang teaches first and second contacts. EX1007, ¶¶112-13; §§VI.E.1.g-h, VI.E.2. Chang also teaches metal one (M1) layer 1510 including a plurality of metal lines that "resides immediately above layer 1503" and provides contact to the self-aligned contacts and gates.[17] EX1007, ¶¶112-13, 97-99, 106. Each metal line is a unitary metal structure formed from a single metal deposition, such as by "a metal damanscene [sic] process" where a "deposited" "metal layer" "fills opening[s]" that were etched according to the desired lines/contacts structure. *Id*., ¶97; EX1002, ¶¶463-64.

[17] Although Chang uses different nomenclature ("M1") than Pethe ("M0") to refer to the lowest metal line/layer above its respective contact structure, both lines/layers (Chang's "M1"/Pethe's "M0") represent a metal line/layer above which additional metal lines/layers may be formed, as known in the art and taught by Huang. EX1002, ¶491.

In addition to the above-discussed disclosures, it would have been obvious to a POSITA to configure Chang-Huang's modified Figure 24-27's structure (§VI.G.1.a) to include higher-level metal layers beyond metal (1) layer in view of Huang. EX1002, ¶¶465-92.

Huang teaches metal M1 lines 74 and M0 vias 72, explaining that "[i]n subsequent process steps, **more metal layers (not shown) may be formed over metal layer M1**." EX1008, ¶17, FIG. 8A (annotated below).

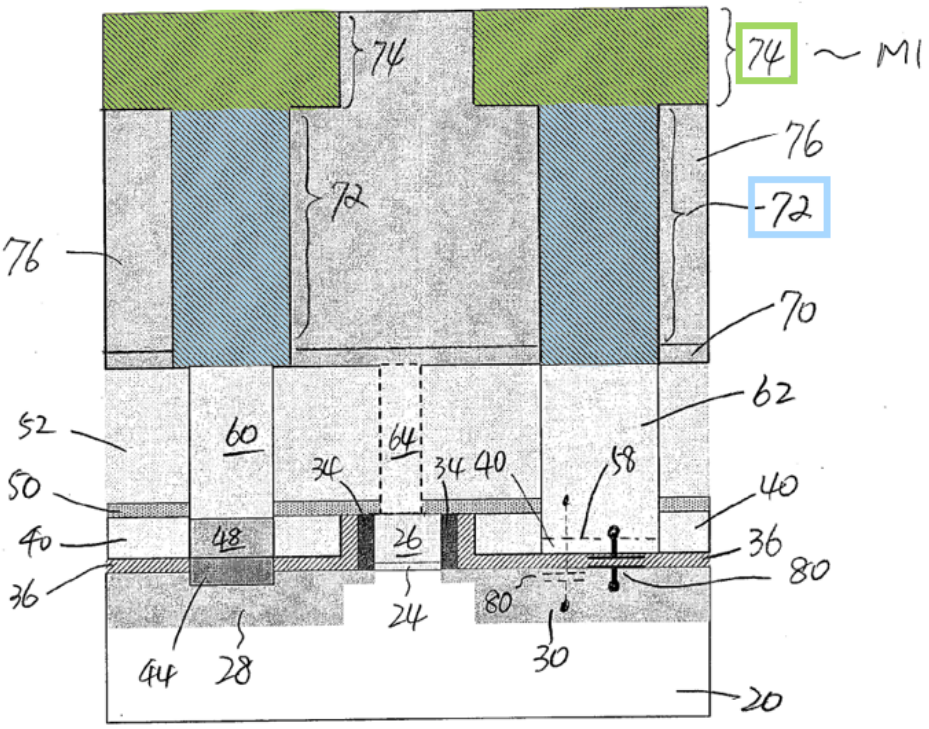


Fig. 8A

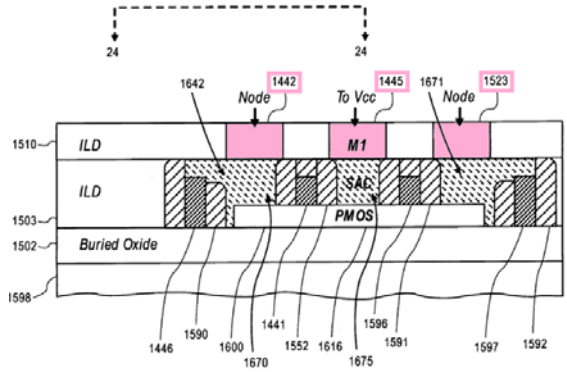
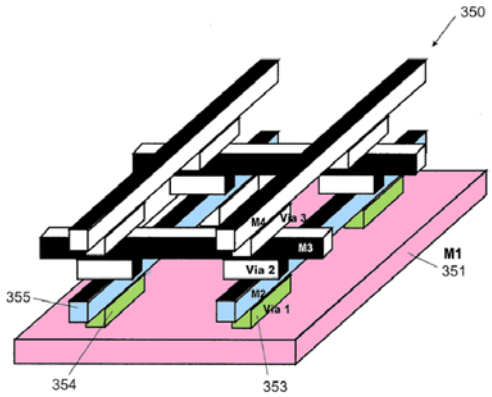
EX1002, ¶478.

Huang's "more metal layers" "formed over metal layer M1" (e.g., metal lines 74 implemented in the M2 layer, and vias 72 implemented in the M1 layer) describe a plurality of additional contacts in the structure. Huang's teachings, in context of Chang's disclosures, would have motivated a POSITA to configure Chang's modified structure (§VI.G.1.a) such that a plurality of third contacts (consistent with Huang) were disposed on Chang's self-aligned contacts, whether disposed only in ILD layer 1503 or in ILD layer 1503 and the metal one layer within the ILD 1510 layer (and thus on parts of the first contacts and on parts of the second contacts). §§VI.G.1; VI.E.1.g-h; EX1002, ¶¶479-480. Given Chang teaches damascene (EX1007, ¶97, 106) and Huang teaches dual-damascene, which involve a single metal deposition, each such contact in the modified structure would have been a monolithically formed structure. EX1002, ¶480.

A POSITA would have had reasons to consult Huang when looking to address BEOL processing of semiconductor devices like discussed in Chang. EX1007, ¶¶112-13; EX1008, ¶17; EX1001, 5:31-6:37; EX1002, ¶481. Such collective teachings/guidance would have led a POSITA to modify Chang's structure with multiple metal layers (e.g., at least metal lines M2 and vias M1). The advantages and necessity of implementing multiple metal layer levels and vias would have been readily apparent to a POSITA. EX1002, ¶¶482-83, 466-68; EX1020, 570; EX1014,

600. A POSITA would have recognized that a single metal layer would be insufficient to handle the complexity of ICs comprising small geometry transistors. EX1007, ¶¶2, 6; EX1002, ¶¶484-85, 468.

Likewise, a POSITA would have been motivated, and found obvious, to use dual-damascene processing to provide such additional lines/vias at least for reasons stated. EX1002, ¶¶465-91; EX1020, 345-49, 464, 497-98, 517-18, 574-79; EX1014, 695, 698; EX1015, 56, 92. It was conventional to repeat dual-damascene processes to provide multiple higher-level metal layers. EX1002, ¶¶467-76; EX1014, 696-98, FIG. 15-3); EX1016, ¶89; EX1017, ¶¶37-40, FIG. 3A. Indeed, Chang's M1 layer is "formed by a metal damanscene [sic] process" (¶97), and a POSITA would have looked to damascene processing to form higher metal layers. Also, use of dual-damascene processing to provide M2 lines and M1 vias over M1 lines was known, and BEOL processing (not described by Chang) was critical to create an IC. EX1002, ¶¶467-85; EX1017, ¶¶37-40, FIG. 3A (annotated below); EX1007, FIG. 27 (annotated below); EX1016, ¶89; EX1014, 696-98; EX1020, 570, 19, 574-78, 611-18.

 FIG. 27	 FIGURE 3A
Chang	**Ning (EX1017)**

Accordingly, it would have been obvious to implement the modified Chang-Huang structure (claim 3) to include M2 lines and M1 vias above the structure's M1 line and used known dual-damascene processes to effectively add them. EX1002, ¶¶466-91. A POSITA would have had a reasonable expectation of success in such implementation given it would have involved known technologies/techniques (*e.g.*, dual-damascene, M2 lines, M1 vias) to a known device/structure (Chang's structure) predictably yielding Chang's modified Figures 24-27 structure (§VI.G.1.a) having monolithically formed structure contacts disposed on parts of the first contacts and on parts of the second contacts as claimed. EX1002, ¶¶489-92.

For similar reasons, using such dual-damascene processing to form M1 vias 72 and metal layer M2 metal lines 74 together in a single deposition in the above discussed Chang-Huang structure, would have likewise predictably resulted in M1 vias 72 and M2 layer metal lines 74 to form a plurality of contacts in the

structure, where the vias and metal lines comprise the same material and contact each other directly (relevant to **claim 9** (*infra* §VI.G.4)). EX1008, ¶17, FIG. 8A; EX1002, ¶¶492-94.

2. Claim 3

Chang in view of Huang discloses/suggests these limitations. (EX1002, ¶¶428-60.)

As discussed in §VI.G.1.a, it would have been obvious to implement an "etching stop layer…", as recited in claim 3, in Chang's structure in view of Huang. §VI.G.1.a. Namely, for reasons discussed in §VI.G.1.a, a POSITA would have been motivated, and found obvious, to modify the above-discussed Chang structure (§§VI.E.1-VI.E.3), to include the claimed etching stop layer, consistent with Huang's teachings and a POSITA's state of art knowledge. EX1002, ¶¶428-60.

3. Claim 8

As discussed, Chang teaches **first and second contacts**. EX1007, ¶¶112-13; §§VI.E.1.g-h, VI.E.2-VI.E.3; EX1002, ¶463. Further, the analysis in §VI.G.2 demonstrates how the Chang-Huang combination discloses/suggests claim 3.

Chang-Huang's combination discussed for claim 3 discloses/suggests the claim 8 in two ways: (1) based on additional teachings of Chang; and (2) based on Chang-Huang's collective teachings.

<u>*Chang*</u>: As explained (§VI.G.1.b), Chang's metal one (M1) layer 1510 includes **a plurality of** metal lines (**third contacts**) that "resides immediately above layer 1503" (**disposed on parts of the first contacts and on parts of the second contacts**) and provides contact to the self-aligned contacts and gates. EX1007, ¶¶112-13, 97-99, 106; EX1002, ¶464. Because each metal "line" or "contact" is a unitary metal structure formed from a single metal deposition, **each third contact is a monolithically formed structure**, as claimed. *Id*. Indeed, the metal lines/contacts may be formed by "a metal damanscene [sic] process" where a "deposited" "metal layer" "fills opening[s]" that were etched according to the lines/contacts desired structure. *Id*. Such features would have been included in Chang-Huang's structure (§§VI.G.1.a, VI.G.2) and resulted in the structure including "third contacts…" as recited in claim 8.

<u>*Chang in view of Huang*</u>: As explained in §IX.G.1.b, a POSITA would have been further motivated, and found obvious, to modify Chang's modified structure to include "**a plurality of third contacts**…" as recited in claim 8, in view of Huang. EX1002, ¶465.

Namely, in light of Huang and a POSITA's state of art knowledge (§VI.G.1.b), the modified Chang-Huang structure (§VI.G.2) would have been predictably modified to include, above its M1 metal layer, M2 lines (and M1 vias),

as taught by Huang. EX1008, ¶17, FIG. 8A. Consequently, the modified Chang-Huang structure (claim 3) would have included a **plurality of third contacts** (*e.g.*, parts of newly formed M2 lines above the structure's M1 lines) **disposed on parts of the first contacts and on parts of the second contacts first and second contacts** (EX1007, ¶¶112-13; §§VI.E.1.g-h, VI.E.3, VI.G.2), as recited in claim 8. EX1002, ¶¶462, 465; §VI.G.1.b. Given such contacts would be formed using dual-damascene techniques, like taught by Huang, **each third contact** (in Chang's structure) would be a **monolithically formed structure** (as claimed). *Id.*

4. Claim 9

Chang-Huang discloses/suggests these limitations. (EX1002, ¶¶492-94, 461-491.)

Chang-Huang's structure discussed for claim 8 would have included M1 vias 72 (**via hole structure**) and M2 layer metal lines 74 (**trace structure**) to form **a third contact**, consistent with features described by Huang, below.

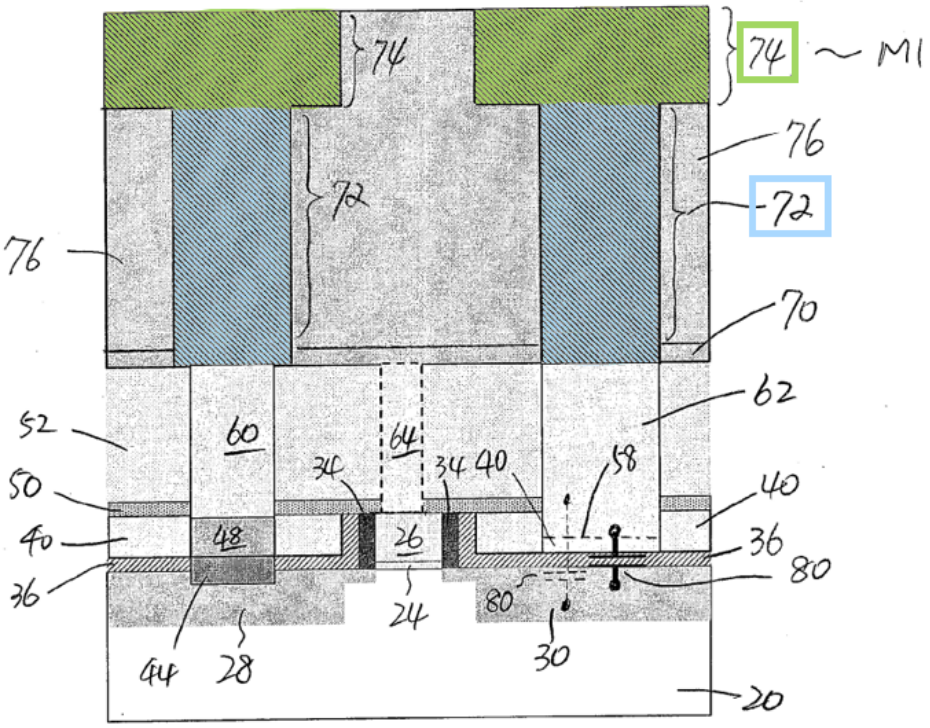


Fig. 8A

EX1002, ¶¶492-94; EX1008, ¶17.

For reasons explained in §VI.G.3, it would have been obvious to use dual-damascene processing to form M1 vias 72 and metal layer M2 metal lines 74 together in a single deposition in the Chang-Huang structure. EX1002, ¶492-94; §§VI.G.1.b, VI.G.3.

Chang-Huang's modified structure would have included a **plurality of third contacts** as in claim 8 (§VI.G.3), where **each third contact** (in Chang-Huang's modified structure) would have comprised **a via hole structure (M1 vias) and a**

trace structure (parts of newly formed M2 lines (EX1001, 5:48-53 (trace structure may be "lines")), which would **comprise the same material and contact each other directly** (as in claim 9) given they are formed using dual-damascene processing as taught by Huang. EX1002, ¶492-94; EX1008, ¶17, FIG. 8A; §§ VI.G.1.b, VI.G.3.

H. Ground 8: Claims 4-5 Are Obvious Over Chang in View of Hong

1. Hong

Hong discloses improved structures for electrically contacting semiconductor device features. EX1010, Abstract, 2:13-58, 8:53-9:27, 10:46-67; *id.*, 2:4-10, 9:55-64, 11:1-9. Hong discloses a "share contact" for FETs that includes contact 442 formed simultaneously between a metal gate 411 and source/drain region 402, and within a plurality of dielectric layers (e.g., layer 406 on layer 401). *Id.*, 8:53-9:27, 10:46-67, FIGs. 7, 9.

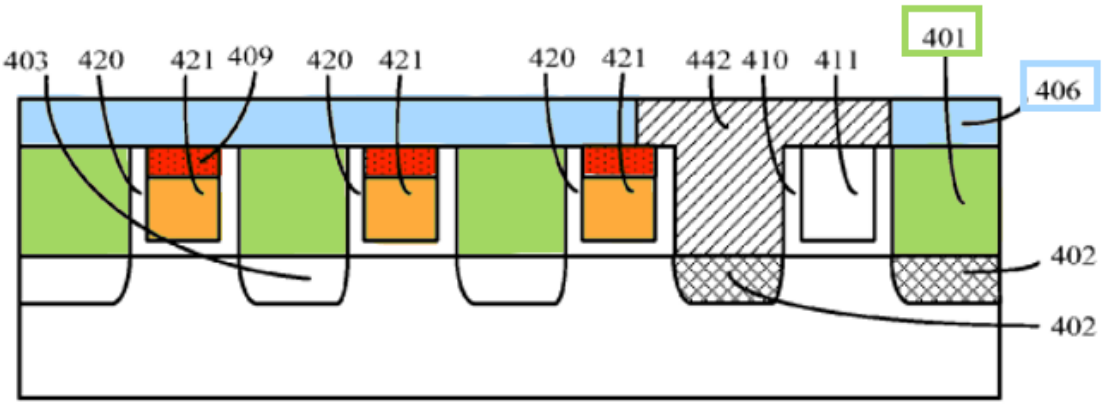


FIG. 7

Id., Fig. 7.; EX1002, ¶¶499-500.

2. Combination of Chang and Hong

As explained, Chang discloses parts of self-aligned contacts 1670, 1671, and self-aligned contact 1675 (**first contacts**) disposed in layer 1503 (**first dielectric layer**) of Figure 24-27's structure (below), where each is a homogeneous metal fill layer formed from a single metal deposition (EX1007, ¶¶93-94, FIGS. 19-20) and therefore is **a monolithically formed structure**. §§VI.E.1.g, VI.E.2-VI.E.3.

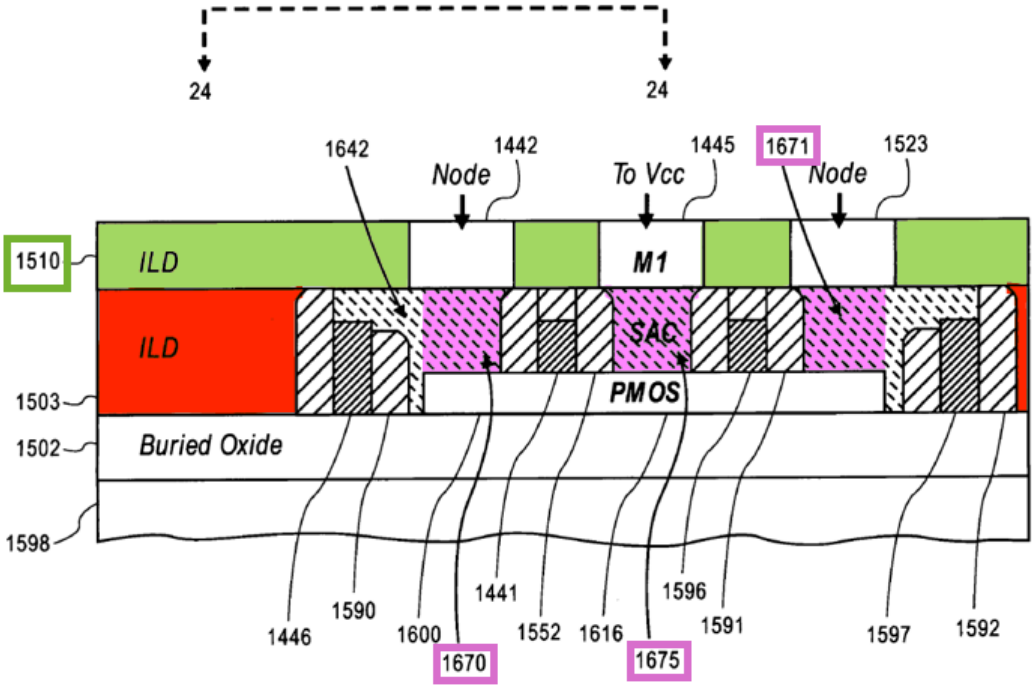


FIG. 27

EX1007, ¶¶113, 93-94, FIGS. 19-20; EX1002, ¶¶496-97.

Notwithstanding Chang's disclosures, it would have been obvious to implement identified Chang's self-aligned contacts (**first contacts**) to be **disposed**

in layer 1510 including an interlayer dielectric (**second dielectric layer**) (relevant to **claim 4**), based on Hong. EX1002, ¶498.

Hong discloses a first contact layer 442 formed in both a first dielectric layer 401 and a second dielectric layer 406. EX1010, 8:54-9:27. A third dielectric layer 409 (i.e., capping layer) is formed on a second metal gate 421, below. *Id*.

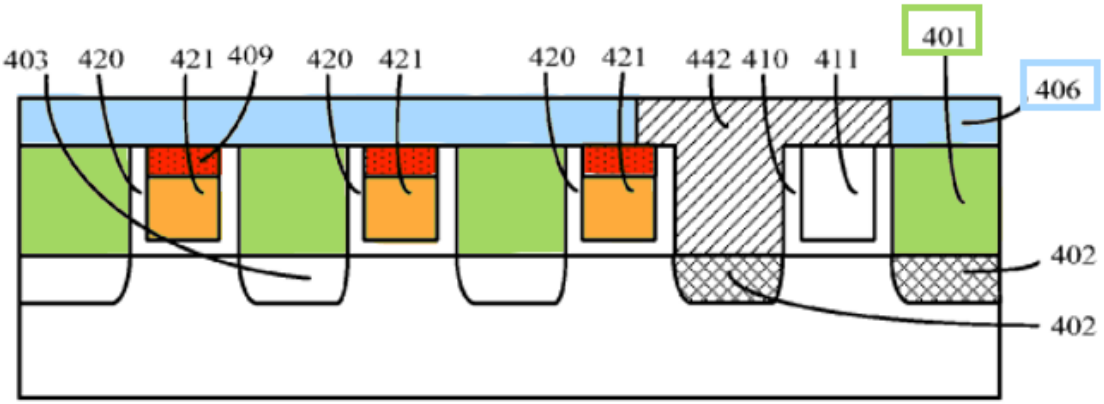


FIG. 7

EX1002, ¶¶499-500.

A POSITA had reasons to consult Hong when looking to address the implementation/formation of such contact areas and related structures. EX1007, ¶¶108-113; EX1010, 8:54-10:56; EX1001, 1:9-13, 5:66-6:37; §VI.H.1; EX1002, ¶501.

A POSITA would have been motivated, and found obvious, to modify Chang's structure to provide a second dielectric layer beneath metal (1) layer, consistent with Hong's teachings and a POSITA's knowledge. EX1002, ¶¶502-11.

It was known that creating metal contacts generally involved depositing a metal fill layer and CMP to remove it from outside desired contact location(s). *Id.*, ¶504. Hong recognizes that such CMP may damage underlying transistor structures, and having a second dielectric layer beneath the metal (1) layer protects the underlying transistor structures and will "aid to increase the stability of the transistor." EX1010, 11:1-9, 9:55-64. Hong addresses known metal gate / spacer damage problems where second gate dielectric layer 420 and third dielectric layer 409 provide full protection to the second metal gate 421 during such etching to create openings for first contact layer 442. *Id.*, 8:54-9:27, 8:3-13, 7:43-54. This solution solves "[t]he problem of exposing the second metal gate 421 caused by technology errors during a process for exposing the first metal gate 411," "thus it may ensure the stability of the transistor." *Id.*, 8:54-64.

Chang's metal (1) layer is similarly fabricated by "metal damascene process" where metal deposition "covers surface 965 and fills opening 940, 941, and 942" and is subsequently "planarized by polishing" to remove the metal everywhere except the openings. EX1007, ¶97. A POSITA would have understood Chang's transistor structures would be susceptible to damage during such polishing, and recognized protection benefits of a second dielectric layer beneath metal (1) layer. EX1002, ¶¶505-07. Guided by such knowledge and by Hong, a POSITA would

have been motivated, and found obvious, to form an additional dielectric layer in Chang's structure beneath the metal (1) layer comprising ILD 1510, such that the self-aligned contacts are disposed in the second dielectric layer (**relevant to claim 4** discussed below). EX1002, ¶508.

A POSITA would have had a reasonable expectation of success of implementing such a modification given it would have involved the application of known semiconductor device structure/fabricating technologies (e.g., dielectric deposition) including gate protection techniques applicable to Chang's gate structures. *Id.*, ¶¶509-11.

Additionally, a POSITA would have recognized Chang discloses the identified parts of self-aligned contacts 1670/1671 (**second contacts**) are disposed in layer 1503 (**first dielectric layer**), each being a homogeneous metal fill layer formed from a single metal deposition (EX1007, ¶¶93-94, FIGS. 19-20) and therefore is **a monolithically formed structure** (§§VI.E.1.h, VI.E.2), below:

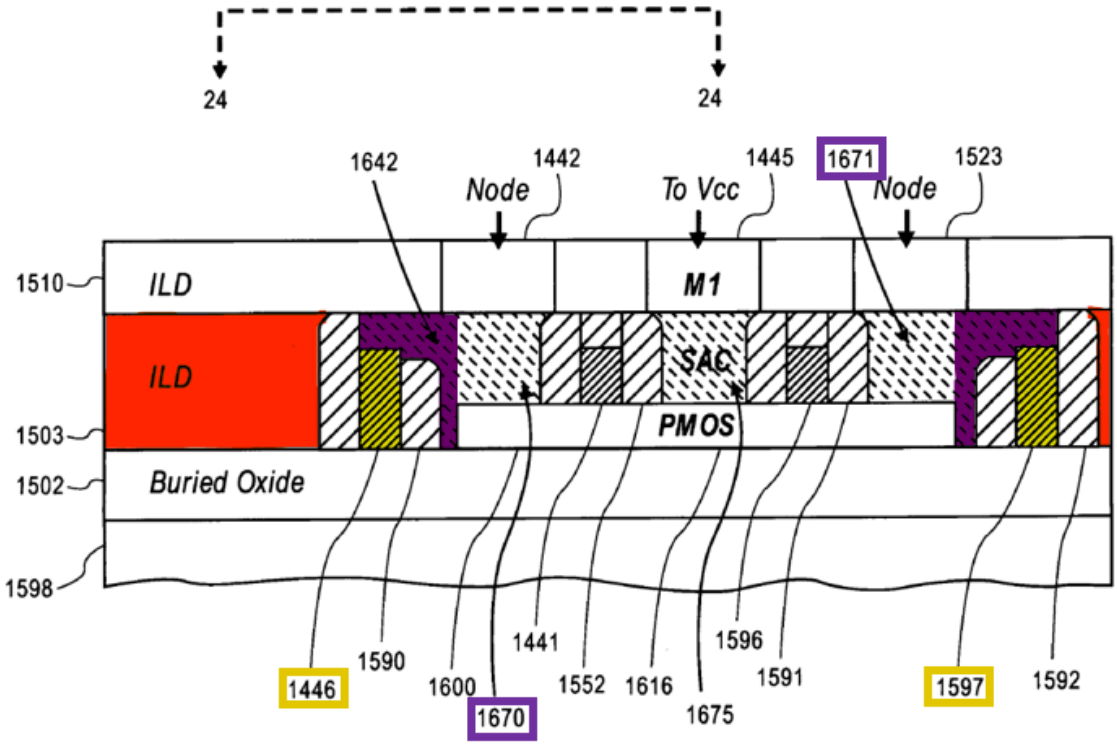


FIG. 27

EX1007, ¶¶112-13; EX1002, ¶¶496-97, 513.

Such features are consistent with the above-discussed Chang teachings in view of Hong for claim 4. For similar reasons, a POSITA would have had the same motivation, rationale, and expectation of success, and would have found obvious, to configure Chang's structure such that the second contacts disposed in the first and second dielectric layers and each second contact is a monolithically formed structure (**as recited in claim 5**). *Supra*; EX1002, ¶¶512-15; *infra* §§VI.H.3-VI.H.4.

3. Claim 4

Chang-Hong discloses/suggests these limitations. EX1002, ¶¶495-511.

As discussed in §VI.H.2, it would have been obvious to configure Chang's structure (claims 1-2 (§VI.E)) such that the first contacts disposed in the first and second dielectric layer and each first contact is a monolithically formed structure in view of Hong. §§VI.H.1-VI.H.2. Namely, for the reasons in §§VI.H.1-VI.H.2, a POSITA would have been motivated, and found obvious, to modify Chang's Figure 24-27 structure to include such features, consistent with Hong's teachings and a POSITA's state of art knowledge, predictable resulting in the structure including the "first contacts" features as recited in claim 4. *Id.*

4. Claim 5

Chang-Hong discloses/suggests these limitations. EX1002, ¶¶512-15.

As discussed in §VI.H.2, it would have been obvious to configure Chang's structure (claims 1-2 (§VI.E)) such that the second contacts disposed in the first and second dielectric layer where each second contact is a monolithically formed structure in view of Hong. §§VI.H.1-VI.H.2. Namely, for the reasons in §§VI.H.1-VI.H.2, a POSITA would have been motivated, and found obvious, to modify Chang's Figure 24-27 structure to include such features, consistent with Hong's

teachings and a POSITA's state of art knowledge, predictable resulting in the structure including the "second contacts…" as recited in claim 5. *Id.*

I. Ground 9: Claim 7 is Obvious Over Chang in View of Bohr

1. Combination of Chang and Bohr

As explained, Chang discloses claim 1. §§VI.E.1, VI.E.3. Notwithstanding the above-discussed disclosures in §§VI.E.1-VI.E.3, it would have been obvious to implement a **salicide layer disposed between each S/D region and each first contact** in Chang's structure in view of Bohr. EX1002, ¶¶516-28.

As explained, Bohr teaches forming a silicide layer (EX1009, 12:61-13:10 ("deposition process…annealing process…") and use of a salicide layer between a source/drain and contact (*id.*, FIGs. 8A-8B). §VI.C.1. As explained, Bohr's silicide is self-aligned, and thus Bohr teaches a salicide layer disposed between a source/drain region and trench contact. *Id.*; EX1009, 12:61-13:8. Bohr's teachings are consistent with a POSITA's state of art knowledge that it was known to include a salicide layer between a source/drain and a contact, such as in a self-aligned trench contact. EX1002, ¶¶519-20; EX1020, 157-58 (conventional salicide processes involving metal deposition/annealing over source/drain regions), FIG. 5.39; *also* EX1001, 4:22-33.

A POSITA knew implementing such a salicide layer would advantageously create a lower resistance contact, and thus would have had reason to look to likewise improve Chang's structure. EX1002, ¶¶518-20, 525; EX1013, 4:63-67, 3:56-58. Consequently, a POSITA would have considered Bohr when implementing a semiconductor structure/device like discussed in Chang. EX1002, ¶521; EX1007, FIG. 27; EX1009, 12:61-14:3.

A POSITA would have been motivated to combine teachings of Chang (*e.g.*, contacts and source/drain regions) and Bohr (*e.g.*, self-aligned silicide (i.e., salicide) layer disposed between a source/drain region and trench contact) to improve Chang's structure by *e.g.*, reducing electrical resistance between Chang's S/D region and self-aligned contacts (1670/1671/1675) (first contacts). EX1002, ¶522-24; §§VI.E.1.f-VI.E.1.g.

Indeed, Bohr teaches known advantages to implementing a salicide layer between a source/drain and contact (*e.g.*, to "reduce[] the electrical resistance between the later formed trench contact…and the diffusion region…"). EX1009, 13:8-10; EX1002, ¶527; EX1013, 4:63-67, 3:56-58. Thus, a POSITA would have looked to achieve similar benefits by using a salicide layer between the S/D region and self-aligned contacts (1670/1671/1675) in Chang's structure. EX1002, ¶¶525-26.

A POSITA would have had the rationale and skill in implementing, and expectation of success in achieving, the above-discussed Chang-Bohr combination to achieve the benefits of using a salicide layer between a diffusion region and trench contact in a structure like that of Chang. EX1002, ¶528; Ex.1009, 1:5-36, 4:5-11, 12:61-13:10. The Chang-Bohr combination would have involved application of known technologies (e.g., salicide layers between source/drain regions and trench contacts) (*e.g.*, EX1013, 4:63-5:30, 5:48-64, 9:5-30, 10:7-35; EX1020, 157-58) according to known methods (e.g., known deposition/annealing processes) to predictably yield a semiconductor structure (Chang's Figure 24-27 structure) with a salicide layer disposed between the source/drain region and each self-aligned contacts 1670/1671/1675 ("**first contacts**") with reduced resistance between them. EX1002, ¶¶522-28; *KSR*, 550 U.S. at 416.

2. Claim 7

Chang in view of Bohr discloses/suggests these limitations. EX1002, ¶¶516-28.

As discussed in §VI.I.1, it would have been obvious to configure Chang's structure (claim 1 (§VI.E)) to include a self-aligned silicide ("salicide") layer disposed between each S/D region and each first contact as claimed in view of Bohr. §VI.I.1. Namely, for the reasons in §VI.I.1, a POSITA would have been motivated,

and found obvious, to modify Chang's Figure 24-27 structure to include such features, consistent with Bohr's teachings and a POSITA's state of art knowledge, predictable resulting in the structure including "a salicide layer…" like in claim 7. *Id.*

VII. DISCRETIONARY DENIAL IS NOT APPROPRIATE

The Stewart Memorandum dated March 26, 2025, titled "Interim Process for PTAB Workload Management," sets out a temporary procedure under which Petitioners will have an opportunity to respond to any discretionary denial arguments PO may raise through a bifurcated briefing process. Petitioners believe discretionary denial is unwarranted and, at the appropriate time, plan to rebut any claims PO may advance to the contrary.

Meanwhile, Petitioners identify below several non-limiting considerations that weigh against discretionary denial:

- The ITC instituted investigation on March 21, 2025, just 23 days before this Petition was filed. The ITC has not even set a schedule, let alone issued any substantive orders. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 11 (Mar. 20, 2020) (expeditious filing weighs against denial); *SharkNinja v. iRobot Corp.*, IPR2021-00545, Paper 11, at 8 (Sept. 8, 2021) (petitioner's diligence and remaining work at the ITC weighs against denial).
- No other forum has adjudicated these claims.
- The Challenged Claims include claims 2-9 not asserted in the ITC.

- Petitioner TSMC has a 94% institution rate and a 100% success in FWDs. Consistent with that track record, the merits here are strong, presenting two sets of grounds addressing all claims based on two primary references. §VI.
- Expert testimony is corroborated by documentary evidence.
- Each of the Petitioners (not to mention the other real parties-in-interest) is responsible for substantial and sustained investments in the U.S.[18]

The ITC lacks authority to invalidate the claims, but the companion district court, which will be stayed, triggered the one-year bar date, thereby limiting Petitioners' options to invalidate the Challenged Claims. *See 3Shape A/S v. Align*

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[18] "TSMC Intends to Expand Its Investment in the United States to US ***$165 Billion*** to Power the Future of AI," https://pr.tsmc.com/english/news/3210 (Mar. 4, 2025); "Apple Will Spend More Than ***$500 billion*** in the U.S. Over the Next Four Years," https://www.apple.com/newsroom/2025/02/apple-will-spend-more-than-500-billion-usd-in-the-us-over-the-next-four-years/ (Feb. 24, 2025); "Trump and TSMC Announce ***$100 Billion*** Plan to Build Five New US Factories," https://www.reuters.com/technology/tsmc-ceo-meet-with-trump-tout-investment-plans-2025-03-03/ (Mar. 4, 2025).

Tech., Inc., IPR2020-00223, Paper 12, at 33-34 (May 26, 2020) (instituting despite parallel ITC case to preserve the "efficiency and integrity of the system"); *Emerson Electric Co., v. Sipco, LLC*, IPR2019-00547, Paper 15, at 9 (Aug. 30, 2019) (IPR proceedings not duplicative of parallel ITC case). The ITC may not even reach the issue of invalidity. *See, e.g.*, *Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).

VIII. MANDATORY NOTICES

Real Party-in-Interest: Petitioners identify the following as the real parties-in-interest: TSMC, Apple Inc., Broadcom Inc., and Qualcomm Inc.

Related Matters: The '747 patent is asserted in *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 1:25-cv-00215 (W.D.Tex.), *Longitude Licensing Ltd. et al. v. Lenovo Group Limited et al.*, Case No. 2:25-cv-00171 (E.D.Tex.), and *Longitude Licensing Ltd. et al. v. Apple, Inc. et al.*, Case No. 337-3809 (ITC).

Counsel and Service Information:

Petitioners identify the following lead and backup counsel and Petitioners each consents and requests that all service and correspondence to them respectively and/or collectively in this matter be electronically provided at the below-provided e-mail addresses.

Lead counsel: Naveen Modi (Reg. No. 46,224)(counsel for TSMC)

Backup counsel:

Counsel for TSMC:

(1) Joseph E. Palys (Reg. No. 46,508);

(2) Joseph Rumpler (Reg. No. 71,544);

(3) Jacob Rothenberg (Reg. No. 77,891);

(4) Howard Herr (*pro hac vice* to be requested); and

(5) Jeremy S. Rashid (Reg. No. 76,229).

Service information: Paul Hastings LLP, 2050 M St., Washington, D.C., 20036, Tel.: 202.398.1700, Fax: 202.398.1705, email: **PH-TSMC-Marlin-IPR@paulhastings.com**.

Counsel for Apple Inc.:

(1) W. Karl Renner (Reg. No. 41,265);

(2) Jeremy J. Monaldo (Reg. No. 58,680);

(3) Gretchen DeVries (Reg. No. 72,505).

Service information: Apple consents to electronic service by email at IPR50095-0269IP1@fr.com (referencing No. 50095-0269IP1 and cc'ing PTABInbound@fr.com, axf-ptab@fr.com, jjm@fr.com, and devries@fr.com).

IX. PAYMENT OF FEES

The PTO is authorized to charge any fees during this proceeding to Deposit Account No. 50-2613.

X. GROUNDS FOR STANDING

Petitioners certify that the ’747 patent is available for review, and they are not barred/estopped from requesting review on the identified grounds.

XI. CONCLUSION

For the reasons above, Petitioners request IPR be instituted.

Respectfully submitted,

Dated: April 17, 2025

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner TSMC

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,147,747 contains, as measured by the word-processing system used to prepare this paper, 13,984 words. This word count does not include the items excluded by 37 C.F.R. §42.24 as not counting towards the word limit.

Respectfully submitted,

April 17, 2025

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202-551-1700

Counsel for Petitioner TSMC

CERTIFICATE OF SERVICE

I hereby certify that on April 17, 2025, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,147,747 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on Patent Center:

NORTH AMERICAINTELLECTUAL PROPERTY CORPORATION
5F., NO.389, FUHE RD., YONGHEDIST.
NEW TAIPEI CITY, 234645
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XII. APPENDIX A (CLAIM LISTING)

Claim 1

[1.a] A semiconductor structure, comprising:

[1.b] a substrate;

[1.c] a first dielectric layer disposed on the substrate;

[1.d] at least two metal gates disposed in the first dielectric layer;

[1.e] a spacer disposed on two sides of the metal gate, wherein the spacer has a truncated top surface;

[1.f] a source/drain region (S/D region) disposed between two metal gates;

[1.g] a plurality of first contacts disposed in the first dielectric layer that are electrically connected to parts of the S/D region;

[1.h] a plurality of second contacts disposed in the first dielectric layer that are electrically connected to one of the metal gates, wherein at least one of the first contacts directly connects at least one of the second contacts; and

[1.i] a hard mask disposed on one of the metal gates, wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

Claim 2

The semiconductor device of claim 1, further comprising a second dielectric layer disposed on the first dielectric layer.

Claim 3

The semiconductor device of claim 2, further comprising an etching stop layer disposed on two sides of the metal gate, and the etching stop layer has a truncated top surface.

Claim 4

The semiconductor device of claim 2, wherein the first contacts disposed in the first dielectric layer and in the second dielectric layer and each first contact is a monolithically formed structure.

Claim 5

The semiconductor device of claim 2, wherein the second contacts disposed in the first dielectric layer and in the second dielectric layer and each second contact is a monolithically formed structure.

Claim 6

The semiconductor device of claim 1, further comprising at least one fin structure disposed on the substrate.

Claim 7

The semiconductor device of claim 1, further comprising a salicide layer disposed between each S/D region and each first contact.

Claim 8

The semiconductor device of claim 3, further comprising a plurality of third contacts disposed on parts of the first contacts and on parts of the second contacts, wherein each third contact is a monolithically formed structure.

Claim 9

The semiconductor device of claim 8, wherein each third contact comprises a via hole structure and a trace structure, wherein the via hole structure and the trace structure comprise the same material and contact each other directly.