

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
and APPLE INC.
Petitioners,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-00865
U.S. Patent No. 9,147,747 B2

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph McAlexander
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)
2003	Merriam-Webster's Collegiate Dictionary (10th ed. 1999)

I. Introduction

The Board should deny institution because no grounds establish the required reasonable likelihood of success against any challenged claim. For example, Grounds 1A-5B fail to identify any the “spacer has a truncated top surface” found in every challenged claim, while the remaining Grounds 6-9 fail to establish—or even to assert—that any of the references have the claimed “at least two metal gates” found in in every challenged claim.

Grounds 1A-5B: *Pethe* is the primary reference in Grounds 1A-5B, and each of these *Pethe* grounds relies solely on *Pethe* as disclosing the “spacer has a **truncated** top surface”¹ limitation found in every challenged claim. But *Pethe* does not describe or disclose a spacer with a truncated top.

To be “truncated,” the spacer must first be formed at one height and then shortened by removing material from its top. *Pethe* describes one embodiment in which spacers are shorter than corresponding spacers in a different embodiment. But *Pethe* does not describe that these shorter spacer examples were truncated (i.e., made shorter by removing material from their tops) as opposed to simply formed shorter in the first place. Accordingly, *Pethe* does not disclose the required

¹ Unless otherwise indicated, all emphases in quotations is added.

“truncated” spacer and each of these *Pethe* grounds fails to establish the required reasonable likelihood of success.

Grounds 6-9: *Chang* is the primary reference in Grounds 6-9, each of which relies solely on *Chang* as teaching the claimed “at least two gates” and their accompanying required characteristics. But *Chang* does not teach the claimed gates and all their required features—and the Petition does not contend otherwise. Instead, the Petition asserts that one pair of *Chang* gates meets some of the claimed gates’ required features, but that a different pair of *Chang* gates meets the claimed gate’s other required features.

All of the claims require that the “at least two metal gates” have at least three claimed features:

- (1) the two gates have a source/drain region between them,
- (2) at least one of those gates has a hard mask thereon, and
- (3) each of the gates is electrically connected to one of the second contacts.

But the Petition points to different gates depending on which of these features it is attempting to find in *Chang*. Specifically, the Petition asserts that one set of *Chang* gates (gates 1441 and 1596) has a hard mask disposed thereon and a S/D region between them. But the Petition does not (and cannot) assert that this same set of gates also has the third required feature, that any of *Chang* gates 1441

and 1596 are electrically connected to any of the second contacts. Rather, the Petition asserts different *Chang* gates—gates 1446 and 1597—are connected to the alleged second contacts.

Thus, none of the *Chang* grounds identify—or even allege—the claimed gates, two gates that have the S/D between them, that have a hard mask on at least one of them, **and** that are connected to a second contact. Accordingly, like the *Pethe* grounds, the *Chang* grounds fail to establish the required likelihood of success, and the Petition should be denied.

II. Semiconductor Transistor Technology Primer

The '747 Patent generally discloses improved structures and methods for fabricating semiconductor transistors, including improved designs for contact structures for interconnecting transistors or components. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (e.g., fin) transistors; and (3) common process steps for creating transistors.

A. Basic Transistor Components

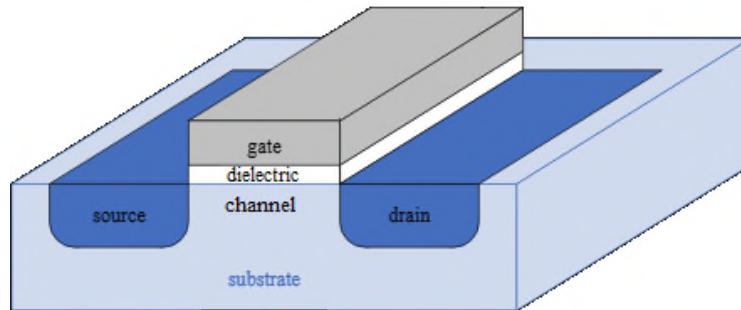
Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical

functions: switching (i.e., turning electrical current on and off) and amplification (i.e., increasing the amplitude of a signal while retaining its electrical characteristics). (EX2002 at 1-2). Where earlier tube devices used a vacuum to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. (EX2002 at 3; EX2001, ¶6).

One type of transistor typically used in an integrated circuit (or “chip”) is a “field effect transistor,” or FET. Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. (EX2002 at 29-34). In a conductor (e.g., a metal), electric current can flow freely. (EX2002 at 29). A dielectric (e.g., silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. (EX2002 at 30). Semiconductors (e.g., silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. (EX2002 at 31-34; EX2001, ¶7).

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. (See, e.g., EX2002 at 510-511). The source, drain and channel comprise

semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



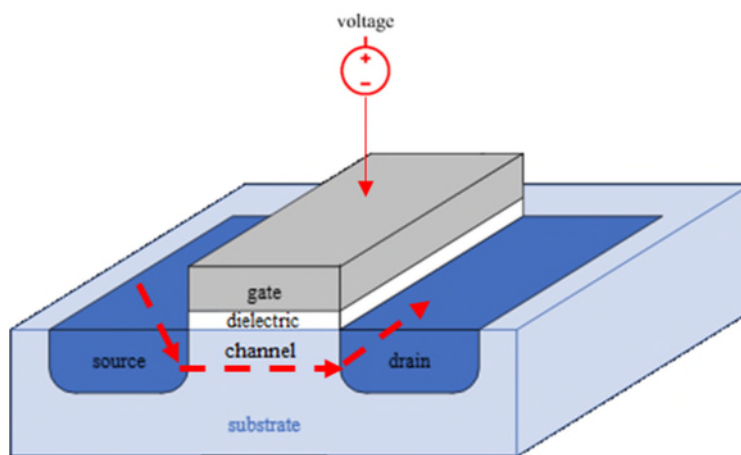
(See, e.g., EX2002 at 510-511; EX2001, ¶8).

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). (EX2002 at 34-36, 510-511). The channel is a region under the gate and between the source and drain and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). (EX2002 at 510-511; EX2001, ¶9).

The gate is a conductor located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. (EX2002 at 510-511). When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation of a “field effect” in the channel. (EX2002 at 510-511). This “field effect” either

builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). (EX2002 at 510-511; EX2001, ¶10).

As illustrated below, this field effect allows electrical current to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping the flow of electrical current. (EX2001, ¶11).



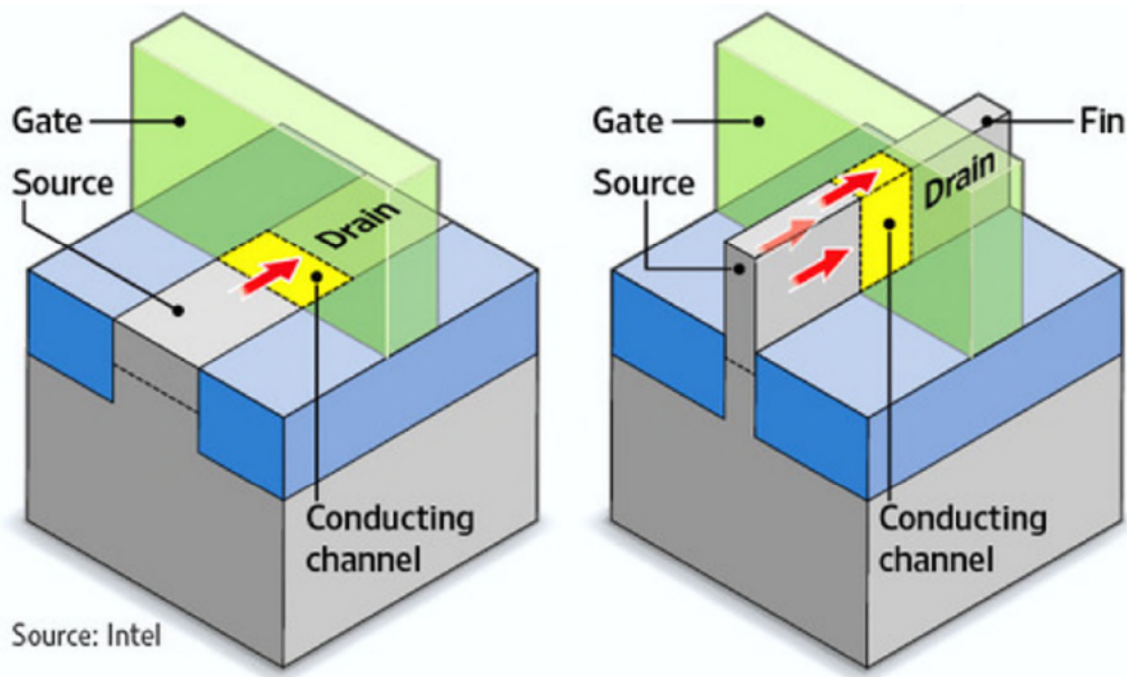
B. Planar vs. Three-Dimensional Transistors

Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more on a chip has been constant

and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.” (EX2001, ¶12).

The simplified illustrative FET transistors illustrated in the previous section all feature a gate built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors. (EX2001, ¶13).

In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



(EX2001, ¶14).

In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.

Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip. In addition, because FinFETs typically leak less current than planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip. (EX2001, ¶16).

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. (EX2001, ¶17).

In the first stage, the semiconductor material itself is created. (EX2002 at 13). For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. (EX2002 at 13; EX2001, ¶18).

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” (EX2002 at 13-14). A wafer acts as a semiconductor substrate on and in which transistors may be formed. (EX2001, ¶19).

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. (EX2002 at 14). Thousands of integrated circuits can be formed on the substrate of a single wafer. (EX2002 at 14; EX2001, ¶20).

In the packaging stage, the wafer is separated into individual chips. (EX2002 at 14-15; EX2001, ¶21).

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in the wafer’s substrate. (EX2002 at 14). These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning,

doping, and heat treatments). (See EX2002 at 29-31, 71). For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. (EX2001, ¶22).

Layering is the operation used to add thin layers to the semiconductor substrate. (EX2002 at 72). The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. (EX2002 at 72; EX2001, ¶23).

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. (EX2002 at 72; EX2001, ¶24).

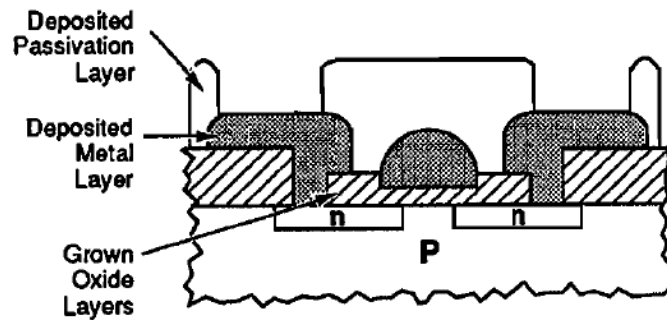


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. (EX2002 at 72-73). This creates a pattern on the wafer surface. (EX2002 at 72-73; EX2001, ¶25).

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. (EX2002 at 72-73; EX2001, ¶26). For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

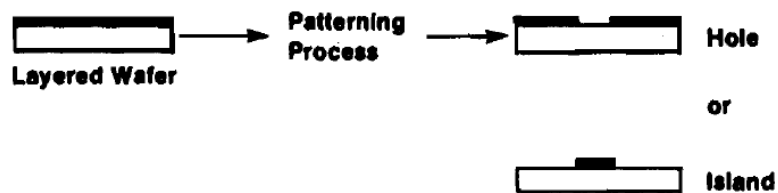


Figure 4.7 Patterning.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

(EX2002 at 73; EX2001, ¶27).

III. The Challenged '747 Patent

The '747 Patent describes the importance of interconnecting contacts in semiconductor devices: “In general, discrete devices in integrated circuits are connected to each other through contact plugs (or contact slots) and interconnection structures, and their related fabrication methods have become an important matter in the next-generation semiconductor devices.” (EX1001 at 1:24-21; EX2001, ¶37).

But the patent also notes that, as semiconductor chips get smaller and smaller, conventional contacts “cannot reach the requirements,” with current

manufacturing being “too complex” and negatively “affecting the conductivity of the contact.” (EX1001 at 1:22-38; EX2001, ¶38).

“[T]o overcome the above-mentioned drawbacks,” the ’747 Patent discloses a new and improved semiconductor device, one featuring, *inter alia*, a truncated spacer and improved contact configurations. (*E.g.*, EX1001 at 1:39-41, claim 1; EX2001, ¶39).

A. An Exemplary ’747 Patent Improved Semiconductor Device

As illustrated below in the annotated Figure 1, the ’747 Patent describes one exemplary method and embodiment as starting with a substrate 10 and fin 16. (EX1001 at 2:39-47). Metal gates 12 (annotated below in orange) are disposed on substrate 10, with a source/drain (“S/D”) region 14 (annotated in yellow) positioned in the fin and between gates:

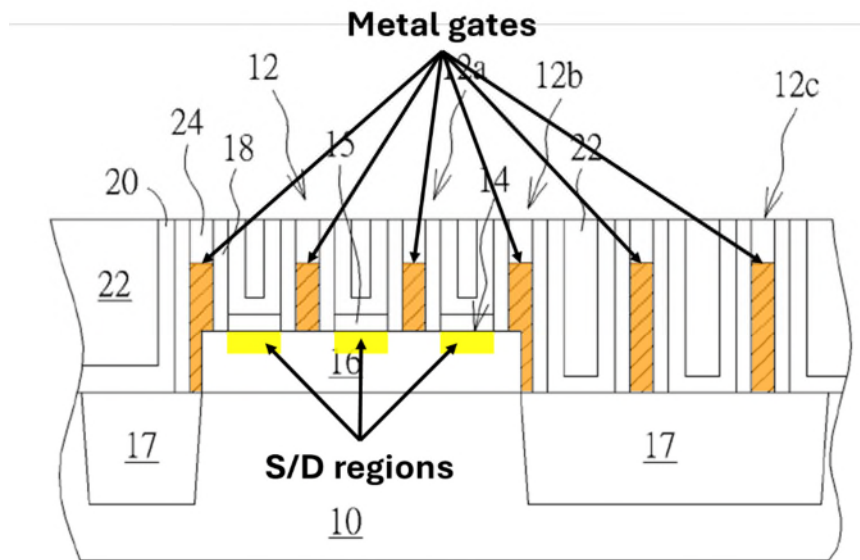


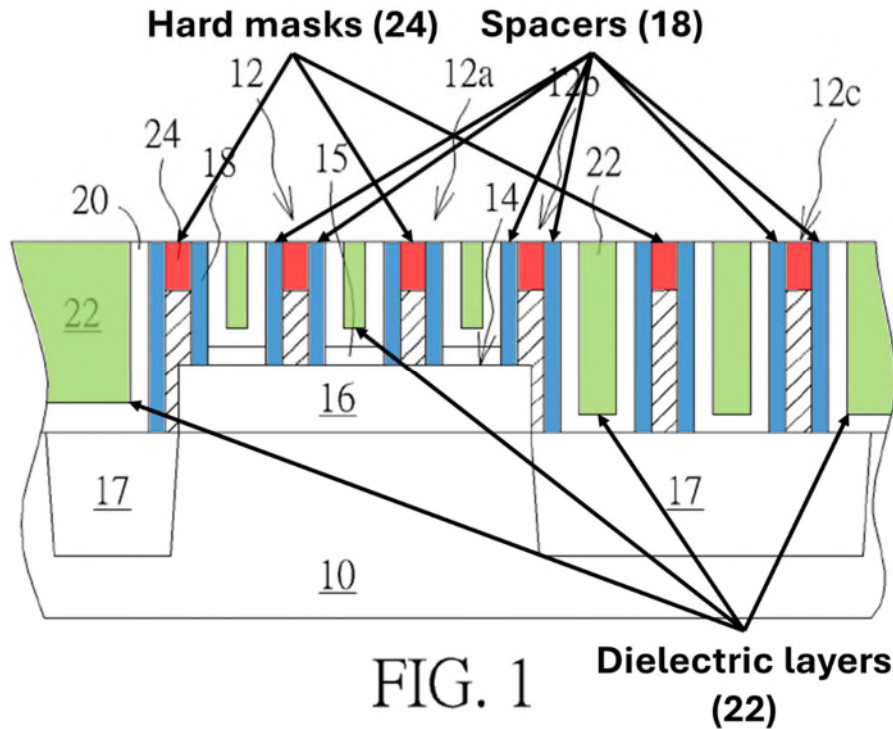
FIG. 1

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(EX1001 at Fig. 1, 2:39-52; EX2001, ¶40).

Additionally, using layering and patterning techniques, a spacer 18 (blue) is formed on two sides of each gate, and a hard mask 24 (shown below red) is formed on the metal gates. A dielectric layer 22 (green) is then formed on the substrate:

² Unless otherwise indicated, all colors and annotations to the challenged patent's figures are added.



(EX1001 at Fig. 1, 2:65-3:19; EX2001, ¶41).

Importantly, spacers 18 and hard masks 24 are not originally formed as depicted in Figure 1. Rather, as the '747 Patent describes, layering is first used to form the spacer and masks at heights taller than their heights shown in Figure 1. But those original spacer and hard mask structures are then patterned, with parts of their tops etched away, thereby shortening them so that their top surfaces are on the same level as the top surface of the dielectric layer 22. (EX1001 at 3:4-19). This results in the spacer having a truncated top surface: “since parts of the spacer 18 . . . are removed during another planarization process, . . . the spacer 18 [has] a truncated top surface”:

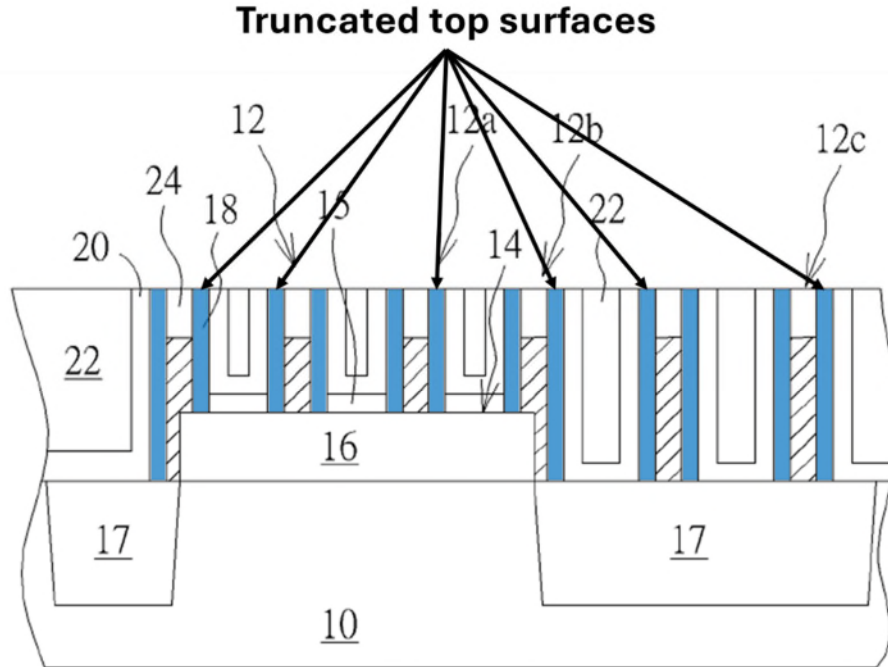


FIG. 1

(EX1001 at Fig. 1, 3:4-19; EX2001, ¶42).

The '747 Patent further describes using layering and patterning techniques to first create trenches and to then form contacts therein. (*E.g.*, EX1001 at 3:47-60, 4:49-5:30). For example, annotated Figure 5 illustrates the result of using patterning techniques to form trenches 32, some of which lead towards S/D region 14. (EX1001 at Figs. 4-5, 3:48-60, 4:22-24). As shown, after these trenches 32 are patterned, conductive salicide layers 34 (annotated in grey) are formed at their bottoms:

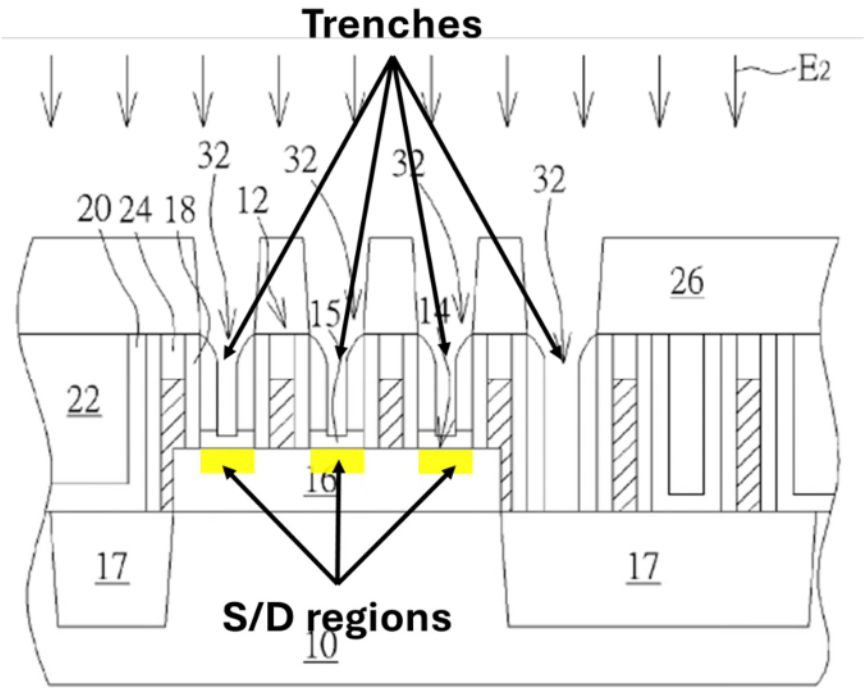


FIG. 4

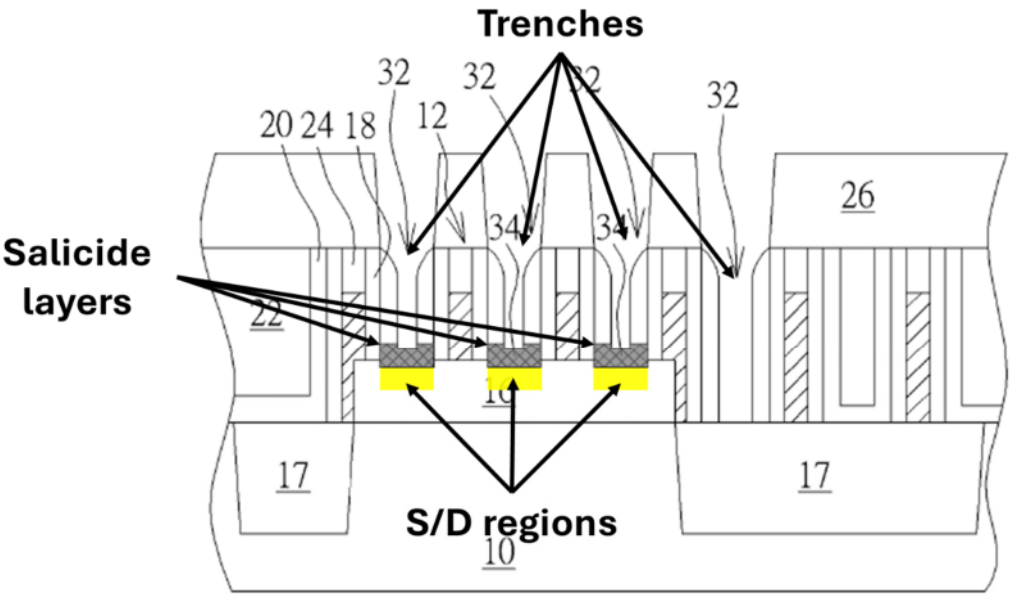
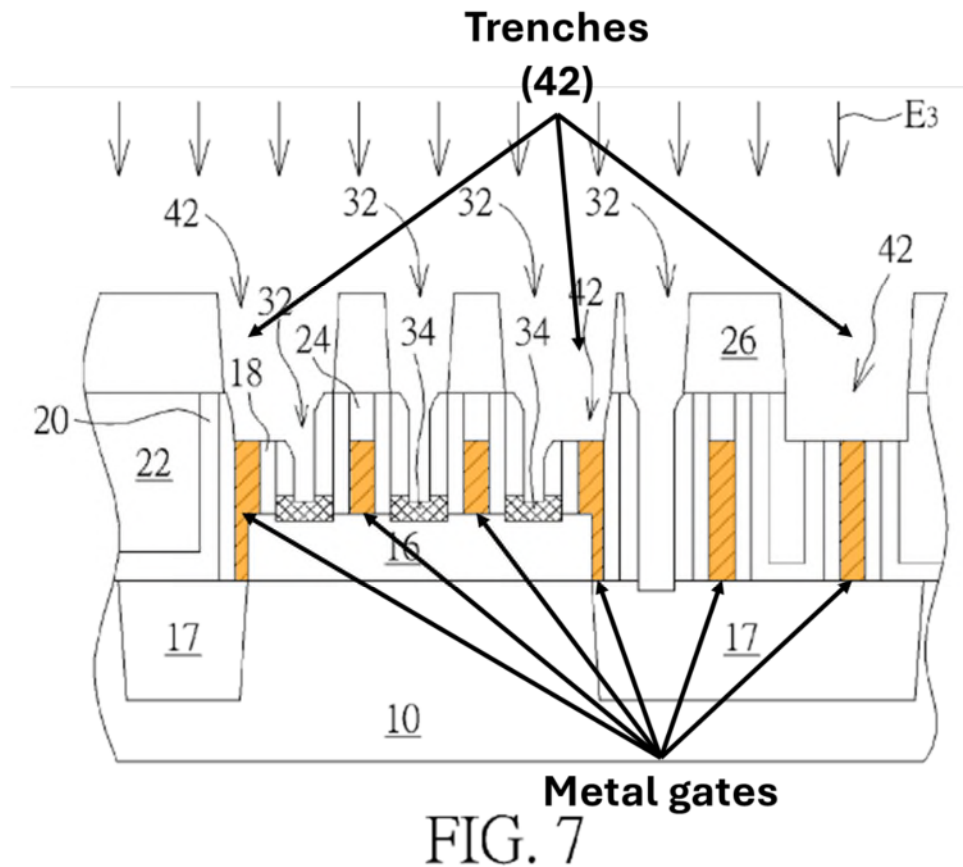


FIG. 5

(EX1001 at Figs. 4-5, 3:48-60, 4:22-24; EX2001, ¶43).

Similarly, annotated Figure 7 illustrates the result of using patterning techniques to form trenches 42, some of which lead towards a metal gate 12:



(EX1001 at Fig. 4, 4:49-67; EX2001, ¶44).

Trenches 32 and 42 are then used to form contacts. As the patent describes, barrier layers 44 and metal layers 46 are deposited within each trench 32, thereby forming a set of first contacts 52 (annotated below in pink) that are “electrically connected [through the salicide layers] to parts of the S/D region”:

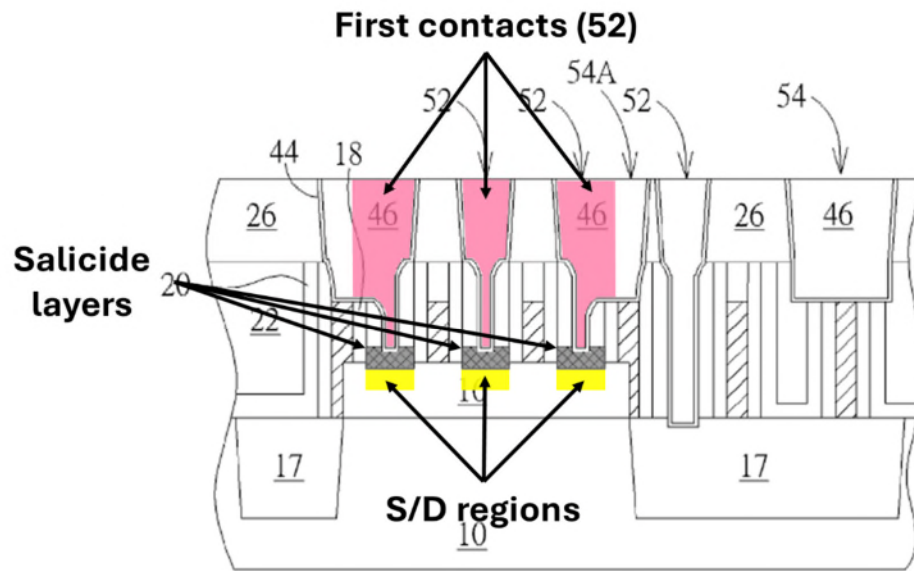
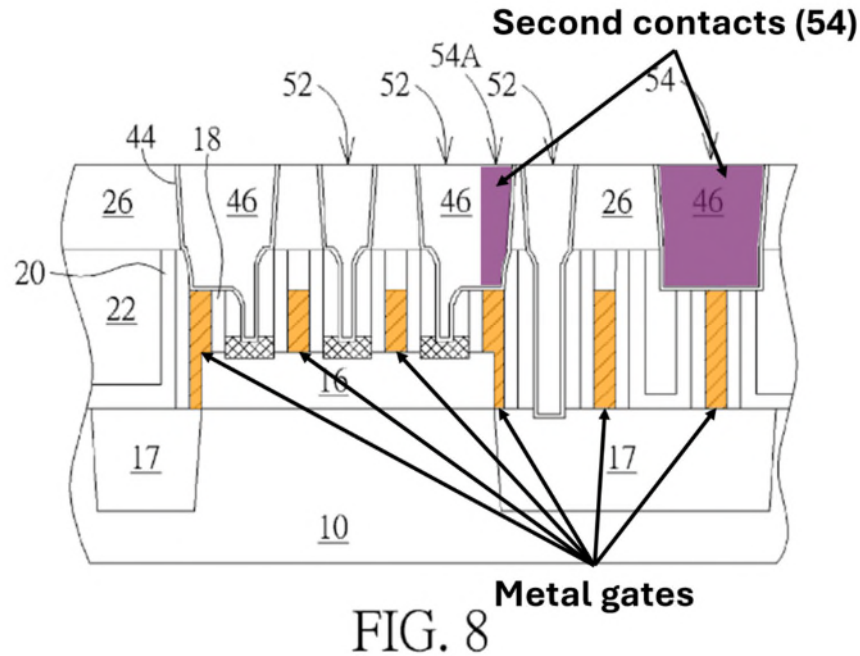


FIG. 8

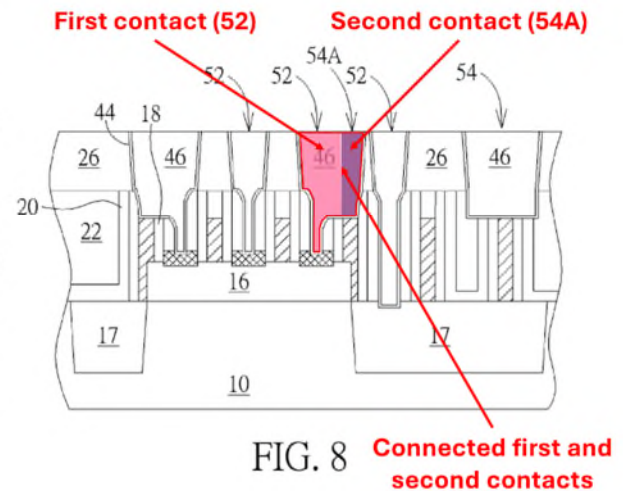
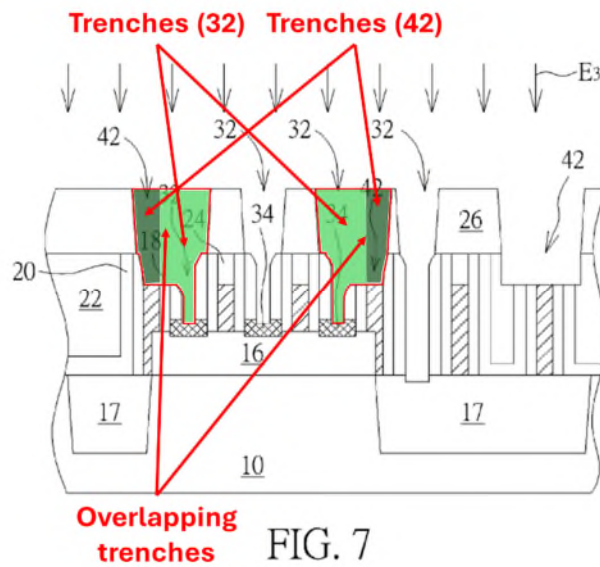
(EX1001 at Fig. 8, 5:1-16; EX2001, ¶45).

In addition, barrier layers 44 and metal layers 46 also are deposited within each trench 42, thereby forming a set of second contacts 54 (annotated below in purple) that are “electrically connected to parts of the metal gate 12”:



(EX1001 at Fig. 8, 5:1-19; EX2001, ¶46).

Another feature of these contacts is that at least one of the first contacts connects to one of the second contacts. As shown below in annotated Figure 7, in at least one instance, a trench 42 is positioned and formed so that it at least partially overlaps with a trench 32. Accordingly, as shown in annotated Figure 8, when these trenches are filled to create their respective first contact 52 and second contact 54, part of that first contact is connected to at least part of the second contact, “such as the second contact 54A”:



(EX1001 at Fig. 4, 4:49-67; EX2001, ¶47).

B. The Challenged Claims

The Petition challenges all of the '747 Patent's claims, namely independent claim 1 and its dependent claims 2-9. Consistent with the foregoing embodiment, each claim is directed towards an innovative semiconductor structure that includes, among other things:

- (1) a spacer having a truncated top; and
- (2) at least two metal gates having multiple required features, including
 - (a) the two gates have a S/D region between them,
 - (b) at least one of those gates has a hard mask thereon, and
 - (c) each of those gates is electrically connected to one of the second contacts.

For example, exemplary claim 1 recites:

1. A semiconductor structure, comprising:
 - a substrate;
 - a first dielectric layer disposed on the substrate;
 - at least two metal gates** disposed in the first dielectric layer;
 - a spacer disposed on two sides of the metal gate, wherein **the spacer has a truncated top surface;**
 - a source/drain region (S/D region) disposed between two metal gates;**
 - a plurality of first contacts; disposed in the first dielectric layer that are electrically connected to parts of the S/D region;
 - a plurality of second contacts** disposed in the first dielectric layer **that are electrically connected to one of the metal gates,** wherein at least one of the first contacts directly connects at least one of the second contacts; and
 - a hard mask disposed on one of the metal gates,** wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

(EX1001 at claim 1).

IV. PTAB Should Deny The Petition Because It Fails To Establish The Required Likelihood Of Success

The Petition asserts eleven different grounds against various selections of claims:

Ground	Claim(s) Challenged	35 U.S.C. §	Reference(s)
1A/1B	1-5, 8	102/103	Pethe
2	6,7	103	Pethe
3	7	103	Pethe + Bohr
4	8-9	103	Pethe + Huang
5A/5B	1-2	102/103	Chang
6	4-6	103	Chang
7	3, 8-9	103	Chang + Huang
8	4-5	103	Chang + Hong
9	7	103	Chang + Bohr

The Petition should be denied because, among other reasons, none of these grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teach or make obvious each limitation in any challenged claim. (EX2001, ¶51).

Grounds 1A-5B: *Pethe* is the primary reference in Grounds 1A-5B, and each of these *Pethe* grounds relies solely on *Pethe* as disclosing the “spacer has a **truncated** top surface” limitation found in every challenged claim. But *Pethe* does not describe or disclose a spacer with a truncated top. (EX2001, ¶52).

To be “truncated,” the spacer must first be formed at one height and then shortened by removing material from its top. *Pethe* describes one embodiment in which spacers are shorter than corresponding spacers in a different embodiment. But *Pethe* does not describe that these shorter spacer examples were truncated (i.e., made shorter by removing material from their tops) as opposed to simply formed

shorter in the first place. Accordingly, *Pethe* does not disclose the required “truncated” spacer and each of these *Pethe* grounds fails to establish the required reasonable likelihood of success. (EX2001, ¶53).

Grounds 6-9: *Chang* is the primary reference in Grounds 6-9, each of which relies solely on *Chang* as teaching the claimed “at least two gates” and their accompanying required characteristics. But *Chang* does not teach the claimed gates and all of their required features, and the Petition does not contend otherwise. Instead, the Petition asserts that one pair of *Chang* gates meets some of the claimed gates’ required features, but that a different pair of *Chang* gates meets the claimed gate’s other required features. (EX2001, ¶54).

All of the claims require that the “at least two metal gates” have at least three claimed features:

- (1) the two gates have a source/drain region between them,
 - (2) at least one of those gates has a hard mask thereon, and
 - (3) each of the gates is electrically connected to one of the second contacts.
- (EX2001, ¶55).

But the Petition points to different gates depending on which of these features it is attempting to find in *Chang*. Specifically, the Petition asserts that one set of *Chang* gates (gates 1441 and 1596) has a hard mask disposed thereon and a

S/D region between them. But the Petition does not (and cannot) assert that this same set of gates also has the third required feature, that any of *Chang* gates 1441 and 1596 are electrically connected to any of the second contacts. Rather, the Petition asserts different *Chang* gates—gates 1446 and 1597—are connected to the alleged second contacts. (EX2001, ¶56).

Thus, none of the *Chang* grounds identify—or even allege—the claimed gates, two gates that have the S/D between them, that have a hard mask on at least one of them, **and** that are connected to a second contact. Accordingly, like the *Pethe* grounds, the *Chang* grounds fail to establish the required likelihood of success, and the Petition should be denied. (EX2001, ¶57).

A. Grounds 1A-5B: *Pethe* Does Not Disclose The Claimed Spacer With A Truncated Top Surface

Each challenged claim requires that the claimed spacer have a truncated” top surface, claiming (among other things):

at least two metal gates disposed in the first dielectric layer;

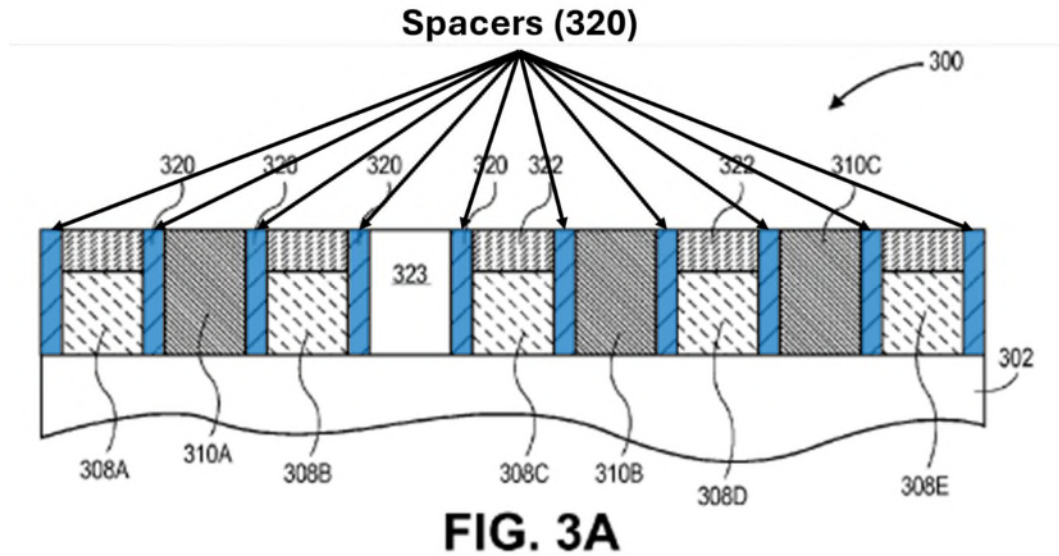
a spacer disposed on two sides of the metal gate, wherein **the spacer has a truncated top surface;**

(*E.g.*, EX1001 at claim 1). Grounds 1A-5B rely solely on *Pethe* as disclosing this limitation, but *Pethe* does not describe a spacer as having a truncated top surface. (*E.g.*, Petition at 23; EX2001, ¶58).

Something that has been “truncated” has been made shorter by removing a part. (EX2003 at 4 (defining “truncated” as “to shorten by or as if by cutting off”). The Petition identifies *Pethe*’s spacer 520 as the claimed spacer and contends that spacer 520 was “truncated by removing material from the feature’s top surface.” (Petition at 23). But *Pethe* does not describe any such truncating or shortening of spacer 520, and the Petition identifies no such description. (Petition at 23; EX2001, ¶59).

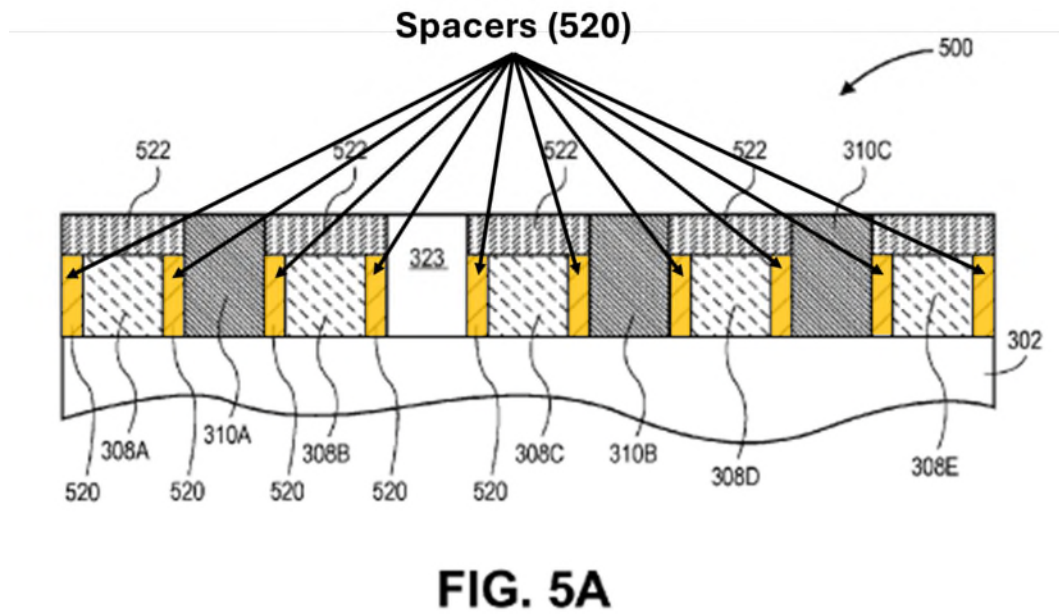
Rather, *Pethe* merely compares the height of spacer 520 relative to a spacer in a different embodiment, describing that spacers 520 is shorter compared to that other spacer. (EX1005 at 12:48-51). But contrary to the Petition, *Pethe* does not disclose how spacer 520 was made relatively shorter, and *Pethe* does not describe any truncating process being performed on spacer 520. (EX2001, ¶60).

Specifically, in one embodiment, *Pethe* describes spacers 320, annotated in blue in the following Figure 3A from *Pethe*:



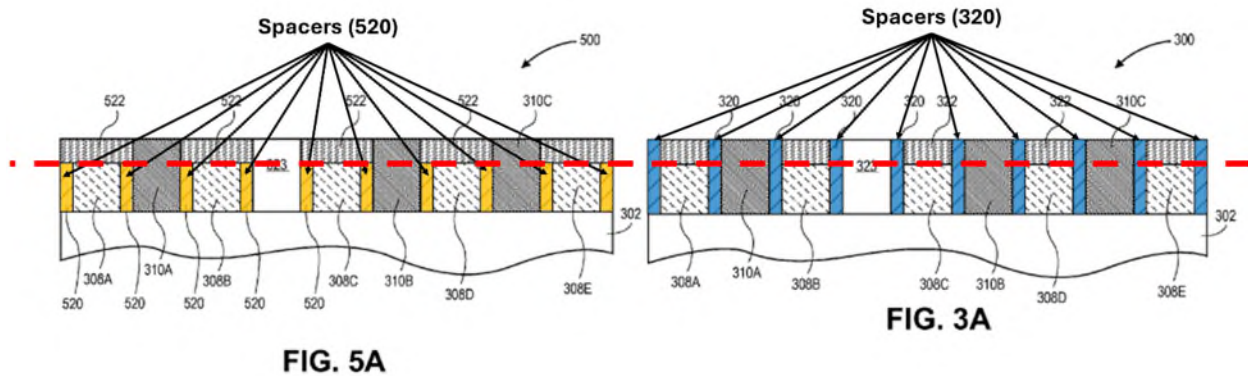
(EX1005 at Fig. 3A, 12:15-17; EX2001, ¶61).

Pethe describes a different embodiment that includes spacers 520 (annotated in orange below), which the Petition alleges disclose the claimed spacer:



(EX1005 at Fig. 5A, 13:42-45; EX2001, ¶62).

Pethe further describes that these spacers 520 are shorter (“recessed”) relative to spacers 320:



(EX1005 at Figs. 3A & 5A, 12:48-51; EX2001, ¶63).

But contrary to the Petition, *Pethe* does not describe that spacers 520 are made shorter than spacers 320 by first forming spacers 520 taller and then etching away their top material. (See Petition at 23-24). The Petition identifies no such description in *Pethe* of any such process being used to make spacers 520. (*E.g.*, Petition at 23-24; EX2001, ¶64).

The Petition cannot because *Pethe* includes no such description—*Pethe* does not describe that these shorter spacer examples were truncated (i.e., made shorter by removing material from their tops) as opposed to simply formed shorter in the first place. Accordingly, *Pethe* does not disclose the required “truncated” spacer and each of these *Pethe* grounds fails to establish the required reasonable likelihood of success. (EX2001, ¶65).

B. Grounds 6-9: Chang Does Not Disclose The Claimed At Least Two Metal Gates

Each challenged claim requires that the “at least two metal gates” have at least three claimed features:

- (1) the two gates have a source/drain region between them,
- (2) at least one of those gates has a hard mask thereon, and
- (3) each of the gates is electrically connected to one of the second contacts.

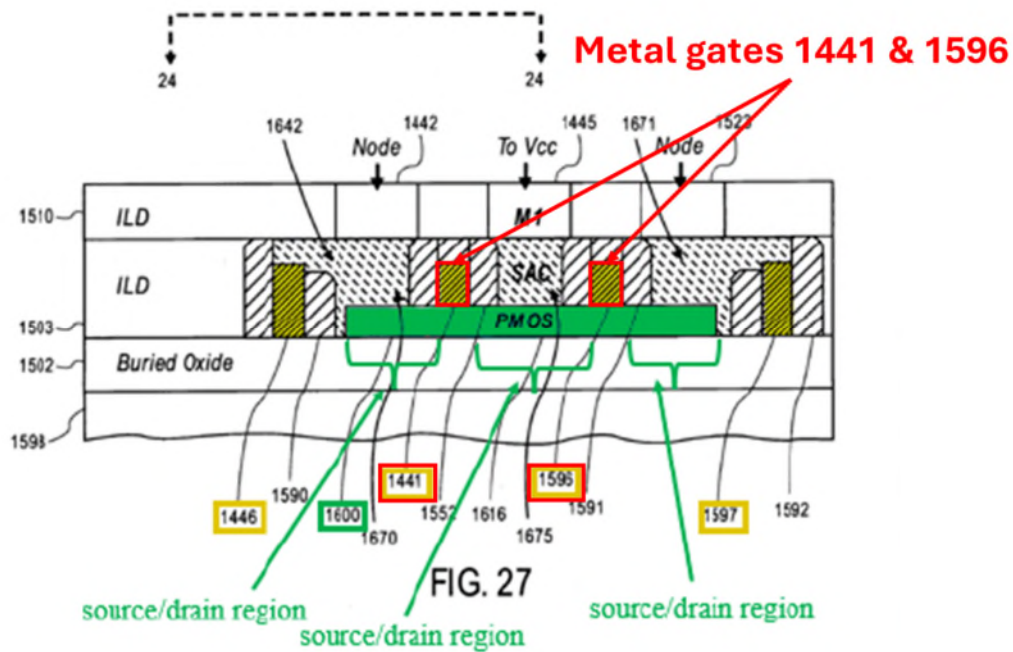
(EX1001 at claim 1; EX2001, ¶66). For example, challenged independent claim 1 (from which all other challenged claims depend) recites the following requirements for the claimed “at least two metal gates”:

1. A semiconductor structure, comprising:
 - a substrate;
 - a first dielectric layer disposed on the substrate;
 - at least two metal gates** disposed in the first dielectric layer;
 - a spacer disposed on two sides of the metal gate, wherein **the spacer has a truncated top surface;**
 - a source/drain region (S/D region) disposed between two metal gates;**
 - a plurality of first contacts; disposed in the first dielectric layer that are electrically connected to parts of the S/D region;
 - a plurality of second contacts** disposed in the first dielectric layer **that are electrically connected to one of the metal gates,** wherein at least one of the first contacts directly connects at least one of the second contacts; and
 - a hard mask disposed on one of the metal gates,** wherein the top surface of the hard mask and the top surface of the first dielectric layer are on the same level.

(EX1001 at claim 1).

Grounds 6-9 each rely solely on *Chang* as teaching the claimed “at least two gates” and their foregoing accompanying required characteristics. But *Chang* does not teach the claimed gates and all of their required features, and the Petition does not contend otherwise. Instead, the Petition asserts that one pair of *Chang* gates meets some of the claimed gates’ required features, but that a different pair of *Chang* gates meets the claimed gate’s other required features. (EX2001, ¶67).

For example, the Petition points to *Chang* gates 1441 and 1596 as gates that meet two of the claimed gate requirements: (1) a S/D region between the gates and (2) a hard mask disposed on one of the gates. The Petition’s first annotated *Chang* Figure 27 illustrates the Petition’s allegation that *Chang* discloses “a source/drain region (S/D region) disposed between the two metal gates 1441, 1596:

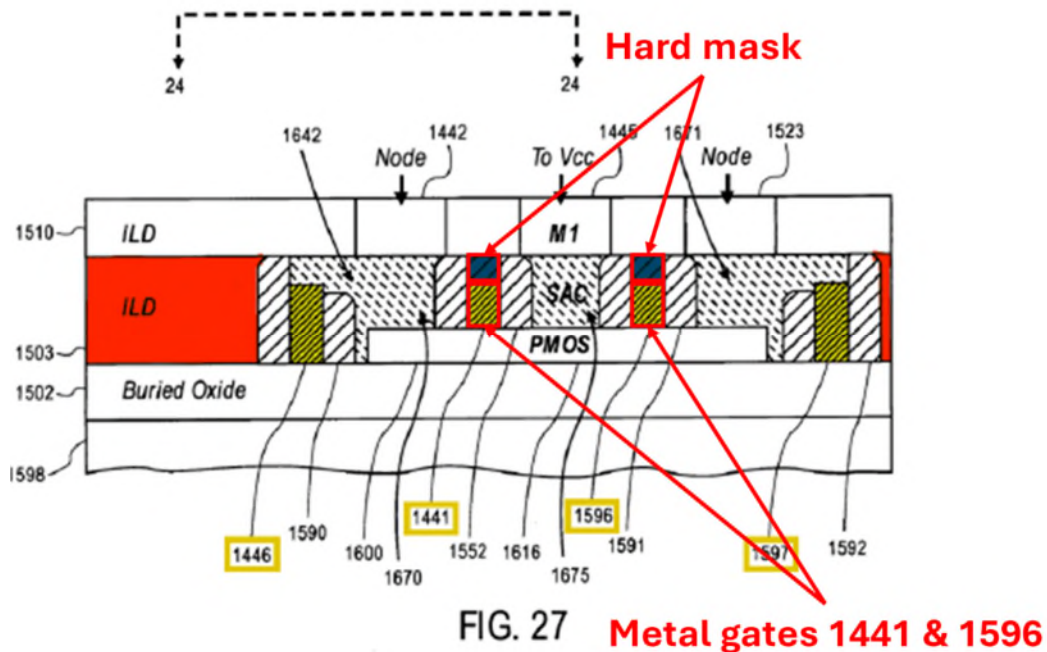


(Petition at 74-75; EX1007 at Fig. 27 (all annotations from Petition except red circles and labels identifying the asserted gates); EX2001, ¶¶68).³

The Petition similarly alleges that *Chang* discloses the claimed hard mask on just two *Chang* gates, those same gates 1441 and 1596. The Petition's second

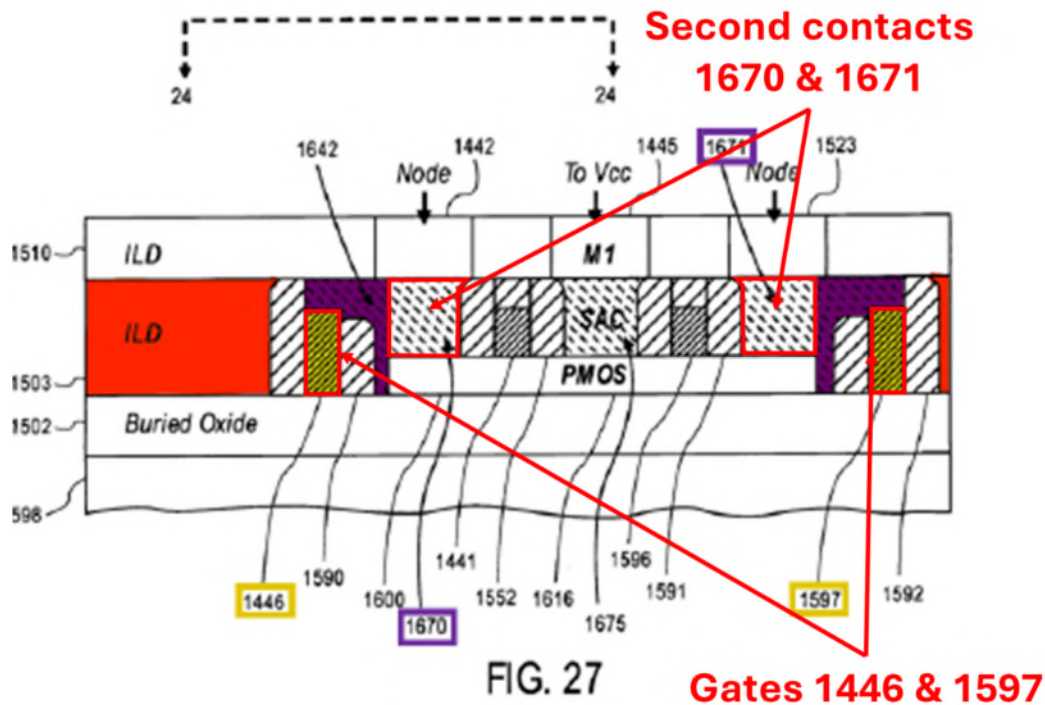
³ This response and the Board need not address whether the Petition's allegations concerning requirements such as the location and existence of the alleged *Chang* source/drain regions, hard masks, and second contacts are correct because, as established in this section, even if true, those allegations do not establish the required likelihood of success.

annotated Figure 27 illustrates its allegation that Chang discloses “a hard mask disposed on gates 1441 and 1596”:



(Petition at 80; EX1007 at Fig. 27 (all annotations from Petition except red circles and labels identifying the asserted gates and hard masks) ; EX2001, ¶69).

But the Petition does not (and cannot) assert that this same set of gates also has the third required feature, that either *Chang* gate 1441 or 1596 is electrically connected to any of the second contacts. (Petition at 77-78). Rather, the Petition asserts only that two different *Chang* gates—gates 1446 and 1597—are connected to the alleged second contacts. The Petition’s third annotated Figure 27 illustrates its assertion that “parts of self-aligned contacts 1670, 1671 ... that are a plurality of contacts electrically connected to gates 1446, 1597”:



(Petition at 77-78; EX1007 at Fig. 27 (all annotations from Petition except red circles and labels identifying the asserted gates and second contacts); EX2001, ¶70).

Thus, *Chang* does not teach the claimed at least two metal gates having all of their required features, and the Petition does not contend otherwise. Instead, the Petition asserts that one pair of *Chang* gates (circled in green below) meets some of the claimed gates' required features, but that a different pair of *Chang* gates (circled in purple) meets the claimed gate's other required features:

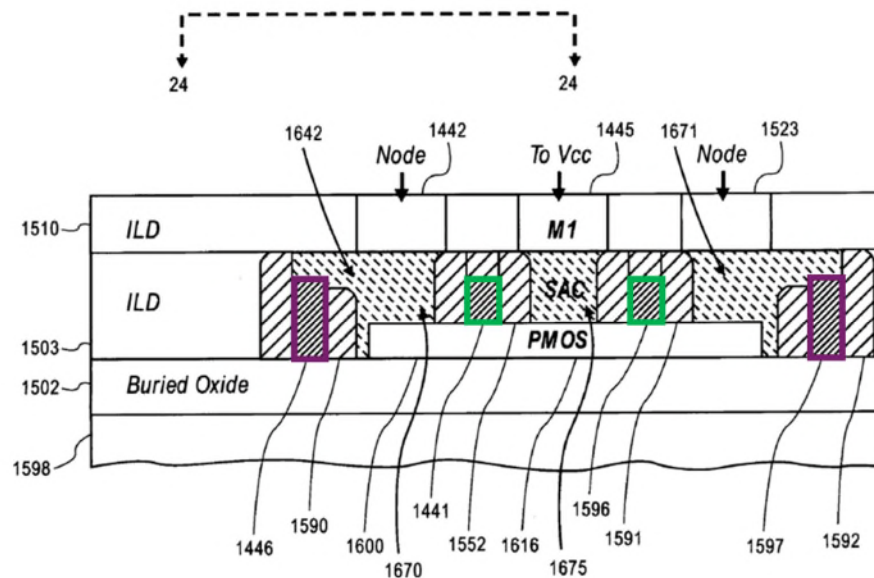


FIG. 27

(EX1007 at Fig. 27; EX2001, ¶71).

Nor does the Petition even argue, much less prove, that it would be obvious to combine the features of these different gates to arrive at the claimed gates. Instead, the Petition relies on its sleight of hand going unnoticed. It should not. (EX2001, ¶72).

In sum, none of the *Chang* grounds identify—or even allege—the claimed gates, two gates that have the S/D between them, that have a hard mask on at least one of them, **and** that are connected to a second contact. Accordingly, like the *Pethe* grounds, the *Chang* grounds fail to establish the required likelihood of success, and the Petition should be denied. (EX2001, ¶73).

V. Conclusion

For the foregoing reasons, the Board should deny institution of the Petition.

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/William A. Meunier/

William A. Meunier (Reg. No. 41,193)

Adam S. Rizk (Reg. No. 66,867)

Michael T. Renaud (Reg. No. 44,299)

MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO, P.C.

One Financial Center

Boston, MA 02111

Telephone: 617-348-1793

Facsimile: 617-542-2241

E-mail: WAMeunier@mintz.com

ARizk@mintz.com

MTRenaud@mintz.com

Mintz-Marlin-IPRs@mintz.com

Reza Dokhanchy (Reg. No. 62,795)

MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO, P.C.

3580 Carmel Mountain Road, Suite 300

San Diego, CA 92130

Telephone: 858-314-1500

RDokhanchy@mintz.com

Tawfik Goma (Reg. No. 67,416)

MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO, P.C.

777 Brickell Avenue, Suite 500

Miami, FL 33131

Tel: (786) 949-6600

TAGoma@mintz.com

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*Counsel to Patent Owner Marlin
Semiconductor Ltd.*

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 4,857. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

Dated: August 15, 2025

/William A. Meunier/

William A. Meunier (Reg. No. 41,193)

CERTIFICATE OF SERVICE

I certify that copies of Patent Owner's Preliminary Response and accompanying Exhibits 2001 through 2003 are being served by electronic mail on the following counsel of record:

Naveen Modi (Reg.# 46,224)
Joseph E. Palys (Reg.# 46,508)
Howard Herr (*pro hac vice* to be requested)
Joseph Rumpler (Reg.# 71,544)
Jeremy S. Rashid (Reg.# 76,229)
Jacob Rothenberg (Reg.# 77,891)
Paul Hastings LLP
2050 M Street NW
Washington, DC 20036
Tel: (202) 551-1700
PH-TSMC-Marlin-
IPR@paulhastings.com

W. Karl Renner (Reg.# 41,265)
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
PTABInbound@fr.com
IPR50095-0269IP1@fr.com
axf-ptab@fr.com

Jeremy J. Monaldo (Reg.# 58,680)
Fish & Richardson P.C.
1000 Maine Ave., S.W., Suite 1000
Washington, DC 20024
Tel: (202) 783-5070
jjm@fr.com

Gretchen DeVries (Reg.# 72,505)
Fish & Richardson P.C.
7 Times Square, 20th Floor
New York, NY 10036
Tel: (212) 765-5070
devries@fr.com

Dated: August 15, 2025

/William A. Meunier/
William A. Meunier (Reg. No. 41,193)