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P.O. Box 1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/331,229	07/28/2015	9093473	NAUP1220USA1	8157

27765 7590 07/08/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Ming-Te Wei, Changhua County, TAIWAN;
UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN;
Wen-Chen Wu, Kaohsiung City, TAIWAN;
Lung-En Kuo, Tainan City, TAIWAN;
Po-Chao Tsao, New Taipei City, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 05/22/2015

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Shelley Kuo	(Depositor's name)
/Shelley Kuo/	(Signature)
06/24/2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/331,229	07/15/2014	Ming-Te Wei	NAUP1220USA1	8157

TITLE OF INVENTION:

METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$960	\$0	\$0	\$960	08/24/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
MENZ, LAURA MARY	2813	438-197000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Winston Hsu
2 Scott Margo
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

UNITED MICROELECTRONICS CORP.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-3105 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Winston Hsu/

Date 06/22/2015

Typed or printed name Winston Hsu

Registration No. 41,526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		14331229		
Filing Date:		15-Jul-2014		
Title of Invention:		METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		
First Named Inventor/Applicant Name:		Ming-Te Wei		
Filer:		Winston Hsu/Shelley Kuo		
Attorney Docket Number:		NAUP1220USA1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	22692914
Application Number:	14331229
International Application Number:	
Confirmation Number:	8157
Title of Invention:	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR
First Named Inventor/Applicant Name:	Ming-Te Wei
Customer Number:	27765
Filer:	Winston Hsu/Shelley Kuo
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1220USA1
Receipt Date:	24-JUN-2015
Filing Date:	15-JUL-2014
Time Stamp:	04:19:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$960
RAM confirmation Number	7812
Deposit Account	503105
Authorized User	HSU, WINSTON
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NAUP1220USA1_AN_1_NP072.pdf	334234 2abe7f4ddb6c56d5662f499200843f08d29a29be	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30578 f86753f1a255f1ac5b5abfb59e481e4258db95e3b	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			364812		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 05/22/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

MENZ, LAURA MARY

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 05/22/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/331,229	07/15/2014	Ming-Te Wei	NAUP1220USA1	8157

TITLE OF INVENTION: METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/24/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27765 7590 05/22/2015
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/331,229	07/15/2014	Ming-Te Wei	NAUP1220USA1	8157

TITLE OF INVENTION: METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	08/24/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
MENZ, LAURA MARY	2813	438-197000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/331,229	07/15/2014	Ming-Te Wei	NAUP1220USA1	8157
27765 7590 05/22/2015 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER MENZ, LAURA MARY	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 05/22/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/331,229	Applicant(s) WEI ET AL.	
	Examiner LAURA MENZ	Art Unit 2813	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 12/31/14.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-10. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Allowable Subject Matter

Claims 1-10 are allowed.

The following is an examiner's statement of reasons for allowance: Prior art fails to teach nor suggest the limitations of claim 1 in combination as recited therein. More specifically prior art fails to teach nor suggest forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates, in combination with the remaining limitations of claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LAURA MENZ whose telephone number is (571)272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Kraig can be reached on (571) 272-8660. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LAURA MENZ/
Primary Examiner, Art Unit 2813

05/17/15

Notice of References Cited	Application/Control No. 14/331,229	Applicant(s)/Patent Under Reexamination WEI ET AL.	
	Examiner LAURA MENZ	Art Unit 2813	Page 1 of 5

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*	B	US-6,121,080 A	09-2000	Wu, Tsung-Chih	438/238
*	C	US-6,133,151 A	10-2000	Lin, Ching-Fu	438/694
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*	K	US-6,661,043 B1	12-2003	Huang et al.	257/243
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NON-PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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*	B	US-2006/0046407 A1	03-2006	Juengling, Werner	438/301
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*	D	US-2006/0189080 A1	08-2006	Lee et al.	438/261
*	E	US-2006/0258109 A1	11-2006	Juengling, Werner	438/301
*	F	US-7,183,156 B2	02-2007	Goldbach et al.	438/248
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*	K	US-7,312,129 B2	12-2007	Goktepel et al.	438/304
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*	B	US-7,812,399 B2	10-2010	Yuda, Takashi	257/369
*	C	US-2011/0147853 A1	06-2011	Lin et al.	257/379
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	F	US-			
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Issue Classification 	Application/Control No. 14331229	Applicant(s)/Patent Under Reexamination WEI ET AL.	
	Examiner LAURA MENZ	Art Unit 2813	

CPC						
Symbol					Type	Version
H01L		29	/	66689	F	2013-01-01
H01L		21	/	823807	I	2013-01-01
H01L		21	/	823828	I	2013-01-01
H01L		21	/	823864	I	2013-01-01
H01L		29	/	165	I	2013-01-01
H01L		29	/	6656	I	2013-01-01
H01L		29	/	66575	A	2013-01-01
H01L		29	/	66636	I	2013-01-01
H01L		29	/	7834	I	2013-01-01
H01L		29	/	7848	I	2013-01-01
H01L		29	/	7816	I	2013-01-01
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CPC Combination Sets						
Symbol			Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	10	
/LAURA MENZ/ Primary Examiner. Art Unit 2813	5/17/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

Issue Classification 	Application/Control No. 14331229	Applicant(s)/Patent Under Reexamination WEI ET AL.
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US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION											
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED						
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CROSS REFERENCE(S)																	
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																

NONE		Total Claims Allowed:	
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(Assistant Examiner)	(Date)		
/LAURA MENZ/ Primary Examiner. Art Unit 2813	5/17/15	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5



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CONFIRMATION NO. 8157

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/331,229	07/15/2014	438	2813	NAUP1220USA1		
APPLICANTS UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN; INVENTORS Ming-Te Wei, Changhua County, TAIWAN; Wen-Chen Wu, Kaohsiung City, TAIWAN; Lung-En Kuo, Tainan City, TAIWAN; Po-Chao Tsao, New Taipei City, TAIWAN; ** CONTINUING DATA ***** This application is a DIV of 12/837,475 07/15/2010 PAT 8816409 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/24/2014						
Foreign Priority claimed 35 USC 119(a-d) conditions met Verified and Acknowledged	☐ Yes ☒ No ☐ Yes ☒ No /LAURA MARY MENZ/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 3	TOTAL CLAIMS 10	INDEPENDENT CLAIMS 1
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES						
TITLE METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Receipt date: 12/31/2014

14331229 - GAU: 2813

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14331229
	Filing Date	2014-07-15
	First Named Inventor	Ming-Te Wei
	Art Unit	2813
	Examiner Name	MENZ, LAURA MARY
	Attorney Docket Number	NAUP1220USA1

U.S.PATENTS								
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1							
U.S.PATENT APPLICATION PUBLICATIONS								
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Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	200743160	TW		2007-11-16			Abstract
	2	200908325	TW		2009-02-16			Abstract
	3	200931599	TW		2009-07-16			Abstract

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.M./

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NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		
EXAMINER SIGNATURE			
Examiner Signature	/Laura Menz/		Date Considered 05/17/2015
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	Examiner Name	N/A
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	Examiner Name	N/A
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	1		

EXAMINER SIGNATURE

Examiner Signature	/Laura Menz/	Date Considered	05/17/2015
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.M./

Search Notes 	Application/Control No. 14331229	Applicant(s)/Patent Under Reexamination WEI ET AL.
	Examiner LAURA MENZ	Art Unit 2813

CPC- SEARCHED		
Symbol	Date	Examiner
H01L 29/66689H01L 29/7816H01L 29/6656H01L 29/66636H01L 29/7834H01L 29/165H01L 21/823828H01L 21/823864H01L 21/823807H01L 29/7848H01L 29/66575	5/17/15	LM

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
USPAT; JPOABS; EPOABS; DERWENT	5/17/15	LM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L	H01L 29/66689H01L 29/7816H01L 29/6656H01L 29/66636H01L 29/7834H01L 29/165H01L 21/823828H01L 21/823864H01L 21/823807H01L 29/7848H01L 29/66575	5/17/15	LM

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14331229
	Filing Date	2014-07-15
	First Named Inventor	Ming-Te Wei
	Art Unit	2813
	Examiner Name	MENZ, LAURA MARY
	Attorney Docket Number	NAUP1220USA1

U.S.PATENTS								
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1							

U.S.PATENT APPLICATION PUBLICATIONS								
Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1							

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	200743160	TW		2007-11-16			Abstract
	2	200908325	TW		2009-02-16			Abstract
	3	200931599	TW		2009-07-16			Abstract

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NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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	Examiner Name	MENZ, LAURA MARY
	Attorney Docket Number	NAUP1220USA1

CERTIFICATION STATEMENT			
Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):			
☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).			
OR			
☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).			
☐ See attached certification statement.			
☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.			
☒ None			
SIGNATURE			
A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.			
Signature	/Scott Margo/	Date (YYYY-MM-DD)	2014-12-30
Name/Print	Scott Margo	Registration Number	56277

Abstract of TW 200743160

A method of manufacturing a metal oxide semiconductor is provided. It comprises forming an offset spacer, and a disposable spacer around the offset spacer. Then, forms a plurality of epitaxial layers outside the disposable spacer, and removes the disposable spacer. In addition, forms a plurality of source/drain extension areas in the substrate outside the offset spacer and the epitaxial layers. Because the source/drain extension areas are formed after the selective epitaxy growth process, the thermal of the selective epitaxy growth process doesn't damage the source/drain extension areas.

200743160

200743160

發明專利說明書

(本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫)

※ 申請案號： 95-117120

※ 申請日期： 95.5.15

※IPC 分類： H01L 21/336

一、發明名稱：(中文/英文)

一種金氧半導體電晶體和互補式金氧半導體電晶體的製作方法 / METHOD OF MANUFACTURING METAL OXIDE SEMICONDUCTOR AND COMPLEMENTARY METAL OXIDE SEMICONDUCTOR

二、申請人：(共 1 人)

姓名或名稱：(中文/英文)

聯華電子股份有限公司 / UNITED MICROELECTRONICS CORP.

代表人：(中文/英文)

胡國強 / HU, KWO-CHAIN

住居所或營業所地址：(中文/英文)

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Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

國 籍：(中文/英文)

中華民國 / TWN

三、發明人：(共 5 人)

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1. 藍邦強 / LAN, BANG-CHIANG

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200743160

3. 林育信 / LIN, YU-HSIN
4. 蔡宗龍 / TSAI, TSUNG-LUNG
5. 蔡成宗 / TSAI, CHENG-TZUNG

國 籍：(中文/英文)

1. 中華民國 / TWN
2. 中華民國 / TWN
3. 中華民國 / TWN
4. 中華民國 / TWN
5. 中華民國 / TWN

四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其

事實發生日期為： 年 月 日。

☐ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號 順序註記】

☐ 有主張專利法第二十七條第一項國際優先權：

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號 順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料 【格式請依：寄存機構、日期、號碼 順序註記】

國外生物材料 【格式請依：寄存國家、機構、日期、號碼 順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

一種製作金氧半導體電晶體的方法，包含提供一基底，且於基底上形成一閘極結構，又於閘極結構周圍形成一偏側壁子，於偏側壁子周圍形成一犧牲側壁子。再者，於閘極結構之兩側形成數個磊晶層，且磊晶層位於犧牲側壁子之外側，之後去除犧牲側壁子，並形成數個汲極/源極延伸區於偏側壁子外側的基底中以及磊晶層中。由於本發明之源極/汲極延伸區係於選擇性磊晶製程之後製作，所以選擇性磊晶製程之高溫，不會破壞源極/汲極延伸區。

六、英文發明摘要：

A method of manufacturing a metal oxide semiconductor is provided. It comprises forming an offset spacer, and a disposable spacer around the offset spacer. Then, forms a plurality of epitaxial layers outside the disposable spacer, and removes the disposable spacer. In addition, forms a plurality of source/drain extension areas in the substrate outside the offset spacer and the epitaxial layers. Because the source/drain extension areas are formed after the selective epitaxy growth process, the thermal of the selective epitaxy growth process doesn't damage the source/drain extension areas.

七、指定代表圖：

(一)本案指定代表圖為：第（ 8 ）圖。

(二)本代表圖之元件符號簡單說明：

500	半導體晶片
502	基底
506	閘極結構
508	閘極氧化層
510、516	摻雜多晶矽層
511	淺溝隔離
512、518	頂保護層
522	偏側壁子
602	磊晶層
702、704	汲極/源極延伸區
806、808	汲極/源極
503	摻雜井
514	閘極絕緣層
802	次偏側壁子
804	主要側壁子

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

九、發明說明：

【發明所屬之技術領域】

本發明係關於一種金氧半導體電晶體和互補式金氧半導體電晶體的製作方法，尤指一種先製作源極/汲極延伸區，再製作磊晶層的金氧半導體電晶體和互補式金氧半導體電晶體的製作方法。

【先前技術】

隨著半導體元件尺寸越來越小，電晶體製程步驟也有許多的改進，以期製造出小體積、高品質的電晶體。

先前技術的電晶體製程是在矽基底上形成閘極結構之後，再利用可降低熱預算(thermal budget)的離子植入法，以於閘極結構相對兩側的矽基底中形成源極延伸(source extension)區與汲極延伸(drain extension)區，或者稱為輕摻雜(lightly doped drain, LDD)源極/汲極。接著，於閘極結構側邊形成側壁子(spacer)，並利用此閘極結構及側壁子做為遮罩，進行離子植入步驟，以於矽基底中形成源極/汲極區。而為了要將電晶體的閘極、源極與汲極適當電性連接於電路中，因此需要形成接觸插塞(contact plug)來進行導通。且為了改善金屬材質之接觸插塞與半導體材質之閘極結構、源極/汲極區之間的歐米接觸(Ohmic contact)，通常會再利用自動對準金屬矽化物(self-aligned silicide, salicide)

製程，在閘極結構、源極/汲極區的表面形成一金屬矽化物。

然而，在進行自動對準金屬矽化物製程中，金屬層中的金屬會擴散進矽基底中並消耗掉源極/汲極區中的矽，不但原本源極/汲極區中的晶格結構會遭到破壞，甚至導致汲極/源極和基底之間的 PN 接合與金屬矽化物過近，而產生漏電。尤其在超淺介面 (ultra shallow junction, USJ) 的設計中，更可能會造成元件失效的狀況。

目前，較佳的解決方法是利用選擇性磊晶成長 (selective epitaxial growth, SEG) 製程，架高電晶體的汲極/源極，以避免金屬矽化物與矽基底直接接觸，同時維持源極/汲極延伸區。但是，選擇性磊晶製程的溫度，高達攝氏 690 度至 790 度，所以會破壞已形成的源極/汲極延伸區。因此如何研發出一種能製作源極/汲極延伸區又同時能製作磊晶層的方法，係為重要該領域重要課題。

【發明內容】

本發明係提供一種製作金氧半導體電晶體的方法，以解決上述問題。

本發明係提供一種製作金氧半導體電晶體的方法，包含提供一基底，且於基底上形成一閘極結構，又於閘極結

構周圍形成一偏側壁子，於偏側壁子周圍形成一犧牲側壁子。再者，於閘極結構之兩側形成數個磊晶層，且磊晶層位於犧牲側壁子之外側，之後去除犧牲側壁子，並形成數個汲極/源極延伸區於偏側壁子外側的基底中以及磊晶層中。

本發明係提供一種製作互補式金氧半導體電晶體的方法，包含提供一基底，並形成一第一閘極結構、一第二閘極結構於基底上，且於第一、第二閘極結構周圍形成第一、第二偏側壁子，再於第二偏側壁子周圍形成一犧牲側壁子。接著，於第二閘極結構之兩側形成數個磊晶層，這些磊晶層位於該犧牲側壁子之外側，然後，去除犧牲側壁子，於第一閘極結構之兩側之基底中形成數個第一汲極/源極延伸區，以及於第二閘極結構之第二偏側壁子外側之基底中形成數個第二汲極/源極延伸區。

本發明係提供一種製作互補式金氧半導體電晶體的方法，包含提供一基底，形成第一、第二閘極結構於基底上，於第一、第二閘極結構周圍形成第一、第二偏側壁子。接著，於第一、第二偏側壁子周圍形成一第一、第二犧牲側壁子，於第一、第二閘極結構之兩側形成數個磊晶層，這些磊晶層分別位於第一、第二犧牲側壁子之外側。然後，去除第一、第二犧牲側壁子，以及於第一、第二閘極結構

之兩側之基底中形成複數個第一、第二汲極/源極延伸區。

由於本發明之源極/汲極延伸區係於選擇性磊晶製程之後製作，所以選擇性磊晶製程之高溫，不會破壞源極/汲極延伸區，使得本發明所製作的電晶體具有超淺介面又具有磊晶層，金屬矽化物與基底不會直接接觸，同時又維持源極/汲極延伸區。

【實施方式】

請參考第 1 圖至第 4 圖，第 1 圖至第 4 圖係為本發明第一較佳實施例之製作方法示意圖。半導體晶片 100 具有一基底 102、一閘極結構 104 和一淺溝隔離(STI)111 包圍著閘極結構 104，且閘極結構 104 包含有一閘極絕緣層 106、一摻雜多晶矽層(doped poly-silicon)108 和一頂保護層(cap layer)110。

隨後利用一沈積(deposition)製程和一非等向性蝕刻(anisotropic etching)製程，於閘極結構 104 周圍形成一偏側壁子(offset spacer)112。接著，在於基底 102 和閘極結構 104 上方沈積一氮化矽層(未顯示)，然後，進行一非等性向性回蝕刻，以於偏側壁子 112 周圍再形成犧牲側壁子 114。

請參考第 2 圖，以閘極結構 104 之頂保護層 110 以及

犧牲側壁子 114 為蝕刻遮罩，進行一蝕刻製程，以於閘極結構 104 相對兩側之基底 102 中分別形成一凹槽(recess)202。接著，進行一選擇性磊晶(selective epitaxial growth, SEG)製程，於各凹槽 202 中形成一磊晶層 204，其中磊晶層 204 之材質可為矽、鍺化矽(SiGe)或者碳化矽(SiC)。然後，去除犧牲側壁子 114，接下來，進行一輕摻雜離子佈植製程和雷射回火(laser anneal)，於閘極結構 104 之偏側壁子 112 兩側的基底 102 和磊晶層 204 之表面，形成汲極/源極延伸區 304。

請參考第 4 圖，再沈積一氮化矽層（未顯示）覆蓋於閘極結構 104、偏側壁子 112、磊晶層 204 和基底 102 上，並進行一非等向性蝕刻，以於偏側壁子 112 周圍再形成一主要側壁子 302。接著，利用頂保護層 110 以及主要側壁子 302 作為離子佈植遮罩，進行一離子佈植和雷射回火，以於主要側壁子 302 外側之磊晶層 204 中形成汲極/源極 402。之後，進行自對準金屬矽化物(salicide)製程，以於閘極結構 104、汲極/源極 402 上方，分別形成金屬矽化物（未顯示）。而其中閘極結構 104 和汲極/源極 402 係構成金氧半導體電晶體。

在此第一較佳實施例中，除上述製作汲極/源極 402 的作法外，另外亦可於製作磊晶層 204 時，直接於選擇性磊

晶時加入摻質，使得形成的磊晶層 204 係為具有摻質的磊晶，可直接作為汲極/源極；又或者可於製作磊晶層 204 時，還是磊晶形成不具有摻質的磊晶層 204，但於磊晶層 204 完成後，犧牲側壁子 114 未去除前，進行離子佈植製程，使磊晶層 204 具有摻質，可作為汲極/源極使用。又上述實施例適用於 PMOS、NMOS，其相關製程為習知此項技藝者所熟知，在此不贅述。

請參考第 5 圖至第 8 圖，第 5 圖至第 8 圖係為本發明第二較佳實施例之製作方法示意圖。半導體晶片 500 具有一基底 502，基底 502 具有摻雜井 503，在此第二較佳實施例中摻雜井 503 係為 N 型井，基底 502 上方具有閘極結構 504、506，且另有淺溝隔離 511 包圍著閘極結構 504、506，其中閘極結構 506 位於摻雜井 503 上方。且閘極結構 504、506 皆包含有閘極絕緣層 508、514、摻雜多晶矽層 510、516 和頂保護層 512、518。

隨後利用一氮化矽沈積製程和一非等向性蝕刻製程，於閘極結構 504 周圍形成偏側壁子 520，接續著，再進行一沈積製程和一非等向性蝕刻製程，於閘極結構 506 周圍形成偏側壁子 522，且偏側壁子 522 由非氮化矽的介電材質所構成。接著，於基底 502 和閘極結構 504、506 上方沈積一層氮化矽層 526。後續在於氮化矽層 526 上方形成一

圖案化硬遮罩 528，例如一圖案化光阻層，且此圖案化硬遮罩 528 係位於閘極結構 504 和部分基底 502 的上方。接下來，對氮化矽層 526 進行一非等性向性蝕刻，並以圖案化硬遮罩 528 為蝕刻遮罩，以於閘極結構 506 之偏側壁子 522 周圍形成一犧牲側壁子 524。接著，利用圖案化硬遮罩 528、閘極結構 506 之頂保護層 518 以及犧牲側壁子 524 作為蝕刻遮罩，進行一蝕刻製程，以於閘極結構 506 相對兩側之基底 502 中各形成一凹槽 530，而凹槽 530 完成後，即可去除圖案化硬遮罩 528。

請參考第 6 圖，接著，進行一選擇性磊晶製程，於各凹槽 530 中分別形成磊晶層 602，其中磊晶層 602 之材質可為矽、鍺化矽(SiGe)或者碳化矽(SiC)。

請參考第 7 圖，進行一蝕刻製程，移除氮化矽層 526、偏側壁子 520、犧牲側壁子 524。接下來，利用一遮罩（未顯示），例如一圖案化光阻層，遮蓋住閘極結構 506 和部分基底 502，並進行一離子佈植製程和雷射回火，以於閘極結構 504 兩側的基底 502 中，形成汲極/源極延伸區 702。爾後，去除覆蓋在閘極結構 506 上的遮罩，並再形成另一個遮罩（未顯示），例如一圖案化光阻層，遮蓋住閘極結構 504 和部分基底 502，進行一離子佈植和雷射回火，以於閘極結構 506 兩側的摻雜井 503 中，以及磊晶層 602 的表面，

形成汲極/源極延伸區 704。在本第二較佳實施例中，汲極/源極延伸區 702 係為 N 型輕摻雜區域，而汲極/源極延伸區 704 係為 P 型輕摻雜區域。另外，除上述先形成汲極/源極延伸區 702，後形成汲極/源極延伸區 704 的製程外，亦可在其他變化型的製程中，先形成汲極/源極延伸區 704，後形成汲極/源極延伸區 702。

請參考第 8 圖，接續著，再沈積一氮化矽層（未顯示）於基底 502 上，並進行一非等向性蝕刻，以閘極結構 504 周圍形成次偏側壁子 802，且於閘極結構 506 之偏側壁子 112 周圍形成主要側壁子 804。接下來，利用一遮罩（未顯示），例如一圖案化光阻層，以遮蓋住閘極結構 506 和部分基底 502，並進行一離子佈植製程和雷射回火，以於閘極結構 504 之次偏側壁子 802 以外之兩側的基底 502 中，形成汲極/源極 806。爾後，去除覆蓋在閘極結構 506 上的遮罩，並再形成另一個遮罩（未顯示），例如一圖案化光阻層，遮蓋住閘極結構 504 和部分基底 502，再進行一離子佈植製程和雷射回火，以於閘極結構 506 之主要側壁子 804 之兩側的磊晶層 602 中，形成汲極/源極 808。另外，除上述先形成汲極/源極 806，後形成汲極/源極 808 的製程外，亦可在其他變化型的製程中，先形成汲極/源極 808，後形成汲極/源極 806。之後，再進行自對準金屬矽化物(salicide)製程，以於閘極結構 504、506、汲極/源極 806、808 上方，

形成金屬矽化物（未顯示）。而其中間極結構 504、506、汲極/源極 806、808 係構成互補式金氧半導體 (complementary metal oxide semiconductor, CMOS) 電晶體。

在此第二較佳實施例中，除上述製作汲極/源極 808 的作法外，亦可於製作磊晶層 602 時，直接於選擇性磊晶時加入摻質，則形成的磊晶層 602 為具有摻質的磊晶，並作為汲極/源極使用；又或者可於製作磊晶層 602 時，還是磊晶形成不具有摻質的磊晶層 602，但於磊晶層 602 完成後，且犧牲側壁子 524 未去除前，進行離子佈植製程，使磊晶層 602 具有摻質，利用其作為汲極/源極。又上述製程是以 PMOS 具有磊晶層的 CMOS 作為說明，而本發明亦適用於 NMOS 具有磊晶層的 CMOS。

請參考第 9 圖至第 12 圖，第 9 圖至第 12 圖係為本發明第三較佳實施例之製作方法示意圖。如第 9 圖所示，半導體晶片 900 具有一基底 902，基底 902 具有摻雜井 903，在此第三較佳實施例中摻雜井 903 係為 N 型井，基底 902 上方具有閘極結構 904、906，且另有淺溝隔離 911 包圍著閘極結構 904、906，其中閘極結構 906 位於該摻雜井 903 上方。且閘極結構 904、906 皆包含有閘極絕緣層 908、914、摻雜多晶矽層 910、916 和一頂保護層 912、918。

隨後利用一沈積製程和一非等向性蝕刻製程，於閘極結構 904、906 周圍形成分別偏側壁子 920、922。接著，於基底 902 和閘極結構 904、906 上方沈積一層氮化矽層（未顯示），並進行一非等向蝕刻製程，於閘極結構 904、906 周圍的偏側壁子 920、922 外側，分別再形成犧牲側壁子 924、926。值得注意的是，偏側壁子 920、922 和犧牲側壁子 924、926 係由不同蝕刻選擇比之材質所組成。

請參考第 10 圖，接著進行一蝕刻製程，以利用閘極結構 904、906 之頂保護層 912、918 及犧牲側壁子 924、926 作為蝕刻遮罩，使得犧牲側壁子 924 兩側之基底 902 中，形成凹槽 1002，且於犧牲側壁子 926 兩側之摻雜井 903 中，形成凹槽 1004。接著，進行一選擇性磊晶製程，於凹槽 1002、1004 中分別形成磊晶層 1006、1008，其中磊晶層 1006、1008 之材質可為矽、鍺化矽(SiGe)或者碳化矽(SiC)。

請參考第 11 圖，進行一蝕刻製程，移除犧牲側壁子 924、926。接下來，於閘極結構 906 和部分基底 902 上形成一圖案化光阻層（未顯示），並進行一離子佈植製程和雷射回火，於閘極結構 904 兩側之偏側壁子 920 外側的基底 902 中，以及磊晶層 1006 的表面，形成汲極/源極延伸區 1102。接著，去除上述之圖案化光阻層，並且形成另一個圖案化光阻層，遮蓋住閘極結構 904 和部分基底 902，並

進行一離子佈植製程和雷射回火，以於閘極結構 906 兩側之偏側壁子 922 外側的摻雜井 903 中，以及磊晶層 1008 的表面，形成汲極/源極延伸區 1104。在本第三較佳實施例中，汲極/源極延伸區 1102 係為 N 型輕摻雜區域，而汲極/源極延伸區 1104 係為 P 型輕摻雜區域。其中，形成汲極/源極延伸區 1102、1104 的順序亦可調換。

請參考第 12 圖，接續著，再沈積一氮化矽層（未顯示）於基底 902 上，並進行一非等向性蝕刻，以閘極結構 904、906 周圍形成主要側壁子 1202、1204。接下來，於閘極結構 906 和部分基底 902 上形成一圖案化光阻層（未顯示），並進行一離子佈植製程和雷射回火，以於閘極結構 904 之主要側壁子 1202 之兩側的磊晶層 1006 中，形成汲極/源極 1206。之後，去除上述之圖案化光阻層，並且於閘極結構 904 和部分基底 902 上形成另一個圖案化光阻層（未顯示），並進行一離子佈植製程和雷射回火，以於閘極結構 906 之主要側壁子 1204 之兩側的磊晶層 1008 中，形成汲極/源極 1208。最後，再進行自對準金屬矽化物(salicide)製程，以於閘極結構 904、906、汲極/源極 1206、1208 上方，形成金屬矽化物（未顯示）。而其中閘極結構 904、906、汲極/源極 1206、1208 係構成互補式金氧半導體電晶體。

在此第三較佳實施例中，除上述製作汲極/源極 1206、

1208 的作法外，亦可於製作磊晶層 1006、1008 時，直接於選擇性磊晶時加入摻質，則形成的磊晶層 1006、1008 為具有摻質的磊晶，可作為汲極/源極；又或者可於製作磊晶層 1006、1008 時，還是磊晶成不具有摻質的磊晶層 1006、1008，但於磊晶層 1006、1008 完成後，且犧牲側壁子 924、926 未去除前，進行離子佈植製程，使磊晶層 1006、1008 具有摻質，將磊晶層 1006、1008 作為汲極/源極使用。本發明並不侷限於上述製程中 PMOS 和 NMOS 於同一製程蝕刻凹槽、進行磊晶，亦可依照需求利用硬遮罩，分別製作 PMOS 和 NMOS 的凹槽和磊晶層。

又值得注意的是，在前述各較佳實施例中，基底之材質可為矽基底、矽覆絕緣基底、或者各種含有矽、鍺、鍺化矽、碳化矽等化合物的基底；閘極絕緣層可由氧化層、氧化氮、氮層、二氧化矽，或矽酸鈣(hafnium silicates)這類高介電常數(High-k)材料所構成。而閘極不只可由上述之多晶矽構成，也可由金屬等導電材質構成，甚至可為虛設(dummy)閘極。另外，犧牲側壁子、主要側壁子則可由 OO、ON、OON、ONO、ONONO 等材質構成，而金屬矽化物的金屬部分可由鈦(Ti)、鈷(Co)、鎳(Ni)等金屬所構成。

由於本發明之源極/汲極延伸區係於選擇性磊晶製程之後製作，所以選擇性磊晶製程之高溫，不會破壞源極/汲

極延伸區，使得本發明所製作的電晶體具有超淺介面又具有磊晶層，金屬矽化物與基底不會直接接觸，同時又維持源極/汲極延伸區。

以上所述僅為本發明之較佳實施例，凡依本發明申請專利範圍所做之均等變化與修飾，皆應屬本發明之涵蓋範圍。

【圖式簡單說明】

第1圖至第4圖係為本發明第一較佳實施例之製作方法示意圖。

第5圖至第8圖係為本發明第二較佳實施例之製作方法示意圖。

第9圖至第12圖係為本發明第三較佳實施例之製作方法示意圖。

【主要元件符號說明】

100、500、900	半導體晶片
102、502、902	基底
104、504、506、904、906	閘極結構
106、508、514、908、914	閘極氧化層
108、510、516、910、916	摻雜多晶矽層
110、512、518、912、918	頂保護層
111、511、911	淺溝隔離
112、520、522、920、922	偏側壁子
114、524、924、926	犧牲側壁子
202、530、1002、1004	凹槽

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204、602、1006、1008	磊晶層
304、702、704、1102、1104	汲極/源極延伸區
402、806、808、1206、1208	汲極/源極
503、903	摻雜井
526	氮化矽層
528	圖案化硬遮罩
802	次偏側壁子
● 302、804、1202、1204	主要側壁子

十、申請專利範圍：

1. 一種製作金氧半導體電晶體的方法，包含：
 - 提供一基底；
 - 形成一閘極結構於該基底上；
 - 於該閘極結構周圍形成一偏側壁子；
 - 於該偏側壁子周圍形成一犧牲側壁子；
 - 於該閘極結構之兩側形成二磊晶層，且該等磊晶層位於該犧牲側壁子之外側；
 - 去除該犧牲側壁子；以及
 - 形成複數個汲極/源極延伸區於該偏側壁子外側的該基底中，以及該等磊晶層中。
2. 如請求項第 1 項所述之方法，其中形成該等磊晶層的步驟，包含：
 - 以該閘極結構及該犧牲側壁子作為遮罩，進行一蝕刻製程，以於該閘極結構兩側之該基底中形成二凹槽；以及
 - 進行一選擇性磊晶製程，以形成該等磊晶層於該等凹槽中。
3. 如請求項第 2 項所述之方法，其中該等磊晶層完成後，進行一離子佈植製程，植入摻質於該等磊晶層中。
4. 如請求項第 2 項所述之方法，其中該選擇性磊晶製程之

磊晶材料包含有摻質。

5. 如請求項第 1 項所述之方法，其中該等汲極/源極延伸區完成後，又包含以下步驟：

形成一主要側壁子於該偏側壁子外側和部分該等磊晶層上方；以及

以該主要側壁子作為遮罩，進行一離子佈植製程，於未被該主要側壁子覆蓋之該等磊晶層中形成複數個汲極/源極。

6. 一種製作互補式金氧半導體電晶體的方法，包含：

提供一基底；

形成一第一閘極結構、一第二閘極結構於該基底上；

於該第一閘極結構周圍形成一第一偏側壁子；

於該第二閘極結構周圍形成一第二偏側壁子；

於該第二偏側壁子周圍形成一犧牲側壁子；

於該第二閘極結構之兩側形成二磊晶層，且該等磊晶層位於該犧牲側壁子之外側；

去除該第一偏側壁子和該犧牲側壁子；

於該第一閘極結構之兩側之該基底中形成二第一汲極/源極延伸區；以及

於該第二閘極結構之該第二偏側壁子外側之該基底中形成二第二汲極/源極延伸區。

7. 如請求項第 6 項所述之方法，其中該第二偏側壁子和該犧牲側壁子係由不同蝕刻選擇比之材質所組成。

8. 如請求項第 6 項所述之方法，其中形成該等磊晶層的步驟，包含：

於該第一閘極結構和部分該基底上方，形成一圖案化硬遮罩；

進行一蝕刻製程，以該圖案化硬遮罩、該第二閘極結構及該犧牲側壁子作為蝕刻遮罩，以於該第二閘極結構兩側形成二凹槽；

去除該圖案化硬遮罩；以及

進行一選擇性磊晶製程，以形成該等磊晶層於該等凹槽中。

9. 如請求項第 6 項所述之方法，其中該等磊晶層完成後，另包含進行一離子佈植製程，植入摻質於該等磊晶層中。

10. 如請求項第 6 項所述之方法，其中該選擇性磊晶製程之磊晶材料包含有摻質。

11. 如請求項第 6 項所述之方法，其中該等第一、第二汲極/源極延伸區完成後，又包含以下步驟：

於該第二偏側壁子外側和部分該等磊晶層上方形成一

主要側壁子，以及於該第一閘極結構周圍形成一次偏側壁子；

於該第二閘極結構和部分該基底上方形成一第一光阻層；

進行一第一離子佈植製程，以於該第一閘極結構之兩側之該基底中，形成二第一汲極/源極；

去除該第一光阻層；

於該第一閘極結構和部分該基底上方形成一第二光阻層；以及

進行一第二離子佈植製程，於未被該主要側壁子覆蓋之該等磊晶層中形成二第二汲極/源極。

12.一種製作互補式金氧半導體電晶體的方法，包含：

提供一基底；

形成一第一閘極結構、一第二閘極結構於該基底上；

於該第一閘極結構周圍形成一第一偏側壁子，於該第二閘極結構周圍形成一第二偏側壁子；

於該第一偏側壁子周圍形成一第一犧牲側壁子，並於該第二偏側壁子周圍該形成一第二犧牲側壁子；

於該第一、第二閘極結構之兩側形成複數個磊晶層，該等磊晶層分別位於該第一、第二犧牲側壁子之外側；

去除該第一、第二犧牲側壁子；以及

於該第一、第二閘極結構之兩側之該基底中形成複數

個第一、第二汲極/源極延伸區。

13.如請求項第 12 項所述之方法，其中形成該等磊晶層的步驟，包含：

形成一圖案化硬遮罩於該基底上；

進行一蝕刻製程，以該圖案化硬遮罩作為蝕刻遮罩，以於該第一、第二閘極結構兩側形成複數個凹槽；

去除該圖案化硬遮罩；以及

進行一選擇性磊晶製程，以形成該等磊晶層於該等凹槽中。

14.如請求項第 12 項所述之方法，其中該等磊晶層完成後，包含以下步驟：

形成一第一圖案化光阻層於該第二閘極結構和部分該基底上；

進行一第一離子佈植製程，植入摻質於該第一閘極結構兩側之該等磊晶層中；以及

去除該第一圖案化光阻層。

15.如請求項第 12 項所述之方法，其中該等磊晶層完成後，包含以下步驟：

形成一第二圖案化光阻層於該第一閘極結構和部分該基底上；以及

進行一第二離子佈植製程，植入摻質於該第二閘極結構兩側之該等磊晶層中。

16.如請求項第 12 項所述之方法，其中該選擇性磊晶製程之磊晶材料包含有摻質。

17.如請求項第 12 項所述之方法，其中該等第一、第二汲極/源極延伸區完成後，又包含以下步驟：

於該第一、第二偏側壁子外側和部分該等磊晶層上方形成一主要側壁子；

於該第二閘極結構和部分該基底上方形成一第一光阻層；

進行一第一離子佈植製程，以於未被該主要側壁子覆蓋之該等磊晶層中形成複數個第一汲極/源極；

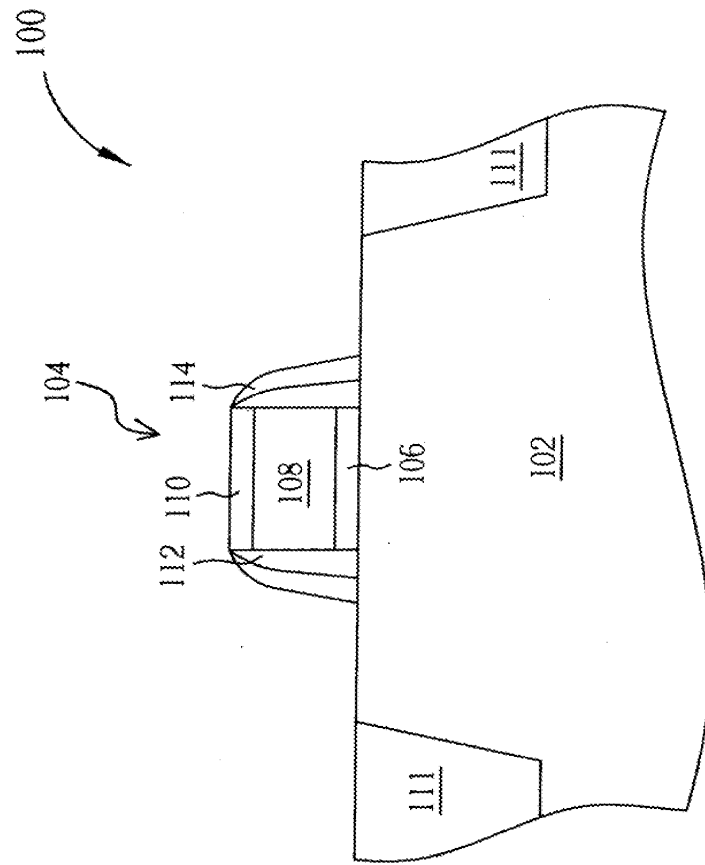
去除該第一光阻層；

於該第一閘極結構和部分該基底上方形成一第二光阻層；以及

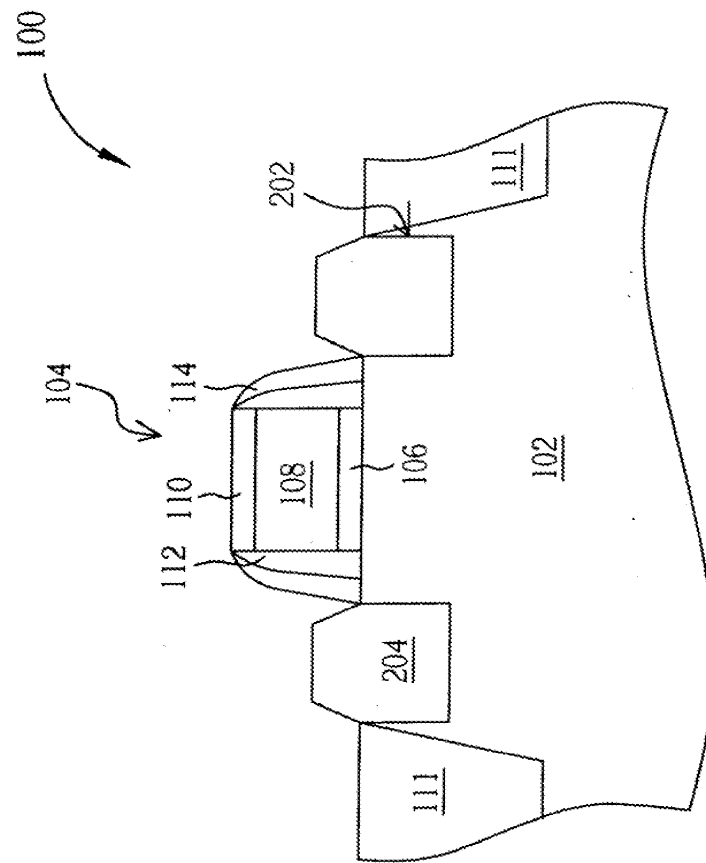
進行一第二離子佈植製程，於未被該主要側壁子覆蓋之該等磊晶層中形成複數個第二汲極/源極。

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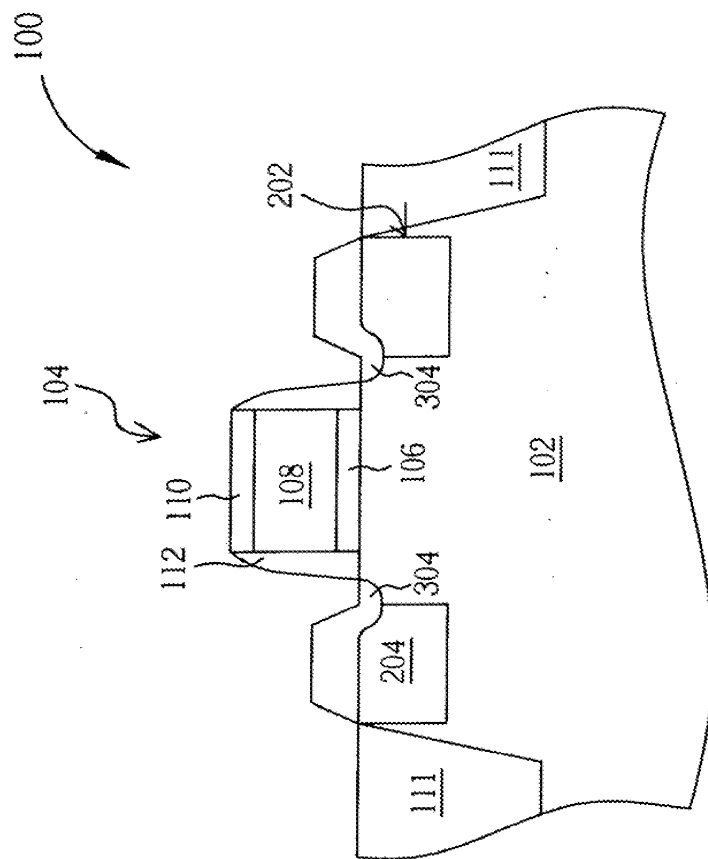
十一、圖式：



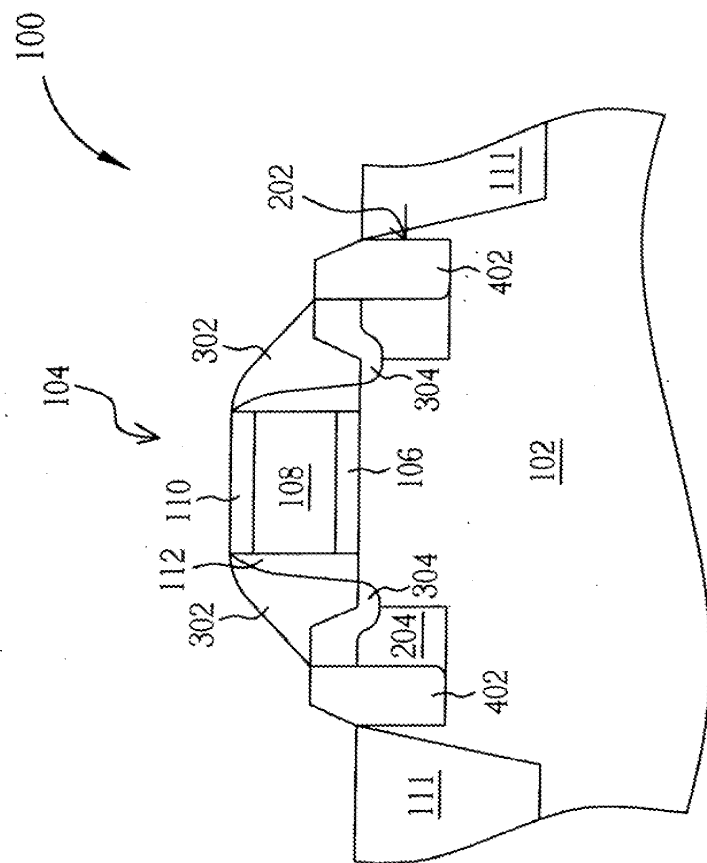
第1圖



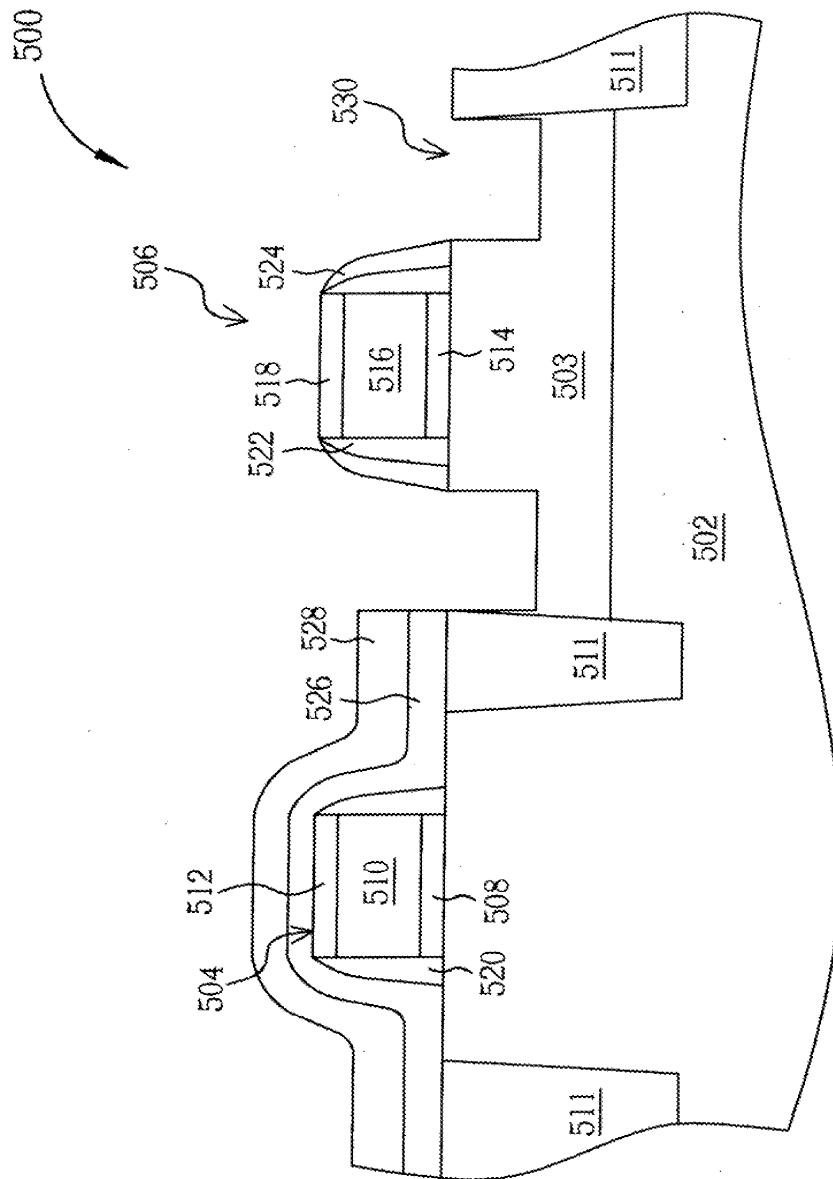
第2圖



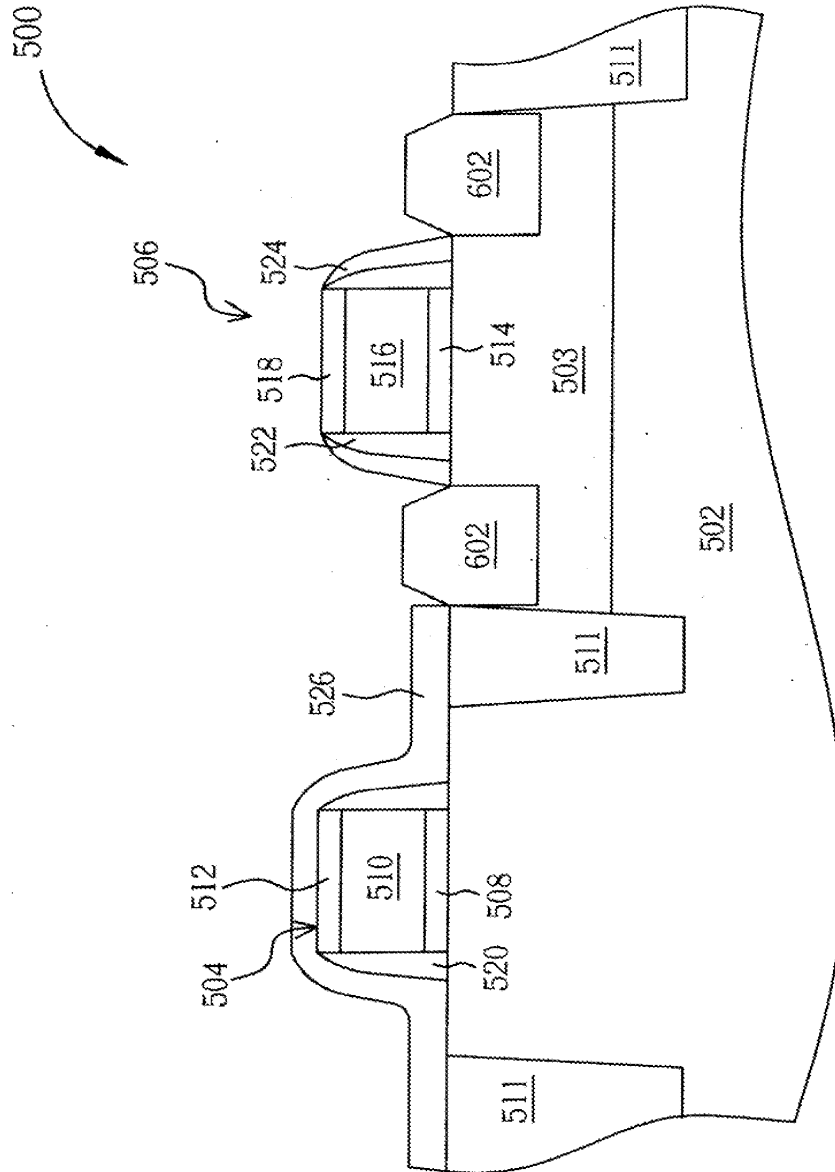
第3圖



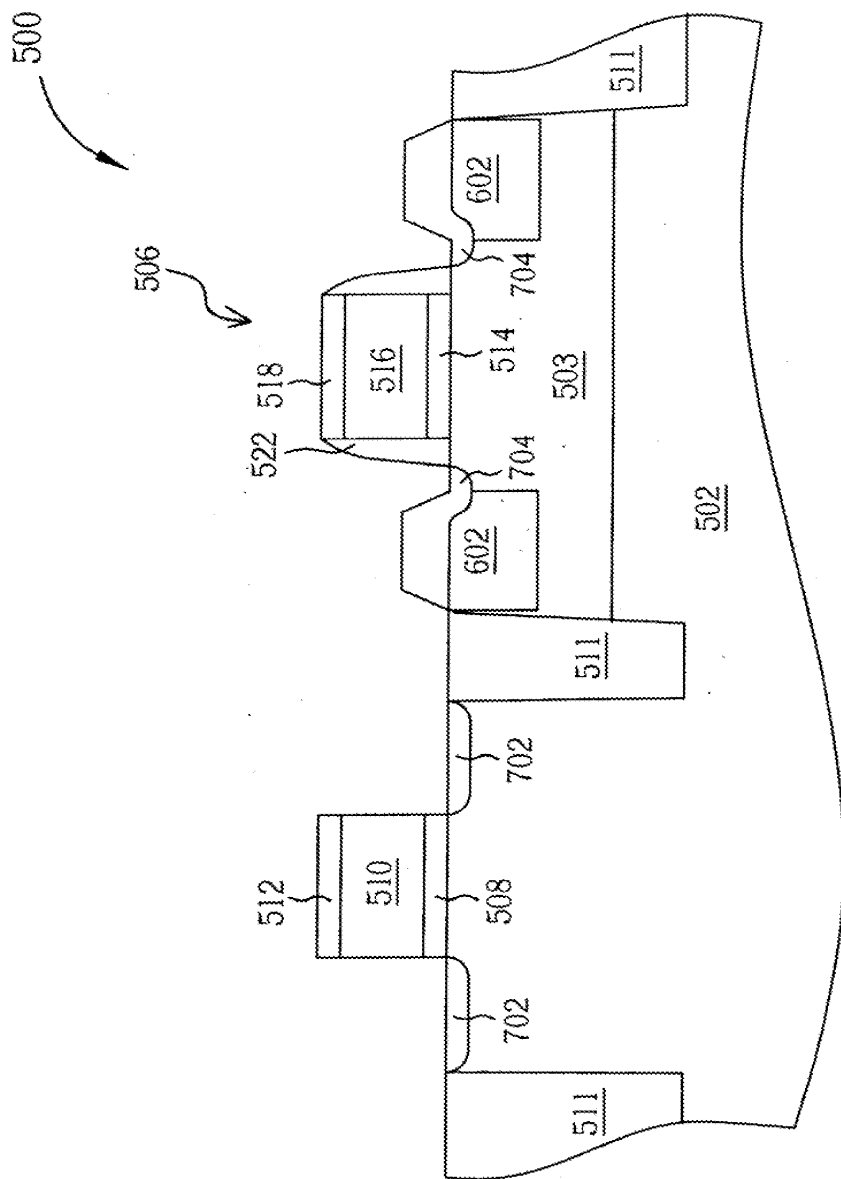
第4圖



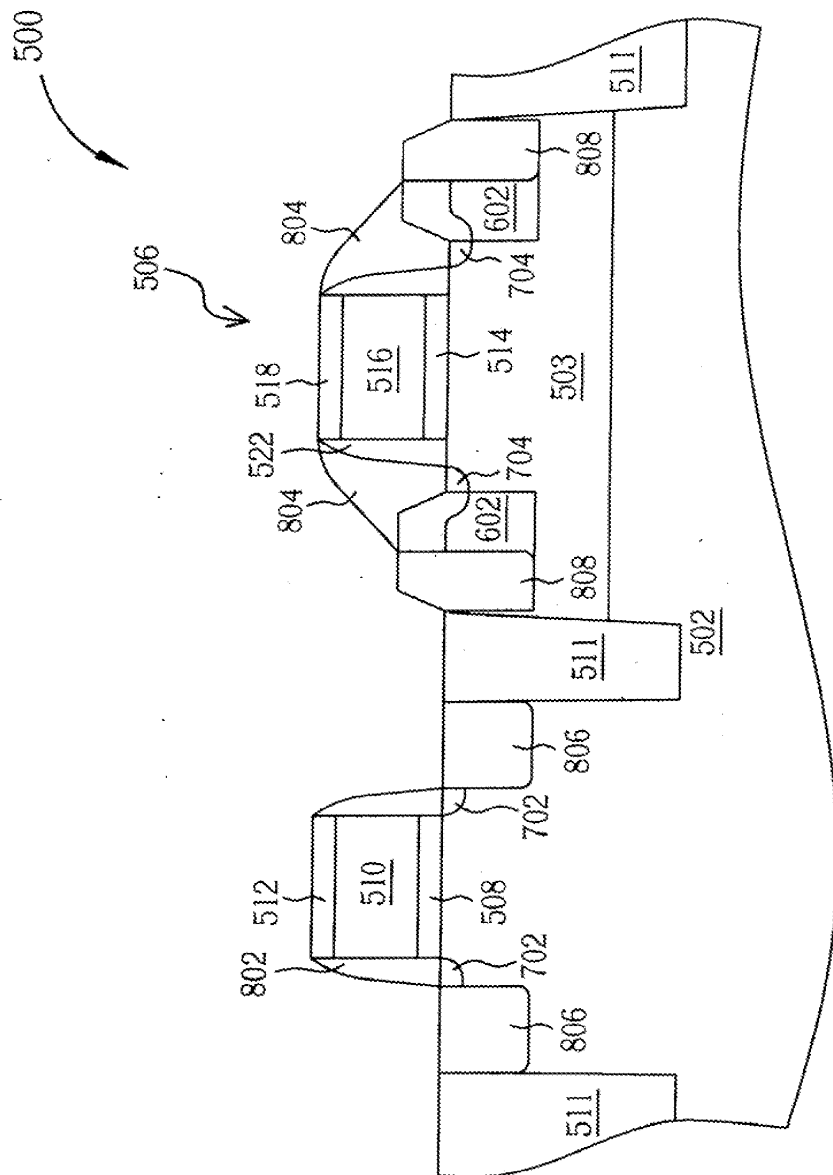
第5圖



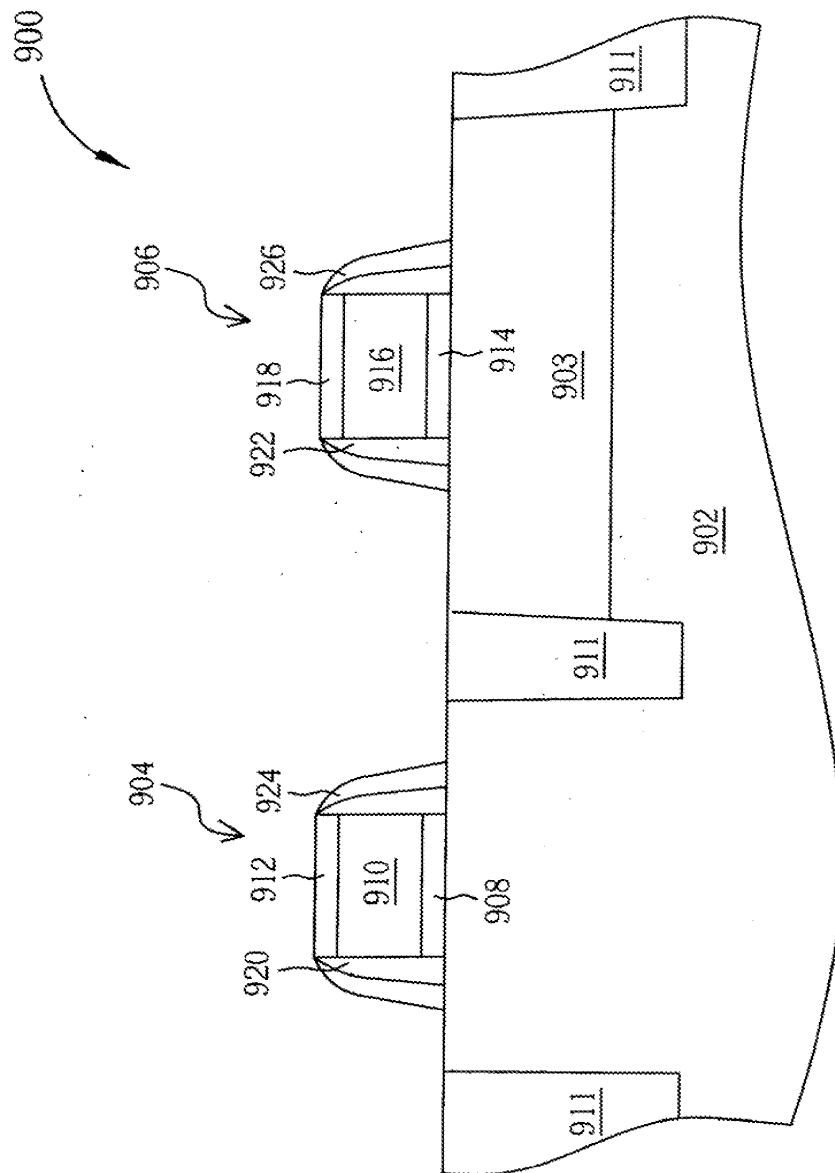
第6圖



第7圖



第8圖



第9圖

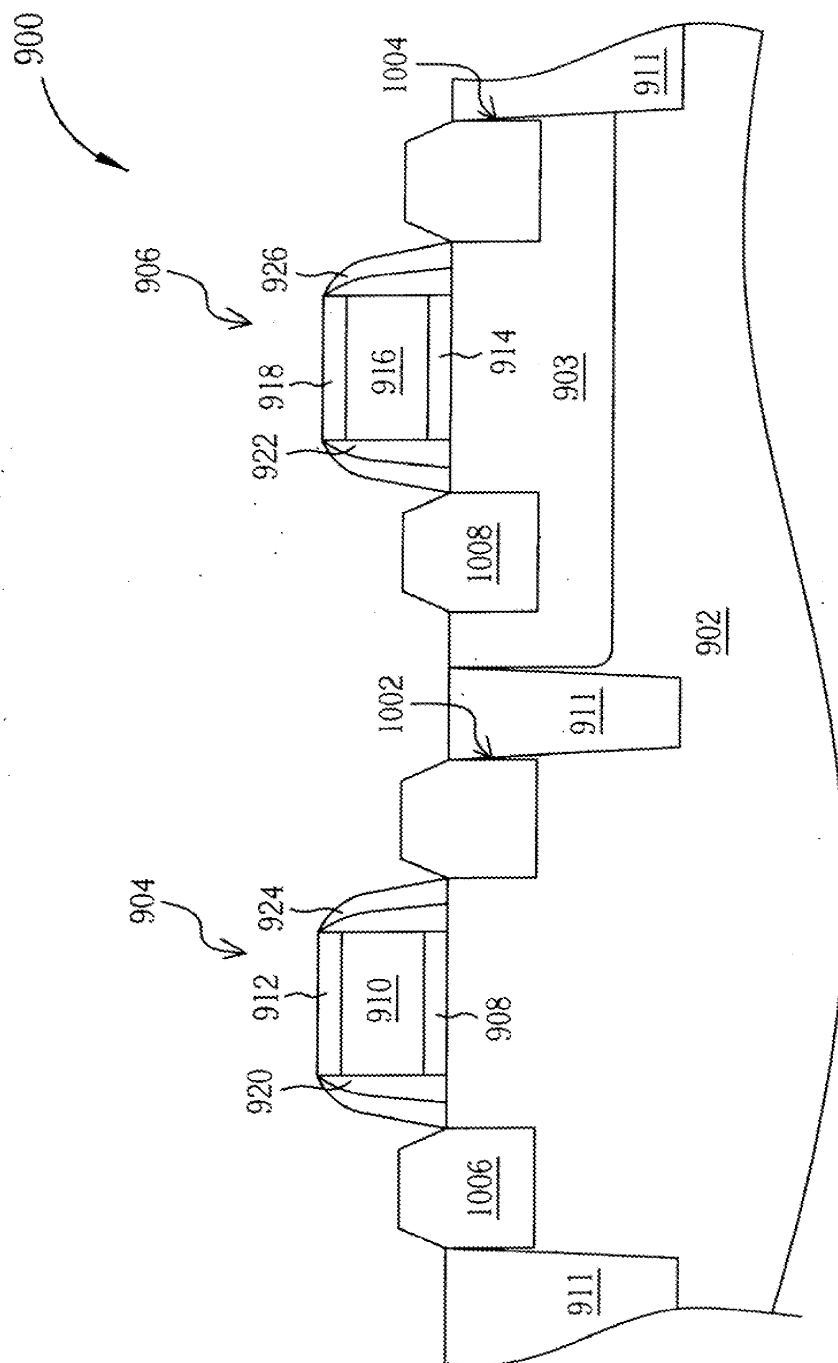
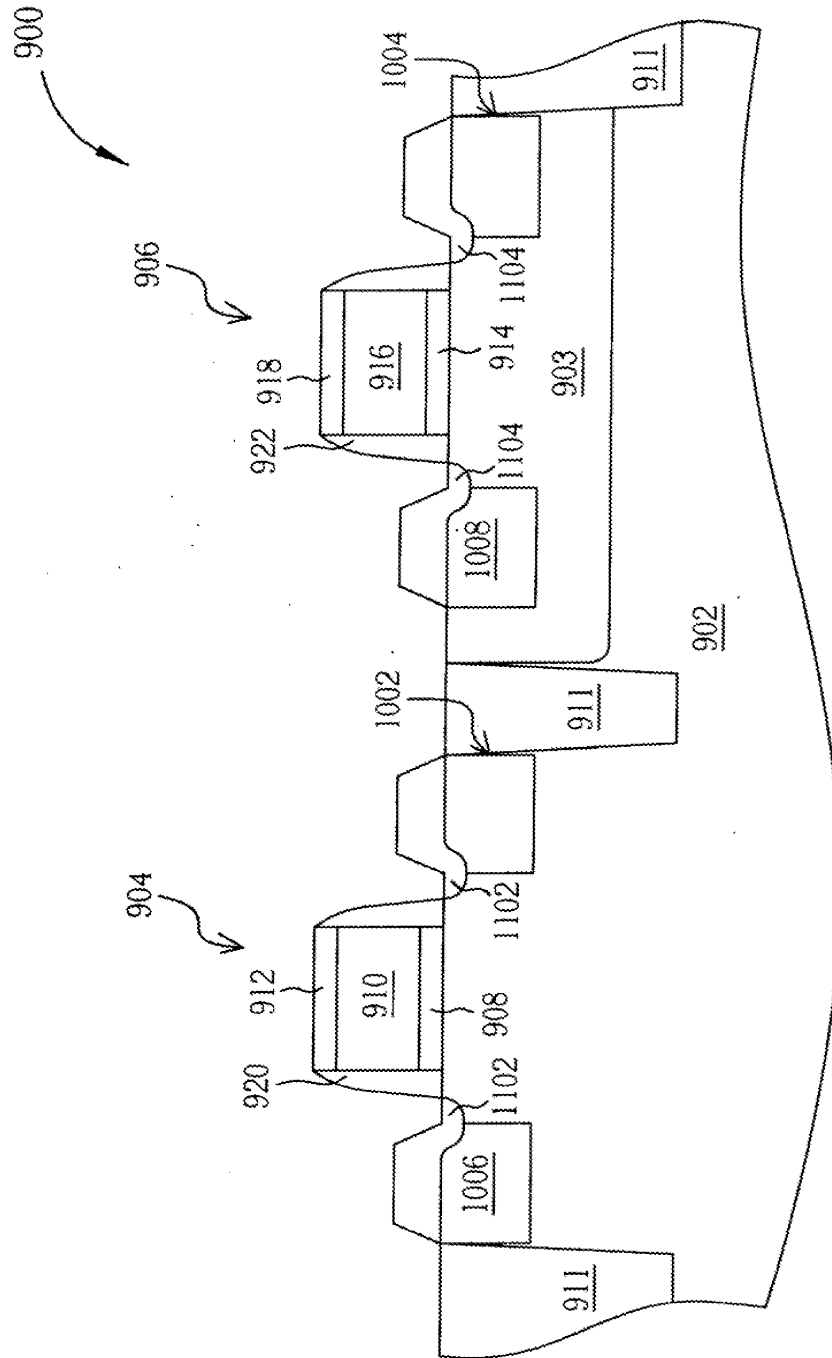
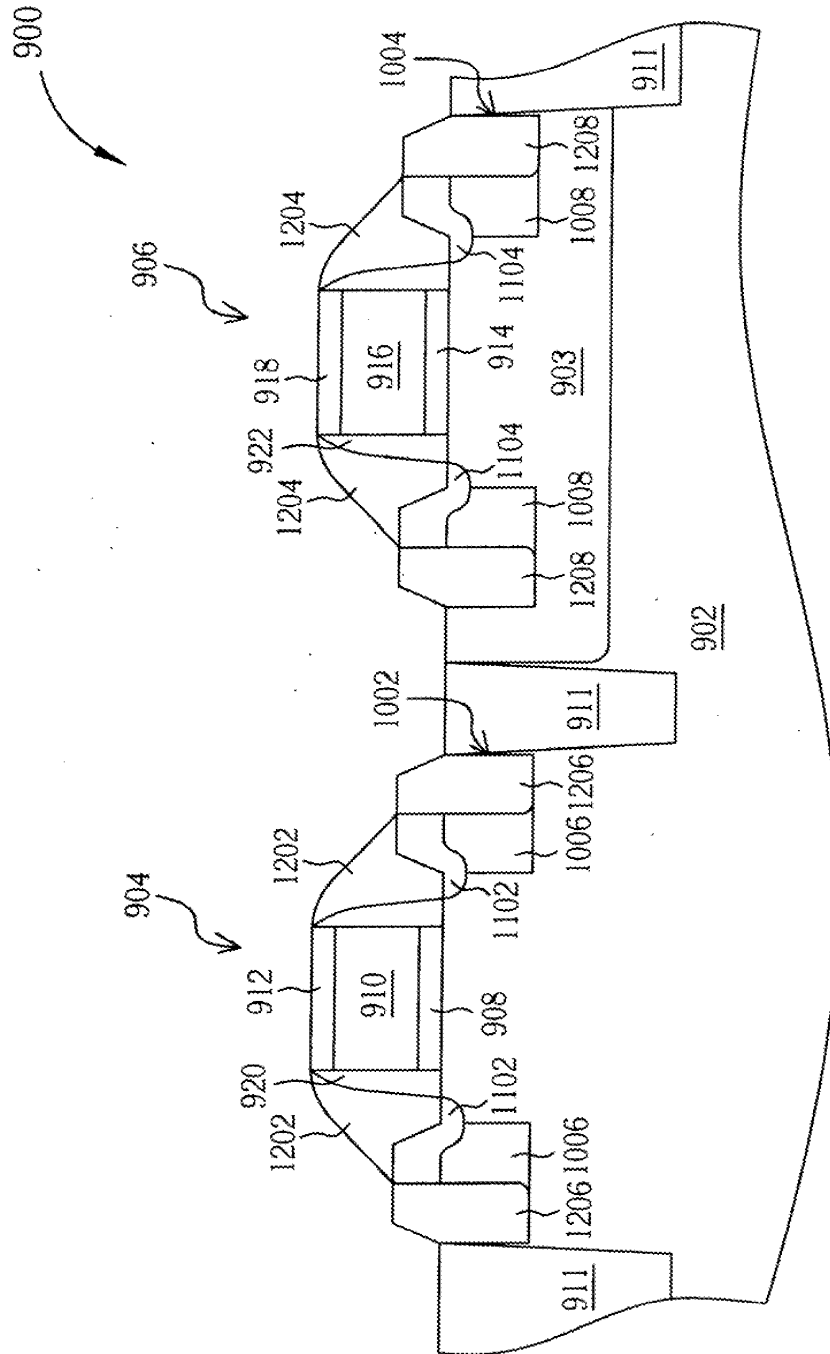


圖
第10



第11圖



第12圖

Abstract of TW 200908325

A semiconductor device includes a gate electrode disposed on a semiconductor substrate and source/drain regions disposed at both sides of the gate electrode, the source/drain regions being formed by implanting impurities. The source/drain regions include an epitaxial layer formed by epitaxially growing a semiconductor material having a different lattice constant from that of the semiconductor substrate in a recessed position at a side of the gate electrode, and a diffusion layer disposed in a surface layer of the semiconductor substrate.

發明專利說明書

(本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫)

※ 申請案號： 97 120490

※ 申請日期： 97.6.2 ※IPC分類：H01L29/78；H01L21/28(2006.01)

一、發明名稱：(中文/英文)

半導體裝置及製造半導體裝置之方法
SEMICONDUCTOR DEVICE AND METHOD FOR
MANUFACTURING SEMICONDUCTOR DEVICE

二、申請人：(共 1 人)

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代表人：(中文/英文)

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日本 JAPAN

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姓 名：(中文/英文)

松本 拓治
MATSUMOTO, TAKUJI

國 籍：(中文/英文)

日本 JAPAN

四、聲明事項：

☐ 主張專利法第二十二條第二項 ☐ 第一款或 ☐ 第二款規定之事實，其事實發生日期為： 年 月 日。

☒ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號 順序註記】

☒ 有主張專利法第二十七條第一項國際優先權：

1. 日本；2007年06月27日；特願2007-169023

2.

☐ 無主張專利法第二十七條第一項國際優先權：

1.

2.

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號 順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料 【格式請依：寄存機構、日期、號碼 順序註記】

國外生物材料 【格式請依：寄存國家、機構、日期、號碼 順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

本發明揭示一種半導體裝置，其包括：一閘極電極，其佈置於一半導體基板上；以及源極/汲極區域，其佈置於該閘極電極之兩側，該等源極/汲極區域係由植入雜質形成。該等源極/汲極區域包括一磊晶層，其藉由於該閘極電極之一側之一凹陷位置中磊晶成長具有與半導體基板不同之晶格常數的一半導體材料而形成，以及一擴散層，其佈置於該半導體基板之一表面層中。

六、英文發明摘要：

A semiconductor device includes a gate electrode disposed on a semiconductor substrate and source/drain regions disposed at both sides of the gate electrode, the source/drain regions being formed by implanting impurities. The source/drain regions include an epitaxial layer formed by epitaxially growing a semiconductor material having a different lattice constant from that of the semiconductor substrate in a recessed position at a side of the gate electrode, and a diffusion layer disposed in a surface layer of the semiconductor substrate.

七、指定代表圖：

(一)本案指定代表圖為：第 (1) 圖。

(二)本代表圖之元件符號簡單說明：

1a	半導體裝置
3	半導體基板
5	隔離膜
7	隔離作用區域
9	閘極電極
11	磊晶層
13	擴散層
15	源極/汲極區域
23	井擴散層
43	應力膜
ch	通道區域
Tr	電晶體

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

(無)

九、發明說明：

【發明所屬之技術領域】

本發明關於半導體裝置及製造半導體裝置之方法。更明確地說，本發明關於一種其中具有不同晶格常數之半導體材料係磊晶成長於閘極電極之側之凹陷部分中的半導體裝置及一種製造其之方法。

本發明包含與2007年06月27日向日本專利局申請的日本專利申請案JP 2007-169023有關之主旨，該申請案之全部內容係以引用的方式併入本文。

【先前技術】

在具有MOS電晶體之半導體裝置中，已積極使用藉由對半導體基板之通道區域施加應力來提升載子遷移率的技術。如此類技術中之一者，已提出使用圖11中顯示之結構。在此結構中，半導體基板101之表面係由隔離膜102隔離，且閘極電極104係佈置成橫跨隔離作用區域103而延伸，並於閘極電極104之兩側提供凹陷部分。由具有與半導體基板101不同之晶格常數之半導體材料構成的磊晶層105係佈置於凹陷部分中，並作為源極/汲極區域。

在此一情況中，例如，於p型MOS (PMOS)電晶體中，具有比構成半導體基板101之矽(Si)大之晶格常數之矽鍺(SiGe)係成長成磊晶層105。從而，對通道區域ch施加壓縮應力，並提升載子遷移率。例如，參考日本未審查專利申請公開案第2006-165012號(專利文件1)。

同時，於n型MOS (NMOS)電晶體中，具有比構成半導

體基板101之矽(Si)小之晶格常數之矽碳(SiC)係成長成磊晶層105。從而，對通道區域ch施加拉伸應力，並提升載子遷移率。例如，參考Kah Wee Ang等人，"Enhanced Performance in 50 nm N-MOSFETs with Silicon-Carbon Source/Drain Regions"，2004年12月，IEDM Tech. Dig.，1069至1071(非專利文件1)。

【發明內容】

在具有上述結構之半導體裝置中，為確保電晶體之特性係彼此相同，抑制對通道區域施加之應力的變動十分重要。對通道區域施加之應力係由磊晶層之深度(即，形成於半導體基板中之凹陷之深度)來控制。

然而，因為在使半導體基板凹陷之蝕刻程序期間發生微負載效應致使凹陷面積減小，故半導體基板中之凹陷之深度隨之減小。因此，磊晶層之深度根據(在作用區域中)半導體基板上之閘極電極之布局而改變。

此外，相對於由矽鍺(SiGe)構成之磊晶層，隨著布局面積增大，結晶缺陷之數目增大，而導致接面洩漏增大。

此外，於MOS電晶體中，布局面積可藉由運用一種結構而減小，該結構中相反電導係數類型之擴散層係佈置成與源極與汲極區域中之一毗鄰，且源極與汲極區域中之一者與相反電導係數類型之擴散層係因佈置作為表面層之矽化物層而短路。在此一結構中，在其中PMOS電晶體之源極/汲極區域使用由矽鍺(SiGe)構成之磊晶層的情況中，提供藉由於半導體基板之表面層中擴散n型雜質(如砷(As)或磷(P))所形成之n型擴散層以作為相反電導係數類型之擴散

層。

然而，n型雜質之擴散率在SiGe中係高於在由矽構成之半導體基板中(即，在砷(As)之情況中高出大約七倍，且在磷(P)之情況中高出大約兩倍)。因此，相反電導係數類型之擴散層(n型擴散層)中之n型雜質係擴散至毗鄰源極/汲極區域(由SiGe構成之磊晶層)中並輕易地到達通道區域，因而增大MOS電晶體之臨限值。

期望提供一種包括磊晶層之半導體裝置，該等磊晶層之深度係在不受布局影響下受控制，且其中避免發生結晶缺陷，因而致能特性之提升，以及提供一種製造該半導體裝置的方法。

根據本發明之一具體實施例，一種半導體裝置包括：一閘極電極，其佈置於一半導體基板上；以及源極/汲極區域，其佈置於該閘極電極之兩側，該等源極/汲極區域係由植入雜質形成。該等源極/汲極區域包括一磊晶層，其藉由於該閘極電極之一側之一凹陷位置中磊晶成長具有與半導體基板不同的晶格常數之半導體材料，以及一擴散層，其佈置於該半導體基板之一表面層中。

根據本發明之另一具體實施例，一種製造一半導體裝置之方法包括：一第一步驟，其於一半導體基板上形成一閘極電極；一第二步驟，其藉由透過一遮罩圖案之蝕刻於該閘極電極之一側使該半導體基板之一表面層凹陷；一第三步驟，其於凹陷部分上形成由具有與該半導體基板不同之晶格常數的半導體材料構成之磊晶層；以及一第四步驟，

其藉由移除該遮罩圖案以曝露該半導體基板之表面層並使雜質擴散至該磊晶層及該半導體基板之表面層中來形成源極/汲極區域，該等源極/汲極區域包括其中雜質經擴散之磊晶層與藉由使雜質擴散至該表面層中而形成之一擴散層。

在根據本發明之具體實施例之半導體裝置與製造半導體裝置之方法中，源極/汲極區域包括磊晶層與擴散層。因此，磊晶層之寬度係藉由改變擴散層之寬度來調整。因此，在不受布局影響下，控制其中將形成磊晶層之半導體基板之凹陷部分的寬度，並控制藉由蝕刻而凹陷之凹陷部分的深度。因此，例如，藉由改變擴散層之寬度將磊晶層之寬度設定成一預定值，在不受布局之影響下，等化其中佈置磊晶層之半導體基板之凹陷部分的深度。此外，由於磊晶層之形成面積(布局面積)係在不受布局之影響下，因對應之擴散層之部分而減小，故而可能獲得具有小數目結晶缺陷之磊晶層。

如上所述，根據本發明之具體實施例，可在不受布局影響下控制其中佈置磊晶層之半導體基板之凹陷部分的深度。因此，可能藉由具有控制深度之磊晶層來抑制對閘極電極下之通道區域所施加之應力的變動。此外，由於可在不受布局影響下獲得具有小數目之結晶缺陷的磊晶層，故而可降低接面洩漏。因此，能夠提升半導體裝置的特性。

【實施方式】

將參考圖式詳細地說明本發明之具體實施例。於此，將

說明在基板上佈置有複數個MOS電晶體之半導體裝置的結構。

第一具體實施例

圖1係顯示根據第一具體實施例之半導體裝置之結構的示意性剖面圖。在圖1中顯示之半導體裝置1a中，由矽(Si)構成之半導體基板3之表面係由隔離膜5隔離，且閘極電極9係佈置成橫跨隔離作用區域7而延伸。於閘極電極9之兩側，使半導體基板3之表面凹陷。由具有與半導體基板3不同之晶格常數之半導體材料構成之磊晶層11係佈置於凹陷部分中，且雜質係擴散至磊晶層11中。此外，相對於閘極電極9，擴散層13係佈置於磊晶層11之外側，擴散層13係藉由使雜質擴散至半導體基板3之表面層而形成。

在第一具體實施例中，於閘極電極9之兩側，其中雜質經擴散之磊晶層11與擴散層13構成源極/汲極區域15。

形成提供於每一閘極電極9之兩側中之每側的磊晶層11，使得具有藉由對應之擴散層13所控制的預定寬度W。例如，採用相同標準之MOS電晶體以在通道長度方向上具有實質相同的預定寬度W。因此，僅於磊晶層11之外側部分提供擴散層13，使得磊晶層11具有相同寬度。此外，在磊晶層11之通道長度方向上之預定寬度W係大約10至100 nm。

在半導體裝置1a上提供之MOS電晶體間之p型MOS (PMOS)電晶體中，磊晶層11使用具有比構成半導體基板3之矽(Si)大之晶格常數的矽鍺(SiGe)。從而，對通道區域

ch施加壓縮應力。

同時，在半導體裝置1a上提供之MOS電晶體間之n型MOS (NMOS)電晶體中，磊晶層11使用具有比構成半導體基板3之矽(Si)小之晶格常數的矽碳(SiC)。從而，對通道區域ch施加拉伸應力。

接著，將參考圖2A至5D說明半導體裝置1a之細部結構。

首先，如圖2A中顯示，製備由單晶矽構成之半導體基板3。半導體基板3具有(例如)約 $10\text{ m}\Omega\cdot\text{cm}$ 之電阻係數。作為半導體基板3，可使用絕緣物上矽(SOI)或包括一矽鍍層之基板，只要基板之表面層係由單晶矽構成。

接著，藉由於半導體基板3之表面層上之熱氧化形成具有約 15 nm 之厚度的襯墊氧化物膜21。然後，藉由低壓CVD (LP-CVD)沈積具有約 160 nm 之厚度的氮化矽膜22。除其中於襯墊氧化物膜21上佈置氮化矽膜22之結構外，亦可使用其中於多晶矽膜上佈置氮化矽膜之結構，或其中於襯墊氧化物膜上佈置氮化矽膜之結構。

接著，如圖2B中顯示，於氮化矽膜22與襯墊氧化物膜21中形成對應隔離膜形成部分之開口22a。於此，藉由微影術形成一光阻圖案(未顯示)，並使用該光阻圖案作為遮罩，蝕刻氮化矽膜22與襯墊氧化物膜21。為執行蝕刻程序，使用反應性離子蝕刻(RIE)系統、電子迴旋共振(ECR)系統或其類似物。在蝕刻程序之後，使用灰化系統或其類似物移除該光阻圖案。

接著，如圖2C中顯示，使用具有開口22a之氮化矽膜22作為遮罩來蝕刻半導體基板3，且從而，在半導體基板3中形成用於形成隔離膜之溝渠3a。溝渠3a之深度係大約0.3 μm 。為執行蝕刻程序，使用反應性離子蝕刻(RIE)系統、電子迴旋共振(ECR)系統或其類似物。

在此狀態中，藉由執行熱氧化程序，一襯層氧化物膜(未顯示)係形成有約4至10 nm之厚度。熱氧化程序係於大約800°C至900°C下實施。襯層氧化物膜可為一含氮氧化物膜。可藉由CVD沈積一氮化物膜來替代該襯層氧化物膜。

接著，如圖2D中顯示，藉由以絕緣膜填充溝渠3a而形成隔離膜5，且半導體基板3之表面係分隔成複數個作用區域7。藉由沈積一絕緣膜(如高密度電漿(HDP)氧化物膜)、一無機膜(如旋塗式玻璃(SOG)膜)、一有機氧化物膜或其類似物來形成隔離膜5以便能填充溝渠3a，且隨後藉由化學機械拋光(CMP)拋光絕緣膜直到曝露氮化矽膜22為止。

接著，如圖2E中顯示，為調整相對於半導體基板3之表面隔離膜5之高度，填充於溝渠3a中之絕緣膜(例如，氧化物膜)係經受濕式蝕刻。蝕刻厚度係(例如)大約40至100 nm。接著，以熱磷酸移除氮化矽膜22以曝露襯墊氧化物膜21。

接著，如圖3A中顯示，在半導體基板3之表面層中形成井擴散層23，並執行通道植入。於此，使用光阻圖案作為遮罩，對其中形成p型MOS電晶體之區域(其後稱為"PMOS區域")及其中形成n型MOS電晶體之區域(其後稱為"NMOS

區域")中之每一者個別執行離子植入。

在PMOS區域中，形成n型井擴散層23。在此一情況中，以200 KeV之植入能量植入約 $1E13$ 原子/ cm^2 之劑量的磷(P)離子。此外，在通道植入中，以100 keV之植入能量植入約 $1E11$ 至 $2E13$ 原子/ cm^2 之劑量的砷(As)離子。

同時，在NMOS區域中，形成p型井擴散層23。在此一情況中，以200 keV之植入能量植入約 $1E13$ 原子/ cm^2 之劑量的硼(B)離子。此外，在通道植入中，以10至20 KeV之植入能量植入約 $1E11$ 至 $2E13$ 原子/ cm^2 之劑量的硼(B)離子。

完成離子植入程序之後，移除該光阻圖案。此外，藉由濕式蝕刻移除襯墊氧化物膜21。

接著，如圖3B中顯示，在半導體基板3之表面上形成閘極絕緣膜25。在此程序中，於其中形成高電壓MOS電晶體之區域中形成厚閘極絕緣膜25，並於其中形成低電壓MOS電晶體之區域中形成薄閘極絕緣膜25。

首先，形成由氧化矽構成之厚閘極絕緣膜25。例如，在針對3.3 V之電源供應電壓所設計之MOS電晶體中，厚度係大約7.5 nm，而在針對2.5 V之電源供應電壓所設計之MOS電晶體中，厚度係大約5.5 nm。然後，藉由使用一光阻圖案作為遮罩之蝕刻移除其中形成低電壓MOS電晶體之區域中的厚閘極絕緣膜25。

接著，在其中形成低電壓MOS電晶體之區域中形成薄閘極絕緣膜25。例如，在針對1.0 V所設計之MOS電晶體

中，厚度係大約1.2至1.8 nm。

閘極絕緣膜25可係藉由快速熱氧化(RTO)形成之熱氧化物膜或氮氧化物膜。此外，為進一步減小閘極洩漏，亦可能使用由以Hf為主或以Zr為主之氧化物製成之高介電膜。

接著，於閘極絕緣膜25上藉由LPCVD沈積構成閘極電極之多晶矽膜27。多晶矽膜27之厚度取決於技術節點，且在90-nm節點下係大約150至200 nm。此外，一般而言，鑑於程序可控制性，厚度傾向於隨節點而減小以便能不增大閘極縱橫比。

接著，雜質係植入至多晶矽膜27中以作為避免閘極空乏之措施。在此步驟中，使用光阻圖案作為遮罩，將磷(P)或砷(As)離子植入至NMOS區域中，並將硼(B)、氟化硼(BF₂)或銦(In)離子植入至PMOS區域中。植入劑量係大約1E15至1E16原子/cm²。於此，術語"避免閘極空乏之措施"指對付措施，其用於對付的事實在於隨閘極絕緣膜之厚度減小，閘極絕緣膜之實體厚度與閘極多晶矽膜中之空乏層之厚度之影響變得不可忽略，且閘極膜之有效厚度不減小，而導致Tr.效能減低。

在此一情況中，為避免植入至多晶矽膜27中之雜質侵入閘極絕緣膜25下之區域，可結合植入氮(N₂)。

此外，作為避免閘極空乏之措施，可沈積SiGe多晶膜來替代用於構成閘極電極的多晶矽膜；可完全矽化閘極電極；或可使用金屬閘極。

接著，於多晶矽膜27上形成在閘極製造程序期間作為遮

罩之遮罩層29。作為遮罩層29，使用氧化矽膜、氮化矽膜或其類似物。遮罩層29之厚度係大約10至100 nm。

接著，如圖3C中顯示，藉由使用一光阻圖案作為遮罩之使用RIE系統或其類似物之蝕刻將遮罩層29圖案化成閘極電極形狀。完成蝕刻程序之後，移除該光阻圖案。

然後，使用RIE系統或其類似物透過圖案化遮罩層29蝕刻多晶矽膜27以形成由圖案化多晶矽膜27構成之閘極電極9。此外，在此程序中，亦可藉由蝕刻來圖案化閘極絕緣膜25。

接著，於閘極電極9之側壁上形成偏移間隔物31。在此步驟中，首先，沈積由TEOS膜、HTO膜、氮化矽膜或其類似物構成之偏移間隔物之絕緣膜，並使絕緣膜經受使用RIE系統之回蝕程序以獲得偏移間隔物31。藉由於閘極電極9之側壁上沈積偏移間隔物31，增大有效通道長度，並可減小短通道效應。此外，在形成偏移間隔物31之前，可能實施藉由RTO或其類似物氧化閘極電極之側壁的步驟。此步驟具有減低為寄生電容之閘極重疊電容之效果。

接著，於閘極電極9之側在半導體基板3之表面上執行囊袋植入(圖式中未顯示輪廓)，並形成延伸擴散層33。在此步驟中，使用光阻圖案作為遮罩，對PMOS區域與NMOS區域中之每一者分別執行離子植入。

在PMOS區域中之囊袋植入中，植入約 $1\text{E}12$ 至 $1\text{E}14$ 原子/ cm^2 之劑量的砷(As)或磷(P)。在延伸擴散層33中，離子植入約 $1\text{E}15$ 至 $2\text{E}15$ 原子/ cm^2 之劑量的硼(B)、氟化硼(BF_2)

或銦(In)。

同時，在NMOS區域中之囊袋植入中，離子植入約 $1\text{E}12$ 至 $1\text{E}14$ 原子/ cm^2 之劑量的硼(B)、氟化硼(BF_2)或銦(In)。在延伸擴散層33中，離子植入約 $1\text{E}14$ 至 $2\text{E}15$ 原子/ cm^2 之劑量的砷(As)或磷(P)。此外，在對NMOS區域施加根據本發明之具體實施例之結構時，可省略延伸擴散層33之形成。

此外，在NMOS區域與PMOS區域上執行囊袋植入之前，為抑制植入時的通道作用，可(例如)藉由植入Ge執行預非晶化。此外，為減小可能在形成延伸擴散層33之後產生瞬間增強擴散(TED)或其類似物之植入缺陷，可額外執行在約 800°C 至 900°C 下之快速熱退火(RTA)處理。

圖3D中顯示之步驟係根據本發明之具體實施例之特性步驟中的一者。

此即，首先，藉由CVD依序形成具有約 10 nm 之厚度之氧化矽膜35與具有約 50 nm 之厚度之氮化矽膜37。儘管在圖式中未顯示，其上可進一步沈積氧化矽膜。

接著，藉由使用一光阻圖案(即，遮罩圖案，未顯示)之蝕刻使包括氧化矽膜35與氮化矽膜37之層壓膜經受圖案化。在此步驟中，使氧化矽膜35與氮化矽膜37經受圖案化使得在通道長度方向上具有預定寬度W之開口係穿透由包括氧化矽膜35與氮化矽膜37之層壓膜構成之側壁而提供於閘極電極9之兩側。從而，部分允許包括氧化矽膜35與氮化矽膜37之層壓膜在每一閘極電極9之每一側上使具有預定寬度W之部分保留於外側。

應注意，例如，採用相同標準之MOS電晶體以具有實質相同的預定寬度W。

接著，藉由使用光阻圖案作為遮罩之RIE執行凹陷蝕刻，其中使半導體基板3凹陷。從而，在半導體基板3之表面(井擴散層23)中形成具有預定寬度W之凹陷部分39。凹陷部分之深度係大約150 nm。源極/汲極區域之接面深度係藉由凹陷部分之深度及稍後執行之退火處理來決定。因此，隨著技術節點提升，縮小進行，且蝕刻深度減小。

完成蝕刻程序之後，移除該光阻圖案。

接著，如圖4A中顯示，在凹陷半導體基板3之表面上(即，在凹陷部分39中)，形成由具有與半導體基板3不同之晶格常數之半導體材料構成的磊晶層11。

如上文中參考圖1所說明的，在PMOS區域中，磊晶層11使用具有比構成半導體基板3之矽(Si)大之晶格常數的矽鍺(SiGe)。在此程序中，NMOS區域係保持由氧化矽膜或包括氧化矽膜與氮化矽膜之層壓膜所覆蓋。含硼(B)之矽鍺(SiGe)係使用二氯矽烷($\text{Si}_2\text{H}_2\text{Cl}_2$)、二硼烷(B_2H_6)、氯化氫(HCl)、氫(H_2)等作為氣體物種在600°C至800°C下磊晶成長。

同時，在NMOS區域中，磊晶層11使用具有比構成半導體基板3之矽(Si)小之晶格常數的矽碳(SiC)。在此程序中，PMOS區域係保持由氧化矽膜或包括氧化矽膜與氮化矽膜之層壓膜所覆蓋。含磷(P)之矽碳(SiC)係使用矽烷(SiH_4)、丙烷(C_3H_6)、磷(PH_3)、氯化氫(HCl)等作為氣體物

種在600°C至800°C下磊晶成長。

接著，如圖4B中顯示，使包括氧化矽膜35與氮化矽膜37之層壓膜經受回蝕程序以於閘極電極9之側形成側壁37a。從而，在作用區域7之部分中曝露半導體基板3之表面A。

接著，如圖4C中顯示，形成源極/汲極區域15。在此步驟中，使用光阻圖案作為遮罩，對PMOS區域與NMOS區域中之每一者分別執行離子植入。

在PMOS區域中，作為p型雜質，離子植入 $1\text{E}15$ 至 $1\text{E}16$ 原子/ cm^2 之劑量的硼(B)或氟化硼(BF_2)。

同時，在NMOS區域中，作為n型雜質，離子植入 $1\text{E}15$ 至 $1\text{E}16$ 原子/ cm^2 之劑量的砷(As)或磷(P)。

完成離子植入程序後，移除該等光阻圖案，並在約800°C至1,100°C下執行活化退火。使用RTA系統、尖波RTA系統或其類似物。

從而，獲得p型或n型MOS電晶體Tr，MOS電晶體中之每一者包括閘極電極9與佈置在閘極電極9之兩側之源極/汲極區域15，該等源極/汲極區域15各自包括其中擴散雜質之磊晶層11與擴散層13。

接著，如圖4D中顯示，藉由矽化曝露之矽表面形成矽化物層。在此步驟中，首先，在天然氧化物膜上執行濕式蝕刻處理，並使用濺鍍系統沈積約10 nm之厚度之(例如)由鎳(Ni)構成之金屬膜。然而，曝露之矽部分係藉由在約300°C至400°C下執行退火處理而矽化。在矽化後保留之金屬膜係藉由濕式蝕刻來移除。然後，在約500°C至600°C下執

行退火處理以形成由矽化鎳構成之矽化物層41。矽化物層41僅以自對準方式形成於由多晶矽構成之閘極電極9、由矽鍺(SiGe)構成之磊晶層11與由單晶矽構成之擴散層13上。

此外，作為金屬膜，除了鎳(Ni)之外可使用鈷(Co)、鈦(Ti)、鉑(Pt)、鎢(W)或其類似物。在此一情況中，獲得矽化鈷(CoSi_2)、矽化鈦(TiSi_2)、矽化鉑(PtSi)、矽化鎢(WSi_2)或其類似物。

接著，如圖5A中顯示，於閘極電極9、磊晶層11與擴散層13上形成由氮化矽構成之應力膜43。在此步驟中，形成不同應力膜43，使得拉伸應力係施加至其中佈置n型MOS電晶體Tr之區域且壓縮應力係施加至其中佈置p型MOS電晶體Tr之區域。

首先，作為應力膜43，藉由LPCVD、p-CVD或其類似物沈積約5至100 nm之厚度之賦予拉伸應力的氮化矽膜(拉伸 Si_3N_4)。接著，作為處理應力膜43所使用之停止膜(未顯示)，藉由CVD或其類似物沈積約100 nm之厚度的氧化矽膜(TEOS膜、PSG膜、BPSG膜、SOG膜或其類似物)。然後，藉由使用光阻圖案作為遮罩之蝕刻移除其中佈置p型MOS電晶體Tr之區域中的停止膜，並使用停止膜作為遮罩，移除應力膜43。在此階段中，pFET之側壁膜亦因蝕刻選擇性/過度蝕刻而移除。

從而，其中佈置n型MOS電晶體Tr之區域係由對通道區域ch施加拉伸應力之應力膜43所覆蓋。

接著，作為應力膜43，藉由CVD或其類似物沈積約5至100 nm之厚度之賦予壓縮應力的氮化矽膜(壓縮Si₃N₄)。然後，在其中佈置n型MOS電晶體Tr之區域中，移除此一賦予壓縮應力之應力膜43。

從而，其中佈置p型MOS電晶體Tr之區域係由對通道區域ch施加壓縮應力之應力膜43所覆蓋。

藉由上述步驟獲得具有與如圖1中顯示之結構相同之結構的半導體裝置1a。下文中將說明接續的步驟。

首先，如圖5B中顯示，藉由CVD沈積約100至1,000 nm之厚度之氧化矽膜45(如TEOS膜、PSG膜、BPSG膜或SOG膜)，以便能覆蓋應力膜43，並藉由CMP執行平坦化。

接著，如圖5C中顯示，於氧化矽膜45與應力膜43中形成通道孔47以便能到達源極/汲極區域15之表面上的矽化物層41。在此步驟中，使用光阻圖案(未顯示)作為遮罩來執行RIE。藉由RIE形成通道孔47後，移除光阻圖案。

然後，如圖5D中顯示，藉由以導電材料填充通道孔47來形成接點49。在此步驟中，首先，藉由濺鍍或CVD沈積氮化鈦(TiN)/鈦(Ti)之層壓膜以作為阻障膜，且隨後藉由CVD沈積鎢(W)膜。鎢膜之厚度係大約100至500 nm。接著，使鎢膜經受CMP或回蝕程序，且從而藉由僅填充通道孔47之內側形成接點49。

接著，於氧化矽膜45上形成連接至接點49之互連線51。在此步驟中，首先，藉由濺鍍沈積鋁(Al)膜，且隨後藉由使用光阻圖案作為遮罩之RIE使鋁膜經受圖案蝕刻。從

而，形成由鋁製成的互連線51。作為互連線51之材料，可使用具有低電阻之銅(Cu)。

儘管在圖式中未顯示接續步驟，然而藉由在一或若干上層中形成互連線，可形成包括二層、三層、四層或四層以上之多層互連結構。從而，可能獲得具有多層互連結構的半導體裝置。

根據上述第一具體實施例，可能獲得其中源極/汲極區域15包括磊晶層11與擴散層13之半導體裝置1a。因此，可藉由改變擴散層13之寬度來調整磊晶層11之寬度。

因此，在參考圖3D所說明之步驟中，其中形成具有對應磊晶層之寬度之預定寬度W的凹陷部分39，藉由在不受作用區域7之閘極電極9之布局的影響下將凹陷部分39之寬度控制成預定寬度W，可能以考慮蝕刻期間之微負載效應之蝕刻深度形成凹陷部分39。明確地說，藉由將凹陷部分39之寬度設定成預定寬度W，可能獲得其中因抑制微負載效應導致蝕刻深度變動的凹陷部分39。

因此，可控制於凹陷部分39中形成之磊晶層11之深度而使其一致。

此外，由於磊晶層11之形成面積(布局面積)係在不受布局之影響下，因對應之擴散層13之部分而減小，故而可能獲得具有小數目結晶缺陷之磊晶層11。

因此，可能藉由具有控制預定深度之磊晶層11來抑制對閘極電極9下之通道區域ch所施加之應力的變動。此外，由於可在不受布局影響下獲得具有小數目之結晶缺陷的磊

晶層11，故而可減小接面洩漏。因此，能夠提升電晶體Tr的特性。

此外，儘管藉由運用此一結構減小磊晶層11之體積，然而可能藉由將磊晶層11之深度設定在特定值來維持對通道區域ch所施加之應力(參考K. Ota等人，"Scalable eSiGe S/D technology with less layout dependence for 45-nm generation"，2006年VLSI技術研討會技術論文輯要，2006年)。

此外，如上所述，由於藉由對應之擴散層13之部分減小磊晶層11之形成面積(布局面積)，故而使覆蓋磊晶層11外側之側壁的應力膜43接近通道區域ch。從而，可增強應力膜43對通道區域ch施加應力的效果。

第二具體實施例

圖6係顯示根據本發明之第二具體實施例之半導體裝置之結構的示意性剖面圖。圖6中顯示之半導體裝置1b具有與根據第一具體實施例於圖1中顯示之半導體裝置1a相同的結構，除了構成源極/汲極區域15之擴散層13的深度係大於磊晶層11之深度外。

在具有此一結構之半導體裝置1b中，除了第一具體實施例之效果外，藉由增大相對於閘極電極9之位於磊晶層11外側之擴散層13之深度，在減小短通道效應之同時，可減小於p-n接面之空乏層的電場，因而可進一步提升接面洩漏。此外，藉由增大擴散層13之深度，減小於接面之基板雜質濃度。因此，可減小接面電容，並可提升MOS電晶體

Tr之操作速度。

第三具體實施例

圖7係顯示根據本發明之第三具體實施例之半導體裝置之結構的示意性剖面圖。圖7中顯示之半導體裝置1c具有與根據第一具體實施例於圖1中顯示之半導體裝置1a相同的結構，除了構成源極/汲極區域15之擴散層13之表面之高度係低於閘極電極9下之半導體基板3之表面之高度外。

在具有此一結構之半導體裝置1c中，覆蓋電晶體Tr之應力膜43係延伸至低於通道區域ch之位置。從而，除了第一具體實施例之效果外，可增強由應力膜43對通道區域ch施加應力的效果。

第四具體實施例

圖8係顯示根據本發明之第四具體實施例之半導體裝置之結構的示意性剖面圖。圖8中顯示之半導體裝置61a具有具備p型MOS電晶體Tr之結構。半導體裝置61a與根據第一具體實施例於圖1中顯示之半導體裝置1a之不同在於僅源極/汲極區域15中之一者包括磊晶層11，且源極/汲極區域15中之另一者僅包括擴散層13。此外，相反電導係數類型(n型)之擴散層(相反電導係數類型擴散層63)係毗鄰擴散層13來佈置。將省略對與第一具體實施例之結構相同之結構的重複說明。

在半導體裝置61a中，提供相反電導係數類型擴散層63以作為相對於井擴散層23之接點區域。相反電導係數類型擴散層63與毗鄰其而佈置之源極/汲極區域15係因佈置於

其表面上之矽化物層41而短路。在半導體裝置61a中，藉由運用此一結構，減小井接點。

在此一結構中，由於擴散層13構成毗鄰相對於井擴散層23(相反電導係數類型擴散層63)之接點區域來佈置並對該接點區域短路之源極/汲極區域15，故而可能避免相反電導係數類型擴散層63中之n型雜質擴散至源極/汲極區域15中並到達通道區域ch。

此即，如圖9之比較性範例中顯示，在其中由矽鍺(SiGe)構成之磊晶層11構成毗鄰相反電導係數類型擴散層63而佈置之源極/汲極區域15的情況中，於相反電導係數類型擴散層63中之n型雜質輕易地擴散至磊晶層11中並到達通道區域ch。如此之理由在於n型雜質之擴散率在SiGe中係高於在由矽構成之半導體基板中(即，在砷(As)之情況中高出大約七倍，且在磷(P)之情況中高出大約兩倍)。

因此，如圖8中顯示，藉由運用其中僅源極/汲極區域15中之一者包括磊晶層11且毗鄰相反電導係數類型擴散層63而佈置之源極/汲極區域15中之另一者包括擴散層13的結構，可能避免相反電導係數類型擴散層63中之n型雜質擴散至通道區域ch中，並可抑制p型MOS電晶體Tr之臨限值的變動。

第五具體實施例

圖10係顯示根據本發明之第五具體實施例之半導體裝置之結構的示意性剖面圖。圖10中顯示之半導體裝置61b具有與根據第四具體實施例之半導體裝置61a相同之結構，

除了源極/汲極區域15中之一者包括與磊晶層11在一起之擴散層13外。

在此一情況中，擴散層13係穿透磊晶層11而佈置在閘極電極9之側。

藉由運用此一結構，磊晶層11在通道長度方向上之寬度可設定成受擴散層13控制之預定寬度W。因此，可獲得與第一具體實施例相同的效果。

習知此項技術者應瞭解，可根據設計要求及其他因素進行各種修改、組合、次組合及變更，只要其係在隨附申請專利範圍或其等效內容的範疇內即可。

【圖式簡單說明】

圖1係顯示根據本發明之第一具體實施例之半導體裝置之結構的示意性剖面圖；

圖2A至2E係顯示根據第一具體實施例之製造半導體裝置之方法中之步驟的示意性剖面圖；

圖3A至3D係顯示根據第一具體實施例之製造半導體裝置之方法中接續圖2E中顯示之步驟之步驟的示意性剖面圖；

圖4A至4D係顯示根據第一具體實施例之製造半導體裝置之方法中接續圖3D中顯示之步驟之步驟的示意性剖面圖；

圖5A至5D係顯示接續圖4D中顯示之步驟之步驟的示意性剖面圖；

圖6係顯示根據本發明之第二具體實施例之半導體裝置

之結構的示意性剖面圖；

圖7係顯示根據本發明之第三具體實施例之半導體裝置之結構的示意性剖面圖；

圖8係顯示根據本發明之第四具體實施例之半導體裝置之結構的示意性剖面圖；

圖9係顯示第四具體實施例之比較性範例的示意性剖面圖；

圖10係顯示根據本發明之第五具體實施例之半導體裝置之結構的示意性剖面圖；以及

圖11係顯示根據先前技術之半導體裝置之結構的示意性剖面圖。

【主要元件符號說明】

1a	半導體裝置
1b	半導體裝置
1c	半導體裝置
3	半導體基板
3a	溝渠
5	隔離膜
7	隔離作用區域
9	閘極電極
11	磊晶層
13	擴散層
15	源極/汲極區域
21	襯墊氧化物膜

22	氮化矽膜
22a	開口
23	井擴散層
25	閘極絕緣膜
27	多晶矽膜
29	遮罩層
31	偏移間隔物
33	延伸擴散層
35	氧化矽膜
37	氮化矽膜
37a	側壁
39	凹陷部分
41	矽化物層
43	應力膜
45	氧化矽膜
47	通道孔
49	接點
51	互連線
61a	半導體裝置
61b	半導體裝置
63	相反電導係數類型擴散層
101	半導體基板
102	隔離膜
103	隔離作用區域

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104	閘極電極
105	磊晶層
A	表面
ch	通道區域
Tr	電晶體

十、申請專利範圍：

1. 一種半導體裝置，其包含：
 - 一閘極電極，其佈置於一半導體基板上；以及
 - 源極/汲極區域，其佈置於該閘極電極之兩側，該等源極/汲極區域係由植入雜質形成，
 - 其中該等源極/汲極區域包括
 - 一磊晶層，其藉由於該閘極電極之一側之一凹陷位置中磊晶成長具有與該半導體基板不同之晶格常數的一半導體材料而形成，以及
 - 一擴散層，其佈置於該半導體基板之一表面層中。
2. 如請求項1之半導體裝置，其中該磊晶層係佈置於該閘極電極之兩側中之每一者，且該擴散層係佈置於該磊晶層外側。
3. 如請求項2之半導體裝置，其中該磊晶層係在該通道長度方向上以一預定寬度佈置。
4. 如請求項2之半導體裝置，其中該擴散層之表面係低於位在閘極電極下之半導體基板的表面。
5. 如請求項1之半導體裝置，其中該等源極/汲極區域中之一者包括該磊晶層，且該等源極/汲極區域中之另一者僅包括該擴散層。
6. 如請求項5之半導體裝置，其中具有與該擴散層不同之電導係數類型之一相反電導係數類型擴散層係佈置成與該擴散層毗鄰，且該擴散層與該相反電導係數類型擴散層係藉由佈置於該源極/汲極區域與該相反電導係數類型

擴散層之表面上之一矽化物層而短路。

7. 如請求項6之半導體裝置，其中該半導體基板係由矽構成，且該磊晶層係由矽鍺構成。
8. 如請求項5之半導體裝置，其中該等源極/汲極區域中之一者包括該磊晶層及佈置於其外側之該擴散層。
9. 如請求項8之半導體裝置，其中該擴散層之表面係低於位在閘極電極下之半導體基板的表面。
10. 一種製造一半導體裝置之方法，其包含：
 - 一第一步驟，其於一半導體基板上形成一閘極電極；
 - 一第二步驟，其藉由透過一遮罩圖案之蝕刻於該閘極電極之一側使該半導體基板之一表面層凹陷；
 - 一第三步驟，其於凹陷部分上形成由具有與該半導體基板不同之晶格常數的半導體材料構成之磊晶層；以及
 - 一第四步驟，其藉由移除該遮罩圖案以曝露該半導體基板之表面層並使雜質擴散至該磊晶層及該半導體基板之表面層中來形成源極/汲極區域，該等源極/汲極區域包括其中雜質經擴散之磊晶層與藉由使雜質擴散至該表面層中而形成之一擴散層。

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十一、圖式：

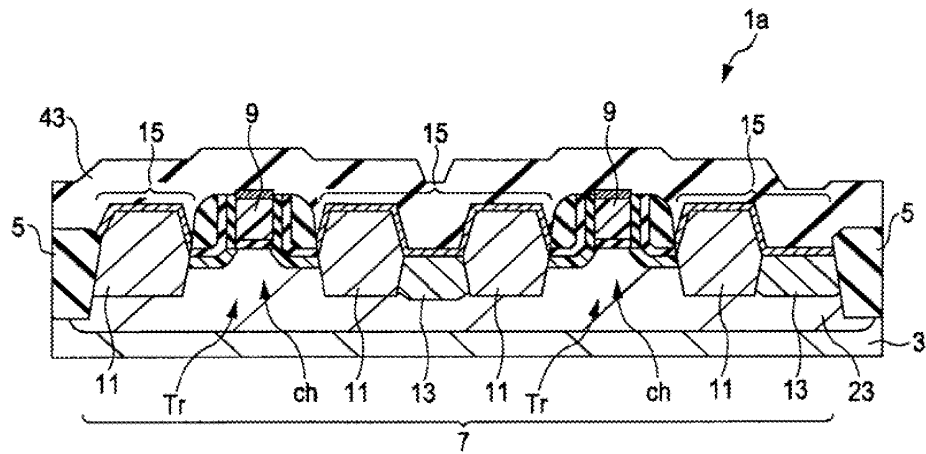
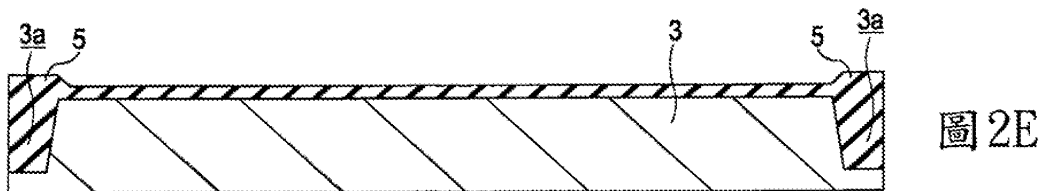
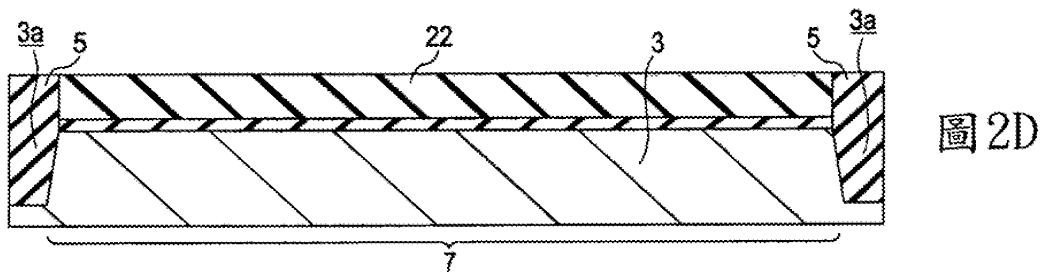
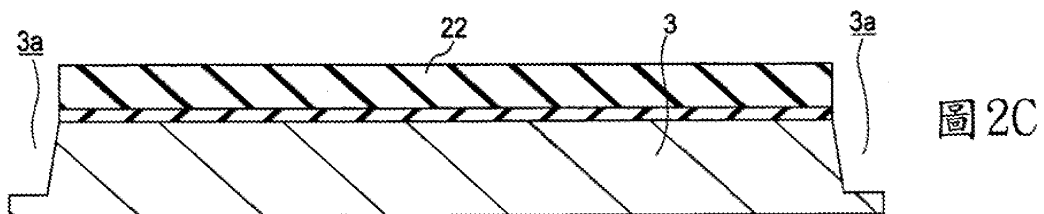
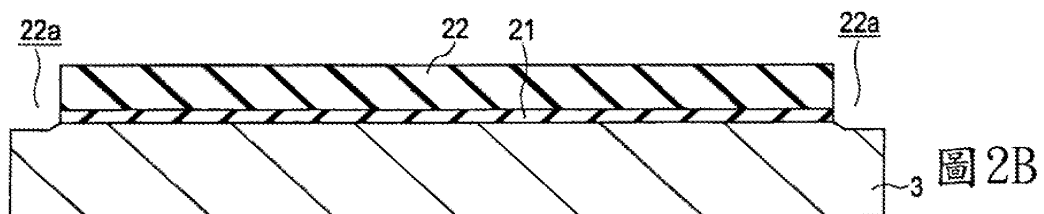
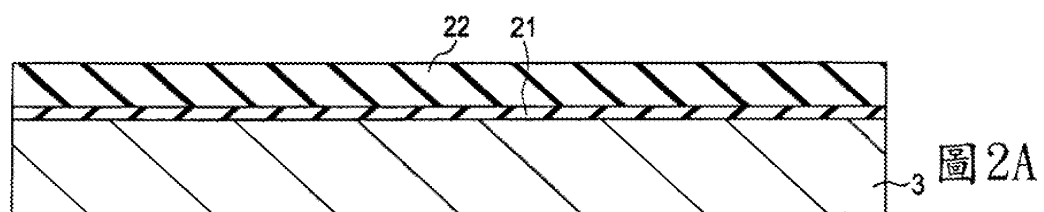
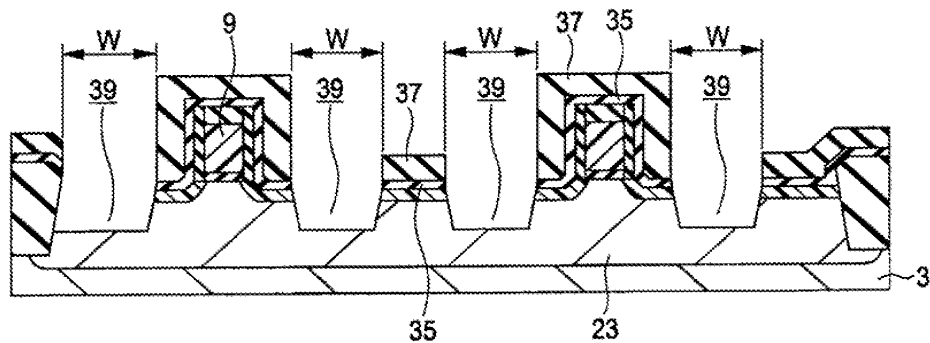
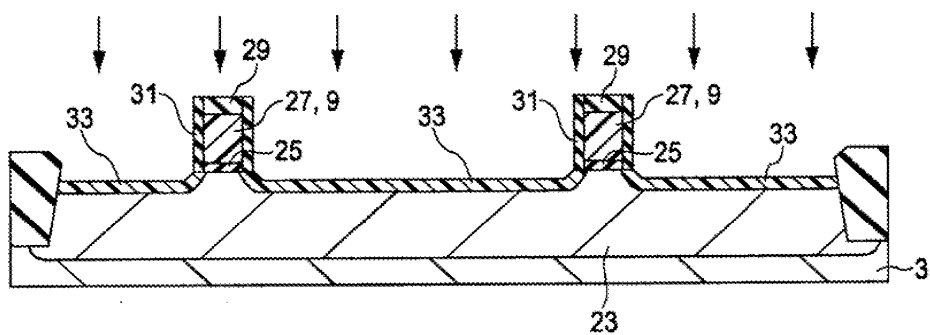
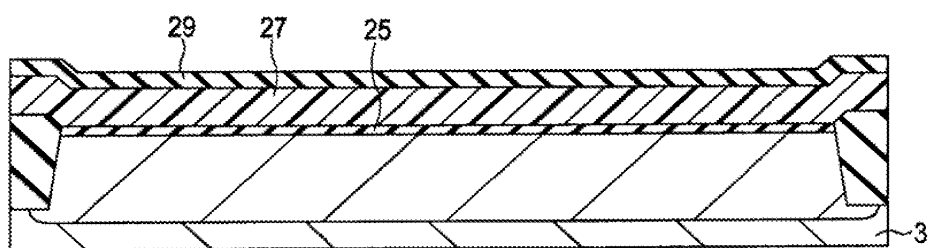
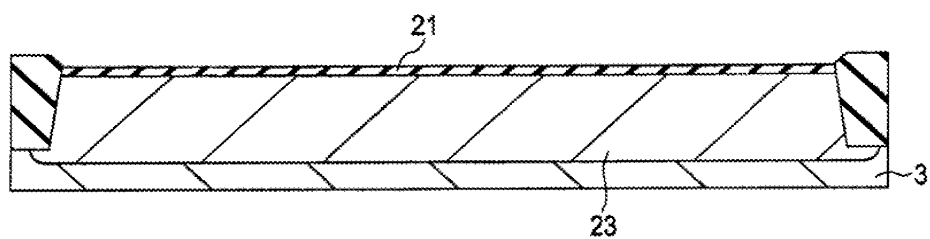


圖 1





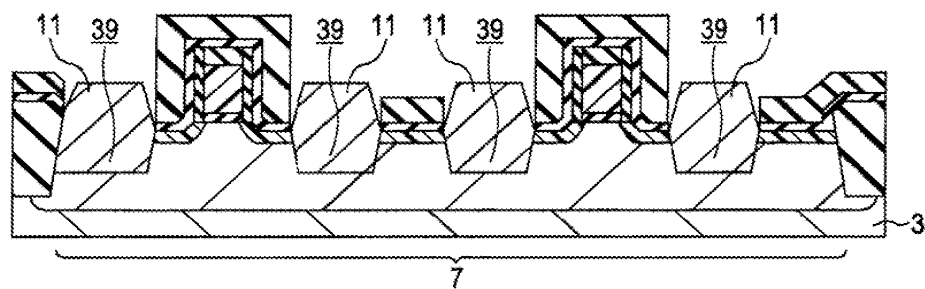


圖 4A

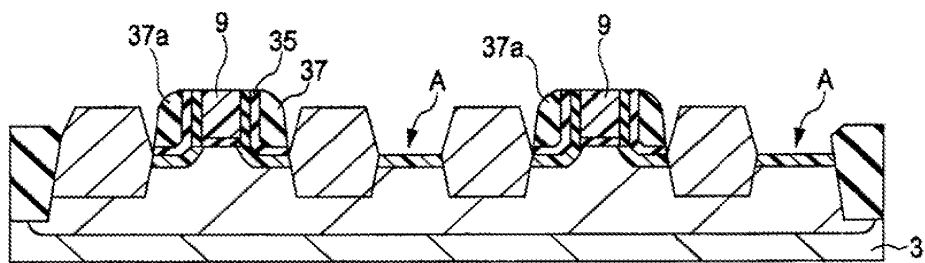


圖 4B

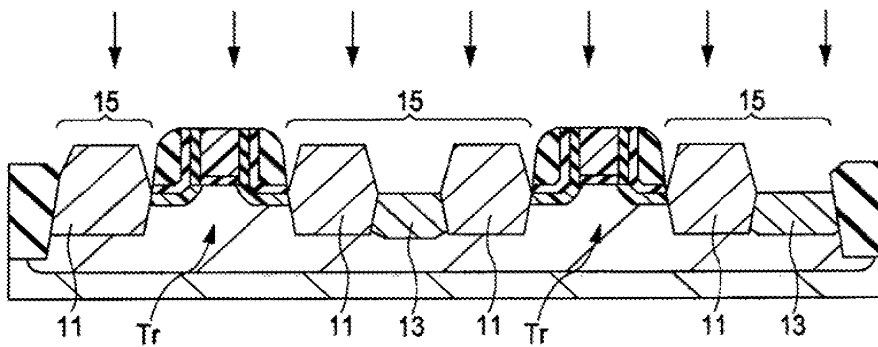


圖 4C

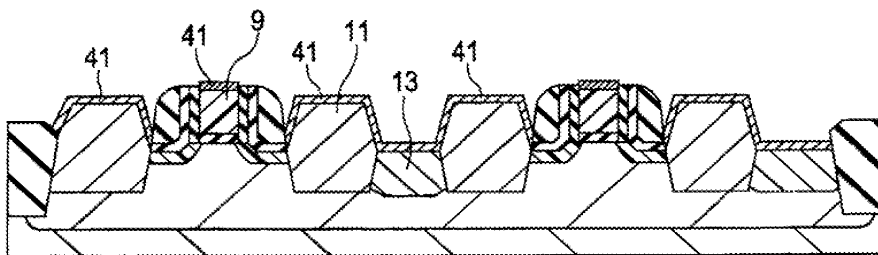


圖 4D

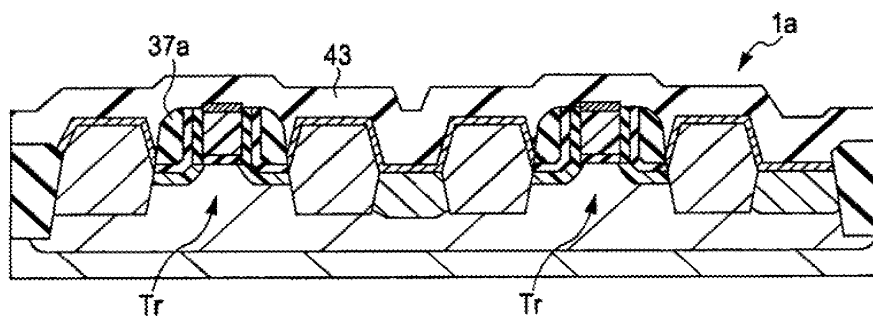


圖 5A

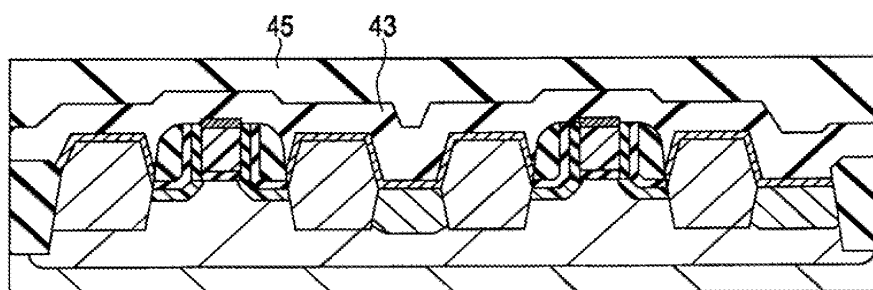


圖 5B

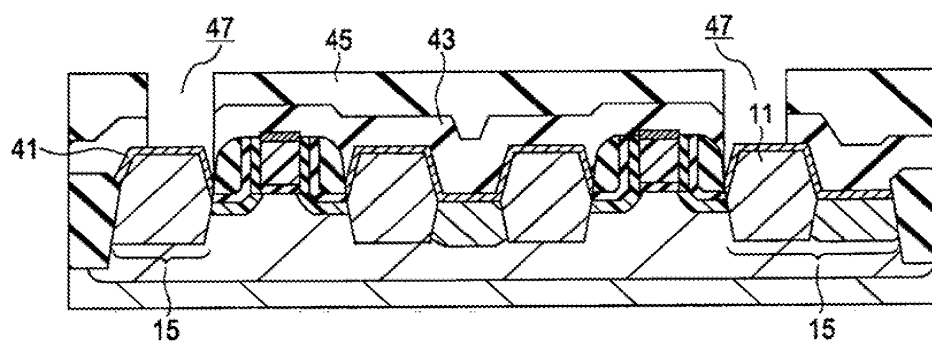


圖 5C

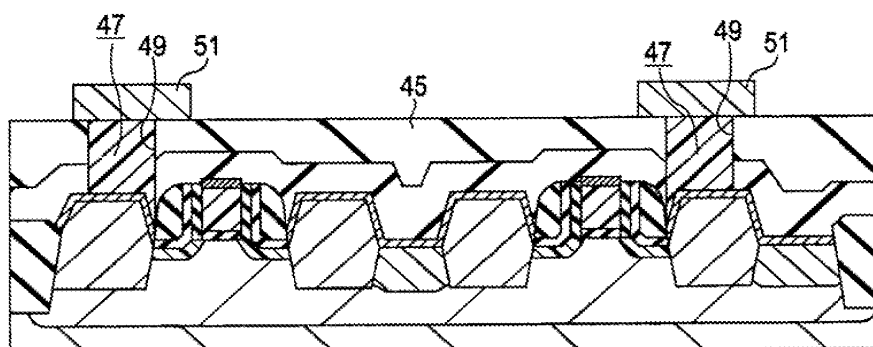


圖 5D

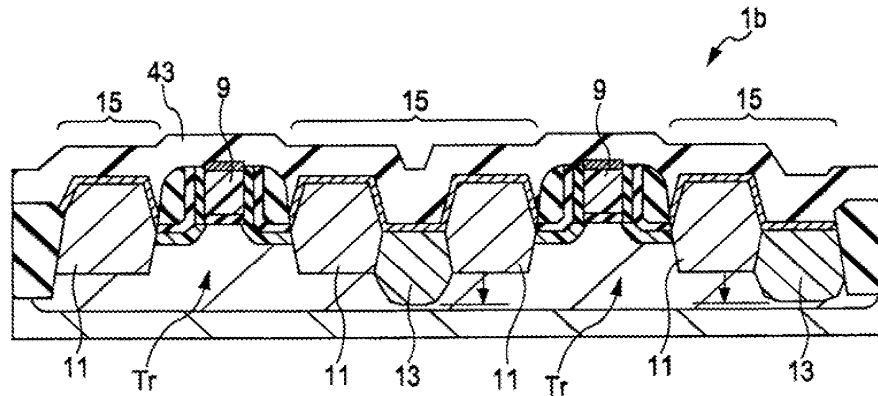


圖 6

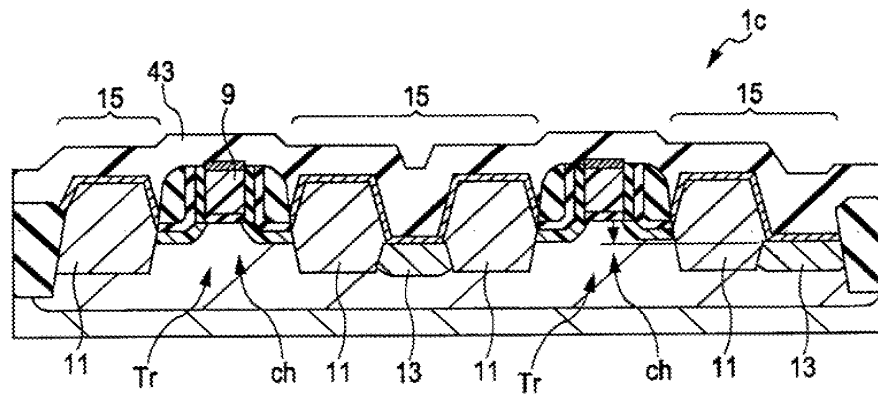


圖 7

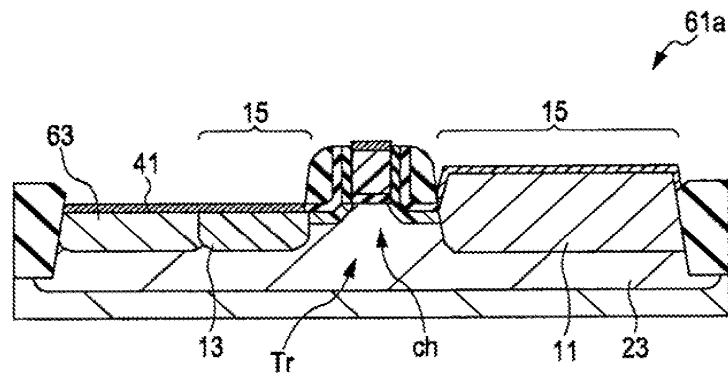


圖 8

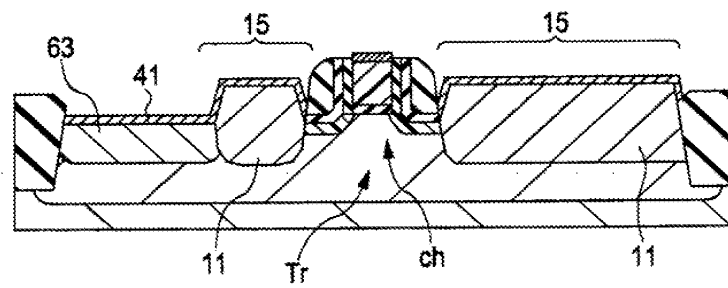


圖 9

Abstract of TW 200931599

A silicon-oxide-nitride-oxide-silicon (SONOS) memory and the corresponding forming method. The memory includes a plurality of select gate structures arranged in an array, a plurality of charge trap spacers that do not contact each other, and a plurality of word lines. The word lines can directly contact the select gates' surfaces of the select gate structures. All of the select gate structures disposed in one line can share two charge trap spacers, and the two charge trap spacers are disposed on the opposed sidewalls of these select gate structures.

200931599

發明專利說明書

(本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫)

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一、發明名稱：(中文/英文)

具有分離式電荷擷取側壁子之記憶體及其製作方法 /
MEMORY HAVING SEPARATED CHARGE TRAP SPACERS
AND METHOD OF FORMING THE SAME

二、申請人：(共 1 人)

姓名或名稱：(中文/英文)

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國 籍：(中文/英文)

中華民國 / TWN

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200931599

國 籍：(中文/英文)

1. 中華民國 / TWN
2. 中華民國 / TWN
3. 中華民國 / TWN

四、聲明事項：

☐ 主張專利法第二十二條第二項 ☐ 第一款或 ☐ 第二款規定之事實，其事實發生日期為： 年 月 日。

☐ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號 順序註記】

☐ 有主張專利法第二十七條第一項國際優先權：

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號 順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料 【格式請依：寄存機構、日期、號碼 順序註記】

國外生物材料 【格式請依：寄存國家、機構、日期、號碼 順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

本發明提供一種矽-氧化矽-氮化矽-氧化矽-矽型 (silicon-oxide-nitride-oxide-silicon，簡稱為 SONOS) 型記憶體及其製作方法。前述記憶體包含有複數個呈陣列排列之選擇閘極結構、複數個不相接觸之電荷擷取側壁子與複數條字元線。字元線可直接接觸選擇閘極結構的選擇閘極表面。位於同一行的選擇閘極結構皆可以共用二個電荷擷取側壁子，且這二個電荷擷取側壁子位於這些選擇閘極結構的相對側壁。

六、英文發明摘要：

A silicon-oxide-nitride-oxide-silicon (SONOS) memory and the corresponding forming method. The memory includes a plurality of select gate structures arranged in an array, a plurality of charge trap spacers that do not contact each other, and a plurality of word lines. The word lines can directly contact the select gates' surfaces of the select gate structures. All of the select gate structures disposed in one line can share two charge trap spacers, and the two charge trap spacers are disposed on the opposed sidewalls of these select gate structures.

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七、指定代表圖：

(一)本案指定代表圖為：第 (15) 圖。

(二)本代表圖之元件符號簡單說明：

200	半導體基底	202	P 型摻雜井
204	選擇閘極結構	206	閘極介電層
208	閘極導電層	212	電荷擷取側壁子
216	N 型摻雜區	234	閘極間介電層
240	字元線		

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

九、發明說明：

【發明所屬之技術領域】

本發明係關於一種非揮發性記憶體及其製作方法，尤指一種 SONOS 型記憶體結構。

【先前技術】

非揮發性記憶體由於具有不因電源供應中斷而造成儲存資料遺失之特性，因此被廣泛使用。而依照單元記憶胞儲存之資料位元數，又可區分為單一位元儲存(single-bit storage)非揮發性記憶體，例如某些氮化物唯讀記憶體(nitride read-only-memory，簡稱為 NROM)、傳統金屬-氧化矽-氮化矽-氧化矽-矽型(metal-oxide-nitride-oxide-silicon，簡稱為 MONOS)記憶體或傳統矽-氧化矽-氮化矽-氧化矽-矽型(silicon-oxide-nitride-oxide-silicon，簡稱為 SONOS)記憶體，與雙位元儲存(dual-bit storage)非揮發性記憶體，例如分離編程虛擬接地(split program virtual ground) SONOS 型(簡稱為 SPVG SONOS)記憶體或分離編程虛擬接地(split program virtual ground) MONOS (簡稱為 SPVG MONOS) 型記憶體，其中 SPVG SONOS 型記憶體與 SPVG MONOS 型記憶體之單元記憶胞由於可儲存二位元之資訊，因此相較於一般單一位元儲存非揮發性記憶體可儲存更大量的資訊，已逐漸成為非揮發性記憶體之主流。

請參考第 1 圖與第 2 圖，第 1 圖與第 2 圖為一習知 SPVG

SONOS 型記憶體之示意圖，其中第 1 圖為習知 SPVG SONOS 型記憶體進行編程(programming)操作時之示意圖，第 2 圖為習知 SPVG SONOS 型記憶體進行抹除(erasing)操作時之示意圖，且於第 1 圖與第 2 圖中僅顯示出單一記憶胞。如第 1 圖所示，SPVG SONOS 型記憶體 10 係形成於一 P 型摻雜井(P well)12 上，其主要包含有一選擇閘極(select gate)14，以及二 N 型之埋入式位元線(buried bit line)位於選擇閘極結構 14 相對側邊之 P 型摻雜井 12 內，分別作為汲極 16 與源極 18。選擇閘極結構 14 與 P 型摻雜井 12 之間包含有一閘極絕緣層 20，而選擇閘極結構 14 上方則包含有一頂蓋層 22。此外，選擇閘極結構 14 之側壁依序包含有一底氧化矽層 24、一氮化矽層 26 與一頂氧化矽層 28，其中氮化矽層 26 係用來作為捕捉電子或電洞的儲存媒介。另外，頂氧化矽層 28 之上方則包含有一字元線 30。

如第 1 圖所示，SPVG SONOS 型記憶體 10 於進行編程操作時係利用源極側邊注入(source-side injection)機制，其電壓操作為對字元線 30 施加一高正電壓，如 6 至 9V 之電壓，對選擇閘極結構 14 施加一低正電壓，如 1V，對源極 18 則施加一正電壓，如 4.5V，並使 P 型摻雜井 12 與汲極 16 之電壓維持在 0V。在此狀況下，穿越選擇閘極結構 14 下方通道(channel)之電子會被捕捉並被侷陷於位於源極 18 之一側之氮化矽層 26 內(如圖中之箭號所示)，藉此改變成不同之啟始電壓(threshold voltage)，以達到儲存資料之功能。此外，透過類似之反向電壓操作即可將電子侷陷於汲極 16 之一側

之氮化矽層 26 內，以儲存另一位元之資料，形成雙位元儲存記憶體。

如第 2 圖所示，當 SPVG SONOS 型記憶體 10 於進行抹除操作時係利用帶對帶電洞注入(band-to-band hot hole injection)機制，其電壓操作為對字元線 30 施加一高負電壓，如 -6 至 -9V 之電壓，對源極 18 則施加一正電壓，如 4.5V，將選擇閘極結構 14 之電壓低於啟始電壓，並使 P 型摻雜井 12 與汲極 16 之電壓維持在 0V。在此狀況下 P 型摻雜井 12 中之電洞會注入源極 18 之一側之氮化矽層 26 內並中和編程操作時侷陷於氮化矽層 26 內之電子，達到資料抹除之作用。此外，侷陷於汲極 16 之一側之氮化矽層 26 內之電子亦可利用類似之電壓操作加以中和。

請參考第 3 圖至第 7 圖，第 3 圖至第 7 圖為一傳統製作 SPVG SONOS 型記憶體之方法示意圖，其中第 3 圖至第 6 圖為部分記憶胞之剖面示意圖，而第 7 圖則為 SPVG SONOS 型記憶體之外觀示意圖。如第 3 圖所示，首先提供一半導體基底 100，並於半導體基底 100 中形成至少一 P 型摻雜井 102，接著再於 P 型摻雜井 102 表面形成複數個選擇閘極結構 104，且各選擇閘極結構 104 由下至上依序包含有一閘極絕緣層 106、一選擇閘極 108 與一頂蓋層 110。

如第 4 圖所示，接著於半導體基底 100 與選擇閘極結構 104 之表面全面沉積一材料層(圖未示)，並利用一回蝕刻製程，全面性地

向下蝕刻前述材料層，直至於各選擇閘極結構 104 之側壁形成犧牲側壁子結構 112，並同時曝露出相鄰之各犧牲側壁子結構 112 間之 P 型摻雜井 102 以形成一開口 114。隨後進行一離子佈植製程，經由各開口 114 於 P 型摻雜井 102 中分別形成一 N 型摻雜區 116，作為埋入式位元線之用。另外於形成 N 型摻雜區 116 後，可進行一驅入(drive-in)製程，以使 N 型摻雜區 116 內之摻質擴散。

如第 5 圖所示，隨後去除各選擇閘極結構 104 側壁之犧牲側壁子結構 112，並於 P 型摻雜井 102、選擇閘極結構 104 與 N 型摻雜區 116 之表面形成一複合介電層 118，作為捕捉電子之儲存媒介。其中，複合介電層 118 為一氧化矽-氮化矽-氧化矽(ONO)介電層，其包含有一底氧化矽層 120、氮化矽層 122 以及一上氧化矽層 124。

最後如第 6 圖與第 7 圖所示，於複合介電層 118 之表面全面沉積一導電層(圖未示)，並利用一微影暨蝕刻製程定義出複數個平行並與選擇閘極結構 104 正交之字元線 126，完成傳統 SPVG SONOS 型記憶體之製作。

然而，由於傳統之複合介電層係為連續結構，會完整地覆蓋到選擇閘極結構，且傳統選擇閘極結構上方製作一頂蓋層，因此傳統方法需另行製作內連接線來控制選擇閘極的電壓。這不但會大幅增加 SPVG SONOS 型記憶體的佈局面積，也導致 SPVG SONOS 型記憶體之製作過程更為繁複。再者，傳統 SPVG SONOS

型記憶體需於選擇閘極結構之側壁製作犧牲側壁子，因此也增加了製程上的複雜度。此外，不論是在進行編程操作時或是進行抹除操作時，傳統方法皆須同時控制 SPVG SONOS 型記憶體之字元線、選擇閘極結構、源極的施加電壓，並使 P 型摻雜井與汲極之電壓維持在特定電壓下，使得 SPVG SONOS 型記憶體之操作過程較為複雜。有鑑於此，申請人乃根據此等缺點及依據多年從事半導體產業之相關經驗，悉心觀察且研究之，而提出改良之本發明，以提升 SONOS 型記憶體之可靠度與良率。

【發明內容】

因此本發明之主要目的為提供一種 SONOS 型記憶體，以解決習知技術無法克服之難題。

本發明提供一種具有分離式電荷擷取側壁子之記憶體，其包含有一半導體基底、複數個不相接觸之選擇閘極結構、複數個不相接觸之電荷擷取側壁子與複數條字元線。半導體基底包含有至少一位於半導體基底表面之第一導電型式摻雜井與複數個位於第一導電型式摻雜井中之第二導電型式摻雜區。選擇閘極結構位於第二導電型式摻雜區之間，排列成至少一行。各選擇閘極結構包含有一設置於第一導電型式摻雜井上之閘極介電層與一設置於閘極介電層上之閘極導電層。前述電荷擷取側壁子位於選擇閘極結構之相對二側壁的表面。各字元線直接接觸各閘極導電層之上表面。

本發明另提供一種製作具有分離式電荷擷取側壁子之記憶體之方法。首先，提供一半導體基底。半導體基底包含有至少一位於半導體基底中的第一導電型式摻雜井。之後，於第一導電型式摻雜井表面形成複數個不相接觸之條狀結構。各條狀結構包含有一設置於第一導電型式摻雜井上之閘極介電層與一設置於閘極介電層上之閘極導電層。接著，於各條狀結構之相對二側壁表面形成分別一電荷擷取側壁子，再進行一離子佈植製程，利用各條狀結構以及各電荷擷取側壁子作為遮罩，於各條狀結構間之第一導電型式摻雜井中分別形成一第二導電型式摻雜區。然後，於第二導電型式摻雜區上形成一閘極間介電層。其後於半導體基底上全面形成一導電層，直接接觸閘極導電層表面。隨後蝕刻導電層與條狀結構，使導電層成為複數個不相接觸且與各第二導電型式摻雜區正交之字元線，並使各條狀結構成為複數個選擇閘極結構。

為讓本發明之上述目的、特徵、和優點能更明顯易懂，下文特舉較佳實施方式，並配合所附圖式，作詳細說明如下。然而如下之較佳實施方式與圖式僅供參考與說明用，並非用來對本發明加以限制者。

【實施方式】

本發明可應用於各式記憶體結構中，例如 SPVG SONOS 記憶體、SPVG MONOS 記憶體、單次可程式記憶體(one-time

programming memory, OTP)、多次可程式記憶體(multi-time programming memory, MTP)、埋入式單次可程式記憶體(embedded one-time programming memory, eOTP)。

請參考第 8 圖至第 15 圖，第 8 圖至第 15 圖為本發明第一較佳實施例製作 SPVG SONOS 型記憶體之方法示意圖，其中為清楚彰顯本發明之特徵，第 8 圖至第 10 圖與第 12 圖至第 14 圖為部分記憶胞之剖面示意圖，而第 11 圖與第 15 圖則為部分 SPVG SONOS 型記憶體之外觀示意圖。需注意的是圖式僅以說明為目的，並未依照原尺寸作圖。如第 8 圖所示，首先提供一半導體基底 200，並利用一圖案化遮罩(未示於圖中)與一離子佈植製程(未示於圖中)於半導體基底 200 中形成至少一 P 型摻雜井 202。接著，利用熱氧化製程或沉積製程於 P 型摻雜井 202 表面形成一層介電層(圖未示)，於介電層表面沉積一層導電層(圖未示)，再於導電層表面形成另一圖案化遮罩(圖未示)，以定義出條狀結構的位置。之後對前述導電層與介電層進行一蝕刻製程，以形成複數個不相接觸之條狀結構 232。各條狀結構 232 由下至上依序包含有一閘極介電層 206 與一閘極導電層 208，其中閘極導電層 208 可作為 SPVG SONOS 型記憶體之選擇閘極。閘極介電層 206 可以包含有氧化矽層等之絕緣材料層，而閘極導電層 208 可以為多晶矽層或金屬層等導電材料所構成。

如第 9 圖所示，接著可先於半導體基底 200 與條狀結構 232

之表面全面沉積一第一氧化矽層 220，覆蓋於條狀結構 232 之側壁。接著，於半導體基底 200 上全面形成一第一氮化矽層 222，覆蓋於第一氧化矽層 220 表面。之後，對第一氮化矽層 222 與第一氧化矽層 220 進行一第一蝕刻製程，暴露出條狀結構 232 之閘極導電層 208 與位於條狀結構 232 間之半導體基底 200，留下位於條狀結構 232 側壁的第一氧化矽層 220 與第一氮化矽層 222。如第 10 圖所示，接著可對第一氮化矽層 222 進行一氧化製程，以使第一氮化矽層 222 的外表面氧化形成一第二氧化矽層 224，藉此於各條狀結構 232 之相對二側壁表面形成分別一具有 I 形結構的電荷擷取側壁子 212，作為電子之儲存媒介。需注意的是，本發明之電荷擷取側壁子 212 可暴露出各條狀結構 232 之閘極導電層 208 的上表面，以使閘極導電層 208 得以直接電連接後續形成的字元線。

於其他實施例中，本發明亦可於半導體基底 200 上全面沉積一第二氧化矽層(圖未示)，覆蓋於第一氮化矽層 222 表面，再對第二氧化矽層進行一第二蝕刻製程，暴露出條狀結構 232 之閘極導電層 208 與位於條狀結構 232 間之半導體基底 200，留下位於第一氮化矽層 222 表面的第二氧化矽層 224，藉此形成電荷擷取側壁子 212。

在本實施例中，電荷擷取側壁子 212 可為一氧化矽-氮化矽-氧化矽(ONO)複合結構，包含有一第一氧化矽層 220、第一氮化矽層 222 以及一第二氧化矽層 224。然而其它複合介電層，例如氮化

矽-氧化矽(NO)介電層、氧化矽-氮化矽(ON)介電層、SiO₂/Ta₂O₅、SiO₂/Ta₂O₅/SiO₂、SiO₂/SrTiO₃、SiO₂/BaSrTiO₂、SiO₂/SrTiO₃/SiO₂、SiO₂/SrTiO₃/BaSrTiO₂、SiO₂/Hf₂O₅/SiO₂等，均可視需要而應用作為電子之儲存媒介。

之後，如第 11 圖所示，進行一自對準之離子佈植製程，利用各條狀結構 232 以及各電荷擷取側壁子 212 作為遮罩，於各條狀結構 232 間之 P 型摻雜井 202 中分別形成一 N 型摻雜區 216，作為記憶體之源極/汲極與埋入式位元線之用。另外，於形成 N 型摻雜區 216 後，可進行一驅入(drive-in)製程，以使 N 型摻雜區 216 內之摻質擴散。值得注意的是，本實施例係以 NMOS 形式之 SPVG SONOS 型記憶體為例說明本發明之方法，因此係於半導體基底 200 中形成 P 型摻雜井 202 與 N 型摻雜區 216，若因產品需求或其他設計考量而欲製作之 SPVG SONOS 型記憶體係為 PMOS 型式，則僅需於半導體基底 200 中利用不同摻質形成 N 型摻雜井與 P 型摻雜區即可。

值得注意的是，本發明亦可於製備閘極導電層 208 之後，先形成一襯氧化層(liner oxide)(圖未示)。再於襯氧化層表面依序沉積一氧化矽層、一氮化矽層與另一氧化矽層，並利用襯氧化層(圖未示)作為回蝕刻製程之蝕刻停止層，形成電荷擷取側壁子 212。而構成電荷擷取側壁子 212 之材料，則可視襯氧化層(圖未示)之有無，選用蝕刻選擇比較高的組合。此外，襯氧化層亦可用來作為 N

型摻雜區 216 之離子佈植製程的犧牲層(sacrificial layer)，以保護 N 型摻雜區 216 表面之晶格結構。

如第 12 圖所示，隨後於半導體基底 200 上全面形成一介電層(圖未示)，覆蓋於條狀結構 232 與 N 型摻雜區 216 上，再對此介電層進行一回蝕刻或化學機械研磨等之平坦化製程，直到暴露出條狀結構 232 之閘極導電層 208，以於 N 型摻雜區 216 上形成一閘極間介電層 234。其後如第 13 圖所示，於半導體基底 200 上全面形成一導電層 236，如一多晶矽層、一金屬矽化物或一金屬層，直接接觸閘極導電層 208 的表面，再於導電層 236 上形成一圖案化遮罩 244。此圖案化遮罩 244 具有複數個不相接觸之條狀開口(未示於圖中)，且各條狀開口與條狀結構 232 正交。

接著如第 14 圖與第 15 圖所示，以圖案化遮罩 244 作為蝕刻遮罩，對導電層 236 與條狀結構 232 進行一蝕刻製程，直到各條狀結構 232 成為複數個不相接觸之選擇閘極結構 204，並使導電層 236 成為複數個不相接觸且與各 N 型摻雜區 216 正交之字元線 240。其中，該蝕刻製程可以去除導電層 236 未被圖案化遮罩 244 所遮蔽之部分，以及條狀結構 232 未被圖案化遮罩 244 所遮蔽之部分，而可以留下部分未被圖案化遮罩 244 所遮蔽之電荷擷取側壁子 212。其後，去除圖案化遮罩 244，完成本實施例 SPVG SONOS 型記憶體之製作。

值得注意的是，於本發明之其他實施例中，形成選擇閘極結構 204 之蝕刻製程也可能會暴露出位於電荷擷取側壁子 212 下方之半導體基底 200，甚至是直接蝕刻掉未被圖案化遮罩 244 所遮蔽之電荷擷取側壁子 212，使得位於同一行的二個選擇閘極結構 204 的電荷擷取側壁子 212 彼此不相連接。請參考第 16 圖與第 17 圖，第 16 圖繪示的是本發明第二較佳實施例 SPVG SONOS 型記憶體之立體示意圖，而第 17 圖繪示的是本發明第三較佳實施例 SPVG SONOS 型記憶體之立體示意圖。如第 16 圖所示，蝕刻製程使得電荷擷取側壁子 212 暴露出位於其下方之半導體基底 200，因此位於同一行的二個選擇閘極結構 204 的電荷擷取側壁子 212 彼此不相連接。如第 17 圖所示，蝕刻製程係完全去除未被圖案化遮罩 244 所遮蔽之電荷擷取側壁子 212。

另需注意的是，於本發明之第一、第二較佳實施例中，電荷擷取側壁子 212 係為一種氧化矽-氮化矽-氧化矽(ONO)的複合結構，而於其他實施例中，電荷擷取側壁子也可以為一種氧化矽-氮化矽-氧化矽-氮化矽(ONON)的複合結構。請參考第 18 圖至第 19 圖，其繪示的是本發明第四較佳實施例製作電荷擷取側壁子之方法示意圖，其中相同的元件或部位沿用相同的符號來表示。如第 18 圖所示，首先提供一半導體基底 200，半導體基底 200 中包含有至少一 P 型摻雜井 202，且半導體基底 200 上包含有與複數個條狀結構 232。各條狀結構 232 由下至上依序包含有一閘極介電層 206 與一閘極導電層 208。

接著，於半導體基底 200 與條狀結構 232 之表面依序沉積一第一氧化矽層 220 與一第一氮化矽層 222，再對第一氮化矽層 222 與第一氧化矽層 220 進行一第一蝕刻製程，暴露出條狀結構 232 之間極導電層 208 與位於條狀結構 232 間之半導體基底 200，留下位於條狀結構 232 側壁的第一氧化矽層 220 與第一氮化矽層 222。

如第 19 圖所示，接著可對第一氮化矽層 222 進行一氧化製程，以使第一氮化矽層 222 的外表面氧化形成一第二氧化矽層 224。其後，再利用一氮化製程，或是利用一沉積製程與一蝕刻製程，於各第二氧化矽層 224 外再形成一層第二氮化矽層 242，藉此於各條狀結構 232 之相對二側壁表面形成分別一具有 I 形結構的電荷擷取側壁子 312。需注意的是，本發明之電荷擷取側壁子 312 可暴露出各條狀結構 232 之間極導電層 208 的上表面，以使間極導電層 208 得以電連接後續形成的字元線。

於其他實施例中，本發明亦可於半導體基底 200 上全面沉積一第二氧化矽層(圖未示)，覆蓋於第一氮化矽層 222 表面，再於半導體基底 200 上全面沉積一第二氮化矽層(圖未示)，覆蓋於第二氧化矽層表面。之後，對第二氮化矽層與第二氧化矽層進行一第二蝕刻製程，暴露出條狀結構 232 之間極導電層 208 與位於條狀結構 232 間之半導體基底 200，留下位於第一氮化矽層 222 表面的第二氧化矽層 224 與位於第二氧化矽層 224 表面第二氮化矽層 242，

藉此形成電荷擷取側壁子 312。

另外，本發明之電荷擷取側壁子也可以具有 L 形結構。請參考第 20 圖至第 21 圖，其繪示的是本發明第五較佳實施例製作電荷擷取側壁子之方法示意圖，其中相同的元件或部位沿用相同的符號來表示。如第 20 圖所示，首先提供一半導體基底 200，半導體基底 200 中包含有至少一 P 型摻雜井 202，且半導體基底 200 上包含有複數個條狀結構 232。各條狀結構 232 由下至上依序包含有一閘極介電層 206 與一閘極導電層 208。接著，於半導體基底 200 與條狀結構 232 之表面依序沉積一第一氧化矽層 220、一第一氮化矽層 222、一第二氧化矽層 224 與一第二氮化矽層 242。

接著如第 21 圖所示，對第二氮化矽層 242、第二氧化矽層 224、第一氮化矽層 222 與第一氧化矽層 220 進行一蝕刻製程，暴露出條狀結構 232 之閘極導電層 208 與位於條狀結構 232 間之半導體基底 200，並留下位於條狀結構 232 相對二側壁之第一氧化矽層 220、第一氮化矽層 222、第二氧化矽層 224 與第二氮化矽層 242，藉此形成一具有 L 形結構的電荷擷取側壁子 412。其中，電荷擷取側壁子 412 可暴露出各條狀結構 232 之閘極導電層 208 的上表面，以使閘極導電層 208 得以電連接後續形成的字元線。

由上述可知，本發明製作記憶體之方法，可直接利用於閘極製作過程中所形成之條狀結構與電荷擷取側壁子作為佈植遮罩來

進行一自對準之離子佈植製程，以形成記憶體所需之 N 型摻雜區 (亦為記憶體之源極/汲極與埋入式位元線)。再者，本發明之選擇閘極可直接與字元線電連接，無須再另行製作選擇閘極與字元線之間的連線結構，因此不但有效地縮小了記憶體的佈局面積，也可以有效地簡化記憶體之製作過程。此外，根據本發明所製作出之記憶體結構，記憶體的操作過程也會更為簡易。如此一來，不但可以提高積體電路的積集度，更可以增加產品的良率與運作效能。

以上所述僅為本發明之較佳實施例，凡依本發明申請專利範圍所做之均等變化與修飾，皆應屬本發明之涵蓋範圍。

【圖式簡單說明】

第 1 圖為習知 SPVG SONOS 型記憶體進行編程操作時之示意圖。

第 2 圖為習知 SPVG SONOS 型記憶體進行抹除操作時之示意圖。

第 3 圖至第 7 圖為一傳統製作 SPVG SONOS 型記憶體之方法示意圖。

第 8 圖至第 15 圖為本發明第一較佳實施例製作 SPVG SONOS 型記憶體之方法示意圖。

第 16 圖繪示的是本發明第二較佳實施例 SPVG SONOS 型記憶體之立體示意圖。

第 17 圖繪示的是本發明第三較佳實施例 SPVG SONOS 型記憶體之立體示意圖。

第 18 圖至第 19 圖繪示的是本發明第四較佳實施例製作電荷擷取側壁子之方法示意圖。

第 20 圖至第 21 圖繪示的是本發明第五較佳實施例製作電荷擷取側壁子之方法示意圖。

【主要元件符號說明】

10	SPVG SONOS 型記憶體	12	P 型摻雜井
14	選擇閘極	16	汲極
18	源極	20	閘極絕緣層
22	頂蓋層	24	底氧化矽層
26	氮化矽層	28	頂氧化矽層
30	字元線	100	半導體基底
102	P 型摻雜井	104	選擇閘極結構
106	閘極絕緣層	108	選擇閘極
110	頂蓋層	112	犧牲側壁子結構
114	開口	116	N 型摻雜區
118	複合介電層	120	底氧化矽層
122	氮化矽層	124	頂氧化矽層
126	字元線	200	半導體基底
202	P 型摻雜井	204	選擇閘極結構
206	閘極介電層	208	閘極導電層
212	電荷擷取側壁子	216	N 型摻雜區
220	第一氧化矽層	222	第一氮化矽層

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224 第二氧化矽層

234 閘極間介電層

240 字元線

244 圖案化遮罩

412 電荷擷取側壁子

232 條狀結構

236 導電層

242 第二氮化矽層

312 電荷擷取側壁子

十、申請專利範圍：

1. 一種具有分離式電荷擷取側壁子之記憶體，其包含有：

一半導體基底，包含有至少一位於該半導體基底表面之第一導電型式摻雜井與複數個位於該第一導電型式摻雜井中之第二導電型式摻雜區；

複數個不相接觸之選擇閘極結構，該等選擇閘極結構位於該等第二導電型式摻雜區之間，排列成至少一行，各該選擇閘極結構包含有一設置於該第一導電型式摻雜井上之閘極介電層與一設置於該閘極介電層上之閘極導電層；
複數個電荷擷取側壁子，位於該等選擇閘極結構之相對二側壁；以及

複數條字元線，直接接觸該等閘極導電層之上表面。

2. 如申請專利範圍第 1 項所述之記憶體，其中二該電荷擷取側壁子係分別沿著該等選擇閘極結構所排列出之該行的相對二側而延伸，並且接觸各該選擇閘極結構之對應側壁。

3. 如申請專利範圍第 1 項所述之記憶體，其中各該選擇閘極結構與二該電荷擷取側壁子接觸，且位於該等選擇閘極結構之側壁的該等電荷擷取側壁子彼此不相接觸。

4. 如申請專利範圍第 1 項所述之記憶體，其中各該電荷擷取側壁子係為一氧化矽-氮化矽-氧化矽(ONO)複合結構。

5. 如申請專利範圍第 1 項所述之記憶體，其中各該電荷擷取側壁子係為一氧化矽-氮化矽-氧化矽-氮化矽(ONON)複合結構。
6. 如申請專利範圍第 1 項所述之記憶體，其中各該電荷擷取側壁子包含有一 I 形結構。
7. 如申請專利範圍第 1 項所述之記憶體，其中各該電荷擷取側壁子包含有一 L 形結構。
8. 如申請專利範圍第 1 項所述之記憶體，其中該等第二導電型式摻雜區係為複數條埋入式位元線。
9. 如申請專利範圍第 1 項所述之記憶體，另包含有一閘極間介電層，位於該等電荷擷取側壁子外側，並覆蓋於該等第二導電型式摻雜區表面。
10. 如申請專利範圍第 1 項所述之記憶體，其中該第一導電型式摻雜井係為 P 型摻雜井，且該等第二導電型式摻雜區係為 N 型摻雜區。
11. 一種製作具有分離式電荷擷取側壁子之記憶體之方法，其包含有：
提供一半導體基底，其包含有至少一位於該半導體基底中的

第一導電型式摻雜井；

於該第一導電型式摻雜井表面形成複數個不相接觸之條狀結構，各該條狀結構包含有一設置於該第一導電型式摻雜井上之閘極介電層與一設置於該閘極介電層上之閘極導電層；

於各該條狀結構之相對二側壁表面形成分別一電荷擷取側壁子；

進行一離子佈植製程，利用該等條狀結構以及該等電荷擷取側壁子作為遮罩，於各該條狀結構間之該第一導電型式摻雜井中分別形成一第二導電型式摻雜區；

於該等第二導電型式摻雜區上形成一閘極間介電層；

於該半導體基底上全面形成一導電層，並直接接觸該等閘極導電層表面；以及

蝕刻該導電層與該等條狀結構，使該導電層成為複數個不相接觸且與各該第二導電型式摻雜區正交之字元線，並使各該條狀結構成為複數個選擇閘極結構。

12. 如申請專利範圍第 11 項所述之方法，其中蝕刻該導電層與該等條狀結構之該步驟包含有：

於該導電層上形成一遮罩，該遮罩具有複數個不相接觸之條狀開口，且各該條狀開口與該等條狀結構正交；以及
以該遮罩作為蝕刻遮罩，對該導電層與該等條狀結構進行一蝕刻製程，直到該條狀結構成為該等選擇閘極結構。

13. 如申請專利範圍第 12 項所述之方法，其中該蝕刻製程去除該導電層未被該遮罩所遮蔽之部分，以及該等條狀結構未被該遮罩所遮蔽之部分，而留下部分未被該遮罩所遮蔽之該等電荷擷取側壁子。

14. 如申請專利範圍第 11 項所述之方法，其中形成該等電荷擷取側壁子之該步驟包含有：

於該半導體基底上全面形成一第一氧化矽層，覆蓋於該等條狀結構之側壁；

於該半導體基底上全面形成一第一氮化矽層，覆蓋於該第一氧化矽層表面；

蝕刻該第一氮化矽層與該第一氧化矽層，暴露出該等條狀結構之該等閘極導電層與位於該等條狀結構間之該半導體基底，留下位於該條狀結構側壁的該第一氧化矽層與該第一氮化矽層；以及

形成一第二氧化矽層，覆蓋於該第一氮化矽層表面，並暴露出該等條狀結構之該等閘極導電層與位於該等條狀結構間之該半導體基底。

15. 如申請專利範圍第 14 項所述之方法，其中於形成該第二氧化矽層之後另包含有：

形成一第二氮化矽層，覆蓋於該第二氧化矽層表面，並暴露

出該等條狀結構之該等閘極導電層與位於該等條狀結構間之該半導體基底。

16. 如申請專利範圍第 11 項所述之方法，其中各該電荷擷取側壁子包含有一 I 形結構。

17. 如申請專利範圍第 11 項所述之方法，其中各該電荷擷取側壁子包含有一 L 形結構。

18. 如申請專利範圍第 11 項所述之方法，其中形成該閘極間介電層之該步驟包含有：

於該半導體基底上全面形成一介電層，覆蓋於該等條狀結構上並填充於該等條狀結構之間；以及
對該介電層進行一平坦化製程，直到暴露出該條狀結構。

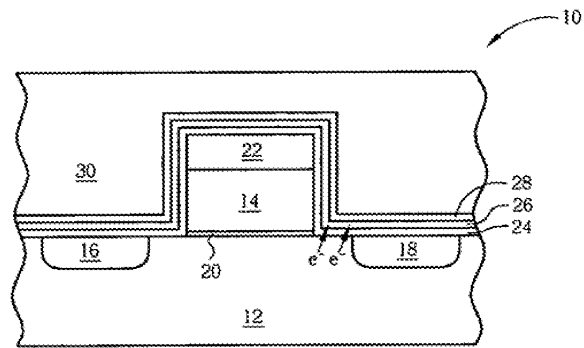
19. 如申請專利範圍第 11 項所述之方法，其中該等第二導電型式摻雜區係為埋入式位元線。

20. 如申請專利範圍第 11 項所述之方法，其中該記憶體係為一分離編程虛擬接地 SONOS 型(split program virtual ground SONOS)記憶體。

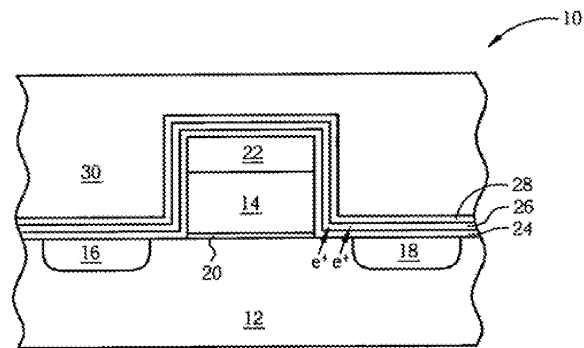
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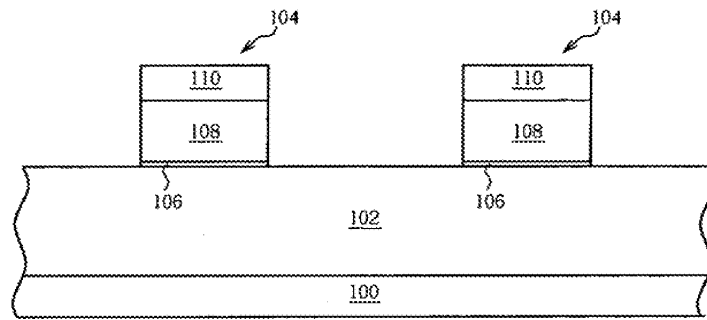




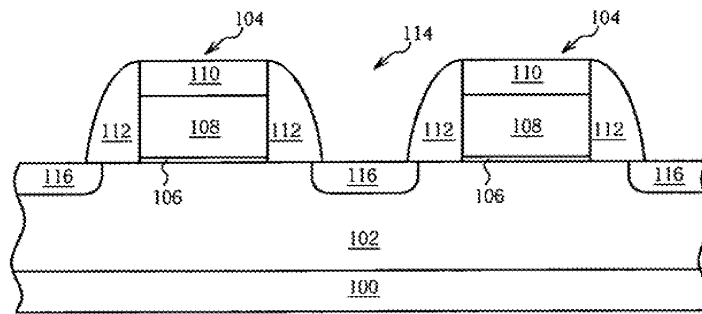
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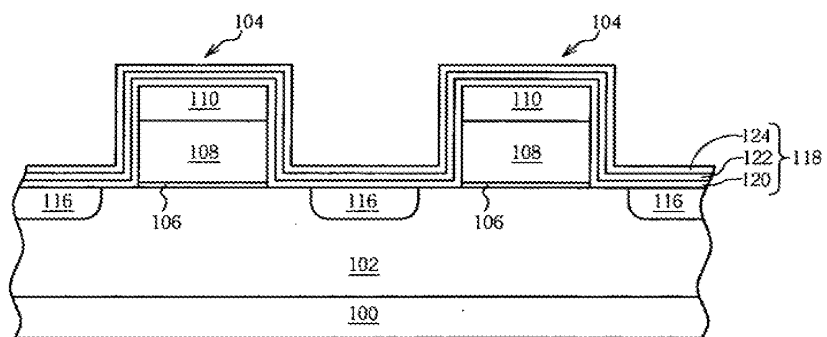
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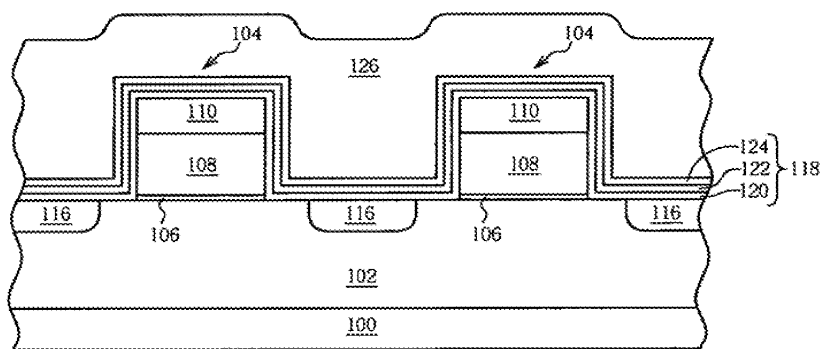
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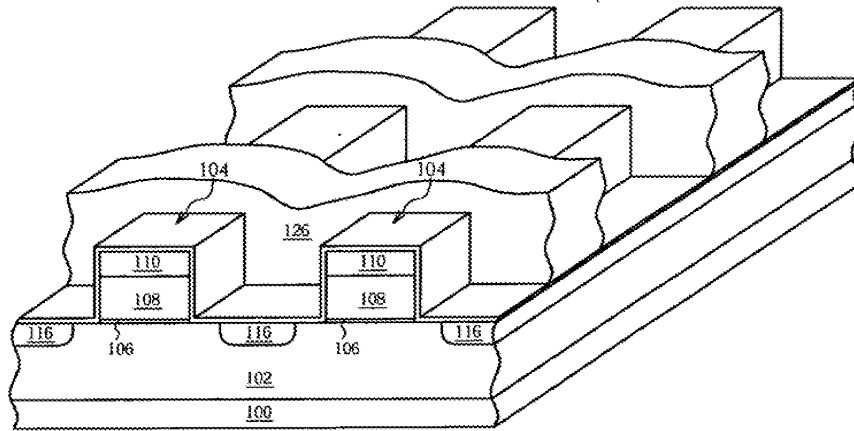
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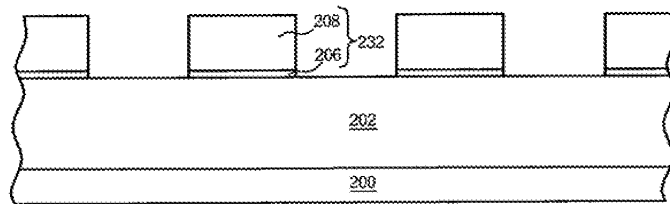
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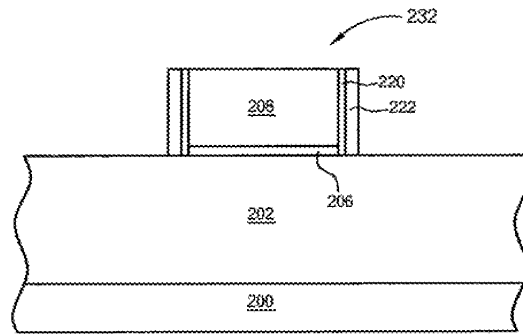
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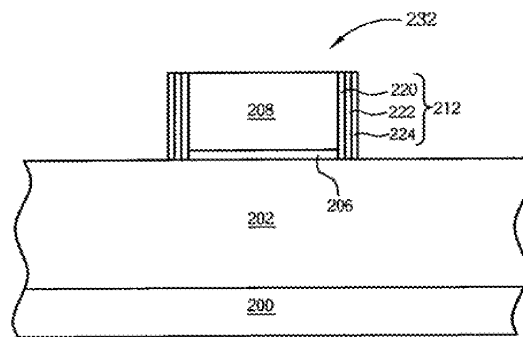
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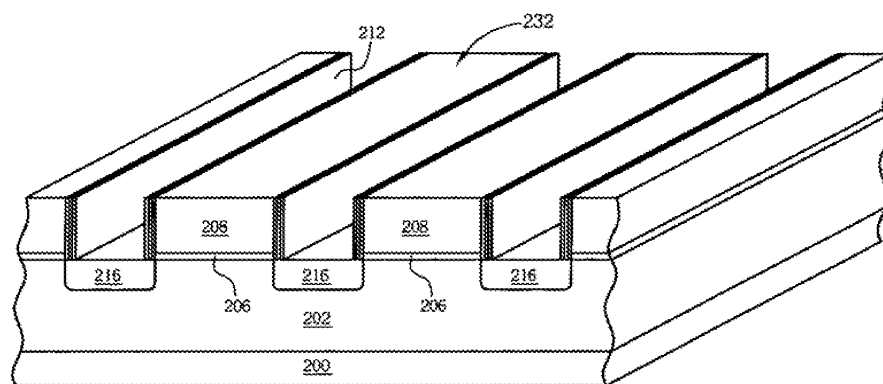
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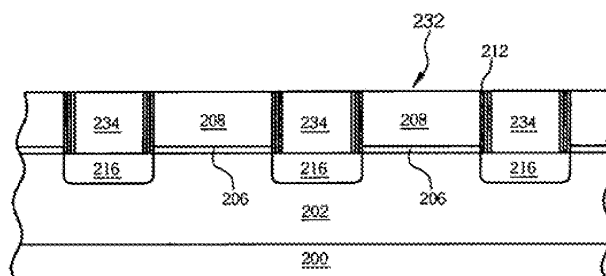
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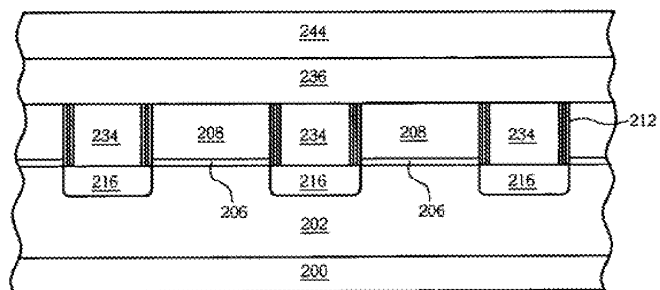
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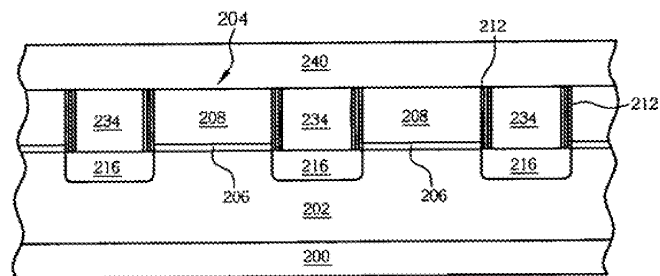
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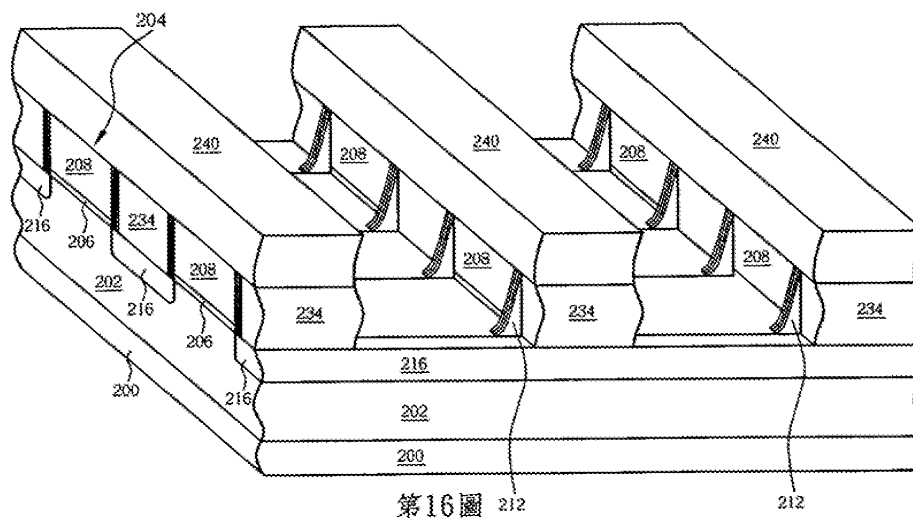
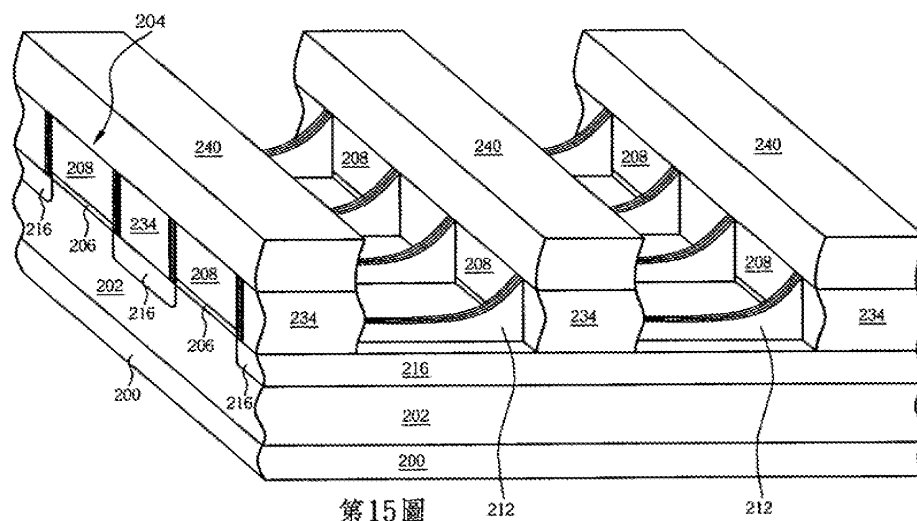
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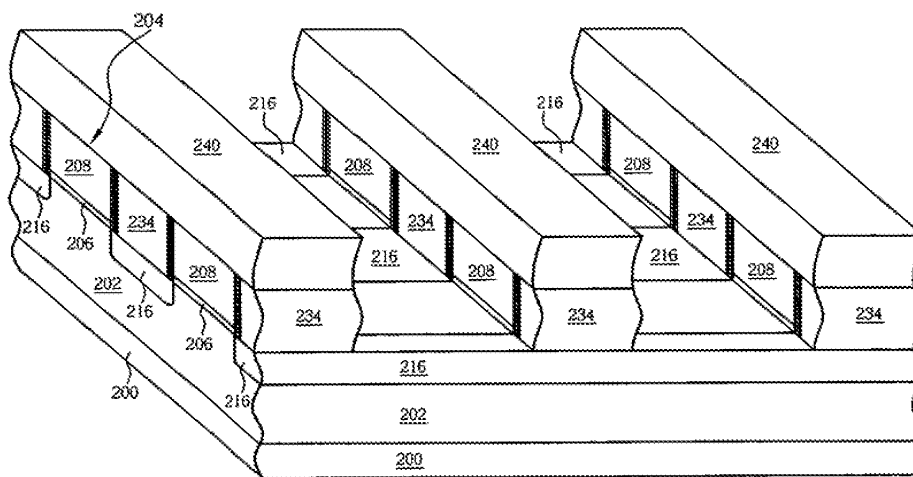


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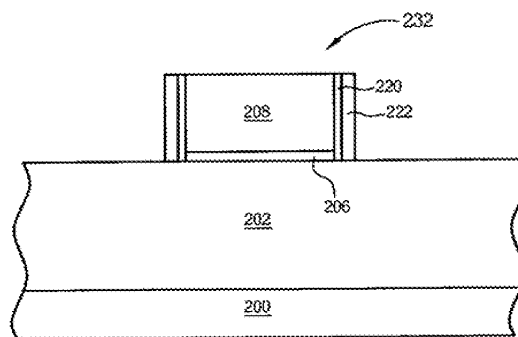


第14圖

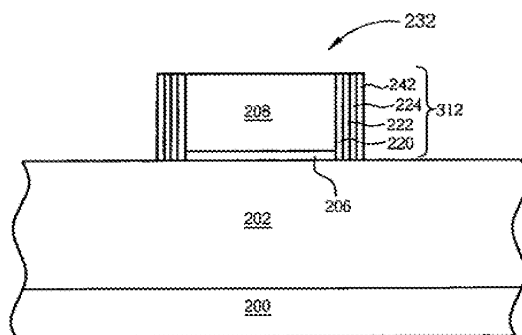




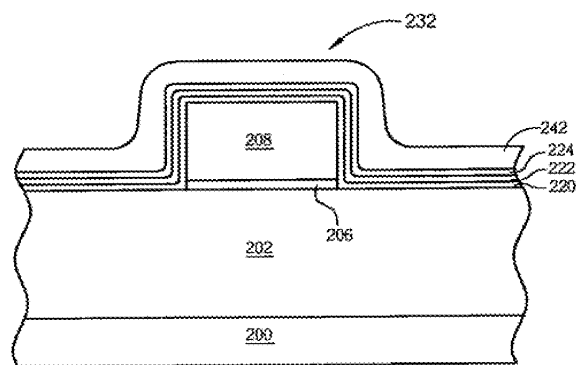
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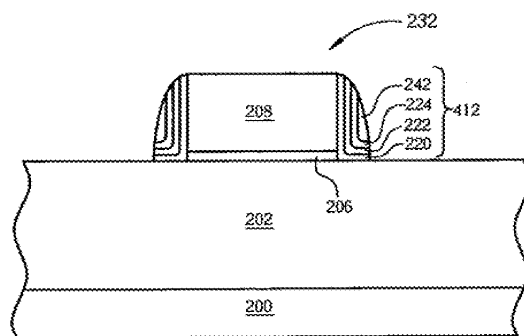
第18圖



第19圖



第20圖



第21圖

Electronic Acknowledgement Receipt	
EFS ID:	21083050
Application Number:	14331229
International Application Number:	
Confirmation Number:	8157
Title of Invention:	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR
First Named Inventor/Applicant Name:	Ming-Te Wei
Customer Number:	27765
Filer:	Winston Hsu/Connie Chen
Filer Authorized By:	Winston Hsu
Attorney Docket Number:	NAUP1220USA1
Receipt Date:	31-DEC-2014
Filing Date:	15-JUL-2014
Time Stamp:	04:12:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2143884.PDF	28998 ec29a7c479e370089cb54b3c893cf7ed7f2cd2ce	no	3

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/331,229	07/15/2014	Ming-Te Wei	NAUP1220USA1

CONFIRMATION NO. 8157

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

PUBLICATION NOTICE



OC000000071614884

Title:METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

Publication No.US-2014-0322883-A1

Publication Date:10/30/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/331,229				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(i))	10	minus 20 = *				x 80 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE				TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE				TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
14/331,229	07/15/2014	2812	1600	NAU1220USA1	10	1

CONFIRMATION NO. 8157

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

FILING RECEIPT



OC000000069814631

Date Mailed: 07/25/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

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Po-Chao Tsao, New Taipei City, TAIWAN;

Applicant(s)

UNITED MICROELECTRONICS CORP., Hsin-Chu City, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 27765

Domestic Priority data as claimed by applicant

This application is a DIV of 12/837,475 07/15/2010

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 07/24/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/331,229**

Projected Publication Date: 10/30/2014

Non-Publication Request: No

Early Publication Request: No

Title

METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ming-Te Wei
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1220USA1

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code	Issue Date	Name	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7176522	B2	2007-02-13	Cheng	
	2	7482656	B2	2009-01-27	Luo	
	3	7611938	B2	2009-11-03	Cheng	
	4	7745847	B2	2010-06-29	Tseng	
	5	7767534	B2	2010-08-03	Yang	
	6	8076194	B2	2011-12-13	Tseng	
	7	8076209	B2	2011-12-13	Yang	
	8	8227890	B2	2012-07-24	Lin	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ming-Te Wei
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1220USA1

	9	5885761		1999-03-23	Duane	
	10	6043116	A	2000-03-28	Kuo	
	11	6133151	A	2000-10-17	Lin	
	12	6153457	A	2000-11-28	Kuo	
	13	7183156	B2	2007-02-27	Goldbach	
	14	7498264	B2	2009-03-03	Mehard	
	15	7670914	B2	2010-03-02	Krivokapic	
	16	7812399	B2	2010-10-12	Yuda	
	17	7678690	B2	2010-03-16	Richter	
	18	6121080		2000-09-19	Wu	
	19	6534414		2003-03-18	Wang	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ming-Te Wei
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1220USA1

	20	6846618		2005-01-25	Hsu	
	21	7709275	B2	2010-05-04	Yang	

U.S.PATENT APPLICATION PUBLICATIONS						
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Examiner Initial*	Cite No	Publication Number	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20050112817	A1	2005-05-26	Cheng	
	2	20060046407	A1	2006-03-02	Juengling	
	3	20060258109	A1	2006-11-16	Juengling	
	4	20070128786	A1	2007-06-07	Cheng	
	5	20070202653	A1	2007-08-30	Hoentschel	
	6	20070278591	A1	2007-12-06	Luo	
	7	20080048217	A1	2008-02-28	Kim	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ming-Te Wei
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1220USA1

	8	20080224212	A1	2008-09-18	LEE	
	9	20090186475	A1	2009-07-23	Ting	
	10	20100081245	A1	2010-04-01	YANG	
	11	20100109045	A1	2010-05-06	Liu	
	12	20100210084	A1	2010-08-19	YANG	
	13	20100227445	A1	2010-09-09	Tseng	
	14	20110147853	A1	2011-06-23	Lin	
	15	20110230027	A1	2011-09-22	Kim	
	16	20120012904	A1	2012-01-19	Wei	
	17	20120043614	A1	2012-02-23	Choi	
	18	20120045873	A1	2012-02-23	Jeong	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ming-Te Wei
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1220USA1

	19	20120045880	A1	2012-02-23	Ma	
	20	20120056245	A1	2012-03-08	Kang	
	21	20120104514	A1	2012-05-03	Park	
	22	20120181625	A1	2012-07-19	KWOK	
	23	20020061625	A1	2002-05-23	Wang	
	24	20020137296	A1	2002-09-26	Satoh	
	25	20020140020	A1	2002-10-03	Wu	
	26	20050030697	A1	2005-02-10	Wu	
	27	20050116293	A1	2005-06-02	Goldbach	
	28	20060105561	A1	2006-05-18	Huh	
	29	20060189080	A1	2006-08-24	Lee	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ming-Te Wei
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1220USA1

	30	20080090360	A1	2008-04-17	Krivokapic	
	31	20100012999	A1	2010-01-21	Park	

.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number	Country Code	Kind Code	Publication Date	Name	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	
	1							

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	
	1		

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	
	Filing Date	
	First Named Inventor	Ming-Te Wei
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP1220USA1

CERTIFICATION STATEMENT			
Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):			
☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).			
OR			
☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).			
☐ See attached certification statement.			
☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.			
☒ None			
SIGNATURE			
A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.			
Signature	/Winston Hsu/	Date (YYYY-MM-DD)	2014-07-13
Name/Print	Winston Hsu	Registration Number	41,526

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:



Practitioners associated with Customer Number:

27765

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number

Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:



The address associated with Customer Number:

27765

OR

☐	Firm or Individual Name	
	Address	
	City	
	Country	
	Telephone	Email

Assignee Name and Address:

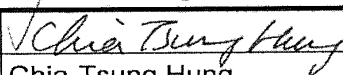
UNITED MICROELECTRONICS CORP.

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	SEP 26 2012
Name	Chia-Tsung Hung	Telephone	+886-3-5782258
Title	CHAIRMAN		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

NAU.0

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: UNITED MICROELECTRONICS CORP.

Application No./Patent No.: _____ Filed/Issue Date: _____

Titled: METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

UNITED MICROELECTRONICS CORP., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Winston Hsu/

Signature

Winston Hsu

Printed or Typed Name

07/13/2014

Date

41,526

Title or Registration Number

PATENT

Docket No NAUP1220USA

ASSIGNMENT OF INVENTION

In consideration of the payment by ASSIGNEE to ASSIGNOR of the sum of One Dollar (\$1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

ASSIGNOR(S) (Inventors):

Name: Ming-Te Wei Nationality: TW

Name: Wen-Chen Wu Nationality: TW

Name: Lung-En Kuo Nationality: TW

Name: Po-Chao Tsao Nationality: TW

Hereby sells, assigns and transfers to

ASSIGNEE(S):

Name: UNITED MICROELECTRONICS CORP.

Address: No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

and the successors and assignees of the ASSIGNEE the entire right, title, and interest in and to any and all improvements which are disclosed in the invention entitled:

"METAL-OXIDE SEMICONDUCTOR TRANSISTOR AND METHOD FOR FABRICATING
THE SAME"

Which is found in :

- (a) + U.S. patent application executed on even date
(b) _____ U.S. patent application executed on _____
(c) _____ U.S. application serial no. _____
(d) _____ patent no. _____ issued _____

NPO#NAU-P1220-USA:0
CUST#UMCD-2009-0375

Assignment, Page 1 of 2

F#NPO-P0002E-US1
DSC0-099U001865

PATENT

and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof

ASSIGNOR hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

ASSIGNOR further covenants that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to ASSIGNOR and will testify as to the same in any interference, litigation or proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.

IN WITNESS WHEREOF, We have hereunto set hand and seal this JUL 08 2010 (Date of signing). (請發明人務必簽署上列日期。)

(Type name of inventor)

Signature of INVENTOR

Ming-Te Wei

Ming-Te, Wei

Wen-Chen Wu

Lung-En Kuo

Lung-En Kuo

Po-Chao Tsao

Po Chao Tsao

PATENT

Docket No NAUP1220USA

ASSIGNMENT OF INVENTION

In consideration of the payment by ASSIGNEE to ASSIGNOR of the sum of One Dollar (\$1.00), the receipt of which is hereby acknowledged, and for other good and valuable consideration.

ASSIGNOR(S) (Inventors):

Name: Ming-Te Wei Nationality: TW

Name: Wen-Chen Wu Nationality: TW

Name: Lung-En Kuo Nationality: TW

Name: Po-Chao Tsao Nationality: TW

Hereby sells, assigns and transfers to

ASSIGNEE(S):

Name: UNITED MICROELECTRONICS CORP.

Address: No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City 300, Taiwan, R.O.C.

and the successors and assignees of the ASSIGNEE the entire right, title, and interest in and to any and all improvements which are disclosed in the invention entitled:

"METAL-OXIDE SEMICONDUCTOR TRANSISTOR AND METHOD FOR FABRICATING
THE SAME"

Which is found in :

- (a) + U.S. patent application executed on even date
(b) _____ U.S. patent application executed on _____
(c) _____ U.S. application serial no. _____
(d) _____ patent no. _____ issued _____

NPO#NAU-P1220-USA:0
CUST#UMCD-2009-0375

Assignment, Page 1 of 2

F#NPO-P0002E-US1
DSC0-099U001865

PATENT

and, in and to, all Letters Patent to be obtained for said invention by the above application or any continuations, continuation-in-part, divisions, renewals, substitutes, or extensions thereof, and as to Letters Patent any reissue or re-examination thereof

ASSIGNOR hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment;

ASSIGNOR further covenants that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said invention and said Letters Patent and legal equivalents as may be known and accessible to ASSIGNOR and will testify as to the same in any interference, litigation or proceeding related thereto and will promptly execute and deliver to ASSIGNEE or its legal representatives any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said invention and said Letters Patent and said equivalents thereof which may be necessary or desirable to carry out the proposes thereof.

IN WITNESS WHEREOF, We have hereunto set hand and seal this JUL 08 2010 (Date of signing). (請發明人務必簽署上列日期。)

(Type name of inventor)

Signature of INVENTOR

Ming-Te Wei

Wen-Chen Wu

Lung-En Kuo

Po-Chao Tsao

吳文成 (Wen-Chen Wu)

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identify theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR Inventor: <u>Ming-Te Wei</u> Date (Optional): <u>JUL 07 2014</u> Signature: <u>Ming-Te Wei</u>	
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 116 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR Inventor: <u>Lung-En Kuo</u> Date (Optional): <u>JUL 07 2014</u> Signature: <u>Lung-En Kuo</u>	
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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
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Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____ The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: <u>Po-Chao Tsao</u> Date (Optional): <u>JUL 07 2014</u> Signature: <u>Po-Chao Tsao</u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.	

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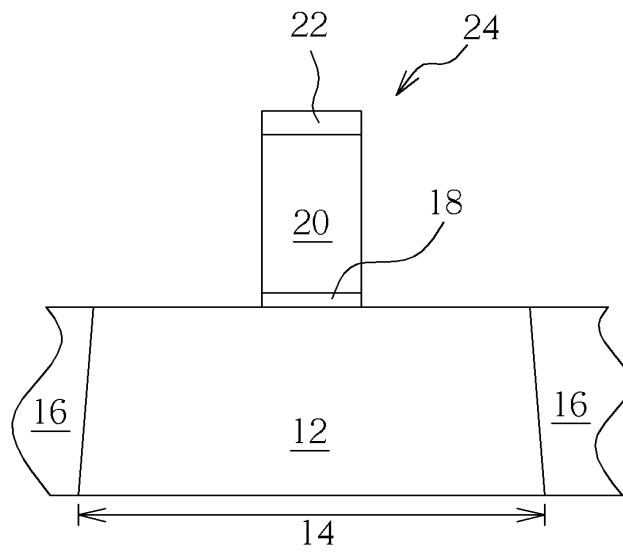


FIG. 1



FIG. 2

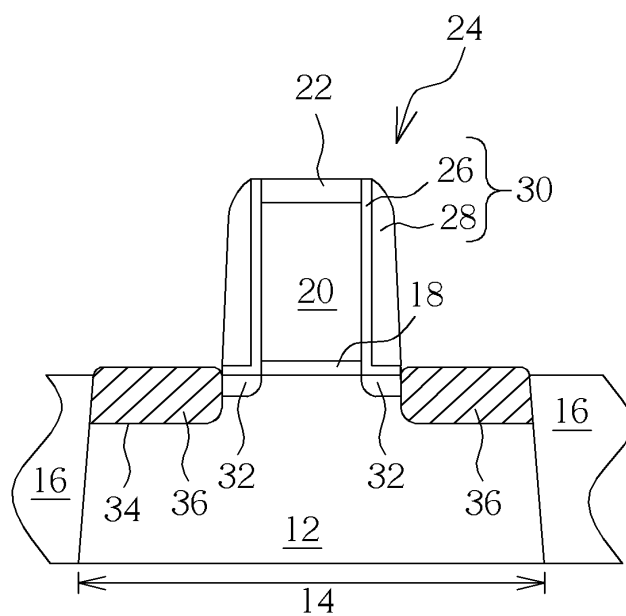


FIG. 3

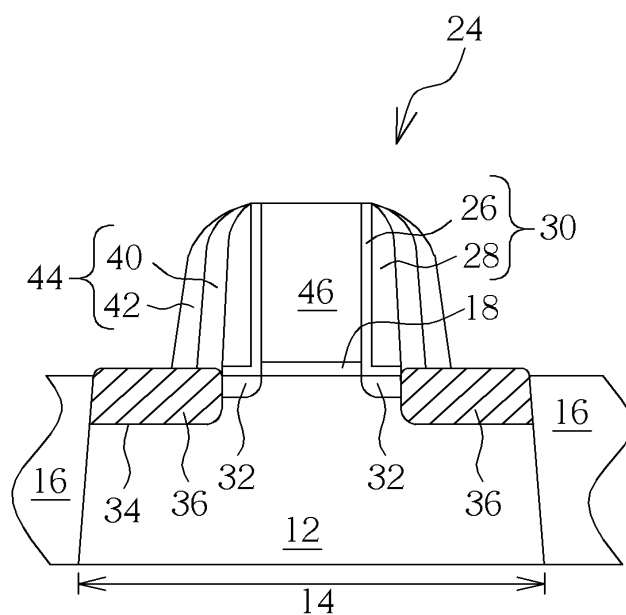


FIG. 4

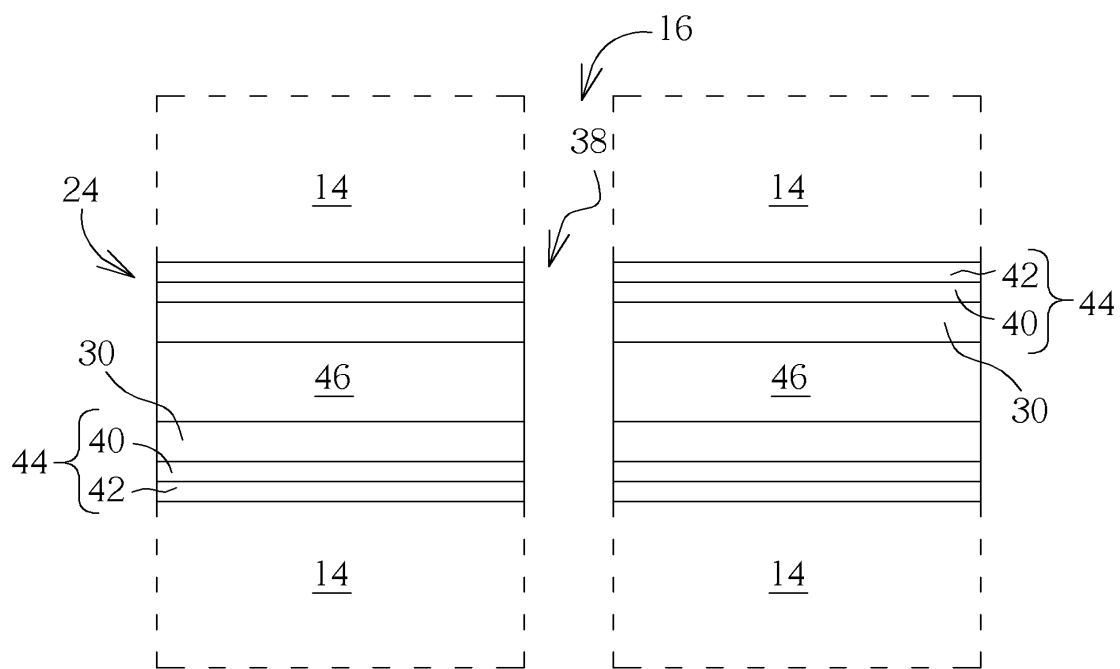


FIG. 5

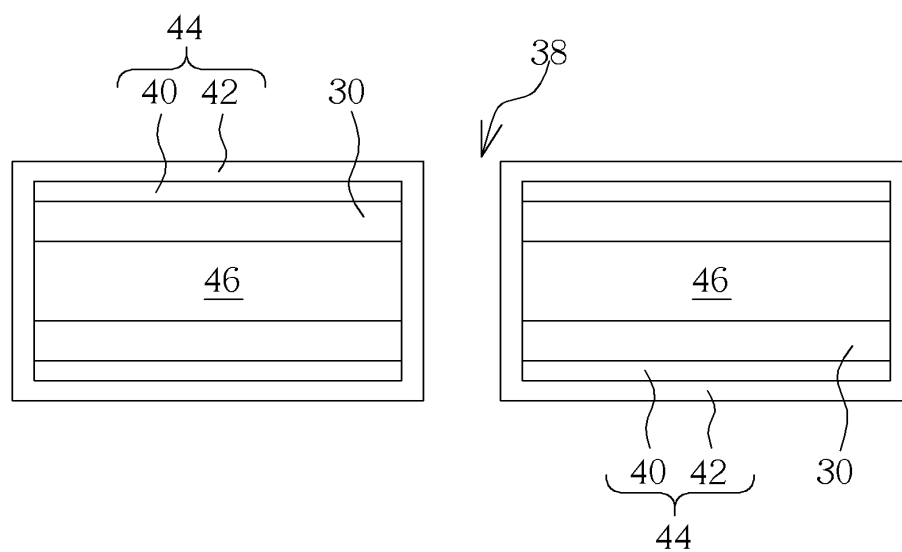


FIG. 6

Abstract of Disclosure

A method for fabricating a metal-oxide semiconductor (MOS) transistor is disclosed. The method includes the steps of: providing a semiconductor substrate; forming a silicon layer on the semiconductor substrate; performing a first photo-etching process on the silicon layer for forming a gate pattern; forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

Claims

What is claimed is:

1. A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:

- providing a semiconductor substrate;
- forming a silicon layer on the semiconductor substrate;
- performing a first photo-etching process on the silicon layer for forming a gate pattern;
- forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and
- after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

2. The method of claim 1, wherein after forming the silicon layer comprises:

- forming a hard mask on the silicon layer;
- performing the first photo-etching process on the hard mask and the silicon layer for forming the gate pattern;
- forming a first spacer around the gate pattern;
- forming a lightly doped drain in the semiconductor substrate adjacent to two sides of the gate pattern;
- forming at least a recess in the semiconductor substrate adjacent to two sides of the first spacer;
- forming the epitaxial layer in the recess;
- removing the hard mask disposed on the silicon layer;
- forming a first dielectric layer on the semiconductor substrate while covering the gate pattern;
- performing the second photo-etching process on the gate pattern, the first spacer, and the first dielectric layer to form the slot in the gate pattern; and
- removing a portion of the first dielectric layer for forming a second spacer.

3. The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.

4. The method of claim 1, wherein the hard mask comprises silicon nitride.

5. The method of claim 2, wherein the step of forming the first spacer comprises:

forming a silicon oxide layer and a silicon nitride layer on the semiconductor substrate; and

etching back the silicon oxide layer and the silicon nitride layer for forming the first spacer.

6. The method of claim 2, wherein the first dielectric layer comprises a silicon oxide layer and a silicon nitride layer.

7. The method of claim 2, wherein after performing the second photo-etching process comprises:

forming a second dielectric layer on the semiconductor substrate; and

removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.

8. The method of claim 7, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

9. The method of claim 2, wherein after forming the second spacer comprises:

forming a second dielectric layer on the semiconductor substrate; and

removing a portion of the second dielectric layer for forming a third spacer.

10. The method of claim 9, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

Title

METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR

Cross Reference To Related Applications

[0001] This application is a division of U.S. application Ser. No. 12/837,475 filed July 15, 2010, and incorporated herein by reference in its entirety.

Background of the Invention

1. Field of the Invention

[0002] The invention relates to a method for fabricating MOS transistor, and more particularly, to a method of defining polysilicon slot before formation of epitaxial layer.

2. Description of the Prior Art

[0003] In the field of semiconductor fabrication, the use of polysilicon material is diverse. Having a strong resistance for heat, polysilicon materials are commonly used to fabricate gate electrodes for metal-oxide semiconductor transistors. The gate pattern fabricated by polysilicon materials is also used to form self-aligned source/drain regions as polysilicon readily blocks ions from entering the channel region.

[0004] As the dimension of semiconductor devices decreases, the fabrication of transistors also improves substantially for fabricating small size and high quality transistors. Conventional approach of fabricating the gate of metal-oxide semiconductor (MOS) transistors typically forms a polysilicon layer on a semiconductor substrate and a hard mask on the polysilicon layer before using two photo-etching processes (PEP) to pattern the polysilicon layer and the hard mask into a gate of the transistor. Preferably, the first photo-etching process is conducted to pattern the hard mask and the polysilicon layer into a plurality of rectangular polysilicon gate pattern as the second photo-etching process forms a polysilicon slot in each of the rectangular gate pattern for separating each gate pattern into two gates. Thereafter, elements including spacers are

formed on the sidewall of the gate and lightly doped drains and epitaxial layer are formed in the semiconductor substrate adjacent to two sides of the spacer.

[0005] However, as the polysilicon slot is preferably formed before the formation of epitaxial layer, the etching ratio involved during the formation of the polysilicon slot typically affects the process thereafter. For instance, if the etching ratio of the second photo-etching process is low, the gate pattern would not be etched through completely to form the polysilicon slot and phenomenon such as polysilicon residue and line end bridge would result, whereas if the etching ratio of the second photo-etching process is high, the hard mask disposed on top of the polysilicon gate pattern would be consumed, which would further induce consumption of the spacer formed on the sidewall of the gate thereafter. As some of the spacer on the sidewall is consumed away, a portion of the gate is exposed and un-wanted epitaxial layer would be formed on the exposed portion of the gate.

Summary of the Invention

[0006] It is an objective of the present invention to provide a method for fabricating a MOS transistor for resolving the aforementioned issue caused by conventional approach.

[0007] According to a preferred embodiment of the present invention, a method for fabricating a metal-oxide semiconductor (MOS) transistor is disclosed. The method includes the steps of: providing a semiconductor substrate; forming a silicon layer on the semiconductor substrate; performing a first photo-etching process on the silicon layer for forming a gate pattern; forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

[0008] According to another aspect of the present invention, a metal-oxide semiconductor (MOS) transistor is disclosed. The MOS transistor includes: a semiconductor substrate; a gate disposed on the semiconductor substrate, wherein the gate comprises four sidewalls, and two of the four sidewalls opposite to each other comprise a spacer thereon while the other two sidewalls opposite to each other comprise no spacer; and an epitaxial layer disposed in the semiconductor substrate adjacent to two sides of the spacer.

[0009] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0010] Figs. 1-6 illustrate a method for fabricating a MOS transistor according to a preferred embodiment of the present invention.

Detailed Description

[0011] Referring to Figs. 1-6, Figs. 1-6 illustrate a method for fabricating a MOS transistor according to a preferred embodiment of the present invention. As shown in Fig. 1, a semiconductor substrate 12, such as a silicon substrate or a silicon-on-insulator (SOI) substrate is provided. At least an active region 14 is defined on the semiconductor substrate 12 and a plurality of shallow trench isolations (STI) 16 are formed for separating the active region 14 from adjacent regions or devices.

[0012] A gate insulating layer (not shown) composed of dielectric material such as oxides or nitrides is deposited on surface of the semiconductor substrate 12, and a polysilicon layer preferably with a depth of approximately 1000 Angstroms and a hard mask are formed sequentially on the gate insulating layer thereafter. In this embodiment, the hard mask could be selected from a material consisting of SiO₂, silicon nitride, and SiON, and the polysilicon layer could

be composed of undoped polysilicon material or polysilicon with N⁺ dopants, which are all within the scope of the present invention.

[0013] Next, a photo-etching process is performed on the hard mask and the polysilicon layer by first forming a patterned photoresist (not shown) on the hard mask and then using the photoresist as mask to carry out a patterning process. The patterning process preferably removes a portion of the hard mask, the polysilicon layer and the gate insulating layer through a single or multiple etching to form a gate pattern 24 composed of patterned gate insulating layer 18, patterned polysilicon layer 20, and patterned hard mask 22 in the active region 14. The patterned photoresist is removed subsequent to the patterning process.

[0014] Next, as shown in Fig. 2, Fig. 2 illustrates a top view of the gate formed after the first photo-etching process. As shown in the figure, a plurality of rectangular gate patterns 24 are formed on the semiconductor substrate 12 after the aforementioned first photo-etching process, in which each gate pattern 24 is composed of a patterned gate insulating layer 18, a patterned gate polysilicon layer 20, and a patterned hard mask 22.

[0015] As shown in Fig. 3, a first stage spacer formation is conducted by first depositing a silicon oxide layer (not shown) and a silicon nitride layer (not shown) on the semiconductor substrate 12. An etching back is carried thereafter to remove a portion of the silicon oxide layer and silicon nitride layer to form a first spacer 30 composed of silicon oxide layer 26 and silicon nitride layer 28 on the sidewall of the gate pattern 24.

[0016] Next, a selective epitaxial growth (SEG) process is performed to form a strained silicon in the semiconductor substrate 12. For instance, a patterned photoresist (not shown) could be formed on the semiconductor substrate, and an etching process is conducted to form two recesses 34 in the semiconductor substrate 12 adjacent to two

sides of the gate pattern 24. A surface clean is carried out thereafter to completely remove native oxides or other impurities from the surface of the recesses 34. Next, a selective epitaxial growth process is performed to substantially fill the two recesses 34 for forming an epitaxial layer 36. Preferably, a light ion implantation could be conducted before the formation of the first spacer 30 and the epitaxial layer 36 to implant n-type or p-type dopants into the semiconductor substrate 12 adjacent to two sides of the gate pattern 24 for forming a lightly doped drain 32, and the material of the epitaxial layer 36 could be selected according to the type of the transistor or demand of the product.

[0017] For instance, if the transistor fabricated were to be a PMOS transistor, an epitaxial layer 36 composed of silicon germanium is preferably formed in the recesses 34 to provide a compressive strain to the channel region of the PMOS transistor thereby increasing the hole mobility of the transistor. Conversely, if the transistor fabricated were to be a NMOS transistor, an epitaxial layer composed of silicon carbide (SiC) is preferably formed in the recesses 34 to provide a tensile strain to the channel region of the NMOS transistor for increasing the electron mobility of the transistor.

[0018] Referring now to Figs. 4 and 5, Fig. 4 illustrates a cross-sectional view of the gate pattern after Fig. 3 and Fig. 5 illustrates a top view of the gate according to this embodiment. As shown in the figures, the hard mask 22 disposed on top of the polysilicon layer 20 is removed, and a spacer material layer, such as a silicon oxide layer (not shown) and a silicon nitride layer (not shown) are deposited sequentially on the semiconductor substrate 12. A photo-etching process is then carried out by first forming a patterned photoresist (not shown) on the polysilicon layer 20 and performing an etching process by using the patterned photoresist as mask to remove the polysilicon layer 20 on top of the shallow trench isolation 16, such as a part of the two ends and central portion of the polysilicon layer 20 for forming at least a polysilicon slot 38

in the rectangular gate pattern 24. The polysilicon slot 38 preferably separates the gate pattern 24 into two independent gates 46. After stripping the patterned photoresist and cleaning off remaining particles from the surface of the semiconductor substrate 12, an etching back is conducted on the deposited silicon oxide layer (not shown) and silicon nitride layer (not shown) for forming a second spacer 44 composed of silicon oxide layer 40 and silicon nitride layer 42 on the sidewall of the gate 46.

[0019] For simplification purpose, only one gate pattern 24 is revealed in Fig. 5 and other doping regions including lightly doped drain and epitaxial layers are also omitted. As shown in the figure, the polysilicon slot 38 preferably divides the gate pattern 24 into two independent portions, and as part of the silicon oxide layer 40 and silicon nitride layer 42 is removed for forming the polysilicon slot 38 and separating the gate pattern 24, no spacer is formed on at least two opposite sidewalls of the gate 46 after the separation. In other words, a second spacer 44 composed of silicon oxide layer 40 and silicon nitride layer 42 is formed on two opposite sidewalls of the polysilicon gate 46, whereas the other two remaining opposite sidewall contain no spacer.

[0020] Preferably, the polysilicon slot 38 is formed after the removal of the hard mask to facilitate a rework process conducted afterwards. For instance, a rework is typically carried out during a lithography for forming the polysilicon slot 38, and as the hard mask 22 is removed from the active region 14 of the semiconductor substrate 12 before rework is carried out, the exposed silicon substrate surface becomes unprotected. Unfortunately, reacting gas such as oxygen used to remove photoresist material during rework typically accumulates native oxides on the surface of the substrate or forms recesses on the substrate. Hence, the present embodiment preferably removes the hard mask 22 from the polysilicon layer 20 and then deposits the aforementioned silicon oxide and silicon nitride layer on the substrate 12. These deposited silicon oxide and silicon nitride

layer could not only be used as material layers for forming the second spacer, but also be used as etching mask for forming the polysilicon slot and protecting the active region.

[0021] In addition to forming the polysilicon slot after removing the hard mask, as addressed in the above embodiment, the polysilicon slot 38 could also be formed at any point after the epitaxial layer 36 is formed, which is within the scope of the present invention.

[0022] Moreover, the above embodiment of forming the second spacer preferably forms a silicon oxide layer and a silicon nitride layer before the etching back process, and then using one single etching back to simultaneously remove a portion of the silicon oxide layer and silicon nitride layer for forming the second spacer. However, the present invention could also deposit a single silicon oxide layer before the polysilicon slot is formed, and then deposit a silicon nitride layer after the formation of the polysilicon slot to form different MOS transistor structures.

[0023] For instance, a silicon oxide layer 40 could be deposited on the semiconductor substrate 12 after removing the hard mask, and after following the aforementioned step for forming the polysilicon slot 38, a silicon nitride layer 42 is deposited on the substrate 12, and a portion of the silicon oxide layer 40 and silicon nitride layer 42 are removed through etching back process to form the second spacer 44. As shown in Fig. 6, as part of the silicon oxide layer 40 is removed during the formation of the polysilicon slot 38, the silicon oxide layer 40 of the second spacer 44 would only be disposed on two opposite sidewall of the gate, and as the silicon nitride layer 42 of the second spacer 44 is deposited after the formation of the polysilicon slot 38, the silicon nitride layer 42 is preferably formed on four sidewalls of the gate 46.

[0024] According to another embodiment of the present invention, a silicon oxide layer 40 could be deposited on the semiconductor

substrate 12 after removing the hard mask, and after following the aforementioned approach for forming the polysilicon slot 38, an etching back is carried out to remove a portion of the silicon oxide layer 40 for forming a second spacer, and then depositing a silicon nitride layer 42 on the substrate 12, and then performing another etching back to remove part of the silicon nitride layer 42 for forming a third spacer. Despite the fabrication sequence of this embodiment is slightly different from the above approach, the same transistor structure as disclosed in Fig. 6 could be fabricated.

[0025] In contrast to the conventional approach of forming polysilicon slot before the epitaxial layer, the present invention uses a first photo-etching process to define a rectangular polysilicon gate pattern, forms an epitaxial layer adjacent to two sides of the gate pattern, and then uses a second photo-etching process to define the polysilicon slot while separating the gate pattern into two gates. As the definition of the polysilicon slot is carried after the formation of the epitaxial layer, issues such as line end bridge of epitaxial layer and growth of epitaxial layer on sidewall of the gate could be prevented substantially.

[0026] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		
First Named Inventor/Applicant Name:		Ming-Te Wei		
Filer:		Winston Hsu/Hitomi Lin		
Attorney Docket Number:		NAUP1220USA1		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
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Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

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EFS ID:	19564241
Application Number:	14331229
International Application Number:	
Confirmation Number:	8157
Title of Invention:	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR
First Named Inventor/Applicant Name:	Ming-Te Wei
Customer Number:	27765
Filer:	Winston Hsu/Kate Yeh
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Attorney Docket Number:	NAUP1220USA1
Receipt Date:	15-JUL-2014
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Time Stamp:	02:08:39
Application Type:	Utility under 35 USC 111(a)

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8	Claims	2002133.PDF	28947 87f79342fe3911dec60d8538ae53be281c9c1fc	no	3
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1220USA1
		Application Number	
Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Ming-Te		Wei		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Changhua County	Country of Residence i	TW		
Mailing Address of Inventor:					
Address 1		No.15, Ln. 97, Pinghe St., Xihu Township			
Address 2					
City	Changhua County	State/Province			
Postal Code		Country i	TW		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Wen-Chen		Wu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Kaohsiung City	Country of Residence i	TW		
Mailing Address of Inventor:					
Address 1		6F., No.60, Ln. 499, Xiuqun Rd., Nanzi Dist.			
Address 2					
City	Kaohsiung City	State/Province			
Postal Code		Country i	TW		
Inventor 3					Remove
Legal Name					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1220USA1
		Application Number	
Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Lung-En		Kuo	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Tainan City	Country of Residence i	TW	

Mailing Address of Inventor:

Address 1	No.22, Ln. 123, Dongqiao 2nd St., Yongkang Dist.			
Address 2				
City	Tainan City	State/Province		
Postal Code		Country i	TW	

Inventor 4	Remove
Legal Name	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Po-Chao		Tsao	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	New Taipei City	Country of Residence i	TW	

Mailing Address of Inventor:

Address 1	5F., No.61, Ln. 26, Zhongping Rd., Xinzhuang Dist.			
Address 2				
City	New Taipei City	State/Province		
Postal Code		Country i	TW	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.		Add
---	--	---------------------

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence information of this application.	
Customer Number	27765
Email Address	winstonhsu@naipo.com Add Email Remove Email

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1220USA1
		Application Number	
Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		

Application Information:

Title of the Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		
Attorney Docket Number	NAUP1220USA1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	3	Suggested Figure for Publication (if any)	

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	27765		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1220USA1
		Application Number	
Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the application number blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	12837475	2010-07-15
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1220USA1
		Application Number	
Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.		
Applicant 1		Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.		
Clear		
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
Name of the Deceased or Legally Incapacitated Inventor :		
If the Applicant is an Organization check here. ☒		
Organization Name	UNITED MICROELECTRONICS CORP.	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1220USA1
		Application Number	
Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		
Mailing Address Information:			
Address 1	No.3, Li-Hsin Road 2,		
Address 2	Science-Based Industrial Park		
City	Hsin-Chu City	State/Province	
Country ⁱ	TW	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
				Remove
If the Assignee or Non-Applicant Assignee is an Organization check here.				☐
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country ⁱ		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP1220USA1
		Application Number	
Title of Invention	METHOD FOR FABRICATING METAL-OXIDE SEMICONDUCTOR TRANSISTOR		

Signature:

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NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Winston Hsu/		Date (YYYY-MM-DD)	2014-07-13	
First Name	Winston	Last Name	Hsu	Registration Number	41526
Additional Signature may be generated within this form by selecting the Add button.				Add	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.