

Silicon Processing

for the VLSI Era

Volume 1 - Process Technology
Second Edition

S. Wolf and R.N. Tauber

**SILICON PROCESSING
FOR
THE VLSI ERA**

**VOLUME 1:
PROCESS TECHNOLOGY
Second Edition**

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**LATTICE PRESS
Sunset Beach, California**

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Published by:

LATTICE PRESS

Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, New Archetype Publishing, Los Angeles, CA.

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Library of Congress Cataloging in Publication Data

Wolf, Stanley and Tauber, Richard N.

Silicon Processing for the VLSI Era
Volume 1: Process Technology

Includes Index

1. Integrated circuits-Very large scale
integration. 2. Silicon. I. Title

ISBN 0-9616721-6-1

9 8 7 6 5 4 3 2 1

PRINTED IN THE UNITED STATES OF AMERICA

To my wife and life editor, Carrol Ann,
and to my children, Jennifer Laura and Stanley Charles Ross

Stanley Wolf

To my partner in life, Barbara

Richard N. Tauber

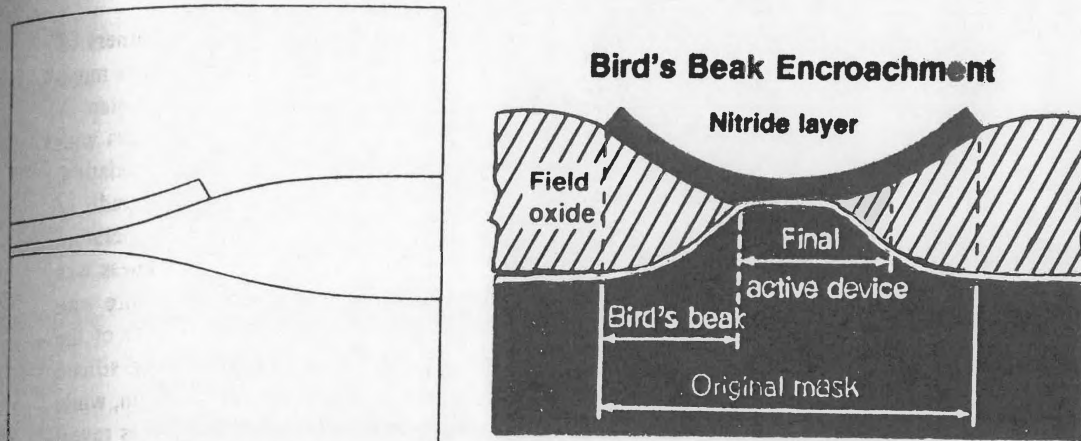


Fig. 8-23 Bird's beak encroachment limits the scaling of channel widths to about 1.5 μm .⁴⁴

There are numerous processing approaches to minimize the bird's beak, and some are described in Volumes 2 and 3 of this series.

HIPOX can be used to minimize bird's beak encroachment since vertical growth is more rapid than lateral growth during high pressure oxidation. As a result, the target field thickness can be reached with less lateral growth; accordingly resulting in a reduced bird's beak.

8.11.2 LOCOS-Induced Gate Oxide Thinning

In LOCOS processing the sequence of steps after growing the field oxide is stripping the protective nitride, growing and stripping a sacrificial oxide, and then growing the gate oxide. After the gate oxide is grown it is found that the edges of the gate can be substantially thinner than the center region. The oxidation in the gate region near the LOCOS edge is reduced by the presence of the thick oxide. The thick field oxide can limit the availability of oxidant in the region at the edge of the gate, resulting in gate oxide thinning. The use of HIPOX to minimize this effect is discussed below.

8.11.3 Trench Corner Rounding

There are two major applications of trench technology in modern devices. In both applications it is necessary to oxidize the inside and top of a trench etched into silicon. As a result, oxidation takes place along two different crystalline planes and two-dimensional effects must be considered. The first use of such trenches is in DRAM capacitors. In this application a deep trench (5-10 μm) is etched into the silicon. A capacitor structure is built in the deep trench. The capacitor dielectric can be either an oxide or a thermal oxide/CVD-nitride combination. The second use of trenches is called the *shallow trench isolation* (STI) structure. In the STI application individual MOS devices are isolated from each other by a shallow trench etched into the silicon. The trench is thermally oxidized and filled with a deposited oxide to make it non-conducting. The device is then built on the plateaus of silicon between the trenches. The use of STI is the most popular isolation technology for advanced devices (i.e., for 0.25 μm technologies, and smaller). See Chap. 16 for more details on STI.

The oxidation profile in a trench will now be examined. When a trench is oxidized, oxidation occurs on the flat regions at the top and bottom of the trench and at both the convex and concave

corners. Marcus and Sheng showed dramatic examples of oxide thinning at the corners of oxidized etched steps in silicon.⁴⁵ Low temperature oxidations (900–950°C) displayed as much as 30% decrease in the oxide thickness at both the concave and convex corners of the step. A later study by Kao *et al.*, examined the retardation of oxidation on cylindrical structures with varying radii of curvature.⁴⁶ They measured the oxidation rates using steam and dry oxidation, over the temperature range of 800–1200°C on flat regions and corners of various radii of curvature, and used SEM photographs to determine the oxide thickness. At low temperature they found significant oxide thinning at the corners while at 1100°C, the oxide thickness was uniform and the corners were well rounded. Fig. 8-24 shows a SEM of such a structure with substantial thinning at both corners. Figure 8-24b, shows a schematic representation of the results. Also shown in Fig. 8-24 are oxides grown on the outside of a cylinder of silicon (convex) and the inside of a silicon hole (concave). Both corners show reduced oxidation, while the oxide on the concave appears to be thinner than the convex. The circular structures reveal that oxidation on the concave is less than on the convex structure. Fig. 8-25 shows a plot of normalized oxide thickness vs. reciprocal radius of curvature for both concave and convex surfaces. That plot shows that the smaller radius of curvature results in thinner oxides, as does oxidation at lower temperature. In all cases the concave surface produced a thinner oxide than the convex surface.

The retarded oxidation observed at both types of surfaces was attributed to the reduced chemical reaction rate (k_s) at the $\text{SiO}_2/\text{silicon}$ interface.⁴⁷ The reduced oxidation rate is believed to arise from viscous stress. The different stresses at the concave (compressive) and convex (tensile) corners account for the increased reduction on concave surfaces. The temperature dependence can be explained by the decrease in oxide viscosity at higher temperatures and less stress. The effect of radius of curvature is explained by noting that as the radius is made smaller (sharper corner) the deformation of the oxide increases. Thus, higher stress occurs in the oxide.

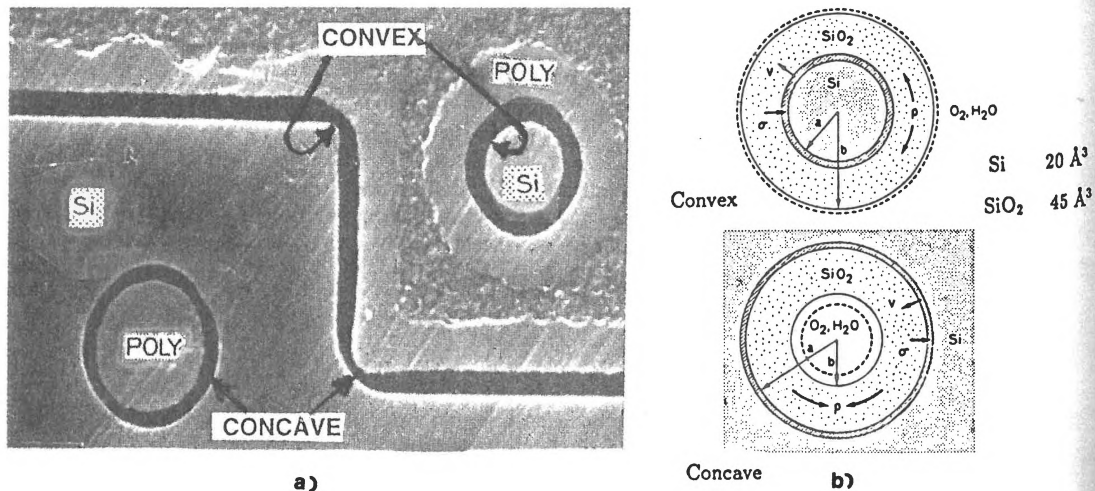


Fig. 8-24 Comparison of convex and concave silicon surfaces a) SEM on top and b) schematic on bottom. The oxide on the hole (concave) is thinner than the oxide on the cylinder (convex).⁴⁶ (© IEEE 1987).