

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd. and Apple Inc.,

Petitioners,

v.

Marlin Semiconductor Ltd.

Patent Owner.

Patent No. 9,093,473 B2

Filing Date: July 15, 2014

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Title: METHOD FOR FABRICATING
METAL-OXIDE SEMICONDUCTOR TRANSISTOR

Inter Partes Review No. IPR2025-00879

PETITION FOR *INTER PARTES* REVIEW

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LIST OF EXHIBITS

Exhibit No.	Description
Ex-1001	U.S. Patent No. 9,093,473 (“’473 Patent”)
Ex-1002	Prosecution History for U.S. Patent No. 9,093,473 (“File History”)
Ex-1003	Declaration of Dr. Eugene Fitzgerald, Ph.D.
Ex-1004	U.S. Patent Publication No. 2009/0309141 (“Okuno”)
Ex-1005	U.S. Patent Publication No. 2008/0251878 (“Mandelman”)
Ex-1006	U.S. Patent Publication No. 2006/0088968 (“Shin”)
Ex-1007	U.S. Patent Publication No. 2008/0142879 (“Chong”)
Ex-1008	S.M. Sze, <i>Physics of Semiconductor Devices</i> . (2d ed. 1981) (excerpted) (“Sze”)
Ex-1009	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted) (“Plummer”)
Ex-1010	Excerpts from C.Y. Chang & S.M Sze, <i>ULSI Technology</i> (1996) “Chang/Sze”
Ex-1011	U.S. Patent Publication No. 2006/0118878 (“Huang”)
Ex-1012	U.S. Patent Publication No. 2010/0159685 (“Chuang”)
Ex-1013	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 1: Process Technology</i> , 2 nd Ed. (2000) (“Wolf1”)
Ex-1014	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 2: Process Integration</i> (1990) (“Wolf2”)
Ex-1015	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 3: The Submicron MOSFET</i> (1995) (“Wolf3”)

Exhibit No.	Description
Ex-1016	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> , Ch. 12: Metallization (2001) (excerpted) (“Quirk”)
Ex-1017	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained-Silicon,” <i>IEEE Transactions on Electron Devices</i> , vol. 51. No. 11, pp. 1790-97 (Nov. 2004) (“Thompson2004”)
Ex-1018	U.S. Pat. Pub. No. 2006/0148151 (“Murthy151”)
Ex-1019	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-76 (2005) (“James”)
Ex-1020	U.S. Patent Publication No. 2006/0292783 (“Lee783”)
Ex-1021	U.S. Patent Publication No. 2008/0157119 (“Tsai”)
Ex-1022	U.S. Patent Publication No. 2006/0115949 (“Zhang”)
Ex-1023	U.S. Patent Publication No. 2004/0262683 (“Bohr”)
Ex-1024	B. J. Ginsberg, J. Burghartz, G. B. Bronner and S. R. Mader, “Selective epitaxial growth of silicon and some potential applications,” in <i>IBM Journal of Research and Development</i> , vol. 34, no. 6, pp. 816-827, Nov. 1990 (“Ginsberg”)
Ex-1025	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” <i>Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM)</i> , pp. 657-60 (Dec. 2004) (“Bai”)
Ex-1026	U.S. Patent No. 6,287,904 (“Lee”)
Ex-1027	U.S. Patent Publication No. 2003/0124847 (“Houston”)
Ex-1028	U.S. Patent Publication No. 2009/0023258 (“Liang”)

Exhibit No.	Description
Ex-1029	U.S. Patent Publication No. 2009/0176069 (“Yang”)
Ex-1030	U.S. Patent No. 6,605,498 (“Murthy”)
Ex-1031	U.S. Patent Publication No. 2008/0199999 (“Weijtmans”)
Ex-1032	U.S. Patent Publication No. 2008/0128746 (“Wang”)
Ex-1033	U.S. Patent Publication No. 2005/0112817 (“Cheng”)
Ex-1034	U.S. Patent No. 6,137,126 (“Avanzino”)
Ex-1035	U.S. Patent Publication No. 2007/0284615 (“Ku”)
Ex-1036	U.S. Patent Publication No. 2005/0260806 (“Chang”)
Ex-1037	U.S. Patent Publication No. 2006/0223255 (“Chen”)
Ex-1038	U.S. Patent Publication No. 2004/0253776 (“Hoffman”)
Ex-1039	U.S. Patent Publication No. 2006/0172556 (“Bather”)
Ex-1040	U.S. Patent No. 6,727,558 (“Duane”)
Ex-1041	U.S. Patent Publication No. 2011/0039390 (“Nieh”)

***Note: All citations herein to page numbers identify the page numbers of the original reference, not the stamped page numbers.**

APPENDIX OF CLAIMS

Claim	Limitation
1[pre]	A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:
1[a]	providing a semiconductor substrate;
1[b]	forming a silicon layer on the semiconductor substrate;
1[c]	performing a first photo-etching process on the silicon layer for forming a gate pattern;
1[d]	forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and
1[e]	after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.
2	The method of claim 1, wherein after forming the silicon layer comprises:
2[a]	forming a hard mask on the silicon layer;
2[b]	performing the first photo-etching process on the hard mask and the silicon layer for forming the gate pattern;
2[c]	forming a first spacer around the gate pattern;
2[d]	forming a lightly doped drain in the semiconductor substrate adjacent to two sides of the gate pattern;
2[e]	forming at least a recess in the semiconductor substrate adjacent to two sides of the first spacer;
2[f]	forming the epitaxial layer in the recess;

Claim	Limitation
2[g]	removing the hard mask disposed on the silicon layer;
2[h]	forming a first dielectric layer on the semiconductor substrate while covering the gate pattern;
2[i]	performing the second photo-etching process on the gate pattern, the first spacer, and the first dielectric layer to form the slot in the gate pattern; and
2[j]	removing a portion of the first dielectric layer for forming a second spacer.
3	The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.
4	The method of claim 1, wherein the hard mask comprises silicon nitride.
5	The method of claim 2, wherein the step of forming the first spacer comprises: forming a silicon oxide layer and a silicon nitride layer on the semiconductor substrate; and etching back the silicon oxide layer and the silicon nitride layer for forming the first spacer.
6	The method of claim 2, wherein the first dielectric layer comprises a silicon oxide layer and a silicon nitride layer.
7	The method of claim 2, wherein after performing the second photo-etching process comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.
8	The method of claim 7, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

Claim	Limitation
9	The method of claim 2, wherein after forming the second spacer comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the second dielectric layer for forming a third spacer.
10	The method of claim 9, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

I. RELIEF REQUESTED

Petitioners request *inter partes* review of U.S. Patent No. 9,093,473 (“’473 Patent”) and cancellation of claims 1-10:

Ground	Challenged Claim(s)	35 U.S.C. § ¹	Reference(s)
1	1, 3	103	Okuno, Shin
2	1-10	103	Chong, Okuno
3	1, 3	103	Mandelman, Shin
4	1-6	103	Chong, Mandelman

II. TECHNOLOGY BACKGROUND

The ’473 Patent discloses methods for fabricating metal-oxide-semiconductor (“MOS”) transistors by defining a gate pattern, forming an epitaxial layer, and “separating the gate pattern into two gates.” Ex-1001, 5:1-12. By July 2010, to which the ’473 Patent purportedly claims priority, such methods were already well-known.

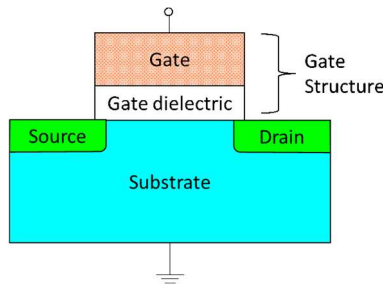
A. MOS Transistors

Introduced in the 1960s, MOS transistors have become a cornerstone of modern electronics. Ex-1003, ¶43; Ex-1008, 431. MOS field-effect transistors (“MOSFETs”) include four regions: *source/drain* regions for current input and output, and a *gate* overlying a *channel* region between the source/drain regions. Ex-1003, ¶43; Ex-1008, 433-34, Fig. 3. The gate (or gate structure) comprises a *gate electrode* (a conductive material like metal or polysilicon) and a gate dielectric (an

¹ This Petition cites to pre-AIA 35 U.S.C. §§102 and 103 for statutory authority.

insulating film like oxide) that separates the gate from the channel underneath.

Ex-1003, ¶43; Ex-1008, 433-34, Fig. 3.



Ex-1003, ¶43. Applying a voltage to the gate creates the channel to connect the source and drain. *Id.* By controlling the conductance of the channel, one can turn on or off a MOSFET and use it as a switch. *Id.*

Conventionally, the source/drain regions are *doped* with *p-type* or *n-type* impurities, while channel regions are oppositely doped. Ex-1003, ¶44; Ex-1008, 433-34; Ex-1009, 76-82. **PMOS** and **NMOS** refer to MOSFETs with p-type or n-type source/drain regions, respectively. Ex-1003, ¶44; Ex-1009, 12-13, 50-51, Figs. 1-11, 2-2. **CMOS** (Complementary MOS) devices include both. Ex-1003, ¶44; Ex-1009, Fig. 1-11.

B. Lightly Doped Drain (“LDD”) Regions and Sidewall Spacers

Since the 1960s, semiconductor fabrication has continuously improved according to Moore’s Law, making individual transistors smaller and, thereby, increasing transistor-density. Ex-1003, ¶46; Ex-1010, xviii-xxi; Ex-1014, 1, Fig. 1-1(b). Shrinking a MOSFET, however, shortens the channel, bringing the source/drain regions closer, Ex-1003, ¶46; Ex-1015, 205, 233-34; Ex-1014, 338,

which consequently increases the potential for the electric field to “penetrate into the source region” (known as *punch-through*), causing unwanted current increase (known as short-channel effects). Ex-1014 at 341; *see* Ex-1003, ¶¶46-47; Ex-1015, 233; Ex-1008, 433; Ex-1016, 211; Ex-1009, 77-78.

By the 1980s, researchers found that controlling the source/drain doping could improve transistor performance by “carefully tailor[ing] the doping profile near the drain junction (and the source junction) in order to minimize short channel effects.” Ex-1009, 78. Introducing LDD regions between the source/drain regions and channel improved performance by controlling electric fields near the channel. Ex-1009, 77-78; Ex-1003, ¶48. Because LDD extends a more heavily doped source/drain region, it is sometimes also referred to as an extension region. Ex-1003, ¶48; Ex-1034, 4:14-23, Fig. 1; Ex-1035, [0021]; Ex-1031, [0007]; Ex-1040, 1:46-51; Ex-1041, [0017]. The textbook figures below depict a method of forming LDD regions. Ex-1009, 76-77; Ex-1003, ¶48.

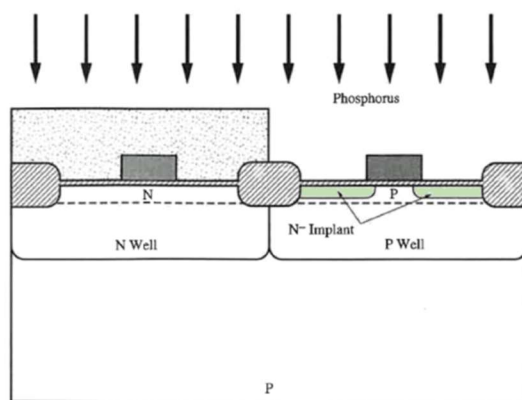


Figure 2-27 Mask 7 is used to cover the PMOS devices. A phosphorus implant is used to form the tip or extension (LDD) regions in the NMOS devices.

Ex-1009, Fig. 2-27

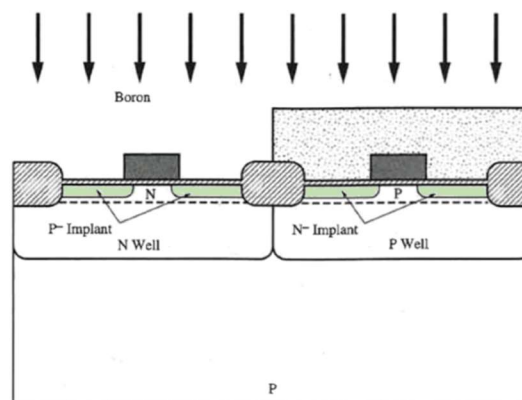


Figure 2-28 Mask 8 is used to cover the NMOS devices. A boron implant is used to form the tip or extension (LDD) regions in the PMOS devices.

Ex-1009, Fig. 2-28

The LDD regions reduce the electric field's effect on the channel by positioning the more heavily doped source/drain regions farther away from the gate using sidewall spacers. Ex-1003, ¶48; Ex-1009, 76-82, 78-80; Ex-1016, 211-13. The '473 Patent admits it is conventional to form LDD. Ex-1003, ¶48; Ex-1001, 1:26-42.

The spacers formed on the sidewalls of the gate also act as masks during heavy doping, protecting the LDD regions underneath. Ex-1009, 80-82, Figs. 2-31 to 2-33; see Ex-1016, 213, Fig. 9.17; Ex-1015, 595-96, Fig. 9-31(f); Ex-1005, [0034]; Ex-1031, [0009]; Ex-1032, [0004]; Ex-1003, ¶49.

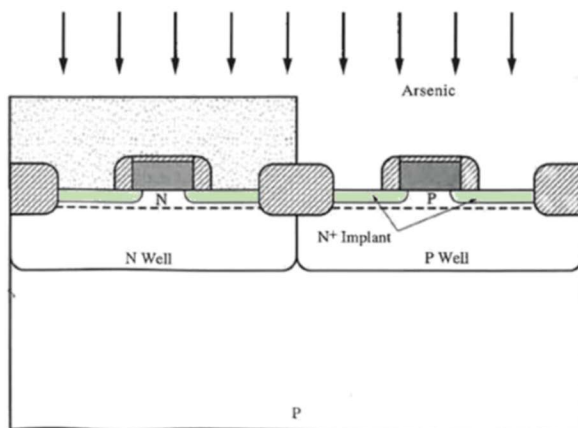


Figure 2-31 After growing a thin "screen" oxide, photoresist is applied and mask 9 is used to protect the PMOS transistors. An arsenic implant then forms the NMOS source and drain regions.

Ex-1009, Fig. 2-31

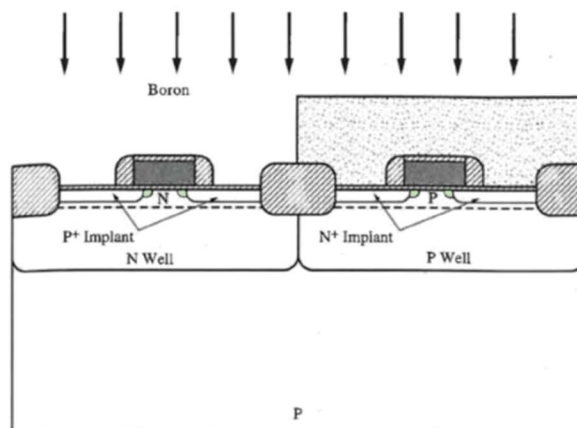


Figure 2-32 After applying photoresist, mask 10 is used to protect the NMOS transistors. A boron implant then forms the PMOS source and drain regions.

Ex-1009, Fig. 2-32

These sidewall spacers are formed by conformally depositing an insulator or dielectric and then etching back to retain only the vertical portions. Ex-1005, [0033]; Ex-1011, [0028]; Ex-1003, ¶50. The '473 Patent admits that forming such sidewall spacers was a conventional approach; such spacers were a staple in source/drain engineering. Ex-1003, ¶50; Ex-1001, 1:26-42.

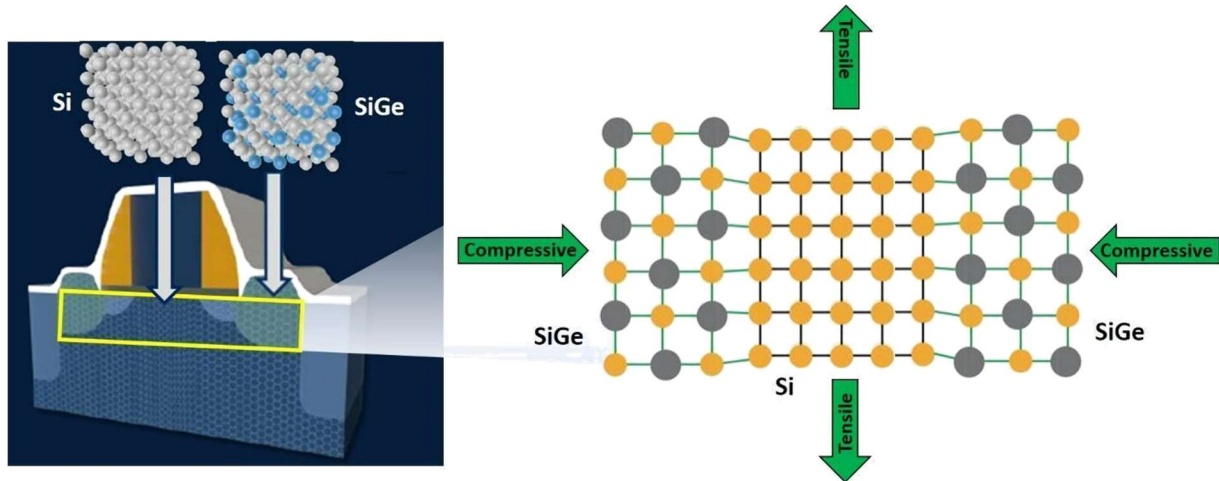
C. Creating Stress with Epitaxially Grown Source/Drain Region

Researchers found that mechanically stressing the silicon in the MOSFET channel increased the mobility of charge carriers, enhancing the transistor's switching speed and drive current. Ex-1003, ¶51; Ex-1019, 2; Ex-1017, 1790-96; Ex-1018, [0005]; Ex-1021, [0004]; Ex-1022 [0004].

One well-known method is to recess the source/drain regions and fill the recesses with *epitaxially* grown materials with differing crystal-lattice spacing. Ex-1003, ¶52; Ex-1020, [0007], [0037]; Ex-1021, [0005]; Ex-1022 [0004]; Ex-1028, [0004]. Epitaxy refers to a conventional semiconductor fabrication process where a crystal layer is grown on a substrate, using techniques like chemical vapor deposition (CVD). Ex-1003, ¶52. Selective epitaxial growth (SEG) involves growing a layer only on a specific area, such as in source/drain regions. *Id.*; Ex-1024, 816. By introducing different materials (and crystal-lattice spacing) into the source/drain regions, different stresses may be provided on the silicon channel region. Ex-1003, ¶52.

For example, *compressive* strain improves PMOS mobility, whereas *tensile* strain improves NMOS mobility. Ex-1003, ¶¶53-54; Ex-1019, 2; Ex-1017, 1790-96; Ex-1018, [0005]; Ex-1021, [0004]. Because germanium is *larger* than silicon, epitaxial silicon-germanium (SiGe) was commonly used in source/drain regions to compressively strain the silicon channel region along the current flow direction (left-

to-right below). Ex-1003, ¶¶53-54; Ex-1019, 2; Ex-1017, 1790-96; Ex-1018, [0046]-[0047]; Ex-1020, [0038]; Ex-1021, [0005]; Ex-1023, [0024], FIG. 4.



Creating tensile strain involves growing a material like silicon carbide (SiC) with atoms (carbon) *smaller* than silicon. Ex-1003, ¶55; Ex-1018, [0005], [0048], [0072]; Ex-1020, [0038]; Ex-1021, [0005]; Ex-1023, [0045]. The '473 Patent admits that “conventional approach” includes forming “epitaxial layer ... in the semiconductor substrate,” i.e., in recesses formed in the substrate. Ex-1001, 1:26-42; Ex-1003, ¶¶56-57.

D. Shallow Trench Isolation

As MOSFET devices shrunk and transistor-density increased, researchers developed a technique to prevent electrical interferences among adjacent devices, using, for example, [shallow trench isolation \(STI\)](#). Ex-1003, ¶58. STI involves etching trenches into the substrate and filing them with an insulating material. Ex-1013, 301; Ex-1003, ¶58. Below is a cross-section (left) and top (right) views of

a MOSFET with an STI. Mandelman's Fig. 4, further below, also shows a top view of MOSFET devices (e.g., 28, 32, and 34) with an STI 20.

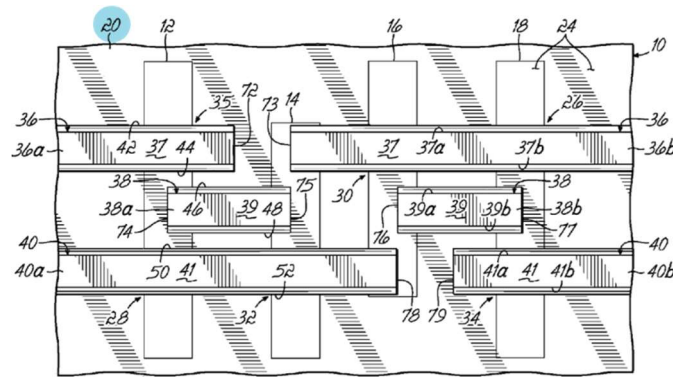
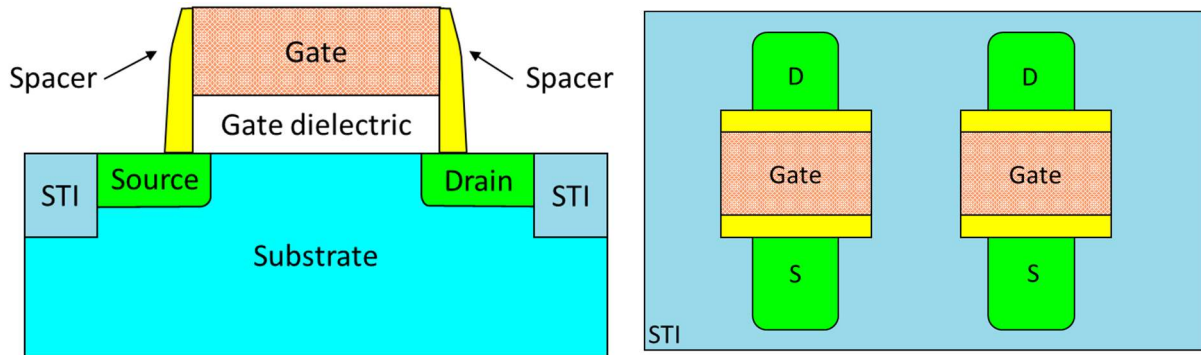


FIG. 4

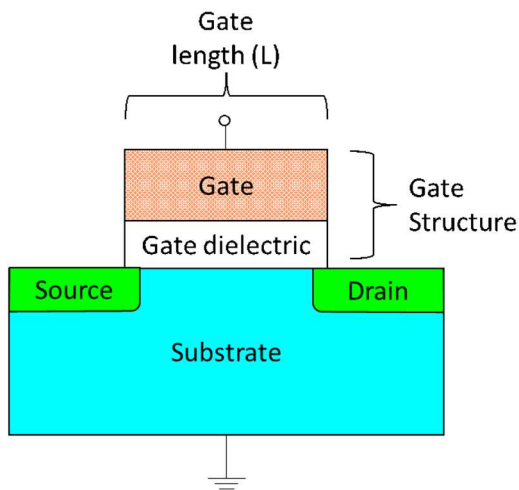
Mandelman (Ex-1005), Fig. 4

An STI allows for narrower isolation regions, enabling densely packed devices and reducing leakage currents. Ex-1003, ¶58. Its use also predates the '473 Patent. *Id.*; Ex-1005, [0029]; Ex-1004, [0031]; Ex-1007, [0033].

E. Gate Patterning

A gate structure is traditionally formed by depositing the constituent layers (e.g., a conductive layer used for the gate electrode and the underlying gate dielectric layer) and patterning them, leaving only a portion of the gate structure with gate

length (L) that overlaps the source and drain. Ex-1003, ¶59; Ex-1005, [0031]. A gate is patterned into either a segment that forms an individual gate or, more commonly (*see* Section II.F), a long continuous strip to be further separated into individual gates in a subsequent process. Ex-1003, ¶59. Patterning a gate to an appropriate length and alignment ensures device performance, as it controls current flow, provides sufficient contact area for the source/drain regions, and reduces parasitic capacitance. *Id.*; Ex-1007, [0005]-[0006], Figs. 3B-C; Ex-1026, 1:40-48.



Illustration

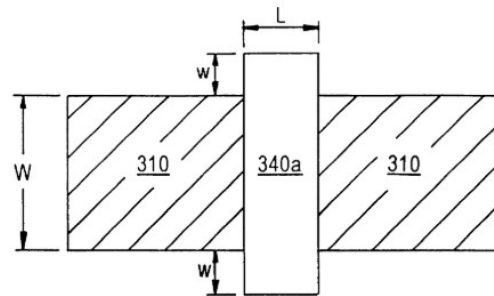


FIG. 3E

Lee, Fig. 3E

Gate patterning is conventionally performed using photolithography and etching (collectively, “photoetching”). Ex-1003, ¶60; Ex-1001, 1:28-36. During photolithography, a photosensitive material (photoresist) is applied on a substrate, and a photomask containing a desired pattern is placed over it. Ex-1003, ¶60. Light filtered by the photomask chemically exposes photoresist to transfer the pattern to the photoresist. *Id.* During subsequent etching, the gate structure underlying the

exposed portions of the photoresist is removed. *Id.*; Ex-1012, [0003], [0025]-[0026]; Ex-1027, [0004]; Ex-1029, [0002].

F. Gate Separation (Gate Cutting)

In photolithography, the photomask must be drawn so the gate pattern ends beyond the minimum width W requirement to effectively prevent “leakage current.” Ex-1026, 4:55-65, Fig. 3E; Ex-1027, [0007], Fig. 3d; Ex-1012, [0005], Fig. 2; Ex-1004, [0005]-[0006], Fig. 3; Ex-1003, ¶¶61-63.

As transistors are scaled, a phenomenon called “line end shortening,” “setback,” or “pullback” occurs because light diffusion at the corners shortens and rounds the gate image transferred to the photoresist. Ex-1026, 2:1-10; Ex-1029, [0003]; Ex-1004, [0005]; Ex-1003, ¶64. As illustrated below, although the rounded corners are only minor when the gate length L is large, the tip becomes completely rounded and exhibits endcap shortening, i.e., “setback” or “pullback,” when the gate length L is small. Ex-1026, 2:11-27, Ex-1004, [0005].

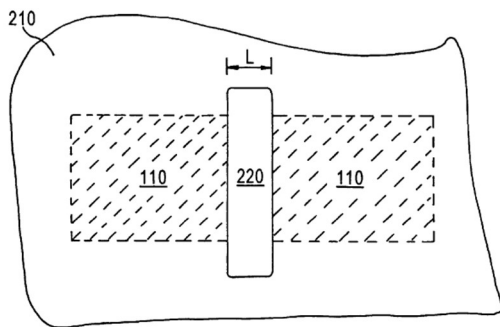


FIG. 2B
PRIOR ART

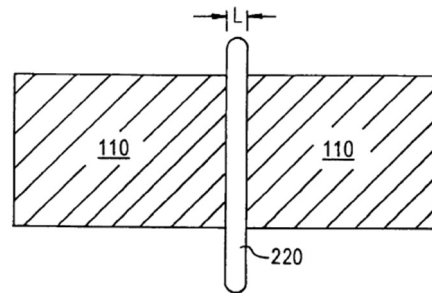
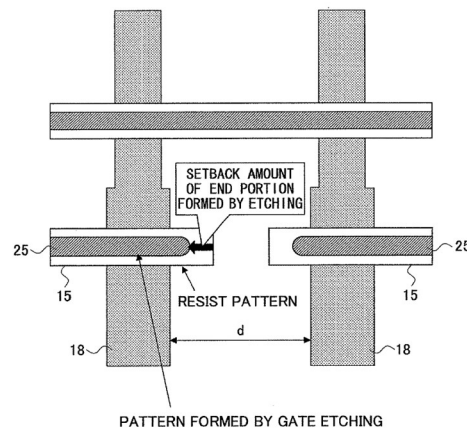


FIG. 2C
PRIOR ART

Lee, Figs. 2B-C

FIG.2



Okuno, Fig. 2

The shorter gate lengths of newer circuit designs (e.g., 150 nm or less) make gate formation harder. Ex-1003, ¶65. To maintain an acceptable margin, the endcap distance has to be increased, thereby decreasing transistor density. Ex-1026, 1:44-50, 2:39-42; Ex-1003, ¶65.

To solve this problem, researchers developed a gate separation/cutting technique to form multiple gates (e.g., 420a and 420b) by separating a continuous strip of a gate pattern (e.g., extended-width gate 420). Ex-1003, ¶66; Ex-1026, FIG. 4B (masking), FIG. 4C (etching).

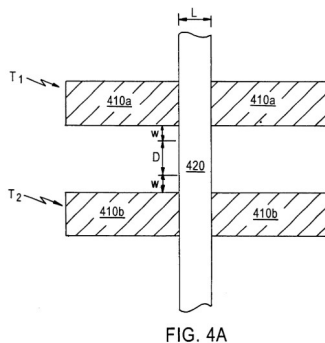


FIG. 4A

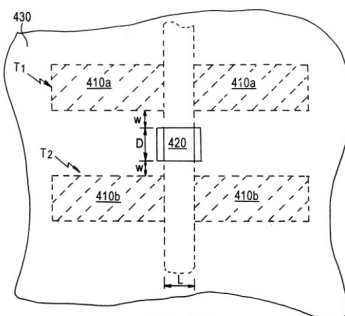


FIG. 4B

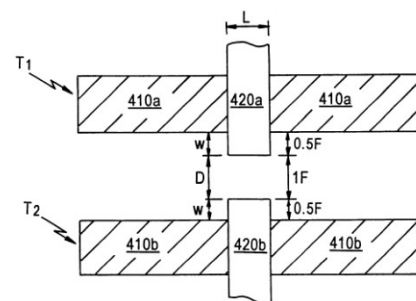


FIG. 4C

Lee, FIGS. 4A-4C

In this way, the separate gates are free of pullback (*id.*, 5:17-21), significantly decreasing transistor spacing and allowing more densely packed transistors than individually patterned gate structures. Ex-1026, 5:1-35; Ex-1005, [0036], [0038], Figs. 3-4; Ex-1004, [0008]; Ex-1012, [0025]-[0026]; Ex-1003, ¶66. As a result, by the time of the '473 Patent, the gate separation technique was the prevalent method for forming gates, and single gate patterning was out of date. Ex-1003, ¶66. Indeed, the '473 Patent admits that separating a gate pattern into multiple gates via photoetching is conventional. Ex-1001, 1:28-39.

III. THE '473 PATENT

A. Brief Description

The '473 Patent relates to a fabrication method of a MOS transistor. Ex-1001, Abstract. A semiconductor substrate 12 includes an active region 14 defined by STIs 16. *Id.*, 2:34-39, Fig. 1. Sequentially deposited on the substrate 12 are a gate insulating layer, a polysilicon layer, and a hard mask, and a **first photo-etching process** is performed to create a patterned gate insulating layer 18, **patterned polysilicon layer 20**, and **patterned hard mask 22**. *Id.*, 2:42-62; Ex-1003, ¶67.

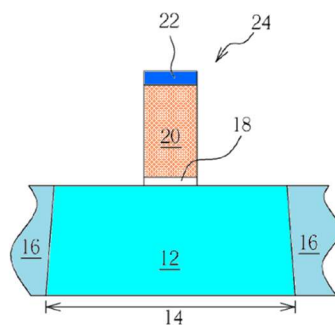


FIG. 1

A spacer 30 is next formed, and a SEG process forms a strained silicon in the two recesses 34 in the substrate 12. Ex-1001, 3:11-21. “Preferably, a light ion implantation could be conducted before the formation of the first spacer 30 and the epitaxial layer 36...for forming a lightly doped drain 32.” *Id.*, 3:21-26. As Fig. 4 illustrates, additional dielectric material is deposited for forming a second spacer 44. At “any point after the epitaxial layer 36 is formed,” a **second photo-etching process** could be performed to separate the gate pattern 24 into two gates 46. *Id.*, 4:27-31, 1:34-42, 5:1-7; Ex-1003, ¶68.

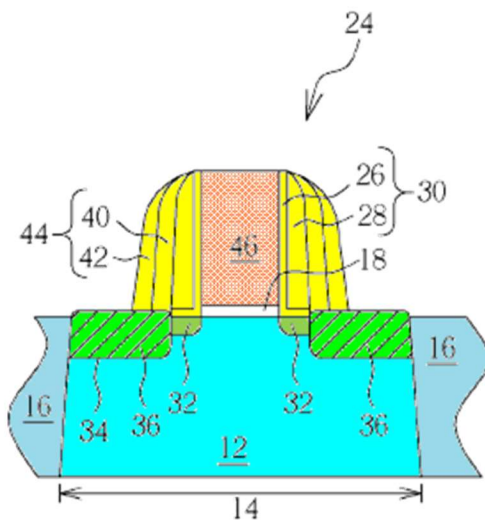


FIG. 4

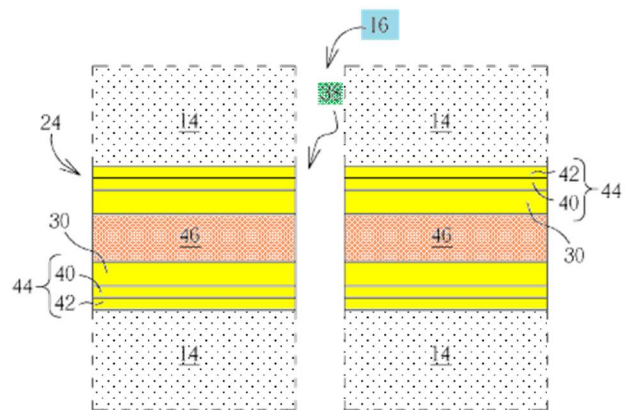


FIG. 5

B. Prosecution History

The '473 Patent was allowed in the first office action. Ex-1002. During prosecution, none of the references used in this petition—Okuno, Shin, Chong, and Mandelman—were considered. Ex-1003, ¶69.

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) and only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); 37 C.F.R. §42.100(b). No terms need construction to resolve the controversy in this forum.²

IV. LEVEL OF ORDINARY SKILL IN the ART

A person of ordinary skill in the art (“POSITA”) would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or related fields and three years of work experience in semiconductor manufacturing, including planar transistors. Additional education could substitute for professional experience, and additional work experience/training could substitute for formal education. Ex-1003, ¶39.

V. PRIOR ART

The application resulting in the ’473 Patent was filed on July 15, 2014, and was a division of a U.S. application filed on July 15, 2010 (Critical Date). Okuno, Shin, Chong, and Mandelman are prior art:

² Petitioners are not conceding that each challenged claim satisfies all statutory requirements, nor waiving any arguments that can only be raised in other forums.

Reference	Filing Date	Publication Date	Pre-AIA Qualification
Okuno (Ex-1004)	08/19/2009	12/17/2009	102(a), (e)
Shin (Ex-1006)	12/08/2005	04/27/2006	102(a), (b), (e)
Chong (Ex-1007)	12/14/2006	06/19/2008	102(a), (b), (e)
Mandelman (Ex-1005)	10/22/2007	10/16/2008	102(a), (b), (e)

VI. CLAIMS 1-10 ARE UNPATENTABLE

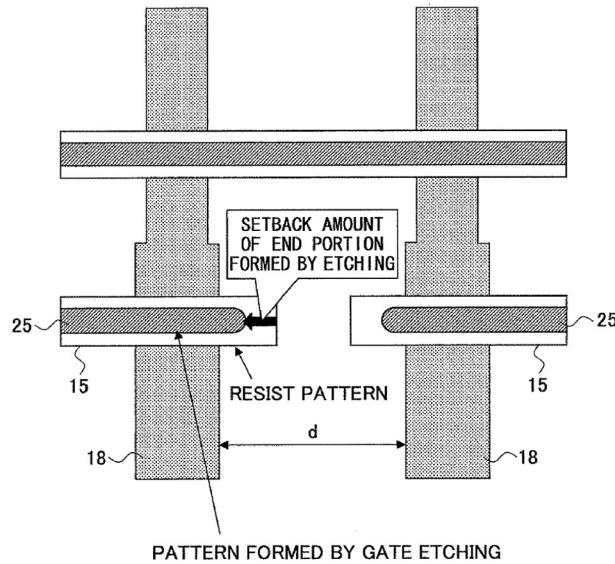
A. Ground 1: Claims 1 and 3 are Obvious Over Okuno and Shin

1. Okuno (Ex-1004)

Because Okuno is in the same field (MOSFETs) and reasonably pertinent to a problem the '473 Patent purports to address (MOSFET fabrication), Okuno is analogous art. Ex-1001, 1:15-17; Ex-1004, [0002]; Ex-1003, ¶74.

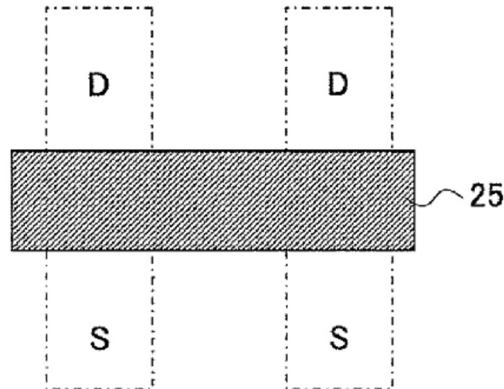
Okuno concerns “reducing the size of a SRAM” and the “protruding amount” of each gate pattern (“the setback position of a gate end portion”). Ex-1004, [0004]. The protruding amount needs to be sufficiently provided in advance when the resist patterns are formed, and this in turn requires sufficient spacing “d” to be provided between the active regions 18. *Id.*

FIG.2

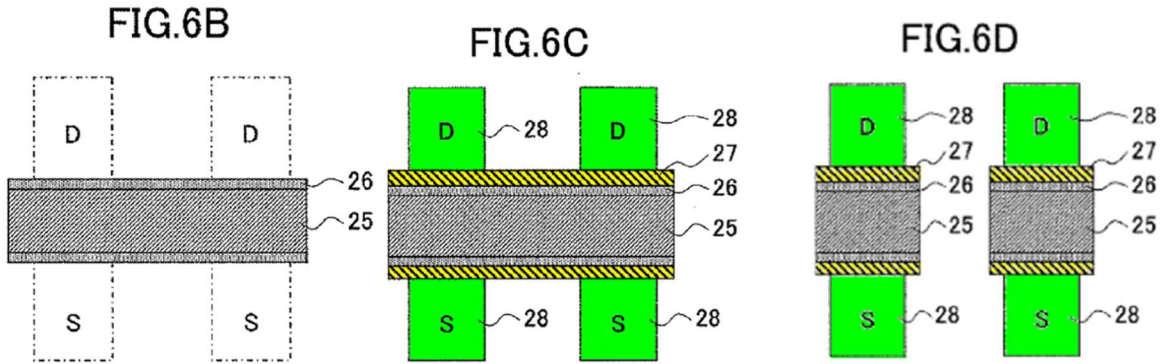


Okuno discloses etching “the gate electrode” as a straight and continuous gate pattern (Fig. 6A). *Id.*, [0026].

FIG.6A

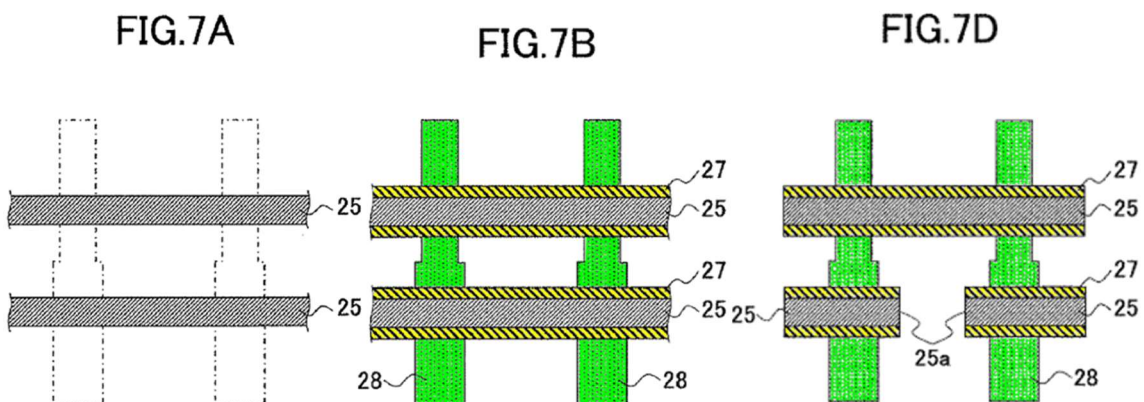


While maintaining the continuous gate electrode, Okuno forms “pocket region 26,” “sidewalls 27,” and “source/drain regions 28.” *Id.*, [0026], Figs. 6B-C. Lastly, the gate is cut and divided to form gate individual gate electrodes. *Id.*, [0026], Fig. 6D.

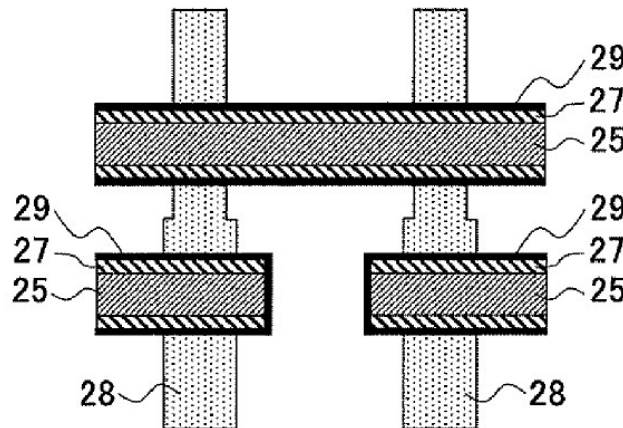


Because gate separation is performed last, “the sidewalls 27 are provided only in the longitudinal direction of the gate ... and are therefore absent from the intervening region between two opposing driver transistors.” *Id.*, [0028]. The absence of spacers on the cut edges “contribut[es] to the size reduction of the cell structure.” *Id.*, [0028]; *see also* [0041].

Okuno’s concept is further illustrated with respect to Figs. 7A-7D. Gate structures lastly are cut and separated in Fig. 7D, thus completing one embodiment. *Id.* at [0032]-[0035], Fig. 7A-D.



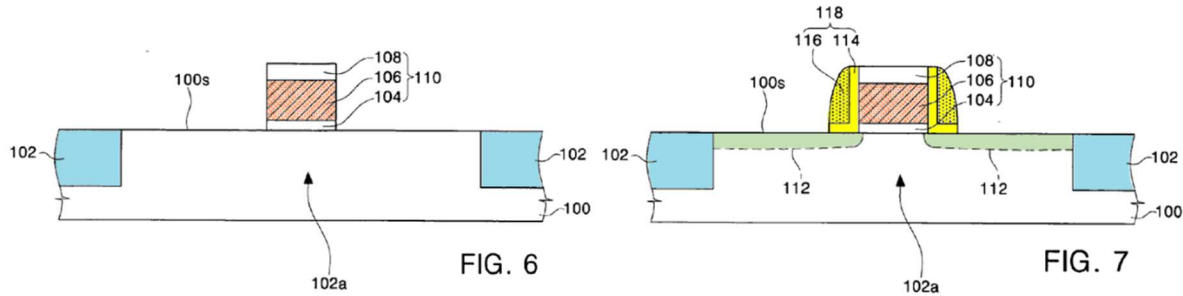
Okuno describes another embodiment (with respect to Fig. 7E), where thin sidewalls are optionally formed after separation of the gate electrodes 25, to cover the exposed gate edges 25a. *Id.*, [0036], Fig. 7E.



2. Shin (Ex-1006)

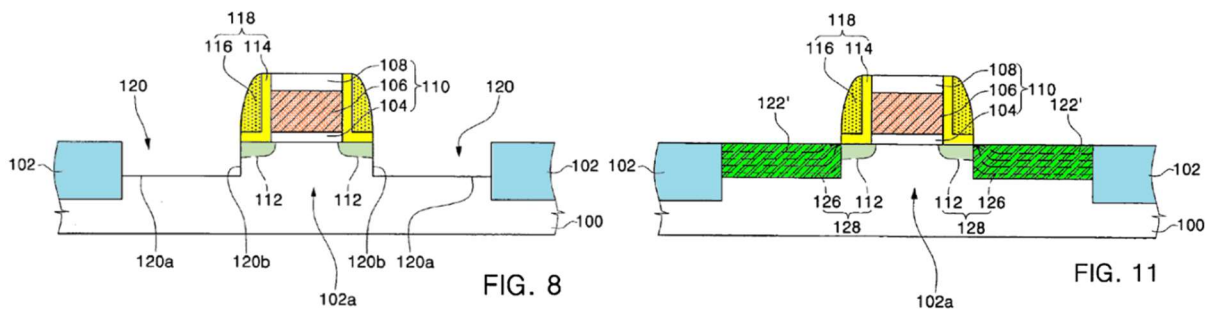
Because Shin is in the same field (MOSFETs) and reasonably pertinent to a problem the '473 Patent purports to address (MOSFET fabrication), Shin is analogous art. Ex-1001, 1:15-17; Ex-1006, [0005]; Ex-1003, ¶82.

Shin addresses methods for implementing “high-performance” MOS transistors as they “scale down i[n] size.” Ex-1006, [0005]. Shin’s fabrication involves separating active region 102a with an isolation layer 102 and forming a **gate pattern 110** made of gate insulating layer 104, a gate electrode 106, and a capping layer pattern 108. *Id.*, [0081], Fig. 6. Next, **low concentration impurity regions 112 are made via LDD implants**, and spacers 118 (an oxide spacer 114 and nitride spacer 116) are formed. *Id.*, [0082], Fig. 7.



Epitaxial layers 122 (SiC or SiGe) are formed in recesses 120. *Id.*, [0083]-[0089].

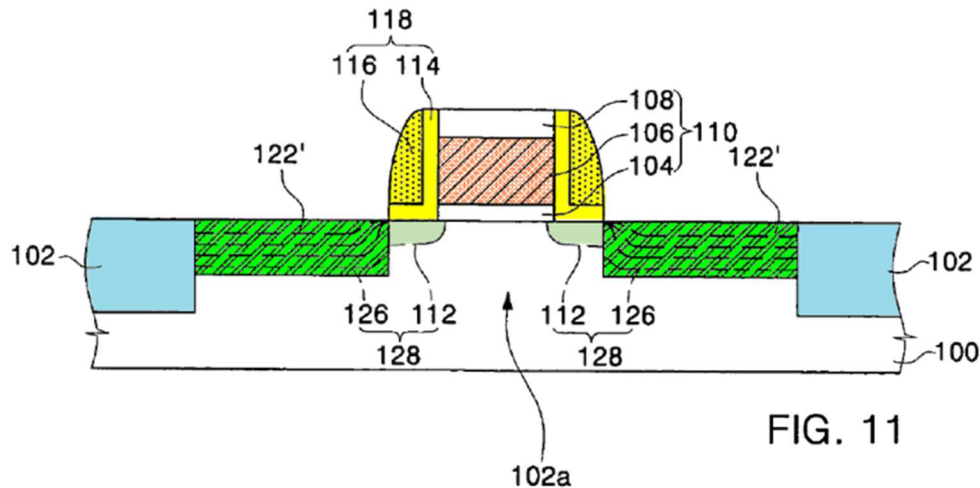
Finally, ion implantation is performed to form source/drain regions 126. *Id.*, [0090].



3. Combining Okuno and Shin

Okuno and Shin disclose similar MOS transistors fabricated on a bulk substrate. Ex-1004, [0002]; Ex-1006, [0005]; Ex-1003, ¶85. Both disclose common elements, including an STI (Ex-1004, [0031]; Ex-1006, [0005], [0081]) and spacers (Ex-1004, [0026]; Ex-1006, [0082]). Both utilize an LDD. Ex-1003, ¶85. For example, Okuno performs “extension implantation” (Ex-1004, [0026], [0033]), which a POSITA would have understood to mean an LDD. Ex-1003, ¶85; Ex-1034, 4:14-23, Fig. 1; Ex-1035, [0021]; Ex-1031, [0007]; Ex-1040, 1:46-51; Ex-1041, [0017]; §II.B. Similarly, Shin teaches forming “low concentration impurity regions 112.” Ex-1006, [0082]. Both also seek to solve similar problems related to

miniaturization, with Okuno seeking to reduce transistor spacing by reducing the “protruding amount” (Ex-1004, [0004], Figs. 3A-C) and Shin seeking to overcome the short channel effect by introduce compressive or tensile stress using epitaxial source/drain regions (Ex-1006, [0005], [0084], Fig. 11. Ex-1003, ¶85.



Shin, Fig. 11

A POSITA would have found it obvious that forming epitaxial source/drain regions, as Shin teaches, in Okuno’s transistors would introduce compressive or tensile stress and increase carrier mobility. Ex-1003, ¶¶86-87; Ex-1004, [0026]; Ex-1006, [0084]; Ex-1031, [0021]-[0026]; Ex-1033, [0044]; Ex-1030, 1:20-34, 3:43-52, 4:19-33; Ex-1006, [0084]; Ex-1031, [0010]; §II.C. Using epitaxial source/drain would enable Okuno’s device to have shorter channel length and higher drive current, furthering Okuno’s goal of increasing transistor density. Ex-1003, ¶87.

Forming an epitaxial source/drain in the recesses was a well-known technique. §II.C; Ex-1003, ¶88. SEG involves forming recesses adjacent to the gate structure

and backfilling them with an epitaxial SiGe or SiC layer to create stress. Ex-1030, 2:37-49, 2:62-65, 4:33-46; Ex-1006, [0010], [0084]; Ex-1031, [0018]-[0021]; §II.C. A POSITA looking for ways to further Okuno's goal of size reduction would have introduced stress to improve its drive current while providing punchthrough suppression and looked to Shin for implementation details. Ex-1003, ¶¶88-89; Ex-1004, [0004]-[0005]; Ex-1006, [0005].

A POSITA would have had a reasonable expectation of success in forming recesses adjacent to Okuno's spacers 27 and backfilling the recesses with an epitaxial layer, as Shin teaches. Ex-1003, ¶90. Such modification would have been minor and within the expertise of a POSITA. *Id.* Shin's SEG process would have simply been added after Okuno's spacer formation and before source/drain implantation. Ex-1006, [0038], [0090]; Ex-1004, [0026], [0033]; Ex-1003, ¶90. After performing SEG, a POSITA would have proceeded with the remaining steps taught by Okuno, including gate separation. Ex-1004, [0028], [0032]-[0035], Figs. 6C, 6D, 7C, 7D; Ex-1003, ¶90.

The combination is therefore an obvious example of (1) implementing a known technique (selectively growing an epitaxial layer) to improve known devices (MOS devices) to achieve predictable results (introducing mechanical stresses into the channel region to improve carrier mobility and overcoming the short channel effect); (2) a choice from a finite number of identified, predictable solutions

(forming source/drain regions mainly through selective epitaxial growth and/or ion implantation); and (3) a teaching, suggestion, or motivation in the prior art (*see* Ex-1006, [0084]). *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416–21 (2007); Ex-1003, ¶91.

4. Claim 1

(a) 1[pre]: “A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:”

To the extent the preamble is limiting, Okuno discloses 1[pre] by disclosing “a manufacturing method” for fabricating MOS transistors for SRAMs. *See* Ex-1004, [0002] (Okuno is directed to “a gate structure of a MOS semiconductor device and a manufacturing method of the same”); [0031]. Specifically, Okuno discloses cutting and dividing a gate structure to form separate gate electrodes after forming the source/drain regions. *Id.*, [0026]; Ex-1003, ¶92.

(b) 1[a]: “providing a semiconductor substrate;”

Okuno discloses 1[a] by fabricating its MOS devices “on a silicon substrate.” *See* Ex-1004, [0031] (“[A]ctive regions of the SRAM are defined by forming ... STI (shallow trench isolation), on a silicon substrate.”); Ex-1003, ¶93.

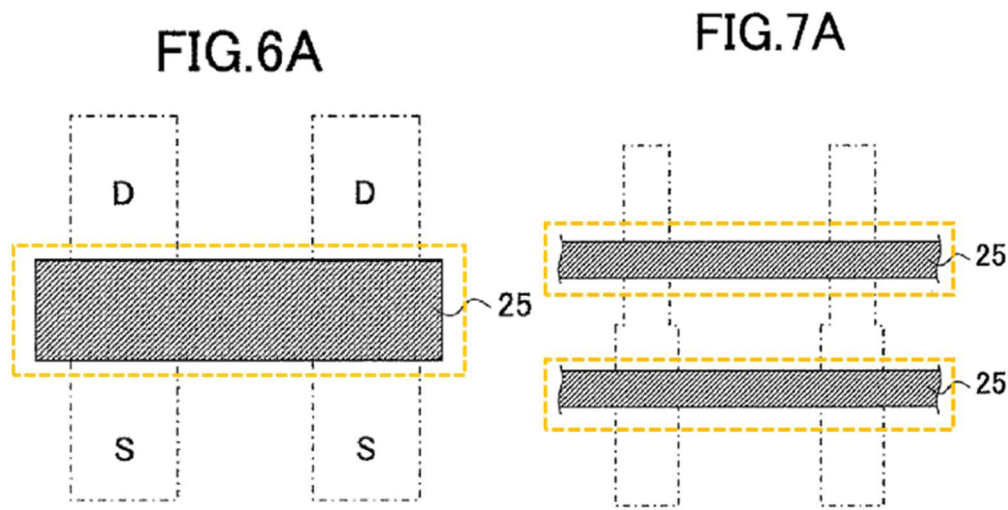
(c) 1[b]: “forming a silicon layer on the semiconductor substrate;”

Okuno discloses 1[b] by depositing a polysilicon film (“silicon layer”) over a gate oxide film on the semiconductor substrate for forming the gate, consistent with the ’473 Patent. Ex-1004, [0031]; Ex-1003, ¶94. As the ’473 Patent explains, “a

polysilicon layer” is formed on a “gate insulating layer” that is “deposited on the surface of the semiconductor substrate 12.” Ex-1001, 2:42-47, 2:55-61.

(d) 1[c]: “performing a first photo-etching process on the silicon layer for forming a gate pattern;”

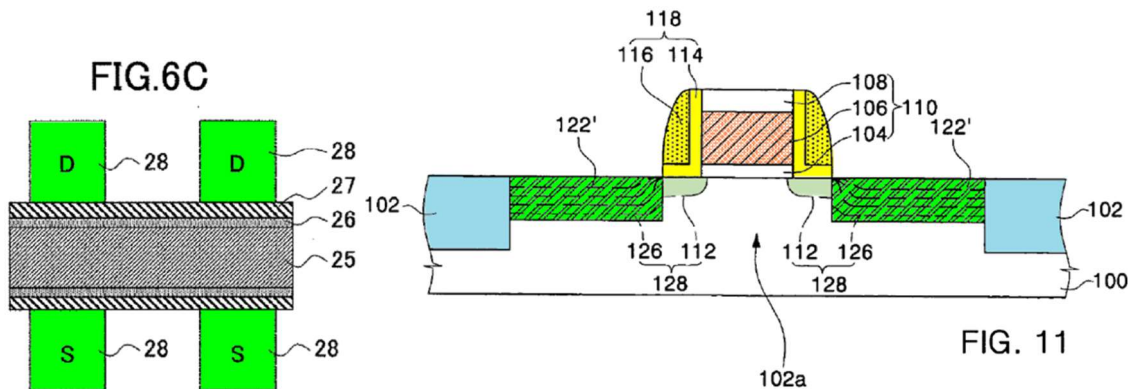
Okuno discloses 1[c] by etching the polysilicon film and gate oxide film according to gate patterning to create “straight and continuous patterns of the gate electrodes 25.” Ex-1004, [0031]-[0032]; *see also id.*, [0026] (“[E]tching of the gate electrode 25 is performed based on a straight and continuous gate pattern, as illustrated in FIG. 6A”); Ex-1003, ¶95. In Okuno, a “conventional method” is performed using a mask and an etchant to form the “gate electrode material film” into a “gate pattern.” Ex-1004, [0032], [0026], Claim 6. A POSITA would have understood that a “photo-etching process” was used to selectively remove portions of the underlying structure to form the gate pattern. Ex-1003, ¶95; §II.E. Figs. 6A and 7A show the gate patterns.



Okuno, Figs. 6A, 7A

- (e) **1[d]: “forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and”**

Okuno and Shin render 1[d] obvious. *See* §VI.A.3. Okuno discloses forming source/drain regions (Ex-1004, [0034], [0026], [0010], Fig. 6D), and Shin discloses growing epitaxial SiGe/SiC layers in recesses in the substrate adjacent to two sides of the gate pattern for forming the source/drain regions (Ex-1006, [0084], Fig. 11). It would have been obvious to use epitaxial SiGe/SiC layer for the source and drain regions 28, as Shin teaches, in the semiconductor substrate adjacent to two sides of Okuno’s gate electrodes 25. Ex-1003, ¶96.



Okuno, Fig. 6D (left); Shin, Fig. 11 (right)

- (f) **1[e]: “after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.”**

Okuno discloses 1[e] by disclosing that after source/drain regions are formed, performing another photoetching process to cut and divide the gate electrodes (“gate pattern”) in designed shapes (i.e., into two gates). Ex-1004, [0026], [0034]; Ex-1003,

¶97. In Okuno, a mask 20 having a predetermined opening 21 is used to expose a portion of the gate pattern. Ex-1004, [0034], Figs. 7C, 7D:

FIG. 7C

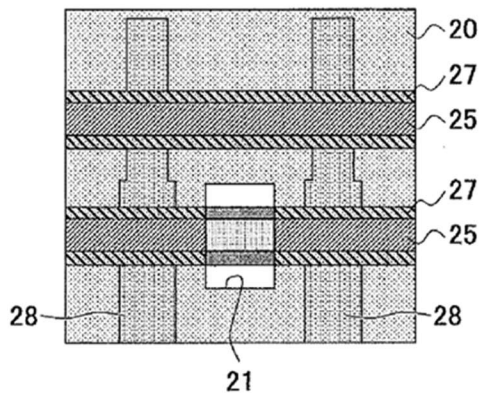
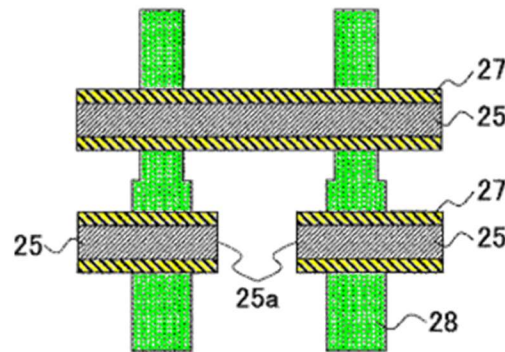


FIG. 7D



Okuno, Figs. 7C-7D

As illustrated above, the portion removed under the opening 21 (i.e., the cut portion) forms a “slot” in the gate pattern to physically separate it into two separate gates.

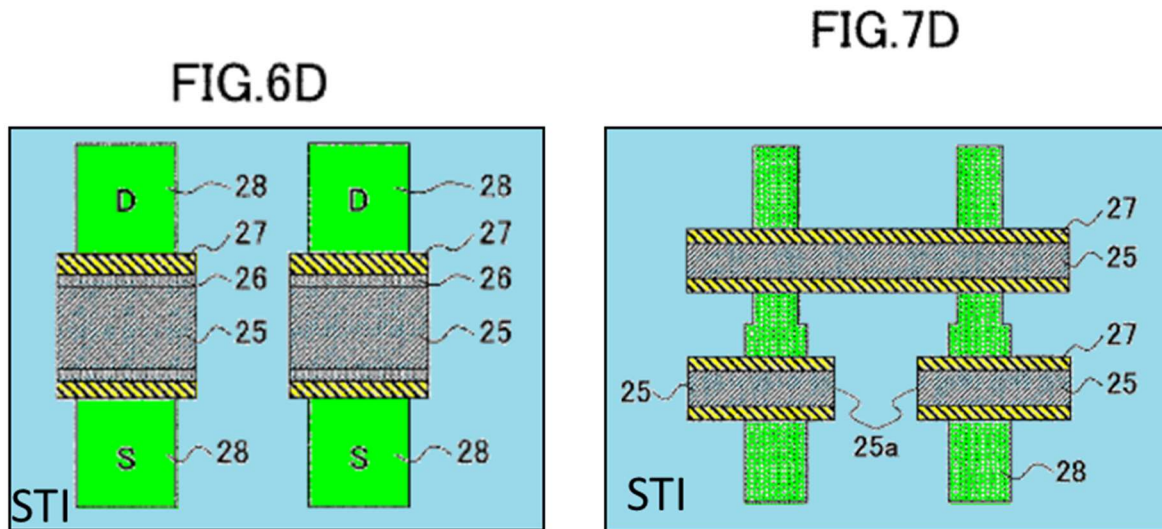
Id., [0035]; Ex-1003, ¶98.

Because Okuno performs the second photoetching after forming the source/drain regions, the second photoetching process would be performed after the formation of the epitaxial SiGe/SiC layer. Ex-1003, ¶99.

- 5. Claim 3. “The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.”**

Okuno and Shin render claim 3 obvious. Okuno discloses that the substrate includes STI regions. Ex-1004, [0031] (“[A]ctive regions of the SRAM are defined

by forming an element separating region (not shown), such as STI (shallow trench isolation), on a silicon substrate.”). Okuno’s figures below are annotated to include STI, consistent with Okuno’s description. Ex-1003, ¶100.



Okuno, Figs 6D and 7D (Modified)

Okuno also discloses that “the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.” Okuno’s second photoetching applies a resist and mask to the entire surface to expose a gate cut portion and subsequently etches away exposed portions of the gate structure. Ex-1004, [0035]; Ex-1003, ¶101. For example, in Okuno, the etching may employ a reactive ion etching (RIE), a widely used technique, using chemically reactive plasma to etch away the silicon layer disposed on the STI regions. Ex-1004, [0034] (using a mixed gas including hydrogen bromide (HBr) and oxygen); Ex-1005, [0033], [0037]; Ex-1003, ¶101.

B. Ground 2: Claims 1-10 are Obvious Over Chong and Okuno

1. Chong (Ex-1007)

Because Chong is in the same field (MOSFETs) and reasonably pertinent to a problem the '473 Patent purports to address (MOSFET fabrication), Chong is analogous art. Ex-1001, 1:15-17; Ex-1007, [0003], [0009]; Ex-1003, ¶102.

Chong discloses using differential spacers to “maximize the performance of” p-channel and n-channel Field-Effect Transistors (PFETs and NFETs) in a CMOS configuration and seeks to overcome challenges brought by scaling of the transistors. Ex-1007, [0003]-[0004], [0009], [0026]. Chong seeks to improve carrier mobility with a punch-through suppression layer, engineered to induce strain and suppress short channel effects. *Id.*, [0007], [0044].

Chong’s CMOS device (NFET 102 and PFET 104) is formed “from conventional deposition, patterning, photolithography, and etching.” *Id.*, [0029]. For example, the PFET 104 includes a PFET gate 122, a PFET gate oxide 124, and a PFET channel 126. *Id.*, [0031]. Surrounding the PFET gate 122 are a PFET first liner 128 and a PFET first spacer 130, which may be made from materials that include oxygen and nitrogen, respectively. *Id.* A PFET source/drain extension 132 is “formed by a low to medium-dose implant” and “extends from the PFET channel 126 in the substrate 118 to facilitate dimensional reductions.” *Id.* “A PFET cap 134, such as a nitride or an oxynitride cap, helps to protect the PFET gate 122 during

subsequent processing steps.” An [isolation structure 136](#), such as a shallow trench isolation is formed within the substrate 118. *Id.*, [0033].

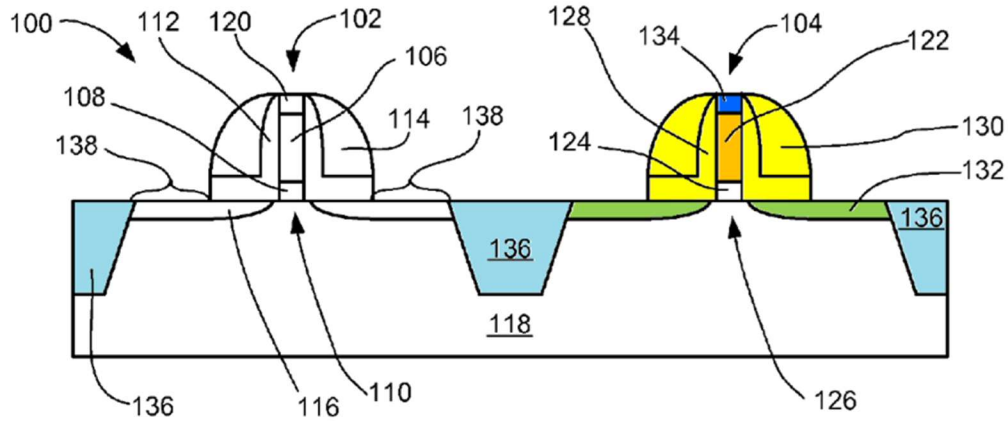


FIG. 1

A PFET recess 400 is formed by selective etching (*id.*, [0038], Fig. 4); a punchthrough suppression layer 500 made from epitaxially grown SiGe is formed within a [PFET source/drain 502](#) (*id.*, [0040]-[0045], Fig. 5); and [the PFET cap 134](#) is removed (*id.*, [0047], Fig. 6).

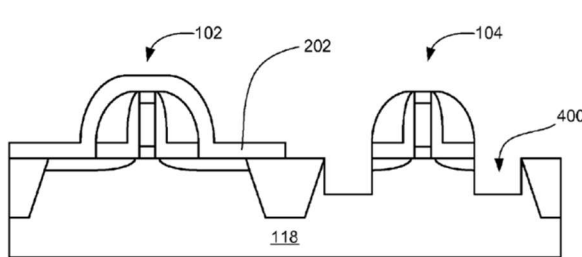


FIG. 4

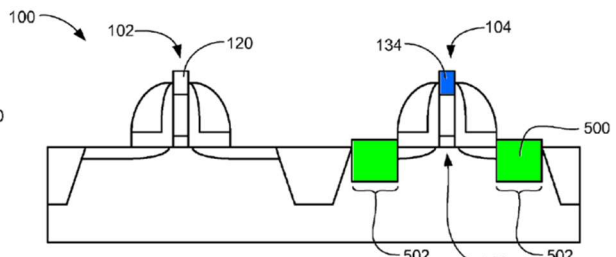


FIG. 5

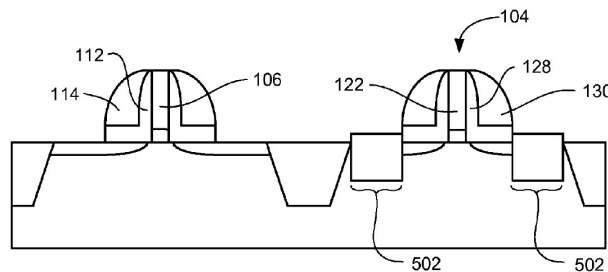


FIG. 6

A PFET second liner 702 and a PFET second spacer 706 are then formed by blanket deposition followed by subsequent etchback. *Id.*, [0049]-[0051], Fig. 7. The liner 702 and spacer 706 may be made from dielectric materials such as oxide and nitride and collectively form part of a differential spacer 708. *Id.*, [0051]-[0052].

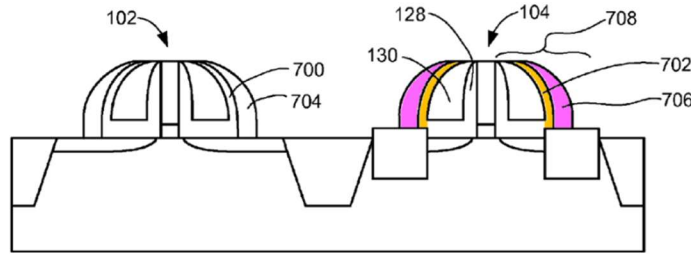


FIG. 7

Thereafter, a differential spacer 902 and source/drain region 900 are formed for the NFET device 102. *Id.*, [0056]. To protect the PFET device 104 from the source/drain implant step of the NFET source/drain 900, a mask 904 is formed over the PFET device 104. *Id.*, [0057], Fig. 9.

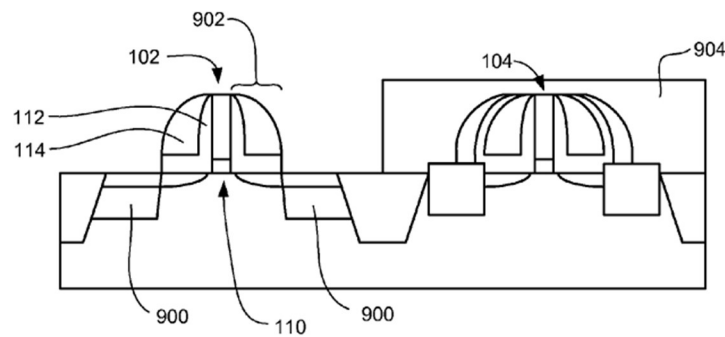


FIG. 9

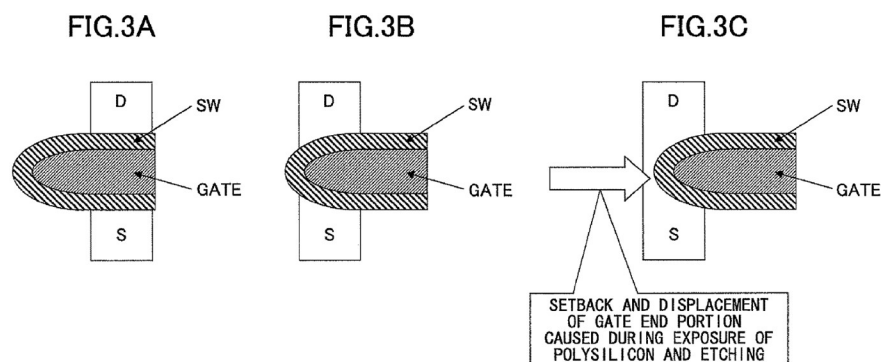
After the NFET source/drain implant, the mask 904 is removed, exposing both NFET and PFET devices for further processing such as a silicide process. *Id.*, [0059]-[0060].

2. Combining Chong and Okuno

(a) A gate-cutting process to separate Chong's gate structures for miniaturization

Chong and Okuno disclose similar MOS transistors fabricated on a bulk substrate. Ex-1004, [0002]; Ex-1007, [0003], [0009], [0026]; Ex-1003, ¶109. Okuno discloses an STI, spacers, and source/drain extensions. §VI.A.3. Chong also discloses these elements. Ex-1007, [0033] (isolation structure 136), [0031] (first liner 128, spacer 130, and source/drain extension 132).

Further, Chong and Okuno both seek to solve problems related to miniaturization of transistors. Ex-1003, ¶110. Okuno seeks to reduce spacing between the neighboring transistors by reducing the “protruding amount.” Ex-1004, [0004], Fig. 2. A protruding amount is needed to account for a setback of the gate etching, which results in the formation of a gate shorter than the length specified in the resist pattern. *Id.*, [0005]; §II.F. If insufficient protruding amount is provided, the gate end could fail to overlap the active region (the source and drain), resulting in a defective device. *Id.*, [0006], Figs. 3B-C.



Okuno, Figs. 3A-C

An excessive protruding amount, on the other hand, would result in poor density, as devices would be spaced farther apart than necessary. Ex-1003, ¶111. Okuno discloses a gate separation technique that allows to form a sufficient protruding amount while spacing the transistors in a compact arrangement. Ex-1004, [0009]-[0011], Fig. 10; Ex-1003, ¶111. Similarly, Chong seeks to facilitate size reduction of transistors while overcoming unintended strain effects that result from scaling of a MOSFET. Ex-1007, [0004].

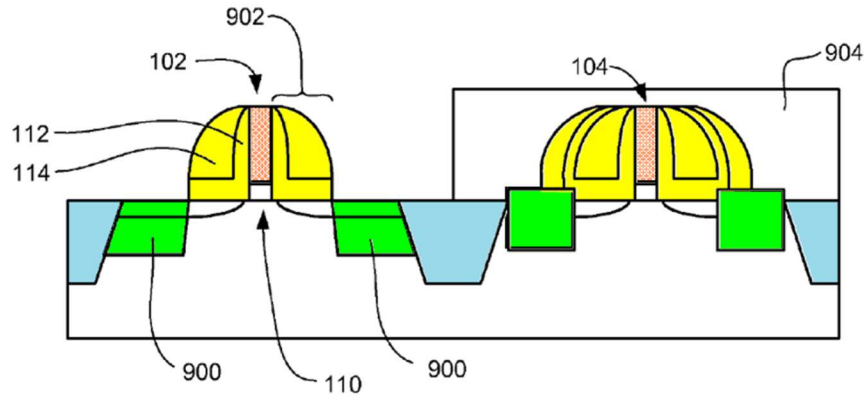
A POSITA would have found it obvious to separate Chong's gate pattern into two gates, as Okuno teaches. §VI.A.4(f); Ex-1004, [0032]; Ex-1005, [0036], [0038], Figs. 3-4; Ex-1026, 5:1-35; Ex-1012, [0025]-[0026]; Ex-1003, ¶112. There are only finite options for patterning gates: patterning each individual gate separately or cutting a single patterned gate strip into multiple gates. Ex-1003, ¶112. As discussed in §II.F, the latter method reduces spacing and increase transistor density by overcoming photolithography limits. *Id.* Gate cutting, applied to Chong's device, would predictably enable size reduction while maintaining control over the strain effects. *Id.*, ¶112.

Further, Okuno is directed to SRAM (static random access memories), which consists of multiple CMOS inverters, which in turn consist of a pair of PMOS and NMOS devices. Ex-1004 at [0003]. Because Chong discloses improving the performance of both NFET and PFET in the CMOS scheme, a POSITA would have

found Okuno's teachings to be applicable to Chong. Ex-1007 at [0026], [0003]; Ex-1003, ¶113.

Performing Okuno's second photoetching process *after* Chong has finalized the fabrication of the source/drain regions would also have been obvious. Ex-1003, ¶114. The '473 Patent admits both techniques (epitaxial layer formation and gate separation) were known (Ex-1001, 1:28-42), and prior art expressly motivates separating the gate pattern after source/drain formation. Okuno is explicit that, with respect to the embodiment shown in Figs. 7A-7D, the second photoetching process is the last step. Ex-1004, [0026] ("***Lastly***,...the gate is cut and divided to form gate electrodes in designed shapes."), [0035] (after gate separation (FIG. 7C), "the basic structure...is completed"); §VI.A.4(e). Because Okuno's gate structure is "cut and divided at the end," "impurities are not implanted into a part of the substrate region from which the gate pattern has been removed," resulting in symmetrical impurity properties. Ex-1004, [0027]. Given Okuno's explicit disclosures, a POSITA would have been motivated to finalize Chong's source/drain regions (including any implantation) before performing the second photoetching process to avoid causing asymmetry in the impurity characteristics. Ex-1003, ¶114. For example, a POSITA would have formed the PFET source/drain 502, formed the NFET source/drain 900, and removed the third mask 904 (which was formed over the PFET 104 to protect it from the implant step of the NFET source/drain 900) before separating Chong's gate.

Ex-1007, [0048], [0055], [0057]; Ex-1003, ¶114. Chong's NFET and PFET gates would have been separated in one photoetching process for efficiency, as illustrated below. Ex-1003, ¶114.



Chong, Fig. 9

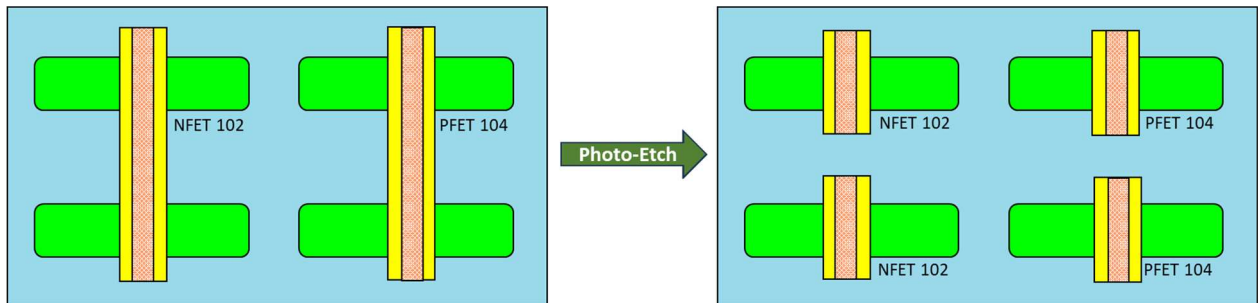


Illustration: Separation of Chong's Gates

This sequence would have prevented the NFET source/drain implant step from causing asymmetrical impurities in the gate end portions, especially in the NFET device 102, which unlike the PFET device 104 is not protected with a mask such as the mask 904 during the source/drain implant step. *Id.*

Performing the gate separation last is consistent with and supplements Chong's disclosures. Chong discloses forming an epitaxial layer by in-situ doping early in the fabrication process: before removing the hard mask 134, adjusting the source/drain concentration with ion implantation, and forming dielectric layers (liner 702 and spacer 706). Ex-1007, [0044], [0047]-[0049], [0058]; Ex-1003, ¶115. If any of the steps for forming the source/drain regions (e.g., growing an epitaxial layer and additional dopant implants) is performed after the gate separation, it will cause the same asymmetrical impurity problem that Okuno seeks to avoid. Ex-1004, [0027]; Ex-1003, ¶115. After gate separation, a POSITA would have proceeded with the silicide formation step, as both Okuno and Chong teach. Ex-1004, [0037]; Ex-1007, [0060]; Ex-1003, ¶115.

A POSITA would have had a reasonable expectation of success, using a conventional photoetch technique such as RIE (reactive ion etching) as Okuno teaches to separate the gate structures. Ex-1004, [0034], Fig. 1; Ex-1003, ¶116. As the '473 Patent admits, separating the gate pattern into two gates and growing an epitaxial layer in the source/drain regions are each a "[c]onventional approach." Ex-1001, 1:28-42.

Moreover, Okuno and Chong's teachings supplement each other: after formation of an epitaxial layer, removal of hard mask 134, and formation of liner 702 and spacer 706 (as disclosed by Chong), a POSITA would have performed

Okuno's photoetching to separate the gates. Ex-1003, ¶117; Ex-1007, [0047]-[0049], [0058].

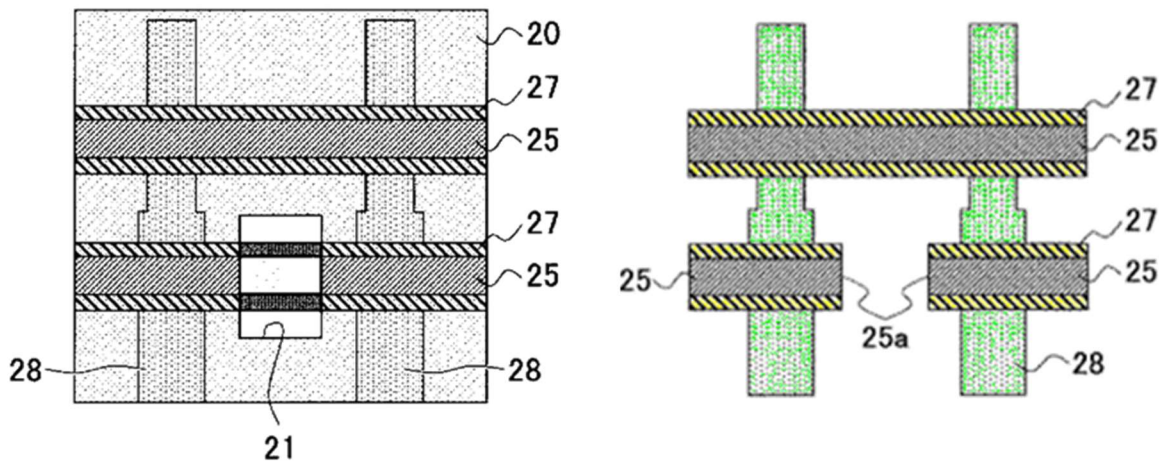
The combination is therefore an obvious example of (1) implementing a known technique (gate-cutting, through photoetching including the step such as RIE, after source drain formation) to improve known devices (MOS devices) to achieve predictable results (reduced transistor spacing, size reduction, and symmetrical impurity characteristics); (2) a choice from a finite number of identified, predictable solutions (cutting a single patterned gate strip into multiple gates or patterning individual gate separately); and (3) a teaching, suggestion, or motivation in the prior art (*see* Ex-1004, [0028]). *See KSR*, 550 U.S. at 416-21; Ex-1003, ¶118.

(b) Gate separation after a dielectric layer is formed on the gate, leaving the cut edges free of the dielectric layer

When combining Okuno's gate separation step with Chong (which discloses forming a liner 702 and spacer 706 on the PFET device), a POSITA would have been motivated to sequence the gate separation so that the cut edges are free of any spacer materials (e.g., the liner 702 and spacer 706), as Okuno teaches, to reduce any "protruding amount" at the cut edge. Ex-1004, [0041]-[0042]; Ex-1003, ¶119.

Okuno expressly motivates leaving no dielectric spacers on the cut edges. Okuno teaches performing gate separation last. Ex-1004, [0026] ("*Lastly*,... the gate

is cut and divided to form gate electrodes in designed shapes.”), [0035] (after gate separation (FIG. 7C), “the basic structure...is completed”); Ex-1003, ¶120; §VI.B.2(a). As a result, “since the gate is cut and divided at the end,” the sidewall spacers “are provided only in the longitudinal direction of the gate” and are “absent from the intervening region between two opposing driver transistors (FIG. 6(d)).” Ex-1004, [0028] (showing sidewall spacer 27 is absent in the cut slot). With respect to the embodiment shown in FIGs. 6D and 7D, Okuno expressly discloses the “size reduction” benefit of leaving the cut edges exposed. *Id.*, [0028].



Okuno, Figs. 7C-7D

Following Okuno’s express teaching, a POSITA would have sequenced Okuno’s gate separation with Chong such that the gate’s differential spacer 708 (including liner 702 and spacer 706) is not left on the cut edges. Ex-1007, [0049]-[0052], Fig. 7; Ex-1003, ¶121.

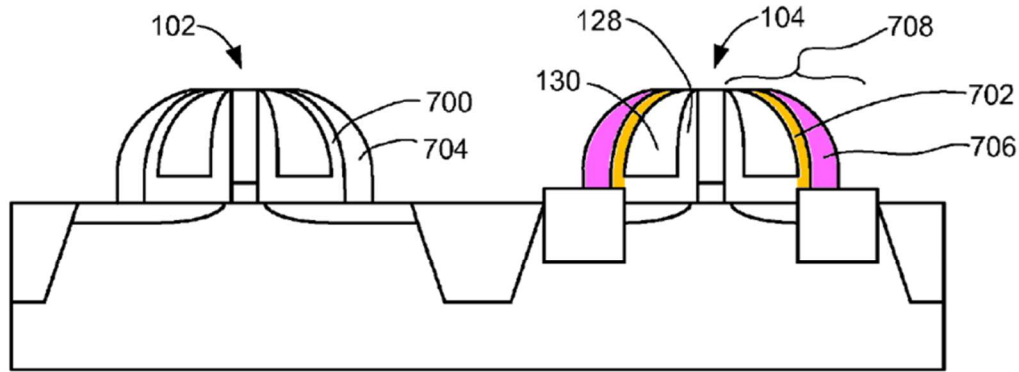


FIG. 7

Chong, Fig. 7

Otherwise, if Chong's liner 702 and spacer 706 are deposited after Okuno's second photoetching process, the two dielectric layers would cover the transverse edges, contrary to Okuno's explicit teaching. Ex-1003, ¶122. Thus, consistent with Okuno's teaching, a POSITA would have deposited the liner 702 and spacer 706 on Chong's PFET gate 122 before performing the second photoetching process. *Id.*

Performing the gate separation after the deposition of the liner 702 and spacer 706 would have yielded predictable benefits. Ex-1003, ¶123. Chong discloses implanting impurities in the NFET source/drain 900 after the formation of the liner 702 and spacer 706 and protecting the PFET with a mask 904 during this implant step. Ex-1007, [0057], Fig. 9. In view of Okuno's teaching, a POSITA would have understood that performing gate separation last (i.e., after the formation of the liner 702 and spacer 706 and the NFET source/drain implant step) would protect Chong's NFET device 102 from the source/drain implantation and increase the symmetry of

the impurity characteristics, resulting in stable operating characteristics. Ex-1003, ¶123.

The size reduction benefit of leaving no spacer material on the cut edges further supports that it was obvious to separate the gates after the liner 702 and spacer 706 are deposited. Ex-1003, ¶124. Chong, like Okuno, seeks to achieve “[s]ize reduction.” Ex-1007, [0004]; Ex-1004, [0004]. Cutting the gates after the liner 702 and spacer 706 are deposited would leave no spacers on the cut edges, allowing the gates to be packed more closely together and enable size reduction. Ex-1003, ¶124.

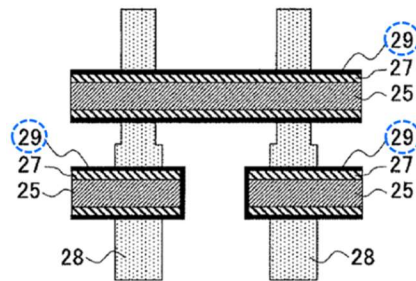
(c) Adding thin sidewall spacers after gate separation to prevent silicide corrosion

After the gate structures are separated by a photoetch process, a POSITA would have been motivated to form thin sidewalls around the gate structures to protect the gate structures from silicide corrosion, as Okuno teaches. Ex-1003, ¶125.

Chong contemplates forming additional spacers. Ex-1007, [0027] (“encompass[ing] a differential spacer design that is not distinguished by the number of spacers”). Although Chong’s PFET configuration is discussed with “a first spacer and a second spacer,” its invention “may encompass ... a design with more than two spacers.” *Id.*

Okuno provides an example of a MOS device having multiple spacers, e.g., one above extension implantation 27 and another optional spacer 29 for silicide protection. Ex-1004, [0041], [0036], Figs. 6D, 7E. Ex-1003, ¶127. For example,

Okuno discloses an embodiment in which, after gate separation, a CVD oxide film is optionally deposited and patterned to form **thin sidewalls 29** on the cut edges. Ex-1004, [0036], Fig. 7E. The thin sidewalls “cover the gate edges 25a of the gate electrodes 25 exposed after the cut and separation process.” *Id.*, [0036]. Okuno explains the rationale for adding the optional CVD oxide film and the thin sidewalls: “silicide may eat away in the lateral direction ... from cut gate edges 25a” during a subsequent silicide process, and the thin sidewall prevents “the silicide corrosion from the gate edges 25a.” *Id.*, [0035]-[0036].



Okuno, Fig. 7E

Chong’s device, as modified in view of Okuno (illustrated below), includes an **additional layer of spacers** (e.g., Okuno’s thin sidewalls 29). Ex-1003, ¶128.

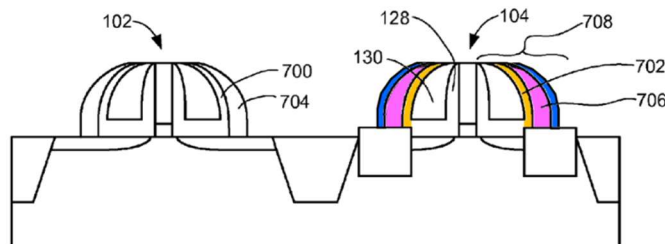


FIG. 7

Chong, Fig. 7 (Modified)

As Okuno teaches, forming a dielectric layer after gate separation would leave spacers on the cut edges, protecting the gate edges 25a from the subsequent silicide process. Ex-1003, ¶128.

A POSITA would have predicted success in forming the thin sidewalls 29 in the Chong-Okuno combination because Okuno teaches that the thin sidewalls can be formed using well-known dielectric material based on a conventional deposition technique (e.g., a CVD oxide film having a width of about 5 nm to 20 nm). Ex-1004, [0036]; Ex-1003, ¶129.

Further, in forming the thin sidewalls 29, it would be obvious to pattern (i.e., etch back) Chong's differential spacers 708 (comprising liner 702 and spacer 706) either before or together with Okuno's thin CVD film. Both options would have been obvious to try. Ex-1003, ¶130. "When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 402-03. In *Uber Techs., Inc. v. X One, Inc.*, for example, the Federal Circuit found that, because there are "only two possible methods" to display a map with plotted locations (server-side plotting and terminal-side plotting), a POSITA had good reason to pursue both. 957 F.3d 1334, 1339 (Fed. Cir. 2020); *see also Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d

1324, 1331 (Fed. Cir. 2009) (finding the claimed methods obvious when there are only three potential solutions to solve the problem).

Here, Chong discloses forming the differential spacers 708 by blanket deposition followed by a subsequent etch back (Ex-1007, [0049]), and there are two known options for sequencing the etch back of Chong's differential spacers 708 with the patterning of an additional dielectric layer (e.g., Okuno's thin CVD film): the differential spacers 708 can be patterned before or together with the additional dielectric layer. Ex-1003, ¶131. Both Okuno and Chong disclose that dielectric layers can be patterned using a conventional technique such as RIE. Ex-1004, [0034]; Ex-1007, [0053]; Ex-1003, ¶131. The '473 Patent also admits that forming spacers on the sidewall of a gate was a conventional technique. Ex-1001, 1:26-42. Using a conventional technique, a POSITA would have tried patterning the differential spacers 708 either before or simultaneously with an additional dielectric layer (e.g., Okuno's thin CVD film). Ex-1003, ¶131. The etching sequence would not have affected the purpose for which the dielectric layers are deposited, i.e., serving as spacers and providing protection for the gate structures. *Id.* Whether differential spacers 708 are patterned before or together with the additional dielectric layer (e.g., Okuno's CVD oxide film), the end product would have been the same: the device would have (1) spacers comprising only the additional dielectric layer in

the cut edges and (2) spacers comprising both the additional dielectric layer and the differential spacers 708 in the remaining edges. Ex-1003, ¶131.

3. Claim 1

(a) 1[pre]: “A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:”

To the extent the preamble is limiting, Chong discloses 1[pre] by disclosing methods for forming NFET and PFET devices with differential spacers. *See* Ex-1007, [0003], [0009], [0026]. In Fig. 1, the PFET device 104, for example, is a MOS transistor. *Id.*, [0029], Fig. 1; Ex-1003, ¶132.

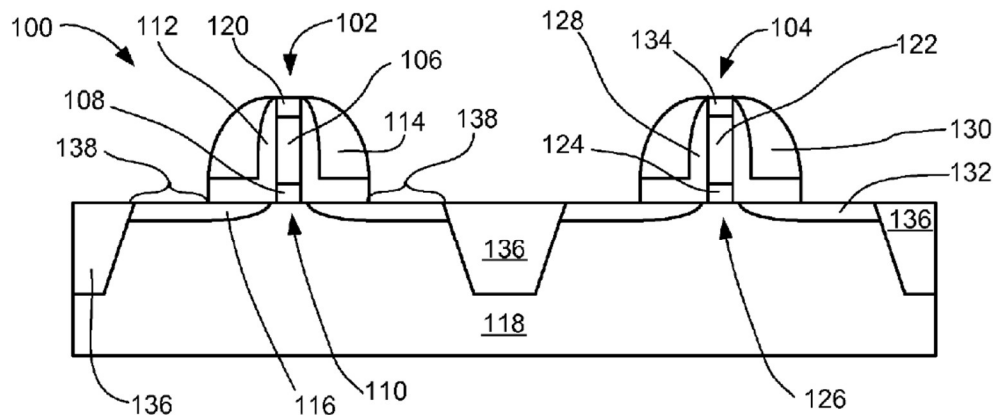


FIG. 1
Chong, Fig. 1

(b) 1[a]: “providing a semiconductor substrate;”

Chong discloses 1[a] by fabricating MOSFET on a semiconductor substrate, such as a substrate 118 that may include “a bulk semiconductor substrate.” *See* Ex-1007, [0003], [0031], [0034], Fig. 1; Ex-1003, ¶133.

(c) 1[b]: “forming a silicon layer on the semiconductor substrate;”

Chong discloses 1[b] by depositing a **PFET gate 122** (“silicon layer”) over a PFET gate oxide 124 on the semiconductor substrate, consistent with the ’473 Patent. Ex-1007, [0031]; Ex-1001, 2:42-47, 2:55-61 (explaining that “a polysilicon layer” is formed on a “gate insulating layer” that is “deposited on the surface of the semiconductor substrate 12”); Ex-1003, ¶134. Chong’s PFET gate 122 may include “silicon [or] polysilicon.” Ex-1007, [0032], Fig. 1.

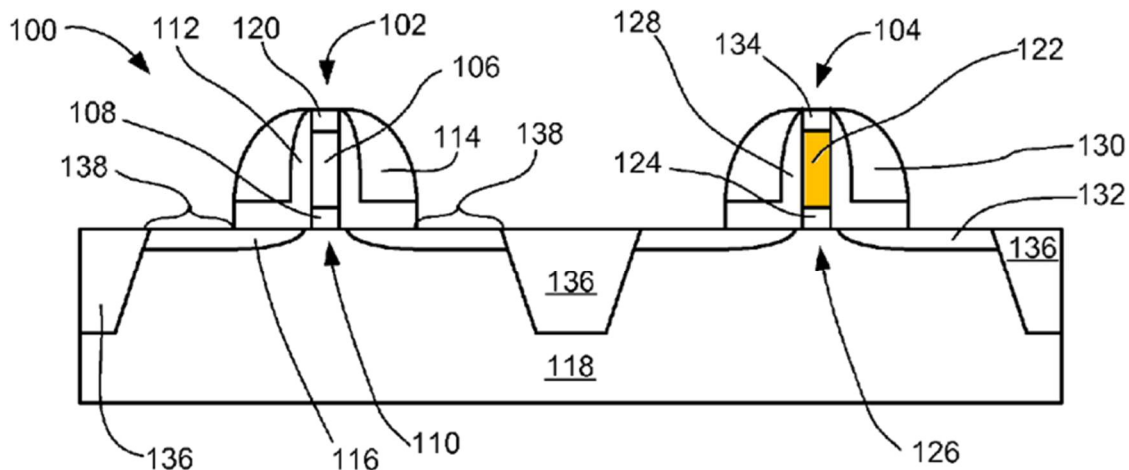


FIG. 1
Chong, Fig. 1

(d) 1[c]: “performing a first photo-etching process on the silicon layer for forming a gate pattern;”

Chong discloses 1[c] by performing patterning, photolithography, and etching to form a gate pattern comprising a PFET gate 122, PFET cap 134, and PFET gate oxide 124. Ex-1007, [0029] (“conventional deposition, patterning, photolithography, and etching” are used to form a PFET device 104); [0030], [0031],

Fig. 1. Ex-1003, ¶135. Photolithography entails applying a photoresist on a wafer, placing a mask with predetermined patterns over the wafer, and etching away the exposed portions of the photoresist and the underlying structure. Ex-1012, [0003], [0025]-[0026]; §II.E. To etch away undesired portions to form the PFET gate 122 and PFET cap 134, a POSITA would recognize, or at least found it obvious, that a photoetching process is performed. Ex-1003, ¶135. The '473 Patent admits that using a photo-etching process “to pattern the polysilicon layer and the hard mask into a gate” is a “[c]onventional approach.” Ex-1001, 1:28-36.

(e) 1[d]: “forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and”

Chong discloses 1[d] by forming recesses 400 in the semiconductor substrate 118 adjacent to two sides of the gate structure. Ex-1007, [0038] (“formation of a PFET recess 400 in the substrate 118”); Ex-1003, ¶136. Within the recesses 400, a punch-through suppression layer 500 may be formed from “epitaxially grown silicon germanium” to induce strain within the channel. Ex-1007, [0040]-[0044].

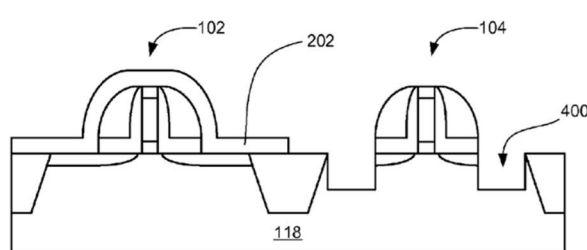


FIG. 4

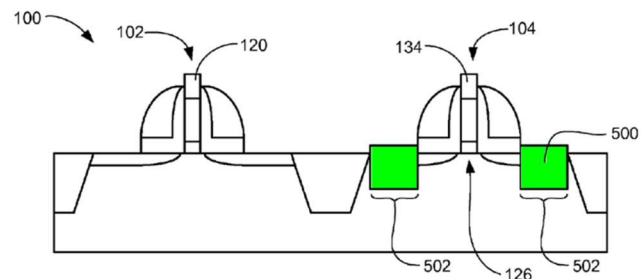


FIG. 5

Chong, Figs. 4-5

- (f) 1[e]: “after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.”

Chong and Okuno render 1[e] obvious. In Chong-Okuno, after the punch-through suppression layer 500 is epitaxially grown to form the PFET source/drain regions (Ex-1007, [0040]-[0044]) and after the NFET source/drain implant is complete (*id.* [0055]-[0057]), a second photoetching would be performed to separate the gates, as Okuno teaches. Ex-1004, [0026], [0034], Figs. 7C, 7D; §VI.B.2(a). The photoetching process is performed “while using the gate pattern to physically separate the gate pattern into two gates” because it is performed “to obtain gate structures cut and separated in predetermined shapes.” *Id.*, [0035]. And as shown in Okuno’s Fig. 7D, the cut portions between the gate electrodes 25 “form a slot in the gate pattern.” Ex-1003, ¶137.

FIG.7C

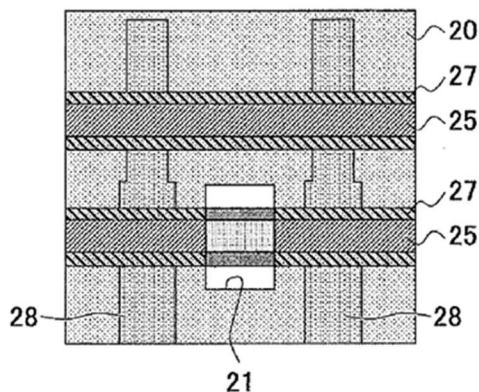
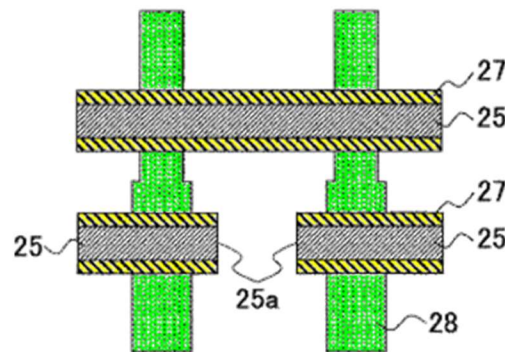


FIG.7D



Okuno, Figs. 7C-7D

4. Claim 2. “The method of claim 1, wherein after forming the silicon layer comprises:”

Chong and Okuno render claim 2 obvious by performing the following steps after forming the silicon layer.

(a) 2[a] “forming a hard mask on the silicon layer;”

Chong discloses 2[a] by forming a PFET cap 134, such as a nitride or an oxynitride cap, on the silicon layer 128. Ex-1007, [0031].

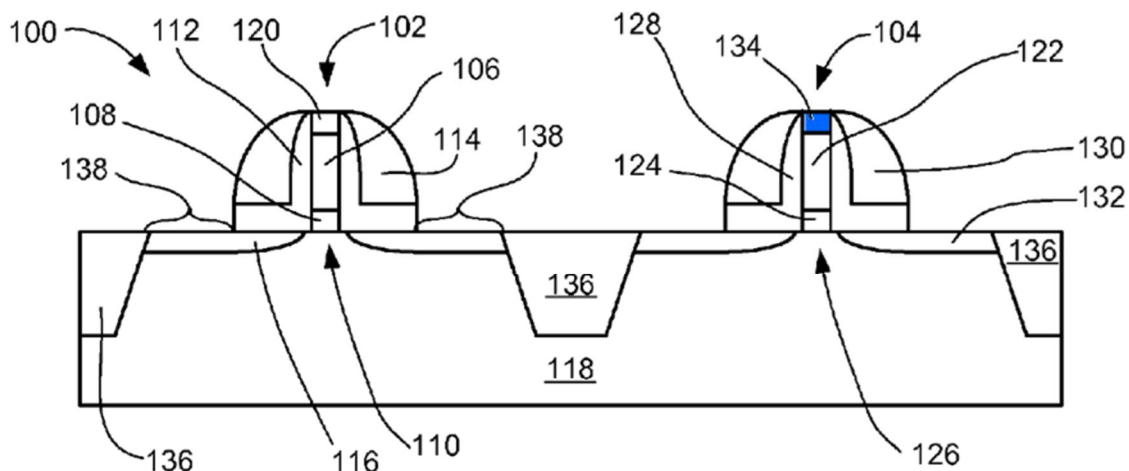


FIG. 1
Chong, Fig. 1

Chong’s PFET cap 134 is a “hard mask” because it is a cap layer intended to “help[] to protect the PFET gate 122 during subsequent processing steps,” consistent with the ’473 patent. *Id.*; Ex-1003, ¶140. As the ’473 patent explains, “the hard mask could be selected from a material consisting of SiO₂, silicon nitride, and SiON.” Ex-1001, 2:47-49.

(b) 2[b] “performing the first photo-etching process on the hard mask and the silicon layer for forming the gate pattern;”

Chong discloses 2[b] by performing the first photo-etching process on the gate structure comprising a PFET cap 134, PFET gate 122, and PFET gate oxide 124 to form the gate pattern, as discussed for 1[c]. Ex-1007, [0029], [0031]; Ex-1003, ¶141; §VI.B.3(d).

(c) 2[c] “forming a first spacer around the gate pattern;”

Chong discloses 2[c] by forming a first liner 128 and a first spacer 130 surrounding the gate 122. Ex-1007, [0031], Fig. 1.

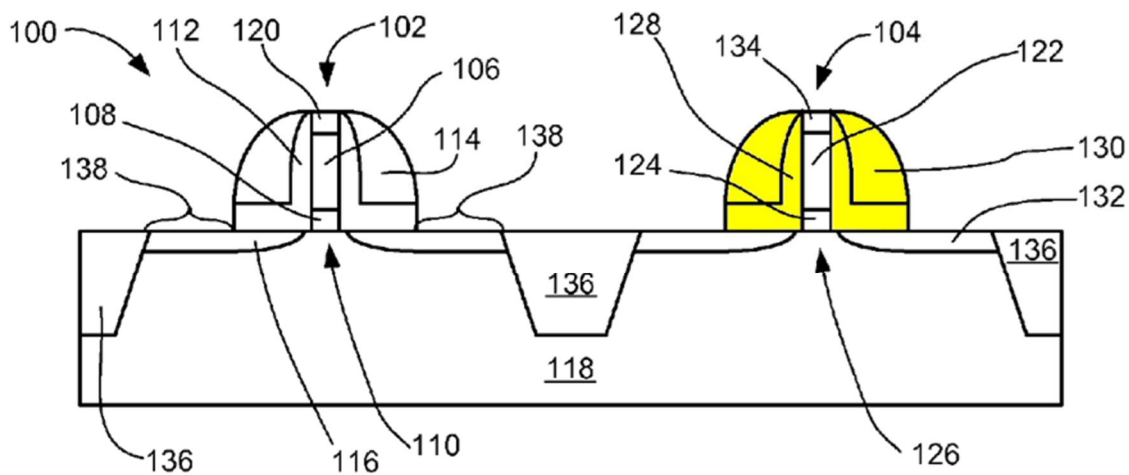


FIG. 1
Chong, Fig. 1

In Chong, the first liner 128 and first spacer 130, individually and collectively, are the “first spacer” formed around the gate pattern. Ex-1003, ¶143.

(d) **2[d] “forming a lightly doped drain in the semiconductor substrate adjacent to two sides of the gate pattern;”**

Chong discloses 2[d] by forming, adjacent to two sides of the gate structure, a source and drain extension 132 (the “lightly doped drain”) by “a low to medium-dose implant” to “facilitate dimensional reductions for the scaling of the” MOSFETs. Ex-1007, [0031].

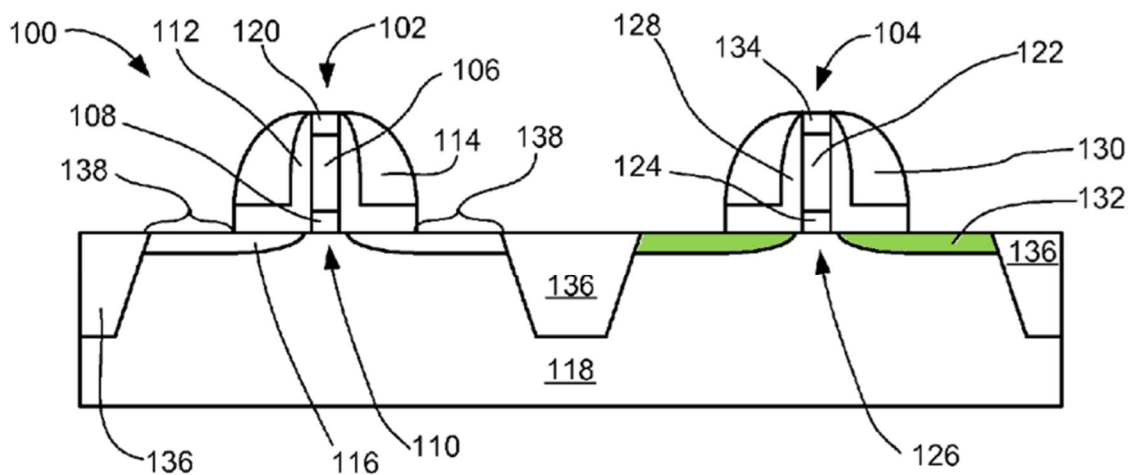


FIG. 1
Chong Fig. 1

A POSITA reading Chong would have understood that the source and drain extension (SDE) is a lightly doped drain. Ex-1040, 1:46-51 (“the source/drain extension (SDE) regions (formerly known as lightly doped drain or LDD regions)”); Ex-1041, [0017] (“[L]ightly-doped source/drain (LDD) regions 22, also commonly known as source/drain extension (SDE) regions 22, is formed.”); Ex-1034, 4:14-23, Fig. 1; Ex-1035, [0021]; Ex-1031, [0007]; Ex-1003, ¶145; §II.B.

(e) **2[e] “forming at least a recess in the semiconductor substrate adjacent to two sides of the first spacer;”**

Chong discloses 2[e] by selectively etching portions of the substrate 118 adjacent to the first liner 128 and spacer 130 (“the first spacer”) for forming recesses 400 in the substrate 118. Ex-1007, [0038], Fig. 4; Ex-1003, ¶146.

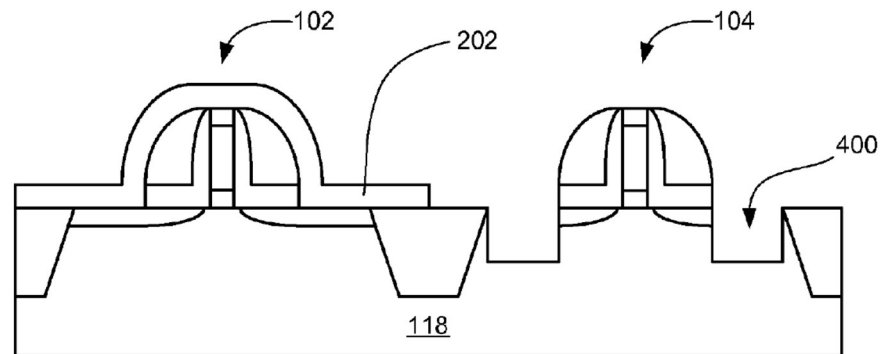


FIG. 4

Chong Fig. 4

(f) 2[f] “forming the epitaxial layer in the recess;”

Chong discloses 2[f] by forming, within the recesses, a punch-through suppression layer 500 using “epitaxially grown silicon germanium” to induce strain within the PFET channel 126. Ex-1007, [0040]-[0044]; §VI.B.3(e); Ex-1003, ¶147.

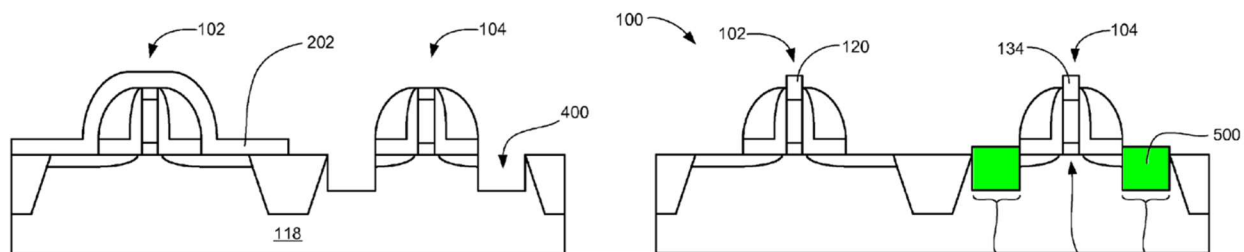


FIG. 4

FIG. 5

Chong, Figs. 4-5

(g) 2[g] “removing the hard mask disposed on the silicon layer;”

Chong discloses 2[g] by removing the PFET cap 134 (the “hard mask,” as discussed in §VI.B.4(a)). Ex-1007, [0047] (“The NFET cap 120, of FIG. 5, and the PFET cap 134, of FIG. 5, have been removed”), Fig. 6; Ex-1003, ¶148.

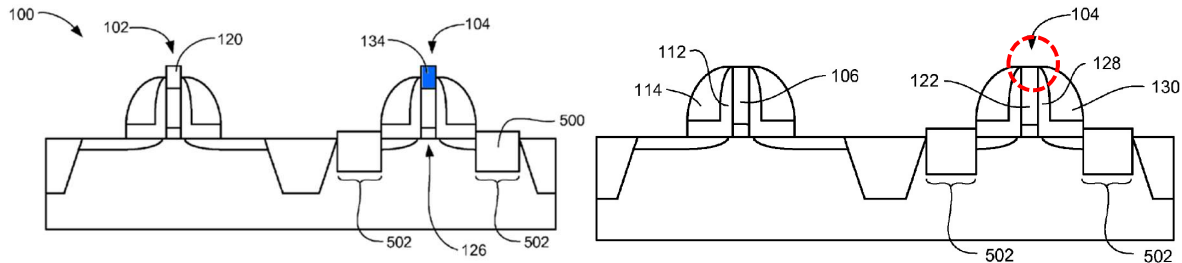


FIG. 5

FIG. 6

Chong, Fig. 5 (with hard mask) and 6 (hard mask removed)

(h) 2[h] “forming a first dielectric layer on the semiconductor substrate while covering the gate pattern;”

Chong discloses 2[h] by disclosing blanket deposition of “a dielectric material, such as a low temperature oxide” for a PFET second liner 702 and a subsequent blanket deposition of “a dielectric material, such as a nitride” for a second PFET spacer 706. Ex-1007, [0049]-[0050], [0052]; Ex-1003, ¶149.

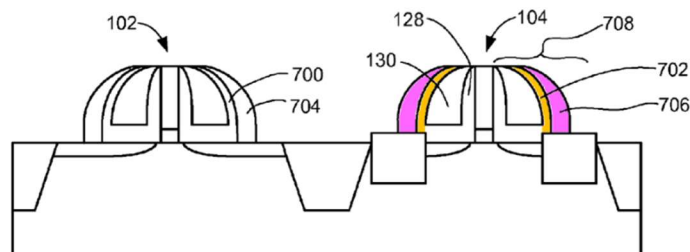


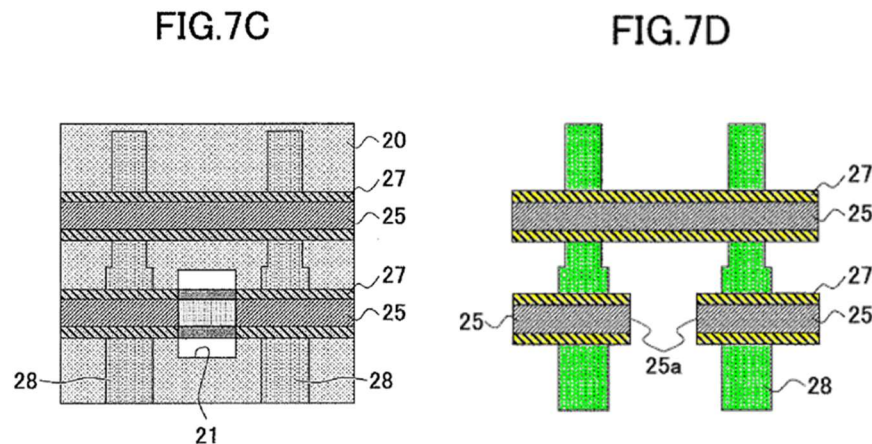
FIG. 7

Chong, Fig. 7

The deposited liner 702 and spacer 706 may be a dielectric material such as an oxide and nitride, respectively. *Id.*, [0052]. The liner 702 and spacer 706, collectively or individually, are thus a “first dielectric layer.” Ex-1003, ¶150. And because they may be formed over the PFET device 104 “by blanket deposition followed by a subsequent etch back” (*id.*, [0049]-[0050]), the liner 702 and spacer 706 “cover[] the gate pattern,” as claimed. Ex-1003, ¶150.

- (i) **2[i] “performing the second photo-etching process on the gate pattern, the first spacer, and the first dielectric layer to form the slot in the gate pattern; and”**

Chong as modified by Okuno renders 2[i] obvious. As discussed for 1[e], Okuno’s gate cutting (“second photo-etching process”) is performed to separate the patterned gate strip into individual gates after the source/drain regions are formed. Ex-1004, [0026], [0034]; §VI.B.3(f).



Okuno, Figs. 7C-7D

Further, as discussed in Section VI.B.2(b), and as Okuno teaches, Chong’s gates would be separated at least after the materials for the liner 702 and spacer 706 (the

“first dielectric layer”) are deposited (e.g., by blanket depositions), so the subsequent etch back to form the differential spacer 708 will leave no spacers on the cut edges, as illustrated in Okuno, Fig. 7D.

Okuno’s second photo-etching process is thus performed on the gate 122 (the “gate pattern”), a first liner 128 and spacer 130 (the “first spacer”), and the liner 702 and spacer 706 (the “first dielectric layer”). Ex-1003, ¶152.

(j) 2[j] “removing a portion of the first dielectric layer for forming a second spacer.”

Chong and Okuno render 2[j] obvious. Chong discloses forming each of the **liner 702** and **spacer 706** by “blanket deposition followed by a subsequent etch back” to form a differential spacer 708. Ex-1007, [0048]-[0049], [0051], Fig. 7.

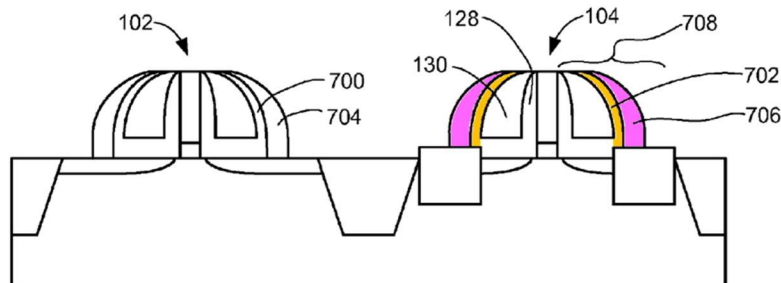


FIG. 7
Chong, Fig. 7

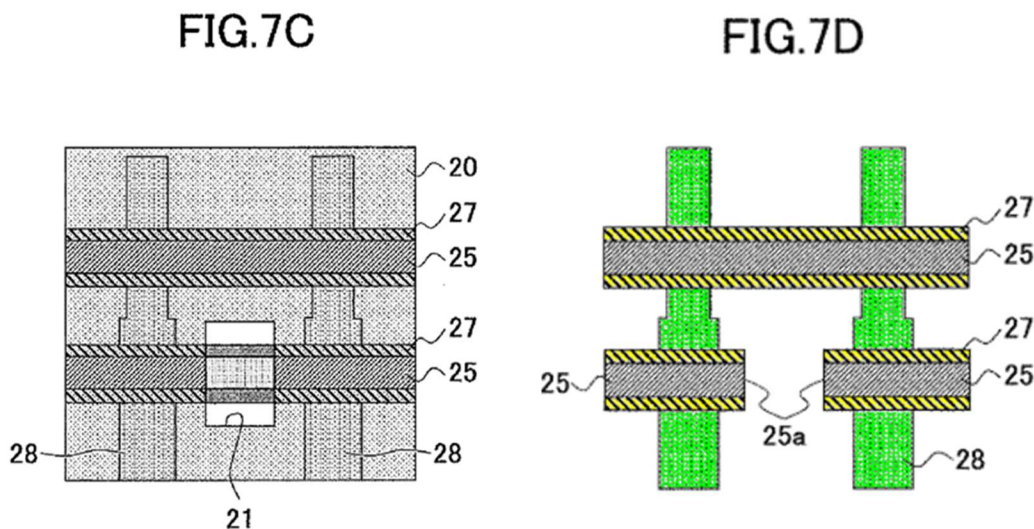
Because the “subsequent etch back” process removes at least a portion of **liner 702** and **spacer 706** for forming a differential spacer 708, Chong discloses “removing a portion of the first dielectric layer for forming a second spacer,” as claimed. Ex-1003, ¶154.

Chong-Okuno renders this limitation obvious regardless of whether the “second spacer” is formed before or after the “second photo-etching process” of 2[i]. “[A]s a general rule [a method] claim is not limited to performance of the steps in the order recited, unless the claim explicitly or implicitly requires a specific order.” *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1345 (Fed. Cir. 2008). Here, the claim do not require forming a second spacer after the second photo-etching process, and the two steps are not tied together in any way. *See Sunoco Partners Mktg. & Terminals L.P. v. U.S. Venture, Inc.*, 32 F.4th 1161, 1177 (Fed. Cir. 2022) (no sequence is required between two steps where “the claim language does not tie [the] two steps together”). Accordingly, Chong’s etching back the dielectric layers to form the second spacer (liner 702 and spacer 706) meets this limitation regardless of its sequence with respect to Okuno’s gate cut process.

Indeed, in the combination, Okuno’s gate cut would occur any time after depositing the dielectric materials. Ex-1003, ¶156. As Okuno explains, the gate cut ensures any “extending width of [the two spacers for] the pocket implantation and the extension implantation from the [cut-side] gate edges 25a is absent.” Ex-1004, [0041]; Ex-1003, ¶156. Thus, as long as the gate cut occurs after the deposition of the dielectric materials, Okuno’s goal would be met, regardless of whether Chong’s etch-back of the dielectric materials for forming the second spacer occurs before or after Okuno’s gate cut. Either sequence would have been obvious to try. Ex-1003,

¶156. Chong discloses a conventional method (e.g., “reactive ion etch”) by which the patterning could be performed. Ex-1007, [0053]. Forming the second spacer in one of the two available ways, i.e., before or after photoetching, using reactive ion etch would have been “the product not of innovation but of ordinary skill and common sense.” *KSR*, 550 U.S. at 403.

Should the Board find that the second spacer may be formed before the second photo-etching process, it would have been obvious to form Chong’s differential spacers 708 **before** performing Okuno’s gate cut process to leave the cut gate edges free of any sidewall spacers. *See* Ex-1004, Claim 1, [0035], Fig. 7D; *see also* [0041]; Ex-1003, ¶157.



Okuno, Figs. 7C-7D

Because Chong’s differential spacers 708 would first be formed along the gate length direction of the gate, Okuno’s gate cut process would cut the gate with the differential spacers so the differential spacers 708 are “absent from the intervening

regions between two opposing driver transistors” and “thus contributing to the size reduction of the cell structure.” Ex-1004, [0028]; Ex-1003, ¶158.

Alternatively, should the Board find that a second spacer must be formed after the second photo-etching process, Chong-Okuno renders this alternative obvious. Chong discloses that the differential spacers 708 are formed by blanket depositions of a dielectric material (such as an oxide) followed by another dielectric material (such as a nitride). It would have been obvious to use Chong’s nitride film “as an etching hard mask before the application of the resist” for Okuno’s gate cut. Ex-1004, [0034]. Under this alternative, a POSITA would have applied Okuno’s resist after Chong’s nitride film, as Okuno teaches. Ex-1004, [0034]; Ex-1003, ¶159. Once the etching is performed to cut the gate, the nitride film would then be removed along with the underlying oxide layer to form Chong’s differential spacers 708. Ex-1003, ¶159. Thus, even if Chong’s oxide/nitride layers are etched back to form the differential spacers *after* performing Okuno’s gate cut process, no spacers would be present in the cut gate edges. *Id.*

5. Claim 3. “The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.”

Chong and Okuno render claim 3 obvious. Chong discloses that the semiconductor substrate comprises isolation structure 136. Ex-1007, [0033]. As

Chong's Fig. 1 shows, the devices are isolated from each other by STIs 136;
Ex-1003, ¶160.

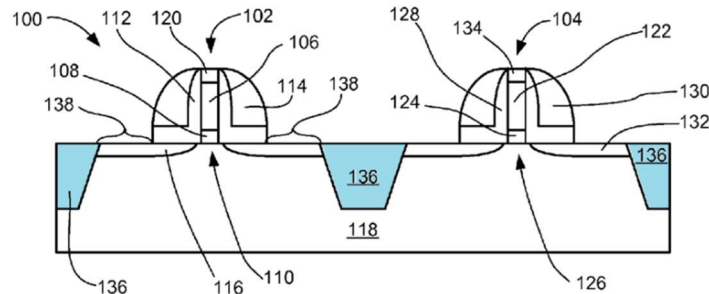
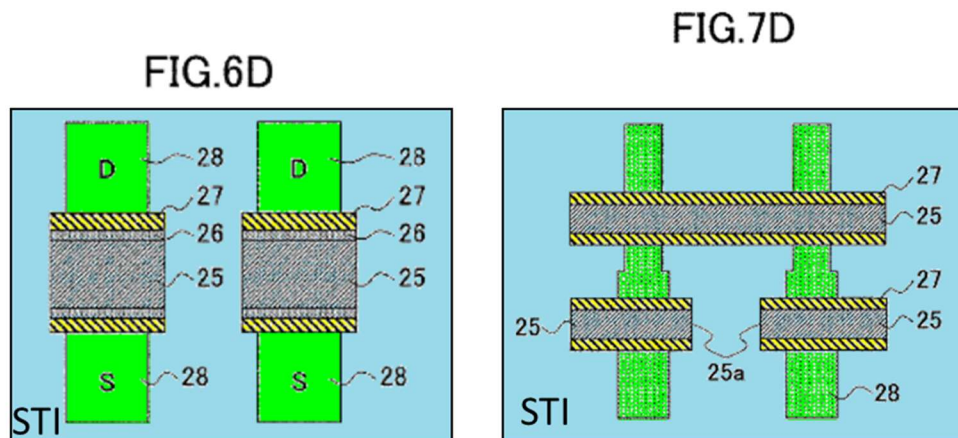


FIG. 1

Chong, Fig. 1

Okuno further discloses that its second photoetching process etches away the patterned polysilicon and gate oxide. Ex-1004, [0031], Figs. 6D, 7D; §VI.A.5.



Okuno, Figs. 6D and 7D (Modified)

A POSITA would have recognized that the second photoetching of Chong-Okuno is done by etching away portions of the gate 122 disposed on the STI structures 136. Ex-1003, ¶162. Indeed, portions of the gate 122 on the STI structures **must** be removed to form two or more separate gates electrically independent from each other, as Okuno's Figs. 6D and 7D show. *Id.*

6. Claim 4. “The method of claim 1, wherein the hard mask comprises silicon nitride.”

As discussed for 2[a], Chong discloses forming a PFET cap 134 (the “hard mask”) made of material “such as a nitride or an oxynitride cap.” Ex-1007, [0031], Fig. 3a; §VI.B.4(a).

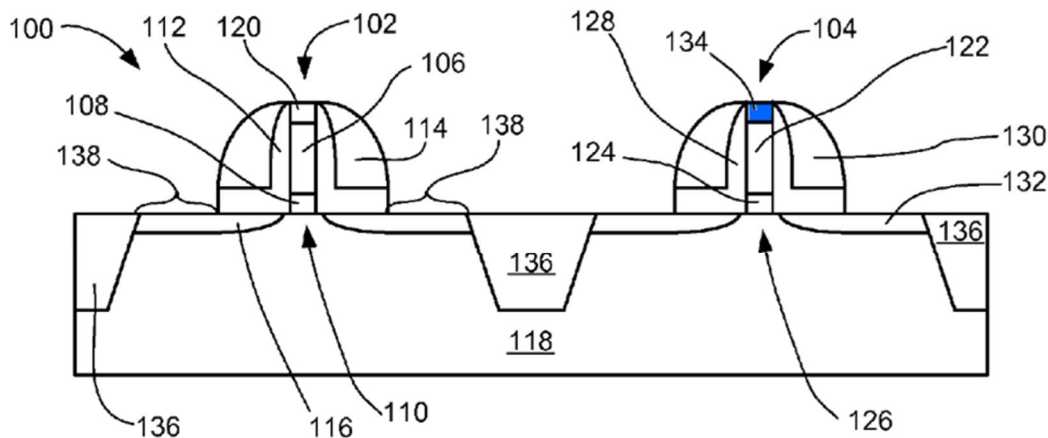


FIG. 1
Chong, Fig. 1

A POSITA would recognize the PFET cap 134 comprises silicon nitride. A “nitride” is a compound with the element nitrogen in the -3 oxidation state whereas an “oxide” is a binary compound of oxygen with another element. Ex-1003, ¶164. In semiconductor manufacturing, a POSITA would have understood that the other element of Chong’s “nitride” and “oxide” compounds is silicon. *Id.* Materials such as silicon nitride (Si_xN_y), silicon oxide (Si_xO_y), and silicon oxynitride (Si_xON_y) are used in semiconductor fabrication for their dielectric properties and are frequently referred to simply as nitride, oxide, and oxynitride, respectively. Ex-1036, [0024] (forming spacers with “composite oxide/nitride materials,” such as “silicon nitride”

and “silicon oxynitride”); Ex-1037, [0020] (a “nitride film” may include “silicon nitride” or “silicon oxynitride”); Ex-1038, [0056]. Chong also discloses using a nitride as a dielectric material. Ex-1007, [0052]. A POSITA would have understood that, consistent with the description of the ’473 Patent (Ex-1001, 2:47-49), Chong’s “nitride” layer is a “hard mask.” Ex-1007, [0031], [0052]; Ex-1003, ¶164.

7. Claim 5. “The method of claim 2, wherein the step of forming the first spacer comprises: forming a silicon oxide layer and a silicon nitride layer on the semiconductor substrate; and etching back the silicon oxide layer and the silicon nitride layer for forming the first spacer”

Chong discloses forming a first liner 128 and spacer 130, which individually and collectively are the “first spacer” formed around the gate pattern. Ex-1007, [0031], Fig. 1.

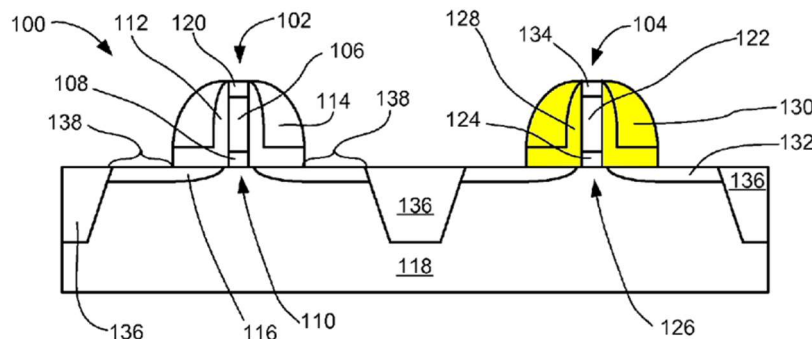


FIG. 1
Chong, Fig. 1

Chong’s first liner 128 and first spacer 138 may be made from a material that includes oxygen and nitrogen, respectively. *Id.*, [0031]; *see also* [0052] (disclosing formation of spacers from dielectric materials such as a “low temperature oxide deposited material” and “nitride”). As discussed for claim 4, a POSITA would have

understood that oxygen and nitrogen-containing materials include a “silicon oxide” and “silicon nitride,” respectively. Ex-1003, ¶166; Ex-1001, 2:39-41; Ex-1036, [0024]; Ex-1037, [0020]; Ex-1038, [0056]; §VI.B.6.

8. Claim 6. “The method of claim 2, wherein the first dielectric layer comprises a silicon oxide layer and a silicon nitride layer.”

Chong discloses that the liner 702 and spacer 706 (the “first dielectric layer”) may include an “oxide deposited material” and a “nitride,” respectively. Ex-1007, [0052]. As discussed for claim 4, “oxide deposited material” and “nitride” (Ex-1007, [0052]) include “silicon oxide” and “silicon nitride,” respectively. Ex-1003, ¶167; Ex-1001, 2:39-41; Ex-1036, [0024]; Ex-1037, [0020]; Ex-1038, [0056]; §VI.B.6. A POSITA would have recognized, or at least find obvious, that the liner 702 and spacer 706 are silicon oxide and silicon nitride, respectively. Ex-1003, ¶167.

9. Claim 7. “The method of claim 2, wherein after performing the second photo-etching process comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.”

Chong and Okuno render obvious claim 7. *First*, Chong discloses that “more than two spacers” may be formed in the PFET device other than the liner 702 and spacer 706 (the “first dielectric layer”). Ex-1007, [0027]. A POSITA would recognize that, to form additional spacers, another dielectric layer (a “second dielectric layer”) must be deposited and patterned. Ex-1003, ¶168; §VI.B.2(c).

Chong thus discloses “forming a second dielectric layer on the semiconductor substrate.”

Second, forming the second dielectric layer “after the second photo-etching process” would have been obvious in view of Okuno, which discloses that, after gate separation, a CVD oxide may be deposited to form thin sidewalls 29 that protect the cut edges 25a from a subsequent silicide process. Ex-1004, [0036]; Ex-1003, ¶169; §VI.B.2(c). Okuno’s thin CVD oxide sidewall spacer is an example of additional spacers contemplated by Chong. Ex-1007, [0027].

Third, Chong-Okuno discloses “removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.” As discussed in Section VI.B.2(c), in the alternative where Chong’s nitride film is used as a hard mask for the gate cut process, a POSITA would have etched back the second dielectric layer (Okuno’s thin sidewalls 29) with the first dielectric layer (liner 702 and spacer 706) to form the claimed second spacer. Ex-1003, ¶170.

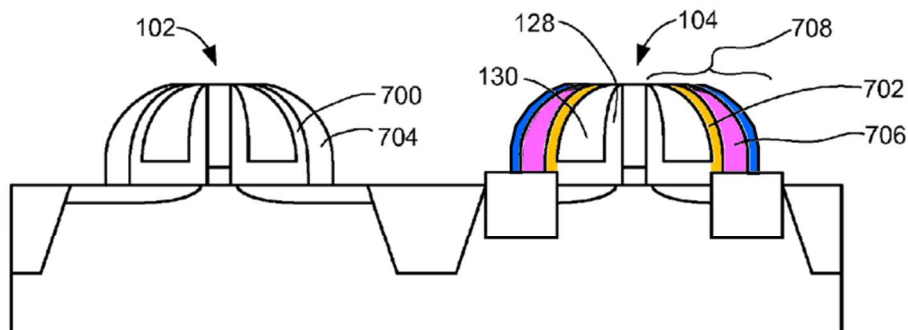
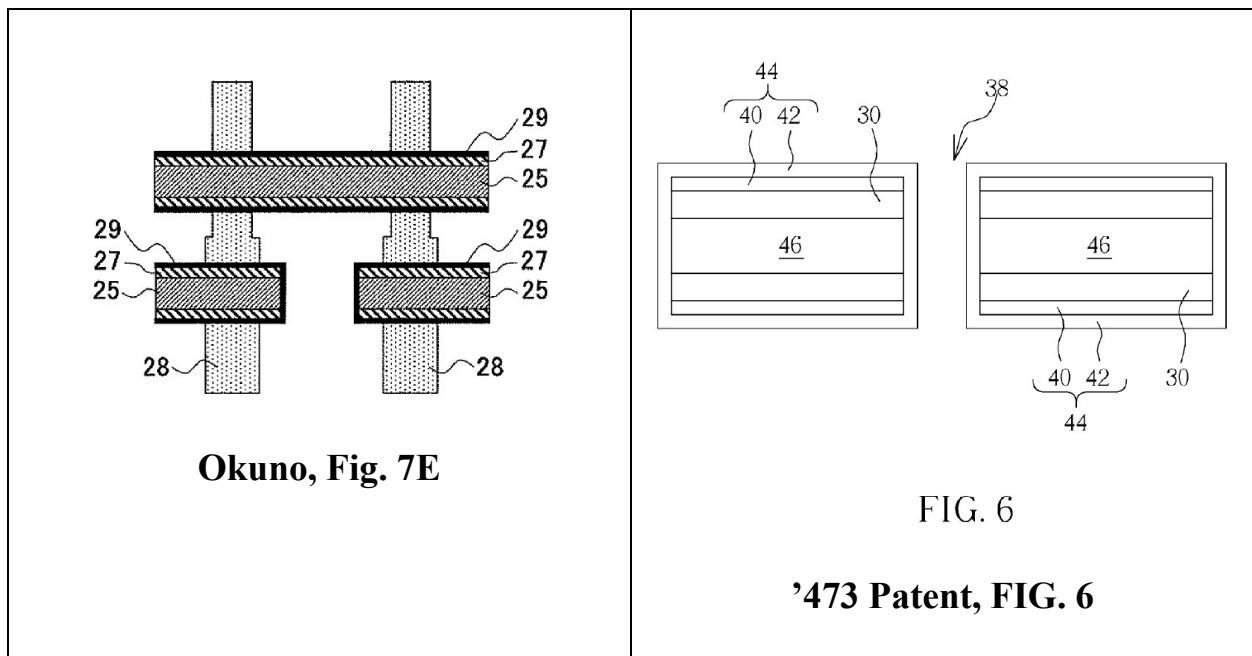


FIG. 7
Chong, Fig. 7 (Modified)

Patterning the two dielectric layers together (e.g., Okuno's CVD oxide film with Chong's liner 702 and spacer 706) after gate separation would result in the formation of a "second spacer." §VI.B.2(c); Ex-1003, ¶171. Because a portion of the first dielectric layer (within the cut slot) would have already been removed during Okuno's gate cut, the resulting "second spacer" would have the first dielectric layer (liner 702 and spacer 706) disposed on two opposite sidewall of the gate while the second dielectric layer (Okuno's thin sidewalls 29) formed on four sidewalls of the gate, consistent with the '473 Patent as illustrated below. Ex-1003, ¶172; Ex-1001, 4:37-55.



10. Claim 8. “The method of claim 7, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.”

Chong renders claim 8 obvious. In Chong-Okuno, liner 702 and/or spacer 706 (the “first dielectric layer”) are deposited before gate separation. Ex-1007, [0047]; §§VI.B.4(h)-4(i). As discussed for claim 6, the liner 702 may include an “oxide deposited material,” which a POSITA would have understood includes a silicon oxide. Ex-1003, ¶173; §VI.B.8. After the gate separation, as discussed for claim 7, it would have been obvious to form a “second dielectric layer” (e.g., Okuno’s CVD oxide) to protect the cut edges from silicide corrosion, as Okuno teaches. §VI.B.9; Ex-1003, ¶173.

It would also have been obvious to use a nitride film, in addition to an oxide film, for the “second dielectric layer.” Ex-1003, ¶174. Oxide and nitride have complementary chemical and material properties that allow them both to be used as alternating dielectric layers to protect the gate structures. Ex-1039, 0032; Ex-1038 at [0056]; Ex-1003, ¶174. Chong similarly discloses using both oxide and nitride films to form spacers. Ex-1007, [0031] (128 and 130), [0052] (702 and 706). The processes for depositing oxide and nitride films (e.g., CVD deposition) are well known. Ex-1003, ¶174; Ex-1004, [0035]-[0036]. A POSITA would have understood that using nitride, in addition to oxide, for the second dielectric layer would have

been nothing more than a routine modification that utilizes well-known materials and processes. Ex-1003, ¶174.

11. Claim 9. “The method of claim 2, wherein after forming the second spacer comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the second dielectric layer for forming a third spacer.”

As discussed for claim 7 (§VI.B.9), Chong discloses forming a second dielectric layer from which additional spacers may be formed (Ex-1007, [0027]), and Okuno provides a specific example of a second dielectric layer, namely a CVD oxide film (Ex-1004, [0036]). As discussed in Section VI.B.2(c), Okuno discloses patterning an additional dielectric layer (e.g., Okuno’s CVD oxide film) after gate separation, and in the alternative where Chong’s liner 702 and spacer 706 are made into a spacer before gate separation, the **liner 702** and **spacer 706** would form the “second spacer” while the additional dielectric layer forming a “third spacer” (e.g., Okuno’s **thin sidewalls 29**).

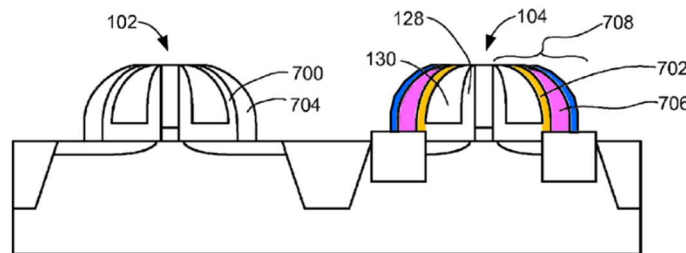
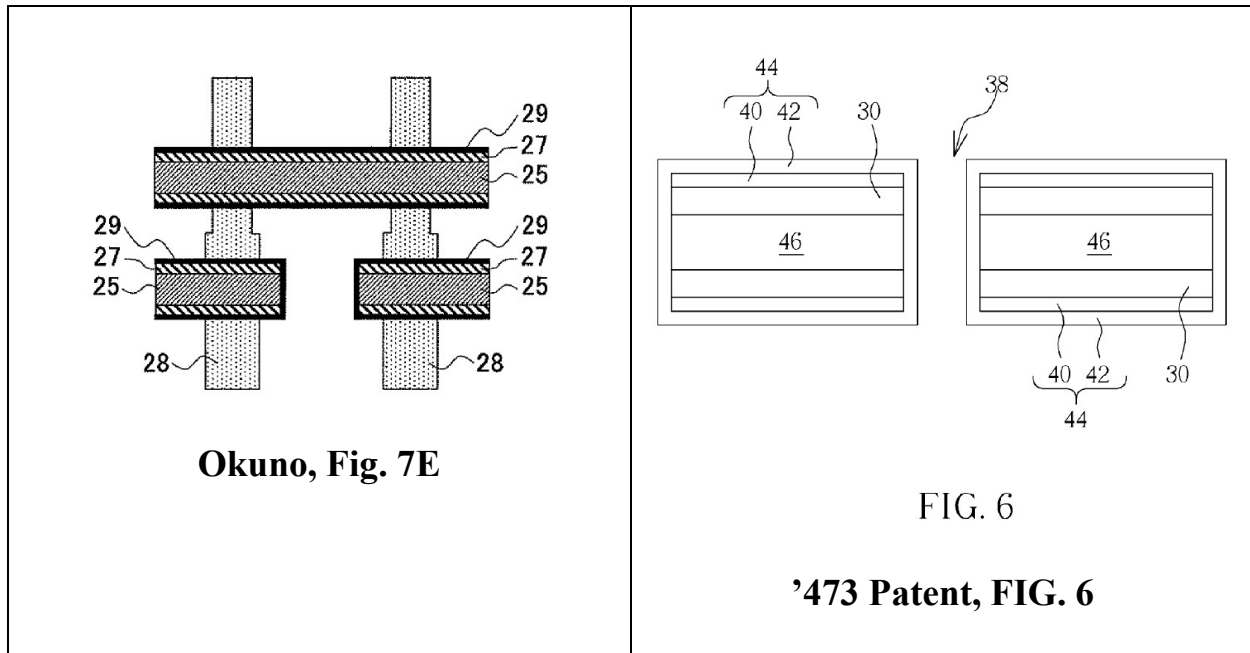


FIG. 7
Chong, Fig. 7 (Modified)

Because a portion of the first dielectric layer would have been removed during etch back to form the spacer, the resulting “second spacer” would be the first

dielectric layer (liner 702 and spacer 706) disposed on two opposite sidewall of the gate while the “third spacer” would have been Okuno’s thin sidewalls 29 that have been formed on four sidewalls of the gate, consistent with the ’473 Patent as illustrated below. Ex-1003, ¶176; Ex-1001, 4:37-55.



12. Claim 10. “The method of claim 9, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.”

Chong renders claim 10 obvious. Chong discloses that liner 702 (the “first dielectric layer”) may include an oxide deposited material such as silicon dioxide. Ex-1007, [0052]. As discussed with respect to claim 8, it would have been obvious to form the “second dielectric layer” by depositing and patterning both silicon oxide and silicon nitride layers after gate separation. *See* §VI.B.10; Ex-1003, ¶177.

C. Ground 3: Claims 1-3 are Obvious Over Mandelman and Shin

1. Mandelman (Ex-1005)

Because Mandelman is in the same field (MOSFETs) and reasonably pertinent to a problem the '473 Patent purports to address (MOSFET fabrication), Mandelman is analogous art. Ex-1001, 1:15-17; Ex-1005, [0003], [0005]; Ex-1003, ¶178.

Mandelman discloses the fabrication of MOS transistors, such as those used in an SRAM, noting that a “continuing objective of SRAM device designers is to more densely pack SRAM memory cells into a smaller integrated circuit,” and smaller geometries (e.g., below the 45 nm node) place “ever-greater demands on the photolithography techniques.” Ex-1005, [0006]-[0010].

In Mandelman, the substrate includes a bulk substrate 11 and STIs 20 formed to isolate active semiconductor regions from each other. *Id.*, [0029], Fig. 5B. A gate dielectric layer 22 is formed on a top surface of the active semiconductor regions 14. *Id.* **Conductor lines** (e.g., 40) are defined by a conventional photolithography and etching process. *Id.*, [0031], Fig. 2. Spacers (e.g., 50, 52) are formed on the sidewalls of conductor line 40 by etching layers of silicon nitride and silicon dioxide. *Id.*, [0033]. **Source/drain regions** are formed by an ion implantation process. *Id.*, [0034].

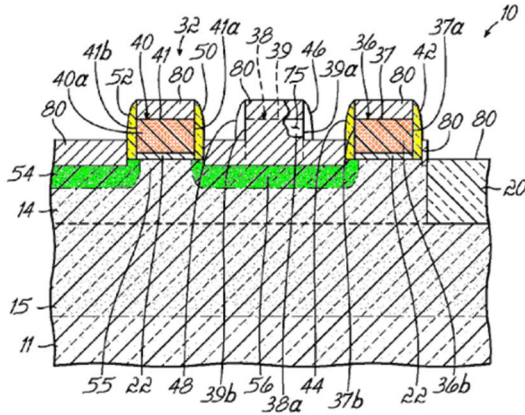


FIG. 5B

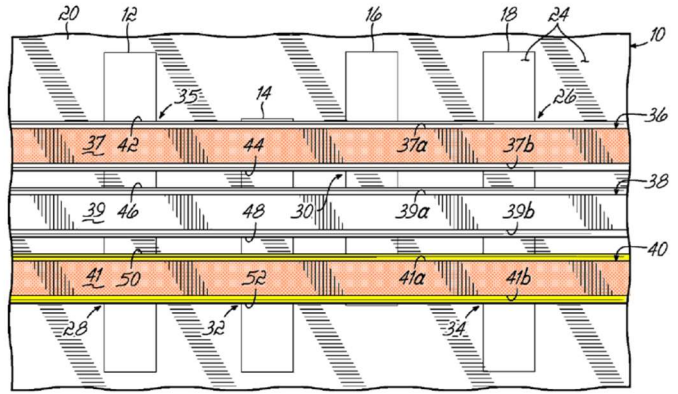


FIG. 2

Subsequently, a second photolithography process is performed to expose portions of the conductor lines 36, 38, and 40 and underlying gate dielectric layer 22. *Id.*, [0036]-[0038], Fig. 3. Segmented conductor lines (e.g., 40a) are therefore created. *Id.*, [0038]-[0039], Fig. 4.

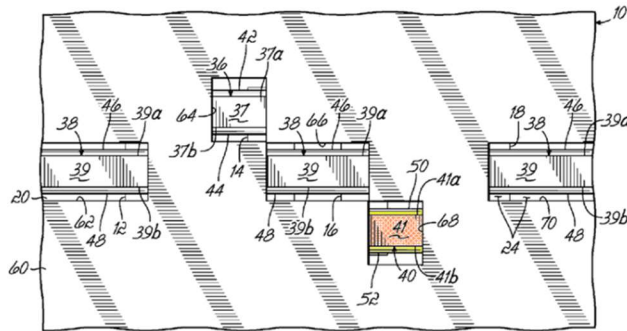


FIG. 3

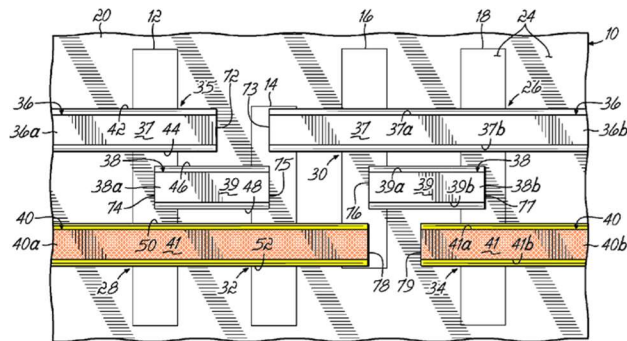


FIG. 4

2. Combining Mandelman and Shin

Mandelman and Shin disclose similar MOS transistors fabricated on a bulk substrate. Ex-1005, [0002]; Ex-1006, [0005]; Ex-1003, ¶181. Like Shin (*see* §VI.A.3), Mandelman discloses conventional elements of a MOS transistor such as STI and spacers. Ex-1005, [0029], [0033]. Further, both seek to solve similar problems related to miniaturization, with Mandelman providing an improved photolithography process suitable for smaller geometries (e.g., below the 45 nm node) (Ex-1005, [0006]-[0010]) and Shin seeking to overcome the short channel effect by forming epitaxial source/drain regions (Ex-1006, [0005]-[0006]).

A POSITA would have found it obvious to fabricate Mandelman's transistors using epitaxial source/drain regions, as Shin teaches, to add advantageous strain. Ex-1003, ¶182; Ex-1005, [0034]; Ex-1006, [0084]; Ex-1031, [0021]-[0026]; Ex-1033, [0044]. An epitaxial source/drain would introduce compressive or tensile stress in the source/drain well areas and increase carrier mobility. Ex-1030, 1:20-34, 3:43-52, 4:19-33; Ex-1006, [0084]; Ex-1031, [0010]; Ex-1003, ¶182; §II.C. Using epitaxial source/drain would enable Mandelman's device to have shorter channel length and higher drive current, furthering Mandelman's goal of increasing transistor density. Ex-1003, ¶182.

A POSITA would have had a reasonable expectation of success. Ex-1003, ¶183. Shin's SEG process would have been simply added after Mandelman's spacer

formation for source/drain formation. Ex-1006, [0038], [0090]; Ex-1005, [0033]-[0034]. After growing an epitaxial layer in the recesses, a POSITA would have proceeded with the remaining steps taught by Mandelman, such as segmenting of the conductor lines using a second photoetching process. Ex-1005, [0070]-[0071]; Ex-1003, ¶183.

The proposed combination is therefore an obvious example of (1) implementing a known technique (selectively growing an epitaxial layer) to improve known devices (MOS devices) to achieve predictable results (introducing mechanical stresses into the channel region to improve carrier mobility and overcoming the short channel effect); (2) a choice from a finite number of identified, predictable solutions (forming source/drain regions mainly through selective epitaxial growth and/or ion implantation); and (3) a teaching, suggestion, or motivation in the prior art (*see* Ex-1006, [0084]). *See KSR*, 550 U.S. at 416-21; Ex-1003, ¶184.

3. Claim 1

(a) 1[pre]

To the extent the preamble is limiting, Mandelman discloses 1[pre] by disclosing a method for fabricating a metal-oxide semiconductor (MOS) transistor. *See* Ex-1005, [0002], [0005], [0069]; Ex-1003, ¶185. Mandelman, for example, discloses MOS transistor 28, 32, and 34, each comprising a conductor line 40, gate

dielectric layer 22, and active semiconductor region 14. Ex-1005, [0030]-[0031], Figs. 4, 5B.

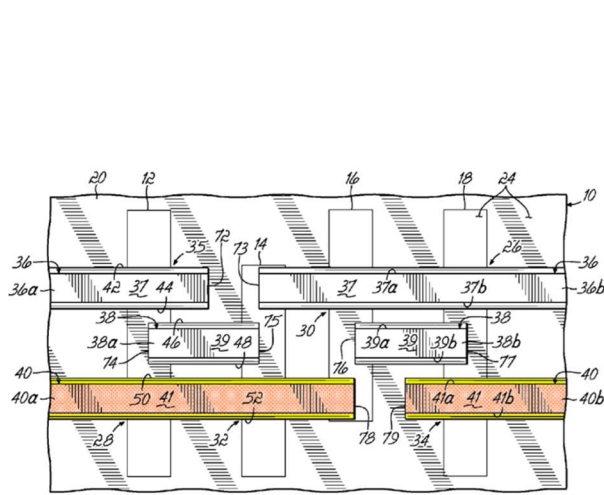


FIG. 4

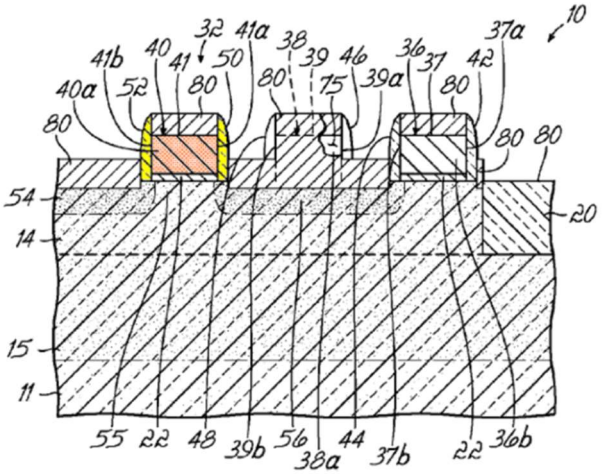


FIG. 5B

Mandelman, Figs. 4 and 5B

(b) 1[a]

Mandelman discloses 1[a] by providing a semiconductor substrate 10. Ex-1005, [0027]; Ex-1001, 2:35-37; Ex-1003, ¶187.

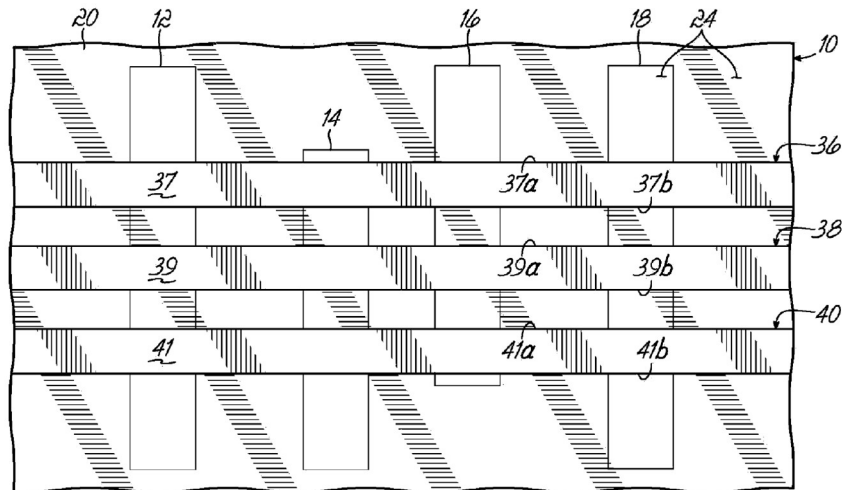


FIG. 1

Mandelman, Fig. 1

(c) 1[b]

Mandelman discloses 1[b] by depositing conductive material on the semiconductor substrate 10. Ex-1005, [0031]. Mandelman's conductive material is a "silicon-containing semiconductor material that primarily contains silicon, such as doped polycrystalline silicon (i.e., doped polysilicon)," consistent with the '473 Patent. *Id.*; Ex-1001, 2:42-47, 2:55-61; Ex-1003, ¶188.

(d) 1[c]

Mandelman discloses 1[c] by performing a first "conventional photolithography and etching process" to form conductor line 40 (the "gate pattern"). Ex-1005, [0031]. Mandelman discloses forming the conductor lines 40 by depositing conductive material in a layer on the gate dielectric layer 22, forming a resist layer that serves as an etch mask, and then etching to remove the exposed areas of the patterned resist layer. *Id.*; Ex-1003, ¶189.

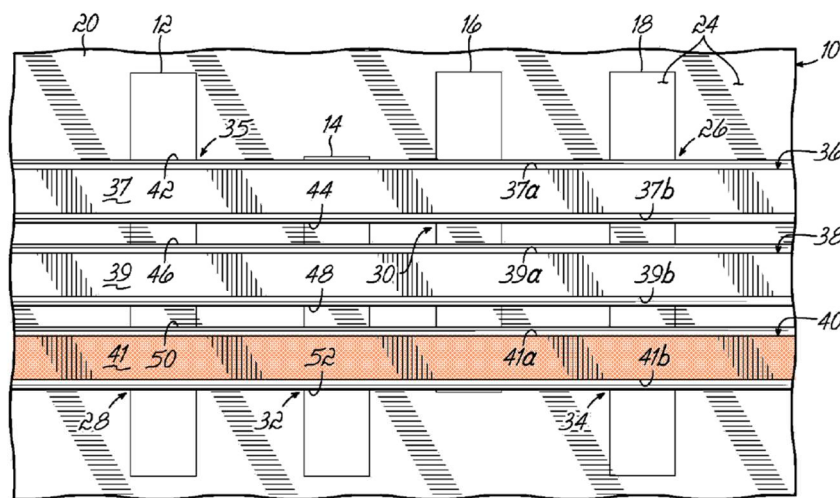


FIG. 2
Mandelman, Fig. 2

(e) 1[d]

As discussed in Section VI.D.1(a), it would have been obvious to add an epitaxial layer to Mandelman's device. Mandelman discloses forming **source/drain regions 54 and 56** adjacent two sides of the **conductor line 40**. Ex-1005, [0033]-[0034], Figs. 2, 5B; Ex-1003, ¶190.

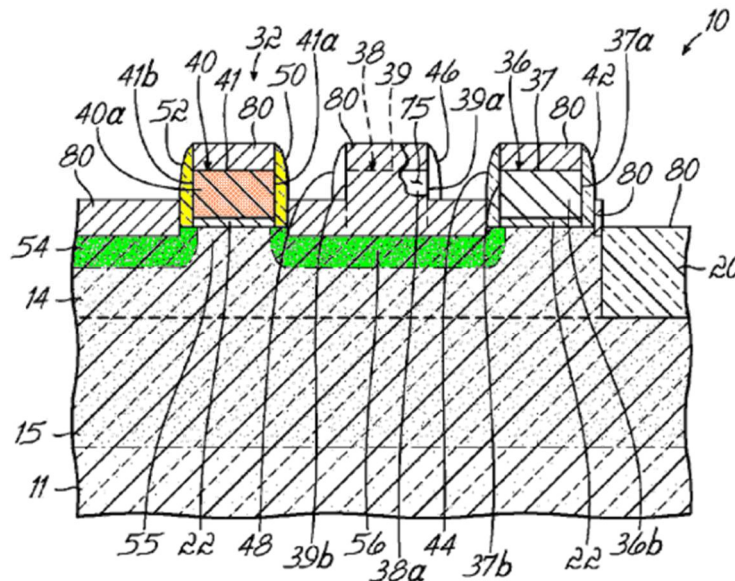


FIG. 5B

Mandelman Fig. 5B

In Mandelman-Shin, an epitaxial layer would be formed in the semiconductor region 10 adjacent to the two sides of the **conductor line 40**, as Shin teaches. §VI.D.1(a); Ex-1003, ¶191.

(f) 1[e]

After the spacers 50 and 52 and source/drain regions are formed, Mandelman discloses performing a second photolithography and etching process on the

conductor lines (“gate pattern”). Ex-1005, [0036]-[0038]; Ex-1003, ¶192. A photoresist layer 60 is applied to the substrate 10, and openings are printed using a “conventional photolithography process.” Ex-1005, [0036], Fig. 3. The exposed portions are then etched. *Id.*, [0037], Fig. 4.

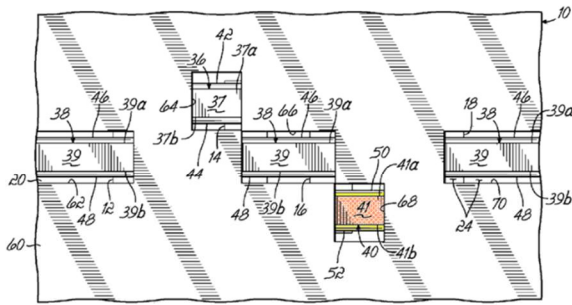


FIG. 3

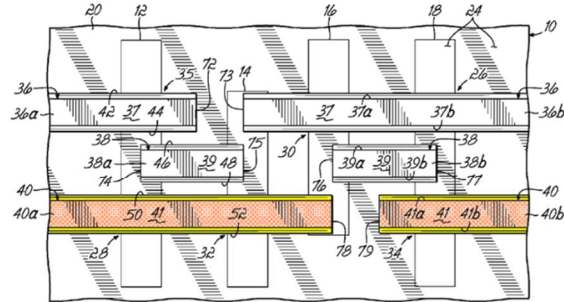


FIG. 4

Mandelman, Figs. 3-4

Because Mandelman discloses performing a second photoetching process after the source and drain regions are formed, in Mandelman-Shin, the second photoetching process would be performed after the formation of the epitaxial layer (which occurred during the source/drain formation). *See* §VI.C.3(e); Ex-1003, ¶193. Moreover, Mandelman’s photoetching process is performed “while using the gate pattern to physically separate the gate pattern into two gates” because it segments the conductor line 40 into segments 40a and 40b. *Id.* (Segment 40a constitutes gate of transistors 28 and 32 while segment 40b constitutes gate of transistor 34.). Ex-1003, ¶193. Lastly, as shown in Fig. 4, each of the cut portions between the segmented conductor lines “form a slot in the gate pattern.” *Id.*

4. Claim 3

Mandelman-Shin renders claim 3 obvious. Mandelman discloses the additional limitations of claim 3 because Mandelman's semiconductor substrate 10 comprises shallow trench isolation regions 20. Ex-1005, [0029] ("A gate dielectric layer 22 (FIG. 5B) is formed on a top surface 24 shared by the active semiconductor regions 12, 14, 16, 18 and shallow trench isolation regions 20."); Ex-1003, ¶195.

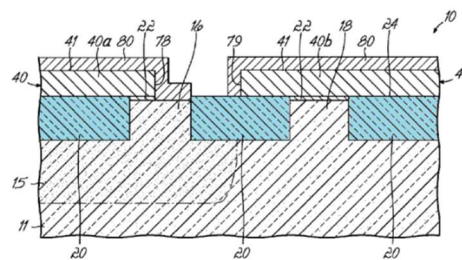


FIG. 5A

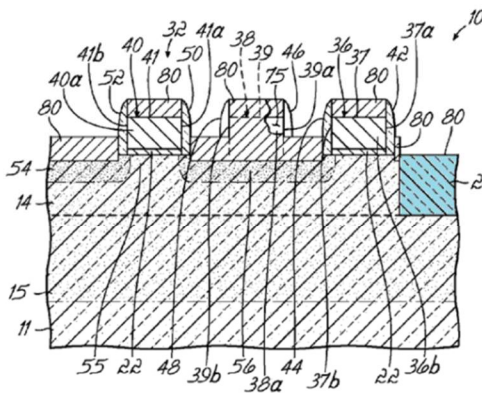


FIG. 5B

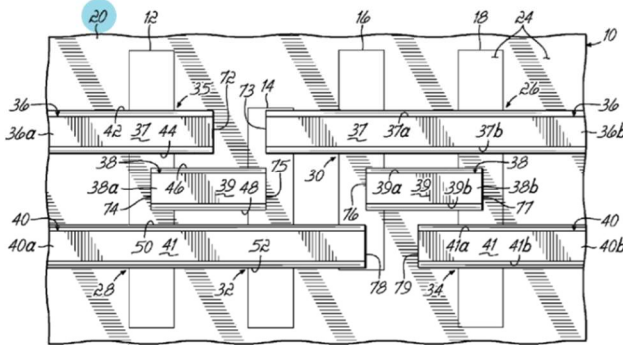


FIG. 4

Mandelman, Figs. 5A-B and 4

Mandelman also discloses that its second photoetching process segments the conductor line 40 into multiple segments (40a and 40b) by removing portions of the conductor line 40 and exposing the underlying shallow trench isolation regions 20. Ex-1005, [0037]-[0038]; Ex-1003, ¶196.

D. Ground 4: Claims 1-6 are Obvious Over Chong and Mandelman

1. Combining Chong and Mandelman

(a) A gate-cutting process to separate Chong's gate structures for miniaturization

Chong and Mandelman disclose similar MOS transistors fabricated on a bulk substrate. Ex-1005, [0002]; Ex-1007, [0003], [0009], [0026]; Ex-1003, ¶197. Both disclose common elements of a MOS transistors, including an STI and spacers. Ex-1005, [0029], [0033]; Ex-1007, [0033], [0031]. Further, Chong and Mandelman seek to solve problems related to miniaturization of transistors. Ex-1003, ¶197. Mandelman seeks to provide an improved photolithography process that meets the demands of smaller geometries (e.g., below the 45 nm node). Ex-1005, [0006]-[0010]. Chong seeks to mitigate unintended strain effects caused by size reduction. Ex-1007, [0004].

A POSITA would have found it obvious to photoetch and separate Chong's gate pattern into two gates, as Mandelman teaches. §VI.C.3(d); Ex-1004, [0032]; Ex-1005, [0036], [0038], Figs. 3-4; Ex-1026, 5:1-35; Ex-1012, [0025]-[0026]; §II.E; Ex-1003, ¶198. There are only finite options for patterning gates: patterning individual gate separately or cutting a single patterned gate strip into multiple gates. Ex-1003, ¶198. Gate cutting, applied to Chong's device, would predictably enable size reduction while maintaining control over the strain effects. *Id.*

(forming **source/drain regions 50 and 52** adjacent two sides of the **conductor line 40**), [0036]-[0037] (photoetch to cut the conductor line 40), Figs. 2, 5B.

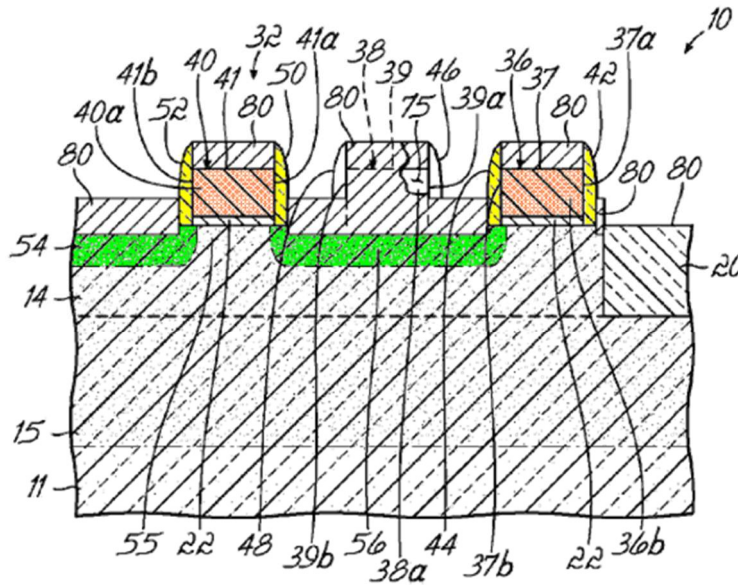


FIG. 5B

Mandelman Fig. 5B

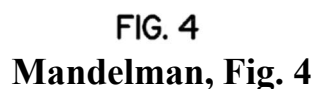
disclosures. Ex-1003, ¶200. Chong discloses forming an epitaxial layer early in the fabrication process by in-situ doping: before removing the hard mask 13, adjusting

the source/drain concentration with ion implantation, and forming dielectric layers (liner 702 and spacer 706). Ex-1007, [0044], [0047]-[0049], [0058]. If any of the steps for forming the source/drain regions (e.g., growing epitaxial layer and dopant implantation) is performed after the gate separation, it will cause the impurity characteristics below the gate electrode end portions to become asymmetrical, which a POSITA would have known to avoid. Ex-1004, [0027]; Ex-1003, ¶200. A POSITA would thus be motivated to perform Mandelman's second photoetching process after the completion of Chong's earlier steps, including the formation of the epitaxial layer. Ex-1003, ¶200.

A POSITA would have had a reasonable expectation of success. Ex-1003, ¶201. Mandelman discloses that gate separation can be done using a well-known technique, including a "conventional photolithography process" and anisotropic dry etching process such as RIE. Ex-1005, [0036]-[0037], Fig. 3. It would have been within a POSITA's expertise to use a conventional photoetch technique such as RIE (reactive ion etching) to separate the gate structures. Ex-1003, ¶201; Ex-1001, 1:28-42.

The combination is therefore an obvious example of (1) implementing a known technique (gate-cutting, through photoetching including the step such as RIE, after source drain formation) to improve known devices (MOS devices) to achieve predictable results (reduced transistor spacing, size reduction, and symmetrical

When combining Mandelman’s gate separation step with Chong, a POSITA would have been motivated to sequence the gate separation so that the cut edges are free of dielectric materials (the liner 702 and spacer 706). Ex-1003, ¶203. Mandelman expressly motivates leaving no dielectric spacers on the cut edges, such that sidewall spacers are not formed on the “transverse edges or ends defining sidewalls 72-79.” Ex-1005, [0039], [0046], Fig. 4. The direct contact establishes “electrically connective bridges,” which help simplify contacts and cell layouts. *Id.*, [0045].



When combining Mandelman and Chong, if Chong's liner 702 and spacer 706 are formed after the second photoetching process, the two dielectric layers would cover the transverse edges, which is contrary to Mandelman's explicit teaching. Ex-1003, ¶204. Thus, consistent with Mandelman's disclosures, a POSITA would have deposited the liner 702 and spacer 706 on Chong's PFET gate 122 before performing Mandelman's second photoetching process. *Id.*

Performing the gate separation after the formation of the liner 702 and spacer 706 would have yielded predictable benefits. Ex-1003, ¶205. Chong discloses implanting impurities in the NFET source/drain 900 after the formation of the liner 702 and spacer 706 and protecting the PFET with a mask 904 during this implant step. Ex-1007, [0057], Fig. 9. In view of Mandelman's teaching, a POSITA would have understood that performing gate separation last (i.e., after the formation of the liner 702 and spacer 706 and the NFET source/drain implant step) would protect Chong's NFET device 102 from the source/drain implant step and increase the symmetry of the impurity characteristics, result in stable operating characteristics. Ex-1003, ¶205.

The size reduction benefit of leaving no spacers on the cut edges further supports that it was obvious to separate the gates after the liner 702 and spacer 706 are formed. Chong, like Mandelman, seeks achieve "[s]ize reduction." Ex-1007, [0004]; Ex-1005, [0006]. Cutting the gates after the liner 702 and spacer 706 are

formed would leave no spacers on the cut edges, allowing the gates to be packed more closely together and enable size reduction. Ex-1003, ¶206.

2. Claim 1

(a) 1[pre]–[d]

Chong discloses 1[pre] through 1[d] as discussed for Ground 2. §§VI.C.3(a)–C.3(e).

(b) 1[e]

Chong-Mandelman renders 1[e] obvious. In Chong-Mandelman, after epitaxially growing a punch-through suppression layer 500 (Ex-1007, [0040]–[0044]) and after the NFET source/drain implant is complete (*id.* [0055]–[0057]), a second photoetching would be performed using a photoresist layer to separate the gates, as Mandelman teaches. Ex-1005, [0038]; Ex-1003, ¶208; §VI.D.1(a). The photoetching process would segment the PFET gate 122 into multiple segments, like Mandelman’s segments 40a and 40b. Ex-1005, [0038]. The exposed portions are then etched, forming a slot (e.g., between sidewalls 78 and 79) in the gate pattern. *Id.*, [0038], Fig. 4.

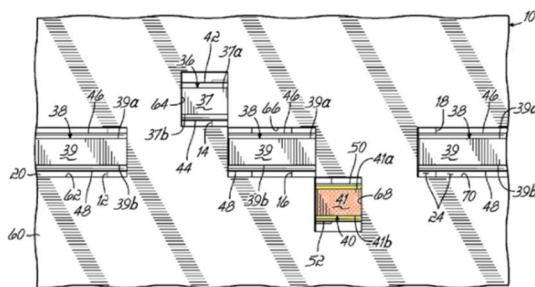


FIG. 3

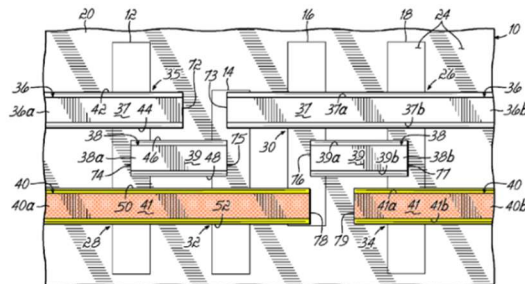


FIG. 4

Mandelman, Figs. 3-4

3. Claim 2. “The method of claim 1, wherein after forming the silicon layer comprises:”

Chong-Mandelman renders claim 2 obvious by performing the following steps after forming the silicon layer.

(a) 2[a]-[h]

Chong discloses 2[a]-[h] as discussed for Ground 2. §§VI.B.4(a)–B.4(h).

(b) 2[i]

Chong and Mandelman render 2[i] obvious. As discussed for 1[e], Mandelman’s gate cutting (“second photoetching process”) is performed to separate the patterned gate strip into individual gates after a punch-through suppression layer 500 is epitaxially grown. Ex-1005, [0038], Fig. 4; §VI.D.2(b); Ex-1003, ¶211. Further, as discussed in §VI.D.1(b), and as Mandelman teaches, Chong’s gates would be separated at least after the materials for the liner 702 and spacer 706 (the “first dielectric layer”) are deposited (for example, by blanket deposition), so the subsequent etch back to form the differential spacer 708 will leave no spacers on the cut edges, as illustrated in Mandelman’s Figures 15-16; Ex-1003, ¶211.

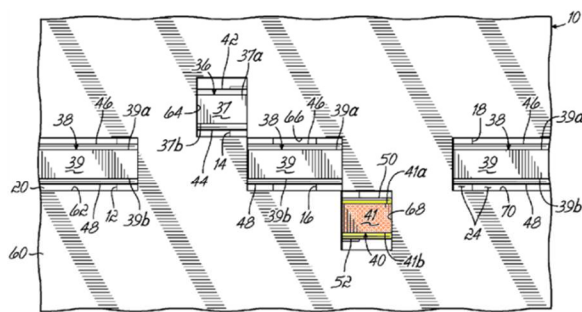


FIG. 3

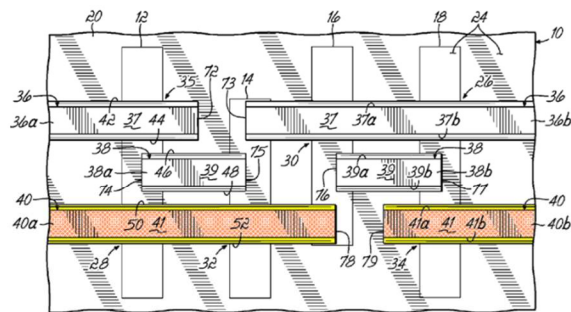


FIG. 4

Mandelman, Figs. 3-4

Mandelman's second photo-etching process is thus performed on the gate 122 (which forms the "gate pattern"), a first liner 128 and spacer 130 (the "first spacer"), and the liner 702 and spacer 706 (the "first dielectric layer"). Ex-1003, ¶212.

(c) 2[j]

Chong in view of Mandelman renders this limitation obvious. As explained in §VI.B.4(h), Chong discloses forming each of the **liner 702** and **spacer 706** by "blanket deposition followed by a subsequent etch back" to remove at least a portion of **liner 702 and spacer 706** ("first dielectric layer") to form a differential spacer 708 ("a second spacer"), as claimed. Ex-1007, [0048], Fig. 7; Ex-1003, ¶213.

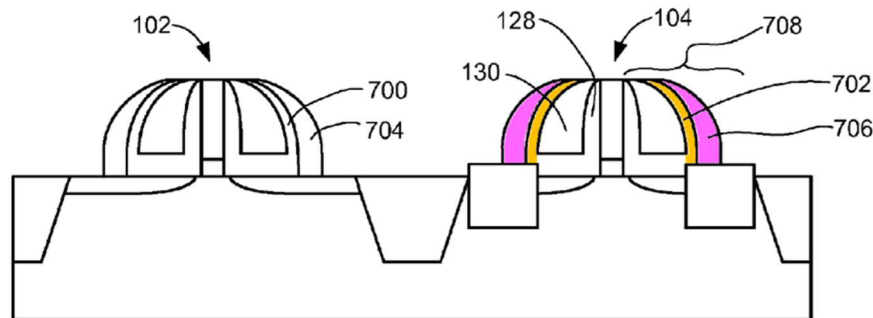


FIG. 7
Chong, Fig. 7

Chong-Mandelman renders this limitation obvious regardless of whether the "second spacer" is formed before or after the "second photo-etching process" of 2[i]. Here, nothing in the claim requires a second spacer to be formed after the second photo-etching process, and the two steps are not tied together in any way. *Baldwin Graphic*, 512 F.3d at 1345; *Sunoco Partners*, 32 F.4th at 1177. Accordingly,

Chong's patterning of the layers 702 and 706 (the "first dielectric layer") to form the second spacer meets this limitation regardless of its sequence with respect to Mandelman's gate cut process ("second photoetching process").

Indeed, in the Chong-Mandelman combination, Mandelman's gate cut ("second photo-etching process") would occur any time after the deposition of the dielectric materials. Ex-1003, ¶215. As Mandelman explains, the goal of the gate cut is to expose the sidewalls 72-79 so they are in "direct physical contact" with a silicide layer "without any intervening structures, such as a spacer." Ex-1007, [0038]-[0039], [0046]. The direct contact establishes "electrically connective bridges," which help simplify contacts and cell layouts. *Id.*, [0045]. Thus, as long as the gate cut occurs after the deposition of the dielectric materials, the goal would be met, regardless of whether Chong's etch-back of the dielectric materials for forming the second spacer occurs before or after Mandelman's gate cut. Either sequence would have been obvious to try. Ex-1003, ¶215. Chong discloses a conventional method (e.g., "reactive ion etch") by which the patterning could be performed. Ex-1007, [0053]. Forming the second spacer in one of the two available ways, i.e., before or after photoetching, using any of the known patterning techniques would have been "the product not of innovation but of ordinary skill and common sense." *KSR*, 550 U.S. at 403; Ex-1003, ¶215.

Should the Board find that the second spacer may be formed before the second photo-etching process, Chong in view of Mandelman renders obvious forming Chong's differential spacers 708 **before** performing Mandelman's gate cut process to leave the cut gate edges without any sidewall spacers. See Ex-1005, [0046]-[0048], Figs. 3-4.

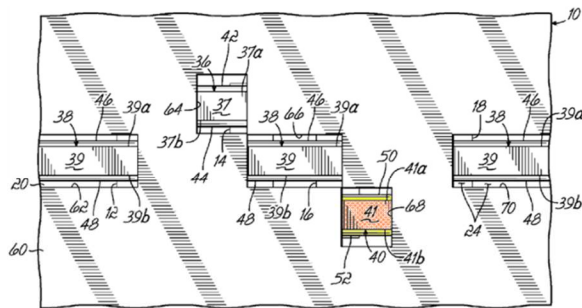


FIG. 3

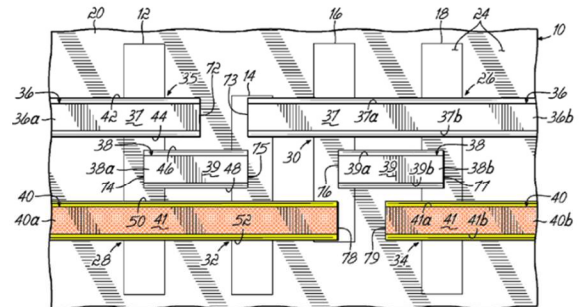


FIG. 4

Mandelman, Figs. 3-4

In this combination, Chong's differential spacers 708 would first be formed along the gate length direction of the gate, and Mandelman's gate cut process would cut the gate with the differential spacers so the differential spacers 708 are not formed on "vertical surfaces" where direct contact with a silicide layer is intended. Ex-1005, [0046]-[0048]; Ex-1003, ¶217.

Alternatively, should the Board find that a second spacer must be formed after the second photo-etching process, Chong-Mandelman renders this alternative obvious. Chong discloses that the differential spacers 708 are formed by blanket depositions of a dielectric material (such as an oxide) followed by another dielectric material (such as a nitride). It would have been obvious to utilize Chong's nitride

film as an “etch mask” during an “anisotropic dry etching process” for Mandelman’s gate cut. Ex-1007, [0031], [0036]; Ex-1003, ¶218. Once the etching is performed to cut the gate, the nitride film would then be removed along with the underlying oxide layer to form Chong’s differential spacers 708. Ex-1003, ¶218. Thus, even if Chong’s oxide/nitride layers are etched back to form the differential spacers *after* performing Mandelman’s gate cut process, spacers would not be present in the cut gate edges. *Id.*

4. Claim 3

Chong-Mandelman renders claim 3 obvious. Chong discloses that the semiconductor substrate comprises **isolation structure 136** and that the isolation structure 136 is a shallow trench isolation (STI). Ex-1007, [0033]. As shown in Chong’s Fig. 1, the PFET device 104 and NFET devices 102 are isolated from each other by the STI 136; Ex-1003, ¶219.

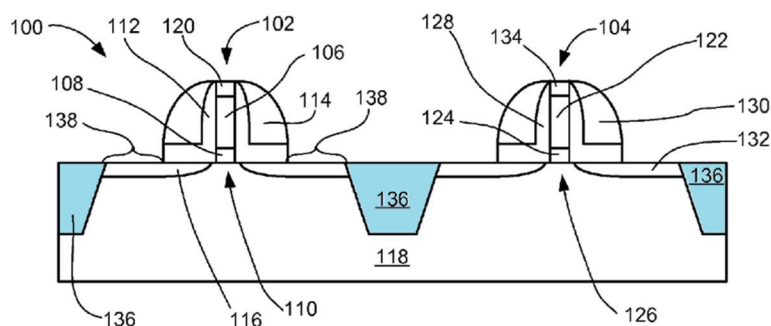


FIG. 1
Chong, Fig. 1

In Chong-Mandelman, “the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.”

Mandelman's second photoetching process segments the conductor line 40 into multiple segments by removing portions of the conductor line 40 and exposing the underlying shallow trench isolation regions 20. Ex-1005, [0037]-[0038].

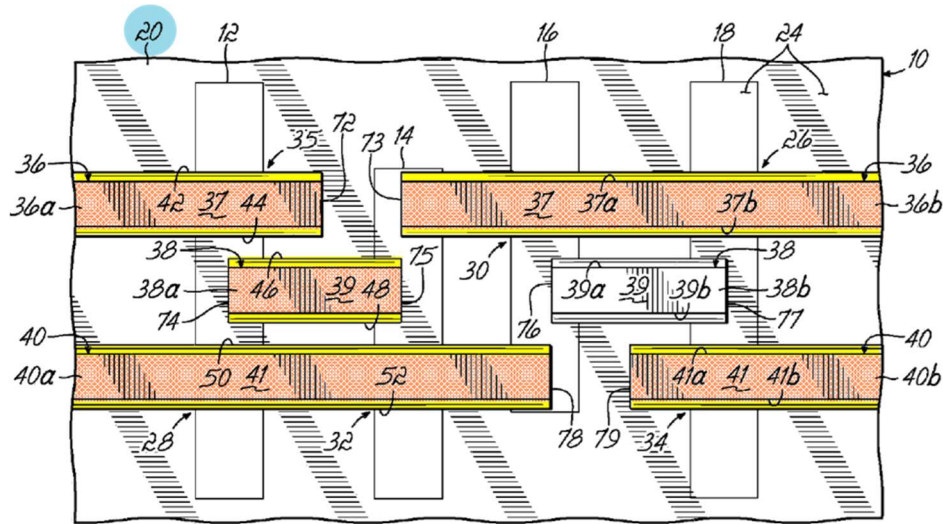


FIG. 4
Mandelman, Fig. 4

A POSITA would have recognized that the second photoetching of Chong-Mandelman is done by etching away portions of the gate 122 disposed on the STI structures 136. Ex-1003, ¶221. Indeed, portions of the gate 122 on the STI structures *must* be removed so that two or more separate gates electrically independent from each other, as shown in Mandelman's Fig. 4, can be formed. *Id.*

5. Claims 4-6

Chong discloses or renders obvious claims 4-6 as discussed for Ground 2. §VI.B.6–B.8.

VII. TRIAL SHOULD BE INSTITUTED

The Stewart Memorandum dated March 26, 2025, titled “Interim Process for PTAB Workload Management,” sets out a temporary procedure under which Co-Petitioners will have an opportunity to respond to any discretionary denial arguments Patent Owner may raise through a bifurcated briefing process. Co-Petitioners believe discretionary denial is unwarranted and, at the appropriate time, plan to rebut any claims Patent Owner may advance to the contrary.

Meanwhile, Co-Petitioners identify below several non-limiting considerations that weigh against discretionary denial:

- The ITC instituted investigation on March 21, 2025, just 27 days before this Petition was filed. The ITC has not even set a schedule, let alone issued any substantive orders. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, at 11 (Mar. 20, 2020) (expeditious filing weighs against denial); *SharkNinja v. iRobot Corp.*, IPR2021-00545, Paper 11, at 8 (Sept. 8, 2021) (petitioner’s diligence and remaining work at the ITC weighs against denial).
- No other forum has adjudicated these claims.
- The Petition challenges every claim of the ’473 Patent and hence all claims asserted in the ITC.

- Co-Petitioner TSMC has a 94% institution rate on the merits and a 100% success in FWDs. Consistent with that track record, the merits here are strong, presenting a ground mapping onto every claim limitation of the '473 Patent.
- Expert testimony is corroborated by documentary evidence.
- Each of the Co-Petitioners (not to mention the other real parties-in-interest) is responsible for substantial and sustained investments in the U.S.³

The ITC lacks authority to invalidate the claims, but the companion district court, which will be stayed, triggered the one-year bar date, thereby limiting Co-Petitioners' options to invalidate the Challenged Claims. *See 3Shape A/S v. Align*

³ “TSMC Intends to Expand Its Investment in the United States to US **\$165 Billion** to Power the Future of AI,” <https://pr.tsmc.com/english/news/3210> (Mar. 4, 2025); “Apple Will Spend More Than **\$500 billion** in the U.S. Over the Next Four Years,” <https://www.apple.com/newsroom/2025/02/apple-will-spend-more-than-500-billion-usd-in-the-us-over-the-next-four-years/> (Feb. 24, 2025); “Trump and TSMC Announce **\$100 Billion** Plan to Build Five New US Factories,” <https://www.reuters.com/technology/tsmc-ceo-meet-with-trump-tout-investment-plans-2025-03-03/> (Mar. 4, 2025).

Tech., Inc., IPR2020-00223, Paper 12, at 33-34 (May 26, 2020) (instituting despite parallel ITC case to preserve the “efficiency and integrity of the system”); *Emerson Electric Co., v. Sipco, LLC*, IPR2019-00547, Paper 15, at 9 (Aug. 30, 2019) (IPR proceedings not duplicative of parallel ITC case). The ITC may not even reach the issue of invalidity. *See, e.g., Beloit Corp. v. Valmet Oy*, 742 F.2d 1421, 1423 (Fed. Cir. 1984).

VIII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest

Co-Petitioners Taiwan Semiconductor Manufacturing Company Limited and Apple Inc., as well as Broadcom Inc. and Qualcomm Inc., are the real parties-in-interest.

B. Related Matters

The '473 Patent has been asserted against Petitioners in *Certain Foreign-Fabricated Semiconductor Devices, Products Containing the Same, and Components Thereof*, Inv. No. 337-TA-1443 (U.S.I.T.C.). In the same proceeding, Patent Owner has alleged infringement by the following entities:

- Taiwan Semiconductor Manufacturing Company Ltd.
- Apple Inc.
- Broadcom Inc.
- Qualcomm Inc.

- Lenovo Group Ltd.
- Motorola Mobile Communication Technology Ltd.
- Motorola (Wuhan) Mobility Technologies Communication Co. Ltd.
- OnePlus Technology (Shenzhen) Co. Ltd.

Additionally, Patent Owner has asserted the '473 Patent against Co-Petitioner Taiwan Semiconductor Manufacturing Company Ltd. in *Longitude Licensing Ltd. v. Lenovo Grp. Ltd. et al.*, Case No. 2:25-cv-00171-JRG (E.D. Tex.). In the same proceeding, Patent Owner has alleged infringement by the following entities:

- Taiwan Semiconductor Manufacturing Company Ltd.
- Lenovo Group Ltd.
- Motorola Mobile Communication Technology Ltd.
- Motorola (Wuhan) Mobility Technologies Communication Co. Ltd.
- OnePlus Technology (Shenzhen) Co. Ltd.

Petitioners are not aware of any other proceedings involving the '473 Patent.

C. Lead and Back-Up Counsel

Petitioners provide the following designation of counsel.

Lead Counsel	Backup counsel
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D. Service Information

Co-Petitioner TSMC consents to service by e-mail at the following addresses:

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- jodiecheng@quinnemanuel.com;
- kevinjang@quinnemanuel.com;
- TSMC-MSL-IPR@finnegan.com.

Co-Petitioner Apple consents to electronic service by email at IPR50095-0268IP1@fr.com (referencing No. 50095-0268IP1 and cc'ing PTABInbound@fr.com, axf-ptab@fr.com, tar@fr.com, and ahn@fr.com)

IX. PAYMENT OF FEES

The Office may charge additional fees to Deposit Account No. 06-0916.

X. GROUNDS FOR STANDING

Petitioners certify the '473 Patent is available for *inter partes* review and Petitioners are not barred or estopped from requesting review on the grounds presented here.

XI. CERTIFICATION UNDER 37 C.F.R. §42.24(d)

As calculated by the “Word Count” feature of Microsoft Word for Microsoft 365, this Petition contains 13,806 words, excluding this Certification and the following: Table of Contents, Table of Authorities, List of Exhibits, List of Challenged Claims, Mandatory Notices, and Certificate of Service.

XII. CONCLUSION

Trial should be instituted and the challenged claims cancelled.

Dated: April 17, 2025

Respectfully submitted,

/ J. Preston Long /

J. Preston Long, Ph.D., Reg.# 65,125
FINNEGAN, HENDERSON, FARABOW,
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901 New York Ave. N.W.
Washington, DC 20001

Lead Counsel for Co-Petitioners

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105(a), **Petition for *Inter Partes* Review, Co-Petitioners' Powers of Attorney, and the associated Exhibits 1001-1041** were served via FedEx International delivery on April 17, 2025, on the correspondence address of record below indicated in the U.S. Patent Office's Patent Center for U.S. Patent No. 9,093,473.

Winston Hsu
North America Intellectual Property Corporation
5F., No. 389, Fuhe Rd., Yonghe Dist.
New Taipei City, - 234645
Taiwan

Courtesy copies have been concurrently served by FedEx Priority Overnight delivery on Patent Owner's litigation counsel at:

Michael T. Renaud
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One Financial Center
Boston, MA 02111

Dated: April 17, 2025

By: / William Esper /
William Esper
Legal Assistant and PTAB Coordinator
FINNEGAN, HENDERSON, FARABOW,
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