

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Taiwan Semiconductor Manufacturing Company Ltd. and Apple Inc.,

Petitioners

v.

Marlin Semiconductor Ltd.,

Patent Owner

Patent No. 9,093,473 B2

Filing Date: July 15, 2014

Issue Date: July 28, 2015

Title: METHOD FOR FABRICATING
METAL-OXIDE SEMICONDUCTOR TRANSISTOR

Inter Partes Review No. IPR2025-00879

**DECLARATION OF PROF. EUGENE FITZGERALD, PH.D.,
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 9,093,473**

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I, Dr. Eugene Fitzgerald, Ph.D., declare as follows:

I. INTRODUCTION

1. My name is Dr. Eugene Fitzgerald. I have been asked to submit this declaration on behalf of Taiwan Semiconductor Manufacturing Company Limited (“TSMC”) in connection with a petition for *inter partes* review of U.S. Patent No. 9,093,473 (“’473 Patent”), which I have been told TSMC is submitting to the Patent Trial and Appeal Board of the United States Patent and Trademark Office.

2. TSMC has retained me as a technical expert to study and provide my opinions on the technology covered by, and the patentability or non-patentability of, claims 1-10 of the ’473 Patent (“Challenged Claims”).

3. This declaration is directed to the Challenged Claims and sets forth certain opinions I have formed, the conclusions I have reached, and the bases for each.

4. Based on my experience, knowledge of the art at the relevant time, analysis of prior art references, and the understanding a person of ordinary skill in the art would have had regarding the claim terms in light of the specification, it is my opinion that each of the Challenged Claims of the ’473 Patent is unpatentable for at least the reasons I discuss below.

5. I am being compensated for services provided in this matter at my standard consulting rate, plus travel expenses. My compensation is in no way

conditioned on the outcome of this investigation or any issue therein, nor is it contingent upon the results of my study or the substance of my testimony. Similarly, my compensation is in no way dependent upon and in no way affects the substance of my statements in this declaration.

II. BACKGROUND AND QUALIFICATIONS

A. Education and Career

6. I have summarized in this section my educational background, career history, and other relevant qualifications.

7. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing, and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of transistors.

8. I received a B.S. in Materials Science and Engineering from the Massachusetts Institute of Technology (“MIT”) in 1985, a M.S. in Materials Science and Engineering from Cornell University in 1987, and a Ph.D. in Materials Science and Engineering from Cornell University in 1989.

9. From 1988 to 1994, I worked as a research scientist at AT&T Bell Laboratories in Murray Hill, N.J., in the Materials Science and Engineering Department. While at AT&T Bell Laboratories, I conducted fundamental research in semiconductor materials and devices, specifically the use epitaxial layers in field

effect transistors (“FETs”).

10. From 1994 to 2000, I was an Associate Professor at MIT. From 2000 to the present, I have been a Professor of Materials Science at MIT, in the Materials Science and Engineering Department. I am currently the Merton C. Flemings-Singapore-MIT-Alliance Professor of Materials Engineering and currently the Lead Principal Investigator of MIT SMART LEES (Singapore- MIT Alliance for Research and Technology, MIT’s Research Center in Singapore, Low Energy Electronic Systems), where I manage the ninety- million-dollar research program.

11. Of specific relevance to this case, my research involves studying semiconductor structures with strained materials, and specifically the use of epitaxially grown germanium alloys—such as silicon germanium (“SiGe”)—to strain semiconductor devices. The use of epitaxial SiGe to form source/drain regions that strain the channel in Metal-Oxide-Semiconductor (“MOS”) transistors, was technology developed by at least the year 2000 (about seven years before the earliest claimed priority date for the ’847 Patent).

12. Early on my research group studied (and we continue to work on) epitaxy growth of SiGe on silicon substrates. *E.g.*, Cheng, Z., Fitzgerald, E. A., & Antoniadis, D. A. (2002). SiGe-on-insulator (SGOI) technology and MOSFET fabrication. *Advanced Materials for Micro- and Nano-Systems (AMMNS)*; Kwon, O., Boeckl, J. J., Lee, M. L., Pitera, A. J., Fitzgerald, E. A., & Ringel, S. A. (2006).

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Monolithic integration of AlGaInP laser diodes on SiGe/Si substrates by molecular beam epitaxy. *Journal of applied physics*, 100(1); Wang, J., Heidelberger, C., Fitzgerald, E. A., & Quitoriano, N. J. (2020). Liquid phase epitaxy SiGe films on a CVD-grown SiGe/Si (0 0 1) graded film. *Journal of Crystal Growth*, 535, 125541.

13. I have received numerous honors and awards for my work. For example, I was a co-recipient of the Institute of Electrical and Electronics Engineers (“IEEE”) 2011 Andrew S. Grove Award for outstanding contributions to solid state devices and technology including “seminal contributions to the demonstration of Si/Ge lattice mismatch strain engineering for enhanced carrier transport properties in MOSFET devices,” the IEEE 2004 EDS George Smith Award for Best Paper for a paper I co-authored entitled “Fully Depleted Strained-SOI n- and p- MOSFETs on Bonded SGOI Substrates and Study of the SiGe/BOX Interface,” and the TMS 1994 Robert Lansing Hardy Medal Award for exceptional promise of a successful career in the field of metallurgy and materials science.

14. I am the founder, co-founder, or a founding team member of the following companies and organizations: AmberWave Systems Corporation (a company focused on strained silicon semiconductor technology); Contour Semiconductor (a company focused on a unique semiconductor fabrication process for non-volatile memory); 4Power LLC (manufacturer of high efficiency, low cost solar cells using III-V thin films on silicon substrates); Paradigm Research LLC

(commercializing true monolithic III-V/Si CMOS integrated circuits); The Innovation Interface (a not-for-profit organization that trains future innovators through university-corporate innovation projects); The Water Initiative (creating customized point-of-drinking water solutions and scaling those solutions through micro-entrepreneurs, developers and government entities), and New Silicon Corporation Pte. Ltd. (III-V+CMOS integrated circuit company).

15. A full list of my research and professional experience, my expert witness or consultant experience, and other activities and awards is further detailed in my curriculum vitae, attached as Appendix C.

16. As a co-founder, professor, and inventor myself, I am familiar with patents, the patent process, patent claims, and patent analysis.

B. Publications

17. A list of the publications that I have authored and patents I have been awarded during my technical career can be found in my Google Scholar Profile <https://scholar.google.com/citations?hl=en&user=YsZ6EjkAAAAJ>.

18. I am a named inventor on over 100 granted United States patents and have authored over 700 peer-reviewed academic journal publications. I have coauthored several publications on strained silicon transistors. For example, I co-authored the book *Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy*, published

in 2018 by CRC press. I also have patents specifically discussing SiGe/silicon strain technology, gate sidewall spacer formation, and lightly doped drains, metal gate electrodes, and MOSFET transistors, all of which are relevant technologies in this case. Some examples of my relevant patents and publications that predate the '847

Patent are:

- Mii, Y. J., Xie, Y. H., Fitzgerald, E. A., Monroe, D., Thiel, F. A., Weir, B. E., & Feldman, L. C. (1991). Extremely high electron mobility in Si/Ge x Si $1-x$ structures grown by molecular beam epitaxy. *Applied Physics Letters*, 59(13), 1611-1613.
- Lee, M. L., & Fitzgerald, E. A. (2003). Optimized strained Si/strained Ge dual-channel heterostructures for high mobility P-and N-MOSFETs. In *IEEE International Electron Devices Meeting 2003* (pp. 18-1). IEEE.
- Lee, M. L., Fitzgerald, E. A., Bulsara, M. T., Currie, M. T., & Lochtefeld, A. (2005). Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors. *Journal of applied physics*, 97(1).
- Fitzgerald, Eugene A., Richard Hammond, and Matthew Currie. (2003). Gate technology for strained surface channel and strained buried channel MOSFET devices. U.S. Patent No. 6,583,015.
- Langdo, T. A., Currie, M. T., Hammond, R., Lochtefeld, A. J., & Fitzgerald, E. A. (2006). Strained-semiconductor-on-insulator device structures. U.S. Patent No. 6,995,430.

III. MATERIALS REVIEWED

19. In forming my opinions regarding the '473 Patent, I reviewed the materials discussed in this declaration, including the references listed in Appendix A. All citations to materials in Appendix A in this declaration are to the

page number of the original reference, not the stamped exhibit page numbers.

IV. LEGAL STANDARDS

20. I am not an attorney and have not been asked to offer my opinion on the law. However, as an expert offering an opinion on whether the claims in the '473 Patent are patentable, I have been told that I am obliged to follow existing law.

A. Anticipation

21. I have been told the following legal principles apply to analysis of patentability pursuant to 35 U.S.C. § 102, a provision in the patent law regarding anticipation. I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable for anticipation if it is shown by preponderance of the evidence (i.e., it is more likely than not) that the claim was anticipated by a prior-art patent or publication.

22. I have been told that for a claim to be anticipated, every limitation of the claimed invention must be disclosed by a single prior-art reference, viewed from the perspective of a person of ordinary skill in the art.

B. Obviousness

23. I have been told that under 35 U.S.C. § 103(a), “[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in § 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the

time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” I have been told that, in *inter partes* review proceedings, a patent claim may be deemed unpatentable if it is shown by preponderance of the evidence (i.e., it is more likely than not) that it would have been obvious.

24. When considering the issues of obviousness, I have been told that I am to do the following:

- a) Determine the scope and content of the prior art;
- b) Ascertain the differences between the prior art and the claims at issue;
- c) Resolve the level of ordinary skill in the pertinent art; and
- d) Consider evidence of secondary indicia of obviousness or non-obviousness (if available).

25. I have been told that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of alleged invention, which I have been asked to assume is just before the earliest claimed priority date of the '473 Patent (i.e., **July 15, 2010**).

26. I have been told that obviousness is a determination of law based on underlying determinations of fact. I have been told that these factual determinations include the scope and content of the prior art, the level of ordinary skill in the art,

the differences between the claimed invention and the prior art, and any objective indications of obviousness or non-obviousness that may exist (although I am not aware of any objective indications of non-obviousness relating to the '473 Patent).

27. I have been told that a prior-art reference may be combined with one or more other references and/or the knowledge of a person of ordinary skill in the art to show obviousness. I also have been told that a person of ordinary skill in the art is presumed to know all relevant prior art. I have been told that the obviousness analysis may account for the inferences and creative steps that a person of ordinary skill in the art would have employed at the time of invention.

28. In determining whether the teachings contained in one prior-art reference would have been combined with the teachings contained in another reference or information known to a person of ordinary skill in the art, I have been told that the following principles may be considered, and I have been asked to consider them:

a) A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

b) The substitution of one known element for another is likely to be obvious if it yields predictable results;

c) The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

d) The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

e) Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

f) A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

g) The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

29. I have been told that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would have employed are also relevant to the obviousness inquiry.

30. I have been told the reasons a person of ordinary skill in the art would

have wanted to modify teachings available in the prior art teachings do not need to match the inventor's reasons for making the claimed invention. In determining whether the subject matter of a patent claim is obvious, I have been told that what matters is the objective reach of the claim and whether it covers an obvious variation of the prior art. I have been told it would be improper to consider only the specific problem the patentee was trying to solve.

31. I have been told that when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been told that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation was likely to have been obvious. I have been told that in many fields, there may be little discussion of obvious combinations, and, in these fields, market demand, not scientific literature, may drive design trends. I have been told that when there was a design need or market pressure and there were a finite number of predictable solutions, a person of ordinary skill in the art would have had good reason to pursue those known options.

32. I have been told that there is no rigid rule that a reference or combination of references must contain a "teaching, suggestion, or motivation" to combine them. But I also understand that any "teaching, suggestion, or motivation" present in the prior art may be useful in establishing a rationale for combining

aspects of the prior art. I have been told this “teaching, suggestion, or motivation” test poses the question as to whether the prior art contains an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

33. I have been told that a claimed invention may be obvious even when the prior art does not teach each claim limitation, so long as the record contains some reason why a person of ordinary skill in the art would have applied the prior art to obtain the claimed invention.

34. When considering the obviousness of claimed dimensions, I have been told obviousness depends on whether a person of ordinary skill in the art would have appreciated that new and unexpected properties (as compared with known dimensions and trends) resulted from the claimed dimensions. I have been told that when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable dimensions by routine experimentation. For example, I have been told that if the prior art teaches the dimensions in a device can be modified to affect the device properties, it is not inventive to discover the optimum or workable dimensions by routine experimentation. I have also been told the prior art does not need to provide the exact method of optimization, and a claim to a device does not become non-obvious simply because the patent’s specification

provides a more comprehensive explication of the known relationships between dimensions and device properties.

35. I have been told that the outcome of optimizing a device dimension may only be patentable if the claimed dimensions are “critical” and produce a new and unexpected result that differs in kind, not merely in degree, from the results of the prior art. I have been told that when obtaining the claimed dimension was within the capabilities of a person of ordinary skill in the art and does not produce any unexpectedly beneficial properties, the optimization of a dimension known to affect device properties would have been obvious.

36. In addition, I have been told that any allegedly new and unexpected result must be “commensurate in scope” with the claimed range of dimensions, meaning the new and unexpected result must apply across the entire range of dimensions recited in the claim.

V. LEVEL OF ORDINARY SKILL IN THE ART

37. I have been informed that a person of ordinary skill in the art (“POSITA”) is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

38. I have been instructed to assume a POSITA is not a specific real

individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

39. A person of ordinary skill in the art (“POSITA”) in reference to the ’473 Patent would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or related fields and three years of work experience in semiconductor manufacturing, such as for example, integrated circuit device (or transistor) design and/or manufacturing. Additional education could substitute for professional experience, and additional work experience/training could substitute for formal education.

40. I have not analyzed the priority date of the ’473 Patent, but I note that the earliest claim of priority listed on the face of the ’473 Patent is July 15, 2010, the filing date of application No. 12/837, 475, from which the ’473 Patent issued as a division. Because all the prior art discussed in this declaration predates July 15, 2010, I have been asked for simplicity to treat **July 15, 2010**, as the priority date for the ’473 Patent. I have also treated this date as the date from which to assess the knowledge available to a person of ordinary skill in the art.

VI. TECHNOLOGY BACKGROUND

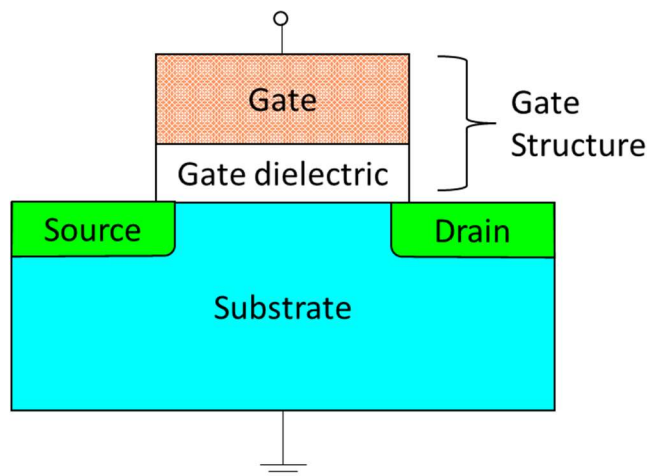
41. I understand that **July 15, 2010** may be the earliest claimed priority date for the ’473 Patent. In my opinion, all the elements in the ’473 Patent were well known before this date.

42. A person of ordinary skill in the art in the timeframe relevant to the '473 Patent would have been familiar with the background information described in subsections A through F below.

A. MOS Transistors

43. Introduced in 1960s, Metal-Oxide-Semiconductor, “**MOS**,” transistors have been a cornerstone of modern electronics for many decades. Ex-1008 at 431. MOS transistors or Field-Effect Transistors (“MOSFETs”), include *source* and *drain* regions that allow for current input and output. Ex-1008 at 433-34, Fig. 3. Electrodes on the source/drain regions allow current into and out of the MOSFET. *Id.* MOSFETs also include a *gate* that overlies a *channel* region between the source and drain regions. *Id.* The gate (or gate structure) comprises a gate or **gate electrode** (typically a metal or another conductive material such as polysilicon) and a gate dielectric (an electrically insulating film/material such as oxide, which a POSITA would have understood is referred to a gate “oxide” or gate “insulator”) that separates the gate from the channel underneath. Ex-1008 at 433-34, Fig. 3. Applying a voltage to the gate creates an electric field through the gate dielectric, which forms a channel underneath the gate electrode to connect or disconnect the source and drain. The electric field controls the conductance of the channel by controlling the number of free carriers in the channel. By controlling the electric field, a MOSFET can act as a switch that conducts current (i.e., turn on) when

desired. The figure below show a conventional arrangement of a MOSFET device.



44. Conventionally, the source/drain regions are *doped* with *p-type* or *n-type* impurities, and the channel region is doped with the other/opposing impurity type. Ex-1008 at 433-34; Ex-1009 at 76-82. A MOSFET with source/drain regions doped with p-type impurity is referred to as a “**PMOS**” or “**PFET**” device; likewise, a MOSFET with n-type impurity is referred to as a “**NMOS**” or “**NFET**” device. Ex-1009 at 12-13, 50-51, Figs. 1-11, 2-2. An integrated circuit with both PMOS and NMOS (or PFET and NFET) devices has a Complementary MOS, “**CMOS**,” structure). Ex-1009, Fig. 1-11.

45. The process of doping the source/drain regions with the appropriate p-type or n-type impurity may be accomplished by ion implantation, in which ionized dopant atoms (*i.e.*, impurity ions) are implanted into the substrate. Advantages of using ion implantation include precise control over dose and depth of dopants, ability to create complex doping profiles, and selection from a wide range of dopants. Ion

implantation also has disadvantages, however, including potential damage to the substrate caused by the high energy ions.

B. Lightly Doped Drain (“LDD”) Regions and Sidewalls

46. Since the 1960s, the silicon fabrication technology has continued to progress to make many improvements according to Moore’s law, making individual transistors smaller and thereby increasing transistor density. Ex-1010 at xviii-xxi; Ex-1014 at 1, Fig. 1-1(b). To shrink a MOSFET, the channel must become shorter, bringing the source and drain regions closer. Ex-1015 at 205, 233-34; Ex-1014 at 338. Consequently, the source/drain electric field may “penetrate into the source region” and cause unwanted current increase. Ex-1014 at 341. This penetration is called *punch-through*, which is an example of what are known as short-channel effects (“SCEs”). Ex-1015 at 233; Ex-1008 at 433; Ex-1016 at 211; Ex-1009 at 77-78.

47. Researchers and engineers recognized such issues as early as the 1970s and developed a variety of techniques to mitigate SCEs. By the 1990s, one ubiquitous technique to mitigate SCEs in high-volume commercial semiconductor fabrication was to use so-called lightly doped drain (“LDD”) regions. Ex-1009 at 76-82; Ex-1016 at 211-13.

48. As early as 1980s, researchers found they could better control transistor performance by controlling the source/drain doping. “The objective is to carefully

tailor the doping profile near the drain junction (and the source junction) in order to minimize short channel effects.” Ex-1009 at 78. For example, it was found that introducing LDD regions between more heavily doped source/drain regions and the channel improved performance by controlling electric fields near the channel. Ex-1009 at 77-78. Because LDD extends a more heavily doped source/drain region, it is sometimes also referred to as an extension region. Ex-1034, 4:14-23, Fig. 1; Ex-1035 at [0021]; Ex-1031 at [0007]; Ex-1040, 1:46-51; Ex-1041 at [0017]. The textbook figures below depict a method of forming LDD regions. Ex-1009 at 76-77.

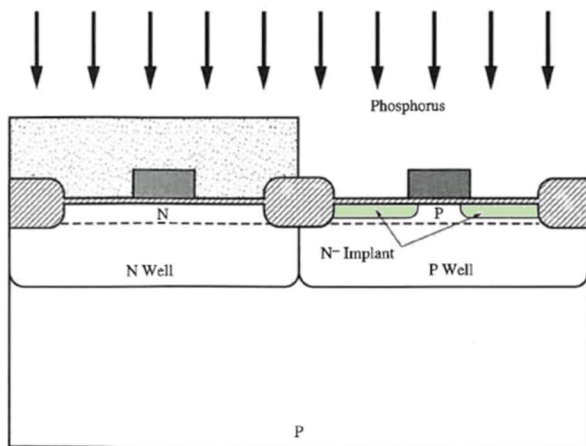


Figure 2-27 Mask 7 is used to cover the PMOS devices. A phosphorus implant is used to form the tip or extension (LDD) regions in the NMOS devices.

Ex-1009, Fig. 2-27

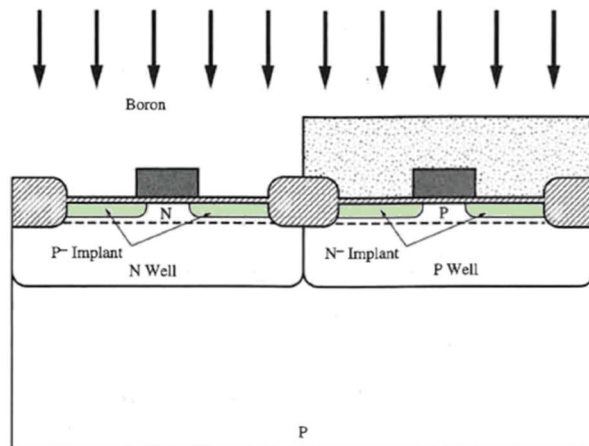


Figure 2-28 Mask 8 is used to cover the NMOS devices. A boron implant is used to form the tip or extension (LDD) regions in the PMOS devices.

Ex-1009, Fig. 2-28

The LDD regions are designed to reduce the effect of the electric field from the source/drain regions on the channel. The '473 Patent admits it is conventional to form LDD. Ex-1001, 1:26-42. With LDD regions, the more heavily doped

source/drain regions are further away from the gate. Ex-1009 at 76-82; Ex-1016 at 211-13. This typically can be achieved with sidewall spacers. Ex-1009 at 78-80.

49. As shown below, sidewall spacers act as masks during the heavy doping process, protecting the LDD regions when forming more heavily doped regions farther away from the channel edge. Ex-1009 at 80-82, Figs. 2-31 to 2-33; see Ex-1016 at 213, Fig. 9.17; Ex-1015 at 595-96, Fig. 9-31(f); Ex-1005 at [0034]. To provide such a masking effect, sidewall spacers are formed on the sidewalls of the gate. Ex-1031 at [0009]; Ex-1032 at [0004].

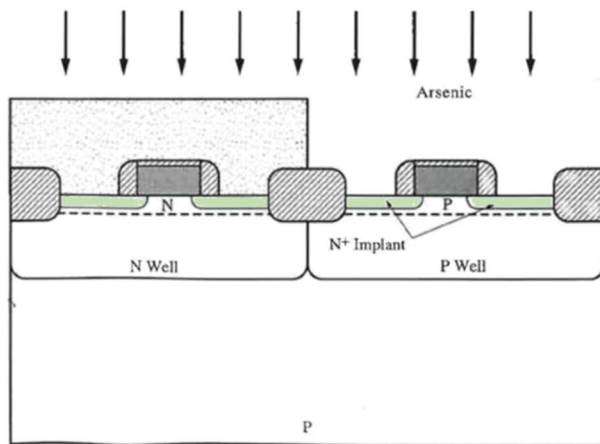


Figure 2-31 After growing a thin "screen" oxide, photoresist is applied and mask 9 is used to protect the PMOS transistors. An arsenic implant then forms the NMOS source and drain regions.

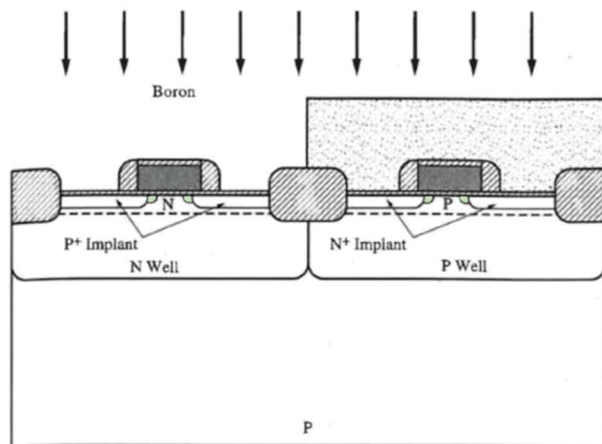


Figure 2-32 After applying photoresist, mask 10 is used to protect the NMOS transistors. A boron implant then forms the PMOS source and drain regions.

Ex-1009, Fig. 2-31

Ex-1009, Fig. 2-32

50. Conventionally, sidewall spacers are formed by conformal deposition of an insulator or dielectric, such as silicon nitride or silicon dioxide, followed by etching back to retain only the vertical parts. Ex-1005 at [0033]; Ex-1011 at [0028]. Indeed, the '473 Patent admits that forming spacers on the sidewall of the gate was

a conventional approach. Ex-1001 at 1:26-42.

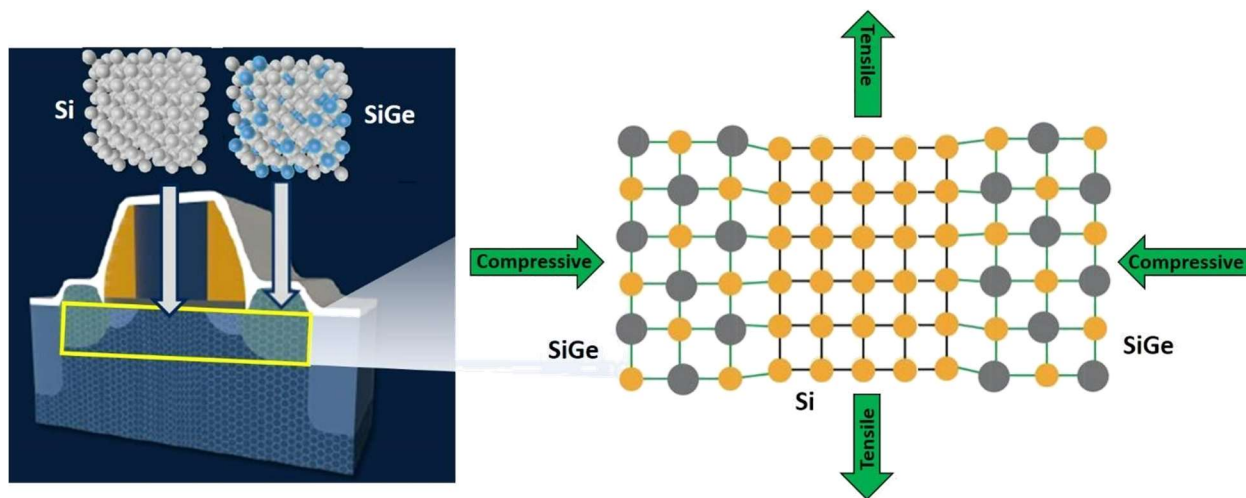
C. Creating Stress with Epitaxially Grown Source/Drain Region

51. Researchers further found that the operating (i.e., switching) speed and current drive of MOSFETs could be increased and improved by imparting stress in the silicon in the channel regions. Ex-1019 at 2; Ex-1017 at 1790-96; Ex-1018 at [0005]; Ex-1021 at [0004]; Ex-1022 [0004].

52. To impart mechanical stress in the channel, those in the art used *epitaxially* grown materials in the recesses of the source/drain regions. An epitaxy (epi) process refers to a conventional semiconductor fabrication technique in which a thin crystal layer is grown on a substrate, using techniques such as chemical vapor deposition (CVD). Epitaxially growing a layer only on a specific area of a substrate (e.g., in the source/drain regions) is known as selective epitaxial growth (SEG). Ex-1024 at 816. These epitaxial source/drain regions had different crystal lattice spacing than the neighboring silicon channel regions. The difference in physical spacing between the source/drain regions and the channel regions creates mechanical stress on the silicon channel.

53. Compressive strain improves PMOS mobility, whereas tensile strain improves NMOS mobility. Ex-1019 at 2; Ex-1017 at 1790-96; Ex-1018 at [0005]; Ex-1021 at [0004]. For PMOS, the most conventional technique known at the time of the '473 Patent uses germanium atoms, or epitaxially grown silicon-germanium

or “SiGe” (i.e., $\text{Si}_{1-x}\text{Ge}_x$) stressors, in the source/drain regions. Because germanium atoms are *larger* than silicon atoms, the epitaxial SiGe source/drain regions would *compressively* strain the silicon channel region along the direction of current flow (left-to-right in the diagram below). Ex-1019 at 2; Ex-1017 at 1790-96; Ex-1018 at [0046]-[0047]; Ex-1023 at [0024], FIG. 4.



54. The effect of the compressive strain in the channel caused by the SiGe source/drain regions was increased mobility of charge carriers, which are holes in PMOS devices. Ex-1019 at 2; Ex-1017 at 1790-96; Ex-1018 at [0005]. Stressing the channel allowed the charge carriers to move more easily through the channel, ultimately enhancing the transistor’s switching speed and drive current. Ex-1019 at 2; Ex-1017 at 1790-96; Ex-1018 at [0005]. By 2005, SiGe had increased PMOS “hole mobility by as much as 50%.” Ex-1019 at 2.

55. Because the charge carriers in NMOS devices are electrons and improving electron mobility in NMOS devices requires *tensile* strain, rather than

compressive strain, along the direction of the current flow. Ex-1019 at 2; Ex-1017 at 1790-96; Ex-1018 at [0005]. Imparting tensile strain with the source/drain regions requires using epitaxial material with atoms *smaller* than silicon, such as the carbon atoms in silicon carbide (SiC) (instead of epitaxially growing SiGe that uses germanium atoms that are larger than silicon to impart compressive strain in the channel region). Ex-1018 at [0005], [0048], [0072]; Ex-1020 at [0038]; Ex-1021 at [0005]; Ex-1023 at [0045].

56. By the time the application for the '473 Patent was filed, epitaxial growth in the source/drain regions had already been used in two generations of high-volume commercial devices. Ex-1017 at 1790-91 (Intel 90nm devices); Ex-1025 at 657-58 (Intel 65nm devices); Ex-1028 at [0004] (“[M]anufacturing source/drain of a MOS transistor with selective epitaxial growth (SEG) technology is used to improve electrical performance of those elements.”).

57. Indeed, the '473 Patent admits that “conventional approach” includes forming “spacers ... on the sidewall of the gate and lightly doped drains and epitaxial layer ... in the semiconductor substrate adjacent to two sides of the spacer,” i.e., in recesses formed in the substrate. Ex-1001 at 1:26-42.

D. Shallow Trench Isolation

58. As MOSFET devices became smaller and more densely packed, researchers developed a technique to isolate devices and to prevent electrical

interferences between adjacent devices. **Shallow trench isolation (STI)** is an example of such a technique. An STI is created by etching trenches into the substrate and filling the trenches with an insulating material. Ex-1013 at 301. A cross section (left) and top view (right) of a MOSFET with an STI is illustrated below. Mandelman's Fig. 4, further below, also shows a top view of MOSFET devices (e.g., 28, 32, and 34) with an STI 20.

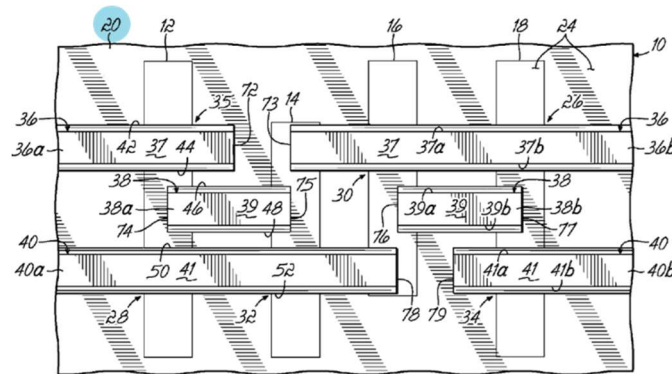
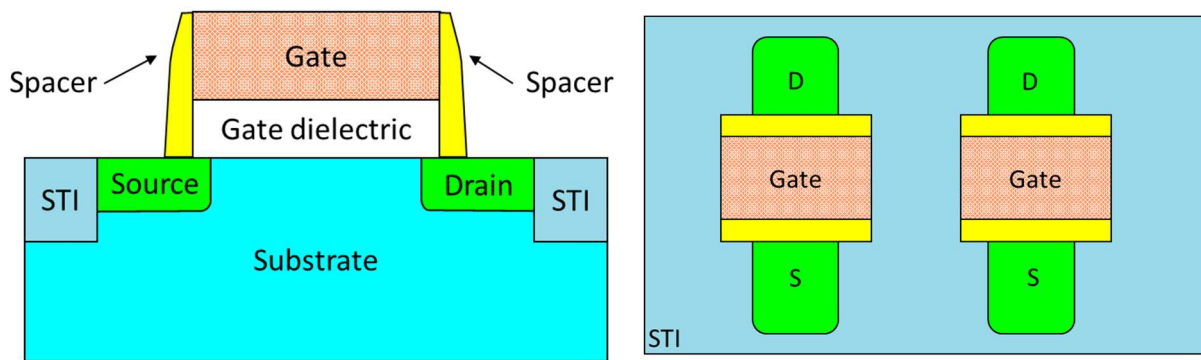


FIG. 4

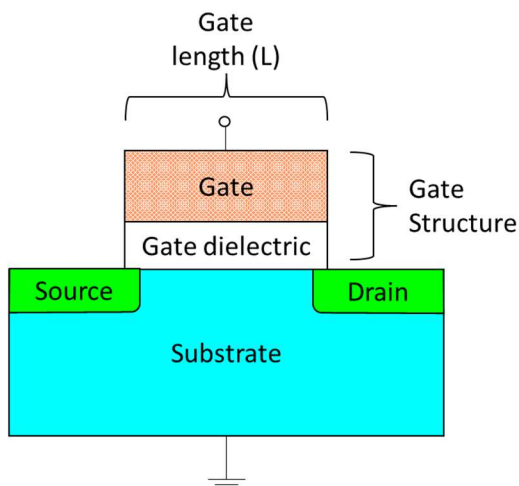
Mandelman (Ex-1005), Fig. 4

An STI allows for narrower isolation regions, enabling densely packed devices and improving electrical performances by reducing leakage currents. The use of an STI

was well known before the '473 Patent. *E.g.*, Ex-1005 at [0029]; Ex-1004 at [0031]; Ex-1007 at [0033].

E. Gate Patterning

59. As explained above, a gate structure comprises a gate electrode, such as polysilicon or other conductive material, overlaying a thin gate dielectric layer. A gate structure is traditionally formed by depositing the constituent layers (e.g., a conductive layer used for the gate electrode and the underlying gate dielectric layer) and patterning them, leaving only a portion of the gate structure with gate length (L) that overlaps the source and drain. Ex-1005 at [0031]. A gate is patterned into either a segment that forms an individual gate or a long continuous strip to be further separated into individual gates in a subsequent process. By the time of the '473 Patent, the latter approach was more widely used, given its benefit on size reduction, as discussed in Section VI.F. Regardless of which method is used, patterning a gate to an appropriate length and alignment is crucial for device performance, as it controls current flow, provides sufficient contact area for the source/drain regions, and reduces parasitic capacitance. Ex-1007 at [0005]-[0006], Figs. 3B-C; Ex-1026, 1:40-48.



Illustration

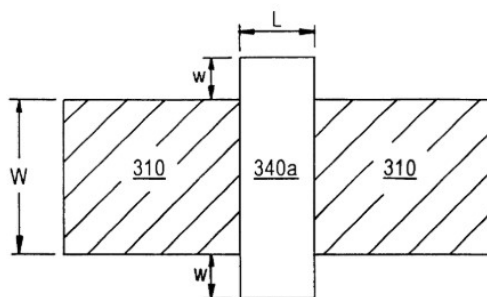


FIG. 3E

Lee, Fig. 3E

60. Gate patterning is conventionally performed using photolithography and etching (collectively, “photoetching”). Ex-1001, 1:28-36 (photoetching is a conventional approach used to pattern a gate structure). During photolithography, a photosensitive material, called a photoresist, is applied on a substrate to be patterned, and a photolithographic mask (in short, a photomask) containing a pattern of the desired features is placed over the photoresist. Light is shone through the photomask, causing the exposed portions of the photoresist to undergo a chemical change and transferring the pattern to the photoresist. In the subsequent etching process, the gate structure underlying the exposed portions of the photoresist is removed. *Id.*; Ex-1012 at [0003], [0025]-[0026]; Ex-1027 at [0004]; Ex-1029 at [0002].

F. Gate Separation (Gate Cutting)

61. In addition to gate patterning, researchers developed another technique known as gate separation (or gate cutting) to overcome limitations in

photolithography.

62. In addition to the length L , it is important that the gate span the entire width W of the source/drain regions because, otherwise, the transistor's "leakage current" (i.e., current flow when the device is off) is not effectively controlled, undermining device performance. Ex-1026 at 4:55-65.

63. To guarantee that the gate meets the minimum width W requirement, during photolithography, the photolithographic mask must be drawn so the gate pattern ends beyond the minimum width W . Ex-1026 at 4:55-65 (endcaps of the gate 340a extending to a width w beyond width W of source/drain regions 310), Fig. 3E; Ex-1027 at [0007], Fig. 3d; Ex-1012 at [0005], Fig. 2; Ex-1004 at [0005]-[0006], Fig. 3.

64. But as the transistors are scaled, a phenomenon known as "line end shortening," "setback," or "pullback"—in which a gate image transferred to the photoresist layer is shortened and rounded as a result of light diffusion at the corners during the lithographic process—becomes a greater problem. Ex-1026 at 2:1-10; Ex-1029 at [0003]; Ex-1004 at [0005]. As illustrated below, although the rounded corners are only minor when the gate length L is large, the tip becomes completely rounded and exhibits endcap shortening, i.e., "setback" or "pullback," when the gate length L is small. Ex-1026 at 2:11-27, Ex-1004 at [0005].

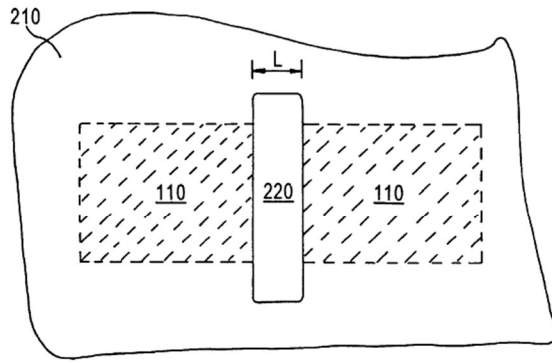


FIG. 2B
PRIOR ART

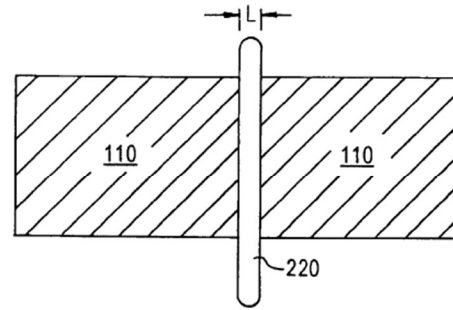
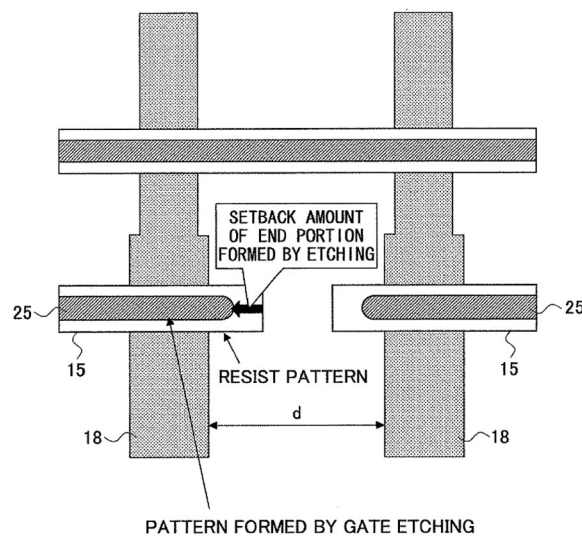


FIG. 2C
PRIOR ART

Lee, Figs. 2B-C

FIG.2

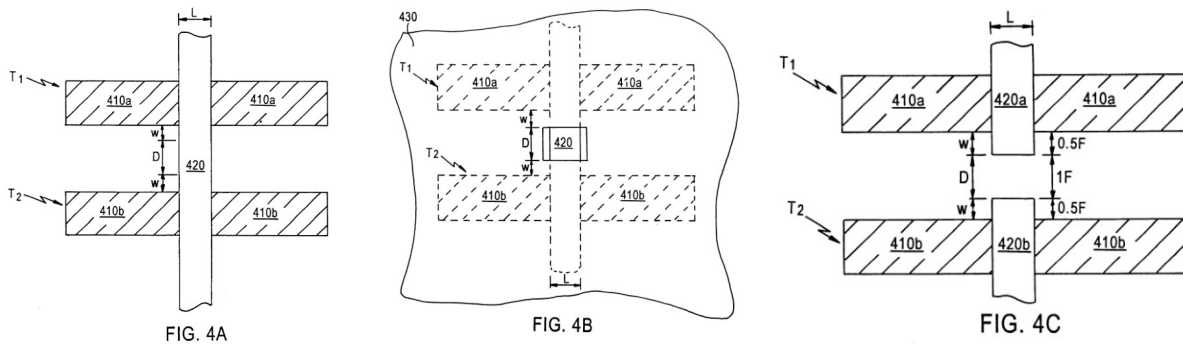


Okuno, Fig. 2

65. The aggressive reduction in gate lengths of newer circuit designs (e.g., 150 nm or less) makes gate formation more difficult due to the limitations of the photolithographic process, and the endcap design rule has to be increased to maintain an acceptable margin. Ex-1026 at 1:44-50, 2:39-42. Individually patterning gate

structures thus decreases transistor density.

66. To solve this problem, long before the '473 Patent, researchers and engineers developed a technique in which multiple gates (e.g., 420a and 420b) are formed by separating a continuous strip of a gate pattern (e.g., extended-width gate 420 shown below). Ex-1026, FIG. 4B (masking), FIG. 4C (etching).



Lee, FIGS. 4A-4C.

This way, the subsequent masking result in separate gates that are free of pullback. *Id.* at 5:17-21. This allows transistors to be formed with significantly decreased spacing, enabling more densely packed MOS transistors on the substrate than individually patterned gate structures. Ex-1026 at 5:1-35; Ex-1005 at [0036], [0038], Figs. 3-4; Ex-1004 at [0008]; Ex-1012 at [0025]-[0026]. As a result, by the time of the '473 Patent, the gate separation technique was the prevalent method for forming gates, and single gate patterning was out of date. Indeed, the '473 Patent admits that separating a gate pattern into multiple gates via photoetching is also conventional. Ex-1001, 1:28-39.

VII. THE '473 PATENT

A. Brief Description

67. The '473 Patent relates to a fabrication method of a MOS transistor. Ex-1001 at Abstract. Figure 1, for example, shows a cross-sectional view of a MOS transistor fabricated on a semiconductor substrate 12. *Id.* at 2:34-36. As illustrated in Fig. 1, an active region 14 is defined on the substrate 12 by a plurality of shallow trench isolations (STI) 16. *Id.* at 2:34-39. Then sequentially deposited on the surface of the substrate 12 are a gate insulating layer (not shown), a polysilicon layer, and a hard mask, 2:42-46, and a **first photo-etching process** has been performed to create a patterned gate insulating layer 18, **patterned polysilicon layer 20**, and **patterned hard mask 22**. *Id.* at 2:52-62.

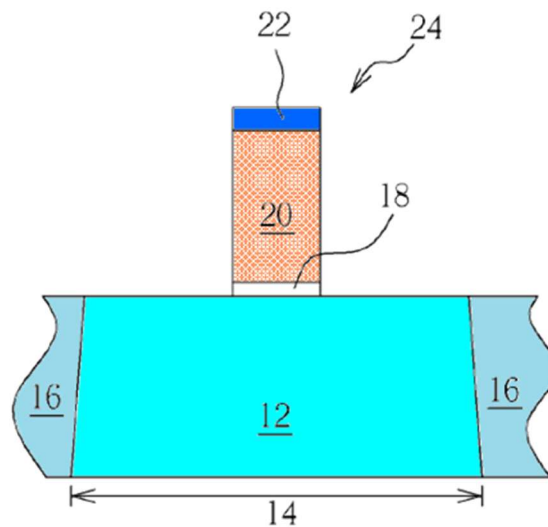
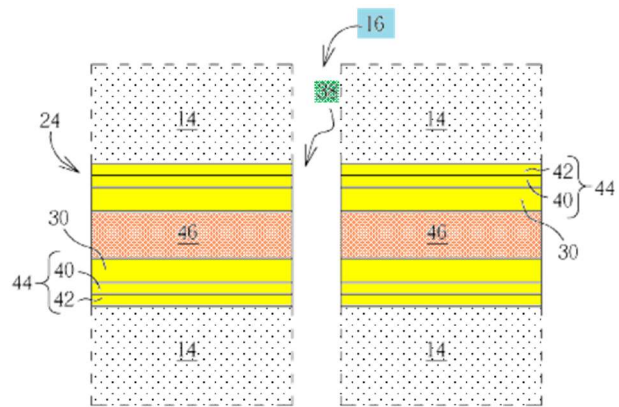
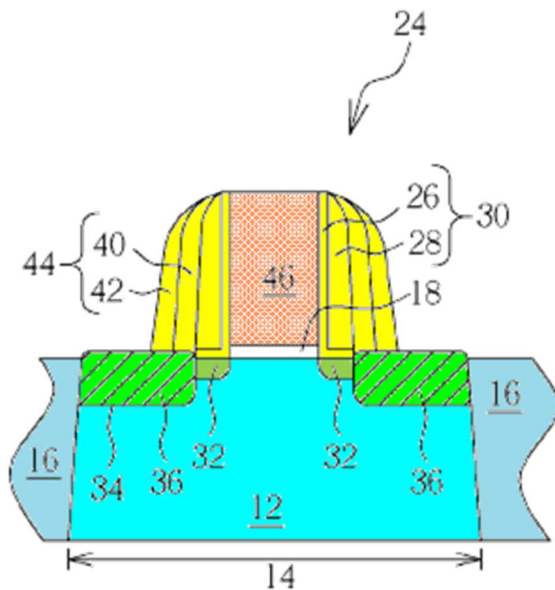


FIG. 1

68. A spacer 30 is then formed, and a selective epitaxial growth (SEG) process is performed to form a strained silicon in the two recesses 34 in the substrate

12. *Id.* at 3:11-21. “Preferably, a light ion implantation could be conducted before the formation of the first spacer 30 and the epitaxial layer 36 ... for forming a lightly doped drain 32.” *Id.* at 3:21-26. As Fig. 4 further illustrates, additional dielectric material is deposited for forming a second spacer 44. At “any point after the epitaxial layer 36 is formed,” a **second photo-etching process** for creating a polysilicon slot 38 that separates the gate pattern 24 into two independent gates 46. *Id.* at 4:27-31; *see also id.* at 1:34-42, 5:1-7.



B. Prosecution History

69. The '473 Patent was allowed in the first office action. *See generally* Ex-1002. During prosecution, the examiner did not consider any of the references used in this petition—i.e., Chong, Okuno, Mandelman, or Shin. As discussed below,

these references render the challenged claims unpatentable.

C. Claim Construction

70. I have been told that claim terms are construed with the meanings they would have to a person of ordinary skill in the art in the context of the patent document. In my analysis of the Challenged Claims, I have therefore applied the meanings of the claim terms as understood by a person of ordinary skill in the art in the context of the asserted patent and asserted claims.

71. In forming my opinions, I do not believe that any express constructions are required because the prior art teaches substantially the same teachings as the '473 Patent's disclosures.

72. If Patent Owner offers constructions of any terms, I reserve the right to address those constructions at a future time.

VIII. PRIOR ART

73. The application that resulted in the '473 Patent was filed on July 15, 2014, and was a division of a U.S. application filed on July 15, 2010, which is the earliest claimed priority date that I assume for the purposes of this declaration.

a) Okuno was filed on August 19, 2009. I have been asked to assume it qualifies as prior art.

b) Shin was published on April 26, 2006. I have been asked to assume it qualifies as prior art.

c) Chong was published on June 19, 2008. I have been asked to assume it qualifies as prior art.

d) Mandelman was published on October 16, 2008. I have been asked to assume it qualifies as prior art.

IX. CLAIMS 1-10 ARE UNPATENTABLE

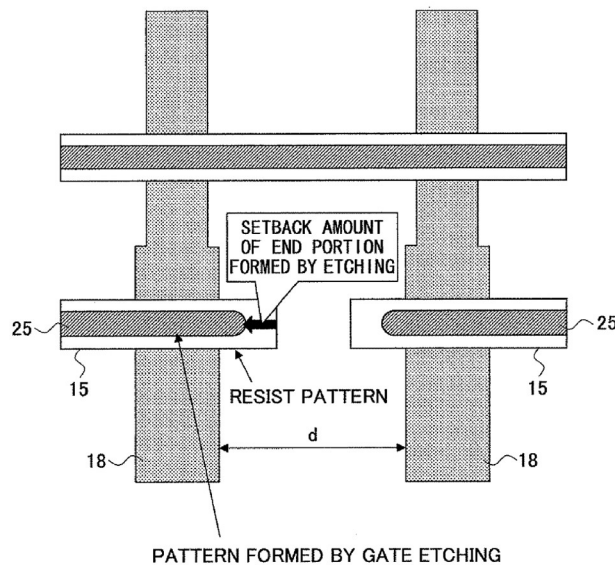
A. Ground 1: Claims 1 and 3 are Obvious Over Okuno and Shin

1. Overview of Okuno (Ex-1004)

74. Because Okuno is in the same field (MOSFETs) and reasonably pertinent to a problem the '473 Patent purports to address (MOSFET fabrication), Okuno is analogous art. Ex-1001 at 1:15-17; Ex-1004 at [0002].

75. Okuno is directed to “a gate structure of a MOS semiconductor device and a manufacturing method of the same.” Ex-1004 at [0001]. Specifically, Okuno concerns “reducing the size of a SRAM” and the “protruding amount” of each gate pattern (i.e., “the setback position of a gate end portion”). *Id.* at [0004]. The gate protruding amount needs to be sufficiently provided in advance when the resist patterns are formed, and this in turn requires sufficient spacing “d” to be provided between the active regions 18. *Id.*

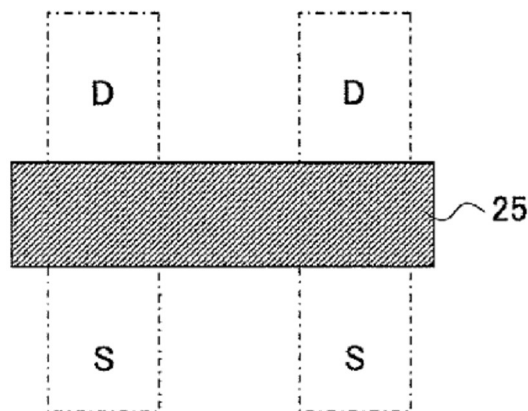
FIG.2



Okuno, Fig. 2

76. Okuno discloses etching “the gate electrode” as a straight and continuous gate pattern (Fig. 6A). *Id.* at [0026].

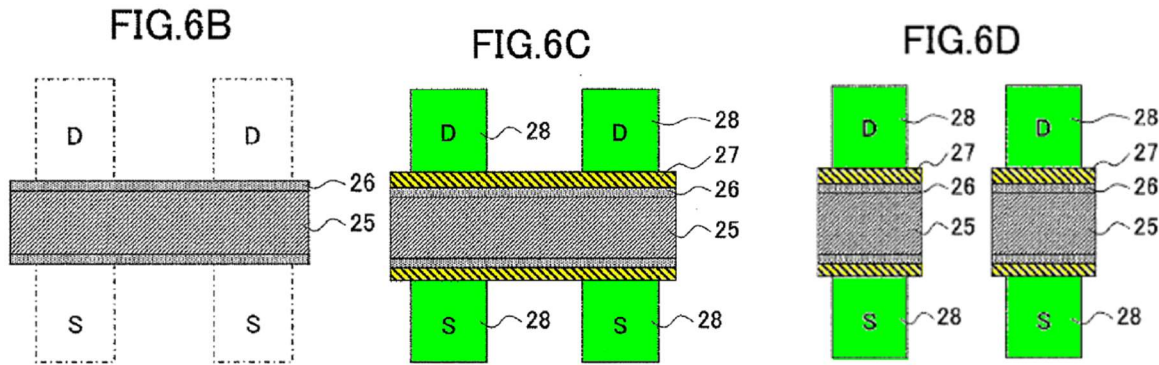
FIG.6A



Okuno, Fig. 6A

77. While maintaining the continuous gate electrode, Okuno forms “pocket

region 26,” “sidewalls 27,” and “source/drain regions 28.” *Id.* at [0026], Figs. 6B-C. Lastly, the gate is cut and divided to form gate individual gate electrodes. *Id.* at [0026], Fig. 6D.

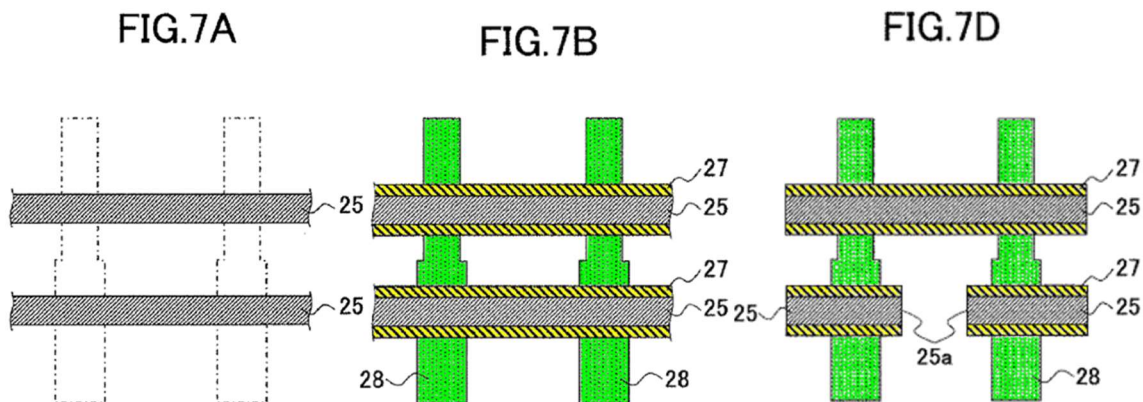


Okuno, Figs. 6B-D

78. Because gate separation is performed last, “the sidewalls 27 are provided only in the longitudinal direction of the gate ... and are therefore absent from the intervening region between two opposing driver transistors.” *Id.* at [0028]. The absence of spacers on the cut edges “contribut[es] to the size reduction of the cell structure.” *Id.*; *see also id.* at [0041] (“the extending width of the pocket implantation and the extension implantation from the gate edges 25a is absent, the protruding amount obtained after the gate etching process can be reduced.”).

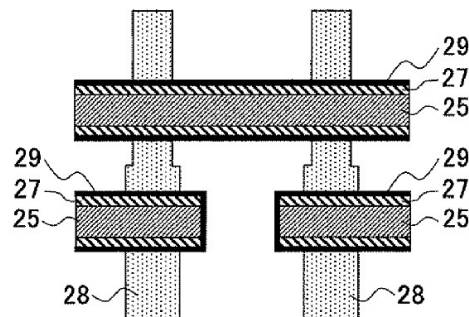
79. The basic concept outlined in Figs. 6A through 6D is further illustrated with respect to Figs. 7A through 7D. Active regions are formed with an element separating region such as STI on a silicon substrate. *Id.* at [0031]. Thereafter, gate patterning is performed to create straight and continuous patterns of the gate

electrodes 25 (Fig. 7A), and spacers 27 are formed followed by **source/drain** formation (Fig. 7B). Lastly, gate structures are cut and separated in predetermined shape (Figs. 7C-7D). *Id.* at [0032]-[0035]. At this point, the basic structure of Okuno's embodiment is completed. *Id.* at [0035].



Okuno, Figs. 7A, 7B, and 7D

80. Okuno provides another embodiment in which, after separation of the gate electrodes 25, thin sidewalls 29 are optionally formed using a CVD oxide film, covering the gate edges 25a of the gate electrodes 25 exposed after the cut and separation process. *Id.* at [0036], Fig. 7E.



Okuno, Fig. 7E

81. Okuno expressly describes when one would elect to perform the additional step of forming thin sidewalls, stating as follows:

Note however that, depending on conditions of a subsequent silicide process, silicide may eat away in the lateral direction (gate width direction) from cut gate edges 25 *a*. In that case, the silicide corrosion from the gate edges 25 *a* can be prevented by carrying out the following processes.

Id. at [0035].

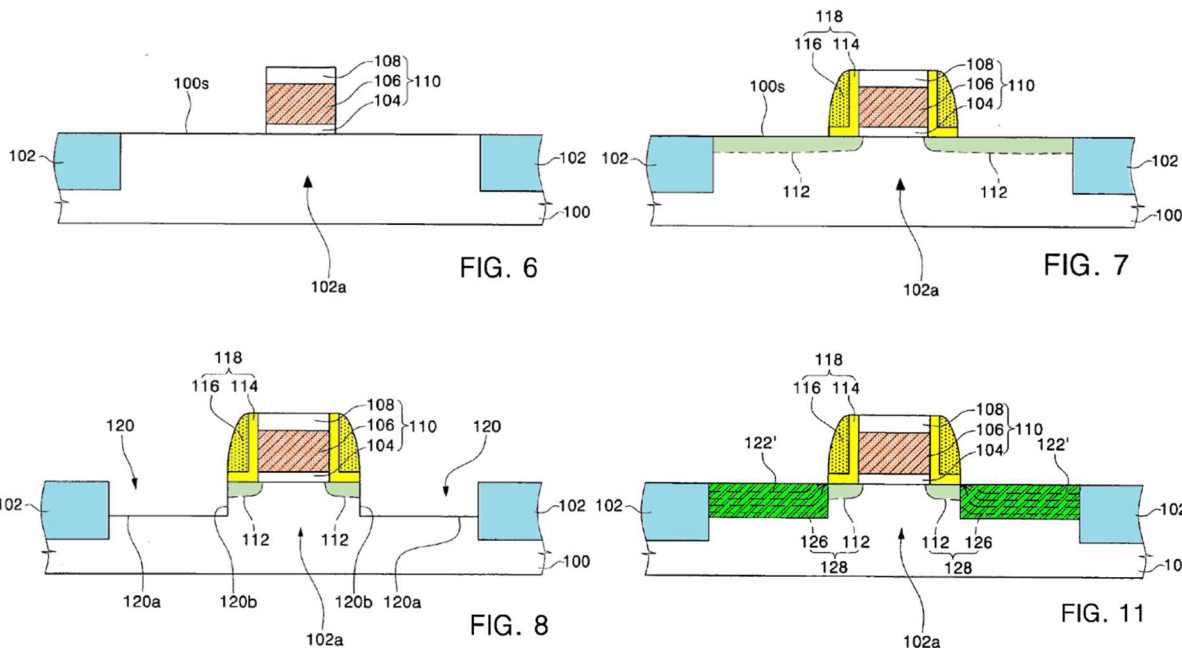
2. Overview of Shin (Ex-1006)

82. Because Shin is in the same field (MOSFETs) and reasonably pertinent to a problem the '473 Patent purports to address (MOSFET fabrication), Shin is analogous art. Ex-1001, 1:15-17; Ex-1006, [0005].

83. Shin similarly addresses methods for implementing “high-performance” MOS transistors as they “scale down i[n] size.” Ex-1006 at [0005]. As Shin explains, when scaling down the MOS transistor size, the channel length is reduced, junction depths of source and drain regions should also be reduced, but this leads to an increase of on-resistance. *Id.* at [0005]. To overcome this problem, selective epitaxial growth was employed, which introduces tensile or compressive stress to the channel region to increase the mobility of carriers in the channel region. *Id.* at [0010].

84. Shin’s fabrication is as follows. Active region 102a is separated from

others with an isolation layer 102, and a **gate pattern 110** made of gate insulating layer 104, a gate electrode 106, and a capping layer pattern 108 is formed. *Id.* at [0081], Fig. 6. Next, **low concentration impurity regions 112** are made via LDD implants, and then spacers 118—made of an oxide spacer 114 and nitride spacer 116—are formed. *Id.* at [0082], Fig. 7. Then **epitaxial layers 122** made of silicon carbide (SiC) or silicon germanium (SiGe) are formed in recesses 120. *Id.* at [0083]-[0089]. Finally, ion implantation is performed to form **source/drain regions 126**, resulting in higher-doped and deeper source/drain regions 126 connecting to the lower-doped LDD regions 112, creating combined optimum doping profiles 128 at both sides of the gate pattern 110. *Id.* at [0090].

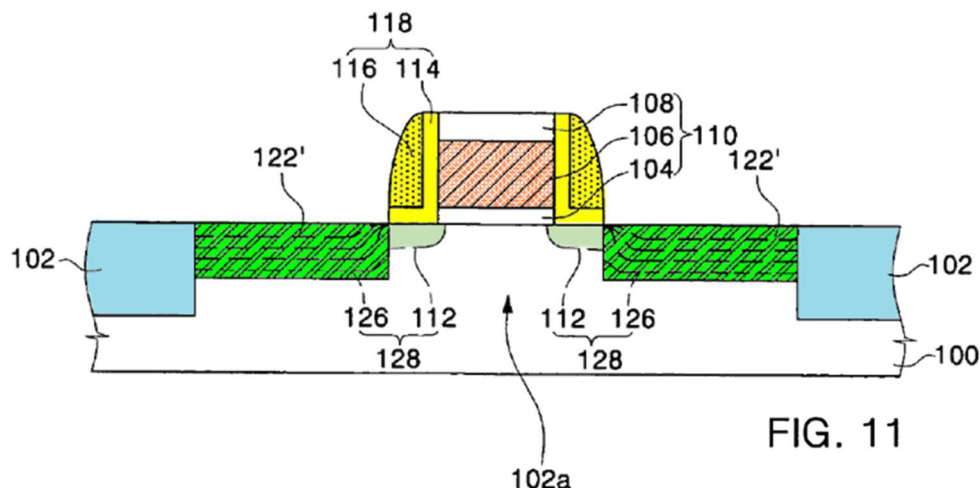


3. Combining Okuno and Shin

85. Okuno and Shin disclose similar MOS transistors fabricated on a bulk

substrate. Ex-1004 at [0002]; Ex-1006 at [0005]. Both disclose common elements of a MOS transistors, including an STI (Ex-1004 at [0031]; Ex-1006 at [0005], [0081]) and spacers. Ex-1004 at [0026] (sidewall spacers 27); Ex-1006 at (insulating spacers 118). Both utilize an LDD. For example, Okuno discloses performing “extension implantation” (Ex-1004 at [0026] at [0033]), which a POSITA would have understood from prior training to mean an LDD. Ex-1034 at 4:14-23, Fig. 1; Ex-1035 at [0021]; Ex-1031 at [0007]; Ex-1040 at 1:46-51; Ex-1041 at [0017]; §VI.B. Similarly, Shin teaches forming “low concentration impurity regions 112” by implanting impurity ions. Ex-1006 at [0082]. Further, Okuno and Shin seek to solve problems related to miniaturization of transistors. Okuno seeks to reduce spacing between the neighboring transistors by reducing the “setback amount.” Ex-1004 at [0004], Figs. 3A-C. Shin seeks to overcome the short channel effect, which becomes a greater problem as MOS devices are scaled down and the channel length is reduced. Ex-1006 at [0005].

86. Although Okuno does not disclose growing an epitaxial layer, Shin provides that teaching. In particular, Shin discloses growing epitaxial layers 122 in recesses 120 adjacent to two sides of the gate pattern 110. Ex-1006 at [0084] (“Referring to FIG. 9, epitaxial semiconductor layers 122 are selectively formed in the recesses 120 using the same methods as the processing steps 5, 7, 9, 11, 13, 15, 17 and 19 shown above in FIGS. 1A and 1B.”), Fig. 11.



Shin, Fig. 11

87. A POSITA would have found it obvious to fabricate Okuno's transistors by forming epitaxial source/drain regions, as Shin teaches, to add advantageous strain in Okuno's transistors. Ex-1004 at [0026]; Ex-1006 at [0084]; Ex-1031 at [0021]-[0026]; Ex-1033 at [0044]. An epitaxial source/drain region would introduce compressive or tensile stress (i.e., well-known benefit of a SEG process) and increase carrier mobility of Okuno's device. Ex-1030 at 1:20-34, 3:43-52, 4:19-33; Ex-1006 at [0084]; Ex-1031 at [0010]; §VI.C, *supra*. Indeed, a POSITA would have recognized that using epitaxial source/drain would enable Okuno's device to have shorter channel length and higher drive current and thereby further Okuno's goal of increasing transistor density.

88. Forming an epitaxial source/drain in the recesses was a well-known technique. From years before July 15, 2010, it was known that SiGe or SiC can be grown epitaxially in the source/drain regions to introduce stress and in turn increase

the carrier mobility and drive current. §VI.C, *supra*. It was also known that the SEG process entails forming recesses adjacent to the gate structure and backfilling the recesses with an epitaxial SiGe layer to create compressive stress (in a PMOS transistor) or with an epitaxial SiC layer to create tensile stress (in an NMOS transistor). Ex-1030 at 2:37-49, 2:62-65, 4:33-46; Ex-1006 at [0010] at [0084]; Ex-1031 at [0018]-[0021]; §VI.C, *supra*. A POSITA looking for ways to introduce stress in Okuno's substrate and improve its drive current while providing punchthrough suppression and would have looked to Shin for implementation details about SEG. Shin was readily available by the time Okuno was filed and published. And like Okuno, Shin is directed to manufacturing method for semiconductor devices and, in particular, facilitating size reduction of MOS devices. *E.g.*, Ex-1004 at [0004]-[0005]; Ex-1006 at [0005].

89. Moreover, Okuno is directed to SRAM (static random access memories), which consists of multiple CMOS inverters, which in turn consist of a pair of PMOS and NMOS devices. Ex-1004 at [0003]. A POSITA would have found Shin's teachings—which address the short channel effect in small MOS devices—to be directly applicable to and beneficial for Okuno's device. Ex-1006 at [0003].

90. A POSITA would have had a reasonable expectation of success in forming recesses adjacent to Okuno's spacers 27 and backfilling the recesses with

an epitaxial layer, as disclosed in Shin. The modification would have been minor and within the expertise of a POSITA. Shin's epitaxial layer is grown in recesses 120 in the semiconductor substrate after the formation of the spacers but before the source/drain regions 126 are formed by ion implantation. Ex-1006 at [0038] at [0090]. Okuno likewise discloses the conventional steps of forming the spacers 27 and then performing source drain implantation to form source drain regions 28. Ex-1004 at [0026], [0033]. Shin's SEG process would have simply been added after Okuno's spacer formation and before source/drain implantation. Ex-1006 at [0038], [0090]; Ex-1004 at [0026], [0033]. After forming recesses in the substrate adjacent to the gate and performing SEG, a POSITA would have proceeded with the remaining steps taught by Okuno, including separation of the gate pattern. Ex-1004 at [0028], [0032]-[0035], Figs. 6C, 6D, 7C, 7D.

91. A POSITA would have viewed this as an obvious example of (1) implementing a known technique (selectively growing an epitaxial layer) to improve known devices (MOS devices) to achieve predictable results (introducing mechanical stresses into the channel region to improve carrier mobility and overcoming the short channel effect); (2) a choice from a finite number of identified, predictable solutions (forming source/drain regions mainly through selective epitaxial growth and/or ion implantation); and (3) a teaching, suggestion, or motivation in the prior art (*see* Ex-1006 at [0084]) that would have led a POSITA to

modify Okuno's MOS transistor to include epitaxially grown source/drain regions, as Shin teaches, to arrive at the claimed invention.

4. Claim 1

(a) 1[pre]: "A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:"

92. To the extent the preamble is limiting, Okuno discloses a "method for fabricating a metal-oxide semiconductor (MOS) transistor" because Okuno discloses "a manufacturing method" for fabricating transistors for static random access memories (SRAMs). *See* Ex-1004 at [0002] (Okuno's invention is directed to "a gate structure of a MOS semiconductor device and a manufacturing method of the same"); [0031] (describing formation of a silicon substrate, a gate oxide film, and a polysilicon film). Specifically, Okuno discloses cutting and dividing a gate structure to form separate gate electrodes after forming the source/drain regions. *Id.* at [0026].

(b) 1[a]: "providing a semiconductor substrate;"

93. Okuno discloses "providing a semiconductor substrate" because Okuno discloses fabricating its MOS devices "on a silicon substrate." *See* Ex-1004 at [0031] ("[A]ctive regions of the SRAM are defined by forming an element separating region (not shown), such as STI (shallow trench isolation), on a silicon substrate.").

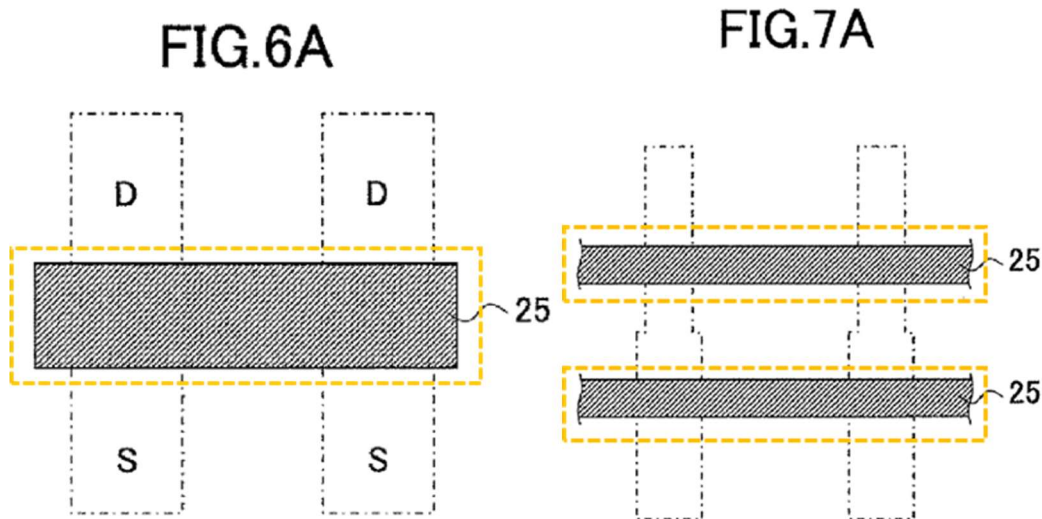
(c) 1[b]: “forming a silicon layer on the semiconductor substrate;”

94. Okuno discloses “forming a silicon layer on the semiconductor substrate” because Okuno discloses depositing a polysilicon film (“silicon layer”) over a gate oxide film on the semiconductor substrate for forming the gate, consistent with the ’473 Patent. Ex-1004 at [0031]. As the ’473 Patent explains, “a polysilicon layer” is formed on a “gate insulating layer” that is “deposited on the surface of the semiconductor substrate 12.” Ex-1001 at 2:42-47, 2:55-61.

(d) 1[c]: “performing a first photo-etching process on the silicon layer for forming a gate pattern;”

95. Okuno discloses “performing a first photo-etching process on the silicon layer for forming a gate pattern” because Okuno discloses etching the polysilicon film and gate oxide film according to gate patterning to create “straight and continuous patterns of the gate electrodes 25.” Ex-1004 at [0031]-[0032]; *see also id.* at [0026] (“[E]tching of the gate electrode 25 is performed based on a straight and continuous gate pattern, as illustrated in FIG. 6A”). As Okuno explains, a “conventional method” of gate patterning is performed using a mask and an etchant to form the “gate electrode material film” into a “gate pattern.” *Id.* at [0032], [0026], Claim 6. A POSITA reading Okuno would have understood that a “photo-etching process” using a photoresist was used to selectively remove portions of the underlying structure to form the gate pattern. §VI.E. Figs. 6A and 7A show the gate

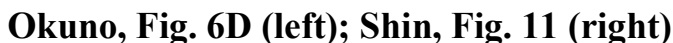
patterns.



Okuno, Figs. 6A, 7A

- (e) 1[d]: “forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and”

96. Okuno and Shin render 1[d] obvious. *See* §IX.A.3. Okuno discloses forming source/drain regions. Ex-1004 at [0034], [0026], [0010], Fig. 6D. Shin further discloses growing epitaxial SiGe or SiC layers in recesses in the substrate adjacent to two sides of the gate pattern for forming the source/drain regions. Ex-1006 at [0084], Fig. 11. As explained in Section IX.A.3, it would have been obvious to use epitaxial SiGe or SiC layer for the source and drain regions 28, as Shin teaches, in the semiconductor substrate adjacent to two sides of Okuno’s gate electrodes 25.



97. Okuno discloses this limitation because Okuno discloses that after source/drain regions are formed, another photoetching process is performed to cut and divide the gate electrodes (“gate pattern”) in designed shapes (i.e., into two gates). Ex-1004 at [0026], [0034]. For example, a mask 20 having a predetermined opening 21 is used to expose a portion of the gate electrode, and etching is then performed. *Id.* at [0034], Figs. 7C, 7D:

FIG. 7C

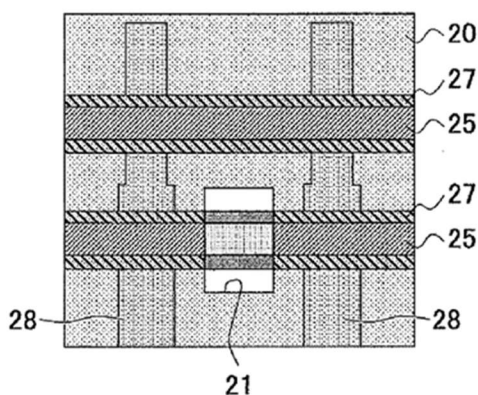
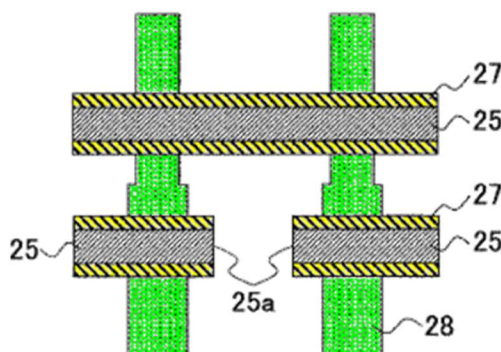


FIG. 7D



Okuno, Figs. 7C-7D

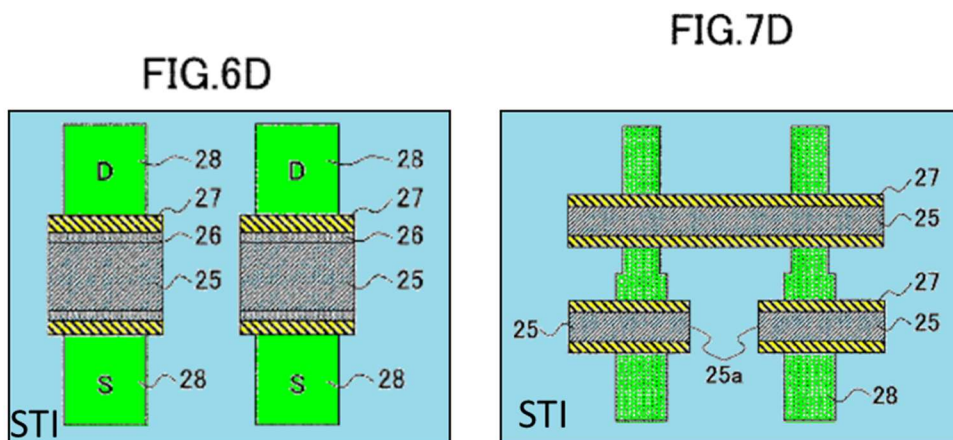
98. As illustrated above, the portion of the gate pattern removed under the predetermined opening 21 (i.e., the cut portion) forms a “slot” in the gate pattern to physically separate it into two separate gates.” *Id.* at [0035].

99. Because Okuno discloses performing the second photoetching process after the source and drain regions are formed, in Okuno-Shin, the second photoetching process would be performed after the formation of the epitaxial layer SiGe or SiC.

5. **Claim 3. “The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.”**

100. Okuno and Shin render claim 3 obvious. Okuno discloses that the semiconductor substrate comprises shallow trench isolation regions. Ex-1004 at

[0031] (“[A]ctive regions of the SRAM are defined by forming an element separating region (not shown), such as STI (shallow trench isolation), on a silicon substrate.”). Okuno’s figures below are annotated to include STI, consistent with Okuno’s description.



Okuno, Figs 6D and 7D (Annotated)

101. Okuno also discloses that “the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.” Okuno’s second photoetching applies a resist and mask to the entire surface to expose a gate cut portion and etches away exposed portions of the gate structure to divide a gate electrode 25 into separated gates. Ex-1004 at [0035]. In Okuno, the etching process may employ a reactive ion etching (RIE), a widely used technique, using chemically reactive plasma to etch away specific material. Ex-1004 at [0034] (using a mixed gas including hydrogen bromide (HBr) and oxygen). RIE is a widely used technique for removing silicon in semiconductor fabrication. This

process involves using chemically reactive plasma to etch away specific material, which in this case is the polysilicon film used for the patterned gate. *Id.* Adding HBr makes the etch profile more anisotropic, resulting in improved vertical etch profile, and the etching highly selective, ensuring precise and controlled removal of the polysilicon film that is disposed on the shallow trench isolation regions. *Id.*

B. Ground 2: Claims 1-10 are Obvious Over Chong and Okuno

1. Overview of Chong (Ex-1007)

102. Because Chong is in the same field (MOSFETs) and reasonably pertinent to a problem the '473 Patent purports to address (MOSFET fabrication), Chong is analogous art. Ex-1001, 1:15-17; Ex-1007 at [0003], [0009].

103. Chong discloses employing differential spacers to “manipulate[] the stresses created within a channel to maximize the performance of both” p-channel Field-Effect Transistor (PFET) and n-channel Field-Effect Transistor (NFET) in a CMOS configuration. Ex-1007 at [0003], [0009], [0026]. Chong explains that “[s]caling of the MOSFET ... has become a major challenge.” *Id.* at [0004]. “For example, as scaling of the MOSFET reaches the submicron era, intended and unintended strain effects can become a design problem,” necessitating “new methods ... to maintain the expected device performance enhancement from one generation of devices to the next.” *Id.* Conventional methods to improve the performance of a transistor device include increasing “the mobility of carriers” with

a strained channel, forming shallow trench isolation structures, and depositing etch stop layers. *Id.* at [0005]. Chong seeks to further improve carrier mobility with a punch-through suppression layer engineered to induce strain and suppress short channel effects. *Id.* at [0007], [0044].

104. Chong's CMOS device is fabricated as follows. An NFET device 102 and a PFET device 104 are formed "from conventional deposition, patterning, photolithography, and etching." *Id.* at [0029]. The PFET device 104, for example, includes a PFET gate 122, a PFET gate oxide 124, and a PFET channel 126. *Id.* at [0031]. Surrounding the PFET gate 122 are a PFET first liner 128 and a PFET first spacer 130, which may be made from materials that include oxygen and nitrogen, respectively. *Id.* The device also includes a PFET source/drain extension 132, which is "formed by a low to medium-dose implant" and "extends from the PFET channel 126 in the substrate 118 to facilitate dimensional reductions." *Id.* "A PFET cap 134, such as a nitride or an oxynitride cap, helps to protect the PFET gate 122 during subsequent processing steps." An isolation structure 136, such as a shallow trench isolation and/or a field oxide, is formed within the substrate 118. *Id.* at [0033].



s formed in the



Chong, Figs. 4-6

106. A PFET second liner 702 and a PFET second spacer 706 are then formed by blanket deposition followed by a subsequent etchback. *Id.* at [0049]-[0051], Fig. 7. The liner 702 and spacer 706 may be made from dielectric materials such as oxide and nitride and collectively form part of a differential spacer 708. *Id.* at [0051]-[0052].

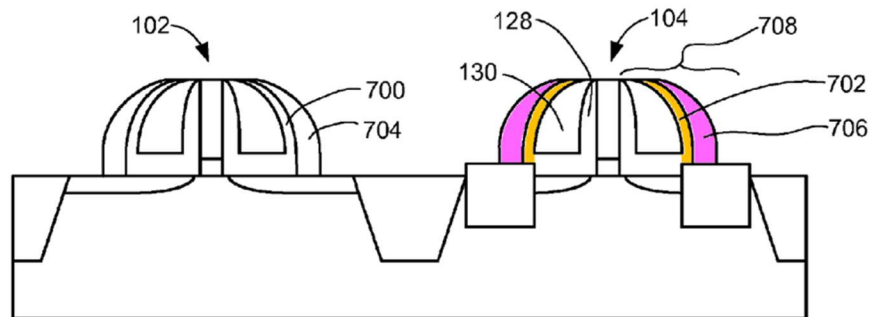


FIG. 7

Chong, Fig. 7

107. Thereafter, a differential spacer 902 and source/drain region 900 are formed on the NFET side. *Id.* at [0056]. To protect the PFET device from the source/drain implant step of the NFET source/drain 900, a mask 904 is formed over the PFET device 104. *Id.* at [0057], Fig. 9.

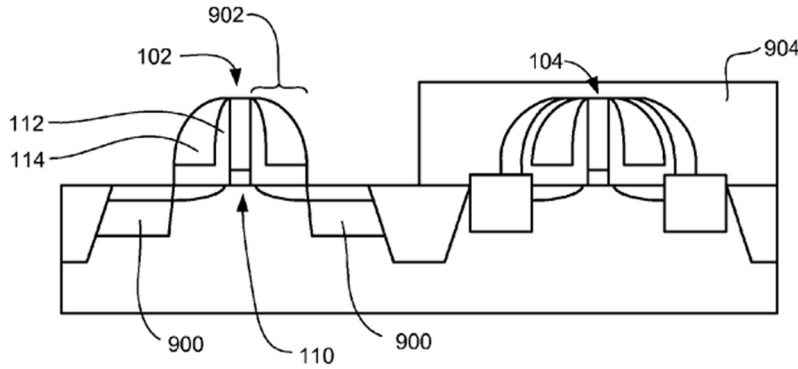


FIG. 9

108. Chong discloses that its invention “encompasses a differential spacer design that is not distinguished by the number of spacers.” Ex-1007 at [0027]. Chong also states that, although its PFET configuration is discussed with “a first spacer and a second spacer,” its invention “may encompass ... a design with more than two spacers.” *Id.*

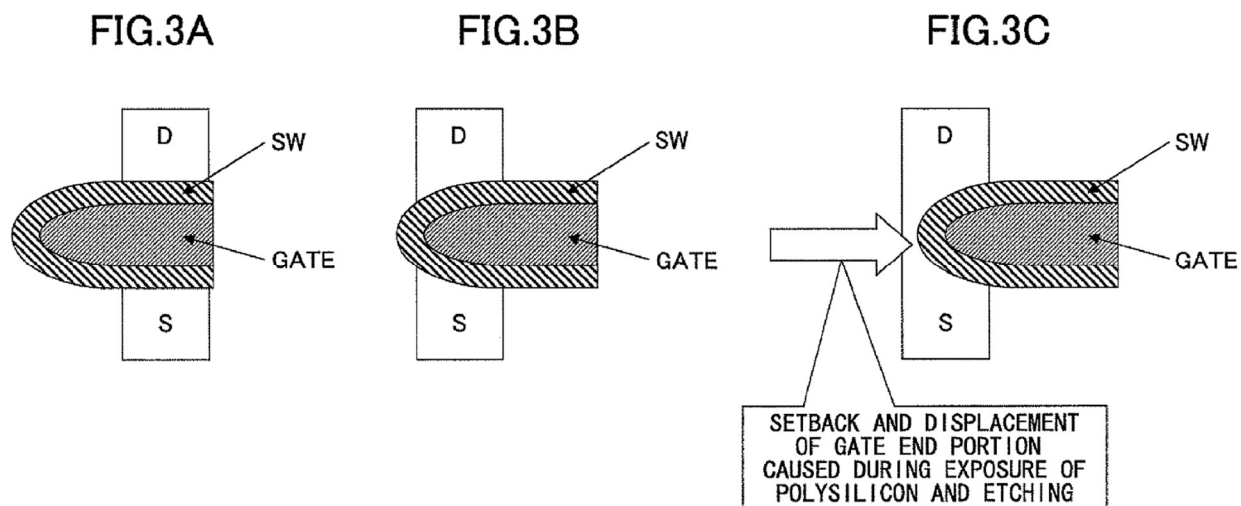
2. Combining Chong and Okuno

(a) A gate-cutting process to separate Chong’s gate structures for miniaturization

109. Chong and Okuno are similar. Both disclose MOS transistors fabricated on a bulk substrate. Ex-1004 at [0002]; Ex-1007 at [0003], [0009], [0026]. Both disclose common elements of a MOS transistors. As discussed for Ground 1, Okuno discloses an STI, spacers, and source/drain extensions. §IX.A.3, *supra*. Chong also discloses these elements. Ex-1007 at [0033] (isolation structure 136), [0031] (first liner 128, spacer 130, and source/drain extension 132).

110. Further, Chong and Okuno seek to solve problems related to

miniaturization of transistors. Okuno seeks to reduce spacing between the neighboring transistors by reducing the “protruding amount.” Ex-1004 at [0004], Fig. 2. A protruding amount is needed to account for a setback of the gate etching, which results in the formation of a gate shorter than the length indicated in the resist pattern. *Id.* at [0005]; §VI.F. If insufficient protruding amount is provided, the gate end could fail to overlap the active region (the source and drain), resulting in a defective device. *Id.* at [0006], Figs. 3B-C.



Okuno, Figs. 3A-C

111. An excessive protruding amount, on the other hand, would result in poor density, as devices would be spaced farther apart than necessary. Okuno discloses a gate separation technique that allows to form a sufficient protruding amount while spacing the transistors in a compact arrangement. Ex-1004 at [0009]-[0011], Fig. 10. Similarly, Chong seeks to mitigate unintended strain effects caused

by size reduction. Ex-1007 at [0004] (“[A]s scaling of the MOSFET reaches the submicron era, intended and unintended strain effects can become a design problem. Consequently, new methods must be developed to maintain the expected device performance enhancement from one generation of devices to the next.”).

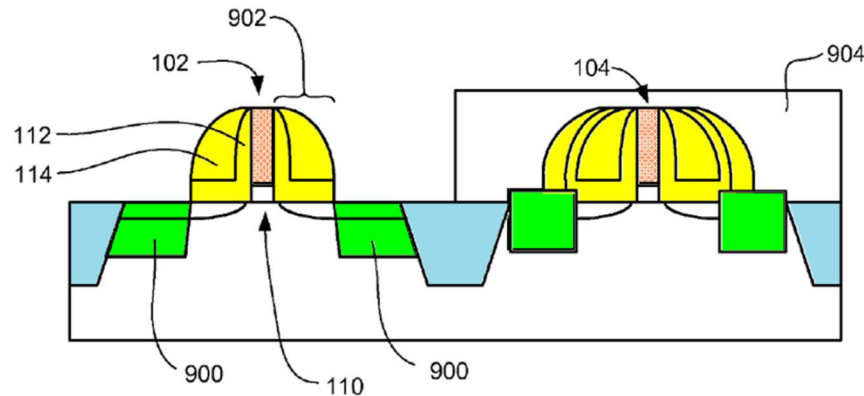
112. A POSITA would have found it obvious to separate Chong’s gate pattern into two gates, as disclosed by Okuno. §IX.A.4(f), *supra*; Ex-1004 at [0032]; Ex-1005 at [0036], [0038], Figs. 3-4; Ex-1026 at 5:1-35; Ex-1012 at [0025]-[0026]. A POSITA would have understood from prior training that there are only finite options for patterning gates: patterning individual gate separately or cutting a single patterned gate into multiple gates. As discussed in Section VI.F, *supra*, the latter method reduces spacing between transistors and achieve size reduction by overcoming the limits of photolithography. Therefore, a POSITA would have been motivated to perform gate cutting to further scale down Chong’s device while maintaining control over the strain effects.

113. Because Chong discloses fabrication of the gate structures but not the gate separation process, a POSITA would have looked to references such as Okuno for implementation details on gate separation. Moreover, Okuno is directed to SRAM (static random access memories), which consists of multiple CMOS inverters, which in turn consist of a pair of PMOS and NMOS devices. Ex-1004 at [0003]. Because Chong discloses improving the performance of both NFET and

PFET in the CMOS scheme, a POSITA would have found Okuno's teachings to be applicable to Chong. Ex-1007 at [0026], [0003].

114. Performing Okuno's second photoetching process *after* Chong has finalized the fabrication of the source/drain regions would also have been obvious. The '473 Patent admits both techniques (epitaxial layer formation and gate separation) were known (Ex-1001 at 1:28-42), and prior art expressly motivates separating the gate pattern after source/drain formation. Okuno is explicit that, with respect to the embodiment shown in Figs. 7A-7D, the second photoetching process is the last step. Ex-1004 at [0026] ("***Lastly***, after impurity implantation is completed, the gate is cut and divided to form gate electrodes in designed shapes."), [0035] (describing that, after gate separation is done as shown in FIG. 7C, "the basic structure according to one embodiment of the present invention is completed"); §IX.A.4(e), *supra*. Okuno explains that, because the gate structure is "cut and divided at the end," "impurities are not implanted into a part of the substrate region from which the gate pattern has been removed," resulting in symmetrical impurity properties. Ex-1004 at [0027]. Given Okuno's explicit disclosures, a POSITA would have been motivated to finalize Chong's source/drain regions (including any implantation) implantation step and before the second photoetching process to avoid causing asymmetry in the impurity characteristics. For example, a POSITA would have formed the PFET source/drain 502, formed the NFET source/drain 900, and

removed the third mask 904 (which was formed over the PFET 104 to protect it from the implant step of the NFET source/drain 900) before separating Chong's gate. Ex-1007 at [0048], [0055], [0057]. Chong's NFET and PFET gates would have been separated in one photoetching process for efficiency, as illustrated below.



Chong, Fig. 9

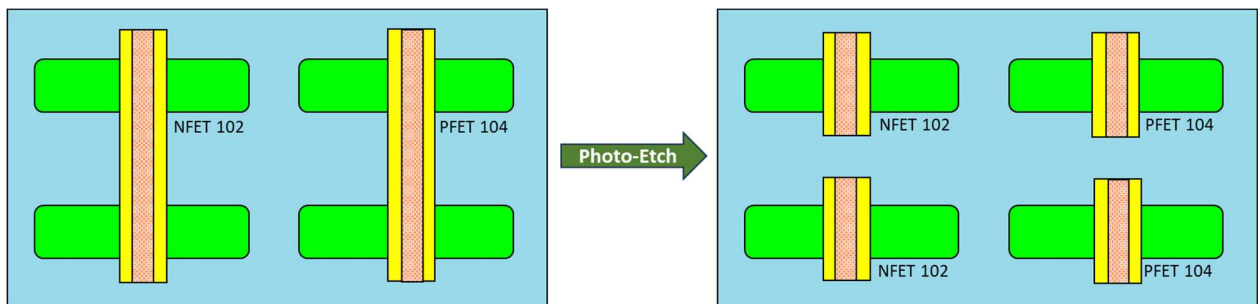


Illustration: Separation of Chong's Gates

This sequence would have prevented the NFET source/drain implant step from causing asymmetrical impurities in the gate end portions, especially in the NFET device 102, which unlike the PFET device 104 is not protected with a mask such as the mask 904 during the source/drain implant step. *Id.*

115. Performing the gate separation last is consistent with and supplements Chong's disclosures. Chong discloses forming an epitaxial layer by in-situ doping early in the fabrication process: before removing the hard mask 134, adjusting the source/drain concentration with ion implantation, and forming dielectric layers (liner 702 and spacer 706). Ex-1007 at [0044], [0047]-[0049], [0058]. If any of the steps for forming the source/drain regions (e.g., growing an epitaxial layer and formation of differential spacer) is performed after the gate separation, it will cause the same asymmetrical impurity problem that Okuno seeks to avoid. Ex-1004 at [0027]. In Chong-Okuno, a POSITA would thus be motivated to perform the second photoetching process after the completion of these earlier steps, including the formation of the epitaxial layer. After gate separation, a POSITA would have proceeded with the silicide formation step, as both Okuno and Chong teach. Ex-1004, [0037]; Ex-1007, [0060].

116. A POSITA would have had a reasonable expectation of success in adding a second photoetching step to Chong's fabrication method. It would have been well within a POSITA's expertise to use a conventional photoetch technique such as RIE (reactive ion etching) as disclosed by Okuno to separate the gate structures. Ex-1004 at [0034], Fig. 1. Indeed, As noted above, the '473 Patent admits that separating the gate pattern into two gates and growing an epitaxial layer in the source/drain regions are each a "[c]onventional approach." Ex-1001 at 1:28-

42.

117. The minimal extent of the modification further supports that a POSITA would have predicted success. As discussed above, Okuno and Chong's teachings supplement each other: after forming the gate structure as disclosed by Chong (e.g., formation of an epitaxial layer, removal of hard mask 134, and formation of liner 702 and spacer 706), a POSITA would have performed photoetching to separate the gates, as disclosed by Okuno. *Id.*; Ex-1007 at [0047]-[0049], [0058]. Separating the gates after the formation of the source/drain regions would have predictably improved the fabrication process by preventing impurities at the gate ends. Ex-1007 at [0044]; Ex-1004 at [0027] (cutting and dividing the gate structure "at the end" prevents impurities from being implanted where gates are cut and results in symmetrical impurity properties); §VI.F, *supra*.

118. A POSITA would have viewed this as an obvious example of (1) implementing a known technique (gate-cutting, through photoetching including the step such as RIE, after source/drain formation) to improve known devices (MOS devices) to achieve predictable results (reduced transistor spacing, size reduction, and symmetrical impurity characteristics); (2) a choice from a finite number of identified, predictable solutions (cutting a single patterned gate strip into multiple gates or patterning individual gate separately); and (3) a teaching, suggestion, or motivation in the prior art (*see* Ex-1004 at [0028]) that would have led a POSITA to

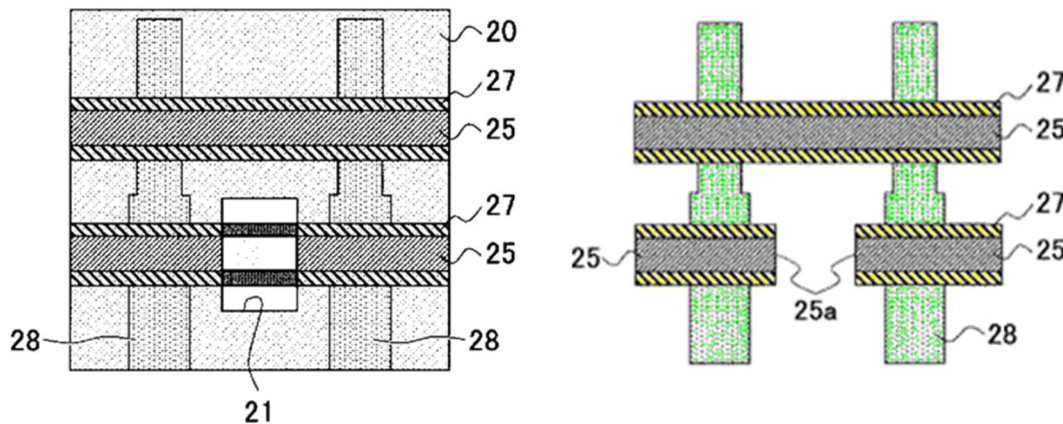
modify Chong's MOS transistor to separate the gate, as Okuno teaches, to arrive at the claimed invention.

(b) Gate separation after a dielectric layer is formed on the gate, leaving the cut edges free of the dielectric layer

119. When combining Okuno's gate separation step with Chong (which discloses forming a liner 702 and spacer 706 on the PFET device), a POSITA would have been motivated to sequence the gate separation so that the cut edges are free of any spacer materials (e.g., the liner 702 and spacer 706), as Okuno teaches, to reduce any "protruding amount" at the cut edge. Ex-1004 at [0041]-[0042].

120. Okuno expressly motivates leaving no dielectric spacers on the cut edges. Okuno discloses forming a spacer 27, forming the source drain region, and then performing a photoetch process as the last step to cut the gate. Ex-1004 at [0026] ("***Lastly***, after impurity implantation is completed, the gate is cut and divided to form gate electrodes in designed shapes."), [0035] (describing that, after gate separation is done as shown in FIG. 7C, "the basic structure according to one embodiment of the present invention is completed"); §IX.B.2(a), *supra*. As a result, "since the gate is cut and divided at the end," unlike the conventional method, "the sidewalls 27 are provided only in the longitudinal direction of the gate" and are "absent from the intervening region between two opposing driver transistors (FIG. 6(d))." *Id.* at [0028] (showing sidewall spacer 27 is absent in the cut slot). With

respect to the embodiment shown in FIGs. 6D and 7D, Okuno expressly discloses the size reduction benefit of leaving the cut edges exposed. *Id.* at [0028] (“This allows the space ‘d’ between the active regions 18 of FIG. 2 to be reduced, thus contributing to the size reduction of the cell structure.”). Because Okuno’s gate structure is “cut and divided at the end,” “impurities are not implanted into a part of the substrate region from which the gate pattern has been removed,” resulting in symmetrical impurity properties. *Id.* at [0027].



Okuno, Figs. 7C-7D

121. Following Okuno’s express teaching, a POSITA would have sequenced Okuno’s gate separation with Chong such that the gate’s differential spacer 708 (including **liner 702** and **spacer 706**) is not left on the cut edges. Ex-1007 at [0049]-[0052], Fig. 7.

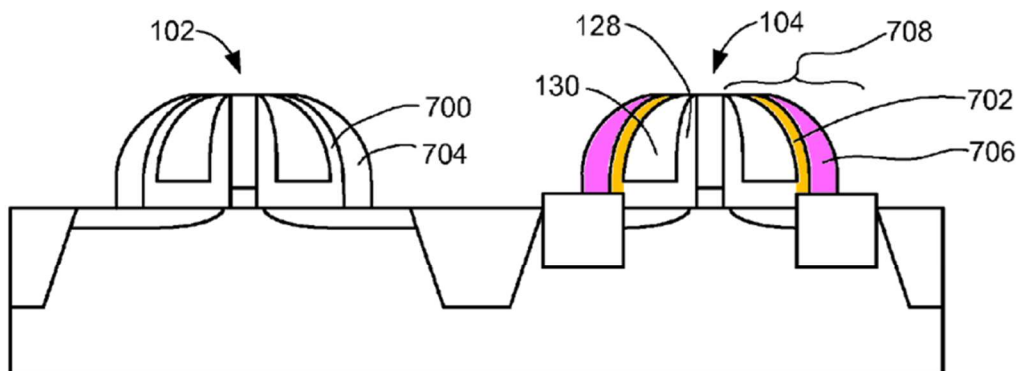


FIG. 7

Chong, Fig. 7

122. Otherwise, if Chong's liner 702 and spacer 706 are deposited after Okuno's second photoetching process, the two dielectric layers would cover the transverse edges, contrary to Okuno's explicit teaching. Thus, consistent with Okuno's disclosures, a POSITA would have deposited the liner 702 and spacer 706 on Chong's PFET gate 122 before performing the second photoetching process. *Id.*

123. Performing the gate separation after the deposition of the liner 702 and spacer 706 would have yielded predictable benefits. Chong discloses implanting impurities in the NFET source/drain 900 after the formation of the liner 702 and spacer 706 and protecting the PFET with a mask 904 during this implant step. Ex-1007 at [0057], Fig. 9. In view of Okuno's teaching, a POSITA would have understood that performing gate separation last (i.e., after the formation of the liner 702 and spacer 706 and the NFET source/drain implant step) would further protect

the PFET device from the source/drain implantation and increase the symmetry of the impurity characteristics, resulting in stable operating characteristics.

124. The size reduction benefit of leaving no spacer material on the cut edges further supports that it was obvious to separate the gates after the liner 702 and spacer 706 are deposited. Chong, like Okuno, seeks to achieve “[s]ize reduction.” Ex-1007 at [0004]; Ex-1004 at [0004]. Cutting the gates after the liner 702 and spacer 706 are deposited would leave no spacers on the cut edges, allowing the gates to be packed more closely together and enable size reduction.

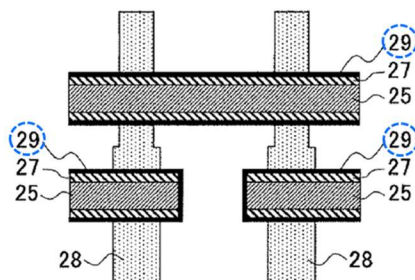
(c) Adding thin sidewall spacers after gate separation to prevent silicide corrosion

125. After the gate structures are separated by a photoetch process, a POSITA would have been motivated to form thin sidewalls around the gate structures to protect the gate structures from silicide corrosion, as Okuno teaches.

126. Chong contemplates forming additional spacers. Chong discloses that its invention “encompasses a differential spacer design that is not distinguished by the number of spacers.” Ex-1007 at [0027]. Chong also states that, although its PFET configuration is discussed with “a first spacer and a second spacer,” its invention “may encompass ... a design with more than two spacers.” *Id.*

127. Okuno provides an example of a MOS device having multiple spacers, e.g., one above extension implantation 27 and another spacer 29 for silicide protection. Ex-1004 at [0041], [0036], Figs. 6D, 7E. For example, Okuno discloses

an embodiment in which, after gate separation, a CVD oxide film is optionally deposited and patterned to form **thin sidewalls 29** on the cut edges. Ex-1004 at [0036], Fig. 7E. The thin sidewalls “cover the gate edges 25a of the gate electrodes 25 exposed after the cut and separation process.” *Id.* at [0036]. Okuno explains the rationale for adding the optional CVD oxide film and the thin sidewalls as follows: “depending on conditions of a subsequent silicide process, silicide may eat away in the lateral direction ... from cut gate edges 25a,” and “[i]n that case, the silicide corrosion from the gate edges 25a can be prevented by” forming the thin sidewall. *Id.* at [0035]-[0036].



Okuno, Fig. 7E

128. Chong’s device, as modified in view of Okuno (illustrated below), includes an **additional layer of spacers** (e.g., Okuno’s thin sidewalls 29).

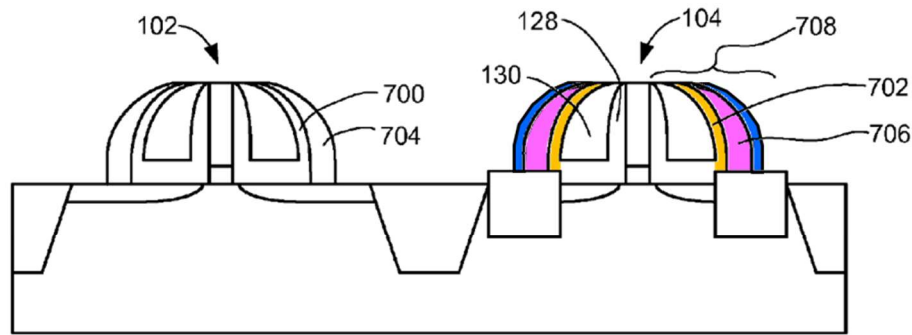


FIG. 7

Chong, Fig. 7 (Modified)

As Okuno expressly teaches, forming a dielectric layer after gate separation and forming spacers such as the thin sidewall spacers 29 from the dielectric layer would create spacers on the cut edges, protecting the gate edges 25a from the subsequent silicide process.

129. A POSITA would have predicted success in forming the thin sidewalls 29 in the Chong-Okuno combination. The thin sidewalls 29 can be formed on the gate structures from a well-known dielectric material using a conventional deposition technique (e.g., a CVD oxide film having a width of about 5 nm to 20 nm), as disclosed by Okuno. *Id.* at [0036].

130. Further, in forming the thin sidewalls 29, it would be obvious to pattern (i.e., etch back) Chong's differential spacers 708 (comprising liner 702 and spacer 706) either before or together with Okuno's thin CVD film. Both options would have been obvious to try. I have been informed that when there is a design need or

market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art is considered to have had good reason to pursue the known options within his or her technical grasp. I have also been informed that when there are only two or three possibilities, a POSITA had good reason to pursue both.

131. Here, Chong discloses forming the differential spacers 708 by blanket deposition followed by a subsequent etch back (Ex-1007 at [0049]), and there are two known options for sequencing the etch back of Chong's differential spacers 708 with the patterning of an additional dielectric layer (e.g., Okuno's thin CVD film): the differential spacers 708 can be patterned before or together with the additional dielectric layer. Both Okuno and Chong disclose that dielectric layers can be patterned using a conventional technique such as RIE. Ex-1004 at [0034]; Ex-1007 at [0053]. The '473 Patent also admits that forming spacers on the sidewall of a gate was a conventional technique. Ex-1001 at 1:26-42. Using a conventional technique, a POSITA would have tried patterning the differential spacers 708 either before or simultaneously with an additional dielectric layer (e.g., Okuno's thin CVD film). The etching sequence would not have affected the purpose for which the dielectric layers are deposited, i.e., serving as spacers and providing protection for the gate structures. Whether differential spacers 708 are patterned before or together with the additional dielectric layer (e.g., Okuno's CVD oxide film), the end product

would have been the same: the device would have (1) spacers comprising only the additional dielectric layer in the cut edges and (2) spacers comprising both the additional dielectric layer and the differential spacers 708 in the remaining edges.

3. Claim 1

(a) 1[pre]: “A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:”

132. To the extent the preamble is limiting, Chong discloses a “method for fabricating a metal-oxide semiconductor (MOS) transistor” because Chong discloses methods for forming NFET device and a PFET device with differential spacers. *See* Ex-1007 at [0003], [0009], [0026]. In Fig. 1, the PFET device 104, for example, is a MOS transistor. *Id.* at [0029], Fig. 1.

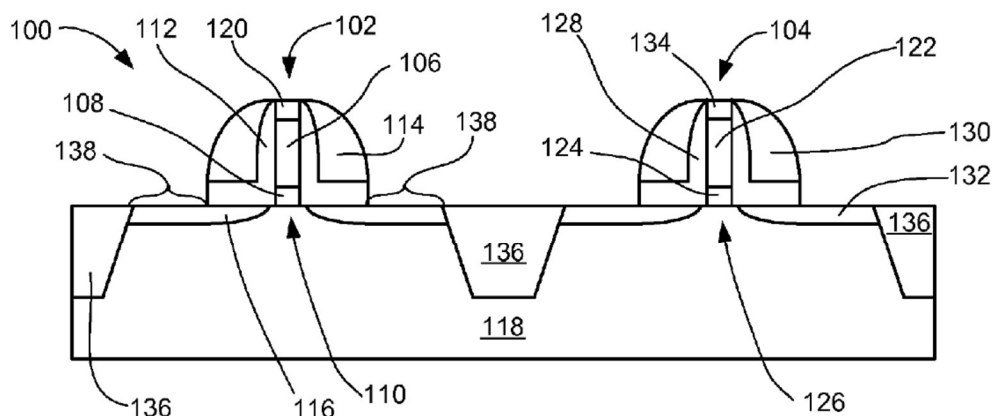


FIG. 1

Chong, Fig. 1

(b) 1[a]: “providing a semiconductor substrate;”

133. Chong discloses “providing a semiconductor substrate” because Chong discloses fabricating MOSFET on a semiconductor substrate, such as a substrate 118

that may include “a bulk semiconductor substrate.” *See* Ex-1007 at [0003], [0031], [0034], Fig. 1.

(c) 1[b]: “forming a silicon layer on the semiconductor substrate;”

134. Chong discloses “forming a silicon layer on the semiconductor substrate” because Chong discloses depositing a PFET gate 122 (“silicon layer”) over a PFET gate oxide 124 on the semiconductor substrate, consistent with the ’473 Patent. Ex-1007 at [0031]; Ex-1001 at 2:42-47, 2:55-61 (explaining that “a polysilicon layer” is formed on a “gate insulating layer” that is “deposited on the surface of the semiconductor substrate 12”). In Chong, the PFET gate 122 may include “any type of conducting material, such as silicon [and] polysilicon.” Ex-1007 at [0032], Fig. 1.

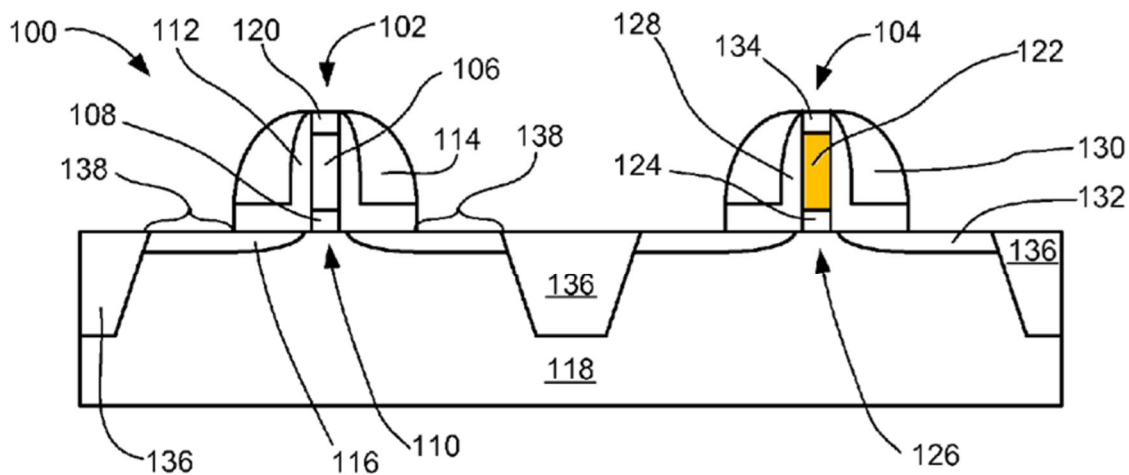


FIG. 1

Chong, Fig. 1

(d) 1[c]: “performing a first photo-etching process on the silicon layer for forming a gate pattern;”

135. Chong discloses “performing a first photo-etching process on the silicon layer for forming a gate pattern” because Chong discloses forming a gate pattern comprising a PFET gate 122, PFET cap 134, and PFET gate oxide 124. Ex-1007 at [0030], [0031], Fig. 1. Chong discloses that “conventional deposition, patterning, photolithography, and etching” are used to form a PFET device 104. *Id.* at [0029], *see also* [0030]-[0031]. Photolithography entails applying a photoresist on a wafer, placing a mask with predetermined patterns over the wafer, and etching away the exposed portions of the photoresist and the underlying structure. Ex-1012 at [0003], [0025]-[0026]; §VI.E. To etch away undesired portions to form the PFET gate 122 and PFET cap 134, a POSITA would recognize, or at least found it obvious, that a photoetching process is performed. The ’473 Patent admits that using a photo-etching process “to pattern the polysilicon layer and the hard mask into a gate” is a “[c]onventional approach” of gate fabrication. Ex-1001 at 1:28-36.

(e) 1[d]: “forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and”

136. Chong discloses this limitation. Chong discloses forming recesses 400 in the semiconductor substrate 118 adjacent to two sides of the gate structure. Ex-1007 at [0038] (“formation of a PFET recess 400 in the substrate 118”). Within the recesses 400, a punch-through suppression layer 500 may be formed from

“epitaxially grown silicon germanium” to induce strain within the channel. *Id.* at [0040]-[0044].

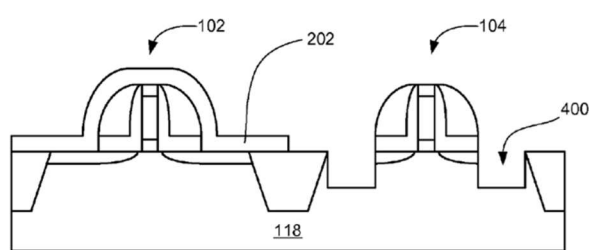


FIG. 4

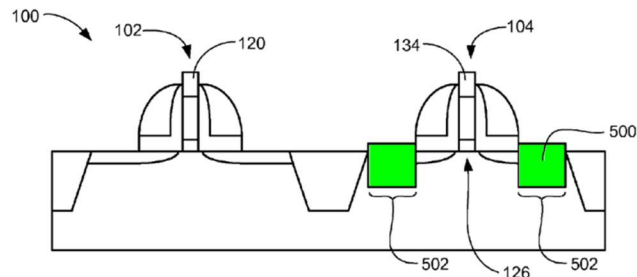


FIG. 5

Chong, Figs. 4-5

- (f) 1[e]: “after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.”

137. Chong and Okuno render 1[e] obvious. In Chong-Okuno, after the punch-through suppression layer 500 is epitaxially grown to form the source/drain regions (Ex-1007 at [0040]-[0044]) and after the NFET source/drain implant is complete (*id.* [0055]-[0057]), a second photoetching would be performed to separate the gates, as disclosed by Okuno. Ex-1004 at [0026], [0034] (describing that a portion of the gate electrode is exposed using a mask 20 with a predetermined opening 21 and then etched), Figs. 7C, 7D; §IX.B.2(a), *supra*. The photoetching process is performed “while using the gate pattern to physically separate the gate pattern into two gates” because it is performed “to obtain gate structures cut and separated in predetermined shapes.” *Id.* at [0035]. And as shown in Okuno’s Fig.

7D, the cut portions between the gate electrodes 25 “form a slot in the gate pattern.”

FIG. 7C

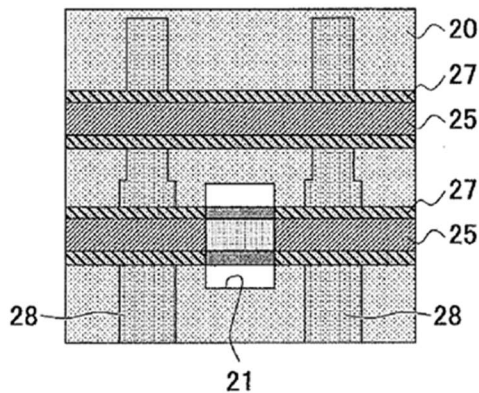
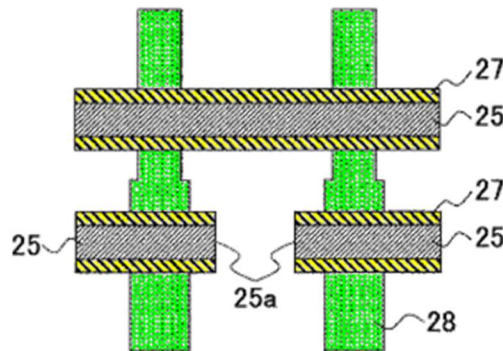


FIG. 7D



Okuno, Figs. 7C-7D

4. Claim 2. “The method of claim 1, wherein after forming the silicon layer comprises:”

138. Chong and Okuno render claim 2 obvious by performing the following steps after forming the silicon layer.

(a) 2[a] “forming a hard mask on the silicon layer;”

139. Chong discloses 2[a] by forming a [PFET cap 134](#), such as a nitride or an oxynitride cap, on the silicon layer 128. Ex-1007 at [0031].

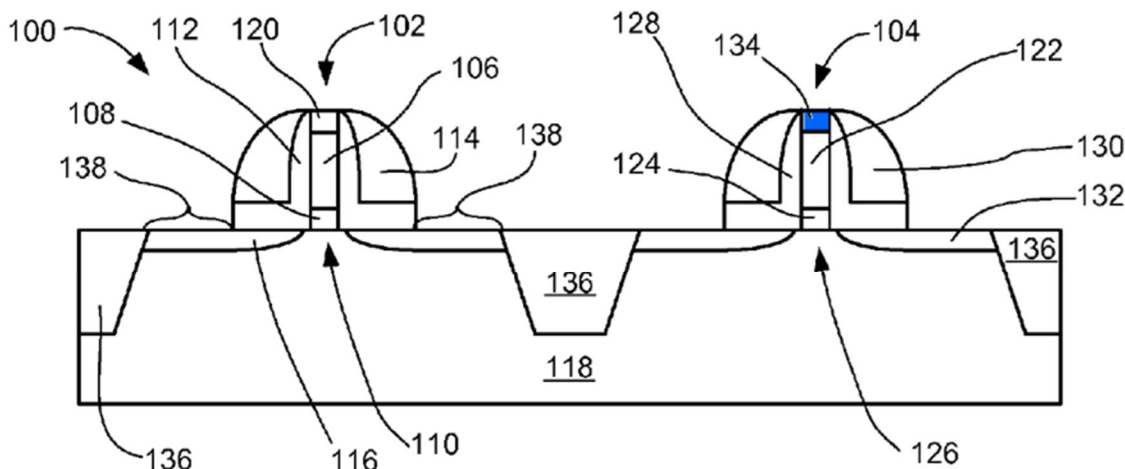


FIG. 1

Chong, Fig. 1

140. Chong's PFET cap 134 is a "hard mask" because it is a cap layer intended to "help[] to protect the PFET gate 122 during subsequent processing steps," consistent with the '473 patent. *Id.* As the '473 patent explains, "the hard mask could be selected from a material consisting of SiO₂, silicon nitride, and SiON." Ex-1001 at 2:47-49.

(b) 2[b] "performing the first photo-etching process on the hard mask and the silicon layer for forming the gate pattern;"

141. Chong discloses 2[b] because it discloses performing the first photo-etching process on the gate structure comprising a PFET cap 134, PFET gate 122, and PFET gate oxide 124 to form the gate pattern, as discussed for 1[c]. Ex-1007 at [0029], [0031]; §IX.B.3(d), *supra*.

(c) 2[c] “forming a first spacer around the gate pattern;”

142. Chong discloses 2[c] because it discloses forming a first liner 128 and a first spacer 130 surrounding the gate 122. Ex-1007 at [0031], Fig. 1.

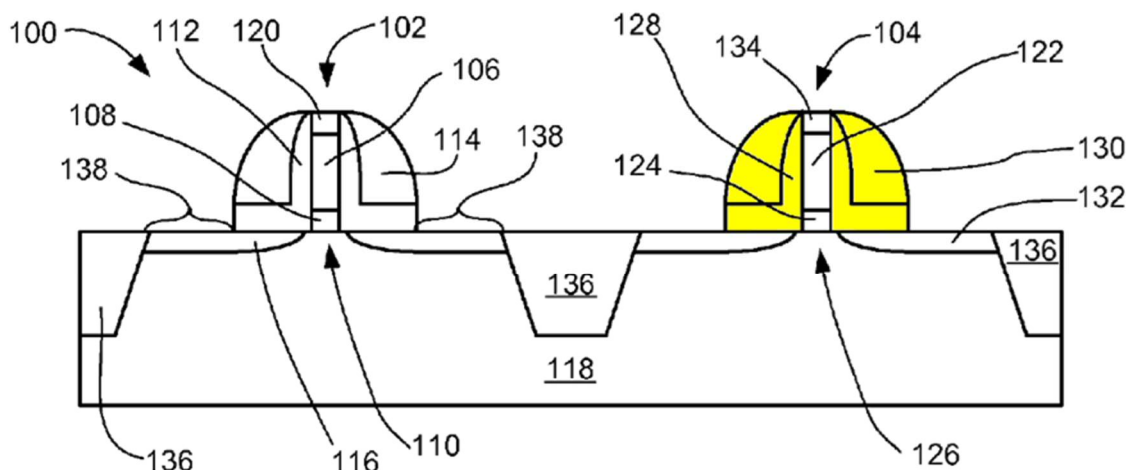


FIG. 1

Chong, Fig. 1

143. In Chong, the first liner 128 and first spacer 130, individually and collectively, are the “first spacer” formed around the gate pattern.

(d) **2[d] “forming a lightly doped drain in the semiconductor substrate adjacent to two sides of the gate pattern;”**

144. Chong discloses 2[d] because it discloses forming, adjacent to two sides of the gate structure, a source and drain extension 132 (the claimed “lightly doped drain”) by “a low to medium-dose implant” to “facilitate dimensional reductions for the scaling of the” MOSFETs. Ex-1007 at [0031].

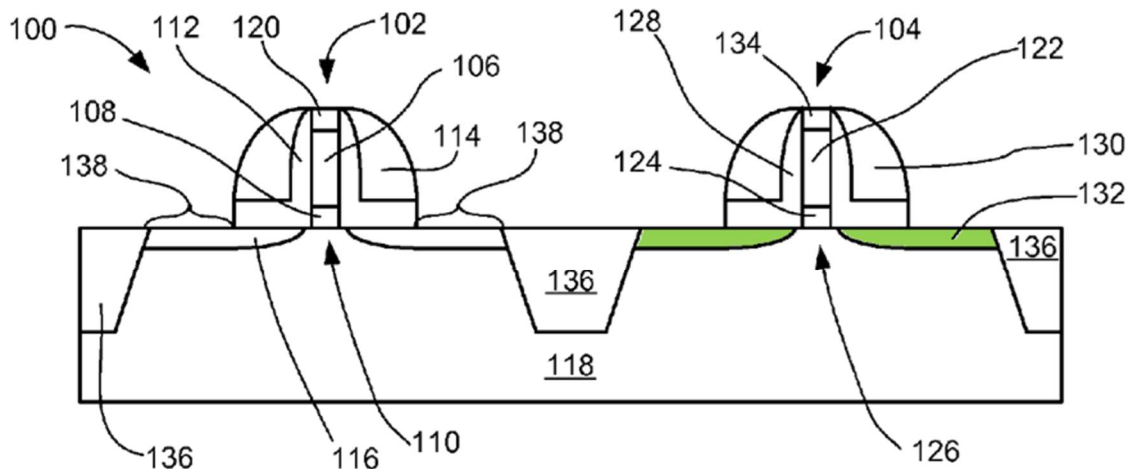


FIG. 1

Chong Fig. 1

145. A POSITA reading Chong would have understood that the source and drain extension (SDE) is a lightly doped drain. Ex-1040 at 1:46-51 (“the source/drain extension (SDE) regions (formerly known as lightly doped drain or LDD regions)”; Ex-1041 at [0017] (“[L]ightly-doped source/drain (LDD) regions 22, also commonly known as source/drain extension (SDE) regions 22, is formed.”); Ex-1034 at 4:14-23, Fig. 1; Ex-1035 at [0021]; Ex-1031 at [0007].

(e) 2[e] “forming at least a recess in the semiconductor substrate adjacent to two sides of the first spacer;”

146. Chong discloses 2[e] because it discloses selectively etching portions of the substrate 118 adjacent to the first liner 128 and spacer 130 (“the first spacer”) for forming recesses 400 in the substrate 118. Ex-1007 at [0038], Fig. 4.

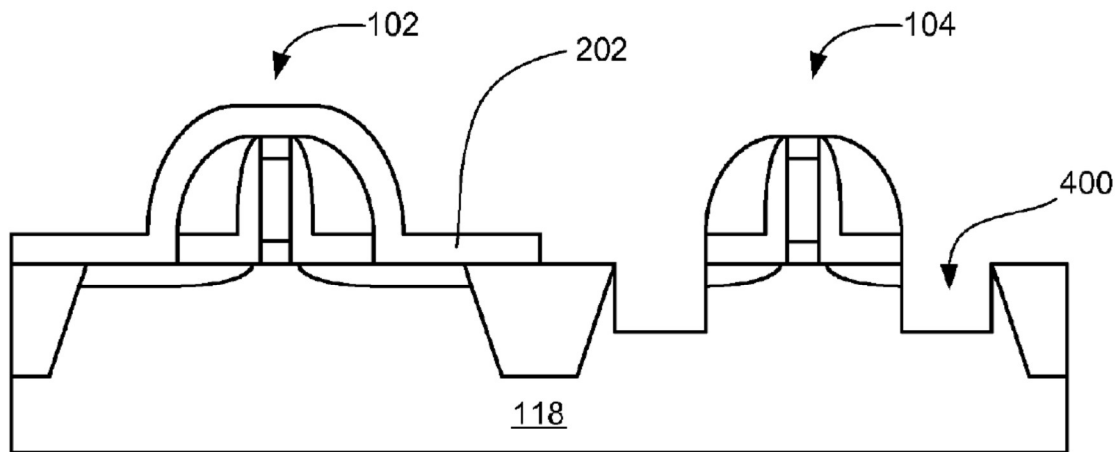


FIG. 4

Chong Fig. 4

(f) 2[f] “forming the epitaxial layer in the recess;”

147. As discussed for 1[d], Chong discloses 2[f] because it discloses forming, within the recesses, a punch-through suppression layer 500 using “epitaxially grown silicon germanium” to induce strain within the PFET channel 126. Ex-1007 at [0040]-[0044]; §IX.B.3(e), *supra*.

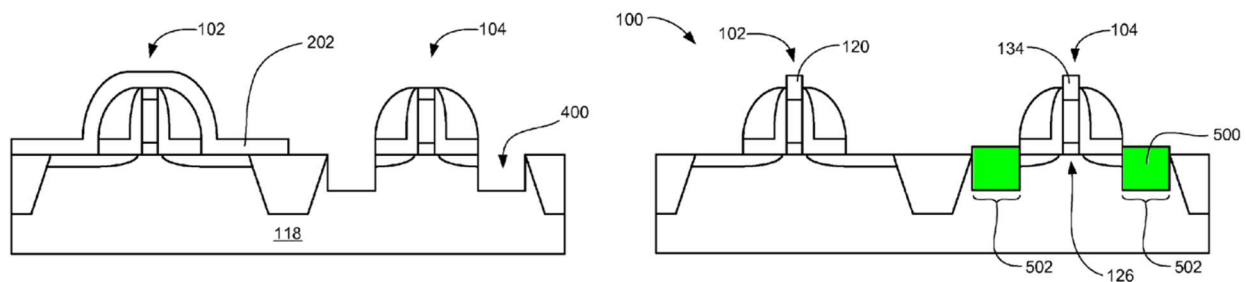


FIG. 4

FIG. 5

Chong, Figs. 4-5

(g) 2[g] “removing the hard mask disposed on the silicon layer;”

148. Chong discloses 2[g] because it discloses removing the PFET cap 134 (the “hard mask,” as discussed in §IX.B.4(a), *supra*). Ex-1007 at [0047] (“The NFET cap 120, of FIG. 5, and the PFET cap 134, of FIG. 5, have been removed”), Fig. 6.

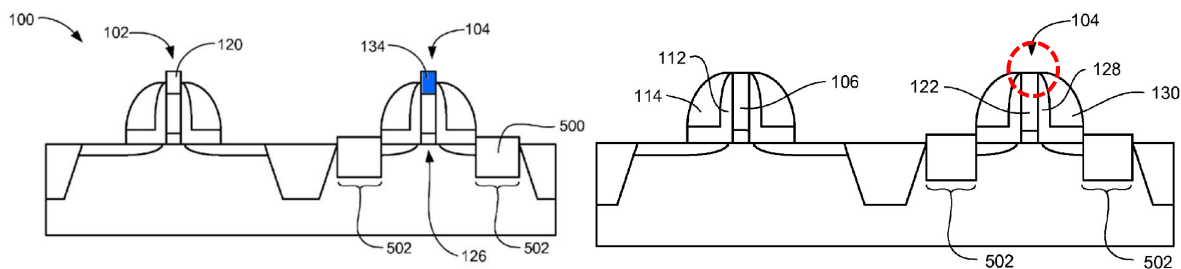


FIG. 5

FIG. 6

Chong, Fig. 5 (with hard mask) and 6 (hard mask removed)

(h) **2[h] “forming a first dielectric layer on the semiconductor substrate while covering the gate pattern;”**

149. Chong discloses 2[h] because it discloses forming a PFET second liner
702 by blanket deposition of “a dielectric material, such as a low temperature oxide”
and a second PFET spacer 706 by a subsequent blanket deposition of “a dielectric
material, such as a nitride.” Ex-1007 at [0049]-[0050], [0052].

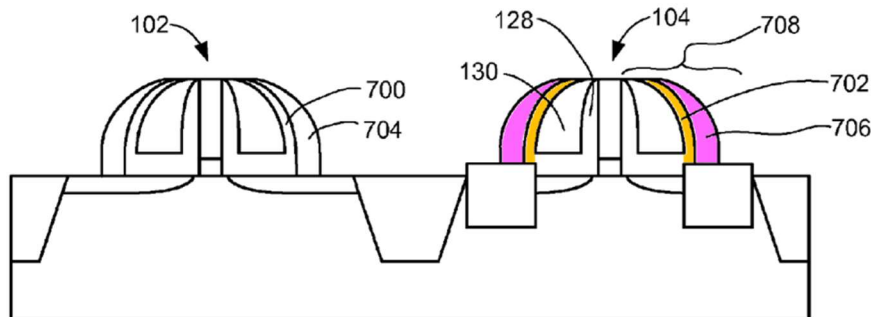


FIG. 7

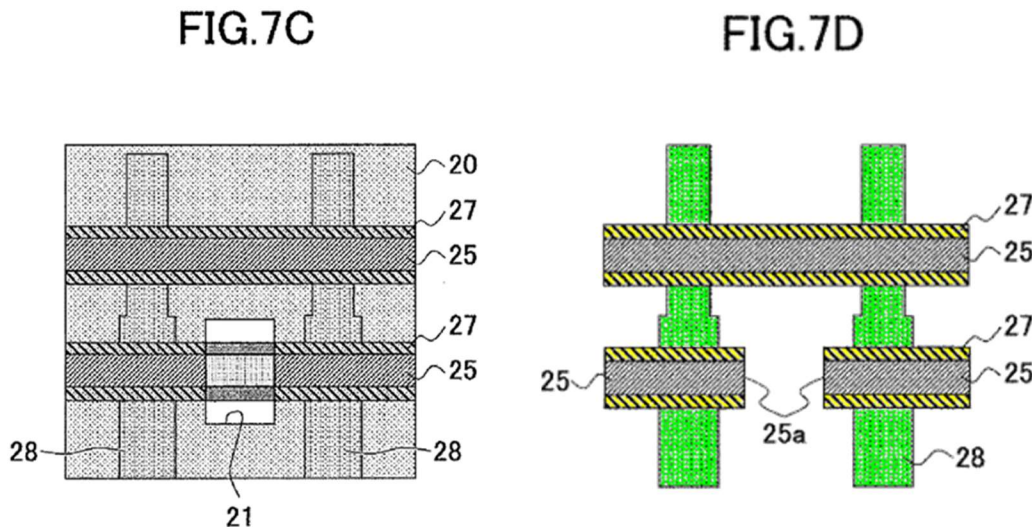
Chong, Fig. 7

150. The deposited liner 702 and spacer 706 may be a dielectric material such as an oxide and nitride, respectively. *Id.* at [0052]. The liner 702 and spacer 706, collectively or individually, are thus a “first dielectric layer.” And because they may be formed over the PFET device 104 “by blanket deposition followed by a subsequent etch back” (*id.* at [0049]-[0050]), the liner 702 and spacer 706 “cover[] the gate pattern,” as claimed.

- (i) 2[i] “performing the second photo-etching process on the gate pattern, the first spacer, and the first dielectric layer to form the slot in the gate pattern; and”

151. Chong as modified by Okuno renders this limitation obvious. As discussed for 1[e], Okuno's gate cutting ("second photo-etching process") is performed to separate the patterned gate strip into individual gates after the source/drain regions are formed. Ex-1004 at [0026], [0034]; §IX.B.3(f), *supra*. Further, as discussed in Section IX.B.2(b), *supra*, and as Okuno teaches, Chong's

gates would be separated at least after the materials for the liner 702 and spacer 706 (the “first dielectric layer”) are deposited (for example, by blanket depositions), so the subsequent etch back to form the differential spacer 708 will leave no spacers on the cut edges, as illustrated in Okuno, Fig. 7D.



Okuno, Figs. 7C-7D

152. Okuno’s second photo-etching process is thus performed on the gate 122 (the “gate pattern”), a first liner 128 and spacer 130 (the “first spacer”), and the liner 702 and spacer 706 (the “first dielectric layer”).

(j) 2[j] “removing a portion of the first dielectric layer for forming a second spacer.”

153. Chong and Okuno render 2[j] obvious. Chong discloses forming each of the **liner 702** and **spacer 706** by “blanket deposition followed by a subsequent etch back” to form a differential spacer 708. Ex-1007 at [0048]-[0049], [0051], Fig. 7.

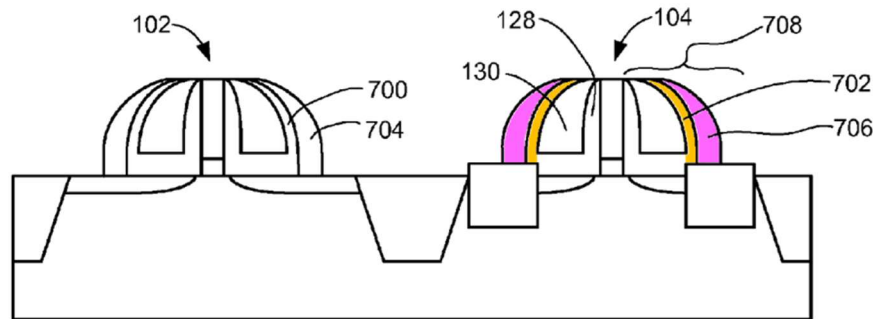


FIG. 7

Chong, Fig. 7

154. Because the “subsequent etch back” process removes at least a portion of liner 702 and spacer 706 for forming a differential spacer 708, Chong discloses “removing a portion of the first dielectric layer for forming a second spacer,” as claimed.

155. Chong-Okuno renders this limitation obvious regardless of whether the “second spacer” is formed before or after the “second photo-etching process” of 2[i]. I have been informed that, as a general rule a method claim is not limited to performance of the steps in the order recited, unless the claim explicitly or implicitly requires a specific order. Here, nothing in the claim requires a second spacer to be formed after the second photo-etching process, and the two steps are not tied together in any way. Accordingly, Chong’s etch back of the dielectric layers to form the second spacer (liner 702 and spacer 706) meets this limitation regardless of its sequence with respect to Okuno’s gate cut process (“second photo-etching process”).

156. Indeed, in the Chong-Okuno combination, Okuno's gate cut ("second photo-etching process") would occur any time after the deposition of the dielectric materials. As Okuno explains, the goal of the gate cut is to ensure any "extending width of [the two spacers for] the pocket implantation and the extension implantation from the [cut-side] gate edges 25a is absent." Ex-1004 at [0041]. Thus, as long as the gate cut occurs after the deposition of the dielectric materials, Okuno's goal would be met, regardless of whether Chong's etch-back of the dielectric materials for forming the second spacer occurs before or after Okuno's gate cut. Either sequence would have been obvious to try. Chong discloses a conventional method (e.g., "reactive ion etch") by which the patterning could be performed. Ex-1007 at [0053]. Forming the second spacer in one of the two available ways, i.e., before or after photoetching, using reactive ion etch would have been the product of ordinary skill and common sense.

157. Should the Board find that the second spacer may be formed before the second photo-etching process, it would have been obvious to form Chong's differential spacers 708 *before* performing Okuno's gate cut process to leave the cut gate edges free of any sidewall spacers. *See* Ex-1004 at Claim 1, [0035], Fig. 7D; *see also id.* [0041] ("the extending width of the pocket implantation and the extension implantation from the gate edges **25a** is absent, the protruding amount obtained after the gate etching process can be reduced.").

FIG.7C

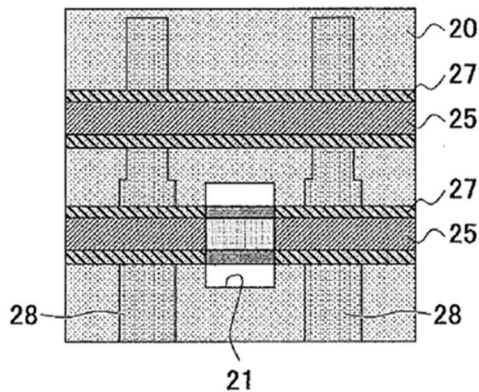
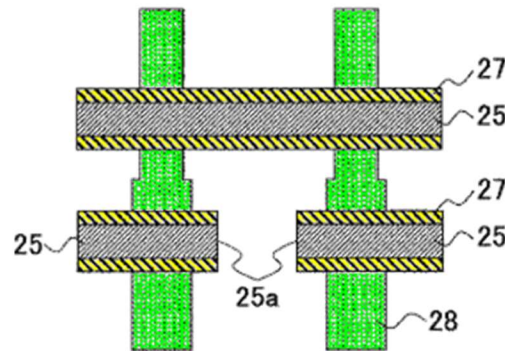


FIG.7D



Okuno, Figs. 7C-7D

158. In this combination, because Chong's differential spacers 708 would first be formed along the gate length direction of the gate, Okuno's gate cut process would cut the gate along with the differential spacers so the differential spacers 708 are "absent from the intervening regions between two opposing driver transistors" and "thus contributing to the size reduction of the cell structure." Ex-1004 at [0028].

159. Alternatively, should the Board find that a second spacer must be formed after the second photo-etching process, Chong-Okuno renders this alternative obvious. Chong discloses that the differential spacers 708 are formed by blanket depositions of a dielectric material (such as an oxide) followed by another dielectric material (such as a nitride). It would have been obvious to use Chong's nitride film "as an etching hard mask before the application of the resist" for Okuno's gate cut. Ex-1004 at [0034]. Under this alternative, a POSITA would have

applied Okuno's resist after Chong's nitride film, as Okuno teaches. Ex-1004 at [0034]. Once the etching is performed to cut the gate, the nitride film would then be removed along with the underlying oxide layer to form Chong's differential spacers 708. Thus, even if Chong's oxide/nitride layers are etched back to form the differential spacers *after* performing Okuno's gate cut process, no spacers would be present in the cut gate edges.

5. **Claim 3. "The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation."**

160. Chong and Okuno render claim 3 obvious. Chong discloses that the semiconductor substrate comprises isolation structure 136, such as a shallow trench isolation (STI). Ex-1007 at [0033]. As shown in Chong's Fig. 1, the devices are isolated from each other by the STIs 136.

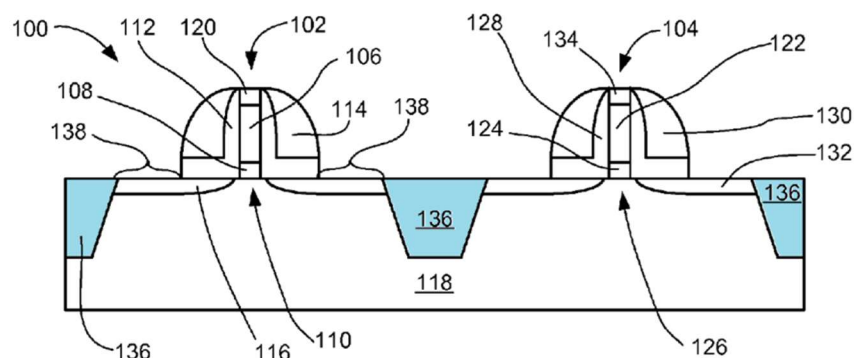
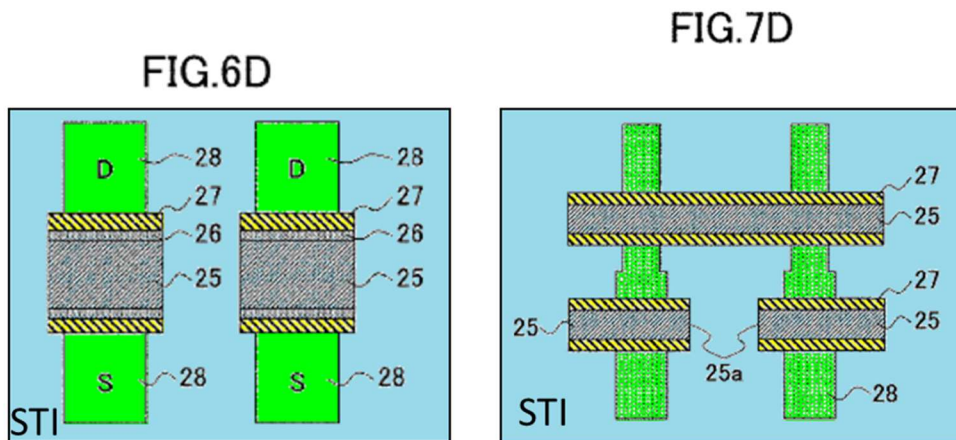


FIG. 1

Chong, Fig. 1

161. Okuno further discloses that “the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation” because Okuno’s second photoetching process etches away the patterned polysilicon and gate oxide. Ex-1004 at [0031], Figs. 6D, 7D; §IX.A.5, *supra*.



Okuno, Figs. 6D and 7D (Modified)

162. A POSITA would have recognized that the second photoetching of Chong-Okuno is done by etching away portions of the gate 122 disposed on the STI structures 136. Indeed, portions of the gate 122 on the STI structures *must* be removed so that two or more separate gates electrically independent from each other, as shown in Okuno’s Figs. 6D and 7D, can be formed. *Id.*

6. Claim 4. “The method of claim 1, wherein the hard mask comprises silicon nitride.”

163. As discussed for 2[a], Chong discloses forming a PFET cap 134 (the “hard mask”) made of material “such as a nitride or an oxynitride cap.” Ex-1007 at [0031], Fig. 3a; §IX.B.4(a), *supra*.

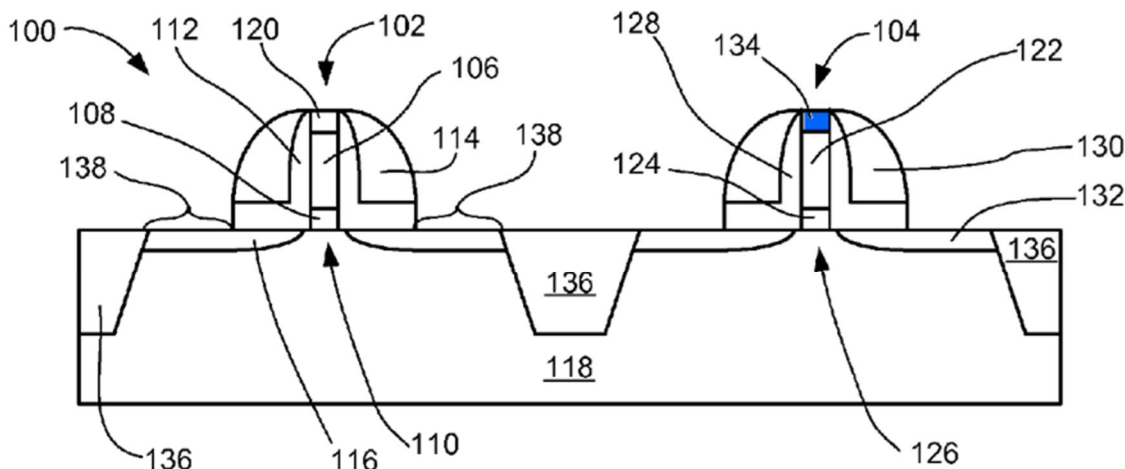
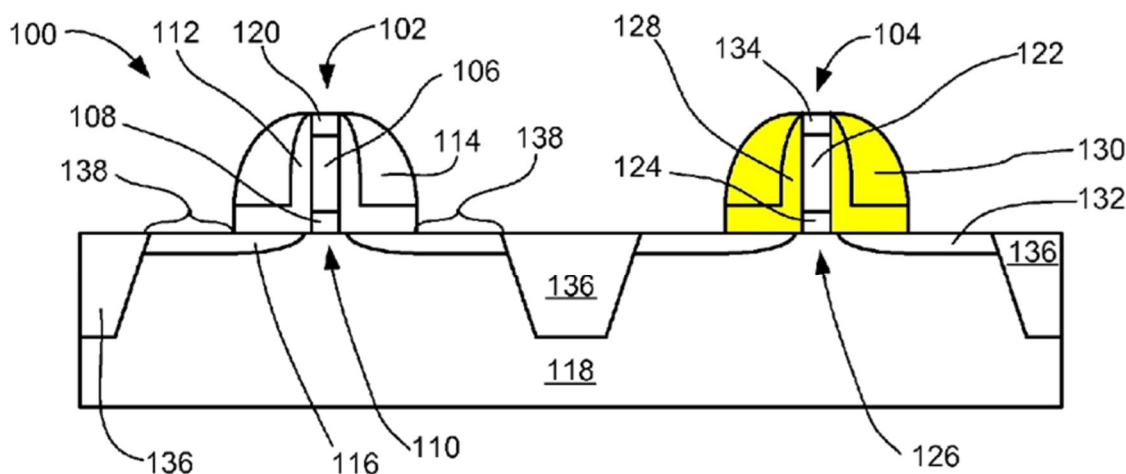


FIG. 1

Chong, Fig. 1

164. A POSITA would recognize the PFET cap 134 comprises silicon nitride. A “nitride” is a compound with the element nitrogen in the -3 oxidation state whereas an “oxide” is a binary compound of oxygen with another element. In semiconductor manufacturing, a POSITA would have understood that the other element of Chong’s “nitride” and “oxide” compounds is silicon. Materials such as silicon nitride (Si_xN_y), silicon oxide (Si_xO_y), and silicon oxynitride (Si_xON_y) are used in semiconductor fabrication for their dielectric properties and are frequently referred to simply as nitride, oxide, and oxynitride, respectively. Ex-1036 at [0024] (forming spacers with “composite oxide/nitride materials,” such as “silicon nitride” and “silicon oxynitride”); Ex-1037 at [0020] (a “nitride film” may include “silicon nitride” or “silicon oxynitride”); Ex-1038 at [0056]. Chong also discloses using a nitride as a dielectric material. Ex-1007 at [0052]. A POSITA would have

7. **Claim 5.** “The method of claim 2, wherein the step of forming the first spacer comprises: forming a silicon oxide layer and a silicon nitride layer on the semiconductor substrate; and etching back the silicon oxide layer and the silicon nitride layer for forming the first spacer”



Chong, Fig. 1

claim 4, a POSITA would have understood that oxygen and nitrogen-containing materials include a “silicon oxide” and “silicon nitride,” respectively. Ex-1001 at 2:39-41; Ex-1036 at [0024]; Ex-1037 at [0020]; Ex-1038 at [0056]; §IX.B.6, *supra*.

8. Claim 6. “The method of claim 2, wherein the first dielectric layer comprises a silicon oxide layer and a silicon nitride layer.”

167. Chong discloses that the liner 702 and spacer 706 (the “first dielectric layer”) may include an “oxide deposited material” and a “nitride,” respectively. Ex-1007 at [0052]. As discussed for claim 4, a POSITA would have understood that “oxide deposited material” and “nitride” (Ex-1007 at [0052]) include “silicon oxide” and “silicon nitride,” respectively. Ex-1001 at 2:39-41; Ex-1036 at [0024]; Ex-1037 at [0020]; Ex-1038 at [0056]; §IX.B.6IX.B.4(a), *supra*. A POSITA would have recognized, or at least find obvious, that the liner 702 and spacer 706 are silicon oxide and silicon nitride, respectively.

9. Claim 7. “The method of claim 2, wherein after performing the second photo-etching process comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.”

168. Chong and Okuno render obvious claim 7. *First*, Chong discloses that “more than two spacers” may be formed in the PFET device other than the liner 702 and spacer 706 (the “first dielectric layer”). Ex-1007 at [0027]. A POSITA would recognize that, to form additional spacers, another dielectric layer (a “second

dielectric layer”) must be deposited and patterned. §IX.B.2(c), *supra*. Chong thus discloses “forming a second dielectric layer on the semiconductor substrate.”

169. *Second*, forming the second dielectric layer “after the second photo-etching process” would have been obvious in view of Okuno, which discloses that, after gate separation, a CVD oxide may be deposited to form thin sidewalls 29 that protect the cut edges 25a from a subsequent silicide process. Ex-1004 at [0036]; §IX.B.2(c), *supra*. Okuno’s thin CVD oxide sidewall spacer is an example of additional spacers contemplated by Chong. Ex-1007 at [0027].

170. *Third*, Chong-Okuno discloses “removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.” As discussed in Section IX.B.2(c), *supra*, in the alternative where Chong’s nitride film is used as a hard mask for the gate cut process, a POSITA would have etched back the second dielectric layer (Okuno’s thin sidewalls 29) with the first dielectric layer (liner 702 and spacer 706) to form the claimed second spacer. §IX.B.2(c), *supra*.

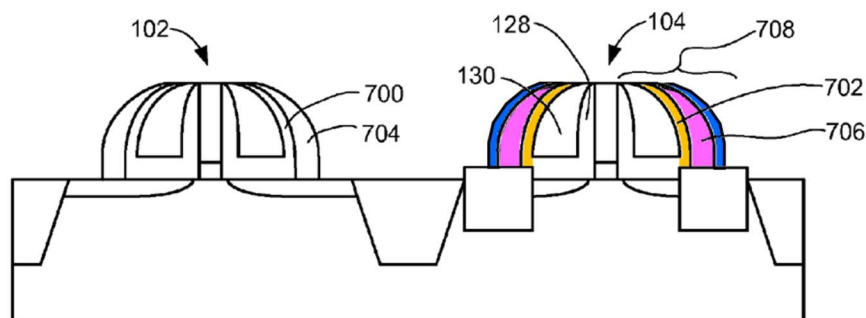
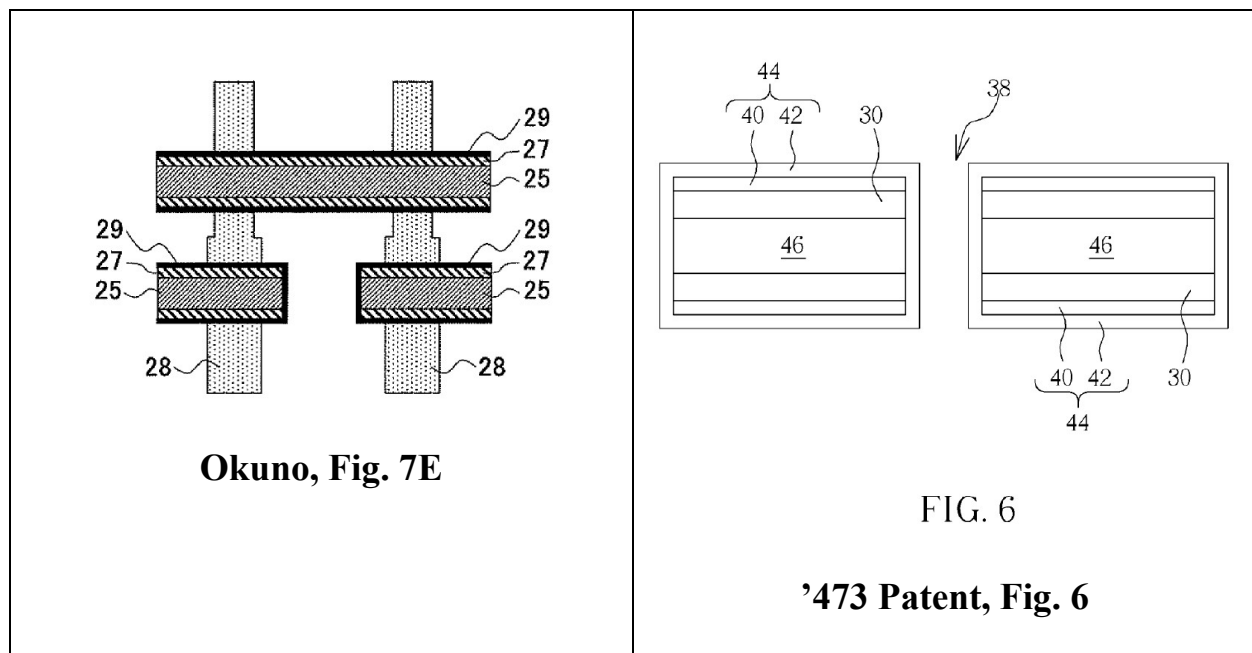


FIG. 7

Chong, Fig. 7 (Modified)

171. Patterning the two dielectric layers together (e.g., Okuno's CVD oxide film with Chong's liner 702 and spacer 706) after gate separation would result in the formation of a "second spacer." §IX.B.2(c).

172. Because a portion of the first dielectric layer (within the cut slot) would have already been removed during Okuno's gate cut, the resulting "second spacer" would have the first dielectric layer (liner 702 and spacer 706) disposed on two opposite sidewall of the gate while the second dielectric layer (Okuno's thin sidewalls 29) would have been formed on four sidewalls of the gate, consistent with the '473 Patent as illustrated by below. *See* '473 Patent, 4:37-55 ("[T]he present invention could also deposit a single silicon oxide layer before the polysilicon slot is formed, and then deposit a silicon nitride layer after the formation of the polysilicon slot to form different MOS transistor structures....").



10. Claim 8. “The method of claim 7, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.”

173. Chong renders claim 8 obvious. In Chong-Okuno, liner 702 and/or spacer 706 (the “first dielectric layer”) are formed before gate separation. Ex-1007 at [0047]; §§IX.B.4(h)-4(i), *supra*. As discussed for claim 6, the liner 702 may include an “oxide deposited material,” which a POSITA would have understood is a silicon oxide. §IX.B.8, *supra*. After the gate separation, as discussed for claim 7, it would have been obvious to form a “second dielectric layer” (e.g., Okuno’s CVD oxide) to protect the cut edges from silicide corrosion. §IX.B.9, *supra*.

174. It would also have been obvious to use a nitride film, in addition to an oxide film, for the “second dielectric layer.” Oxide and nitride have complementary chemical and material properties that allow them both to be used as alternating dielectric layers to protect the gate structures. *Id.* Ex-1039 at [0032]; Ex-1038 at [0056]. Chong similarly discloses using both oxide and nitride films to form spacers. Ex-1007 at [0031] (128 and 130), [0052] (702 and 706). The processes for depositing oxide and nitride films are well known. For example, as Okuno discloses, a POSITA could use CVD (chemical vapor deposition) to deposit both the oxide and nitride films. Ex-1004 at [0035]-[0036]. A POSITA would have understood that using nitride, in addition to oxide, for the second dielectric layer would have been

nothing more than a routine modification that utilizes well-known materials and processes.

11. **Claim 9. “The method of claim 2, wherein after forming the second spacer comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the second dielectric layer for forming a third spacer.”**

175. As discussed for claim 7 (§IX.B.9, *supra*), Chong discloses forming a second dielectric layer from which additional spacers may be formed (Ex-1007 at [0027]), and Okuno provides a specific example of a second dielectric layer, namely a CVD oxide film (Ex-1004 at [0036]. As discussed in Section IX.B.2(c), Okuno discloses patterning an additional dielectric layer (e.g., Okuno’s CVD oxide film) after gate separation, and in the alternative where Chong’s liner 702 and spacer 706 are made into a spacer before gate separation, the liner 702 and spacer 706 would form the “second spacer” while the additional dielectric layer forming a “third spacer” (e.g., Okuno’s thin sidewalls 29).

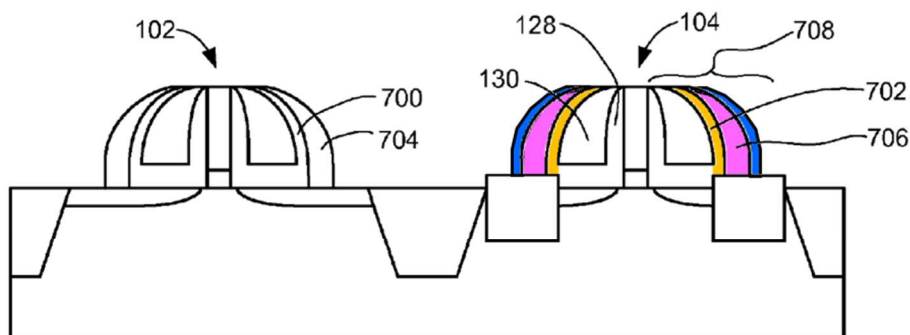
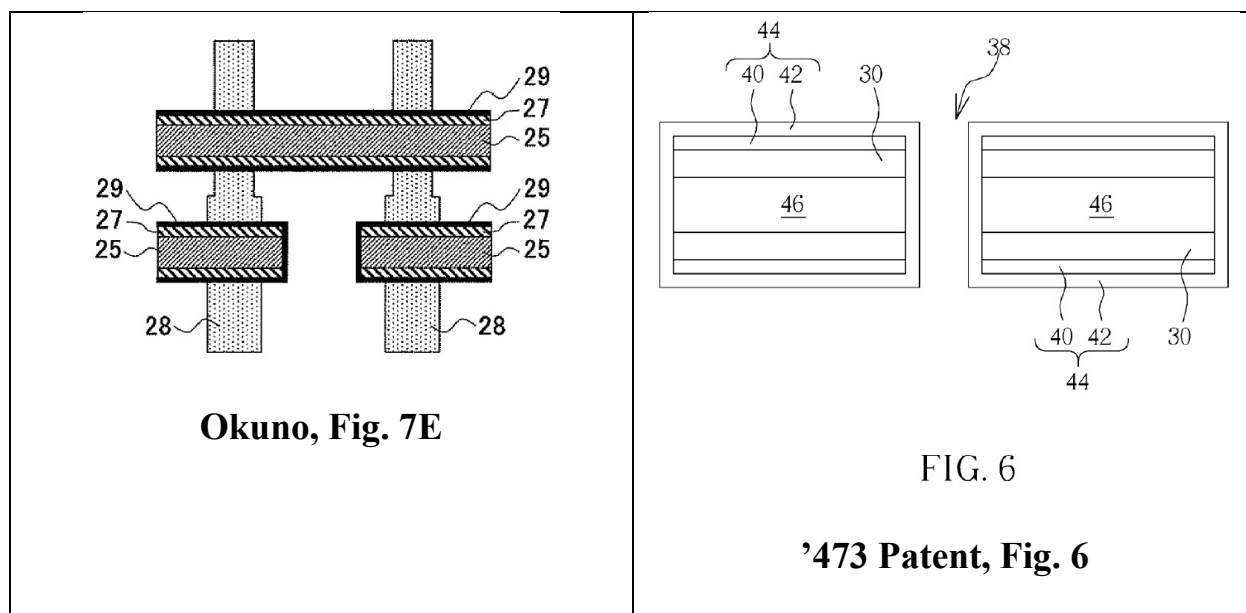


FIG. 7

Chong, Fig. 7 (Modified)

176. Because a portion of the first dielectric layer would have been removed during etch back to form the spacer, the resulting “second spacer” would be the first dielectric layer (liner 702 and spacer 706) disposed on two opposite sidewall of the gate while the “third spacer” would have been Okuno’s thin sidewalls 29 that have been formed on four sidewalls of the gate, consistent with the ’473 Patent as illustrated by below.



See also Ex-1001 at 4:37-55 (“[T]he present invention could also deposit a single silicon oxide layer before the polysilicon slot is formed, and then deposit a silicon nitride layer after the formation of the polysilicon slot to form different MOS transistor structures....”).

12. **Claim 10. “The method of claim 9, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.”**

177. Chong renders claim 10 obvious. Chong discloses that liner 702 (the

“first dielectric layer”) may include an oxide deposited material such as silicon dioxide. Ex-1007 at [0052]. As discussed with respect to claim 8, it would have been obvious to form the “second dielectric layer” by depositing and patterning both silicon oxide and silicon nitride layers after gate separation. *See* §IX.B.10, *supra*.

C. Ground 3: Claims 1-3 are Obvious Over Mandelman and Shin

1. Overview of Mandelman (Ex-1005)

178. Mandelman discloses the structure and fabrication of MOS transistors, such as those used in the memory cells of an SRAM device. Mandelman notes that a “continuing objective of SRAM device designers is to more densely pack SRAM memory cells into a smaller integrated circuit,” and smaller geometries (e.g., below the 45 nm node) place “ever-greater demands on the photolithography techniques.” Ex-1005 at [0006]-[0010].

179. In Mandelman, the substrate includes a bulk substrate 11 and STIs 20 formed to isolate active semiconductor regions from each other. *Id.* at [0029], Fig. 5B. A gate dielectric layer 22 is formed on a top surface of the active semiconductor regions 14. *Id.* **Conductor lines** (e.g., 40) are defined by a conventional photolithography and etching process. *Id.* at [0031], Fig. 2. Spacers (e.g., 50, 52) are formed on the sidewalls of conductor line 40 by etching layers of silicon nitride and silicon dioxide. *Id.* at [0033]. And source/drain regions are formed by an ion implantation process. *Id.* at [0034].



180. Subsequently, a second photolithography process is performed with a photoresist layer 60 to expose portions of the conductor lines 36, 38, and 40 and underlying gate dielectric layer 22. *Id.* at [0036]-[0038], Fig. 3. As a result, segmented conductor lines are created, such as segment 40a having vertical surface on sidewall 78 overlying the active semiconductor region 16. *Id.* at [0038]-[0039], Fig. 4.



Mandelman, Figs. 3-4

2. Combining Mandelman and Shin

181. Mandelman and Shin disclose similar MOS transistors fabricated on a bulk substrate. Ex-1005 at [0002]; Ex-1006 at [0005]. Like Shin (*see* §IX.A.3), Mandelman also discloses conventional elements of a MOS transistor such as STI and spacers. Ex-1005 at [0029], [0033]. Further, both Mandelman and Shin seek to solve problems related to miniaturization of transistors. Specifically, Mandelman seeks to provide an improved photolithography process that meet the demands of smaller geometries (e.g., below the 45 nm node) (Ex-1005 at [0006]-[0010]), and Shin seeks to overcome the short channel effect by forming epitaxial source/drain regions (Ex-1006 at [0005]-[0006]).

182. A POSITA would have found it obvious to fabricate Mandelman's transistors using epitaxial source/drain regions, as Shin teaches, to add advantageous strain. Ex-1005 at [0034]; Ex-1006 at [0084]; Ex-1031 at [0021]-[0026]; Ex-1033 at [0044]. An epitaxial source/drain would introduce compressive (or tensile stress) in the source/drain well areas and increase carrier mobility of Mandelman's device. Ex-1030, 1:20-34, 3:43-52, 4:19-33; Ex-1006 at [0084]; Ex-1031 at [0010]; §VI.C. Using epitaxial source/drain would enable Mandelman's device to have shorter channel length and higher drive current and, thereby, further Mandelman's goal of increasing transistor density.

183. A POSITA would have had a reasonable expectation of success. Shin's

SEG process would have been simply added after Mandelman's spacer formation for source/drain formation. Ex-1006 at [0038], [0090]; Ex-1005 at [0033]-[0034]. After growing an epitaxial layer in the recesses, a POSITA would have proceeded with the remaining steps taught by Mandelman, such as segmenting of the conductor lines using a second photoetching process. Ex-1005 at [0070]-[0071].

184. A POSITA would have viewed this as an obvious example of (1) implementing a known technique (forming source/drain regions mainly through selective epitaxial growth and/or ion implantation) to improve known devices (MOS devices) to achieve predictable results (introducing mechanical stresses into the channel region to improve carrier mobility and overcoming the short channel effect); (2) a choice from a finite number of identified, predictable solutions (epitaxially growing source/drain regions); and (3) a teaching, suggestion, or motivation in the prior art (*see* Ex-1006 at [0084]) that would have led a POSITA to modify Mandelman's MOS transistor to include epitaxially grown source/drain regions, as Shin teaches, to arrive at the claimed invention.

3. Claim 1

(a) 1[pre]: "A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:"

185. To the extent the preamble is limiting, Mandelman discloses a method for fabricating a metal-oxide semiconductor (MOS) transistor. *See* Ex-1005 at [0002] ("The invention generally to integrated circuit fabrication and, in particular,

to a design structure for the memory cells of an SRAM device.”). A conventional SRAM memory cell, for example, consists of six MOS transistors. *Id.* at [0005] at [0069].

186. Mandelman, for example, discloses MOS transistor 28, 32, and 34, each comprising a conductor line 40, gate dielectric layer 22, and active semiconductor region 14. Ex-1005 at [0030]-[0031], Figs. 4, 5B.

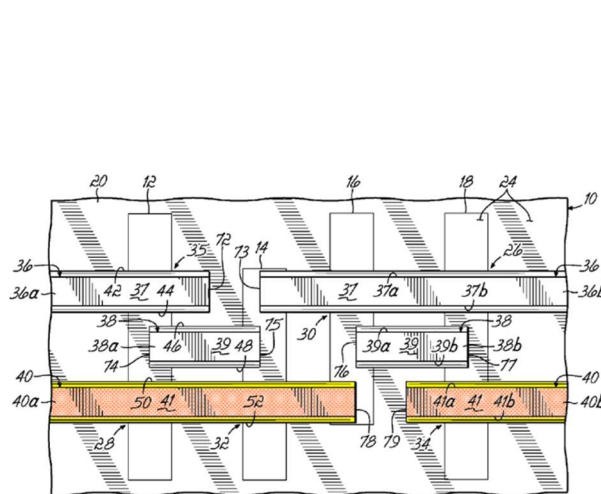


FIG. 4

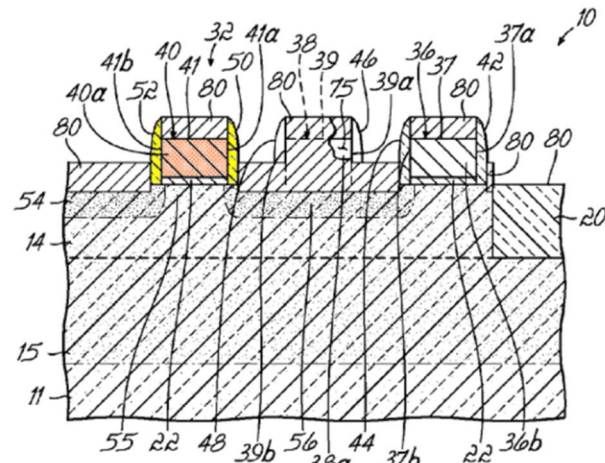
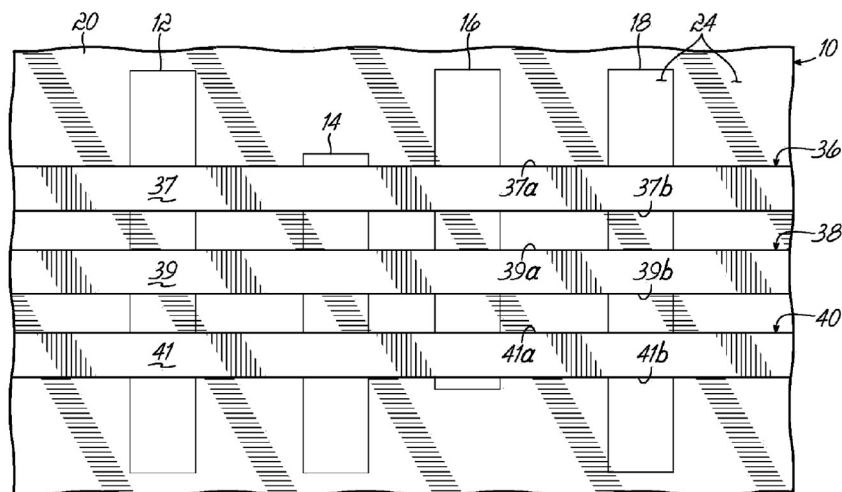


FIG. 5B

Mandelman, Figs. 4 and 5B

(b) 1[a]: “providing a semiconductor substrate;”

187. Mandelman discloses 1[a] by providing a semiconductor substrate 10. Ex-1005 at [0027] (“The substrate 10 and active semiconductor regions 12, 14, 16, 18 are formed from a silicon-containing semiconductor material that primarily contains silicon.”); Ex-1001, 2:35-37.



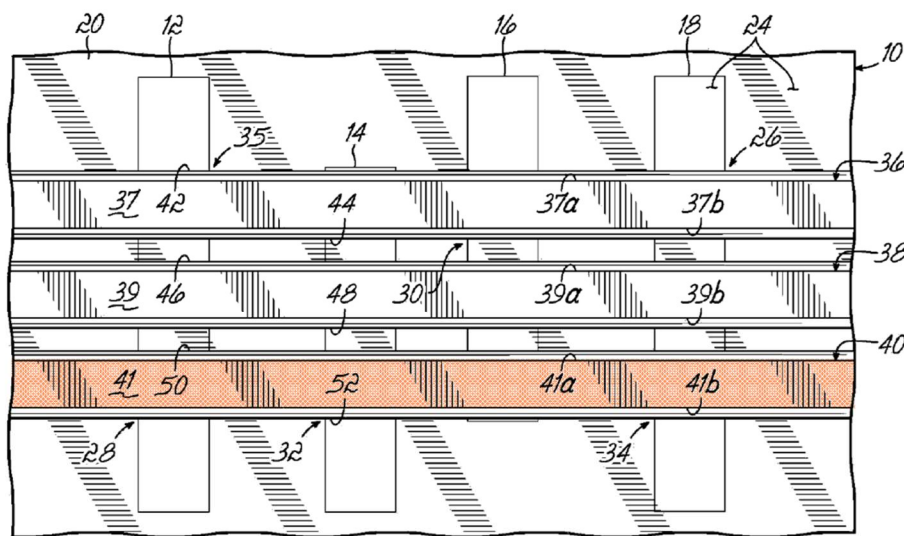
Mandelman, Fig. 1

(c) 1[b]: “forming a silicon layer on the semiconductor substrate;”

188. Mandelman discloses 1[b] by depositing conductive material on the semiconductor substrate 10. Ex-1005 at [0031]. Mandelman’s conductive material is a “silicon-containing semiconductor material that primarily contains silicon, such as doped polycrystalline silicon (i.e., doped polysilicon),” consistent with the ’473 patent. *Id.*; Ex-1001, 2:42-47, 2:55-61.

(d) 1[c]: “performing a first photo-etching process on the silicon layer for forming a gate pattern;”

189. Mandelman discloses this limitation because it discloses performing “a conventional photolithography and etching process” (the “first photo-etching process”) to form **conductor line 40** (the “gate pattern”). Ex-1005 at [0031]. Mandelman discloses forming the **conductor lines 40** by depositing conductive



Mandelman, Fig. 2

190. As discussed in Section IX.D.1(a), *supra*, it would have been obvious to add an epitaxial layer to Mandelman's device. Mandelman discloses forming source/drain regions 54 and 56 adjacent two sides of the conductor line 40. Ex-1005 at [0033]-[0034], Figs. 2, 5B.

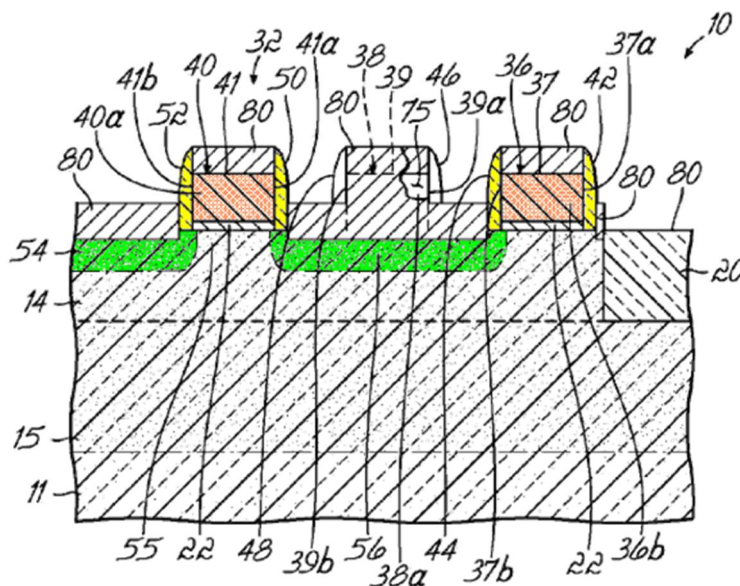


FIG. 5B

Mandelman Fig. 5B

191. In Mandelman-Shin, an epitaxial layer would be formed in the semiconductor region 110 adjacent to the two sides of the conductor line 40, as Shin teaches. §IX.D.1(a), *supra*.

- (f) 1[e]: “after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.”

192. After the spacers 50 and 52 and source/drain regions are formed, Mandelman discloses performing a second photolithography and etching process on the conductor lines (“gate pattern”). Ex-1005 at [0036]-[0038]. A photoresist layer 60 is applied to the substrate 10, and openings are printed using a “conventional photolithography process.” *Id.* at [0036], Fig. 3. The exposed portions are then

etched. *Id.* at [0037], Fig. 4.

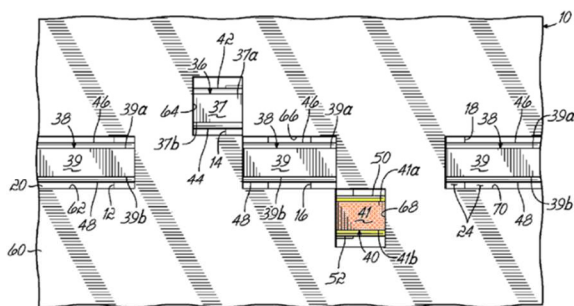


FIG. 3

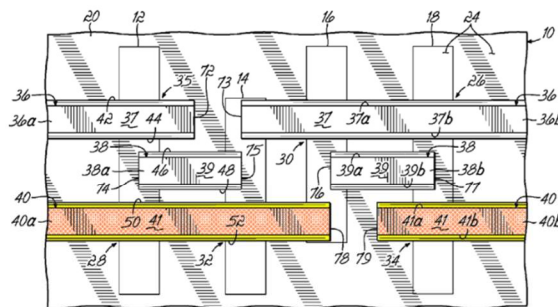


FIG. 4

Mandelman, Figs. 3-4

193. Because Mandelman discloses performing the second photoetching process after the source and drain regions are formed, in Mandelman-Shin, the second photoetching process would be performed after the formation of the epitaxial layer (which occurred during the source/drain formation). *See* §IX.C.3(e), *supra*.

194. Mandelman's photoetching process is performed "while using the gate pattern to physically separate the gate pattern into two gates" because it segments the conductor line 40 into segments 40a and 40b. *Id.* (Segment 40a constitutes gate of transistors 28 and 32 while segment 40b constitutes gate of transistor 34.). Lastly, as shown in Fig. 4, each of the cut portions between the segmented conductor lines "form a slot in the gate pattern."

- 4. Claim 3. “The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.”**

195. Mandelman-Shin renders claim 3 obvious. Mandelman discloses the additional limitations of claim 3. Mandelman discloses that the semiconductor substrate 10 comprises shallow trench isolation regions 20. Ex-1005 at [0029] (“A gate dielectric layer 22 (FIG. 5B) is formed on a top surface 24 shared by the active semiconductor regions 12, 14, 16, 18 and shallow trench isolation regions 20.”).

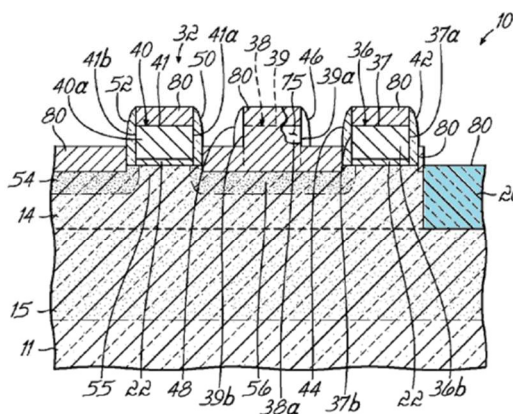


FIG. 5B

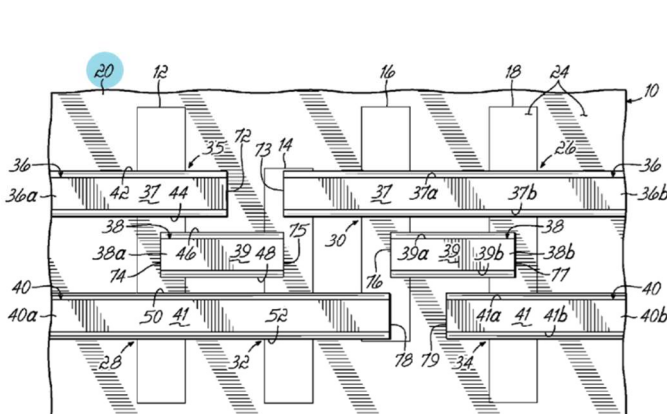


FIG. 4

Mandelman, Figs. 5A-B and 4

196. Mandelman also discloses that its second photoetching process segments the conductor line 40 into multiple segments (40a and 40b) by removing portions of the conductor line 40 and exposing the underlying shallow trench isolation regions 20. Ex-1005 at [0037]-[0038].

D. Ground 4: Claims 1-6 are Obvious Over Chong and Mandelman

1. Combining Chong and Mandelman

(a) A gate-cutting process to separate Chong's gate structures for miniaturization

197. Chong and Mandelman disclose similar MOS transistors fabricated on a bulk substrate. Ex-1005 at [0002]; Ex-1007 at [0003], [0009], [0026]. Both disclose MOS transistors fabricated on a bulk substrate. Ex-1005 at [0002]; Ex-1007 at [0003], [0009], [0026]. Both disclose common elements of a MOS transistors, including an STI and spacers. Ex-1005 at [0029], [0033]; Ex-1007 at [0033], [0031]. Further, Chong and Mandelman seek to solve problems related to miniaturization of transistors. Mandelman noting that demands on “size reduction” and limitations with “conventional photolithography techniques” (Ex-1005 at [0008], [0010]) result in a “significant density penalty,” provides an improved photolithography process that meets the demands of smaller geometries (e.g., below the 45 nm node). Ex-1005 at [0006]-[0010]. Chong seeks to mitigate unintended strain effects caused by size reduction. Ex-1007 at [0004].

198. A POSITA would have found it obvious to photoetch and separate Chong's gate pattern into two gates, as disclosed by Mandelman (*see* §IX.C.3(d), *supra*), after the formation of the epitaxial layer to reduce spacing between transistors and achieve size reduction by overcoming the limits of photolithography. Ex-1004 at [0032]; Ex-1005 at [0036], [0038], Figs. 3-4; Ex-1026 at 5:1-35;

Ex-1012 at [0025]-[0026]; §VI.E. A POSITA would have understood from prior training that there are only finite options for patterning gates: patterning individual gate separately or cutting a single patterned gate strip into multiple gates. As such, a POSITA would have recognized that performing gate cutting would enable Chong's device to scale down further while maintaining control over the strain effects.

199. Performing the second photoetching process *after* the formation of epitaxially grown source/drain regions would also have been obvious. The '473 Patent admits both techniques (epitaxial layer formation and gate separation) were known (Ex-1001 at 1:28-42), and prior art expressly motivates separating the gate pattern after forming the epitaxial layer. Mandelman discloses performing the second photoetch process after forming source/drain regions. Ex-1005, [0033]-[0034] (forming source/drain regions 50 and 52 adjacent two sides of the conductor line 40), [0036]-[0037] (photoetch to cut the conductor line 40), Figs. 2, 5B.

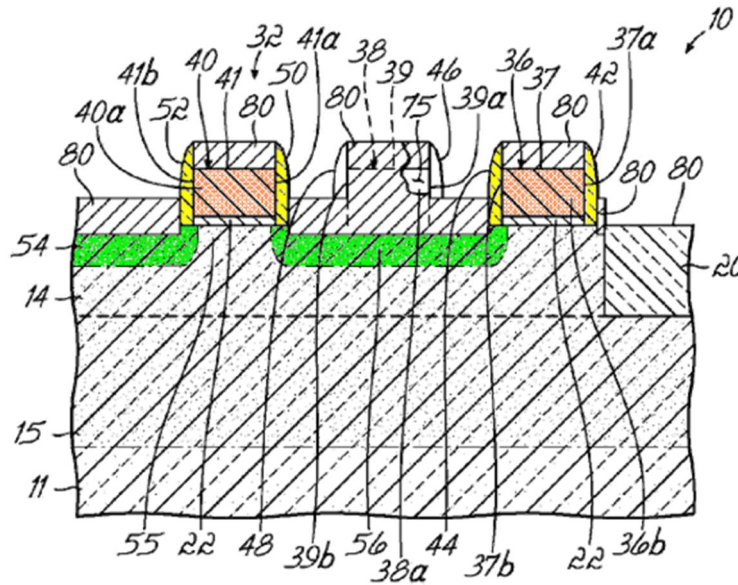


FIG. 5B

Mandelman Fig. 5B

200. Performing gate separation last is consistent with and supplements Chong's disclosures. Chong discloses forming an epitaxial layer early in the fabrication process by in-situ doping: before removing the hard mask 13, adjusting the source/drain concentration with ion implantation, and forming dielectric layers (liner 702 and spacer 706). Ex-1007 at [0044], [0047]-[0049], [0058]. If any of the steps for forming the source/drain regions (e.g., growing epitaxial layer and dopant implantation) is performed after the gate separation, it will cause the impurity characteristics below the gate electrode end portions to become asymmetrical, which a POSITA would have known to avoid. Ex-1004 at [0027]. A POSITA would thus be motivated to perform Mandelman's second photoetching process after the completion of Chong's earlier steps, including the formation of the epitaxial layer.

201. A POSITA would have had a reasonable expectation of success in adding a second photoetching step to Chong's fabrication method. Mandelman discloses that gate separation can be done using a well-known technique, including a "conventional photolithography process" and anisotropic dry etching process such as RIE. Ex-1005 at [0036]-[0037], Fig. 3. It would have been well within a POSITA's expertise to use a conventional photoetch technique such as RIE (reactive ion etching) to separate the gate structures. Ex-1001, 1:28-42. Separating the gates after an epitaxial layer is formed would have predictably improved the fabrication process by preventing impurities at the gate ends. Ex-1007 at [0044]; *see* Ex-1004 at [0027]; §VI.F.

202. A POSITA would have viewed this as an obvious example of (1) implementing a known technique (gate-cutting, through photoetching including the step such as RIE, after source/drain formation) to improve known devices (MOS devices) to achieve predictable results (reduced transistor spacing, size reduction, and symmetrical impurity characteristics); (2) a choice from a finite number of identified, predictable solutions (cutting a single patterned gate into multiple gates or patterning individual gate separately); and (3) a teaching, suggestion, or motivation in the prior art (*see* Ex-1005 at [0036]-[0037]) that would have led a POSITA to modify Chong's MOS transistor with Mandelman's gate separation, to arrive at the claimed invention.

(b) Gate separation after a dielectric layer is formed on the gate, leaving the cut edges free of the dielectric layer

203. When combining Mandelman’s gate separation step with Chong, a POSITA would have been motivated to sequence the gate separation so that the cut edges are free of dielectric materials (the liner 702 and spacer 706). Mandelman expressly motivates leaving no dielectric spacers on the cut edges, such that sidewall spacers are not formed on the “transverse edges or ends defining sidewalls 72-79.” Ex-1005 at [0039], [0046], Fig. 4. The direct contact establishes “electrically connective bridges,” which help simplify contacts and cell layouts. *Id.* at [0045].

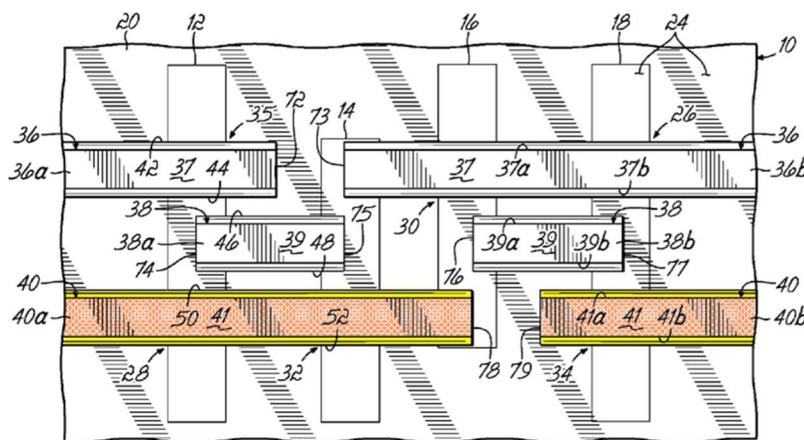


FIG. 4

Mandelman, Fig. 4

204. When combining Mandelman and Chong, if Chong's liner 702 and spacer 706 are formed after the second photoetching process, the two dielectric layers would cover the transverse edges, which is contrary to Mandelman's explicit teaching. Thus, consistent with Mandelman's disclosures, a POSITA would have

formed the liner 702 and spacer 706 on Chong's PFET gate 122 before performing the second photoetching process. *Id.*

205. Performing the gate separation after the formation of the liner 702 and spacer 706 would have yielded predictable benefits. Chong discloses implanting impurities in the NFET source/drain 900 after the formation of the liner 702 and spacer 706 and protecting the PFET with a mask 904 during this implant step. Ex-1007 at [0057], Fig. 9. In view of Mandelman's teaching, a POSITA would have understood that performing gate separation last (i.e., after the formation of the liner 702 and spacer 706 and the NFET source/drain implant step) would further protect Chong's NFET device 102 from the source/drain implant step and increase the symmetry of the impurity characteristics, result in stable operating characteristics.

206. The size reduction benefit of leaving no spacers on the cut edges further supports that it was obvious to separate the gates after the liner 702 and spacer 706 are formed. Chong, like Mandelman, seeks achieve "[s]ize reduction." Ex-1007 at [0004]; Ex-1005 at [0006]. Cutting the gates after the liner 702 and spacer 706 are formed would leave no spacers on the cut edges, allowing the gates to be packed more closely together and enable size reduction.

2. Claim 1

(a) 1[pre]–[d]

207. Chong discloses 1[pre] through 1[d] as discussed for Ground 2.

§IX.C.3(a)–C.3(e), *supra*.

- (b) 1[e]: “after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.”

208. Chong-Mandelman renders 1[e] obvious. In Chong-Mandelman, after epitaxially growing a punch-through suppression layer 500 (Ex-1007 at [0040]-[0044]) and after the NFET source/drain implant is complete (*id.* [0055]-[0057]), a second photoetching would be performed using a photoresist layer to separate the gates, as Mandelman teaches. Ex-1005 at [0038]; §IX.D.1(a). The photoetching process would segment the PFET gate 122 into multiple segments, like Mandelman’s segments 40a and 40b. *Id.* The exposed portions are then etched, forming a slot (e.g., between sidewalls 78 and 79) in the gate pattern. *Id.* at [0038], Fig. 4.

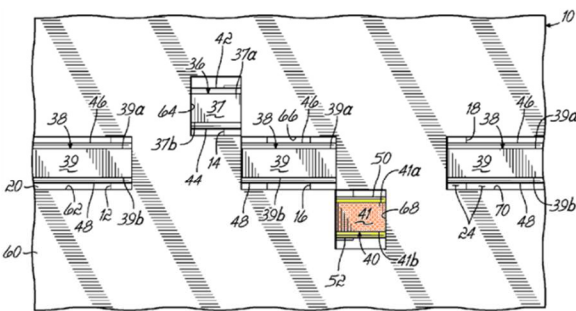


FIG. 3

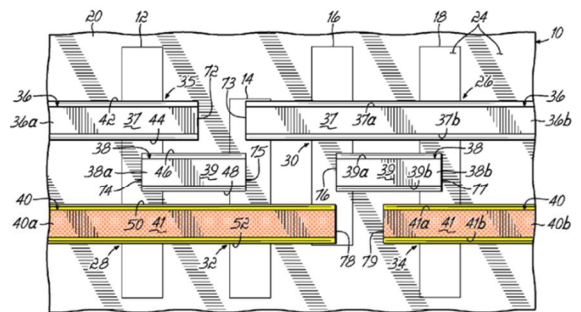


FIG. 4

Mandelman, Figs. 3-4

3. Claim 2. “The method of claim 1, wherein after forming the silicon layer comprises:”

209. Chong-Mandelman renders claim 2 obvious by performing the following steps after forming the silicon layer.

(a) 2[a]-[h]

210. Chong discloses 2[a] through 2[h] as discussed for Ground 2. §IX.B.4(a)–B.4(h), *supra*.

(b) 2[i] “performing the second photo-etching process on the gate pattern, the first spacer, and the first dielectric layer to form the slot in the gate pattern; and”

211. Chong and Mandelman render 2[i] obvious. As discussed for 1[e], Mandelman’s gate cutting (“second photoetching process”) is performed to separate the patterned gate into individual gates after a punch-through suppression layer 500 is epitaxially grown. Ex-1005 at [0038], [0070]–[0071], Fig. 16; §IX.D.2(b), *supra*. Further, as discussed in Section IX.D.1(b), *supra*, and as Mandelman teaches, Chong’s gates would be separated at least after the materials for the liner 702 and spacer 706 (the “first dielectric layer”) are deposited (for example, by blanket deposition), so the subsequent etch back to form the differential spacer 708 will leave no spacers on the cut edges, as illustrated in Mandelman’s Figures 15-16.

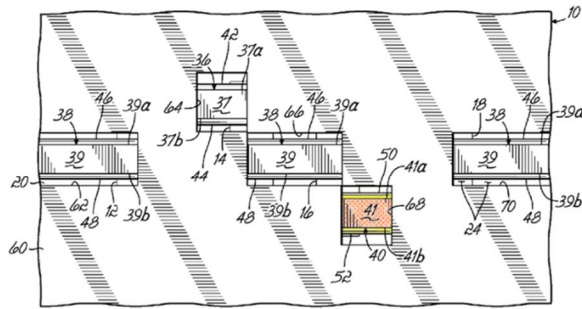


FIG. 3

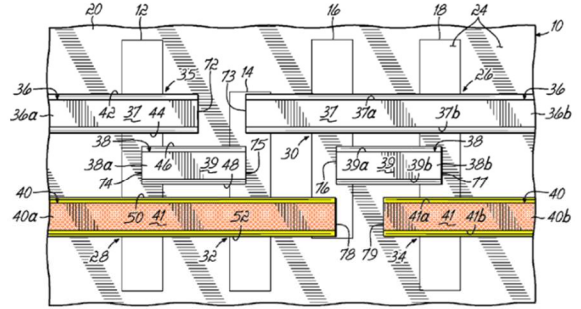


FIG. 4

Mandelman, Figs. 3-4

212. Mandelman's second photo-etching process is thus performed on the gate 122 (which forms the "gate pattern"), a first liner 128 and spacer 130 (the "first spacer"), and the liner 702 and spacer 706 (the "first dielectric layer").

(c) 2[j] "removing a portion of the first dielectric layer for forming a second spacer."

213. Chong in view of Mandelman renders this limitation obvious. As explained in §IX.B.4(h), Chong discloses forming each of the **liner 702** and **spacer 706** by "blanket deposition followed by a subsequent etch back" to remove at least a portion of liner 702 and spacer 706 ("first dielectric layer") to form a differential spacer 708 ("a second spacer"), as claimed. Ex-1007 at [0048], Fig. 7.

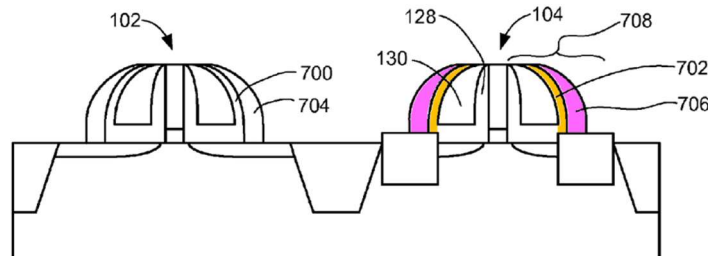


FIG. 7

Chong, Fig. 7

214. Chong-Mandelman renders this limitation obvious regardless of whether the “second spacer” is formed before or after the “second photo-etching process” of 2[i]. Here, nothing in the claim requires a second spacer to be formed after the second photo-etching process, and the two steps are not tied together in any way. Accordingly, Chong’s patterning of the layers 702 and 706 (the “first dielectric layer”) to form the second spacer meets this limitation regardless of its sequence with respect to Mandelman’s gate cut process (“second photoetching process”).

215. Indeed, in the Chong-Mandelman combination, Mandelman’s gate cut (“second photo-etching process”) would occur any time after the deposition of the dielectric materials. As Mandelman explains, the goal of the gate cut is to expose the sidewalls 72-79 so they are in “direct physical contact” with a silicide layer “without any intervening structures, such as a spacer.” Ex-1007 at [0038]-[0039], [0046]. The direct contact establishes “electrically connective bridges,” which help simplify contacts and cell layouts. *Id.* at [0045]. Thus, as long as the gate cut occurs after the deposition of the dielectric materials, the goal would be met, regardless of whether Chong’s etch-back of the dielectric materials for forming the second spacer occurs before or after Mandelman’s gate cut. Either sequence would have been obvious to try. Chong discloses a conventional method (e.g., “reactive ion etch”) by which the patterning could be performed. Ex-1007 at [0053]. Forming the second spacer in one of the two available ways, i.e., before or after photoetching, using any

of the known patterning techniques would have been the product of ordinary skill and common sense.

216. Should the Board find that the second spacer may be formed before the second photo-etching process, Chong in view of Mandelman renders obvious forming Chong's differential spacers 708 *before* performing Mandelman's gate cut process to leave the cut gate edges without any sidewall spacers. See Ex-1005, [0046]-[0048], Figs. 3-4.

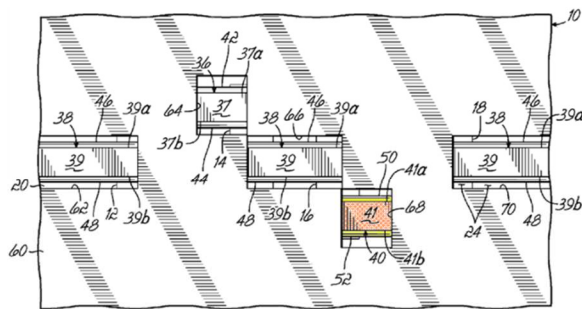


FIG. 3

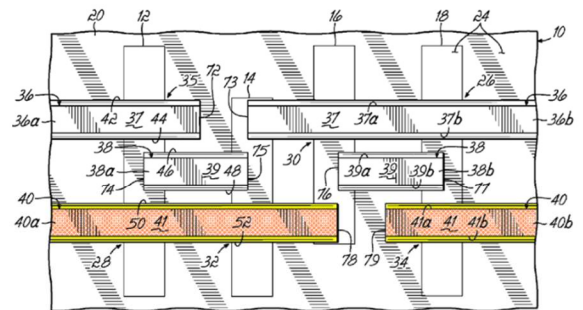


FIG. 4

Mandelman, Figs. 3-4

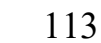
217. In this combination, Chong's differential spacers 708 would first be formed along the gate length direction of the gate, and Mandelman's gate cut process would cut the gate with the differential spacers so the differential spacers 708 are not formed on "vertical surfaces" where direct contact with a silicide layer is intended. Ex-1005 at [0046]-[0048].

218. Alternatively, should the Board find that a second spacer must be formed after the second photo-etching process, Chong-Mandelman renders this

alternative obvious. Chong discloses that the differential spacers 708 are formed by blanket depositions of a dielectric material (such as an oxide) followed by another dielectric material (such as a nitride). It would have been obvious to utilize Chong's nitride film as an "etch mask" during an "anisotropic dry etching process" for Mandelman's gate cut. Ex-1007 at [0031], [0036]. Once the etching is performed to cut the gate, the nitride film would then be removed along with the underlying oxide layer to form Chong's differential spacers 708. Thus, even if Chong's oxide/nitride layers are etched back to form the differential spacers *after* performing Mandelman's gate cut process, spacers would not be present in the cut gate edges.

4. Claim 3. "The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation."

219. Chong-Mandelman renders claim 3 obvious. Chong discloses that the semiconductor substrate comprises [isolation structure 136](#) and that the isolation structure 136 is a shallow trench isolation (STI). Ex-1007 at [0033]. As shown in Chong's Fig. 1, the PFET device 104 and NFET devices 102 are isolated from each other by the STI 136.



Chong, Fig. 1

113

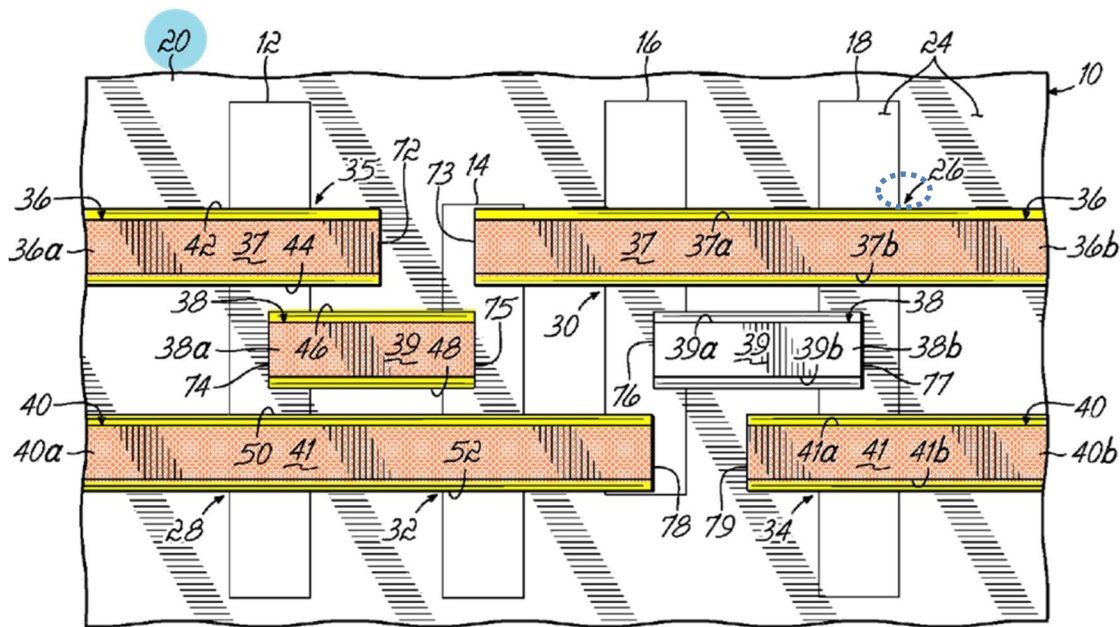


FIG. 4

Mandelman, Fig. 4

221. A POSITA would have recognized that the second photoetching of Chong-Mandelman is done by etching away portions of the gate 122 disposed on the STI structures 136. Indeed, portions of the gate 122 on the STI structures *must* be removed so that two or more separate gates electrically independent from each other, as shown in Mandelman's Fig. 4, can be formed. *Id.*

5. Claims 4-6

222. Chong discloses or renders obvious claims 4-6 as discussed for Ground 2. §IX.B.6–B.8, *supra*.

X. CONCLUSION

223. As discussed above, it is my opinion that the Challenged Claims of the

'473 Patent are unpatentable because they are anticipated by the prior art, because they would have been obvious to a person of ordinary skill in view of the prior art, or both.

224. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested proceeding before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the proceeding and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

225. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner raises and to account for new information as it becomes available to me.

226. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 17th day of April 2025, in FL.

By: _____

Dr. Eugene Fitzgerald, Ph.D.

Appendix A

Exhibit No.	Description
Ex-1001	U.S. Patent No. 9,093,473 (“’473 Patent”)
Ex-1002	Prosecution History for U.S. Patent No. 9,093,473 (“File History”)
Ex-1004	U.S. Patent Publication No. 2009/0309141 (“Okuno”)
Ex-1005	U.S. Patent Publication No. 2008/0251878 (“Mandelman”)
Ex-1006	U.S. Patent Publication No. 2006/0088968 (“Shin”)
Ex-1007	U.S. Patent Publication No. 2008/0142879 (“Chong”)
Ex-1008	S.M. Sze, <i>Physics of Semiconductor Devices</i> . (2d ed. 1981) (excerpted) (“Sze”)
Ex-1009	J.D. Plummer et al., <i>Silicon VLSI Technology: Fundamentals, Practice and Modeling</i> (2000) (excerpted) (“Plummer”)
Ex-1010	Excerpts from C.Y. Chang & S.M Sze, <i>ULSI Technology</i> (1996) “Chang/Sze”
Ex-1011	U.S. Patent Publication No. 2006/0118878 (“Huang”)
Ex-1012	U.S. Patent Publication No. 2010/0159685 (“Chuang”)
Ex-1013	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 1: Process Technology</i> , 2 nd Ed. (2000) (“Wolf1”)
Ex-1014	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 2: Process Integration</i> (1990) (“Wolf2”)
Ex-1015	Excerpts from S. Wolf, <i>Silicon Processing for the VLSI Era, Vol. 3: The Submicron MOSFET</i> (1995) (“Wolf3”)
Ex-1016	M. Quirk & J. Serda, <i>Semiconductor Manufacturing Technology</i> , Ch. 12: Metallization (2001) (excerpted) (“Quirk”)

Exhibit No.	Description
Ex-1017	S.E. Thompson et al., “A 90-nm Logic Technology Featuring Strained-Silicon,” IEEE Transactions on Electron Devices, vol. 51. No. 11, pp. 1790-97 (Nov. 2004) (“Thompson2004”)
Ex-1018	U.S. Pat. Pub. No. 2006/0148151 (“Murthy151”)
Ex-1019	D. James, “2004 – The Year of 90-nm: A Review of 90 nm Devices,” 2005 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp. 72-76 (2005) (“James”)
Ex-1020	U.S. Patent Publication No. 2006/0292783 (“Lee783”)
Ex-1021	U.S. Patent Publication No. 2008/0157119 (“Tsai”)
Ex-1022	U.S. Patent Publication No. 2006/0115949 (“Zhang”)
Ex-1023	U.S. Patent Publication No. 2004/0262683 (“Bohr”)
Ex-1024	B. J. Ginsberg, J. Burghartz, G. B. Bronner and S. R. Mader, “Selective epitaxial growth of silicon and some potential applications,” in IBM Journal of Research and Development, vol. 34, no. 6, pp. 816-827, Nov. 1990 (“Ginsberg”)
Ex-1025	P. Bai et al., “A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57 μm^2 SRAM Cell,” Technical Digest of the 2004 IEEE International Electron Devices Meeting (IEDM), pp. 657-60 (Dec. 2004) (“Bai”)
Ex-1026	U.S. Patent No. 6,287,904 (“Lee”)
Ex-1027	U.S. Patent Publication No. 2003/0124847 (“Houston”)
Ex-1028	U.S. Patent Publication No. 2009/0023258 (“Liang”)
Ex-1029	U.S. Patent Publication No. 2009/0176069 (“Yang”)
Ex-1030	U.S. Patent No. 6,605,498 (“Murthy”)

Exhibit No.	Description
Ex-1031	U.S. Patent Publication No. 2008/0199999 (“Weijtmans”)
Ex-1032	U.S. Patent Publication No. 2008/0128746 (“Wang”)
Ex-1033	U.S. Patent Publication No. 2005/0112817 (“Cheng”)
Ex-1034	U.S. Patent No. 6,137,126 (“Avanzino”)
Ex-1035	U.S. Patent Publication No. 2007/0284615 (“Ku”)
Ex-1036	U.S. Patent Publication No. 2005/0260806 (“Chang”)
Ex-1037	U.S. Patent Publication No. 2006/0223255 (“Chen”)
Ex-1038	U.S. Patent Publication No. 2004/0253776 (“Hoffman”)
Ex-1039	U.S. Patent Publication No. 2006/0172556 (“Bather”)
Ex-1040	U.S. Patent No. 6,727,558 (“Duane”)
Ex-1041	U.S. Patent Publication No. 2011/0039390 (“Nieh”)

Appendix B

Claim	Limitation
1[pre]	A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:
1[a]	providing a semiconductor substrate;
1[b]	forming a silicon layer on the semiconductor substrate;
1[c]	performing a first photo-etching process on the silicon layer for forming a gate pattern;
1[d]	forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and
1[e]	after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.
2	The method of claim 1, wherein after forming the silicon layer comprises:
2[a]	forming a hard mask on the silicon layer;
2[b]	performing the first photo-etching process on the hard mask and the silicon layer for forming the gate pattern;
2[c]	forming a first spacer around the gate pattern;
2[d]	forming a lightly doped drain in the semiconductor substrate adjacent to two sides of the gate pattern;
2[e]	forming at least a recess in the semiconductor substrate adjacent to two sides of the first spacer;
2[f]	forming the epitaxial layer in the recess;
2[g]	removing the hard mask disposed on the silicon layer;

Claim	Limitation
2[h]	forming a first dielectric layer on the semiconductor substrate while covering the gate pattern;
2[i]	performing the second photo-etching process on the gate pattern, the first spacer, and the first dielectric layer to form the slot in the gate pattern; and
2[j]	removing a portion of the first dielectric layer for forming a second spacer.
3	The method of claim 1, wherein the semiconductor substrate comprises at least a shallow trench isolation, and the step of forming the slot in the gate pattern further comprises removing the silicon layer disposed on the shallow trench isolation.
4	The method of claim 1, wherein the hard mask comprises silicon nitride.
5	The method of claim 2, wherein the step of forming the first spacer comprises: forming a silicon oxide layer and a silicon nitride layer on the semiconductor substrate; and etching back the silicon oxide layer and the silicon nitride layer for forming the first spacer.
6	The method of claim 2, wherein the first dielectric layer comprises a silicon oxide layer and a silicon nitride layer.
7	The method of claim 2, wherein after performing the second photo-etching process comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the first dielectric layer and the second dielectric layer for forming the second spacer.
8	The method of claim 7, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

Claim	Limitation
9	The method of claim 2, wherein after forming the second spacer comprises: forming a second dielectric layer on the semiconductor substrate; and removing a portion of the second dielectric layer for forming a third spacer.
10	The method of claim 9, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

Appendix C

EUGENE FITZGERALD

Massachusetts Institute of Technology

Department of Materials Science
and Engineering, Cambridge, MA 02138

Email : eafitz@mit.edu

Education and Training

M.I.T.	Materials Science and Engineering	B.S., 1985
Cornell University	Materials Science and Engineering	M.S., 1987
Cornell University	Materials Science and Engineering	Ph.D, 1988

Research and Professional Experience

Current Position: MIT	Merton C. Flemings-SMA Chair Professor of Materials Engineering	2003-present
MIT SMART Singapore-MIT Alliance for Research and Technology, MIT's Research Center in Singapore)	Chief Executive Officer	2019-2024
MIT SMART Low Energy Electronic Systems	Lead Principal Investigator	2012-2024
Nanyang Technological University EEE	Visiting Professor	2014-2020
Cornell University Johnson School of Management	Visiting Professor of Management	2006-2014
Massachusetts Institute of Technology, Department of Materials Science and Engineering	Professor	2000-present
Massachusetts Institute of Technology, Department of Materials Science and Engineering	Associate Professor	1994-2000
AT&T Bell Laboratories	Research Scientist	1988-1994

Areas of Research Experience and Expertise:

Semiconductor Materials, Processes, and Devices; III-V (compound) Semiconductors (GaAs, InP, GaN, etc.); IV Semiconductors (Si, Ge, Sn, C); Heteroepitaxy; III-V/Si heteroepitaxy; defects in lattice-mismatched films; III-V devices (LEDs, HEMTs, etc); IV (Silicon, Germanium) devices (detectors, MOSFETs, etc); solar cell devices; integrated circuits; water purification, materials and processes; innovation processes; commercialization and entrepreneurship; serial innovator and entrepreneur

Expert Witness/Legal Technical Consultant Experience:

Time Frame: June 2013 – December 2016

Firm: Kramer Levins (2013-2014), Finnegan (2014-mid 2015), Vasquez Benisek & Lindgren (mid 2015-December 2015) NOTE: each firm retained me as the same case approached trial over three years

Client: Initial: Seoul Semiconductor; Final: Everlight Electronics Co., LTD et al (Defendant)

Adverse: Boston University

Venue: District Court of Massachusetts - Boston

Role as Expert Witness : **trial testimony**, deposition, expert reports, declarations

Comment: Expert witness testimony was key for invalidating BU patent asserted against Client (Defendant). Federal Appeals Court decision.

Time Frame: July 2015 – 2016

Firm: Steptoe and Johnson

Client: Raytheon

Adverse: Sony

Venue: Patent Trial and Appeal Board (IPR)

Role as Expert Witness : deposition (2), expert reports, declarations (2)

Time Frame: September 2016 – July 2017

Firm: Covington and Burling

Client: Samsung

Adverse: Lexington

Venue:

Role as Expert Witness : expert reports

Time Frame: March 2018 – February 2019

Firm: Dentons (Defendant)

Client: Rayvio

Adverse: Seoul Semiconductor

Venue: IPR

Role as Expert Witness : expert reports, deposition

Comment: Expert witness reports and **testimony key for invalidating patent** asserted on Client (Defendant)

Time Frame: Nov 2018 – October 2019

Firm: Ropes and Gray

Client: IQE

Adverse: Solar Junction Corporation

Venue: New York Arbitration, NYC

Role as Expert Witness: expert reports, expert witness in Trade Secret arbitration trial

Comment: Expert witness **trial testimony key in very favorable outcome** for client (Defendant)

Time Frame: November 2017 – 2023

Firm: Wilson Sonsini

Client: Epistar
Adverse: Lowe's Company and Home Centers
Venue: LA District Court (trial late 2020)
Role as Expert Witness: expert reports, depositions (infringement and invalidity; 5 patents, two days of depositions with two different adverse firms), trial expert witness.
Comment: Expert witness **testimony at trial was key in very favorable outcome** for client (Plaintiff)

(note: due to change in law and timing with Covid, there was an **additional trial** in LA court focused on damages only. I testified as the Plaintiff expert witness again, and won max damages).

Time Frame: Jan 2022 – present
Firm: Kramer Levins
Client: Rohm
Adverse: Maxpower
Venue: JAMS, San Francisco
Role as Expert Witness: expert reports, expert witness in IP/licensing arbitration trial
Comment: Arbitration held December 2022 (Defendant). Expert witness **testimony at trial was key to Defense win.**

Technology Transition and Company Formation:

Co-Founder and Chairman, New Silicon Corporation (nsc) Pte. Ltd., Singapore (2016-present): a fabless integrated circuit company with proprietary out-sourced fabrication technology based on III-V devices incorporated into silicon manufacturing processes
Co-Founder and Chairman, AmberWave Systems Corporation (1998-2004): Invented, commercialized, and properly anticipated introduction of strained silicon technology by silicon CMOS industry. Pioneered AmberWave's internal IP group and process for creating IP-base for licensing. Intel licensed AmberWave's technology in 2007, and TSMC later purchased IP portfolio.
Founder and LLC Member-Manager, Paradigm Research LLC (2005-present): Implementation of profitable global out-sourced research model to exploit disequilibrium in current technology supply chain; developed first III-V-Si CMOS IC in partnership with Raytheon
Co-Founder and LLC Member-Manager, 4Power LLC (2005-present): A disruptive business model for high-end solar cells, based on a novel III-V/Si technology which allows for unprecedented efficiency and low weight at low cost
Co-Founder and Executive Director, Innovation Interface (2008-2014): a novel corporate-university interface for innovation production and learning
Founding Team and Principal, The Water Initiative (2007-2017): innovation in point-of-use water purification systems; sold and deployed >100,000 systems in central valley of Mexico

Synergistic Activities and Awards (Highlights)

- *2016 Cornell Distinguished Alumni Award, Department of Materials Science and Engineering
- *2011 IEEE Andrew S. Grove Award (outstanding contributions to solid-state devices and technology): specifically, "For seminal contributions to the demonstration of Si/Ge lattice mismatch strain engineering for enhanced carrier transport properties in MOSFET devices"

- *IEEE 2004 EDS George Smith Award
- *Member, MIT President's Committee on "The Future of MIT Education", 2013
- *Member, MIT President's Committee on "The Innovation Initiative", 2013
- *Chair, External Advisory Board, Institute for Materials Research, Ohio State University (present)
- *Founding Faculty Team creating MIT's Innovation and Entrepreneurship Minor (2016)
Launched first core class "Venture Engineering" for the new MIT I&E minor. Course is bridging the gap between MIT's Sloan School of Management and MIT's Engineering School to deliver broad problem-solving skills (including forming new organizations) to engineers
- *Member of start-up team that developed highly successful Advanced Materials program in the Singapore-MIT Alliance, 1998-2009
- *MITx/edX 3.086 Innovation and Commercialization
First innovation class on MITx launched in fall of 2013. Recognized as a factor which can aid US innovation and economic growth by the White House, Executive Branch, US Government
- *Developed Master of Engineering Degree, DMSE MIT. Interdisciplinary engineering degree, adding emphasis on non-technical aspects of technology evolution and development; also became dual-degree program in Singapore-MIT Alliance 2
- *Created 3.207 Technology Development and Evaluation (circa 2001). Led MIT students and Singaporean students located in Singapore (real-time distance education technology) through the analysis of technology, potential applications, intellectual property, and business models for embryonic technology
- *Robert Lansing Hardy Medal (promising young scientist), TMS, 1994

Books

E.A. Fitzgerald, A. Wankerl, C. Schramm, *Inside Real Innovation* (World Scientific, Singapore), 2011. (multiple printings)

Publications and Patents

More than 500 published technical articles

More than 100 patents issued

>990 publications and patents in Google Scholar

More than 38,000 citations

Hindex=102

<https://scholar.google.com/citations?user=YsZ6EjkAAAAJ&hl=en>